Formal Sign-off with Formal Coverage

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Agenda

- Sign-off
- Coverage
  - Simulation coverage
  - Formal coverage
- End-to-End Formal Verification
- Sign-off with Coverage
- Use on the ARM® Next-Generation CPU Design

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Sign-off

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Sign-offs

- What does sign-off mean to program managers?
  - Ready for tape-out
- Sign-off requires
  - Commitment to finish – else task is optional, and may be killed
  - Metrics to measure progress
  - Nightly/weekly regression runs
- Common sign-off flows
  - Static timing
  - Simulation (spreadsheet and coverage)
  - Power
  - RTL-vs-gates LEC

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What Do We Mean by Formal Sign-off

- When formal is done, no bug is left behind
- In addition to Formal Sign-off methodology, we also need:
  - Commitment & accountability
    - For chosen design blocks, formal is the only technology used for functional verification, replacing not supplementing simulation
    - Cannot tapeout until formal is done
  - Metrics to measure progress
    - Manager's dashboard – coverage, bug rate, run time
    - Progress tracker through weighed run-status transition graph
  - Weekly/nightly regression runs
    - Setup, once formal testbench matures, to easily catch bugs due to RTL changes

Formal Sign-off Can Offer More Confidence Than Simulation Sign-off!

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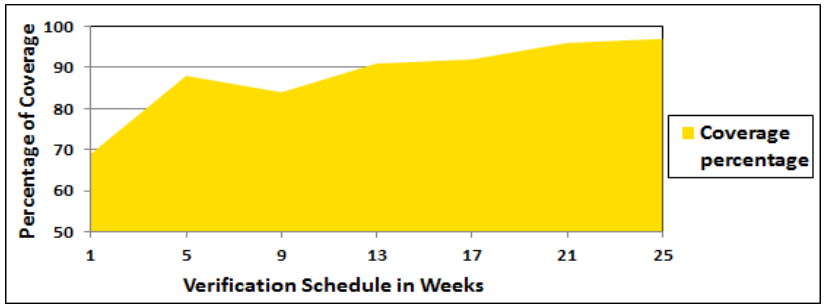
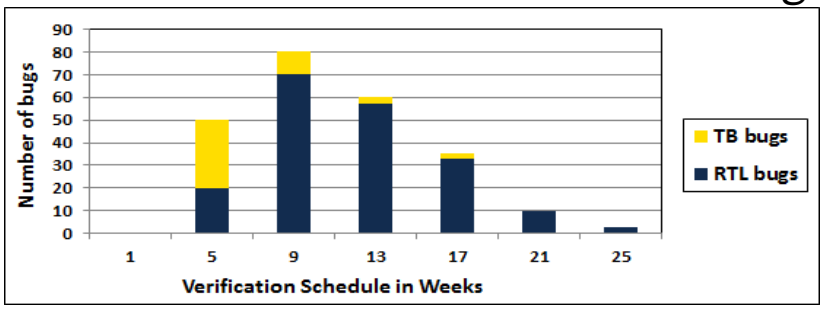
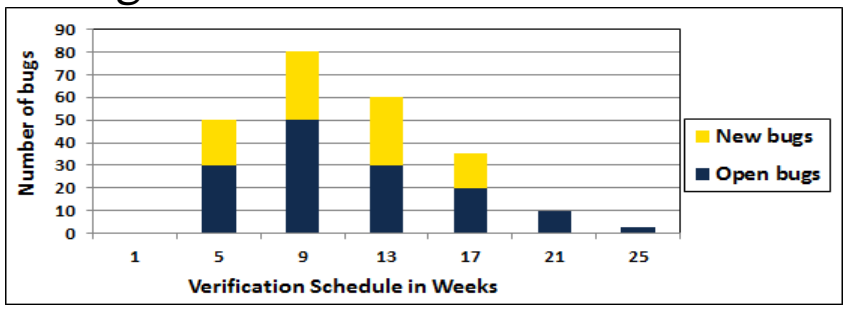
Tracking Progress Is Important for Verification Sign-off

Coverage tracking

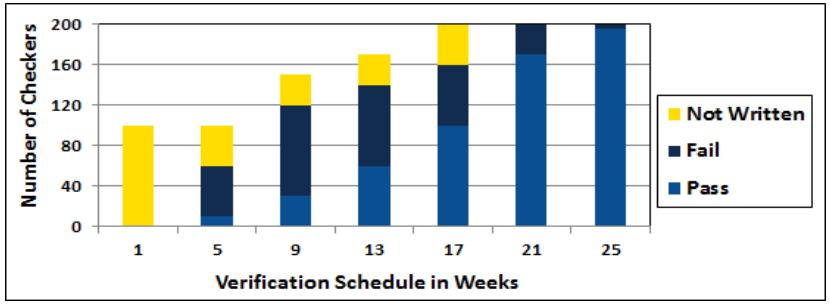


Bug tracking





Runtime status



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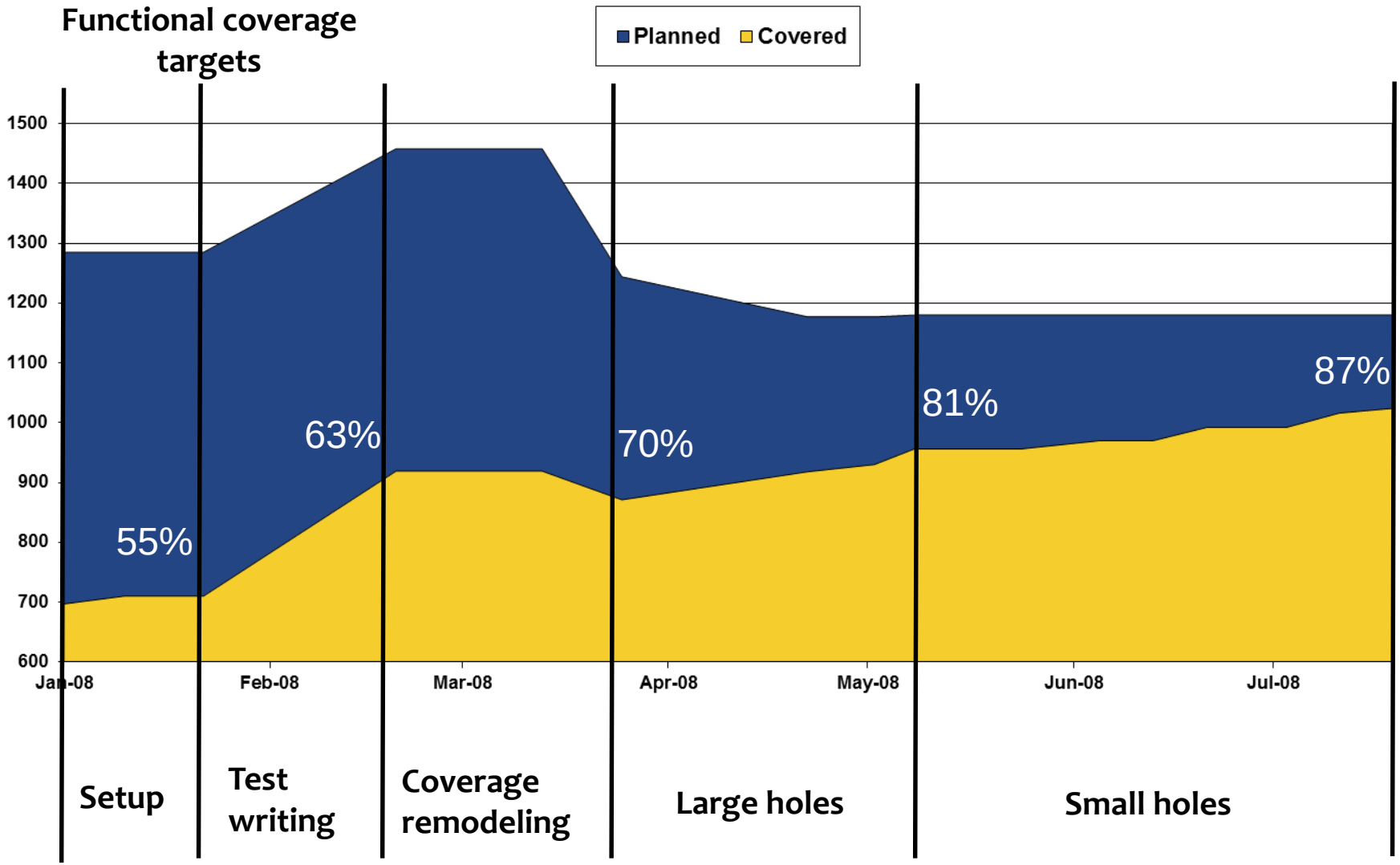
Coverage Closure Is an Important Sign-off Item



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But Coverage Is Not the Be-all and End-all

"The perfect is the enemy of good"

-Voltaire (1772)

- Coverage is not perfect
  - Bugs are missed even with 100% coverage
- But…
  - Helps measure progress
  - Helps identify blind-spots

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How to Pick the Right Formal Metrics?

- To track progress, an ideal metric answers:
  - How much of the design and what is being verified?
    - Quantifies work done so far
  - How much of the design and what is not being verified?
    - Quantifies work left to do

- To indicate sign-off, an ideal metric answers:
  - Checkers: is my list of checkers complete?
  - Constraints: have I over-constrained the testbench to disallow legal stimuli?
  - Complexity: is my achieved proof depth sufficient?

We will use Formal Coverage to quantify each of the three questions

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Coverage

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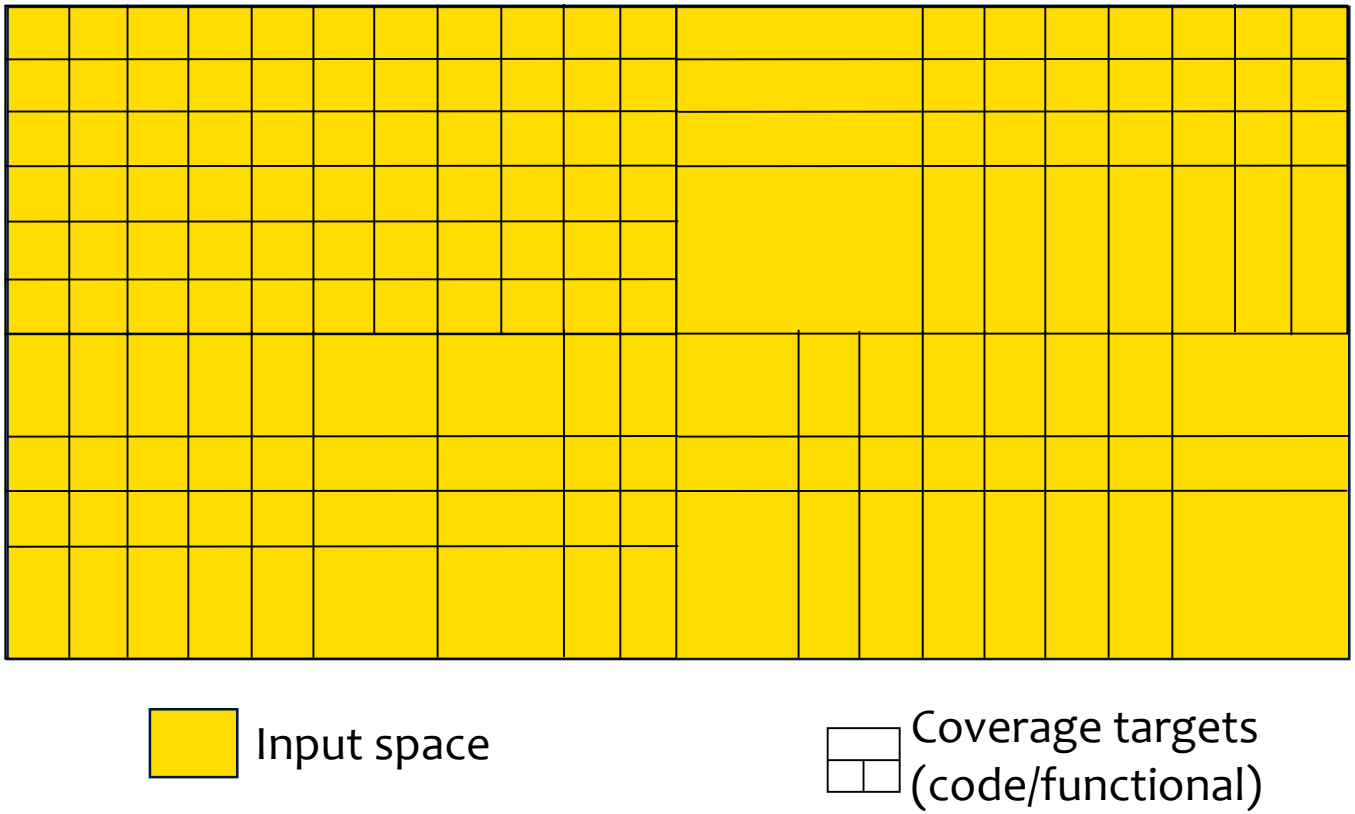
Coverage Grid



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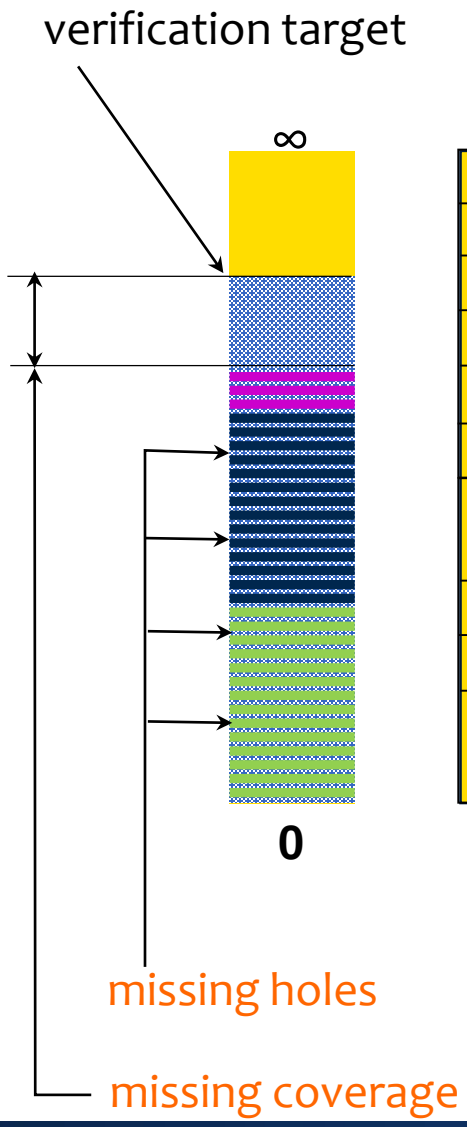
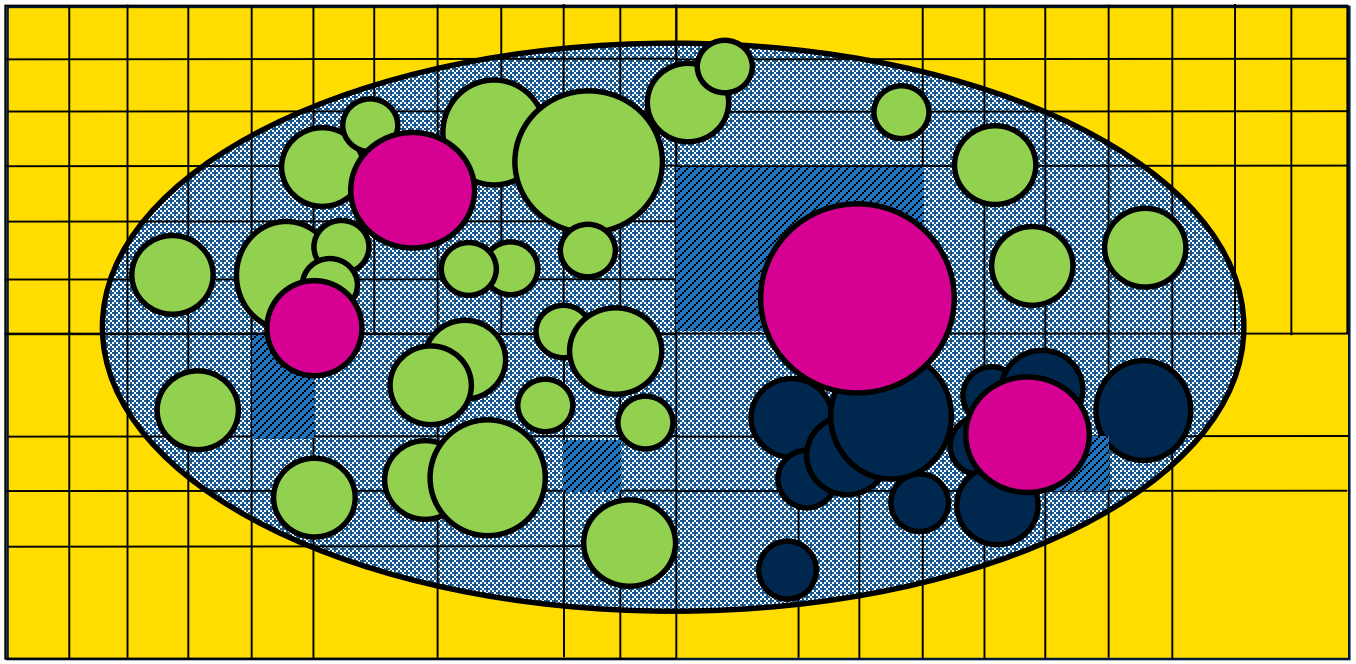
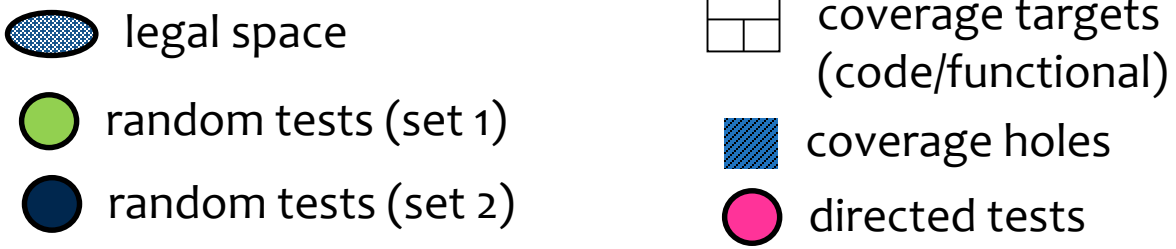
Formal & Simulation Difference: Verification Closure (1/2)



Simulation: 0+





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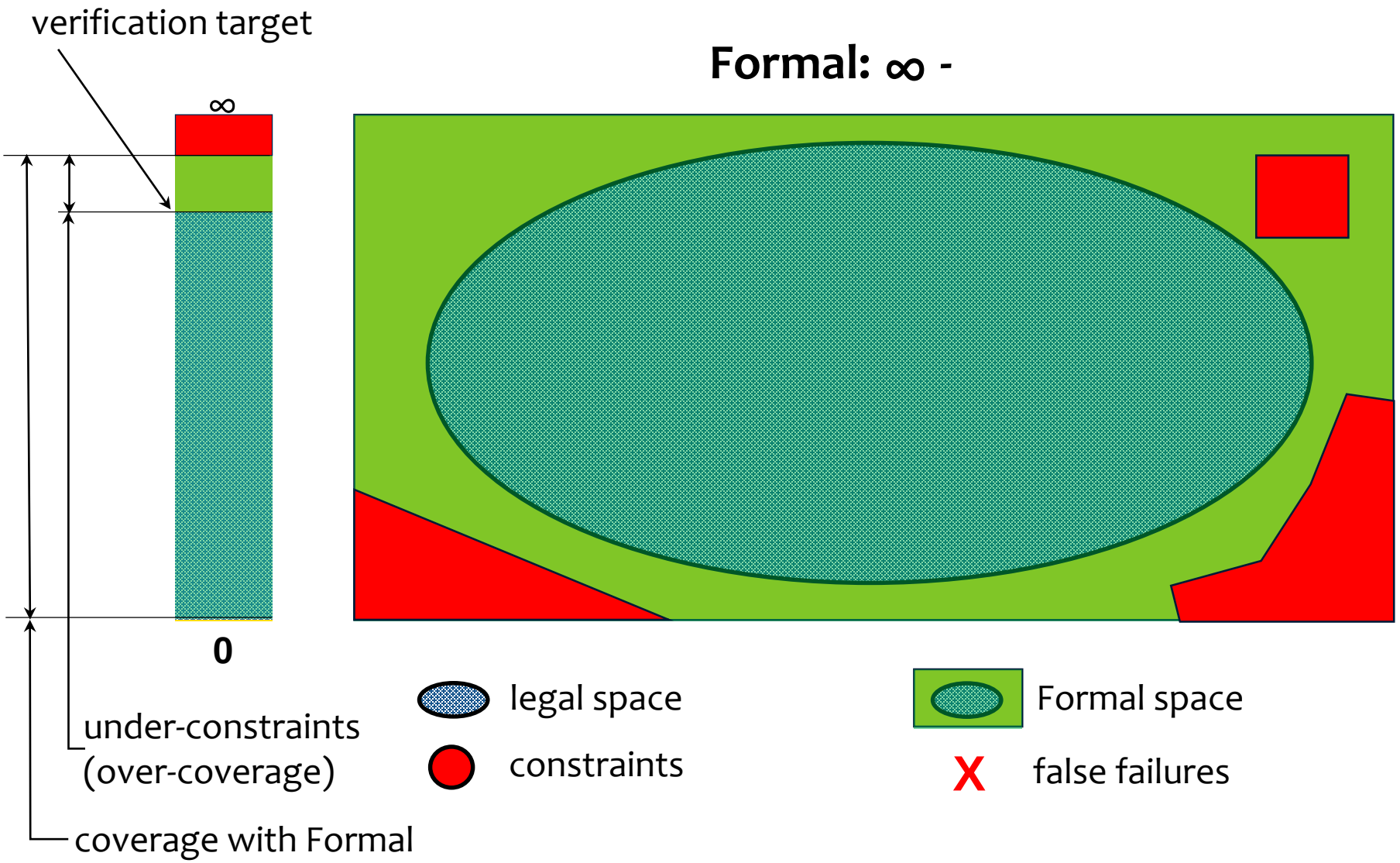
Formal & Simulation Difference: Verification Closure (2/2)



Different Types of Coverage

- What to Measure (targets)
  - Structural coverage
    - Statement (line) coverage
    - Branch coverage
    - Expression coverage
    - FSM coverage
    - Toggle coverage
  - Functional coverage
  - Will not cover in this talk – assume line coverage from now on
- When to Measure
  - Controllable (controlling inputs)
    - Reachability coverage (analogous of classical simulation coverage)
  - Observable (observing at outputs or checkers)
    - COI coverage
    - Proof Core coverage (analogous to mutation coverage in simulation tools)

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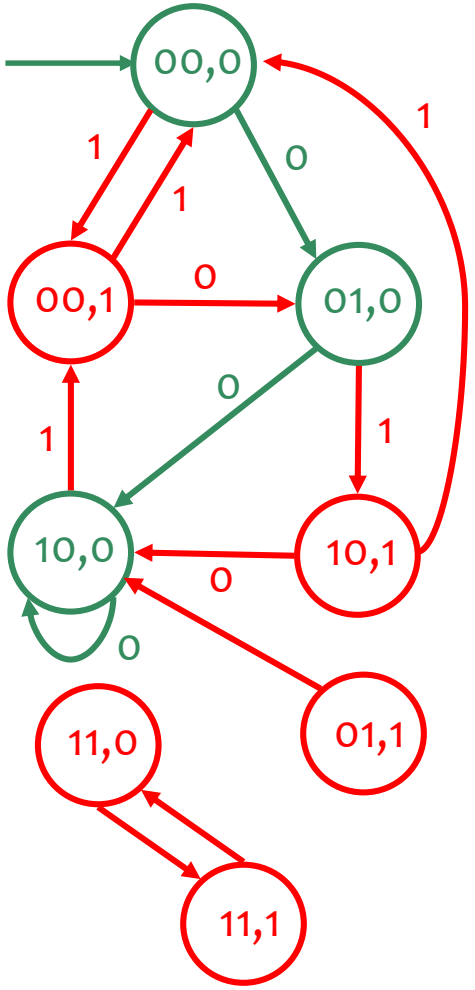
Simulation Coverage (a = 0)

```
input a;
reg b;
reg [1:0] st;

always @(posedge clk or negedge rst)
  if (~rst) st <= 2'b00;
  else case( st )
    2'b00: if (~a) st <= 2'b01;
    2'b01: st <= 2'b10;
    2'b10: if (a) st <= 2'b00;
    endcase

always @(posedge clk or negedge rst)
  if (~rst) b <= 1'b0;
  else if (~a | b) b <= 1'b0;
  else b <= 1'b1;
```



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End-to-End Formal Verification

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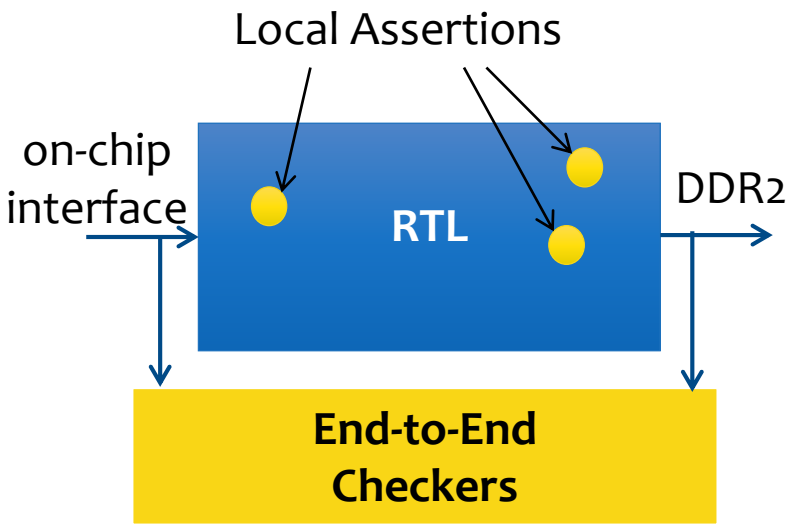
What is End-to-End Formal?

- Local Assertions – easier to verify
  - Internal RTL assertions, embedded in RTL
- End-to-End Checkers – hardest to verify
  - Model end-to-end functionality
  - **Can replace simulation**
  - Often requires Abstraction Models to manage complexity



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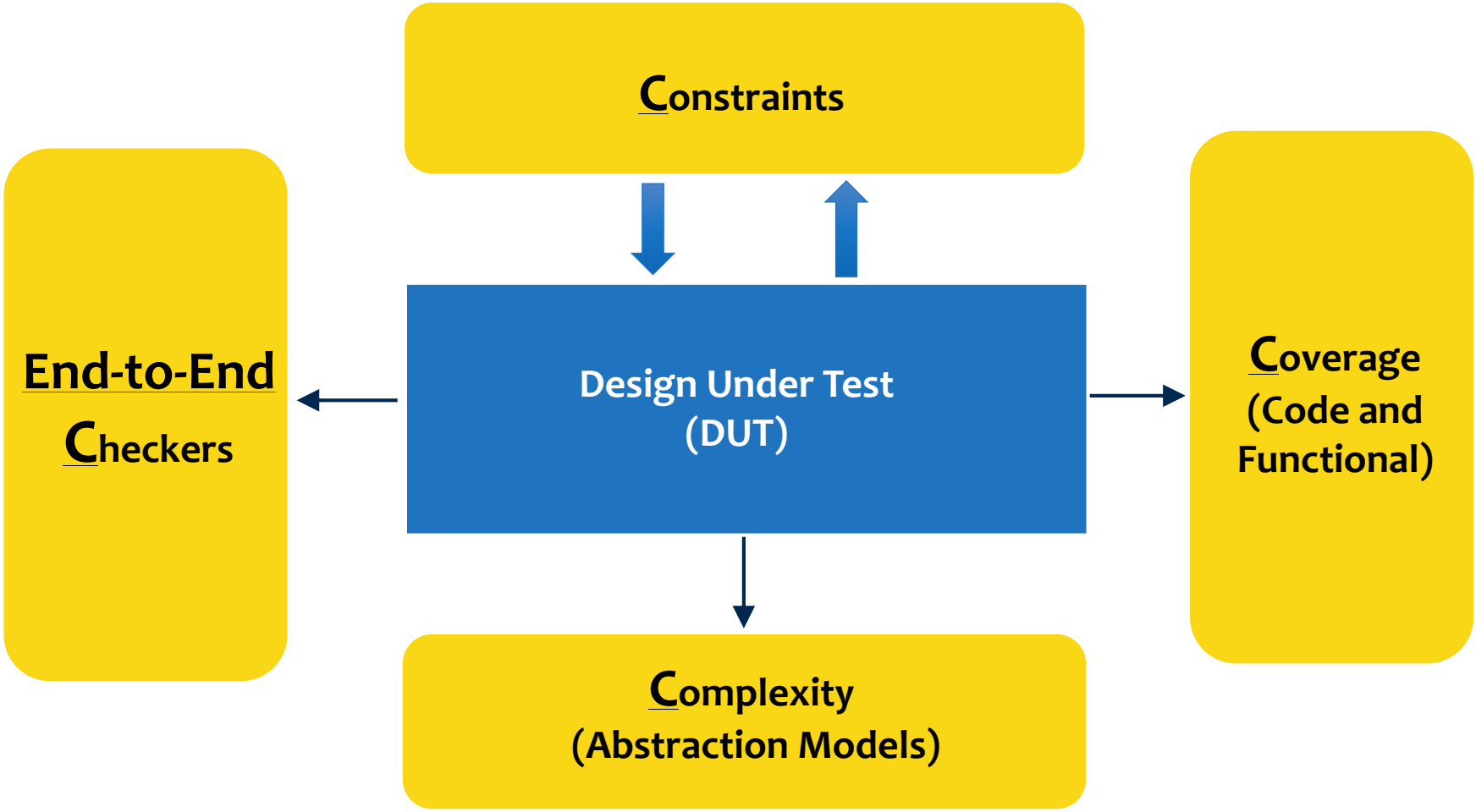
Testbench Architecture for End-to-End Formal

Need to Quantify Completeness of Other 3 C's



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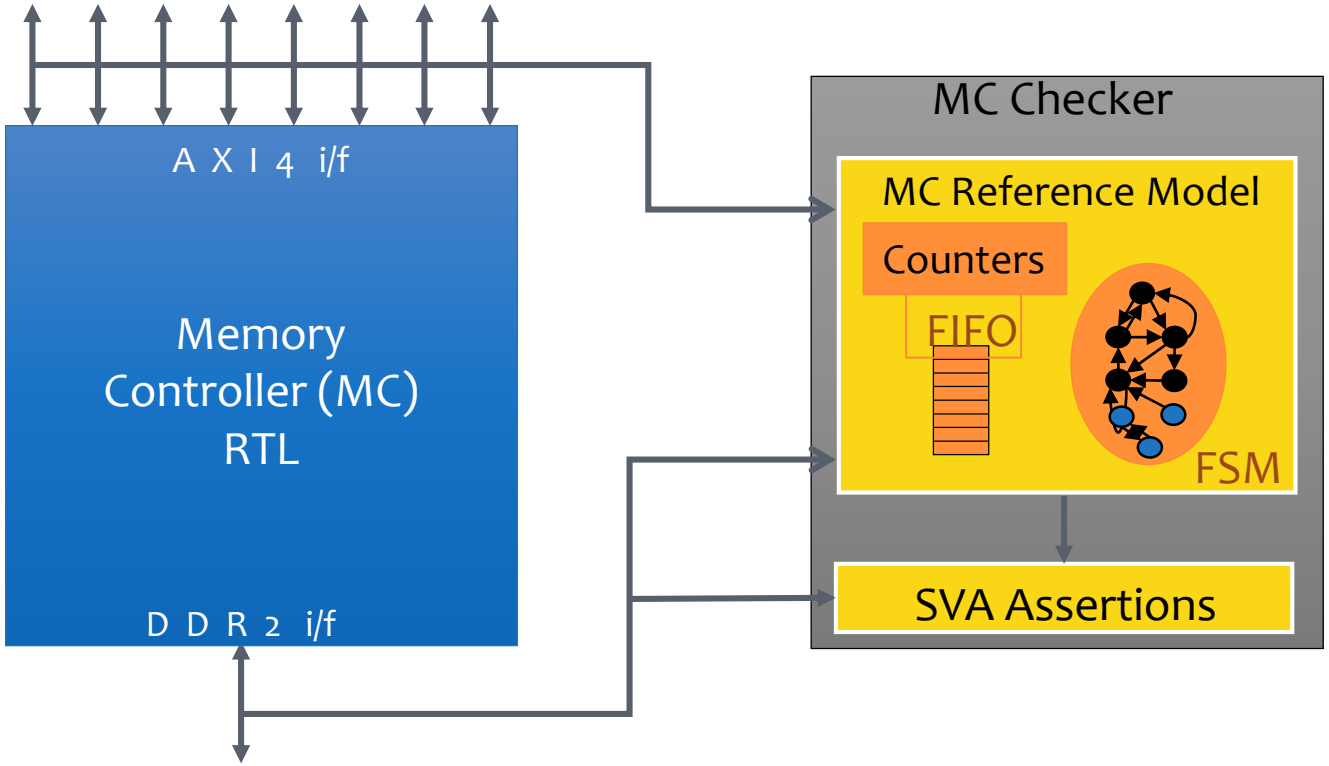
End-to-End Checkers

- 95% of End-to-End Checker is in SV or Verilog; rest is SVA
  - Developing synthesizable reference model is as big an effort as writing RTL



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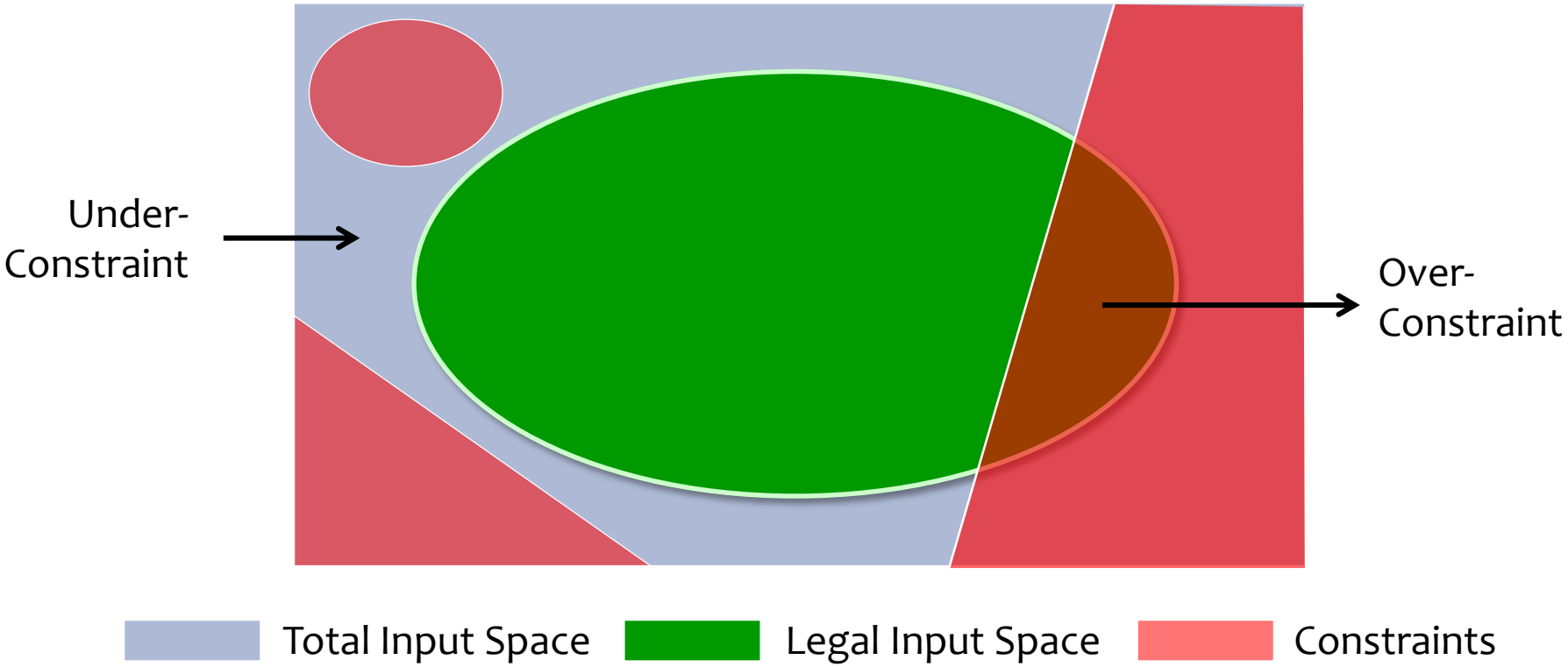
Constraints

- Used to restrict input space to contain only legal input sequences
- Need to watch out for under-constraints & over-constraints



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Where Complexity Comes From

Checker: (st == 2'b01) => ~b

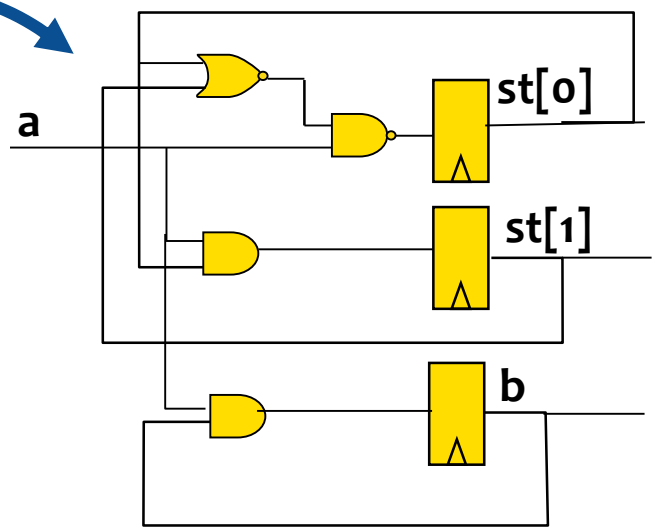
RTL

```
input a;
reg b;
reg [1:0] st;

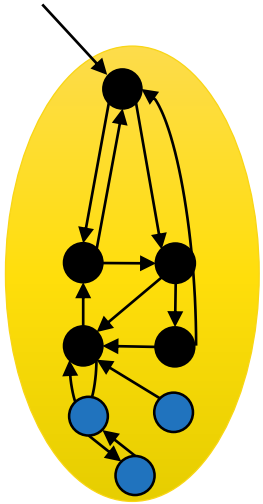
always @(posedge clk or negedge rst)
 if (~rst) st <= 2'b00;
 else case( st )
       2'b00:  if (~a) st <= 2'b01;
       2'b01:  st <= 2'b10;
       2'b10:  if (a) st <= 2'b00;
       endcase

always @(posedge clk or negedge rst)
 if (~rst) b <= 1'b0;
 else if (~a | b) b <= 1'b0;
 else b <= 1'b1;
```

Internal Netlist



Internal STG



$2^3 = 8$

$2^{10} = 1{,}024$

$2^{20} = 1{,}048{,}576$

$2^{30} = 1{,}073{,}741{,}824$

Formal Complexity Comes from Search Space Explosion and can lead to inconclusive (bounded) results!

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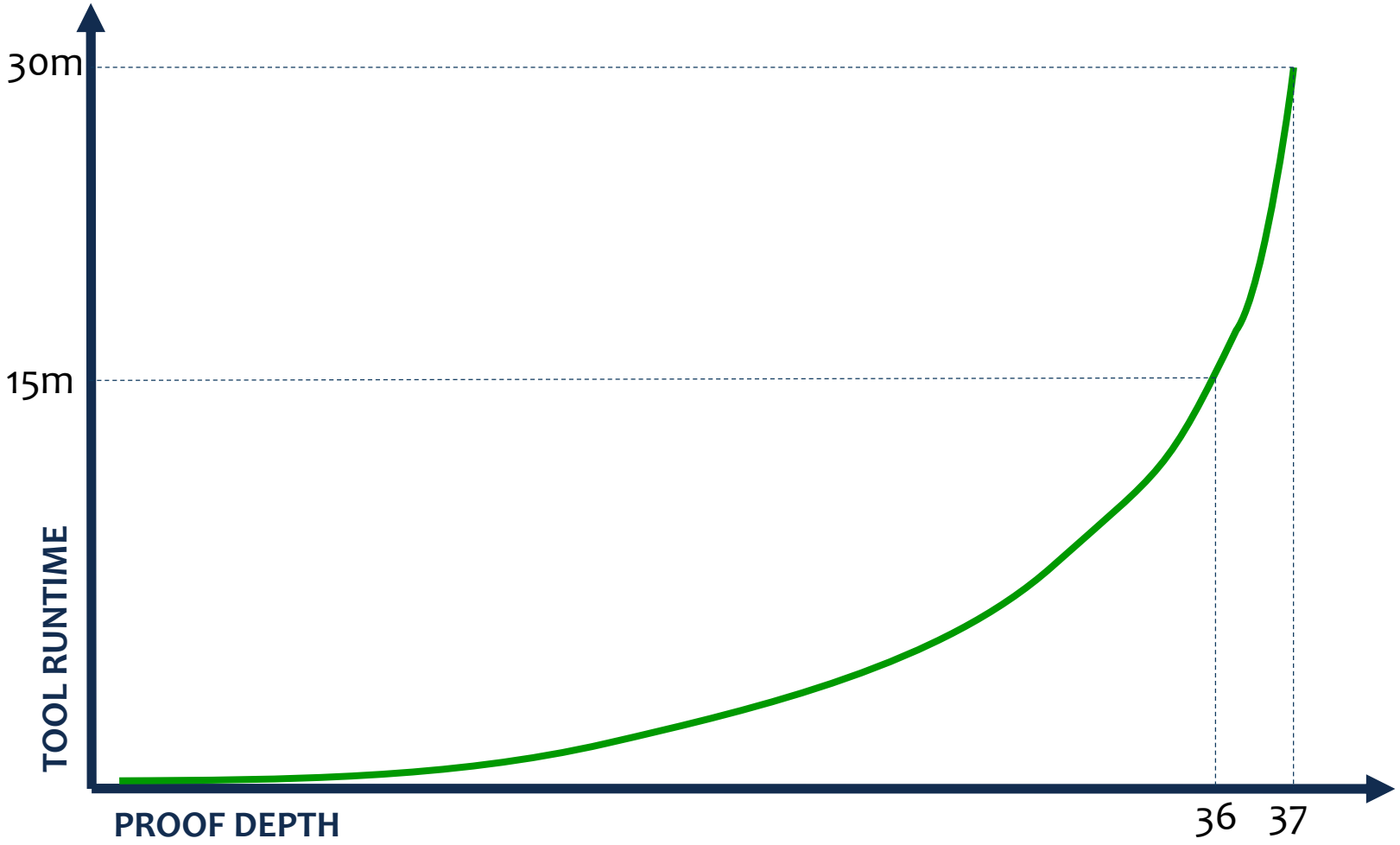
Can't Fight the Exponential Complexity!



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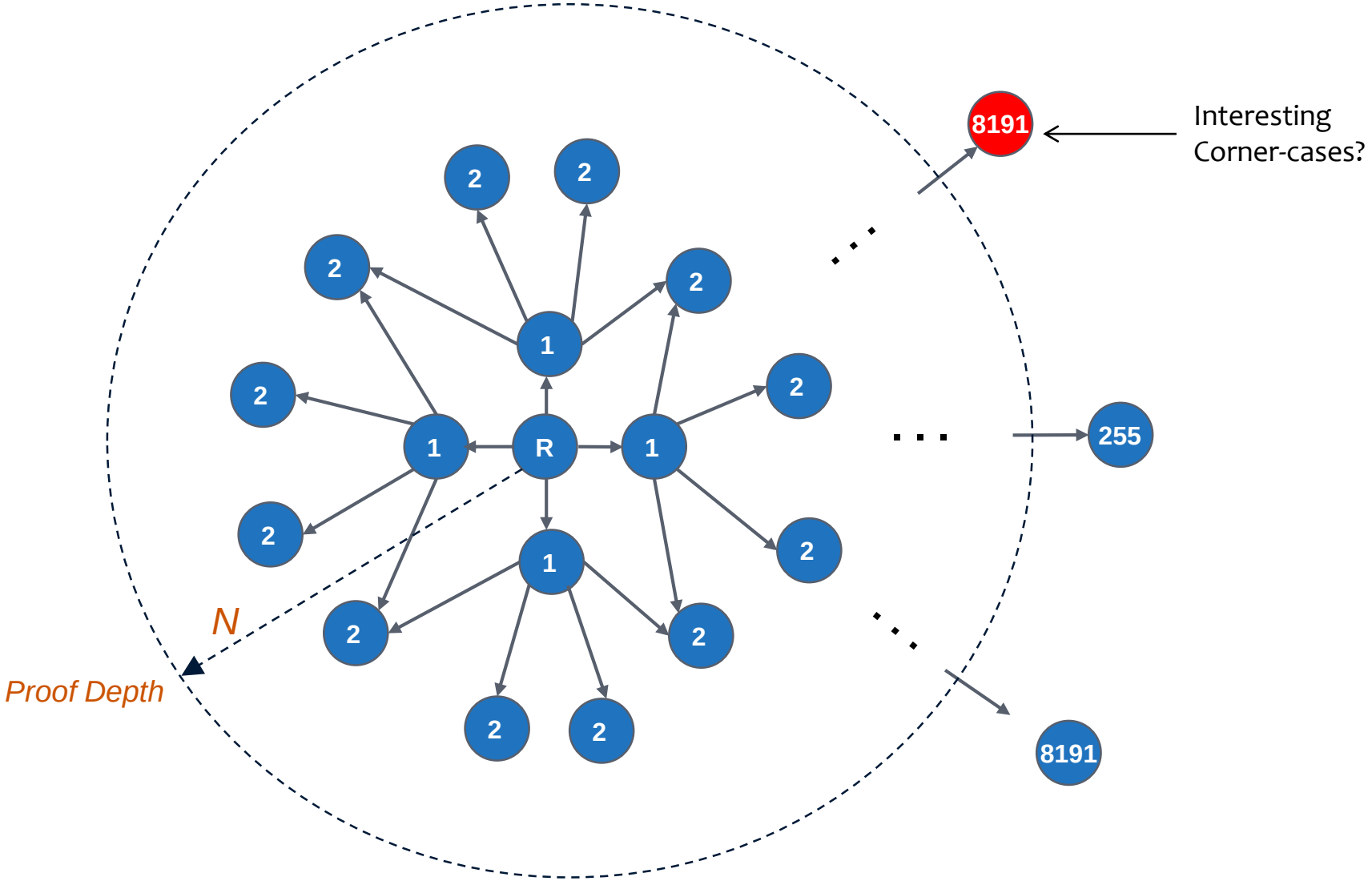
Formal Covers All State Transitions Within Proof Depth



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Formal Coverage

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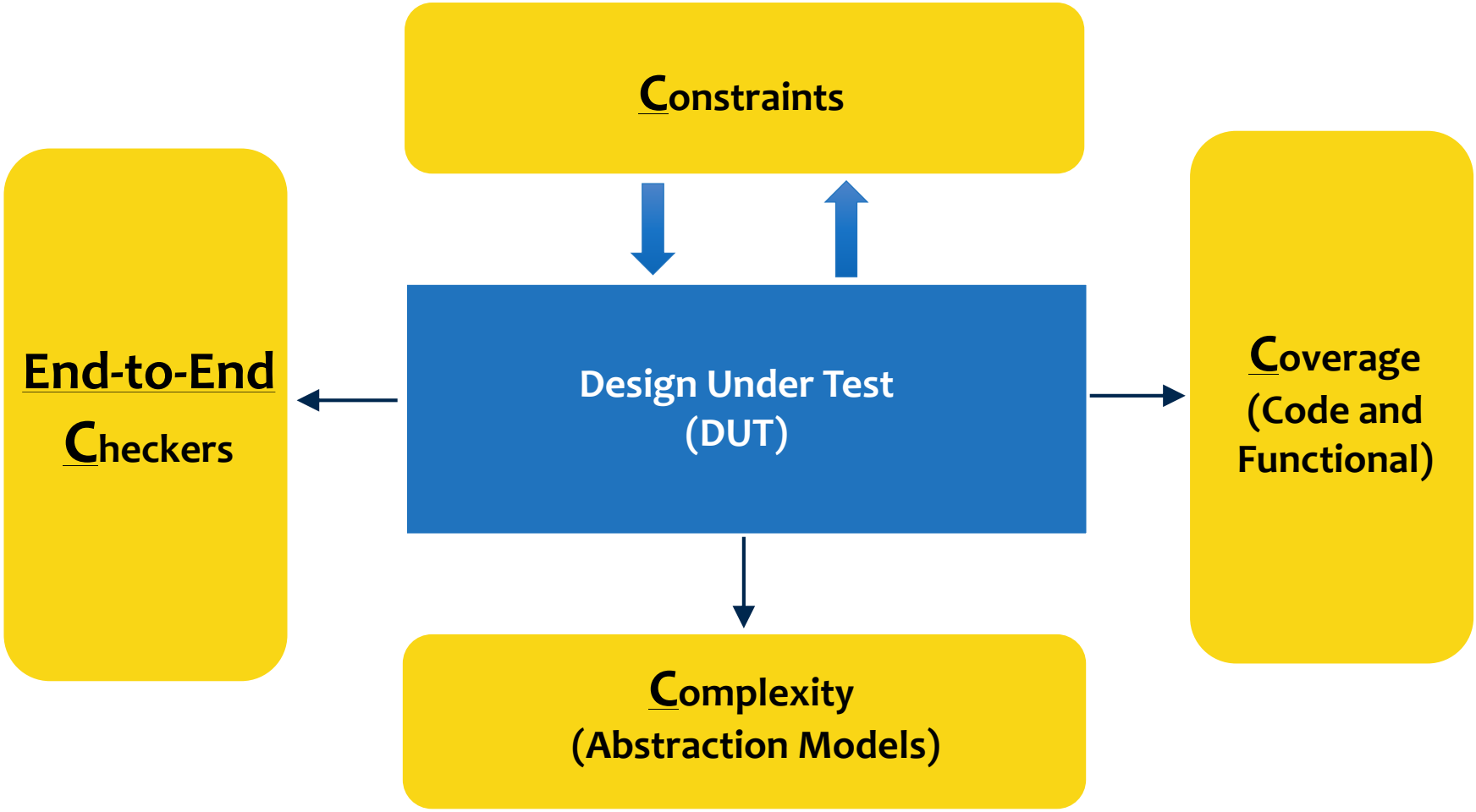
Testbench Architecture for End-to-End Formal

Quality of Formal Depends on all 4 Cs!



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Formal Coverage Measure Goodness of Three C's

- Constraints: Environment may be over-constrained
  - Intentional: avoided some hard to model or verify input combinations
  - Unintentional: bugs in constraints; forgot to remove intentional over-constraints
- Complexity: Sign-off on bounded proof
  - A checker is verified up to proof depth N
  - If a target is not covered in N cycles, proof depth is not sufficient
- Checkers: Measures completeness of the checkers
  - Which portion of logic is used to prove the checkers

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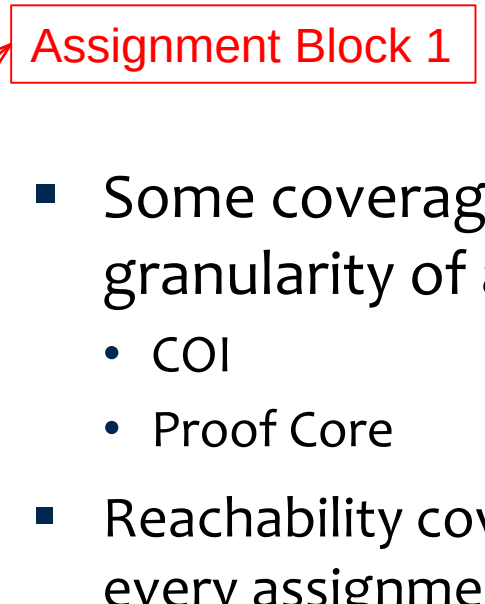
Assignment Blocks

```
reg p, q;
always @(*) begin
  if (a) begin
    p = d1;
    q = e1;
  end else begin
    p = d2;
    if (b) begin
      q = e2;
    end else begin
      p = d3;
      q = e3;
    end
  end
```



- Some coverages are at the granularity of assignment blocks
  - COI
  - Proof Core
- Reachability covers some portion of every assignment block!
  - Unless testbench is totally vacuous

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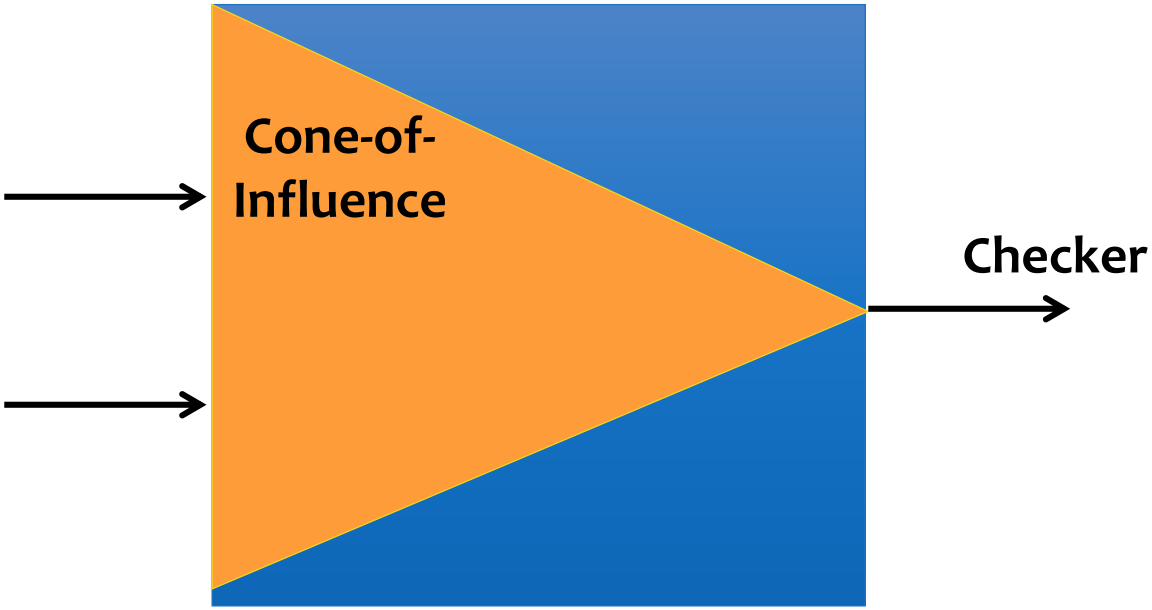
Cone-of-Influence (COI) Coverage

- COI is cheap to compute, but is conservative



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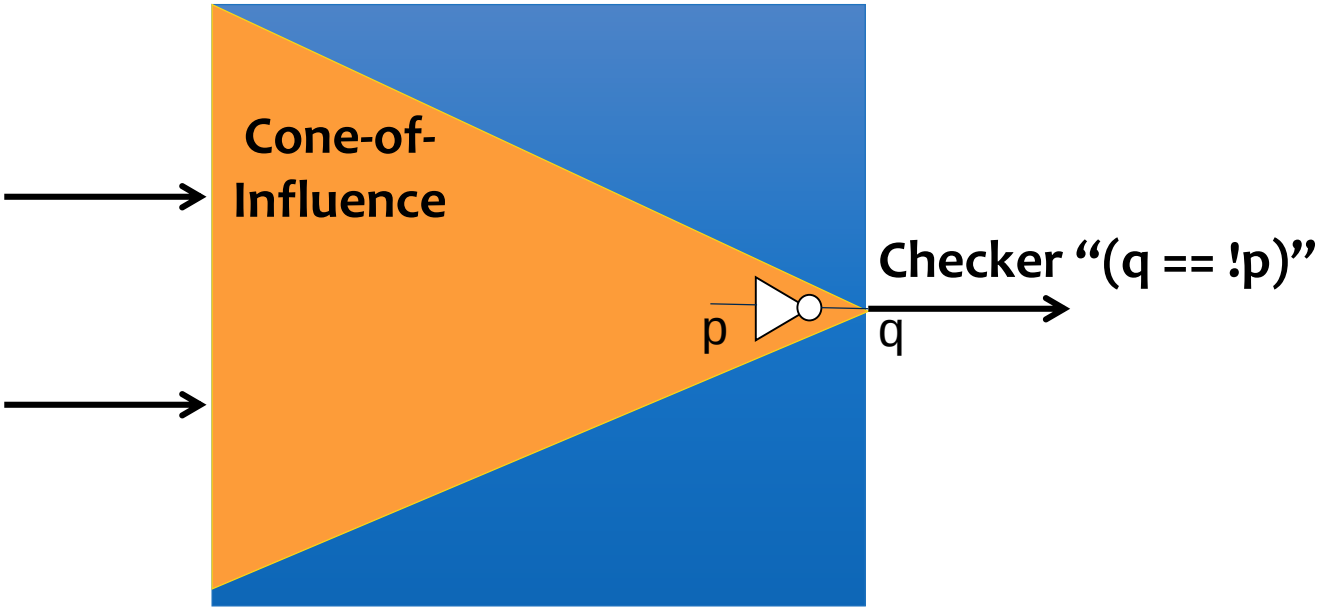

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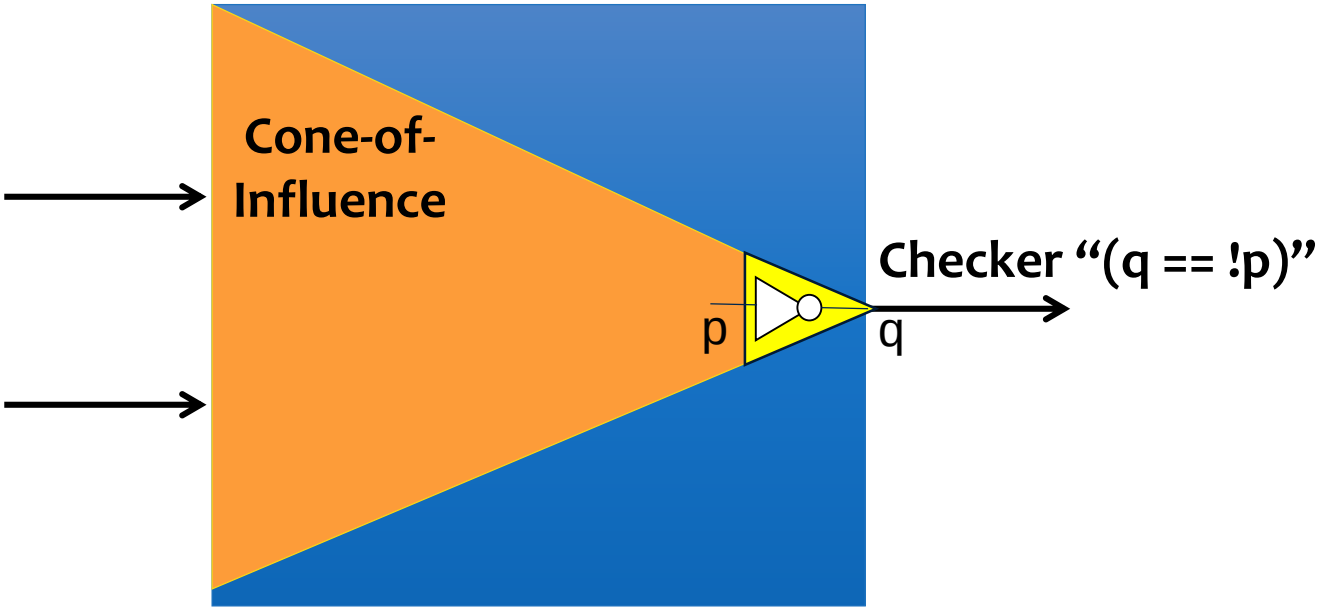
Cone-of-Influence (COI) Coverage

- Would like to cover only the logic needed for the proof



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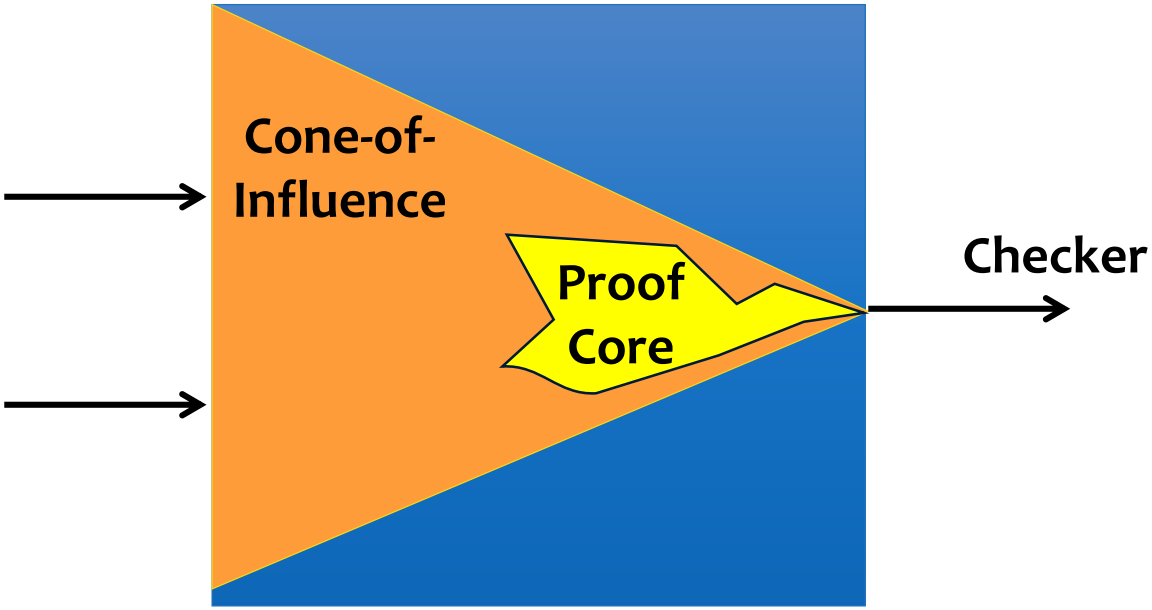
COI vs Proof Core (for Checkers)

- Proof Core is more expensive to compute, but is almost "exact"
  - Granularity is assignment block (not fine-grained), like COI, not Reachability
  - May be slightly conservative sometimes (not so much in practice)
    - Not much conservative in practice
    - 100% coverage does not mean no bugs, so "almost exact" is "good enough"



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COI vs Proof Core Trade-offs

	COI	Proof Core
Cost to compute	Small (netlist traversal)	Larger (must finish proofs)
Value	Some	A lot

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Example – Proof Core

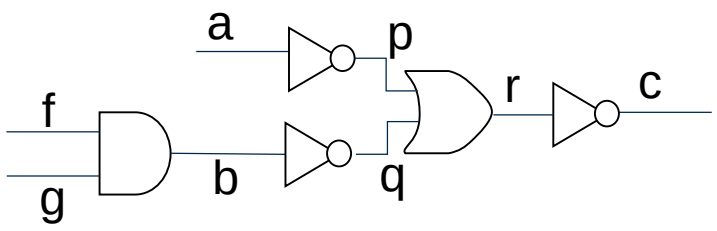
```
reg b, p, q, r, c;
always @(*) begin
  b = f && g;

  if (a) p = 1'b0;
  else p = 1'b1;

  if (b) q = 1'b0;
  else q = 1'b1;

  r = p || q;

  if (r) c = 1'b0;
  else c = 1'b1;
end
```




```
prop_a_and_b:
assert property(@(posedge clk)
disable iff (rst)
   (c = (a && b)));
```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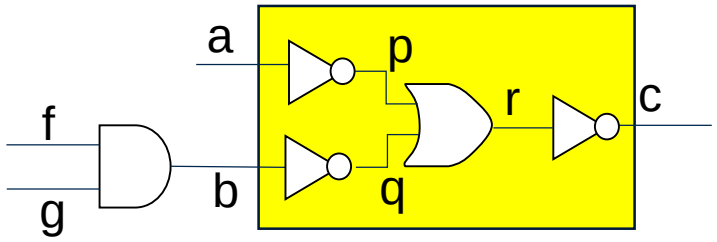


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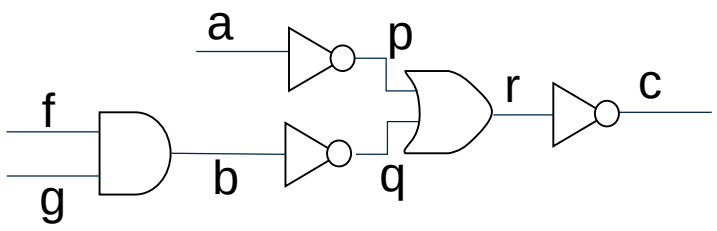


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```
prop_a:
assume property(@(posedge clk)
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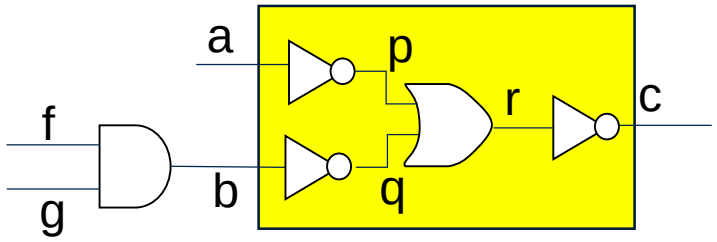


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Reachability Coverage

- In N cycles (depth of the shallowest proof):
  - Which coverage targets are reached?
  - Which coverage targets cannot be reached (including provably unreachable)?
  - Which are undetermined? (likely none within the Proof Core)
- Unless total vacuity (constraints conflict), every assignment block will have something covered!

```
reg q, r, c;
always @(*) begin
  if (b) q = 1'b0;
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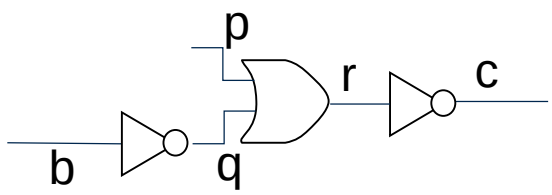


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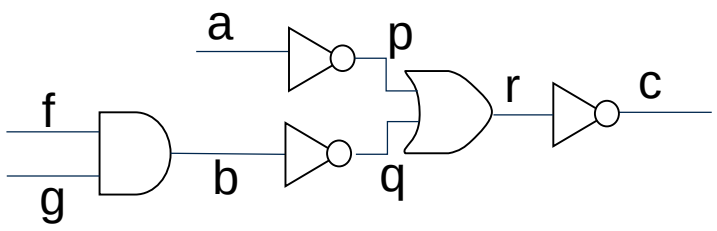


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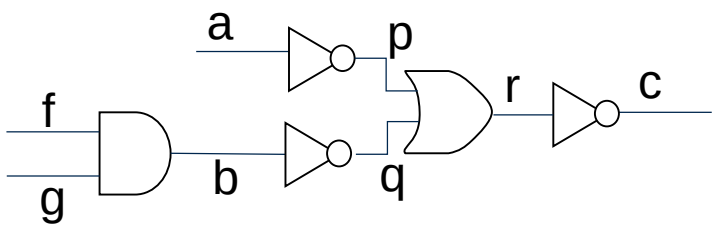
  r = p || q;

  if (r) c = 1'b0;
  else c = 1'b1;
end
```




```
prop_a_and_b:
assert property(@(posedge clk)
disable iff (rst)
   (c = (a && b)));
```

```
prop_a:
assume property(@(posedge clk)
disable iff (rst)
   a);
```

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Example – Reachability

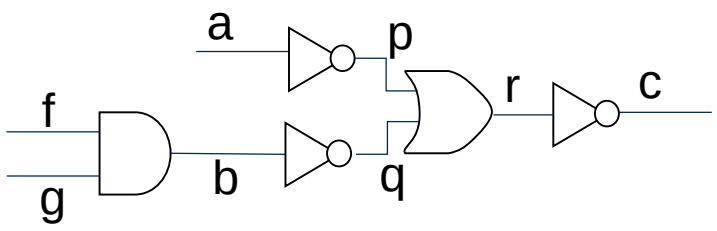
```
reg b, p, q, r;
always @(*) begin
  b = f && g;

  p = !a;

  if (b) q = 1'b0;
  else q = 1'b1;

  r = p || q;

  if (r) c = 1'b0;
  else c = 1'b1;
end
```




```
prop_a_and_b:
assert property(@(posedge clk)
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```

```
prop_a:
assume property(@(posedge clk)
disable iff (rst)
   a);
```


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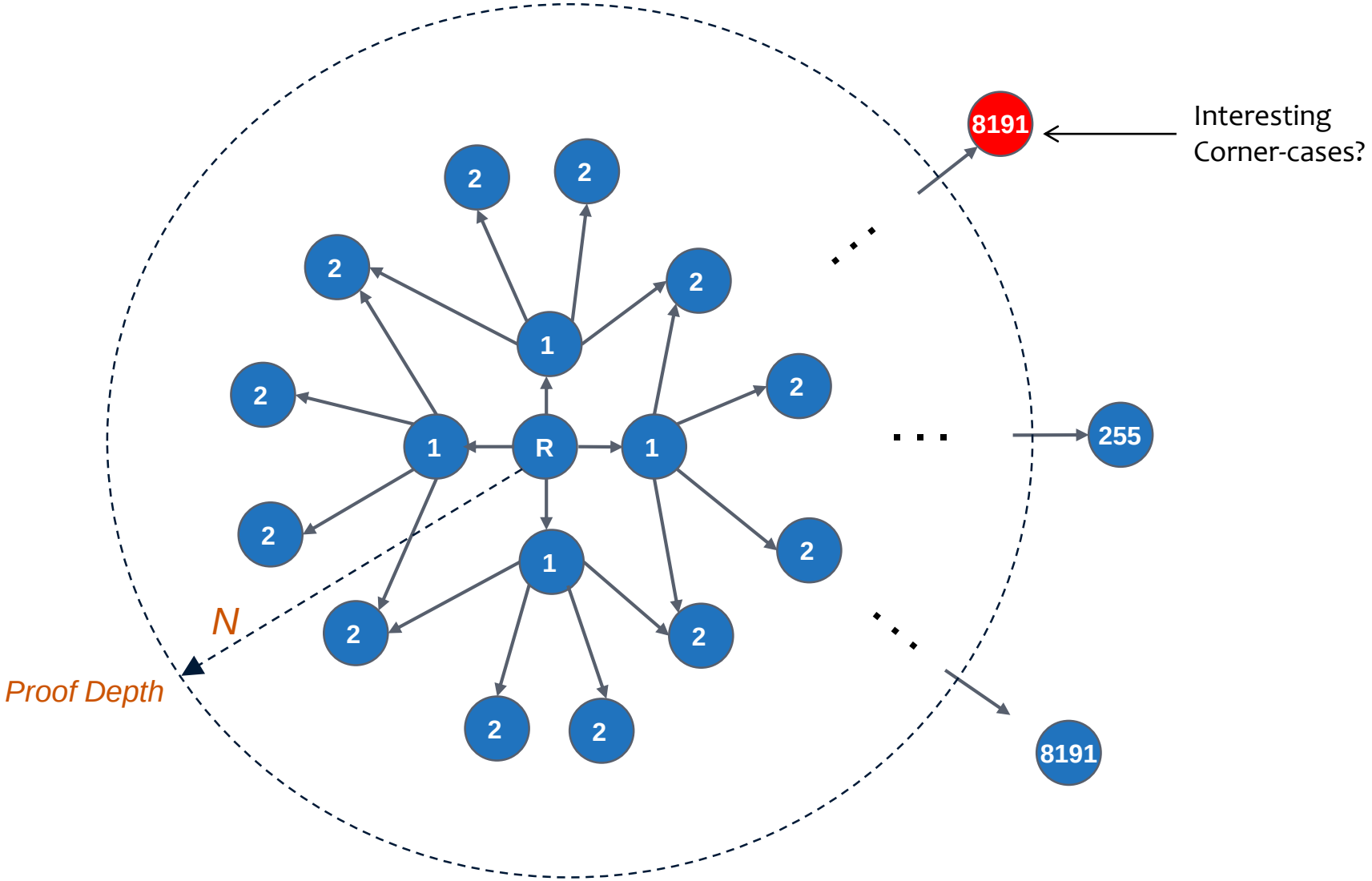
Formal Covers All State Transitions Within Proof Depth



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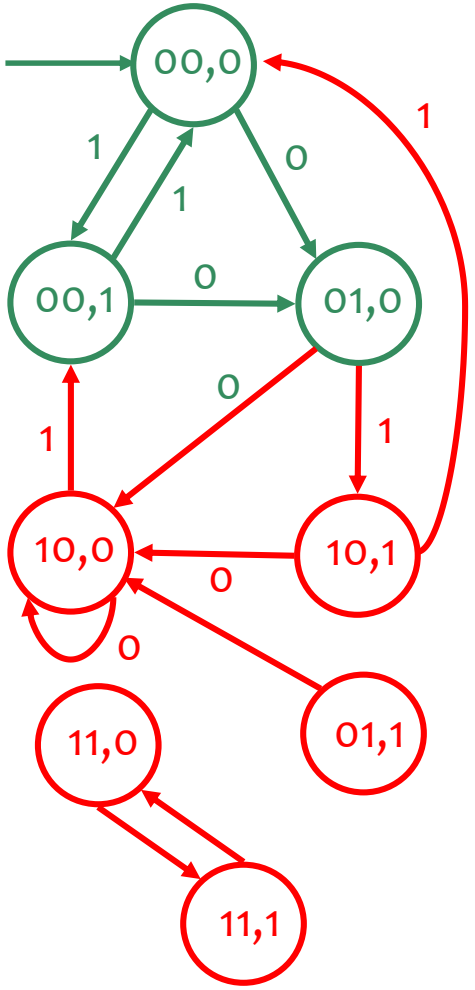
Formal Coverage (depth = 1)

```
input a;
reg b;
reg [1:0] st;

always @(posedge clk or negedge rst)
  if (~rst) st <= 2'b00;
  else case( st )
    2'b00: if (~a) st <= 2'b01;
    2'b01: st <= 2'b10;
    2'b10: if (a) st <= 2'b00;
    endcase

always @(posedge clk or negedge rst)
  if (~rst) b <= 1'b0;
  else if (~a | b) b <= 1'b0;
  else b <= 1'b1;
```



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COI vs Proof Core Trade-offs

	COI	Proof Core	Reachability
Checkers	✔	✔ ✔	
Constraints		✔	✔ ✔
Complexity (Proof Depth)		✔	✔ ✔

- Best coverage option
  - Intersection of Proof Core and Reachability (up to N clocks)
    - Outside either means not used in verification, or not exercisable
  - If constraints are not mature (illegal inputs)
    - Proof Core is smaller than final Proof Core (a subset of logic is enough for CEX)
    - Reachability is larger than final Reachability (illegal transitions are possible)
    - Can start with COI

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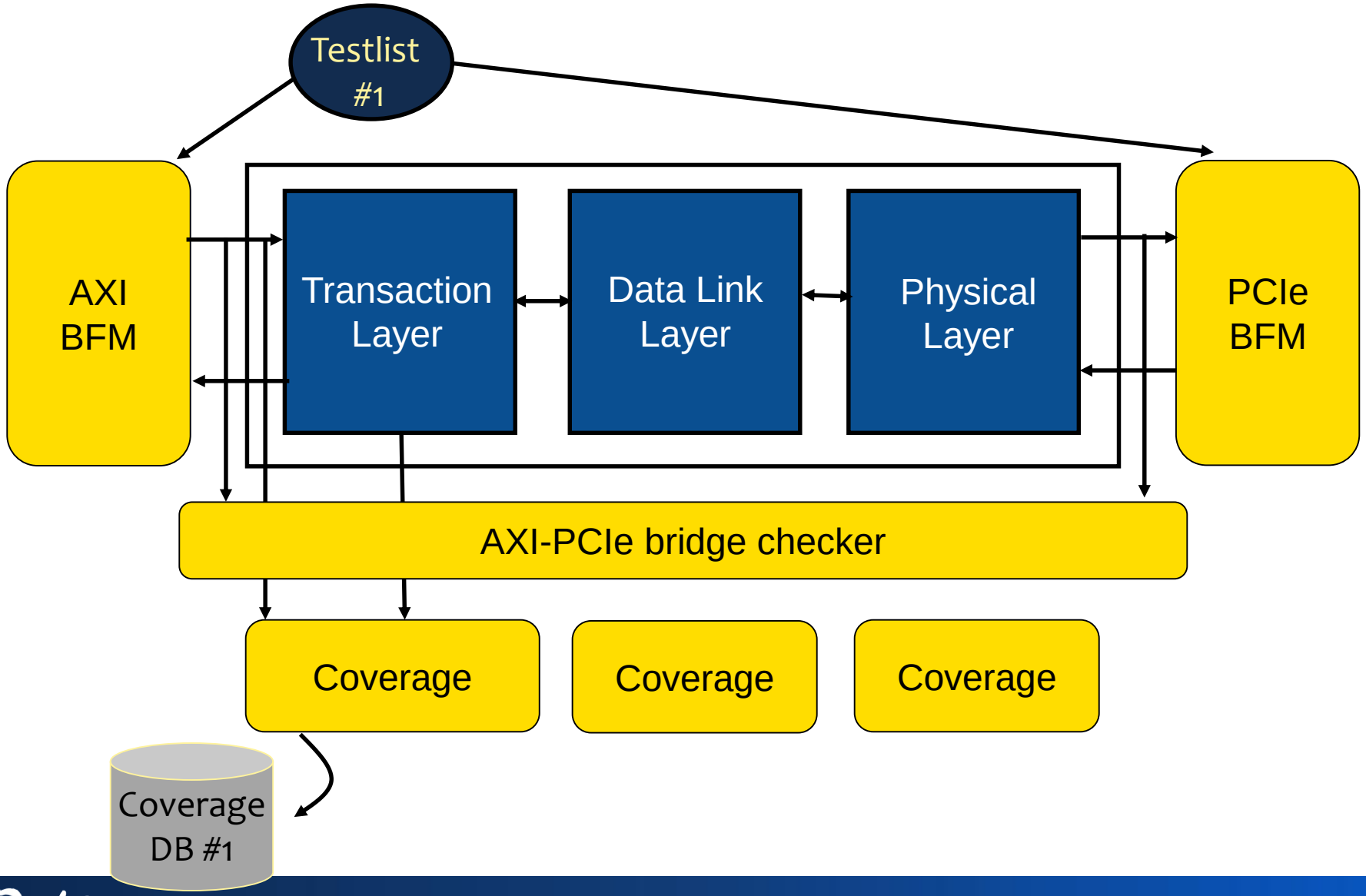
Simulation Coverage Collection



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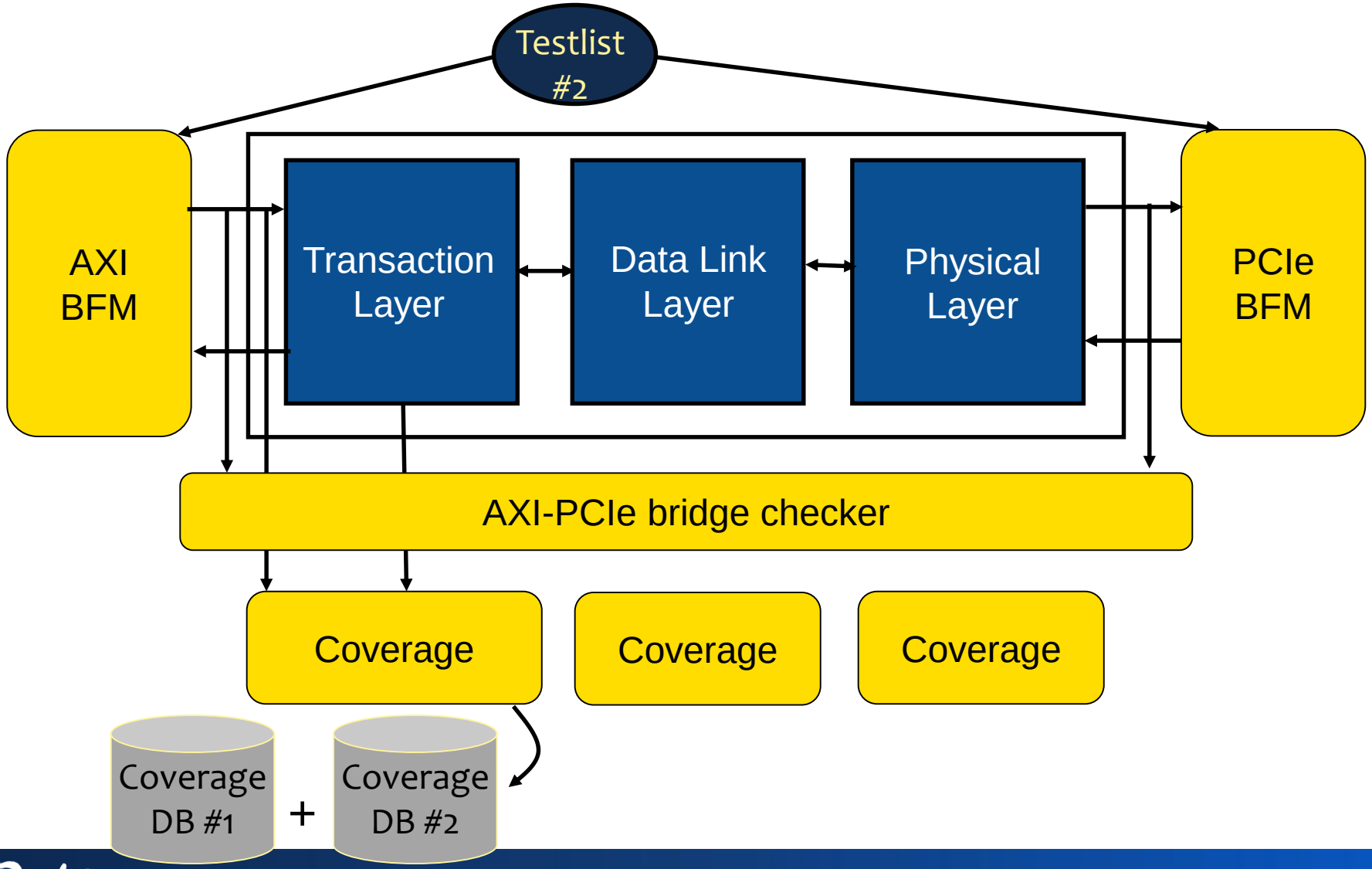
Simulation Coverage Collection



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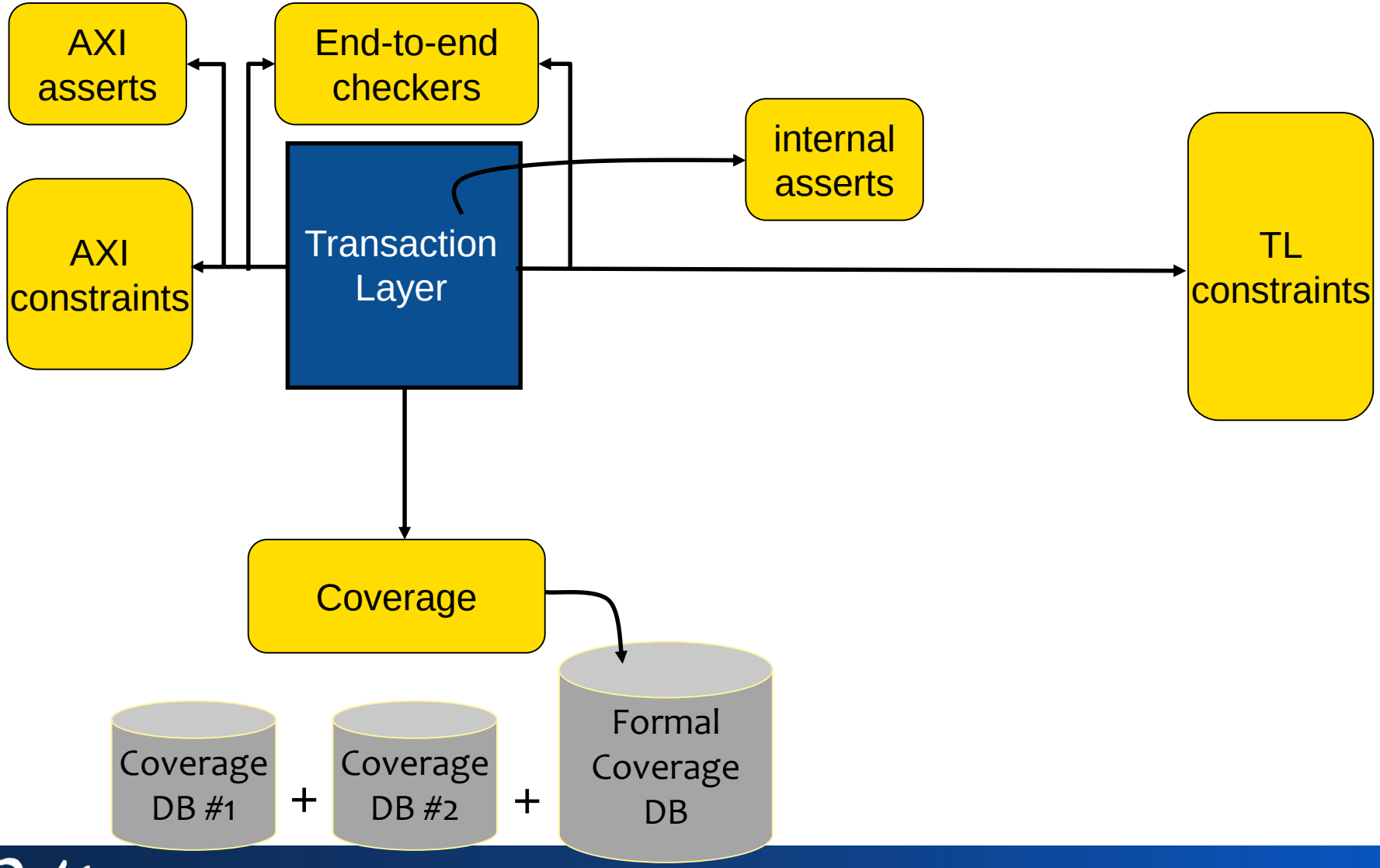
Merged with Formal Coverage – Some Day…



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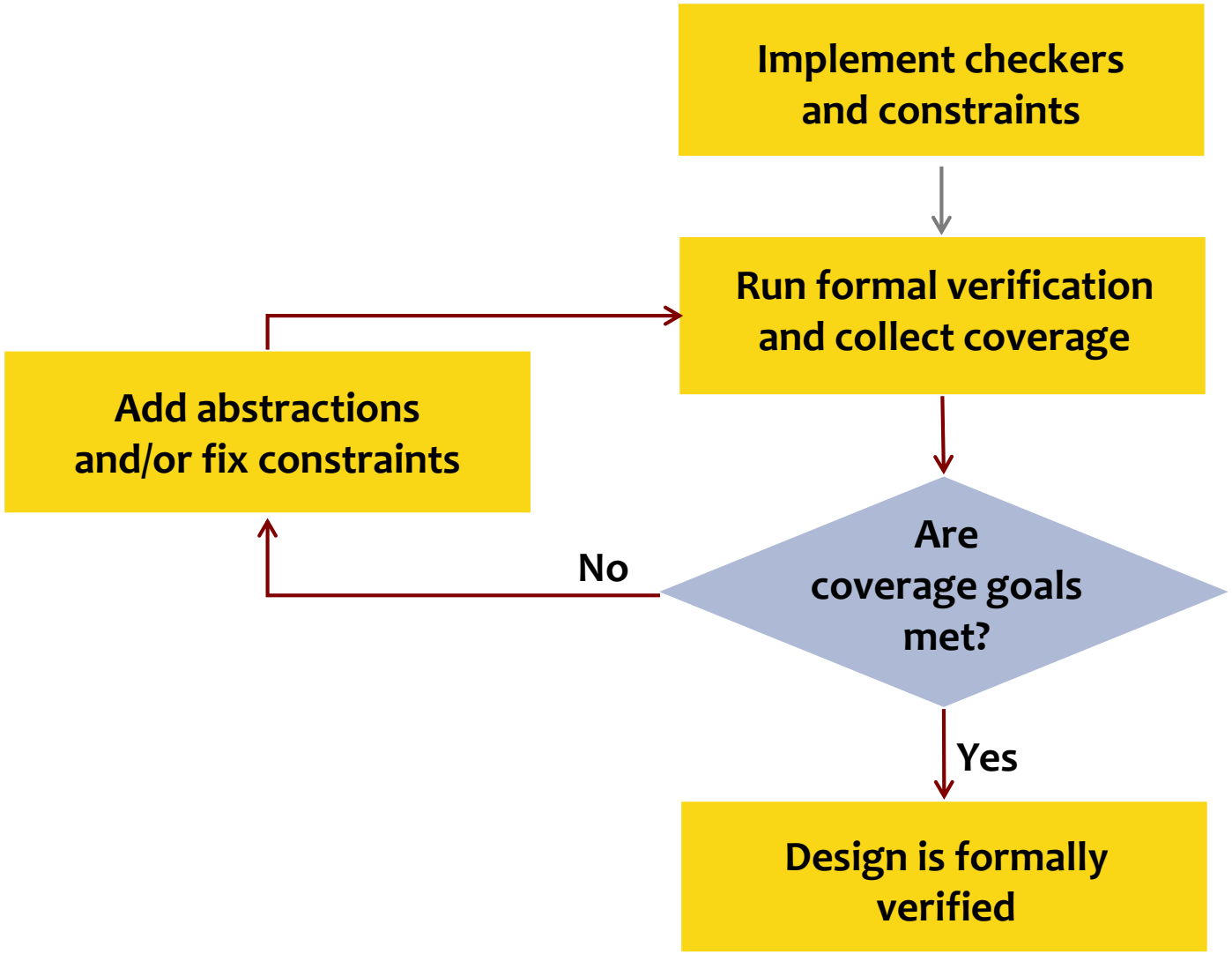
Formal Coverage Methodology



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Where Formal Coverage Is Important for Formal Sign-off

- Constraints – check for over-constrained environment
  - Intentional: avoided some hard to model, or verify, input combinations
  - Unintentional: bugs in constraints; forgot to remove intentional over-constraints
- Complexity – sign-off on bounded proof
  - All checkers are verified up to proof depth N
  - Any target that is not reachable in N clocks is not covered
- Checkers – does not verify completeness of Checkers
  - No different than simulation!

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Thank You!

Unique Methodology. Highest Coverage. Fastest Time to Market.

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