

bits	name		Big Endian Network Order	
3	primary op		An carries	
2	dest Addr mode		Dn modulo size, high no effect	
3	dest reg			
1	secondary op	quicks and extra	Double(1)/Float(0) Default is D	
2	size	L is default size		
2	src Addr mode	5	0 equals 32	
3	src reg	quick	branch signed from PC+1	
Addr mode			size	
#00	An	Not CFR src	#00	.W
#01	(An)		#01	.L
#10	Dn	Not CFR src	#10	.Q
#11	Special		#11	.D/.F
Special				
#000	PC	Not float	Not CFR src	
#001	(PC+)/(-SP)	special write	For PCX subroutine	
#010	IP	Not float	Not CFR src	
#011	(IP+)/(-RP)	special write	For IPX threaded code	
#100	SP	Not float	Not CFR src	
#101	(SP+)/(+SP)	Once (x)(+x) RW	NIP semantics	
#110	RP	Not float	Not CFR src	
#111	(RP+)/(+RP)	Once (x)(+x) RW	NIP semantics	
ops	D		F	
#000	MOV	No dest read	MVQ	quick src args
#001	ADD		ADQ	unsigned 5 bit
#010	MLL	Multiply lower	MLQ	for compact
#011	SUB		SBQ	code
#100	CFR (specials)	No dest read	BPL	quick branch
#101	AND		BMI	0 and -1 do sign
#110	ORR		BZE	of 16 bit
#111	XOR		BNZ	displacement
D/F ops (size)	D/F			
#000	FDV	Divide		
#001	FAD			
#010	FML			
#011	FSB			
#100	FBP	quick branch		
#101	FBM	0 and 1 do sign		
#110	FBD	of 16 bit	Branch denormal zero	

#111	FBI	displacement	Branch infinity	
For efficient floats with own register set use vectors				

CFR src					
An	halves				
Dn	fulls				
PC	PCX	fast exchange			
IP	IPX	of registers			
SP	SPX	improves code			
RP	RPX	good stuff			
The src MUST be an address for CFR					
halves An					
Blocks of 8	B,W,L = half		F		
#000	EXH	Exchange halves	DTF	Double to float	
#001	SXL	Sign extend low	FTD	Float to double	
#010	INU	Increase upper	FIR	Float Inv root	
#011	DCU	Decrease upper	FAT	Float ATN	
#100	SLT	Shift left Q half	FEX	Float EXP	
#101	SRT	Shift right Q half	FLN	Float LN	
#110	ADU	Add upper	FSN	Float SIN	
#111	SBU	Subtract upper	FCS	Float COS	
fulls Dn					
Blocks of 8	W,L,Q		D		
#000	ABS	Absolute	DTQ	Double to quad	
#001	SGN	Sign to 0 or -1	QTD	Quad to double	
#010	NOT	Not	FIR	Double Inv root	
#011	CPL	Complement	FAT	Double ATN	
#100	WTO (group)	Write target over	FEX	Double EXP	
#101	CLR	Clear to zero	FLN	Double LN	
#110	ASR	Arith shift right	FSN	Double SIN	
#111	LSR	Logic shift right	FCS	Double COS	
	W	L	Q		
WTO group			WTO		
WTO is set write target override for following instruction for 3 operands					
Only affects following instruction if at all					
When used with MOV, MVQ, CFR but not specials except WTO makes a reserved nop pair					
These reserved nop pairs may be assigned other function					
WTO a MOV b,c becomes a = b/c, b = remainder for example				DIV	
Similar with WTO MVQ all done unsigned				DVQ	

(@COM n (COM m d16)) spare opcode space			
#nnn11nn0 011sssss opcode form points to			
#mmm11mm0 011000			
#dddddddd dddddddd			
Difficult to use directly			
Only first of pair, branches delay second as delay slot.			
Second after branch may or may not speculative execute and commit			
Allow setting up and special COM?			
#mmm11mm0 011000			
#dddddddd dddddddd is the instruction replaced by profile COM			
mmm	profile counter number to increase		
mm	recall to register except PC		
If register is PC just increment profile counter			
Any immediates are ordered in the main instruction stream			
(BRK/TRP/HPR/CIV m d16) spare opcode space			
#mmm11mm0 111000			
#dddddddd dddddddd			
Except when mm is PC nnn is register special below			
#mmm			
#000	Processor serial number		
#001	Clock counter for cycles since power on (timing)		
#010	Clocks stalled since on for efficiency measure		
#011	Clock with boost cycles since on		
#100	Branch miss count since on		
#101	Branch hit count since on		
#110	Data cache miss since on		
#111	Instruction cache miss since on		
When nn is PC clear profile register nnn			
The register specials are only cleared via power cycle			

NOP stability code watermark set				
src,dst	PC,PC	PC,other	other,PC	PC
MLL	1	31	31	
MLQ				32
halves				32
fulls				32
BPL				32
BMI				32
BZE				32
BNZ				32
AND	1	31	31	
ORR	1	31	31	
XOR	1	31	31	
476	4	124	124	224
All evaluate as nop unless assigned				
Possible extension opcodes * sizes			1428	
There are many other nops. Mainly on src,dest choices				