bits	name		Big Endian Network Order	
3	primary op			
2	dest Addr mode			
3	dest reg			
1	secondary op	quicks and extra	D(1)/F(0) Default is D	
2	size	L is default size		
2	src Addr mode	5	0 equals 32	
3	src reg	quick	branch signed from PC+1	
Addr mode			size	
#00	An	Not CFR src	#00	W
#01	(An)		#01	L
#10	Dn	Not CFR src	#10	Q
#11	Special		#11	D/F
Special				
#000	PC	Not float	Not CFR src	
#001	(PC+)/(-SP)	special write	For PCX subroutine	
#010	IP	Not float	Not CFR src	
#011	(IP+)/(-RP)	special write	For IPX threaded code	
#100	SP	Not float	Not CFR src	
#101	(SP+)/(+SP)	Once (x)(+x) RW	NIP semantics	
#110	RP	Not float	Not CFR src	
#111	(RP+)/(+RP)	Once (x)(+x) RW	NIP semantics	
ops	D		F	
#000	MOV	No dest read	MVQ	quick src args
#001	ADD		ADQ	unsigned 5 bit
#010	MLL	Multiply lower	MLQ	for compact
#011	SUB		SBQ	code
#100	CFR (specials)	No dest read	BPL	quick branch
#101	AND		BMI	0 and -1 do sign
#110	ORR		BZE	of 16 bit
#111	XOR		BNZ	displacement
D/F ops (size)	D/F			
#000	FDV	Divide		
#001	FAD			
#010	FML			
#011	FSB			
#100	FBP	quick branch		
#101	FBM	0 and 1 do sign		
#110	FBD	of 16 bit	Branch denormal zero	

#111	FBI	displacement	Branch infinity	

CFR src				
An	halves			
Dn	fulls			
PC	PCX	fast exchange		
IP	IPX	of registers		
SP	SPX	improves code		
RP	RPX	good stuff		
The src MUST be an address for CFR				
halves An				
Blocks of 8	B,W,L = half		F	
#000	EXH	Exchange	DTF	Double to float
#001	SXL	Sign extend low	FTD	Float to double
#010	INU	Increase upper	FIR	Float Inv root
#011	DCU	Decrease upper	FAT	Float ATN
#100	SLT	Shift left Q half	FEX	Float EXP
#101	SRT	Shift right Q half	FLN	Float LN
#110	ADU	Add upper	FSN	Float SIN
#111	SBU	Subtract upper	FCS	Float COS
fulls Dn				
Blocks of 8	W,L,Q		D	
#000	ABS	Absolute	DTQ	Double to quad
#001	SGN	Sign to 0 or -1	QTD	Quad to double
#010	NOT	Not	FIR	Double Inv root
#011	CPL	Complement	FAT	Double ATN
#100	LOR	Any set = -1	FEX	Double EXP
#101	LAN	Any clear = 0	FLN	Double LN
#110	ASR	Arith shift right	FSN	Double SIN
#111	ROR	Rotate right	FCS	Double COS

D (dst\src)	PC vectors	IP	SP	RP	
PC	BRK		Reserved extension opcodes		
IP	TRP		8 * 8 = 64		
SP	HPR (P)	supervisor (P)			
RP	CIV (H)	hypervisor (H)			
F	PC	IP	SP	RP	
PC	COM (0 to 31)	User opcode	Reserved vector prefix opcodes		
IP	compressed	extensions	8 * 8 = 64		
SP	pair	eval as nop			
RP	extensions	if not used (32)			
register D	PC	IP	SP	RP	
is src	FCN (float constant)				
is dest	@BRK	@TRP (P)	@HVR (H)	@CIV (H)	Set d64
register F	PC	IP	SP	RP	
is src	FCN (float constant)				
is dest	@COM				Set d32
Blocks of 8	supervisor (P)		hypervisor (H)		
#000	SNP	super nop	HNP	hyper nop	
#001	SUP	set user PT d64	SSP	set super PT d64	
#010	EIN	enable interrupt	EVM	enable virt mem	
#011	DIN	disable interrupt	DVM	disable virt mem	
#100	WTI	await interrupt	CLI	clear interrupt	
#101	CLS	clear supervisor	CLH	clear hypervisor	
#110	RSS	reset super	RSH	reset hyper	
#111	SIL	illegal super	HIL	illegal hyper	
HPR is hypervisor trap					
BRK is user mode breakpoint trap					
CIV is set call interrupt vector (interrupt 0 is page fault)					
SUP and SSP followed by d64 immediate					
COM instruction pairs last can be tail recursive					
COM first can not be					
This makes (@COM n COM m d16) a spare opcode space					

src,dst	PC,PC	PC,other	other,PC	PC
MLL	WTO group		31	
MLQ				32
halves				32
fulls				32
BPL				32
BMI				32
BZE				32
BNZ				32
AND		32	31	
ORR		32	31	
XOR		32	31	
444	96	0	124	224
All evaluate as nop unless assigned				
Possible extension opcodes				
	W	L	Q	D/F
WTO group	WTO			
WTO is write target override for src,dst to src,src,wtodst of next instruction				

(@COM n (COM m d16)) spare opcode space				
#nnn11nn0 011ssss opcode form points to				
#mmm11mm0 011000				
#dddddddd dddddddd				
Difficult to use directly				
Only first of pair, branches delay second as delay slot.				
Second after branch may or may not speculative execute and commit				
Allow setting up and special COM?				
#mmm11mm0 011000				
#dddddddd dddddddd		is the instruction replaced by profile COM		
mmm	profile counter number to increase			
mm	recall to register except PC			
If register is PC just increment profile counter				
Any immediates are ordered in the main instruction stream				
(BRK/TRP/HPR/CIV m d16) spare opcode space				
#mmm11mm0 111000				
#dddddddd dddddddd				