VLSI Project Report

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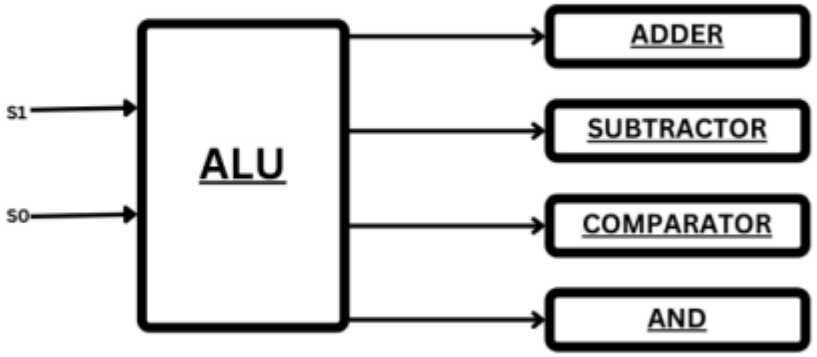
The project required ALU Design that can perform a 4-Bit addition, subtraction, comparison, ANDing.
The complete Design Process was accomplished using Verilog,NGSpice and MAGIC.
The Spice files were used to calculate the maximum delay possible in the circuit using a python script.

The Pre-Layout Process required implementing the ALU in Verilog and NGSpice.
The Post-Layout Process required us to implement the whole circuit in MAGIC and compare our results.

Block Diagram:-

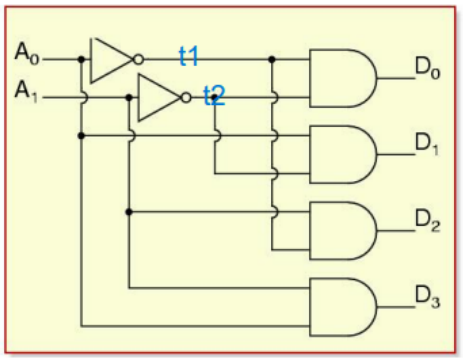


Decoder:-

Here ALU block acts as router to out computational circuit. The operations that needed to be done by ALU is as follows

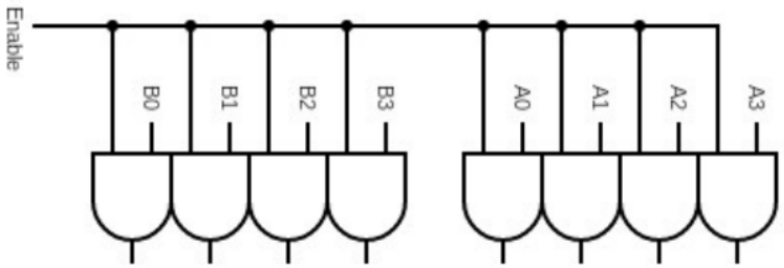
S1	S0	operation
0	0	Add
0	1	Subtract
1	0	Compare
1	1	And

To establish this, we can use a 2-4 decoder.



Enable Block:

This is made-up of 8 AND gates whose main purpose is send our values A3A2A1A1, B3B2B1B0 to their respective block if enable is 1 else 0.



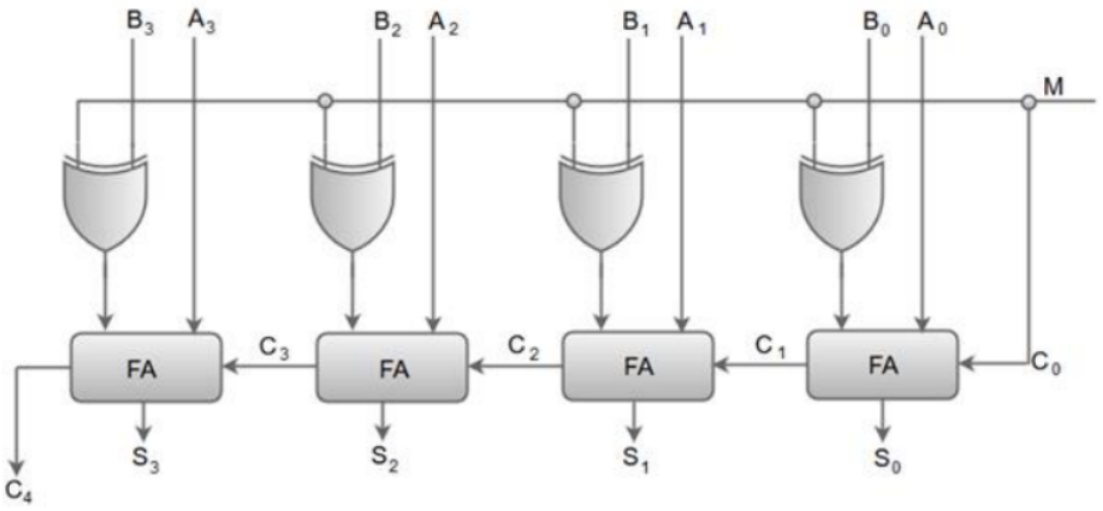
Adder/Subtractor:

Here instead of making a separate Adder and Subtractor we can use a single block which can both act as adder and subtractor. So here we can tie out C0/M wite to S0 directly which would give us an ADDER if input is 00 and a SUBTRACTOR if out input is 01.

Adder operation is A3A2A1A1+ B3B2B1B0

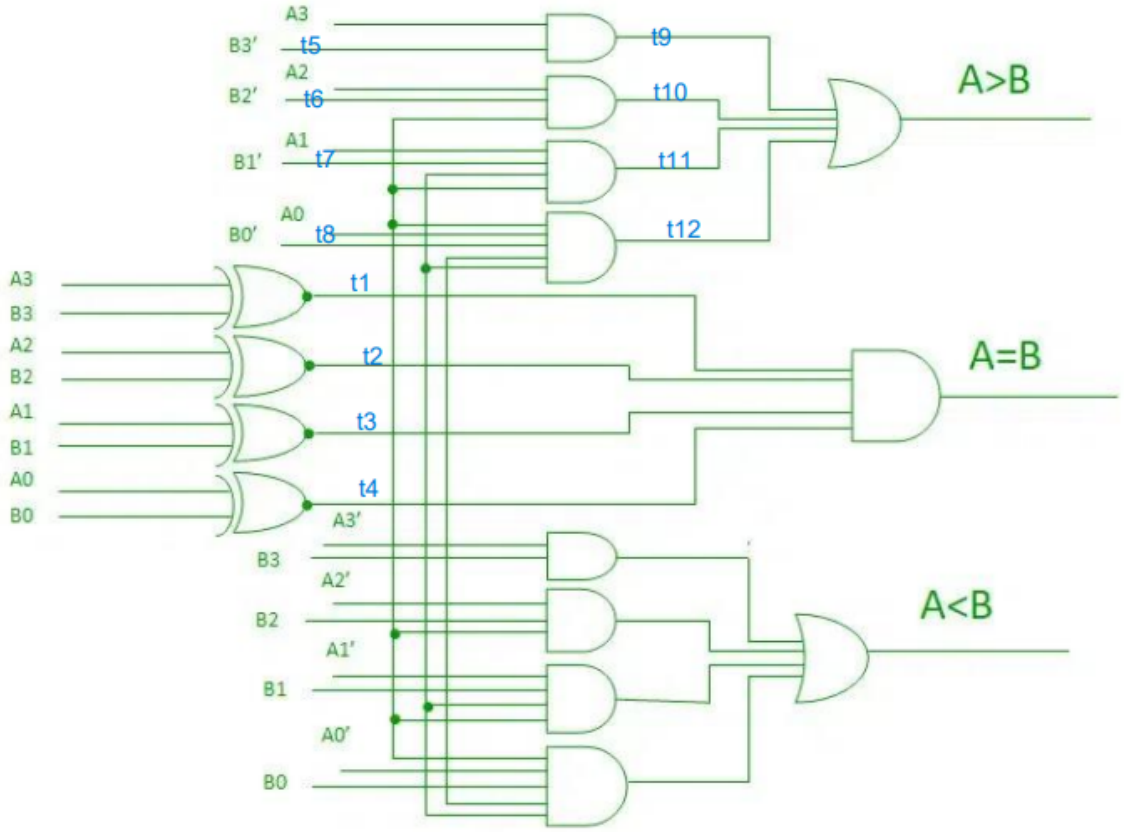
Subtractor operation is A3A2A1A1- B3B2B1B0

4 bit adder-subtractor:



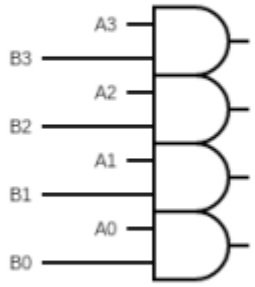
Comparator:

This block would compare our 4-Bit number and give result whether A3A2A1A1 is greater than or less than or equal to B3B2B1B0.



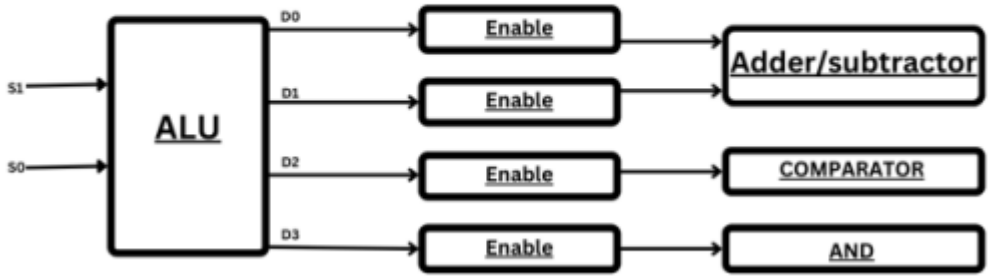
AND Block:

This block Performs AND operation on A3&B3; A0&B0; A1&B1; A0&B0.



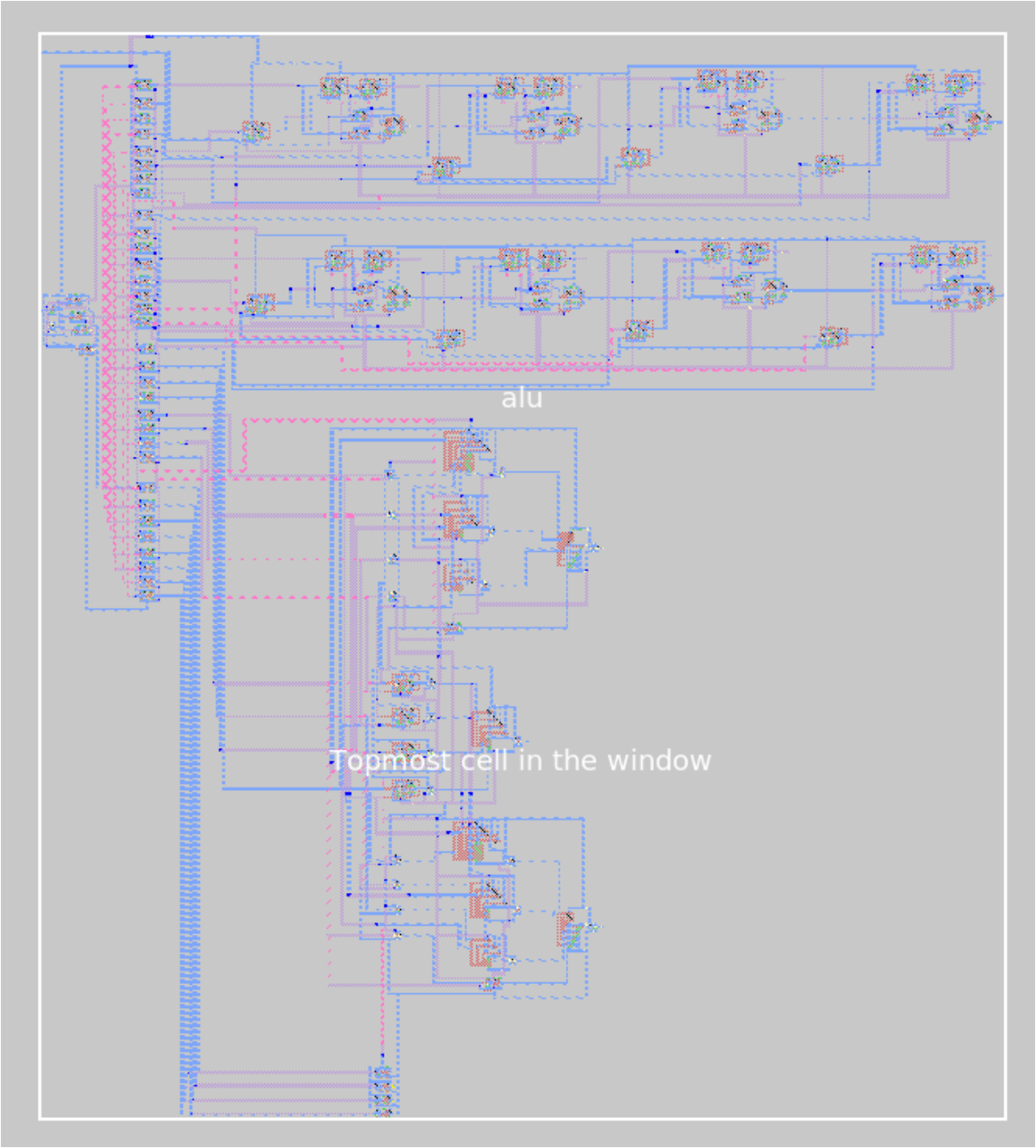
Combining all these blocks would give us our ALU.

The final design included would be as follows;

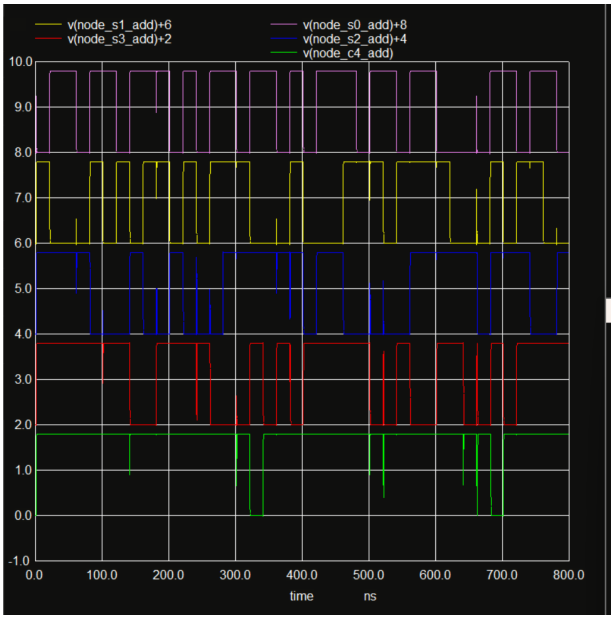


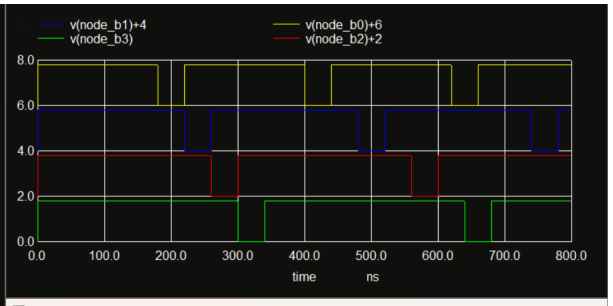
MAGIC:-

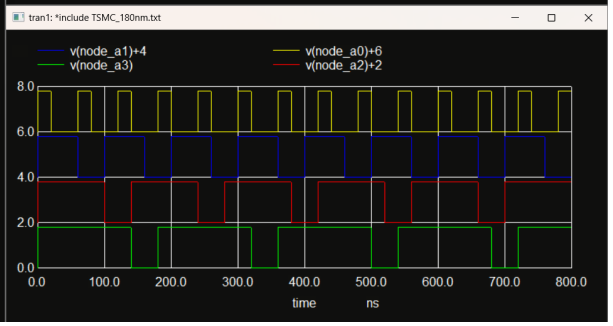
Final ALU Design:-

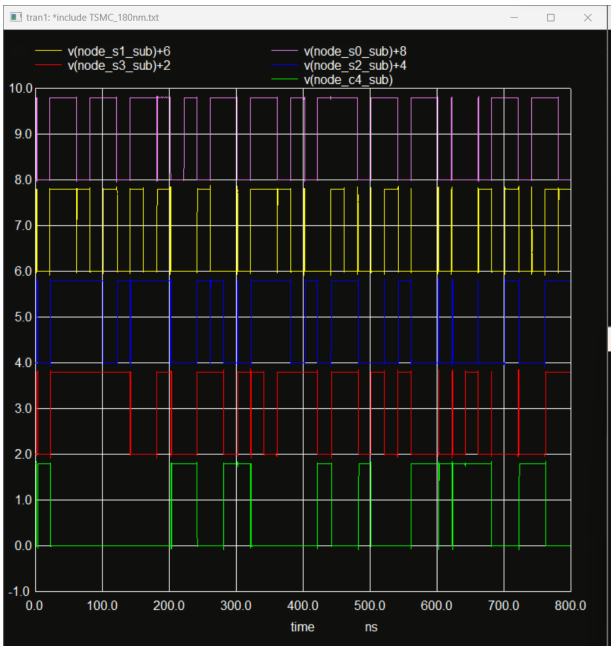


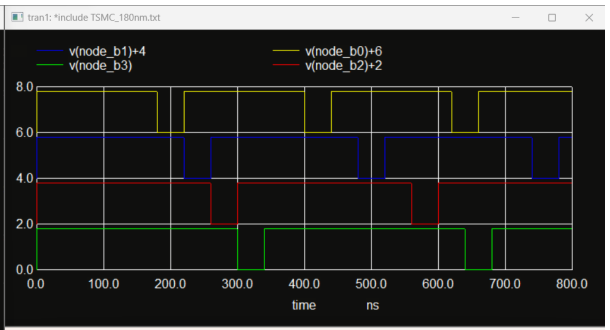
NGSpice:-

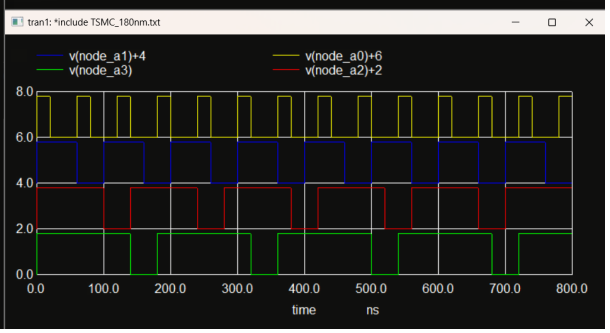

v(node_s1_add)+6
v(node_s3_add)+2
v(node_s0_add)+8
v(node_s2_add)+4
v(node_c4_add)
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
time
ns

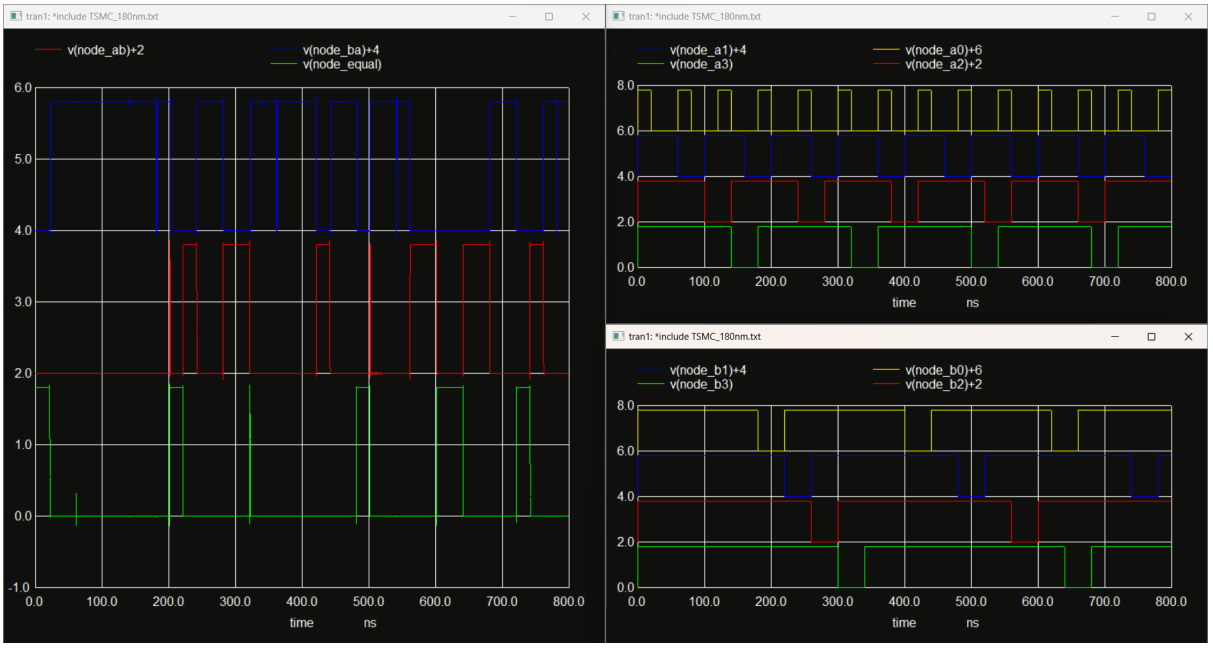

v(node_b1)+4
v(node_b3)
v(node_b0)+6
v(node_b2)+2
8.0
6.0
4.0
2.0
0.0
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
time
ns

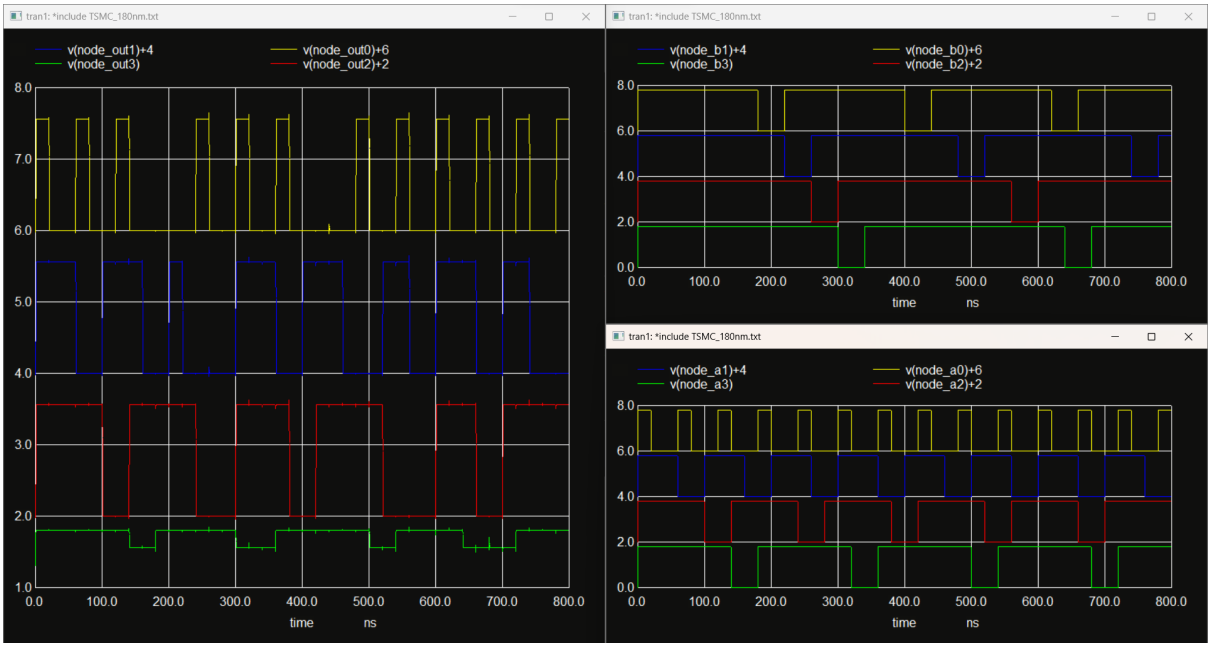

tran1: *include TSMC_180nm.txt
v(node_a1)+4
v(node_a3)
v(node_a0)+6
v(node_a2)+2
8.0
6.0
4.0
2.0
0.0
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
time
ns


tran1: *include TSMC_180nm.txt
v(node_s1_sub)+6
v(node_s3_sub)+2
v(node_s0_sub)+8
v(node_s2_sub)+4
v(node_c4_sub)
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
time
ns

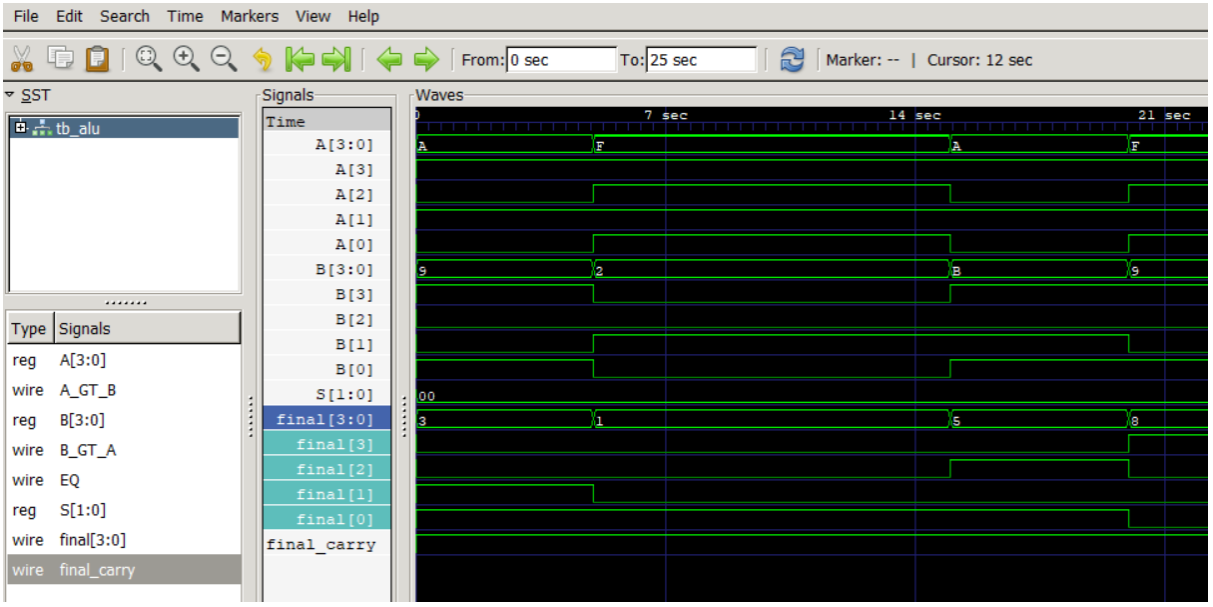

tran1: *include TSMC_180nm.txt
v(node_b1)+4
v(node_b3)
v(node_b0)+6
v(node_b2)+2
8.0
6.0
4.0
2.0
0.0
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
time
ns

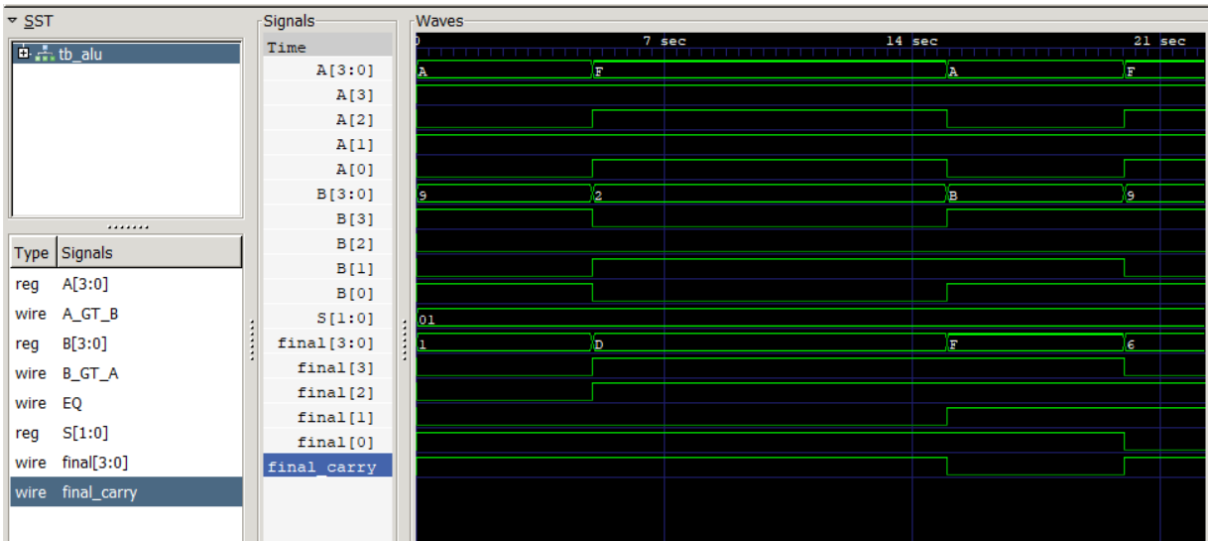

tran1: *include TSMC_180nm.txt
v(node_a1)+4
v(node_a3)
v(node_a0)+6
v(node_a2)+2
8.0
6.0
4.0
2.0
0.0
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
time
ns

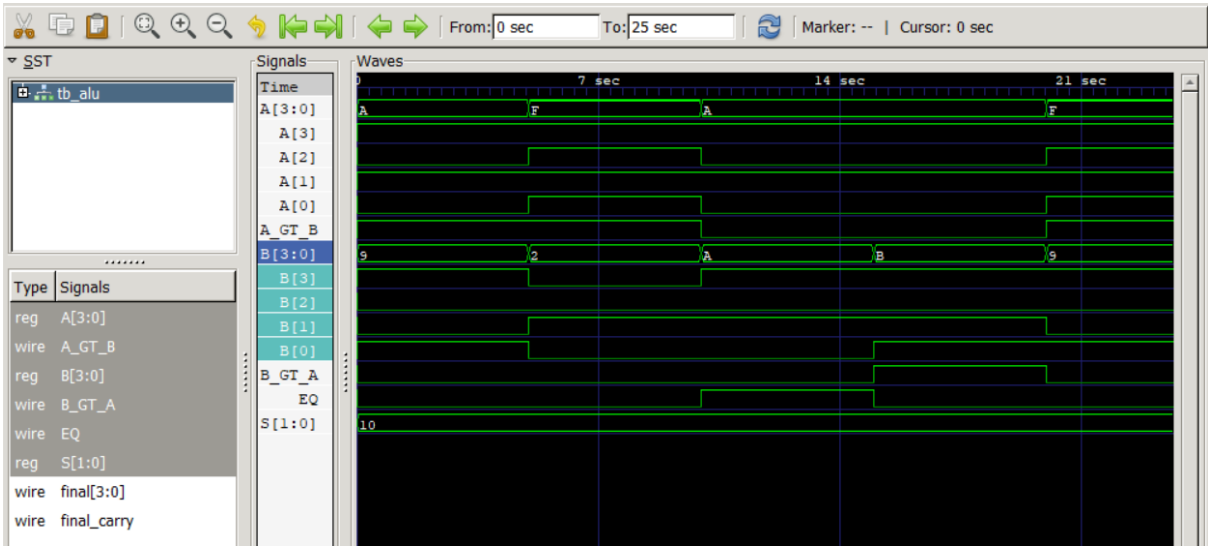

tran1: *include TSMC_180nm.txt
v(node_ab)+2
v(node_ba)+4
v(node_equal)
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
time
ns
tran1: *include TSMC_180nm.txt
v(node_a1)+4
v(node_a3)
v(node_a0)+6
v(node_a2)+2
8.0
6.0
4.0
2.0
0.0
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
time
ns
tran1: *include TSMC_180nm.txt
v(node_b1)+4
v(node_b3)
v(node_b0)+6
v(node_b2)+2
8.0
6.0
4.0
2.0
0.0
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
time
ns

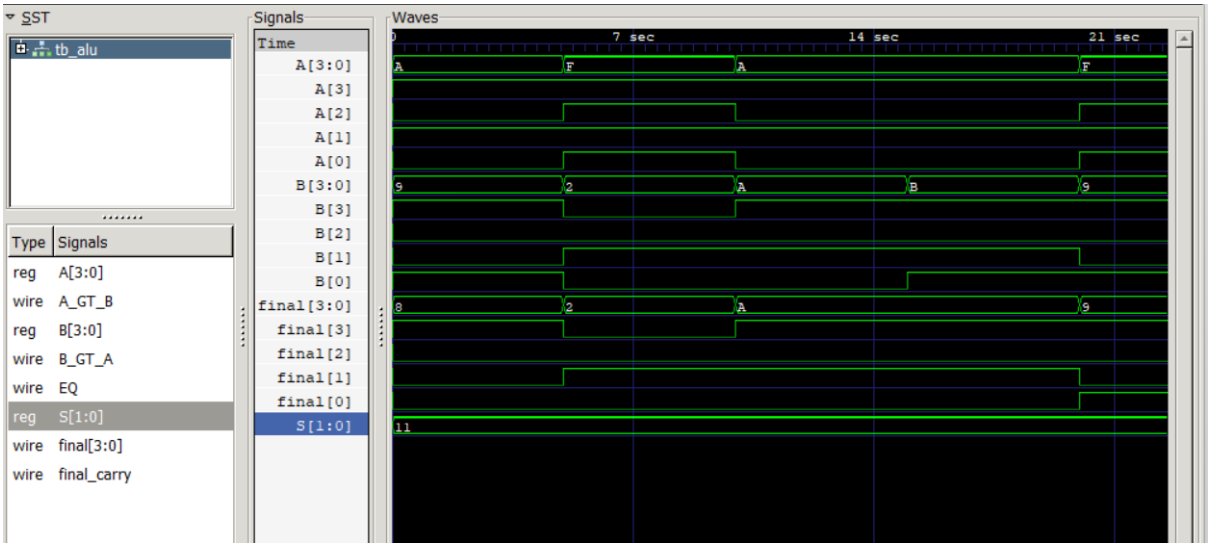

tran1: *include TSMC_180nm.txt
v(node_out1)+4
v(node_out3)
v(node_out0)+6
v(node_out2)+2
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
time
ns
tran1: *include TSMC_180nm.txt
v(node_b1)+4
v(node_b3)
v(node_b0)+6
v(node_b2)+2
8.0
6.0
4.0
2.0
0.0
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
time
ns
tran1: *include TSMC_180nm.txt
v(node_a1)+4
v(node_a3)
v(node_a0)+6
v(node_a2)+2
8.0
6.0
4.0
2.0
0.0
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
time
ns

Verilog:-


File Edit Search Time Markers View Help
From: 0 sec
To: 25 sec
Marker: --
Cursor: 12 sec
SST
tb_alu
Type Signals
reg A[3:0]
wire A_GT_B
reg B[3:0]
wire B_GT_A
wire EQ
reg S[1:0]
wire final[3:0]
wire final_carry
Signals
Time
A[3:0]
A[3]
A[2]
A[1]
A[0]
B[3:0]
B[3]
B[2]
B[1]
B[0]
S[1:0]
final[3:0]
final[3]
final[2]
final[1]
final[0]
final_carry
Waves
7 sec
14 sec
21 sec


SST
tb_alu
Type Signals
reg A[3:0]
wire A_GT_B
reg B[3:0]
wire B_GT_A
wire EQ
reg S[1:0]
wire final[3:0]
wire final_carry
Signals
Time
A[3:0]
A[3]
A[2]
A[1]
A[0]
B[3:0]
B[3]
B[2]
B[1]
B[0]
S[1:0]
final[3:0]
final[3]
final[2]
final[1]
final[0]
final_carry
Waves
7 sec
14 sec
21 sec





Some of the problems faced during the course of the project were getting familiarised with the new technology that is Verilog, NGSpice and MAGIC.
Verilog required us to check for every block using the testbench module, which at first was a little hard to write.
In NGSpice, there were multiple nodes to be dealt with, which sometimes caused problems.
Doing MAGIC was a time consuming process and a little cumbersome.

There were problems with overlaps and metal contacts which had to be fixed. Also some warnings were introduced which had to be removed too.

Delay Analysis:-

Comparator:-

output1.txt

```
1   tpd                    =  8.32121e-10 input = a0 output = out0
2   tpd                    =  1.22075e-09 input = a0 output = out1
3   tpd                    =   failed input = a0 output = out2
4   tpd                    =  8.32121e-10 input = a1 output = out0
5   tpd                    =  1.22075e-09 input = a1 output = out1
6   tpd                    =   failed input = a1 output = out2
7   tpd                    =  8.32121e-10 input = a2 output = out0
8   tpd                    =  1.22075e-09 input = a2 output = out1
9   tpd                    =   failed input = a2 output = out2
0   tpd                    =  8.32121e-10 input = a3 output = out0
1   tpd                    =  1.22075e-09 input = a3 output = out1
2   tpd                    =   failed input = a3 output = out2
3   tpd                    =   failed input = b0 output = out0
4   tpd                    =  1.35770e-09 input = b0 output = out1
5   tpd                    =  8.03218e-10 input = b0 output = out2
6   tpd                    =   failed input = b1 output = out0
7   tpd                    =  1.35770e-09 input = b1 output = out1
8   tpd                    =  8.03218e-10 input = b1 output = out2
9   tpd                    =   failed input = b2 output = out0
0   tpd                    =  1.35770e-09 input = b2 output = out1
1   tpd                    =  8.03218e-10 input = b2 output = out2
2   tpd                    =   failed input = b3 output = out0
3   tpd                    =  1.35770e-09 input = b3 output = out1
4   tpd                    =  8.03218e-10 input = b3 output = out2
5
```

Since I am running the delay part on WSL for complete ALU Design, it takes a lot of time to compute the complete number of delays.

Subtractor:-

```
 1   tpd                    =  1.07943e-09 input = a0 output = s0_sub
 2   tpd                    =  1.02343e-09 input = a0 output = s1_sub
 3   tpd                    =  1.03037e-09 input = a0 output = s2_sub
 4   tpd                    =  1.08245e-09 input = a0 output = s3_sub
 5   tpd                    =  1.07943e-09 input = a1 output = s0_sub
 6   tpd                    =  1.02343e-09 input = a1 output = s1_sub
 7   tpd                    =  1.03037e-09 input = a1 output = s2_sub
 8   tpd                    =  1.08245e-09 input = a1 output = s3_sub
 9   tpd                    =  1.07943e-09 input = a2 output = s0_sub
10   tpd                    =  1.02343e-09 input = a2 output = s1_sub
11   tpd                    =  1.03037e-09 input = a2 output = s2_sub
12   tpd                    =  1.08245e-09 input = a2 output = s3_sub
13   tpd                    =  1.07943e-09 input = a3 output = s0_sub
14   tpd                    =  1.02343e-09 input = a3 output = s1_sub
15   tpd                    =  1.03037e-09 input = a3 output = s2_sub
16   tpd                    =  1.08245e-09 input = a3 output = s3_sub
17   tpd                    =  1.48440e-09 input = b0 output = s0_sub
18   tpd                    =  1.49332e-09 input = b0 output = s1_sub
19   tpd                    =  -8.27840e-09 input = b0 output = s2_sub
20   tpd                    =  -7.97400e-09 input = b0 output = s3_sub
21   tpd                    =  1.48440e-09 input = b1 output = s0_sub
22
```

AND_Block:-

output3.txt

```
1   tpd                    =  5.03069e-10 input = a0 output = out0
2   tpd                    =  5.06214e-10 input = a0 output = out1
3   tpd                    =  5.15741e-10 input = a0 output = out2
4   tpd                    =  4.97265e-10 input = a0 output = out3
5   tpd                    =  5.03069e-10 input = a1 output = out0
6   tpd                    =  5.06214e-10 input = a1 output = out1
7   tpd                    =  5.15741e-10 input = a1 output = out2
8   tpd                    =  4.97265e-10 input = a1 output = out3
9   tpd                    =  5.03069e-10 input = a2 output = out0
0   tpd                    =  5.15741e-10 input = a1 output = out2
1
```

ADDER:-

```
1   tpd                 =  1.19317e-09 input = a0 output = s0_add
2   tpd                 =  1.22218e-09 input = a0 output = s1_add
3   tpd                 =  1.20548e-09 input = a0 output = s2_add
4   tpd                 =  1.20397e-09 input = a0 output = s3_add
5   tpd                 =  1.19317e-09 input = a1 output = s0_add
6   tpd                 =  1.22218e-09 input = a1 output = s1_add
7   tpd                 =  1.20548e-09 input = a1 output = s2_add
8   tpd                 =  1.20397e-09 input = a1 output = s3_add
9   tpd                 =  1.19317e-09 input = a2 output = s0_add
10  tpd                 =  1.22218e-09 input = a2 output = s1_add
11  tpd                 =  1.20548e-09 input = a2 output = s2_add
12  tpd                 =  1.20397e-09 input = a2 output = s3_add
13  tpd                 =  1.19317e-09 input = a3 output = s0_add
14  tpd                 =  1.22218e-09 input = a3 output = s1_add
15  tpd                 =  1.20548e-09 input = a3 output = s2_add
16  tpd                 =  1.20397e-09 input = a3 output = s3_add
17  tpd                 =  1.64660e-09 input = b0 output = s0_add
18  tpd                 =  1.78520e-09 input = b0 output = s1_add
19  tpd                 =  1.65451e-09 input = b0 output = s2_add
20  tpd                 =  1.60561e-09 input = b0 output = s3_add
21  tpd                 =  1.64660e-09 input = b1 output = s0_add
22  tpd                 =  1.78520e-09 input = b1 output = s1_add
23  tpd                 =  1.65451e-09 input = b1 output = s2_add
24  tpd                 =  1.60561e-09 input = b1 output = s3_add
25
```

Maximum Delay till now is observed in the adder circuit.

Critical path:-
Input b0 to output s1_add