Timer — NE/SA/SE555/SE555C

DESCRIPTION

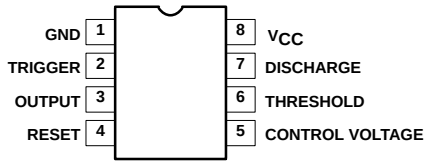
The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

FEATURES

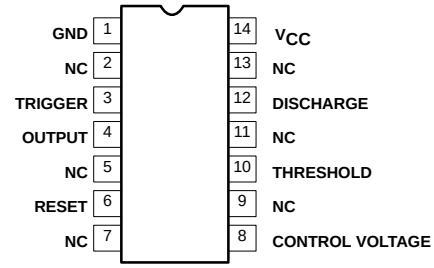
- Turn-off time less than 2µs
- Max. operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

PIN CONFIGURATIONS

D, N, FE Packages



F Package



TOP VIEW

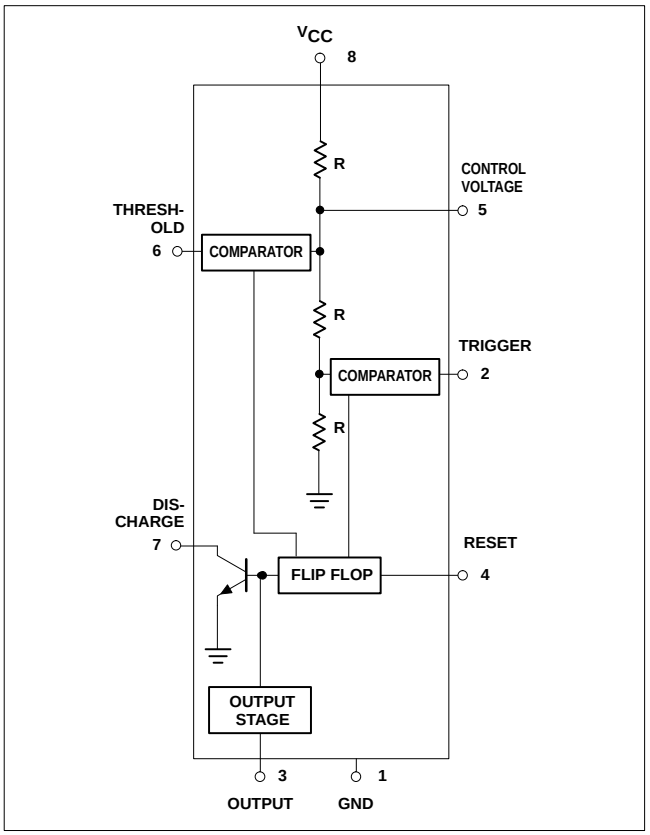
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation

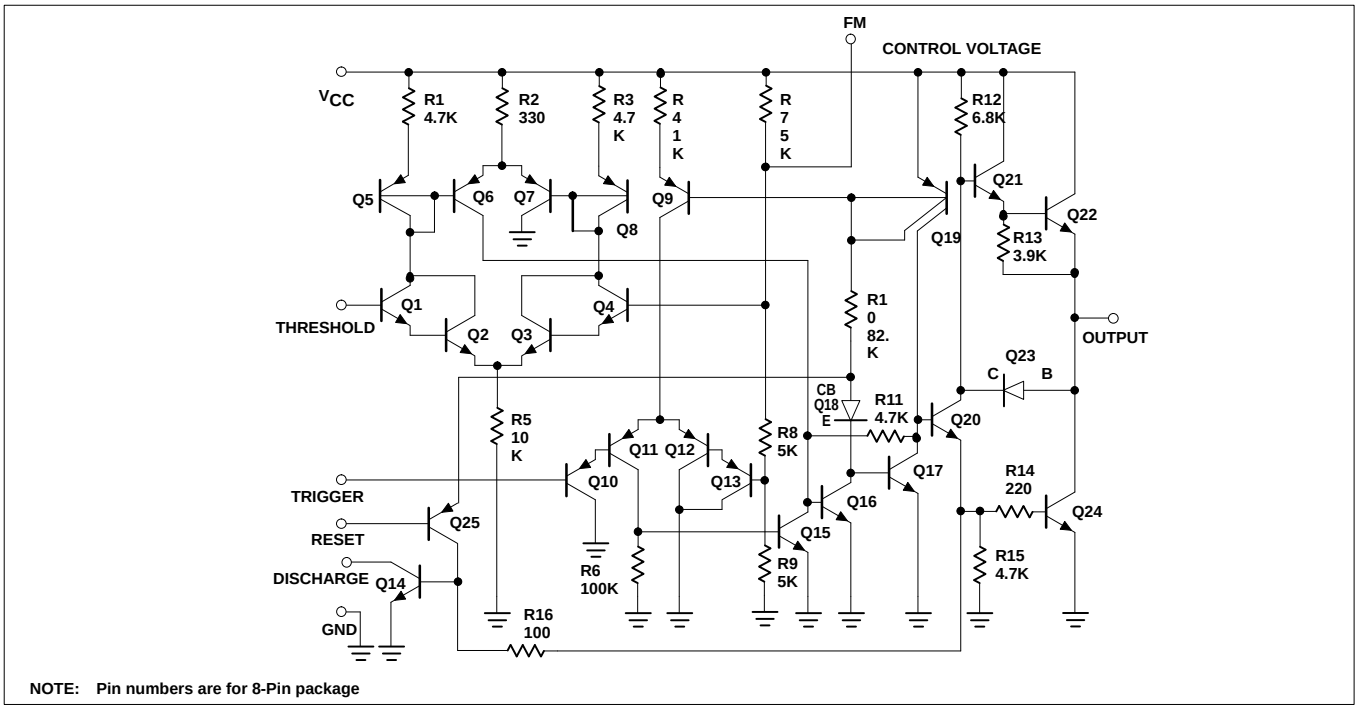
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE555D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE555N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA555N	0404B
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA555D	0174C
8-Pin Hermetic Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CFE	
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555CN	0404B
14-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555N	0405B
8-Pin Hermetic Cerdip	-55°C to +125°C	SE555FE	
14-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CF	0581B

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



NOTE: Pin numbers are for 8-Pin package

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	SE555	+18	V
	NE555, SE555C, SA555	+16	V
P_D	Maximum allowable power dissipation[1]	600	mW
T_A	Operating ambient temperature range		
	NE555	0 to +70	°C
	SA555	-40 to +85	°C
	SE555, SE555C	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

1. The junction temperature must be kept below 125°C for the D package and below 150°C for the FE, N and F packages. At ambient temperatures above 25°C, where this limit would be derated by the following factors:
   D package 160°C/W
   FE package 150°C/W
   N package 100°C/W
   F package 105°C/W

DC AND AC ELECTRICAL CHARACTERISTICS

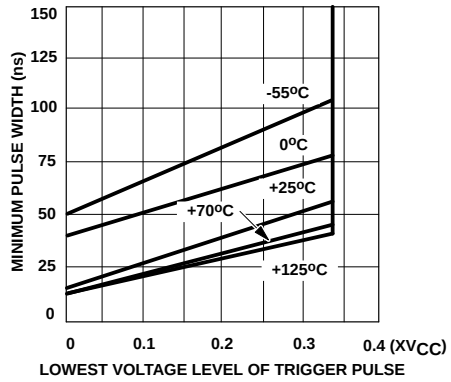
T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low	V_{CC}=5V, R_L=∞		3	5		3	6	mA
	state)[1]	V_{CC}=15V, R_L=∞		10	12		10	15	mA
	Timing error (monostable)	R_A=2kΩ to 100kΩ							
t_M	Initial accuracy[2]	C=0.1μF		0.5	2.0		1.0	3.0	%
$\Delta t_M/\Delta T$	Drift with temperature			30	100		50	150	ppm/°C
$\Delta t_M/\Delta V_S$	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
	Timing error (astable)	R_A, R_B=1kΩ to 100kΩ							
t_A	Initial accuracy[2]	C=0.1μF		4	6		5	13	%
$\Delta t_A/\Delta T$	Drift with temperature	V_{CC}=15V			500			500	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.15	0.6		0.3	1	%/V
V_C	Control voltage level	V_{CC}=15V	9.6	10.0	10.4	9.0	10.0	11.0	V
		V_{CC}=5V	2.9	3.33	3.8	2.6	3.33	4.0	V
V_{TH}	Threshold voltage	V_{CC}=15V	9.4	10.0	10.6	8.8	10.0	11.2	V
		V_{CC}=5V	2.7	3.33	4.0	2.4	3.33	4.2	V
I_{TH}	Threshold current[3]			0.1	0.25		0.1	0.25	μA
V_{TRIG}	Trigger voltage	V_{CC}=15V	4.8	5.0	5.2	4.5	5.0	5.6	V
		V_{CC}=5V	1.45	1.67	1.9	1.1	1.67	2.2	V
I_{TRIG}	Trigger current	V_{TRIG}=0V		0.5	0.9		0.5	2.0	μA
V_{RESET}	Reset voltage[4]	V_{CC}=15V, V_{TH} =10.5V	0.3		1.0	0.3		1.0	V
I_{RESET}	Reset current	V_{RESET}=0.4V		0.1	0.4		0.1	0.4	mA
	Reset current	V_{RESET}=0V		0.4	1.0		0.4	1.5	mA
V_{OL}	Output voltage (low)	V_{CC}=15V							
		I_{SINK}=10mA		0.1	0.15		0.1	0.25	V
		I_{SINK}=50mA		0.4	0.5		0.4	0.75	V
		I_{SINK}=100mA		2.0	2.2		2.0	2.5	V
		I_{SINK}=200mA		2.5			2.5		V
		V_{CC}=5V							
		I_{SINK}=8mA		0.1	0.25		0.3	0.4	V
		I_{SINK}=5mA		0.05	0.2		0.25	0.35	V
V_{OH}	Output voltage (high)	V_{CC}=15V							
		I_{SOURCE}=200mA		12.5			12.5		V
		I_{SOURCE}=100mA	13.0	13.3		12.75	13.3		V
		V_{CC}=5V							
		I_{SOURCE}=100mA	3.0	3.3		2.75	3.3		V
t_{OFF}	Turn-off time[5]	V_{RESET}=V_{CC}		0.5	2.0		0.5	2.0	μs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

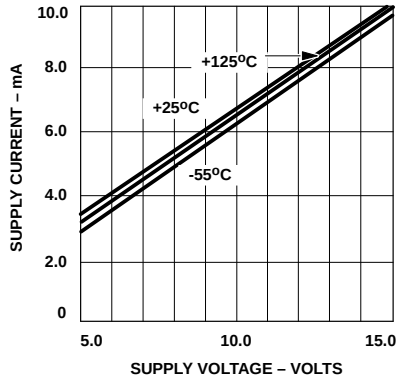
NOTES:
1. Supply current when output high typically 1mA less.
2. Tested at V_{CC}=5V and V_{CC}=15V.
3. This will determine the max value of R_A+R_B, for 15V operation, the max total R=10MΩ, and for 5V operation, the max. total R=3.4MΩ.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to 0.8×V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS

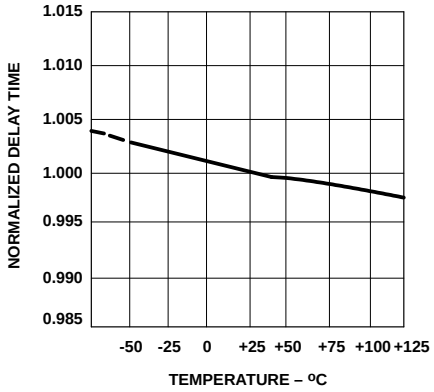
Minimum Pulse Width Required for Triggering



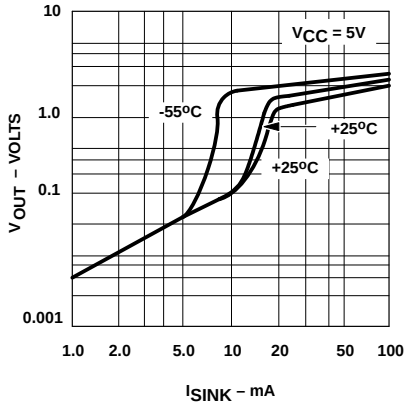
Supply Current vs Supply Voltage



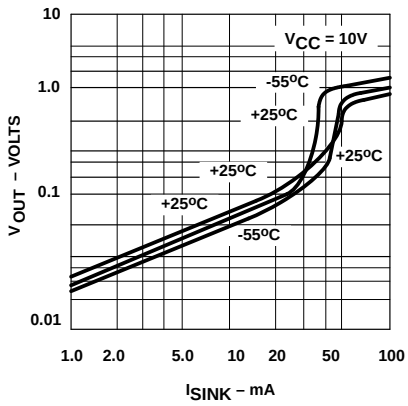
Delay Time vs Temperature



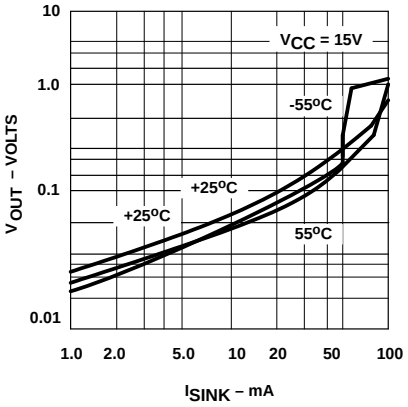
Low Output Voltage vs Output Sink Current



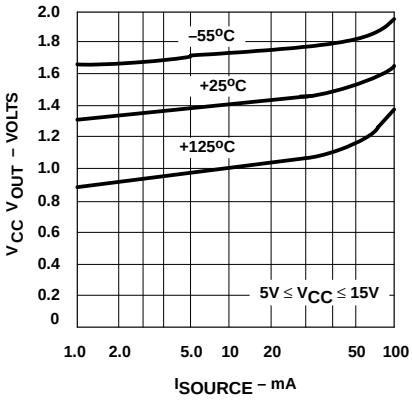
Low Output Voltage vs Output Sink Current



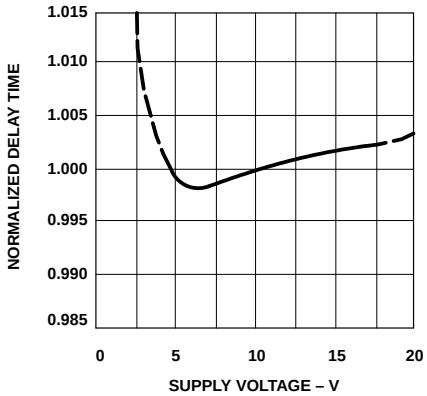
Low Output Voltage vs Output Sink Current



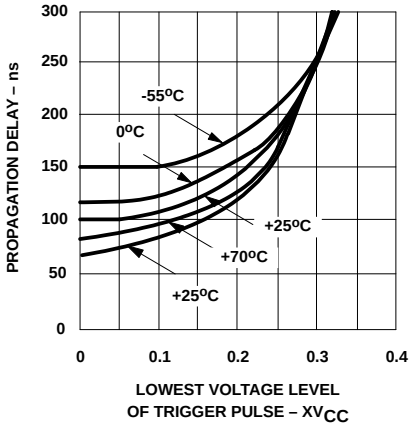
High Output Voltage Drop vs Output Source Current



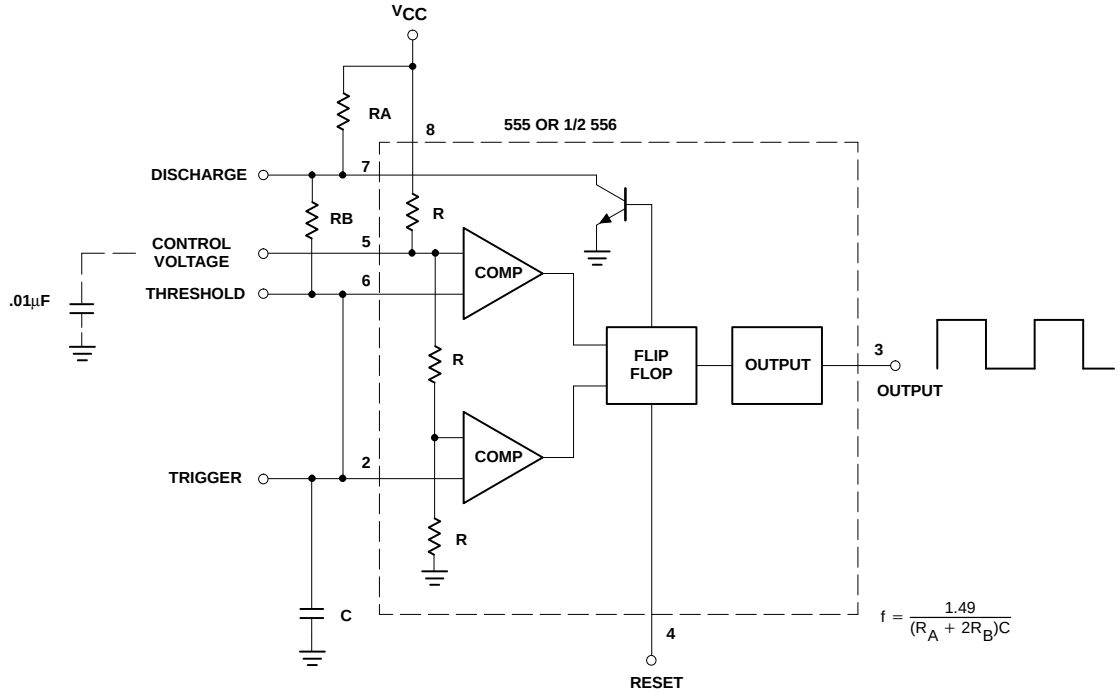
Delay Time vs Supply Voltage



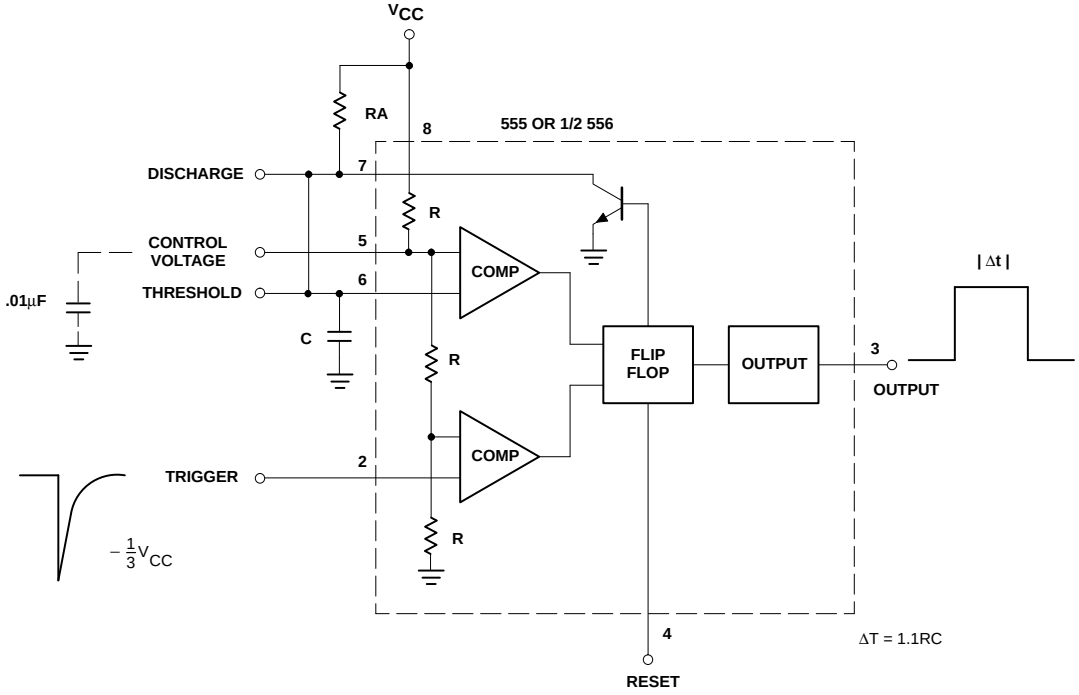
Propagation Delay vs Voltage Level of Trigger Pulse



TYPICAL APPLICATIONS



Astable Operation



Monostable Operation

TYPICAL APPLICATIONS

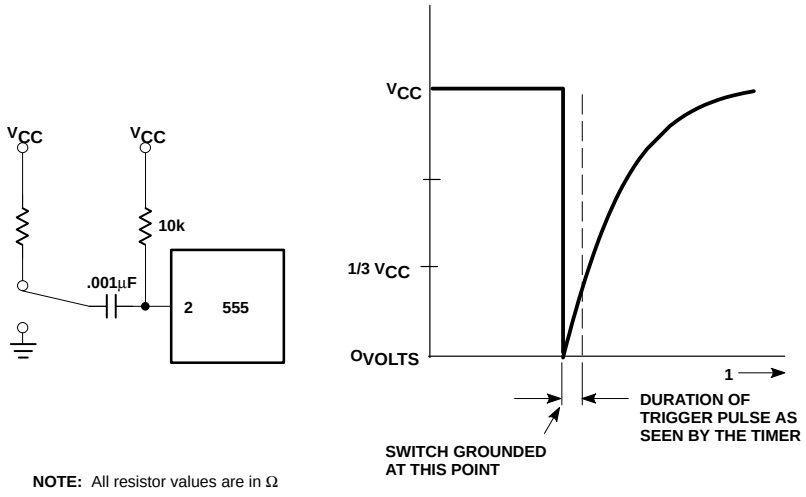


Figure 1. AC Coupling of the Trigger Pulse

Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 1, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bi-stable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the “turn-off time”. This is the measurement of the amount of time required after the threshold reaches 2/3 V_{CC} to turn the output low. To explain further, Q_1 at the threshold input turns on after reaching 2/3 V_{CC}, which then turns on Q_5, which turns on Q_6. Current from Q_6 turns on Q_{16} which turns Q_{17} off. This allows current from Q_{19} to turn on Q_{20} and Q_{24} to given an output low. These steps cause the 2µs max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low, Q_{10} is on and turns on Q_{11} which turns on Q_{15}. Q_{15} turns off Q_{16} and allows Q_{17} to turn on. This turns off current to Q_{20} and Q_{24}, which results in output high. When the trigger is released, Q_{10} and Q_{11} shut off, Q_{15} turns off, Q_{16} turns on and the circuit then follows the same path and time delay explained as “turn off time”. This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.