

Lab 3

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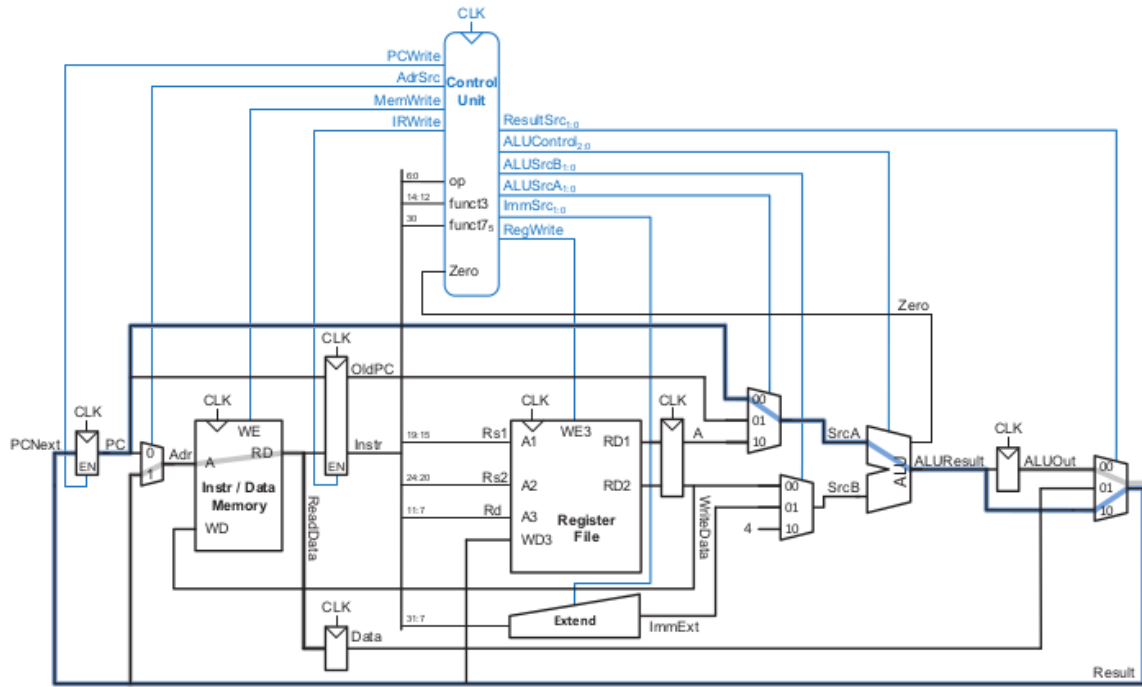
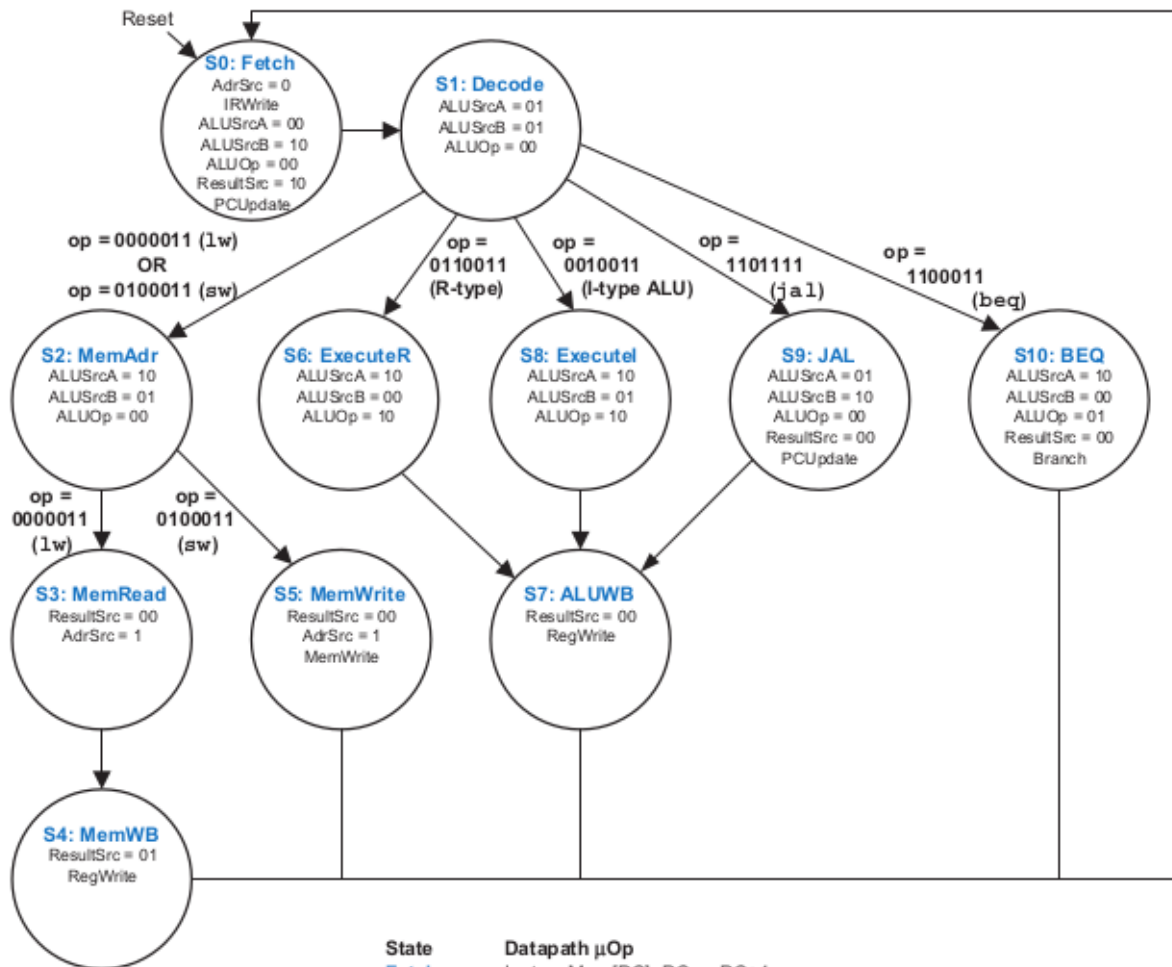


Figure 7.46 Multicycle processor potential critical paths



State	Datapath μ Op
Fetch	Instr \leftarrow Mem[PC]; PC \leftarrow PC+4
Decode	ALUOut \leftarrow PCTarget
MemAdr	ALUOut \leftarrow rs1 + imm
MemRead	Data \leftarrow Mem[ALUOut]
MemWB	rd \leftarrow Data
MemWrite	Mem[ALUOut] \leftarrow rd
ExecuteR	ALUOut \leftarrow rs1oprs2
Executel	ALUOut \leftarrow rs1opimm
ALUWB	rd \leftarrow ALUOut
BEQ	ALUResult = rs1-rs2; if Zero, PC = ALUOut
JAL	PC = ALUOut; ALUOut = PC+4

Figure 7.45 Complete multicycle control FSM

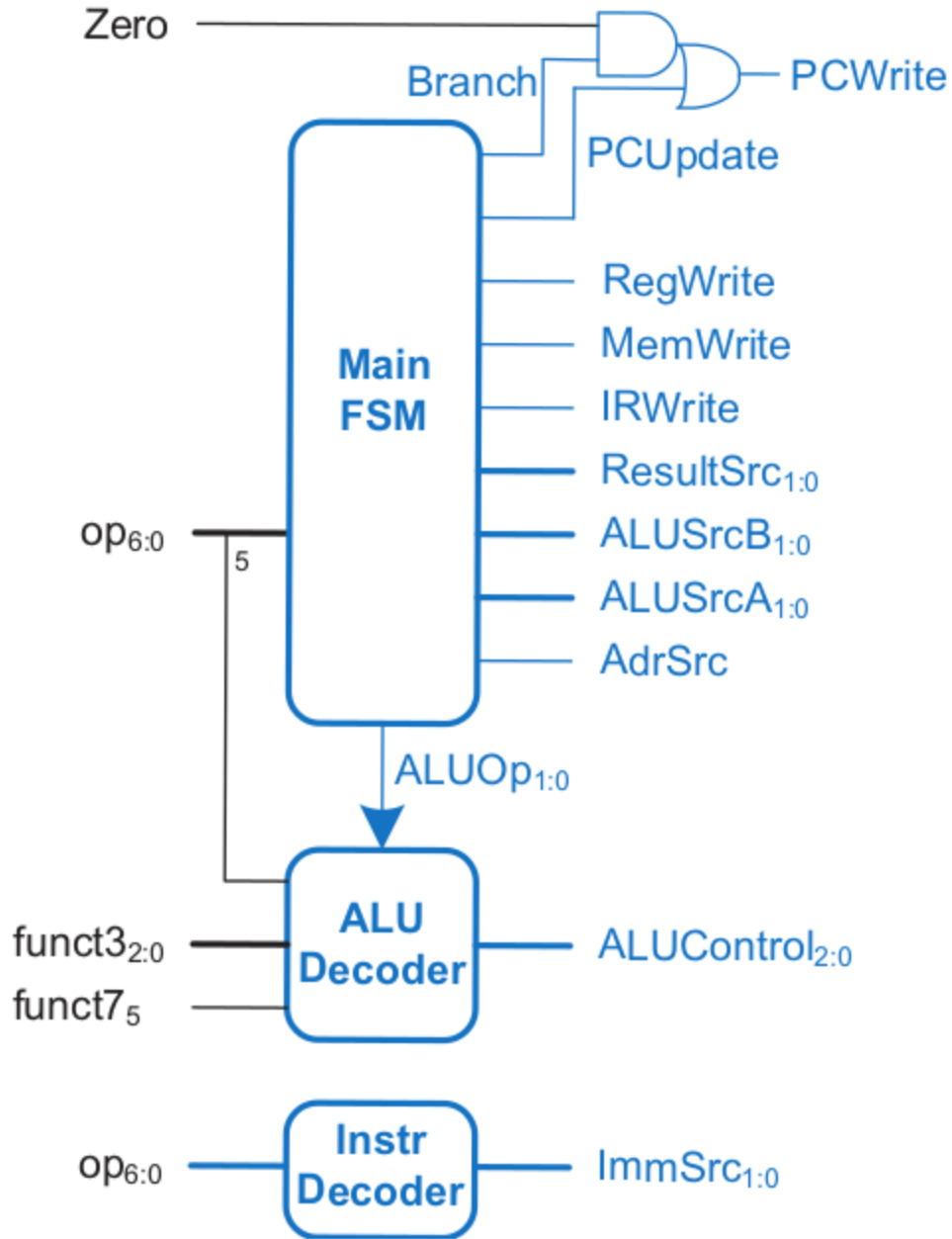


Table 7.5 *ImmSrc* encoding.

ImmSrc	ImmExt	Type	Description
00	{{20{Instr[31]}}, Instr[31:20]}	I	12-bit signed immediate
01	{{20{Instr[31]}}, Instr[31:25], Instr[11:7]}	S	12-bit signed immediate
10	{{20{Instr[31]}}, Instr[7], Instr[30:25], Instr[11:8], 1'b0}	B	13-bit signed immediate
11	{{12{Instr[31]}}, Instr[19:12], Instr[20], Instr[30:21], 1'b0}	J	21-bit signed immediate