A data-sheet for your CPU, consisting of **at most 4 A4 pages**.

Overall Architecture of CPU

1. Summary of Architecture
   1. We implemented the MIPS ISA with a bus architecture that is compliant with Intel’s Avalon bus interface as to make it possible to synthesize our CPU onto an FPGA
2. Diagram of Architecture
   1. Diagram

      Description automatically generated
3. Summary of Each Module (Talk about components, layman language,  highlight clever/important feature decisions)
   1. ALU
   2. Decode
   3. Next\_Instruction
   4. Load Store
   5. RAM
   6. Registers
4. Area and Timing Summary for “Cyclone IV E ‘Auto’” Quartus

Testing Suite

1. General Approach for Testing
   1. Assembler
   2. Testbench Generated by Bash Scripts
   3. Set of Testbenches (Test many groups of instructions; do many (30-40) small tests, then one or two large testbench with >100 instructions)
2. Flow-chart describing testing flow/approach
3. Explain Testing Logic