London, United Kingdom
krishagrawal112.github.io

Krish Agrawal

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Education

Zürich, Switzerland **ETH Zürich** **Sep 2023 - Jul 2024**

- 1/3 exchange students from Imperial chosen in MSc Electrical Engineering and Information Technology.
- Relevant Coursework: Deep Learning, Advanced Machine Learning, VLSI1: HDL Based Design on FPGAs

London, United Kingdom **Imperial College London** **Oct 2020 - Sep 2023**

- MEng Electronic and Information Engineering (Computer Engineering)
- Grade: 78.34% - On track for 1:1, top 10% of cohort
- Relevant Coursework: Introduction to Machine Learning, Computer Vision, Demystifying Machine Learning, Digital Systems Design, Advanced Computer Architecture, Operations Research

Employment

Undergraduate Researcher **Imperial College London** **Apr 2023 - Sep 2023**

- Undertaking a 6-month Undergraduate Research Opportunity (UROP) supervised by Dr. Christos Bouganis to work on extending fpgaConvNet, a software toolchain for mapping and accelerating convolutional neural networks (CNNs) onto FPGAs.
- Induced Activation Sparsity: Investigating ways to fine-tune pretrained CNNs for more sparsity in a hardware-aware manner.
- Dynamic Scheduling: Exploring new ways to dynamically skip zero-input Multiply-Accumulate operations in hardware to speed up computation.

Hardware/Software Intern **Arm Ltd.** **Jul 2022 - Sep 2022**

- Interned for 12 weeks in the Generic Interrupt Controller (GIC) team of the Systems IP division in Cambridge, United Kingdom.
- Requirement Tracing Testing: Converted the existing requirement-tracing test infrastructure from Shell scripts to a standardized and scalable form using Pytest, a software testing framework for Python.
- Functional Coverage for a Component: Implemented functional coverage in SystemVerilog for the testbench of a block in an upcoming release at the time.

Projects

- **Medical Image Segmentation - UNet:** Used PyTorch to train and test a CNN with a UNet architecture.
- **House Price Prediction - Neural Networks:** Created a library in Python to train and test a fully-connected neural network from scratch. Used PyTorch to train, test, and hyperparameter-tune a network.
- **Arithmetic Accelerator on FPGA:** Designed a digital hardware block in Verilog to compute cosine using CORDIC and integrated it with a NIOSII processor via a custom instruction
- **Image Processor on FPGA for Autonomous Rover:** Implemented an image processing pipeline on a DE10-Lite FPGA Board with RGB-HSV conversion and Gradient Edge-Detection in Verilog.

Awards and Scholarships

- **Dean's List (Year 1 & 2)** (2021, 2022). Awarded to top 10% of the cohort.
- **Departmental Funding** (2023). 1/3 students to receive full-time research funding for 6 months.
- **Swiss-European Mobility Programme Scholarship** (2023) To attend ETH Zürich as an exchange student.

Languages and Technologies

- Python; PyTorch; Verilog/SystemVerilog; C++; Javascript; Chisel/Scala
- Git; Weights and Biases; AWS (DynamoDB); Quartus Prime; ModelSim