TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2078 Bhadra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic *(EX 401)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

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1. Define analog and digital signal. What are the advantages of digital system over analog system? [2+2]
2. Explain BCD, Excess-2 , Gray and ASCII Code with examples. [4×1.5]
3. a) Define SOP and POS form and convert F = A + BC + ABC into its canonical form. [2+2]
4. Simplify Σm (0, 1, 2, 8, 10, 14, 15) d =(3, 7, 11, 13) using k-map, write its standard product of sum expression and realize it using NOR gates only. [4+3]
5. Implement the given function F = Σ (0, 2, 3, 5, 8, 12, 14) using only one 8:1 MUX. Add the binary numbers 1011 and 1101 by using Full adders. [4+3]
6. Design a 3 bit binary multiplier using binary parallel adder (BPA). [6]
7. Find out the simplest logic circuit as far as possible for the 'e' segment of the seven segment display decoder. [6]
8. Convert SR flip-flop to T filp-flop and draw the timing diagram of SR flip flop. [4+2]
9. Describe the operation of 4-bit parallel in serial out shift register with its truth table and timing diagram for a given data sequence 1101. [6]
10. Design a 3-bit Asynchrounous up/down counter with its truth table and explain it working principle. [6]
11. Design a sequential circuit with T flip-flop and two inputs X and Y. If X=1 and Y=0 the circuit goes through 00 to 01 to 11 to 10. When X=Y=1, the circuit goes through the transition from 00 to 10 to 01 to 11. When X = 0 and Y=1, the circuit goes through 00 to 11 to 10 to 00. When X = Y = 0, the circuit 00 to 01 to 10 to 11 and repeats. [12]
12. Define PLA (Programmable Logic Array). Implement the full substractor using PLA. [2+3]
13. Design and describe 24 hr digital clock. [5]

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