TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2076 Ashwin

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic *(EX 401)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt <u>All</u> questions.*
- ✓ *The figures in the margin indicate <u>Full Marks</u>.*
- ✓ *Assume suitable data if necessary.*

1. Differentiate between edge and level triggering system with example.
2. Define Gray Code and convert $(11101)_{\text{Gray code}}$ to binary. When $(FF)_H$ is ANDed with $(CA)_H$ what will be the resulting number.
3. Simplify $F(A, B, C, D) = \Sigma(2, 3, 6, 7, 9, 10, 11)$ and $d = \Sigma(5, 8, 12)$ using K-map. Result in SOP and POS form.
4. Define encoder. Design 4×16 Decoder using 2×4 Decoder only.
5. Explain 2-bit fast Adder with its logical diagram and write the advantage of fast Adder.
6. Explain the operation of J-K flip flop with its logical diagram characteristics table, characteristics equation, excitation table and timing diagram.
7. Explain the 4-bit SISO shift Register with its timing diagram.
8. Design Mod-5 synchronous counter using JK flip flop.
9. Design sequential machine that has one input x and one output z. The machine is required to give output 1 when it contains message 1101 using S-R flip flop.
10. Design 12-Hr. digital clock.
11. Write short notes: (Any two)
    a) Ring counter
    b) Binary parallel Adder
    c) PLA

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