

TRIBHUVAN UNIVERSITY
 INSTITUTE OF ENGINEERING
Examination Control Division
 2080 Baishakh

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic (EX 401)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt All questions.
- ✓ The figures in the margin indicate Full Marks.
- ✓ Assume suitable data if necessary.



1. What is importance of coding? Explain about ASCII code briefly. [1+2]
2. Convert the following number system.
 - a) $(101101.011)_2 = (?)_{10}$
 - b) $(110111)_{\text{gray}} = (?)_2$
 - c) $(524)_8 = (?)_{16}$
 - d) $(125.25)_{10} = (?)_2$[1.5×4]
3. Describe positive and negative logic with an example. Construct Ex-NOR gate using only NOR gates. [2+3]
4. Simplify the following expression using K-map. Express it in SOP format and realize it using NAND gate only. [2+3]
- Y= F(M,N,O,P)= $\sum m(0,1,2,8,12,14,15)+d(5,10,11)$ [4+2]
5. Realize a full-adder circuit using a single 1:4 demultiplexer and logic gates. [5]
6. What is a priority encoder? Find out logic expressions and draw the logic circuit of 4 to 2 priority encoder. [2+4]
7. How can we use flip-flop as a state machine? Convert SR flip-flop to JK flip-flop. [2+5]
8. Differentiate between combinational and sequential logic circuits. Explain the operation of a synchronous decade counter with timing diagrams. [2+6]
9. Describe the logic operation of 4-bit parallel-in serial out shift register with timing diagram of 1011 input data. [6]
10. Design a synchronous mod-5 up-counter using SR flip-flops and draw its timing diagram. [6+2]
11. Design a synchronous machine which has one input, x and one output, z. The output is required to give high when input contains 110 serial message. Implement only JK flip-flops. [10]
12. What is a ROM? Explain it how one bit memory is stored as '1' or '0', based on BJT circuit. [2+4]
13. With the help of block diagram explain the operation of multiplexing display circuit. [4]

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 2079 Bhadra

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Subject: - Digital Logic (EX 401)

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1. Write down the advantages of digital systems. Define BCD and excess-3 codes. [2+4]
2. Perform the following code conversions. [4×1.5]
 - a) $(329.54)_{10} = (?)_{16}$
 - b) $(BD.1A)_{16} = (?)_{10}$
 - c) $(01010111)_{\text{gray}} = (?)_2$
 - d) $(1010 0111)_{\text{excess-3}} = (?)_{\text{BCD}}$
3. Explain the positive and negative logic level of digital system. Show that positive logic level XOR gate is equivalent to negative logic level XNOR gate. [2+3]
4. Simplify the given function using K-map. $F = \sum_m (1,2,3,8,9,10,11,14) + d \sum_m (0,4,12)$. Realize the simplified Boolean function using NAND Gate. [4+2]
5. Realize full-adder using a single 4:1 MUX and logical gates. Design the BCD to seven segment decoder. Obtain the simplest logic expressions for segments "a" and "e" also draw their circuits. [4+6]
6. What is an encoder? Explain 8 to 3 line encoder with circuit diagram and truth table. [1+5]
7. Explain the operation of D flip-flop with necessary diagrams truth tables and make its excitation table. [6]
8. Explain the operation of 4-bit serial-in-parallel out (SIPO) register with timing diagram for the given data pattern 1101. [6]
9. Differentiate between synchronous and asynchronous counters. Design a mod-6 synchronous counter using JK flip-flops. [2+7]
10. A synchronous machine has 1-bit input 'X'. The output 'Y' goes high when input contains the message '101'. Draw the state diagram, derive the transition table (state table), excitation table and design circuit. Use only T flip-flops. [10]
11. What is a memory device? Distinguish between PAL and PLA memory devices. [2+4]
12. With the help of block diagram explain the operation of frequency counter circuit. [4]

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 2078 Bhadra

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Subject: - Digital Logic (EX 401)

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1. Define analog and digital signal. What are the advantages of digital system over analog system? [2+2]
2. Explain BCD, Excess-2, Gray and ASCII Code with examples. [4×1.5]
3. a) Define SOP and POS form and convert $F = A + BC + ABC$ into its canonical form. [2+2]
4. Simplify $\Sigma m(0, 1, 2, 8, 10, 14, 15)$ d = (3, 7, 11, 13) using k-map, write its standard product of sum expression and realize it using NOR gates only. [4+3]
5. Implement the given function $F = \Sigma(0, 2, 3, 5, 8, 12, 14)$ using only one 8:1 MUX. Add the binary numbers 1011 and 1101 by using Full adders. [4+3]
6. Design a 3 bit binary multiplier using binary parallel adder (BPA). [6]
7. Find out the simplest logic circuit as far as possible for the 'e' segment of the seven segment display decoder. [6]
8. Convert SR flip-flop to T filp-flop and draw the timing diagram of SR flip flop. [4+2]
9. Describe the operation of 4-bit parallel in serial out shift register with its truth table and timing diagram for a given data sequence 1101. [6]
10. Design a 3-bit Asynchronous up/down counter with its truth table and explain it working principle. [6]
11. Design a sequential circuit with T flip-flop and two inputs X and Y. If X=1 and Y=0 the circuit goes through 00 to 01 to 11 to 10. When X=Y=1, the circuit goes through the transition from 00 to 10 to 01 to 11. When X = 0 and Y=1, the circuit goes through 00 to 11 to 10 to 00. When X = Y = 0, the circuit 00 to 01 to 10 to 11 and repeats. [12]
12. Define PLA (Programmable Logic Array). Implement the full subtractor using PLA. [2+3]
13. Design and describe 24 hr digital clock. [5]



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2078 Kartik

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Year / Part	I/I	Time	3 hrs.

Subject: - Digital Logic (EX 401)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
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1. List out the advantages of digital signal over the analog signal. [3]
2. Explain ASCII and EBCDIC codes with example. [1.5+1.5]
3. Convert the following number system. [2×2]
 - a) $(5A.B)_{16} = (?)_{\text{Excess-3}}$
 - b) $(1011011)_2 = (?)_{\text{BCD}}$
4. Define universal gates with example. Explain positive and negative logic. [2+2]
5. Design three input exclusive NOR gate using NOR gates only. [3]
6. Given function $F = A(B' + C) + BD$, change into its canonical form. Define max term and min term. [3+2]
7. Simplify the given function using K-map $F = \Pi(0, 1, 4, 7, 8, 10, 11, 12)$ and $D = (2, 3, 6, 9, 15)$ and implement the final expression using NAND gate only. [4+2]
8. Define and design 2-bit binary fast adder. Draw the circuit diagram of full subtractor using half subtractor. [5+2]
9. Implement the given function $F = \Sigma(0, 1, 3, 6, 10, 12, 14)$ using 8×1 MUX only. [4]
10. Define race around condition. What are the limitation of SR flip flop? Convert JK flip flop to SR flip flop. [2+2+4]
11. Mention the application of shift Register. Explain the circuit diagram of 3-bit switched tail ring counter. [2+4]
12. Design the synchronous MOD-6 counter using -ve edge triggered JK flip flop. [6]
13. Design a sequential machine that detects three consecutive zeros from an input data stream x by making output $y=1$. (Use SR flip flop in your design) [10]
14. Differentiate between PROM and PLA. Implement the following boolean functions using PAL. [2+2×2]
 - a) $A(x, y, z) = \Sigma(2, 4, 5, 7)$
 - b) $B(x, y, z) = \Sigma(0, 2, 6)$
15. Explain the operation of digital clock with neat and clean diagram. [5]

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 2076 Chaitra

Exam.	Regular		
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Subject: - Digital Logic (EX 401)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt All questions.
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1. Write the basic difference between analysis and digital signals with examples. [3]
2. Perform the following code conversions. [1.5×4]
 - (i) $(430.25)_8 = (?)_{16}$
 - (ii) $(39.75)_{10} = (?)_8$
 - (iii) $(17)_{10} = (?)_{\text{gray}}$
 - (iv) $(17)_{\text{excess-3}} = (?)_{\text{BCD}}$
3. a) State and prove De-Morgan's laws. [2]
- b) Realize 3 inputs XOR gates using NAND gates only. [3]
4. Define minterms and maxterms. Simplify the following using k-map and implement the result using NOR gates only. [2+4+2]

$$F(A,B,C,D) = \Sigma m(0,1,2,5,8,14) + d(4,10,13)$$
5. Implement 1:16 demultiplexer using 1:2 demultiplexer. [4]
6. What is hazard? Explain types of hazards with hazard cover techniques used in K-map simplification. [1+4]
7. Define excess-3 code with examp. Design a binary to excess-3 code converter circuit using basic gates. [2+5]
8. Differentiate between combinational and sequential circuit. Explain working principle of master slave JK flip-flop. [2+4]
9. Define shift registers with its application. Explain the working principle of 4 bit Ring counter with its timing diagram. [2+5]
10. Design a 3 bit synchronous up counter where the bit combination of each states are in gray system. (Use T-flip-flop in your design.) [8]
11. Using melay circuit with J-K flip-flops design a synchronous sequence detector that produces output $Z=1$ when it detects the serial input $X=010$. [10]
12. Differentiate between RAM and ROM. Implement $F1 = \Sigma(1,2,4,6)$ and $F2 = \Sigma m(0,2,3)$ using PROM. [2+4]
13. What are the applications of digital devices? Explain frequency counter. [1+4]



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2076 Ashwin

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Year / Part	I/I	Time	3 hrs.

Subject: - Digital Logic (EX 401)

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1. Differentiate between edge and level triggering system with example.
2. Define Gray Code and convert (11101)_{Gray code} to binary. When (FF)_H is ANDed with (CA)_H what will be the resulting number.
3. Simplify $F(A, B, C, D) = \Sigma(2, 3, 6, 7, 9, 10, 11)$ and $d = \Sigma(5, 8, 12)$ using K-map. Result in SOP and POS form.
4. Define encoder. Design 4×16 Decoder using 2×4 Decoder only.
5. Explain 2-bit fast Adder with its logical diagram and write the advantage of fast Adder.
6. Explain the operation of J-K flip flop with its logical diagram characteristics table, characteristics equation, excitation table and timing diagram.
7. Explain the 4-bit SISO shift Register with its timing diagram.
8. Design Mod-5 synchronous counter using JK flip flop.
9. Design sequential machine that has one input x and one output z. The machine is required to give output 1 when it contains message 1101 using S-R flip flop.
10. Design 12-Hr. digital clock.
11. Write short notes: (Any two)
 - a) Ring counter
 - b) Binary parallel Adder
 - c) PLA

TRIBHUVAN UNIVERSITY
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 2075 Chaitra

Exam.	REGISTRATION		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic (EX 401)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt All questions.
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1. Write down the advantages and disadvantages of digital signals over analog signals. [4]
2. Convert the following: [1.5×4]
 - a) $(53.125)_{10} = (?)_2$
 - b) $(615)_8 = (?)_{BCD}$
 - c) $(10011)_{Gray} = (?)_8$
 - d) $(11001001)_{excess-3} = (?)_8$
3. State and prove De Morgan's theorem. Design X-NOR gate using anyone of universal gate. [4+2]
4. Simplify the following expressions using K-map and also draw the logical circuit.

$$Y(A, B, C, D) = \Sigma (0, 2, 3, 4, 7, 8, 10, 13) \text{ and}$$

$$d = \Sigma (5, 6, 12)$$

5. Construct the 3-bit magnitude comparator circuit. [5]
6. Implement the following function using 8×1 MUX. [5]

$$F(A, B, C, D) = \Sigma (0, 2, 3, 6, 7, 8, 12, 13, 15)$$
7. Construct Full Adder using half Adder. [4]
8. Explain operation of S-R flip-flop with its logical diagram characteristics table, characteristics equation excitation table and timing diagram. [8]
9. Convert J-K flip flop to S-R flip flop. [6]
10. Explain the working principle of 4-bit parallel in serial out shift register with its timing diagram. [6]
11. Construct an Asynchronous Decade counter. [5]
12. Design a sequential machine that detects 101 from input stream X by making Y is 1. Using J-K flip-flop. [10]
13. What is ROM? Implement given functions $F_1(A, B, C) = \Sigma (2, 3, 5, 6)$ and $F_2(A, B, C) = \Sigma (0, 1, 5)$ using ROM. [1+4]
14. Draw the circuit diagram of frequency counter. [4]
