



TRIBHUVAN UNIVERSITY  
INSTITUTE OF ENGINEERING  
**Examination Control Division**  
2078 Kartik

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	1 / 1	Time	3 hrs.

**Subject: - Digital Logic (EX 401)**

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt **All** questions.
- ✓ The figures in the margin indicate **Full Marks**.
- ✓ Assume suitable data if necessary.

1. List out the advantages of digital signal over the analog signal. [3]
2. Explain ASCII and EBCDIC codes with example. [1.5+1.5]
3. Convert the following number system. [2×2]
  - a)  $(5A.B)_{16} = (?)_{\text{Excess-3}}$
  - b)  $(1011011)_2 = (?)_{\text{BCD}}$
4. Define universal gates with example. Explain positive and negative logic. [2+2]
5. Design three input exclusive NOR gate using NOR gates only. [3]
6. Given function  $F = A(B'+C) + BD$ , change into its canonical form. Define max term and min term. [3+2]
7. Simplify the given function using K-map  $F = \Pi(0,1,4,7,8,10,11,12)$  and  $D = (2,3,6,9,15)$  and implement the final expression using NAND gate only. [4+2]
8. Define and design 2-bit binary fast adder. Draw the circuit diagram of full subtractor using half subtractor. [5+2]
9. Implement the given function  $F = \Sigma(0,1,3,6,10,12,14)$  using  $8 \times 1$  MUX only. [4]
10. Define race around condition. What are the limitation of SR flip flop? Convert JK flip flop to SR flip flop. [2+2+4]
11. Mention the application of shift Register. Explain the circuit diagram of 3-bit switched tail ring counter. [2+4]
12. Design the synchronous MOD-6 counter using -ve edge triggered JK flip flop. [6]
13. Design a sequential machine that detects three consecutive zeros from an input data stream  $x$  by making output  $y=1$ . (Use SR flip flop in your design) [10]
14. Differentiate between PROM and PLA. Implement the following boolean functions using PAL. [2+2×2]
  - a)  $A(x,y,z) = \Sigma(2, 4, 5, 7)$
  - b)  $B(x,y,z) = \Sigma(0, 2, 6)$
15. Explain the operation of digital clock with neat and clean diagram. [5]