TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2079 Bhadra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic (*EX 401*)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Write down the advantages of digital systems. Define BCD and excess-3 codes. [2+4]
2. Perform the following code conversions. [4×1.5]
   a) $(329.54)_{10} = (?)_{16}$
   b) $(BD.1A)_{16} = (?)_{10}$
   c) $(01010111)_{gray} = (?)_2$
   d) $(1010\ 0111)_{excess\text{-}3} = (?)_{BCD}$
3. Explain the positive and negative logic level of digital system. Show that positive logic level XOR gate is equivalent to negative logic level XNOR gate. [2+3]
4. Simplify the given function using K-map. $F = \sum_m (1,2,3,8,9,10,11,14) + d\sum_m (0,4,12)$. Realize the simplified Boolean function using NAND Gate. [4+2]
5. Realize full-adder using a single 4:1 MUX and logical gates. Design the BCD to seven segment decoder. Obtain the simplest logic expressions for segments "a" and "e" also draw their circuits. [4+6]
6. What is an encoder? Explain 8 to 3 line encoder with circuit diagram and truth table. [1+5]
7. Explain the operation of D flip-flop with necessary diagrams truth tables and make its excitation table. [6]
8. Explain the operation of 4-bit serial-in-parallel out (SIPO) register with timing diagram for the given data pattern 1101. [6]
9. Differentiate between synchronous and asynchronous counters. Design a mod-6 synchronous counter using JK flip-flops. [2+7]
10. A synchronous machine has 1-bit input 'X'. The output 'Y' goes high when input contains the massage '101'. Draw the state diagram, derive the transition table (state table), excitation table and design circuit. Use only T flip-flops. [10]
11. What is a memory device? Distinguish between PAL and PLA memory devices. [2+4]
12. With the help of block diagram explain the operation of frequency counter circuit. [4]

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