Delhi Skill and Entrepreneurship University

Credit Scheme and detailed syllabi of
Semester–III B.Tech. Network Engineering and Security

S. No.	Course Type	Course Name	Hours / week			Credits
			L	T	P	
1	DCC	Data Communication & Computer Networks (Theory)	3	0	0	3
2	DCC	Operating Systems (Theory)	2	0	0	2
3	DCC	Introduction to Microprocessors with 8085 and 8086 (Theory)	2	0	0	2
4	DCC	Data Communication & Computer Networks (Practical)	0	0	2	1
5	DCC	Operating Systems (Practical)	0	0	2	1
6	DCC	Introduction to Microprocessors with 8085 and 8086 (Practical)	0	0	2	1

Name of the course: Data Communication and Computer Networks (Theory) / Semester – III BTech Network Engineering and Security

<table>
<tr><td colspan="5">Course Title: Data Communication and Computer Networks (Theory)</td></tr>
<tr><td colspan="2">Type of Course: DCC</td><td>Level of Course:</td><td>Delivery Sub Type of the course:</td><td></td></tr>
<tr><td colspan="2">Course code:</td><td>No. of credits: 3</td><td>L-T-P: 3-0-0</td><td>Learning hours: 45 Hrs</td></tr>
<tr><td colspan="5">Pre-requisite and Co-requisite of Course: Basic mathematics (probability, calculus, linear algebra etc.), digital logic and circuits, concepts of operating systems.</td></tr>
<tr><td colspan="5">Department: B.Tech Network Engineering and Security</td></tr>
<tr><td colspan="5">Syllabus:</td></tr>
<tr><td colspan="5">Course objectives
To develop a thorough understanding of the fundamental principles and theories of Computer Networks.</td></tr>
<tr><td colspan="5">Course content</td></tr>
<tr><td>Module/ Unit</td><td>Topic</td><td>L</td><td>T</td><td>P</td></tr>
<tr><td>1</td><td>Overview of data communication and Networking:

Introduction: Data communications: components, data representation (ASCII, ISO etc.), direction of data flow (simplex, half duplex, full duplex)
Networks: distributed processing, network criteria, physical structure (type of connection, topology), categories of network (LAN, MAN,WAN); Internet: brief history, internet today; Protocols and standards.
Reference models: OSI reference model, TCP/IP reference model, their comparative study.</td><td>6</td><td></td><td></td></tr>
<tr><td>2</td><td>Physical Layer:
Overview of data (analog & digital), Concepts of Signal to Noise Ratio (SNR) and bandwidth, data rate, baud rate etc, signal (analog & digital), transmission (analog & digital) & transmission media (guided & non-guided); Digital modulation and multiplexing: NRZ, ASK, PSK, FSK, QAM, TDM, FDM, WDM, OFDM
Circuit switching: time division & space division switch, TDM bus; Telephone network.</td><td>8</td><td></td><td></td></tr>
<tr><td>3</td><td>Data Link layer and MAC layer:

Types of errors, framing (character and bit stuffing), error detection & correction methods; Flow control Protocols: Stop & wait ARQ, Go-Back- N ARQ, Selective repeat ARQ, HDLC

MAC: Point to point protocol, LCP, NCP, FDDI, token bus, token ring; Reservation, polling, concentration. Multiple access</td><td>8</td><td></td><td></td></tr>
</table>

	protocols: Pure ALOHA, Slotted ALOHA, CSMA, CSMA/CD, FDMA, TDMA, CDMA; Traditional Ethernet, fast Ethernet and WiFi			
4	Network layer: Internetworking & devices: Repeaters, Hubs, Bridges, Switches, Router, Gateway; Addressing : Internet address, classful address, subnetting; Routing : techniques, static vs. dynamic routing , routing table for classful address. Routing algorithms: shortest path algorithm, flooding, distance vector routing, link state routing; Protocols: ARP, RARP, IP, ICMP, IPV6; Unicast and multicast routing protocols.	9		
5	Transport layer: Process to process delivery, UDP, TCP; Congestion control algorithm: Leaky bucket algorithm, Token bucket algorithm, choke packets Quality of service: techniques to improve Qos.	8		
6	Application layer and Security aspects: Protocols: DNS, SMTP, POP, SNMP, FTP, HTTP etc. Security: Cryptography, user authentication, security protocols in internet, SSL/TLS, Firewalls, SSH, HTTPS, FTPs, secure DNS, VPN, SSH tunneling	6		

Scheme of Evaluation:

As per Regulation 2A, DSEU

Recommended Books and References:

Text:

A. S. Tanenbaum – "Computer Networks (4th Ed.)" – Pearson Education/PHI

B. A. Forouzan – "Data Communications and Networking (3rd Ed.) " – TMH

References:

W. Stallings – "Data and Computer Communications (5th Ed.)" – PHI/ Pearson Education

Kurose and Rose – " Computer Networking -A top down approach featuring the internet" – Pearson Education

Comer – "Internetworking with TCP/IP, vol. 1, 2, 3(4th Ed.)" – Pearson Education/PHI

Learning outcomes:

Master Fundamental Concepts: Gain a solid grasp of all layers of computer networks

Hyperlinks of suggested e-Resources:

https://online.stanford.edu/courses/cs144-introduction-computer-networking

https://ocw.mit.edu/courses/6-829-computer-networks-fall-2002/

https://onlinecourses.nptel.ac.in/noc25_cs15/preview

https://courses.ea.asu.edu/computer-networking-in-organizations-cis-194/

https://engineering.purdue.edu/online/courses/computer-network-systems
Pedagogical approach: Classroom teaching using chalk board and/or audio-video systems, flip classroom, presentation, group discussion, hands on problem solving, case studies.
Additional information (if any)

Name of the course: Operating Systems (Theory) / BTech Network Engineering and Security Semester-III

Course Title: Operating Systems (Theory)			
Type of Course: DCC	Level of Course:	Delivery Sub Type of the course:	
Course code:	No. of credits:	L-T-P: 2-0-0	Learning hours: 30
Pre-requisite and Co-requisite of Course: Basic understanding of computers, number systems, digital logic and basic mathematics			
Department: BTech Network Engineering and Security			
Course objectives To have in depth understanding on how operating systems work			

Course content

Module/ Unit	Topic	L	T	P
1	Introduction: Concept of Operating Operating systems, Generations of Operating Systems, Types of Operating Systems, OS Services, System Calls, Structure of an OS – Layered, Monolithic, Microkernel Operating Systems, Concept of Virtual Machine. Case study on Linux/UNIX and Windows Operating Systems.	4		
2	Processes: Definition, Process Relationship, Different states of a Process, Process State transitions, Process Control Block (PCB), Context switching. Thread: Definition, Various states, Benefits of threads, Types of threads, Concept of multithreads, Process Scheduling: Foundation and Scheduling objectives, Types of Schedulers, Scheduling criteria: CPU utilization, Throughput, Turnaround Time, Waiting Time, Response Time; Scheduling algorithms: Pre-emptive and Non pre-emptive, FCFS, SJF, RR; Multiprocessor scheduling: Real Time scheduling: RM and EDF	4		
3	Inter-process Communication: Critical Section, Race Conditions, Mutual Exclusion, Hardware Solution, Strict Alternation, Peterson's Solution, The Producer Consumer Problem, Semaphores, Event Counters, Monitors, Message Passing, Classical IPC Problems: Reader's & Writer Problem, Dinning Philosopher Problem etc.	6		
4	Deadlocks: Definition, Necessary and sufficient conditions for Deadlock, Deadlock Prevention, Deadlock Avoidance: Banker's algorithm, Deadlock detection and Recovery.	6		

5	Memory Management: Basic concept, Logical and Physical address map, Memory allocation: Contiguous Memory allocation– Fixed and variable partition– Internal and External fragmentation and Compaction; Paging: Principle of operation Page allocation Hardware support for paging, Protection and sharing, Disadvantages of paging. Virtual Memory: Basics of Virtual Memory – Hardware and control structures – Locality of reference, Page fault , Working Set , Dirty page/Dirty bit – Demand paging, Page Replacement algorithms: Optimal, First in First Out (FIFO), Second Chance (SC), Not recently used (NRU) and Least Recently used (LRU)	6		
6	I/O Hardware: I/O devices, Device controllers, Direct memory access Principles of I/O Software: Goals of Interrupt handlers, Device drivers, Device independent I/O software, Secondary-Storage Structure: Disk structure, Disk scheduling algorithms File Management: Concept of File, Access methods, File types, File operation, Directory structure, File System structure, Allocation methods (contiguous, linked, indexed), Free-space management (bit vector, linked list, grouping), directory implementation (linear list, hash table), efficiency and performance. File systems: FAT, FAT32, Ext3/4, ZFS and BtrFS. Disk Management: Disk structure, Disk scheduling – FCFS, SSTF, SCAN, C-SCAN, Disk reliability, Disk formatting, Boot-block, Bad blocks	4		

Scheme of Evaluation:

As per Regulation 2A, DSEU

Recommended Books and References:

BOOKS:

Operating System Concepts Essentials, 9th Edition by Avi Silberschatz, Peter Galvin, Greg Gagne, Wiley Asia Student Edition

Operating Systems: Internals and Design Principles, 5th Edition, William Stallings, Prentice Hall of India.

REFERENCE BOOKS:

Operating Systems: A Modern Perspective, 2nd Edition by Gary J. Nutt, Addison-Wesley

Design of the Unix Operating Systems, 8th Edition by Maurice Bach, Prentice-Hall of India

Learning outcomes:

In depth understanding of operating systems concepts

In depth understanding on processes and threads, interprocess communications and deadlocks, deadlock prevention and avoidance techniques In depth understanding of memory management In depth understanding of IO hardware, disk management, file system management Ability to design and implement multithreaded programs Ability to analyze cpu utilization, throughput, turnaround time, waiting time, response time, bottlenecks etc.
Hyperlinks of suggested e-Resources: https://ocw.mit.edu/courses/6-828-operating-system-engineering-fall-2012/ https://onlinecourses.nptel.ac.in/noc24_cs108/preview https://onlinecourses.nptel.ac.in/noc24_cs80/preview https://www.coursera.org/learn/akamai-operating-systems
Hyperlinks of suggested e-resources on the web
Pedagogical approach: Classroom teaching on board or audio visual medium as and when necessary Flip classroom Quiz, presentation (As felt necessary by the teacher)
Additional information (if any)

Name of the course: Introduction to Microprocessors with 8085 and 8086 (Theory) / Semester – III B. Tech Network Engineering and Security

Course Title: Introduction to microprocessors with 8085 and 8086 (Theory)			
Type of Course: DCC	Level of Course:	Delivery Sub Type of the course:	
Course code:	No. of credits: 3	L-T-P: 3-0-0	Learning hours: 45 Hrs
Pre-requisite and Co-requisite of Course: Basic mathematics , concept of analog and digital circuits, basic computer knowledge			
Department: B.Tech Network Engineering and Security			
Syllabus:			

Course objectives

The main objective of this course is to

Understand the architecture of the 8085 microprocessor, its instruction set and write programs in assembly language .

Interface 8085 microprocessor with memory and various I/O devices.

Understand the differences in the architecture and addressing modes of 8 bit and 16 bit Microprocessor.

Course content

Module/ Unit	Topic	L	T	P
1	Introduction to Microprocessors Introduction to microprocessors, microcomputers and single chip microcomputers. Classification of microprocessors (mention of different microprocessors being used). Components of the microcomputer system : Arithmetic and logic unit, Register unit, control Unit, Memory (idea of RAM and ROM) and System Bus (address, data and control). Computer Languages (definition only): Assembly language, Machine language, Low Level language and High Level Language, compiler and interpreter. Applications .	8		
2	8085 Microprocessor Architecture: Features: functional block diagram of 8085 microprocessor (architecture), General purpose registers, register pairs, flags, stack pointer, program counter, De-multiplexing of buses, generation of control signals, pin description of microprocessor 8085.	8		
3	8085 Instruction sets: Assembly language programming basics, classifications of instructions, Instruction set of 8085, addressing modes, instructions and data formats. Introduction to machine cycles: instruction cycle, machine cycle and T- states, Timing diagram: Opcode fetch, Memory read, Memory write, I/O read and I/O write.	8		

4	8085 Programming (Assembly Language) : Data transfer operations, Arithmetic operations, logical operations , Branch Operations, Delay loops, counters and time delay. Stack and subroutine, Code Conversion, BCD arithmetic and 16 bit data operations. 8085 software and Hardware interrupts.	8		
5	Interfacing peripherals with 8085: Basic interfacing concepts, memory mapping (address decoding), Memory mapped I/O and I/O mapped I/O. 8255 Programmable peripheral interface (PPI) , 8254 Programmable interval timer, ADC and DAC chip interfacing. 8259 programmable interrupt controller (basic concept only).	8		
6	Advanced Microprocessors: RISC and CISC (concept only), Architecture of 8086 microprocessor (BIU and EU), 8086 Addressing Modes	5		

Scheme of Evaluation:

As per Regulation 2A, DSEU

Recommended Books and References:

Text:

Microprocessor Architecture, Programming and Applications with 8085, Ramesh S. Gaonkar, Penram international Publishing- V Edition.

Microprocessor 8085 and its interfacing , Sunil Mathur PHI, Second Edition

The intel Microprocessor , Architecture , Programming and Interfacing – Barry B Brey, PearsonEducation/PHI , VI Edition.

References:

Microprocessors , PC Hardware and Interfacing ,N Mathivanan, PHI

The x86 Microprocessors Architecture , Programming and Interfacing (8086 to Pentium) Lyla B.Das, Pearson

Microprocessors and Microcontrollers Architecture, programming and System design 8085, 8086, 8051, 8096, Krishna Kant , PHI, Second Edition

Learning outcomes:

At the end of this course students will be able to apply knowledge and demonstrate proficiency in designing hardware interfaces for memory and I/O as well as write assembly language programs for target microprocessors in real time applications .

Hyperlinks of suggested e-Resources:

https://www.geeksforgeeks.org/architecture-of-8085-microprocessor

https://archive.nptel.ac.in/courses/108/105/108105102/

https://nptel.ac.in/courses/108103157

Pedagogical approach: Classroom teaching, flip classroom, presentation, Assignments, Quizes, group discussions, hands on practice.
Additional information (if any)

Name of the course: Data Communication and Computer Networks (Lab) / Semester – III BTech Network Engineering and Security

<table>
<tr><td colspan="6">Course Title: Data Communication and Computer Networks (Lab)</td></tr>
<tr><td colspan="2">Type of Course: DCC</td><td>Level of Course:</td><td colspan="2">Delivery Sub Type of the course:</td><td></td></tr>
<tr><td colspan="2">Course code:</td><td>No. of credits: 1</td><td colspan="2">L-T-P: 0-0-2</td><td>Learning hours: 30 Hrs</td></tr>
<tr><td colspan="6">Pre-requisite and Co-requisite of Course: Basic mathematics (probability, calculus, linear algebra etc.), digital logic and circuits, concepts of operating systems, C/C++ programming</td></tr>
<tr><td colspan="6">Department: B.Tech Computer Science Engineering</td></tr>
<tr><td colspan="6">Syllabus:</td></tr>
<tr><td colspan="6">Course objectives
To develop a thorough understanding of the practical aspects of Computer Networks by means of hands-on experiments.</td></tr>
<tr><td colspan="6">Course content</td></tr>
<tr><td>Module/ Unit</td><td colspan="3">Topic</td><td>L</td><td>T</td><td>P</td></tr>
<tr><td>1</td><td colspan="3">Introduction to tools and software frameworks:

Familiarization with NS2, Cisco Packet Tracer, Nmap, Tcpdump, Wireshark etc.

Familiarization with socket programming with C and C++ on Linux OS platform.

NIC Installation & Configuration (Windows/Linux).</td><td></td><td></td><td>6</td></tr>
<tr><td>2</td><td colspan="3">Physical Layer and Data Link Layer:
Implement the data link layer framing methods such as character, character-stuffing and bit stuffing.
Write a program to compute CRC code for the polynomials CRC-12, CRC-16 and CRC CCIP.
Develop a simple data link layer that performs the flow control using the sliding window protocol, and loss recovery using the Go-Back-N mechanism.</td><td></td><td></td><td>6</td></tr>
<tr><td>3</td><td colspan="3">Network layer:

Familiarization with Networking cables (CAT5, UTP) and Connectors (RJ45, T-connector), Hubs, Switches, Routers.

Implement Dijkstra's algorithm to compute the shortest path.

Take an example subnet of hosts and obtain a broadcast tree for the subnet.

Implement distance vector routing algorithm for obtaining routing tables at each node</td><td></td><td></td><td>6</td></tr>
</table>

4	Transport layer: Capture Packets Using Wireshark/TCPDump, view and analyze captured packets. Run Nmap scan, Operating System Detection using Nmap Simulate using NS2 and find number of packets dropped by TCP/UDP, packets dropped due to congestion			6
5	Application layer and Security aspects: Capture and analyze DNS, SMTP, POP, SNMP, FTP, HTTP packets using TCPdump/Wireshark. Set up SSH servers and SSH tunneling between local machines. Set up OpenVPN and Wireguard servers and clients. Generate symmetric key, and asymmetric key-pairs and encrypt data using GPG on Linux OS platform. Set up UFW and/or IPTables firewall on Linux platform.			6

Scheme of Evaluation:

As per Regulation 2A, DSEU

Recommended Books and References:
Text:

A. S. Tanenbaum – "Computer Networks (4th Ed.)" – Pearson Education/PHI
B. A. Forouzan – "Data Communications and Networking (3rd Ed.) " – TMH

References:

W. Stallings – "Data and Computer Communications (5th Ed.)" – PHI/ Pearson Education
Kurose and Rose – " Computer Networking -A top down approach featuring the internet" – Pearson Education
Comer – "Internetworking with TCP/IP, vol. 1, 2, 3(4th Ed.)" – Pearson Education/PHI

Learning outcomes:

Master Fundamental Concepts: Gain a solid grasp of all layers of computer networks

Hyperlinks of suggested e-Resources:

https://online.stanford.edu/courses/cs144-introduction-computer-networking
https://ocw.mit.edu/courses/6-829-computer-networks-fall-2002/
https://onlinecourses.nptel.ac.in/noc25_cs15/preview
https://courses.ea.asu.edu/computer-networking-in-organizations-cis-194/
https://engineering.purdue.edu/online/courses/computer-network-systems

Pedagogical approach:
Classroom teaching using chalk board and/or audio-video systems, flip classroom, presentation, group discussion, hands on problem solving, case studies.

Additional information (if any)

Name of the course: Operating Systems (Practical) / BTech Network Engineering and Security
Semester-III

Course Title: Operating Systems (Practical)			
Type of Course: DCC	Level of Course:	Delivery Sub Type of the course:	
Course code:	No. of credits:	L-T-P: 0-0-1	Learning hours: 30
Pre-requisite and Co-requisite of Course: Basic understanding of computers, number systems, digital logic and basic mathematics			
Department: BTech Network Engineering and Security			
Course objectives To have in depth understanding on how operating systems work			
Course content			

Module/ Unit	Topic	L	T	P
1	Installation of Linux OS (Debian/Ubuntu/Fedora etc.) File system structure of Linux OS, Environment variables, installation software packages and libraries.			6
2	Linux command line and basic commands: pwd, cd, ls, mkdir, rmdir, touch, cat, date, cp, mv, rm, grep, clear, piping (|), chmod, chown, chgrp, man, find, passwd, useradd, usermod, tar, ssh, scp, wget, alias, history, sort, uniq, ln, tree, echo, less, more, uname, whoami, head, tail, zip, unzip, sudo, apt etc.			6
3	Process Management: ps, kill, top. System Information: uname, df, du, free, strace. Networking: ping, ifconfig, netstat. Writing shell scripts			4
4	Linux system calls (using C/C++): fork(), exit(), exec(), open(), read(), write(), close(), getpid(), alarm(), sleep(), memcpy(), pipe(), shmget(), getpid(), mmap(), kill(), socket(). Write C/C++ programs to demonstrate the usage of the above system calls. Tracing system calls using strace.			8
5	Multithreading using the pthread library			6

Scheme of Evaluation:

As per Regulation 2A, DSEU

Recommended Books and References:
BOOKS:

Unix: Concepts and Applications, Sumitabha Das, 4th Edition, McGraw Hill
Operating Systems: Internals and Design Principles, William Stallings, 5th Edition,

Prentice Hall of India. REFERENCE BOOKS: Operating Systems: A Modern Perspective, 2nd Edition by Gary J. Nutt, Addison-Wesley Design of the Unix Operating Systems, 8th Edition by Maurice Bach, Prentice-Hall of India
Learning outcomes: In depth understanding of operating systems concepts In depth understanding on processes and threads, interprocess communications and deadlocks, deadlock prevention and avoidance techniques In depth understanding of memory management In depth understanding of IO hardware, disk management, file system management Ability to design and implement multithreaded programs Ability to analyze cpu utilization, throughput, turnaround time, waiting time, response time, bottlenecks etc.
Hyperlinks of suggested e-Resources: https://ocw.mit.edu/courses/6-828-operating-system-engineering-fall-2012/ https://onlinecourses.nptel.ac.in/noc24_cs108/preview https://onlinecourses.nptel.ac.in/noc24_cs80/preview https://www.coursera.org/learn/akamai-operating-systems
Hyperlinks of suggested e-resources on the web
Pedagogical approach: Classroom teaching on board or audio visual medium as and when necessary Flip classroom Quiz, presentation (As felt necessary by the teacher)
Additional information (if any)

Name of the course: Introduction to Microprocessors with 8085 and 8086 (Lab) / Semester – III BTech Network Engineering and Security

<table>
<tr><td colspan="5">Course Title: Introduction to Microprocessors with 8085 and 8086 (Lab)</td></tr>
<tr><td colspan="2">Type of Course: DCC</td><td>Level of Course:</td><td>Delivery Sub Type of the course:</td><td></td></tr>
<tr><td colspan="2">Course code:</td><td>No. of credits: 1</td><td>L-T-P: 0-0-2</td><td>Learning hours: 30 Hrs</td></tr>
<tr><td colspan="5">Pre-requisite and Co-requisite of Course: Basic mathematics , binary arithmetic and logical operations , Basic computer knowledge .</td></tr>
<tr><td colspan="5">Department: B.Tech Computer Science Engineering</td></tr>
<tr><td colspan="5">Syllabus:</td></tr>
<tr><td colspan="5">Course objectives
To analyze ,design and simulate various programming based on 8085 microprocessors and also interfacing it with I/O devices (peripherals).</td></tr>
<tr><td colspan="5">Course content</td></tr>
<tr><td>Module/ Unit</td><td>Topic</td><td>L</td><td>T</td><td>P</td></tr>
<tr><td>1</td><td>Introduction to tools and software frameworks:

Introduction and usage of 8085 and 8086 simulators, Study of 8085 programming training Kit (How to operate)</td><td></td><td></td><td>6</td></tr>
<tr><td>2</td><td>Introduction to 8085 Instructions (data transfer, Arithmetic and logical)
Write
Assembly language program to copy data from one register to another register .
Assembly language program to copy data from one memory to another memory/Exchange data from one memory to another memory using direct and indirect addressing.
Assembly language program to transfer a block of data from one memory location to another memory location
Assembly language program to add two 8 bit hexadecimal numbers (with and without carry) stored in two different registers (B and C) and store the result in another register (D).
Assembly language program to add two 8 bit numbers (with and without carry) stored at two different memories (XXXX and YYYY) and store the result at another memory(ZZZZ).
Assembly language program to subtract two 8 bit hexadecimal numbers (with and without carry) stored in two different registers (B and C) and store the result in another register (D).</td><td></td><td></td><td>7</td></tr>
</table>

	Assembly language program to subtract two 8 bit numbers (with and without borrow) stored at two different memories (XXXX and YYYY) and store the result at another memory(ZZZZ). Two 8 bit hexadecimal numbers are stored in registers B and C . Illustrate the result of instructions OR B, AND B, NOT B and XOR B			
3	Introduction to 8085 Instructions (Branch Instructions) Write Assembly language program to multiply two 8 bit numbers using repetitive addition Assembly language program to divide two 8 bit numbers using repetitive subtraction Assembly language program to find largest /smallest number from Assembly language program to arrange data in ascending/descending order Assembly language program to find sum of 10 hexadecimal number stored at memory and store sum and carry at different locations Assembly language program to search a number from a given list Assembly language program to find square and square root for a given number .			7
4	Time Delays and Interfacing using PPI 8255/8254/DAC/ADC. Display FF to 00H with same delay in each count, LED blinking (delay 1 second) using 8255, Square wave generation (Period 400μs) using 8254, DC motor, Seven segment display, Solid state relay (at least three interfacing programs). Note: *This list is a list of recommended programs/exercises. However the faculty may ask students to perform experiments as per availability of materials/equipment in the lab.*			10

Scheme of Evaluation:

As per Regulation 2A, DSEU

Recommended Books and References:

Text:

Microprocessor Architecture, Programming and Applications with 8085, Ramesh S. Gaonkar, Penram international Publishing - V Edition.

Microprocessor 8085 and its interfacing, Sunil Mathur PHI, Second Edition

The Intel Microprocessor, Architecture, Programming and Interfacing – Barry B Brey, PearsonEducation/PHI, VI Edition.

References: Microprocessors, PC Hardware and Interfacing, N Mathivanan, PHI The x86 Microprocessors Architecture, Programming and Interfacing (8086 to Pentium) Lyla B. Das, Pearson Microprocessors and Microcontrollers Architecture, programming and System design 8085, 8086, 8051, 8096, Krishna Kant, PHI, Second Edition
Learning outcomes: At the end of this course students will be able to apply knowledge and demonstrate proficiency in designing hardware interfaces for memory and I/O as well as write assembly language programs for target microprocessors for real time applications .
Hyperlinks of suggested e-Resources: https://www.geeksforgeeks.org/architecture-of-8085-microprocessor https://archive.nptel.ac.in/courses/108/105/108105102/ https://nptel.ac.in/courses/108103157
Pedagogical approach: Classroom teaching, flip classroom, presentation, Assignments, Quizzes, group discussions, hands on practice.
Additional information (if any)