Krishna Chemudupati

407-808-7141 | krishkc@seas.upenn.edu | LinkedIn | GitHub | Portfolio

Education

University of Pennsylvania – *Vagelos Integrated Program in Energy Research* Philadelphia, PA
MSE Electrical Engineering (3.6/4.0); BSE Electrical Engineering, BA Physics (3.3/4.0) *May 2027*
Concentrations & Minors: Computer Engineering, System-on-a-Chip, Mathematics, CS, Data Science

Coursework: Digital Circuits (Grad), Analog Circuits (Grad), Mixed Signal Circuits (Grad), Semiconductor Memory Circuits (Grad), Computer Organization (Grad), Embedded Devices (Grad), HW/SW Co-design (Grad), ML (Grad), SystemVerilog, Signal Processing, DSA, Control Systems, Photonics, Electrodynamics, Statistical Mechanics, Thermodynamics, Programming, Multivariate Calculus, PDEs, Linear Algebra

Technical Skills

Circuit Design & Simulation: Cadence Virtuoso, LTspice, Ngspice, Electric VLSI, Quartus Prime, ModelSim, Sentaurus TCAD, MATLAB, Altium, SolidWorks
Programming & Machine Learning: Python, C, C++, Java, OCaml, SystemVerilog, Verilog, CUDA, HTML/CSS/JavaScript, PyTorch, TensorFlow, Scikit-learn, NumPy, Pandas, Matplotlib
Embedded Systems & Tools: ATmega328PB, Arduino, Raspberry Pi, Jetson Orin Nano, ROS2, FreeRTOS, Oscilloscope, Logic Analyzer, Keithley Analyzer, SPI, I2C, UART, Git
Verification & Debug: Verilator, cocotb, Surfer, VCD waveform analysis, constrained-random testbenches, coverage-driven verification

Projects

5-Stage Pipelined RISC-V RV32IM Processor | *SystemVerilog, Verilator, cocotb, Surfer* Jan 2026 – Present

- Designed 5-stage pipelined RV32IM processor with MX/WX/WM bypassing and hazard detection/stalling; supports all 32 instructions in RV32IM ISA with proper byte alignment for multi-byte loads/stores
- Built 32-bit Carry Lookahead Adder (CLA) with hierarchical gp1/gp4/gp8 architecture for efficient carry propagation; implemented 8-stage pipelined divider using iterative hardware algorithm
- Currently implementing writeback cache with AXI-Lite interface for memory subsystem integration
- Passed Dhrystone benchmark (190k+ instructions) with cycle-accurate tracing; improved from 4.7 MHz (single-cycle) to 27.5 MHz (pipelined) on Lattice iCE40 FPGA
- Developed cocotb testbench with directed tests for pipeline hazards, branch mispredictions, and memory dependencies; debugged forwarding paths and stall logic using Surfer waveform analysis
- Created detailed schematics with signal names, bus widths, and hierarchical module diagrams; generated FPGA resource reports tracking LUT usage and critical paths

LLM-Driven SystemVerilog Design & Verification Agent | *Python, OpenAI API, Verilator, Surfer* Dec 2025

- Built GPT-4o powered RTL generator accepting plain English hardware descriptions; generates SystemVerilog design modules and fully self-checking testbenches with assertions and automatic VCD waveform generation
- Implemented closed-loop verification: iteratively compiles with Verilator, parses error logs, and re-prompts LLM until lint/simulation passes (up to 10 attempts); auto-generates constrained-random testbenches
- Coverage-driven flow tracks functional coverage, identifies untested corners, generates targeted stimulus; parses output to detect timing violations, latch inference, multi-driven nets
- Generates SystemVerilog assertions, covergroups, and scoreboards; produces layered testbenches with drivers, monitors, and reference models following industry-standard verification methodology
- Supports diverse designs: combinational (adder, mux, decoder, multiplier), sequential (counter, shift register, FIFO, FSM), and communication (UART TX, SPI controller, I2C state machine)

Ring Oscillator-Based True Random Number Generator | *SystemVerilog, Verilator, Python* Fall 2025

- Designed hardware entropy source using 8 ring oscillators with varied inverter counts (3, 5, 7, 9, 11 inverters) producing different propagation delays (100-170ps) for phase variation
- Implemented entropy extraction via XOR of all oscillator outputs; added sampling divider for controlled output rate and synchronization chain to avoid metastability issues
- Created Python-driven Verilator simulation with configurable bit generation and statistical verification suite
- Validated randomness through Shannon entropy measurement (target ∼1.0), autocorrelation analysis for pattern detection, and basic NIST test compatibility; achieved ∼50% ones/zeros distribution

Transistor-Level VLSI Design Suite | *Cadence Virtuoso (45nm), Electric VLSI (22nm)* Spring – Fall 2025

- Memories: 64-bit 3T1C DRAM with decoder, sense amps, refresh controller (68ns write, 0.21ns read); 64-bit 6T SRAM with precharge, write drivers, differential sense amps (137.5ps access, 35.2μW)

- Arithmetic: 4x4 Dadda multiplier with Elmore-delay sizing (36% faster at 125ps, 2.5x lower energy at 50fJ); 8-bit RCA with K-map XOR2, tau-model sizing (43.6% faster, 123ps, 3.56fJ)
- 16:1 LUT from 2:1 MUX hierarchy; parametric sweeps: 68.8% faster (117ps), 58.4% higher freq (914 MHz), 46.6% lower energy (332fJ)
- Analog: Wideband TIA for optical receivers; 8-stage architecture (CG preamplifier, CS gain, differential chain, output buffer); 406 kΩ trans-impedance, 300 MHz bandwidth, 1.38 mW power
- Verified via boundary tests, counter-driven address sweeps, exhaustive coverage; scripted Python to extract Cadence simulations; validated sense amp thresholds, retention, worst-case delays

16×4 Dynamic RAM (64-bit 3T1C DRAM) | *Cadence Virtuoso, 45nm CMOS* Fall 2025

- Designed 3T1C DRAM architecture with separate read/write wordlines for electrically isolated access paths; 1pF storage capacitor balancing retention time, sensing margin, and area
- Implemented 4-to-16 row decoder, PMOS-based bitline precharge, inverter-based sense amplifiers (switching thresholds: 0.662V high, 0.573V low), and autonomous refresh controller cycling all 16 rows within 32ms
- Two-phase non-overlapping clock scheme ensuring no contention between precharge, evaluation, and sensing phases; measured write-high delay 68.377ns, write-low 6.128ns, read-high 0.21ns, read-low 57ps
- Achieved FOM = 6.19×10^{-18} mm^2·W·s; comprehensive 55-page technical report with transistor sizing rationale based on measured delay, retention, and energy

16×4 Static RAM (64-bit 6T SRAM) | *Electric VLSI, 22nm HP CMOS* Spring 2025

- Designed 6T SRAM cell with cross-coupled inverters; implemented 16-row column slice architecture with shared bitline infrastructure for 4-bit word access
- Built peripheral circuits: two-level row decoder (NAND2 + NOR2 reducing from 160 to optimized transistor count), bitline precharge with NAND2-gated enable, tristate write drivers, and cross-coupled differential sense amplifier with clocked positive feedback
- Two-phase non-overlapping clock (clka, clkb) separating precharge and evaluation; measured read delay 121.1ps (fall), 118.9ps (rise); write delay 45.2ps (fall), 137.5ps (rise)
- Power consumption 35.2μW at 3.57 GHz; achieved FOM = 1.16×10^{-37} using formula 60·BitcellArea·Power·Delay^2

4×4 CMOS Array Multiplier | *Cadence Virtuoso, 45nm CMOS* Fall 2025

- Implemented Braun array architecture with partial-product AND gates and diagonal carry propagation through half/full adder rows; baseline using minimum-sized static CMOS gates
- Optimized critical path using Elmore-delay RC modeling: replaced bag-of-gates full adder with compact complementary static-CMOS design reducing internal logic depth; analytically sized gates along diagonal carry-propagation staircase
- Exhaustive verification across all 256 input combinations (4-bit × 4-bit) with 100% functional correctness; captured 5.5M+ raw waveform measurements for baseline, 3.5M+ for optimized
- Baseline: 196.6ps worst-case delay; Optimized: 125ps (36% improvement), 50fJ active energy (2.5× reduction); characterized both active and leakage energy across all input states

8-bit Ripple Carry Adder | *Electric VLSI, 22nm HP CMOS* Spring 2025

- Designed cascaded full-adder bit-slices where carry output feeds next stage's carry input; baseline with minimum-sized transistors (W=L=22nm) at 0.8V supply
- Delay optimization: replaced multi-level NAND/NOR/INV XOR2 with 12-transistor K-map minimized static CMOS implementation reducing logical depth; tau-model sizing (W=1.22×min) with 1V supply
- Verified all 8 input combinations per full-adder; cascaded tests including full carry propagation through all 8 stages
- Baseline: 218ps worst-case delay; Optimized: 123ps (43.6% improvement), 3.56fJ energy; comprehensive 92-page report with area/delay scaling analysis for 1/2/4/8-bit adders

16:1 Lookup Table for FPGA CLB | *Cadence Virtuoso, 45nm CMOS* Fall 2025

- Implemented 16:1 LUT from hierarchical 2:1 pass-gate MUX network; baseline using minimum-sized inverters and pass transistors
- Multi-variable optimization: parametric sweeps alternating wmux and wbuf until convergence; optimal sizing wmux=208nm, wbuf=120nm with stage-dependent widths (120nm to 10μm across hierarchy)
- Validated all 16 address combinations with counter-type input pattern (I3 LSB with 2ns period through I0 MSB with 16ns period); verified correct data propagation for all states
- Baseline: 374.5ps delay, 577 MHz max freq, 622.1fJ energy; Optimized: 117ps (68.8% faster), 914 MHz (58.4% higher), 332.2fJ (46.6% lower)

Wideband Transimpedance Amplifier | *Cadence Virtuoso, 45nm CMOS* Fall 2025

- Designed 8-stage TIA for high-speed optical receiver: common-gate preamplifier (low input impedance), common-source gain stage, source-follower differential conversion (CD1/CD2), 4-stage differential amplifier chain, output buffer
- Comprehensive 45nm process characterization: ID-VDS curves, threshold voltage extraction via gm method, Cgs/Cgd vs ID modeling, process fT measurement for both NMOS and PMOS
- Hand calculations validated against simulation: trans-impedance 406 kΩ (112.27 dBΩ), upper -3dB bandwidth 300.4 MHz, integrated noise 121.3 nA$_{rms}$, output swing 0.6 Vpp

- Power consumption 1.38 mW; stability analysis with phase margin verification; 49-page technical report comparing hand calculations vs. SPICE simulation for all metrics

Interactive MOS Capacitor Simulator | *Python, Matplotlib, Semiconductor Physics* Fall 2025

- Built interactive MOS capacitor depth profile simulator with real-time slider-based gate voltage control (-2.0V to +2.0V range) and automatic axis scaling
- Calculates and visualizes electric field distributions in oxide and semiconductor, electrostatic potential profiles, carrier density (electrons/holes) with logarithmic scaling, and band diagrams (Ec, Ev, EF, Ei energy levels)
- Implemented physics-accurate semiconductor modeling including depletion region calculations; professional matplotlib dashboard with 4 synchronized subplots updating in real-time

CircuitSmith: Analog Circuit Modeling Library | *Python, PyTorch, OpenAI API, Matplotlib, SciPy* 2025

- Developed comprehensive analog circuit modeling library supporting amplifiers (Common Source, Source Follower, Common Gate), differential circuits (Differential Pair, Current Mirror), OpAmps (Two-Stage), and filters (RC/RLC Low-Pass, RLC Band-Pass)
- Implemented frequency response analysis (Bode plots, magnitude/phase), parameter sweeps for sensitivity analysis, Monte Carlo analysis for statistical performance bounds, and transient simulation (step/sine/noisy signal response)
- Integrated LLM-powered design generation: accepts specifications like "Design a two-stage opamp with 60dB gain" and generates complete circuit blocks with parameters and validation
- Provided CLI interface for analysis and sweeps, complete API documentation, and 10 runnable examples with professional matplotlib visualizations

Energy-Aware ML Model Quantization Benchmark | *Python, PyTorch, CUDA, Transformers, nvidia-smi* 2025

- Built production-ready 8-step automated benchmarking harness for ML model energy measurement across FP32, FP16 (automatic mixed precision), and INT8 (quantization) modes
- Implemented zero-I/O design with all data GPU-resident; asynchronous power logging via nvidia-smi subprocess at 100ms sampling rate with CUDA synchronization for accurate timing
- Computed comprehensive metrics: latency (mean/median/std), throughput (samples/sec), power consumption (Watts), energy (Joules/inference, mJ), energy efficiency (inferences/Joule), accuracy, and GPU memory usage
- Benchmarked GPT-2 language model on pre-tokenized datasets; delivered 2,500+ lines of Python across 13+ modules with reproducible results (fixed random seeds), CSV/JSON output, and automated multi-trial experiment runner

F1 Tire Strategy Optimization & Degradation Analysis | *Python, XGBoost, LOWESS, Monte Carlo, FastF1 API* 2025

- Proved Charles Leclerc would have won 2022 Hungarian GP (P6 → P1) with optimal strategy; achieved 28.02 ± 3.00 seconds improvement with 81.6% win probability across 5,000 Monte Carlo simulations
- Built data pipeline using FastF1 API for telemetry extraction with 107% rule application and fuel mass correction; implemented LOWESS regression learning degradation curves for each compound (Soft: ∼0.20 s/lap, Medium: ∼0.04 s/lap, Hard: ∼0.02 s/lap)
- Developed deterministic optimization and Monte Carlo simulation with Common Random Number (CRN) variance reduction; optimal 2-stop strategy (M:26, M:27, S:17) outperformed actual 4-stop by 28 seconds
- Trained 600-tree XGBoost model (MAE 0.0405 s/lap, R^2 0.74) with features including lap position, tire age, fuel load, weather; top feature importance: avg_pace_first3 (38.2%)
- Generated 7 publication-quality figures at 300 DPI; statistical significance: t = 862.14, p ¡ 0.001

PX4/ULog Aircraft Telemetry Analysis Suite | *Python, PX4 Autopilot, pyulog, Matplotlib* 2025

- Developed comprehensive ULog analysis toolkit for fixed-wing aircraft with 5 analysis scripts: text analysis, PDF visualization, CSV export, readable reports, and interactive HTML dashboards
- Supports 118 telemetry topics with configurable parameters; generated publication-quality PDF reports with 12 summary metrics and color-coded HTML dashboards
- First test flight results: 43.8s duration, 48.2m distance, 4.9 m/s max speed (17.5 km/h), 14.1m max altitude AGL, 0.80m GPS accuracy with 13 satellites, IMU at 199.2 Hz (18,567 samples, no dropouts)
- Implemented statistical analysis: min/max/mean calculations, battery performance assessment, GPS quality metrics; exported structured data to CSV and JSON for external analysis

Smart Bicycle Brake Light System | *C (bare-metal), ATmega328PB, I2C, ADC, PWM* 2025

- Designed smart bicycle brake light with 3-axis accelerometer (LIS3DH, ±2g range), ambient light sensor (LDR), and high-brightness LED strip via MOSFET PWM driver
- Achieved SRS requirements: IMU sampling at 100 Hz, brake state update within 50ms; deceleration detection (-0.2g for 30ms) triggers LED to 100% within 100ms; ambient light-based brightness control (10-60% duty cycle)
- Implemented moving average filter (N=7) reducing false triggers by 94.4%; smooth 500ms LED fade-out after braking for professional visual effect
- Built custom drivers for LIS3DH IMU and TWI (I2C); IMU noise ¡ 0.05g RMS after filtering; LDR distinguishes dark (¡50 lux) and bright (¿300 lux) conditions
- Complete bare-metal firmware with I2C, ADC, PWM, interrupts; real-time UART logging for debugging; achieved 3.2 hours runtime on battery; BOM cost: $70.50

Ultrasonic Theremin Musical Instrument | *C, ATmega328PB, HC-SR04, PWM, ADC* 2025

- Built theremin-like instrument with distance-controlled pitch (3-152cm range) using HC-SR04 ultrasonic sensor and ambient light-controlled volume via photoresistor
- Implemented 8 discrete musical notes (C6-C7, 1046-2093 Hz) with calculated OCR0A values; linear mapping formula: OCR0A = (16/149) × SENSOR_VALUE + 13.68
- Developed 10-level volume mapping (5-50% duty cycle) using ADC photoresistor reading (ADC0, range 95-989); used separate PWM outputs (OC0A for frequency, OC0B for volume)
- Tested three timer modes (Normal, CTC, PWM) and verified 440 Hz (A4) square wave with oscilloscope; timer prescaler 256 yielding f_timer = 62.5kHz

Embedded Pong Game with Wireless Control | *C, ATmega328PB, SPI, ST7735 LCD, ESP32, Blynk* 2025

- Implemented complete Pong game with ball physics, velocity tracking, paddle collision detection, computer AI opponent, and score tracking (winning at 2 points) on ATmega328PB at 16MHz
- Integrated ST7735 TFT LCD (160×128 pixels, RGB565 16-bit color) via SPI; implemented LCD command/data differentiation (D/CX pin control) and custom LCD_GFX graphics library with drawing primitives
- Added joystick control via ADC (channels 4-5, PC4-PC5), PWM-based buzzer for audio feedback, and RGB LEDs for scoring indication; verified SPI communication with Logic Analyzer
- Integrated ESP32 for wireless Blynk app control; game constants: paddle 4×20 pixels at 3 pixels/frame, ball 3-pixel radius

MOSFET-Based Analog Metal Detector | *ALD1103 MOSFET, LTspice, Altium Designer* 2025

- Designed beat-frequency metal detector using two LC oscillators: fixed at 50.9 kHz, variable at 48.5 kHz producing 900 Hz baseline beat frequency; metal proximity shifts variable inductor from 9.75 mH to 8.67 mH
- Implemented differential amplifier/mixer detecting frequency shift; output tone changes from 977 Hz (no metal) to ∼4 kHz (metal detected) — clear 4× frequency shift for reliable detection
- Built common-source and common-drain amplifier stages using ALD1103 quad-MOSFET array; calculated transconductance 317 μS, output amplifier gain -3.17 with 10 kΩ drain resistor
- Validated via hand calculations, LTspice simulations, and hardware measurements; designed PCB within 100mm × 120mm constraints; identified empirical tuning requirements (RC filter performed better without capacitor due to phase interactions)

Citadel-CorrelationOne Summer Invitational Datathon – $10,000 Winner | *Python, ARIMA, Random Forest, PageRank* Summer

- Won $10,000 cash prize analyzing "Life, Liberty, and the Pursuit of Healthy Living: Unraveling the Hidden Costs of Ultra Processed Foods in the United States" with 4-person team
- Built Random Forest model achieving MSE 213.85, R^2 0.80 for predicting environmental impact; identified ultra-processed foods (UPFs) have 2.4× emissions coefficient vs. minimally processed baseline, moderately processed at 1.7×
- Applied ARIMA time series forecasting and PageRank graph analysis for supply chain modeling (nodes as material sources, edges as transportation networks); integrated stock market, USDA agricultural, EIA emissions, and food access atlas data
- Discovered states with high dairy/grain consumption show lower CO2 emissions and food desert severity; quantified food industry's 25% contribution to global greenhouse emissions

2-Axis Analog Plotter with Closed-Loop Feedback Control | *Arduino, DC Motors, Potentiometers* 2024

- Built 2-axis plotter with closed-loop feedback control using potentiometer-based position sensing (1 V/cm sensitivity) and differential amplifier error correction; motor characterization: 3.2 RPM/V, leadscrew 1.6mm pitch with 40:1 gearbox
- Achieved loop gain 0.00226 (both axes), difference amplifier gain K=10; positional accuracy within 0.1-0.6V deviation across ±6V range; natural anti-overshoot behavior from closed-loop design
- Implemented coordinate-based movement with interpolation for diagonal paths (0.5cm increments); plotted square, triangle, and complex fish design with semicircle algorithm using 10-segment arc division
- PWM-to-DC voltage conversion via RC filter; motor speed reduction proportional to decreasing error voltage demonstrating closed-loop control advantages over Lab 9 open-loop baseline

F1/18th: Accessible Autonomous Racing Platform | *Raspberry Pi 5, ROS2, Computer Vision, CAD* Summer 2024

- Developed 1/18-scale autonomous racing platform as accessible alternative to expensive F1TENTH; tested Jetson Orin Nano vs Raspberry Pi 5, selected RPi 5 for superior processing speed and lower cost
- Implemented lane detection pipeline using thresholding and sliding window algorithm with parabolic trajectory fitting; integrated ROS2 nodes for hardware-software integration across computing, perception, and control layers
- Designed custom chassis and camera mounts using CAD tools enabling rapid prototype iteration; integrated motor control with ESC for rear motor drivetrain
- VIPR Summer Research (Vagelos Integrated Program in Energy Research); team of 7 researchers; poster presentation demonstrating CV-based autonomous navigation on real hardware

Network Router with Dijkstra's Algorithm | *C++, Graph Algorithms, Data Structures* 2024

- Implemented shortest path routing using Dijkstra's algorithm with efficient adjacency list graph representation and min-heap priority queue for optimal O((V+E) log V) performance
- Supports both directed and undirected graph topologies with two routing modes: single-source (paths from source to all vertices) and single-pair (optimal path between two specific nodes)

- Built custom graph.cpp/h, heap.cpp/h, and stack.cpp/h data structure implementations; passed all 20 test cases with correct path calculations

Personal Portfolio Website | *HTML5, CSS3, JavaScript (ES6+), Firebase, GitHub Pages* 2024

- Built modern portfolio site with dark theme, Inter typography, and Canvas-based animated particle background with performance optimization (visibility API awareness, responsive particle count, threshold-based connection rendering)
- Integrated Firebase Firestore for real-time blog post management and Firebase Authentication for secure admin access; admin panel for content management
- Implemented accessibility compliance: semantic HTML5, ARIA labels, keyboard navigation, color contrast compliance; responsive design with CSS Grid and Flexbox
- Deployed on GitHub Pages (free tier) with Firebase free tier (50K reads/day, 20K writes/day, 1GB storage); $0/month operational cost

CoralDoctor: Coral Reef Health Monitoring System | *IoT Sensors, Microcontroller, PCB Design* 2024

- Developed coral health assessment system through environmental monitoring with multi-sensor integration for temperature, pH, light, and salinity measurement
- Built real-time data logging and analysis framework with alert system for reef stress conditions; designed for field deployment in marine environments
- Created data visualization and interpretation framework with biological validation of stress indicators

Experience

Ferroelectric Compute-in-Memory Researcher Feb 2025 – Present

Jariwala Lab, University of Pennsylvania *Philadelphia, PA*

- Characterizing ferroelectric diodes in MFM and MIFM structures using AlScN with HfO_2 interlayers across varied scandium concentrations, substrates, and electrode configurations for selector-free crossbar arrays enabling MAC operations and neuromorphic compute-in-memory
- Supporting design of CMOS-compatible BEOL peripheral circuitry for read/write operations in 40nm process; solving pA-level current sensing challenges through state-of-the-art transimpedance amplifier and comparator design
- Contributing to simulation efforts through multidimensional Preisach hysteresis modeling and Sentaurus TCAD device simulations for FeD switching behavior prediction
- Developing PCB probe card instrumentation for automated device measurement; characterizing cryogenic FeD behavior for low-temperature memory applications
- Training new graduate and undergraduate researchers on device characterization workflows, measurement instrumentation, and data analysis pipelines
- Under review as co-first author on FeD multilevel arrays and as author on low-temperature FeDs (targeting *Nature Electronics*)

Co-Lead Autonomous Systems Researcher Mar 2024 – Feb 2025

xLab (Mangharam Lab), University of Pennsylvania *Philadelphia, PA*

- Conducted research on real-time autonomy for embedded systems, focusing on vision-based lane detection and SLAM using ROS2 and OpenCV
- Developed and optimized algorithms for 1/18th scale autonomous vehicle; implemented CUDA-optimized OpenCV lane detection on Jetson Orin Nano, reducing inference latency by 36%
- Integrated custom PCB hardware with NVIDIA Jetson platform for low-latency control; designed PCB for power distribution and sensor routing; verified signal integrity for HW/SW integration
- Built and validated sensor interface drivers for LiDAR, IMU, and camera modules using SPI/I2C protocols; validated ROS2 autonomy stack through systematic regression testing
- Debugged sensor data flow across HW/SW interfaces using waveform analysis and automated log parsing scripts

Teaching Assistant – CIS 1100 (Intro to Computer Science) Aug 2024 – Present

University of Pennsylvania *Philadelphia, PA*

- Deliver weekly recitations and mentor students in Python programming, object-oriented design, pandas, and web scraping with Beautiful Soup
- Facilitate debugging sessions and reinforce core CS concepts including data structures, algorithms, and computational thinking
- Cultivate long-term computational thinking through hands-on guidance and tailored instruction; support 30+ students per section

Teaching Assistant – ESE 1120 (Intro to Electrical Engineering) Dec 2024 – Present

University of Pennsylvania *Philadelphia, PA*

- Teach weekly recitations and supervise lab sections for introductory course in electricity and magnetism with focus on circuits
- Guide students through Kirchhoff's laws, resistive networks, RC transients, and energy storage concepts
- Reinforce theoretical concepts through hands-on circuit construction, measurement with oscilloscopes and multimeters, and structured experimentation

Propulsion & Avionics Engineer Sep 2023 – Present

Penn Aerospace Club *Philadelphia, PA*

- Contributing to propulsion, avionics, and autonomous flight systems for competitive aircraft platform
- Design and implement control surface actuation, wireless communication for remote piloting, and onboard autonomy
- Support technical documentation through detailed design reports and flight readiness reviews
- Designed PCB-based avionics and validated HW/SW integration; ranked 3rd globally in AIAA Design Build Fly competition

Project Consultant Sep 2023 – Present

Penn Climate Ventures *Philadelphia, PA*

- Conduct market and technical research to evaluate climate tech startups across energy, transportation, and sustainable materials sectors
- Assess business models, scalability, and environmental impact to support VC funding strategy and innovation acceleration
- Deliver strategic recommendations to early-stage founders on go-to-market strategy, competitive positioning, and technical feasibility

Sustainability Consultant Sep 2023 – Present

Penn Sustainability Consulting *Philadelphia, PA*

- Advise organizations on implementing sustainable practices through data-driven analysis and targeted recommendations
- Deliver client reports focused on energy efficiency, supply chain optimization, and carbon reduction strategies
- Conduct life cycle assessments and develop metrics frameworks for tracking environmental impact

Resident Advisor Aug 2024 – Present

Hill College House, University of Pennsylvania *Philadelphia, PA*

- Support first-year students through mentorship, community-building, and academic guidance
- Facilitate programming and foster supportive residential environment for 40+ residents
- Respond to student concerns and connect residents with campus resources; coordinate with professional staff on community development initiatives

Peer Advisor Mar 2024 – Present

Penn Engineering & College of Arts and Sciences *Philadelphia, PA*

- Advise incoming students in Engineering and the College on academic planning, campus resources, and community engagement
- Facilitate onboarding and support smooth transition to university life; conduct one-on-one advising sessions during orientation and throughout academic year