

ESE 3190 Final Project - Metal Detector

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Introduction

The goal of this final project for ESE 3190 was to design, simulate, construct, and characterize a working metal detector using MOSFET-based analog circuitry. The detector leverages the principle of inductive sensing: when an alternating magnetic field generated by a custom air-core inductor interacts with nearby metal, eddy currents are induced in the metal that generate opposing magnetic fields. According to Lenz's Law, this opposition effectively reduces the inductance of the sensing coil, thereby increasing the resonant frequency of an LC oscillator built around it. This frequency change serves as the basis for detection.

To implement this, the final circuit integrates four key subsystems, each developed and studied in earlier labs: (1) a reference LC oscillator with a fixed commercial inductor, (2) a variable oscillator using the custom inductor, (3) a differential mixer that outputs a beat frequency based on the frequency difference between the two oscillators, and (4) a PMOS common-source amplifier and buffer stage that amplifies this beat signal and drives an audio output.

When no metal is present near the sensing coil, the variable oscillator operates at a slightly lower frequency than the fixed reference oscillator, resulting in a small but nonzero beat frequency. This beat signal is processed by the mixer and amplified to produce a soft, continuous tone from the speaker. As a metallic object approaches the coil, the inductance of the variable oscillator decreases, increasing its oscillation frequency. When the two oscillators momentarily match in frequency, the beat signal vanishes, resulting in silence at the output. As the metal is brought even closer, the variable oscillator's frequency surpasses that of the fixed oscillator, and a new beat signal emerges – this time at a higher frequency. The speaker accordingly emits a louder, higher-pitched tone, providing a clear and intuitive acoustic indicator of the metal's proximity.

This frequency-based detection mechanism is made possible by the careful integration of several discrete subsystems, each responsible for a specific stage in the signal generation, processing, or output chain. While the core functionality relies on subtle shifts in oscillation frequency, the successful implementation of the detector as a physical system also depends on thoughtful design at a broader architectural level.

This type of analog metal detector has a range of practical applications due to its sensitivity to changes in inductance. Common use cases include locating buried metallic objects such as nails, pipes, or cables during construction and renovation work. It can also be used in archaeological fieldwork to identify metal artifacts beneath the soil surface. On a smaller scale, similar circuits are employed in quality control systems to detect metal contamination in food or packaging lines. Educationally, the design serves as an excellent demonstration of resonance, analog amplification, and frequency domain processing in undergraduate electronics courses. The analog signal chain used in this detector, from matched LC oscillators through a nonlinear mixer to amplification and output, is a foundational architecture with wide ranging relevance. In RF and communication systems, similar oscillator-mixer chains are used for frequency translation in receivers and transmitters. Superheterodyne radios, for example, mix a high frequency signal with a local oscillator to produce an intermediate frequency (IF), closely mirroring this detector's architecture. Analog proximity and displacement sensors exploit the same principle, using frequency shifts in LC oscillators to measure distance or material properties. Beat frequency oscillators (BFOs), used in audio range metal detectors, sonar, and musical synthesizers, also rely on frequency mixing to produce low frequency signals from high frequency sources. The amplifier and filter stages that follow are broadly applicable for signal conditioning before audio or ADC interfacing.

Design Strategy

The full metal detector system can be decomposed into five distinct macro-scale circuit blocks: the oscillator stage, the mixer stage, the current mirror, the amplification chain, and the CS-CD output stage. Each serves a crucial role in transforming a frequency shift (caused by the presence of nearby metal) into a detectable acoustic signal. The design and behaviour of each block are tightly coupled, and any deviation in performance at one stage can compromise the functionality of the entire system. Below, we describe each of these subsystems in detail.

Oscillators

The oscillator stage is responsible for generating the two high-frequency sinusoidal signals whose difference forms the basis of metal detection. It consists of two LC oscillator circuits built using an ALD1103 quad-MOSFET array, one serving as a fixed reference and the other incorporating a custom-wound air-core inductor as its sensing element. Each oscillator forms a feedback loop using cross-coupled MOSFETs and a tank circuit composed of a center-tapped inductor and capacitors. The resonant frequency of each oscillator is governed by the relation

$$f = \frac{1}{2\pi\sqrt{LC}}$$

In the fixed oscillator, the inductance remains constant, ensuring a stable reference frequency around 50.9 kHz. In contrast, the variable oscillator uses a hand-wound air-core coil with an inductance of 9.75 mH, that reacts to nearby metal by reducing its inductance to 8.67 mH, which in turn increases its oscillation frequency. These two signals are later processed by the mixer to extract their frequency difference.

Current Mirror

The current mirror sets the biasing conditions for the differential amplifier that serves as the core of the mixer stage. Implemented using two matched NMOS transistors, the mirror ensures that a fixed tail current flows through the differential pair regardless of small fluctuations in supply voltage or temperature. The tail current is set by a resistor R_{var3} , which determines the gate-source voltage of the reference transistor in the mirror configuration. This reference current is then mirrored into the differential pair, effectively defining the operating point of the mixer and ensuring that it functions in the saturation region. Precise control of this bias current is critical, as it directly impacts the gain and linearity of the differential amplifier.

Mixer Stage

The mixer is implemented as a differential pair using another ALD1103, with the tail current provided by the previously described current mirror. The two oscillator outputs are connected to the gates of the input transistors in the differential pair, while a resistive load and capacitive coupling form the summing node at the output. This topology acts as a multiplier: when two signals of slightly different frequency are applied to the gates, the output contains components at both the sum and difference frequencies. The high-frequency sum component is rejected by

downstream filtering, while the low-frequency difference—the beat frequency—remains. This beat signal encodes the frequency mismatch between the oscillators and forms the basis for audible detection. The differential mixer output is then routed to a common-source amplifier stage for further gain. Because the mixer operates as a nonlinear element, its performance is highly sensitive to bias conditions, making the preceding current mirror a critical enabler of consistent, reliable behavior.

First Common-Source Amplifier

The first stage of amplification consists of a PMOS common-source amplifier connected directly to the differential output of the mixer. This amplifier is biased using a fixed gate voltage V_b and operates in the saturation region to provide voltage gain. Because the mixer's output signal—representing the beat frequency between the two oscillators—is typically in the range of a few hundred hertz to several kilohertz, this amplifier is designed to offer significant gain at low frequencies while maintaining linearity. The gain is set by the transconductance of the PMOS transistor and the value of the drain resistor, and it ensures that even small beat signals (on the order of millivolts) are made clearly visible in subsequent stages. This first common-source stage is essential for distinguishing the beat frequency from background noise and mixer artifacts.

Low-Pass Filter

Following the initial amplification, the signal passes through a passive RC low-pass filter. This filter is critical for rejecting high-frequency content, particularly remnants of the oscillator sum frequency (around 100 kHz) and switching artifacts introduced by the nonlinear mixer. The cutoff frequency of the filter is chosen to be above the maximum expected beat frequency (5 kHz) but well below the oscillator range, thereby allowing the desired signal to pass while attenuating unwanted high-frequency components. In practice, this filtering step sharpens the frequency selectivity of the detector and improves the clarity and stability of the output signal, especially when driving audio hardware.

Output CS-CD Cascade Stage

The filtered signal is then passed into a second PMOS common-source amplifier for additional gain. This stage uses a similar topology and biasing scheme as the first amplifier, but it is followed immediately by a source follower (common-drain buffer) stage using an NMOS power transistor. The source follower provides a low output impedance necessary to drive the speaker load without distortion or voltage sag, particularly when delivering several milliamps of current. Together, the second CS stage and CD buffer act as the final gain and drive chain, converting a small filtered voltage signal into a strong, audible output through the speaker. This final stage is responsible for rendering the frequency-domain behavior of the oscillators into a human-perceivable tone, completing the signal path of the metal detector.

Hand Calculations

Oscillator Frequency Calculations

Each oscillator in the circuit is based on an LC tank that determines its oscillation frequency via the standard resonance formula:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

where f is the resonant frequency in hertz (Hz), L is the inductance in henries (H), and C is the capacitance in farads (F).

Oscillator A

$$L = 10 \text{ mH} = 10 \times 10^{-3} \text{ H}, \quad C = 2 \times 560 \text{ pF} = 1120 \text{ pF} = 1.12 \times 10^{-9} \text{ F}$$
$$f_A = \frac{1}{2\pi\sqrt{(10 \times 10^{-3})(1.12 \times 10^{-9})}} = \frac{1}{2\pi\sqrt{1.12 \times 10^{-11}}} \approx \frac{1}{2\pi \cdot 3.346 \times 10^{-6}} \approx 47.6 \text{ kHz}$$

Oscillator B

$$L = 9.6 \text{ mH} = 9.6 \times 10^{-3} \text{ H}, \quad C = 2 \times 560 \text{ pF} = 1120 \text{ pF} = 1.12 \times 10^{-9} \text{ F}$$
$$f_B = \frac{1}{2\pi\sqrt{(9.6 \times 10^{-3})(1.12 \times 10^{-9})}} = \frac{1}{2\pi\sqrt{1.0752 \times 10^{-11}}} \approx \frac{1}{2\pi \cdot 3.278 \times 10^{-6}} \approx 48.5 \text{ kHz}$$

These calculations predict that the oscillators will operate with a small frequency difference of about 900Hz under nominal conditions, producing a near-zero beat frequency when no metal is nearby. This small difference results in a quiet output tone, which becomes louder and more distinct when metal shifts the variable inductor's value and thus its oscillator frequency. However, in practice, the measured frequencies on the oscilloscope were slightly higher than these theoretical predictions. This behaviour is expected and likely due to the actual effective capacitance being lower than the nominal value used in calculations. Factors contributing to this include:

- **Capacitor Tolerance** The 560 pF ceramic capacitors used may have a tolerance of $\pm 10\%$, meaning their actual values could be closer to 500 pF.
- **Low Parasitic Capacitance** PCB layouts may introduce less stray capacitance than anticipated, further reducing total C .
- **Light Tank Loading** Minimal capacitive loading from the MOSFETs in the oscillator circuits results in less deviation from ideal resonance behavior.

The capacitor values of 1120pF for Oscillator A (from two 560pF capacitors in parallel) and 780pF for Oscillator B (from two 390pF capacitors in parallel) were deliberately chosen to make the measured frequency difference between the two oscillators as small as possible, even though the ideal resonance equation predicts a slightly larger separation; this ensured minimal audible output in the absence of nearby metal.

MOSFET Biasing and Region of Operation

To ensure proper operation of the amplifying and oscillator stages, it is important to verify that the MOSFETs operate in the saturation region. Saturation occurs when

$$V_{DS} > V_{GS} - V_{th}$$

where $|V_{th}| \approx 0.7$ V for both NMOS and PMOS transistors in the ALD1103 family.

However, it is also acceptable to justify saturation qualitatively by referencing the ALD1103 datasheet's I_{DS} vs. V_{DS} curves. These show that for $V_{GS} \gtrsim 2$ V, the drain current becomes relatively flat with increasing V_{DS} , indicating operation in saturation.

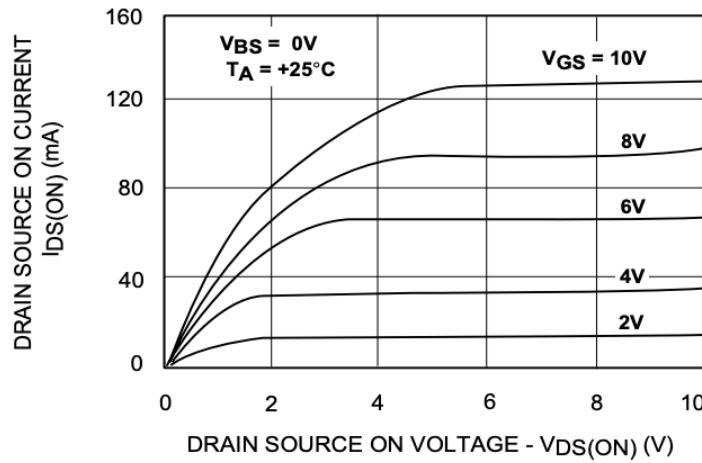


Figure 1: ALD1103 NMOS output characteristics showing saturation behavior at $V_{GS} = 2$ V.
Source: ALD1103 datasheet [1].

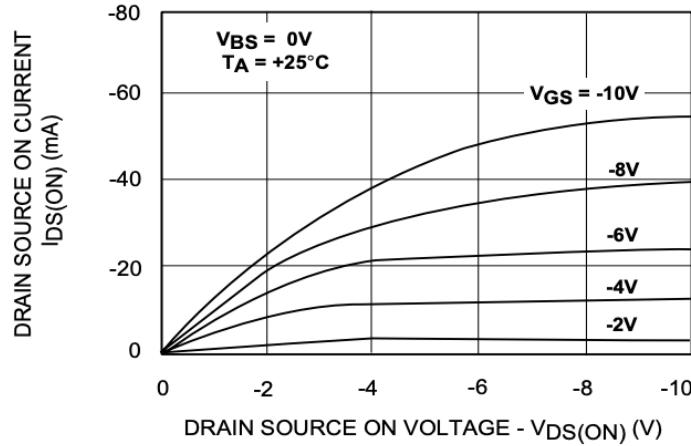


Figure 2: ALD1103 PMOS output characteristics showing saturation behavior at $V_{GS} = -2$ V.
Source: ALD1103 datasheet [1].

These curves confirm that the transistor enters saturation at relatively low V_{DS} values for $|V_{GS}| = 2$ V, validating the use of this bias voltage in our design. While this justification confirms that $|V_{GS}| \approx 2$ V

ensures saturation, we now proceed to apply this design target to bias the transistors in our circuit. Specifically, we use this criterion to compute appropriate gate voltages via resistive dividers from the 5 V supply. For each stage of the circuit, we identify the NMOS and PMOS transistors and determine resistor values that yield gate voltages satisfying $|V_{GS}| \approx 2$ V, thereby ensuring saturation while maintaining simplicity and symmetry in the biasing network.

To support our analysis, we estimate the MOSFET drain current equations in the saturation region using empirical data from the ALD1103 datasheet. The idealized drain current in saturation is given by

$$I_D = \frac{1}{2}k' \frac{W}{L} (V_{GS} - V_{TH})^2$$

for NMOS transistors, and

$$I_D = \frac{1}{2}k' \frac{W}{L} (V_{SG} - |V_{TH}|)^2$$

for PMOS transistors, where k' is the process transconductance parameter and W/L is the transistor aspect ratio.

NMOS Estimation:

According to the ALD1103 datasheet, an NMOS device biased at $V_{GS} = 2$ V conducts $I_D = 200 \mu\text{A}$, and has a threshold voltage of $V_{TH} \approx 0.74$ V. Substituting into the NMOS equation

$$\begin{aligned} 200 \times 10^{-6} &= \frac{1}{2}k' \frac{W}{L} (2 - 0.74)^2 = \frac{1}{2}k' \frac{W}{L} \cdot (1.26)^2 \\ &\Rightarrow \frac{1}{2}k' \frac{W}{L} \approx \frac{200 \times 10^{-6}}{1.5876} \approx 126 \mu\text{A/V}^2 \end{aligned}$$

PMOS Estimation:

Similarly, for the matched PMOS transistor in the ALD1103, the datasheet specifies $I_D = 200 \mu\text{A}$ at $V_{SG} = 2$ V with $|V_{TH}| \approx 0.74$ V. Substituting

$$\begin{aligned} 200 \times 10^{-6} &= \frac{1}{2}k' \frac{W}{L} (2 - 0.74)^2 = \frac{1}{2}k' \frac{W}{L} \cdot (1.26)^2 \\ &\Rightarrow \frac{1}{2}k' \frac{W}{L} \approx 126 \mu\text{A/V}^2 \end{aligned}$$

Therefore, for both NMOS and PMOS devices in this project, we use the following saturation region model

$$I_D \approx 126 \mu\text{A/V}^2 \cdot (V_{GS} - V_{TH})^2 \quad (\text{NMOS}), \quad I_D \approx 126 \mu\text{A/V}^2 \cdot (V_{SG} - |V_{TH}|)^2 \quad (\text{PMOS})$$

Oscillator A and B

Oscillator A and B share the same symmetric topology, consisting of a cross-coupled NMOS pair and PMOS current source loads, forming a positive feedback loop that sustains oscillation. The biasing network applies a supply voltage of $V_{DD} = 5$ V across resistive dividers to establish gate, source, and drain voltages. Importantly, this topology inherently ensures that all transistors operate in the saturation region during normal oscillation.

In the cross-coupled configuration, the NMOS transistors have their drains connected to the gates of the opposite device. As one NMOS begins to conduct more than the other, it pulls its drain voltage lower, which in turn reduces the gate voltage of the other NMOS, further turning it off. This regenerative switching behavior requires high gain and is only possible if the NMOS devices remain in saturation. Structurally, this is achieved by maintaining the NMOS sources near ground and allowing the drains to swing close to V_{DD} , producing a large V_{DS} .

The PMOS devices are configured as diode-connected current sources, with their sources near V_{DD} and their gates biased below this value through large resistors. Because the drains of the PMOS transistors swing toward ground, the V_{SD} remains large throughout oscillation. As a result, the PMOS devices also remain in saturation and provide high output impedance, which is essential for sustaining oscillations.

In this design, the choice of resistor values and the full 5 V supply ensures sufficient gate-source voltage to place all transistors in their intended regions. Moreover, the very structure of the oscillator—particularly its use of positive feedback and full-swing differential nodes—guarantees that both NMOS and PMOS transistors operate in saturation without needing individual bias point calculations.

This structural saturation is supported qualitatively by the ALD1103 datasheet, which shows that $|V_{GS}| \approx 2$ V ensures saturation for both NMOS and PMOS devices. Our oscillator design naturally meets and exceeds this threshold throughout its operation.

Mixer Stage Biasing

There are 6 transistors to account for in the mixer stage: two from the PMOS Loads for the differential pair, two NMOS transistors from the differential pair, and two NMOS transistors from the current mirror that sets the tail current of the differential pair.

The NMOS transistors in the current mirror were biased to 2V at their V_G as their sources were grounded. This allowed V_{GS} to be 2V, and thus allow the saturation to be satisfied as previously discussed through analysis of the ALD1103N's output characteristics. Since this gate voltage was set by the $10k\Omega$ potentiometer RV_3 , to drop from 5V VDD, the potentiometer was set to enable a value of $6k\Omega$ drop before the gate and a $4k\Omega$ drop to GND. The saturation current through the NMOS tail current setter can be found using the previously established empirical model, where $V_{GS} = 2V$.

$$I_D \approx 126 \mu A/V^2 \cdot (V_{GS} - V_{TH})^2$$

with $V_{TH} = 0.74$ V, we calculate the drain current as:

$$I_D = 126 \times 10^{-6} \cdot (2 - 0.74)^2 = 126 \times 10^{-6} \cdot (1.26)^2 = 126 \times 10^{-6} \cdot 1.5876 \approx 200 \mu A$$

Therefore, the tail current delivered by the mirrored NMOS device is approximately $200 \mu A$.

In the mixer stage, both NMOS transistors forming the differential pair receive the same AC input signal, composed of the sum of oscillator outputs $V_{osc1} + V_{oscA}$. However, one of the gates is connected through a large resistor, which introduces a slight DC voltage drop relative to the other gate. As a result, both gates share the same time-varying AC waveform, but have slightly different DC levels.

This configuration creates a small DC differential across the two gates, which in turn leads to asymmetric current splitting through the differential pair. The transistor with the higher DC gate voltage draws slightly more current, while the other draws less, though the total current is constrained by the NMOS current mirror tail to approximately $200 \mu A$.

Despite this imbalance, both transistors remain in the saturation region. As found through the LTSpice analysis, the source node in common sits near $V_S \approx 0.9$ V, while the gates oscillate around a DC level of approximately 2 V as derived by tuning the $100k\Omega$ RV_1 to enable a value of $60k\Omega$ drop before the gate and a $40k\Omega$ drop to GND. Thus:

$$V_{GS} \approx 2 - 0.9 = 1.1 \text{ V}$$

With drain voltages pulled near $V_D = 5$ V by the active PMOS loads, we have:

$$V_{DS} \approx V_D - V_S = 5 - 0.9 = 4.1 \text{ V}$$

Comparing this with the saturation requirement:

$$V_{DS} > V_{GS} - V_{TH} = 1.1 - 0.74 = 0.36 \text{ V}$$

confirms that both NMOS transistors remain in saturation. The use of the $1 M\Omega$ resistor provides sufficient gate bias separation to enable differential current response while preserving linearity and proper operating region for both transistors.

For the PMOS transistors, where the sources direct to VDD (5V), and the gates both connect to the drain of one of the NMOS transistors from the diff pair. The drain of PMOS₁ is connected

to the gate of PMOS₁, meaning it is diode connected. This allows for the saturation condition to be vacuously satisfied as $|V_{DS}| > |V_{GS} - V_{THP}|$ is always true when $V_D = V_G$, as is the case for PMOS₁. PMOS₂, the active load for one side of the differential pair, is not diode-connected. Its gate is tied to $V_G = 2$ V, its source is connected to $V_S = V_{DD} = 5$ V, and its drain is tied to the drain of the NMOS differential pair transistor that receives the lower DC gate voltage. From simulation, this drain node sits at approximately $V_D \approx 2.63$ V.

To verify that PMOS₂ operates in saturation, we check the standard saturation condition

$$V_{SD} > V_{SG} - |V_{TH}|$$

The relevant voltages are

$$V_{SG} = V_S - V_G = 5 - 2 = 3 \text{ V}$$

$$V_{SD} = V_S - V_D = 5 - 2.63 = 2.37 \text{ V}$$

$$V_{SG} - |V_{TH}| = 3 - 0.74 = 2.26 \text{ V}$$

Substituting yields

$$V_{SD} = 2.37 \text{ V} > 2.26 \text{ V}$$

Therefore, PMOS₂ is confirmed to operate in the saturation region. This ensures it provides high output impedance, allowing for proper current steering and differential signal amplification in the mixer stage.

Mixer & Output Stage CS Amplifier Biasing

The PMOS common-source (CS) amplifier following the differential pair serves to amplify the mixed oscillator output. To ensure proper operation in the saturation region, the gate voltage must be selected to achieve the desired $|V_{SG}| = 2 \text{ V}$, given that the source of the PMOS is tied to $V_{DD} = 5 \text{ V}$. This implies a gate voltage of:

$$V_G = V_S - V_{SG} = 5 \text{ V} - 2 \text{ V} = 3 \text{ V}$$

To generate this bias voltage, the gate is driven by a resistive voltage divider implemented using a potentiometer between V_{DD} and ground. The potentiometer was tuned to produce a $40 \text{ k}\Omega$ drop from 5 V to the gate node, followed by a $60 \text{ k}\Omega$ drop from the gate to ground, yielding the desired 3 V gate voltage. This configuration ensures that the PMOS operates well within the saturation region, enabling high gain and linear amplification of the downconverted mixer output.

An identical biasing strategy is employed for the subsequent PMOS CS amplifier in the output stage, following the low-pass filter. In this case, the potentiometer RV_4 was adjusted similarly to achieve the same 3 V gate bias for consistent amplification.

Output Stage CD Amplifier Biasing

The final stage of the signal chain employs an NMOS CD amplifier to buffer the amplified signal before driving the speaker load. In this configuration, the drain is tied directly to $V_{DD} = 5 \text{ V}$, and the output is taken from the source, which drives an 8Ω speaker.

To ensure operation in the saturation region and sufficient headroom, we selected $V_{GS} \approx 2 \text{ V}$ as a design target. Using the empirical saturation current model derived from the ALD1103 datasheet

$$I_D = 126 \mu\text{A}/\text{V}^2 \cdot (V_{GS} - V_{TH})^2$$

with $V_{TH} = 0.74 \text{ V}$, we compute the drain (and source) current as:

$$I_D = 126 \times 10^{-6} \cdot (2 - 0.74)^2 = 126 \times 10^{-6} \cdot 1.5876 \approx 200 \mu\text{A}$$

The corresponding source voltage, across the 8Ω speaker, is:

$$V_S = I_D \cdot R_L = 200 \times 10^{-6} \cdot 8 = 1.6 \text{ mV}$$

To maintain the desired $V_{GS} = 2 \text{ V}$, the gate voltage must be set to:

$$V_G = V_S + V_{GS} \approx 1.6 \text{ mV} + 2 \text{ V} = 2.0016 \text{ V} \approx 2 \text{ V}$$

This gate voltage was produced using a $100 \text{ k}\Omega$ potentiometer RV_5 , tuned to drop $60 \text{ k}\Omega$ from 5 V to the gate and $40 \text{ k}\Omega$ from the gate to ground, thereby setting the gate to approximately 2 V. This ensures that the transistor operates in saturation while providing low output impedance for effective signal buffering to the speaker.

Filter Stage Capacitor

In the original design, a low-pass filter was placed after the mixer stage to suppress high-frequency components resulting from the multiplication of the two oscillator signals. This filter typically consists of an RC network, where a capacitor is placed to ground at the node between the CS amplifier and the subsequent output stage. However, through experimental testing, it was observed that removing the capacitor entirely (such that the circuit relied on just the series resistor) led to a clearer and more responsive audio signal, especially when metal was present near the sensing coil.

This behaviour can be explained by considering the nature of the signal generated at the output of the mixer. The mixer produces a sum of frequencies, with the most important component being the difference frequency, which falls within the audible range. However, if the capacitor in the low-pass filter is too large, or if the cutoff frequency is too low, even these desirable difference frequencies can be attenuated, resulting in reduced volume or distortion of the output signal.

In addition, the subsequent stages - particularly the CS and CD amplifiers - inherently provide some bandwidth limitation due to their parasitic capacitances and the finite gain-bandwidth product of the MOSFETs. Thus, an explicit capacitor may be redundant or even detrimental, especially if it reduces the signal amplitude below the threshold needed to drive the speaker effectively.

Therefore, by omitting the capacitor from the RC filter, the system preserves the critical low-frequency content while still attenuating higher-frequency components through the natural roll-off of the circuit. This simplification led to a louder and more accurate output tone, with clearer differentiation between metal-present and metal-absent conditions, justifying its exclusion in the final design.

Nevertheless, it is informative to consider what the filter response would have been if the capacitor had been included. With a series resistance of $R = 100\Omega$, and a capacitor C placed from the signal node to ground, the resulting RC low-pass filter would exhibit a -3 dB cutoff frequency given by:

$$f_c = \frac{1}{2\pi RC}$$

Assuming a target cutoff frequency of $f_c = 5\text{ kHz}$, selected to preserve the difference frequencies generated by the mixer (typically in the audible range), the required capacitor value would be:

$$C = \frac{1}{2\pi \cdot 100\Omega \cdot 5000\text{ Hz}} \approx 318\text{ nF}$$

Although this value is more reasonable for practical implementation than larger values associated with lower cutoffs, testing revealed that even this modest capacitor led to reduced volume and responsiveness. This is because as metal is introduced and the beat frequency increases, the signal's spectral energy shifts toward and beyond the cutoff point, causing attenuation precisely when stronger output is desired.

Additionally, the inherent parasitic capacitances of the CS and CD amplifier stages - particularly gate-drain and gate-source capacitances - already introduce high-frequency roll-off. The addition of a discrete filter capacitor compounded this effect and led to over-filtering. Therefore, omitting the capacitor preserved more of the signal's amplitude variation across frequency shifts and yielded better auditory sensitivity to nearby metallic objects.

Output CS Amplifier Drain Resistor

The drain resistor for the output PMOS common-source (CS) amplifier was chosen to be $R_D = 10\text{ k}\Omega$ in order to maximize voltage gain while still permitting sufficient headroom and signal swing in the amplified output. Since the output stage primarily drives the gate of a high-input-impedance common-drain (CD) buffer, there is minimal current demand, allowing a higher resistance without compromising bandwidth or stability.

To assess the implications of this design choice, we use the small-signal voltage gain formula for a transistor in saturation:

$$A_V = -g_m R_D$$

The empirical drain current model for the ALD1103 PMOS at the chosen bias point $V_{SG} = 2\text{ V}$ and threshold voltage $|V_{TH}| = 0.74\text{ V}$ gives:

$$I_D = 126\text{ }\mu\text{A/V}^2 \cdot (2 - 0.74)^2 = 126 \times 10^{-6} \cdot 1.5876 \approx 200\text{ }\mu\text{A}$$

The corresponding transconductance is:

$$g_m = \frac{2I_D}{V_{SG} - |V_{TH}|} = \frac{2 \cdot 200 \times 10^{-6}}{1.26} \approx 317\text{ }\mu\text{S}$$

Substituting into the gain equation:

$$A_V = -g_m R_D = -317 \times 10^{-6} \cdot 10\,000 = -3.17$$

$$A_V \approx -3.17$$

This gain was desirable for significantly amplifying the weak difference-frequency signal emerging from the mixer stage. It enhanced the signal amplitude while preserving fidelity, enabling the downstream CD stage to drive the speaker more effectively. The $10\text{ k}\Omega$ resistance thus represented a balanced choice between high gain and acceptable biasing margins.

Simulation Results

To verify circuit functionality prior to hardware implementation, the full metal detector system was simulated in LTspice. The simulated circuit includes all major blocks: the fixed and variable LC oscillators, the mixer stage formed by a differential pair, a PMOS common-source amplifier, an RC low-pass filter, and a final common-drain (CD) amplifier for buffering the output. Time-domain waveforms were collected at key nodes to observe the generation, mixing, and propagation of the beat frequency signal. Some component values were modified relative to the hardware design to ensure oscillator startup and stable simulation. The fixed oscillator was designed to operate near 50kHz, and the variable oscillator near 49kHz, using a 9.6mH inductor - the experimentally measured inductance of the variable inductor - with appropriately tuned capacitors. These values allowed observable beat behavior while ensuring simulation convergence.

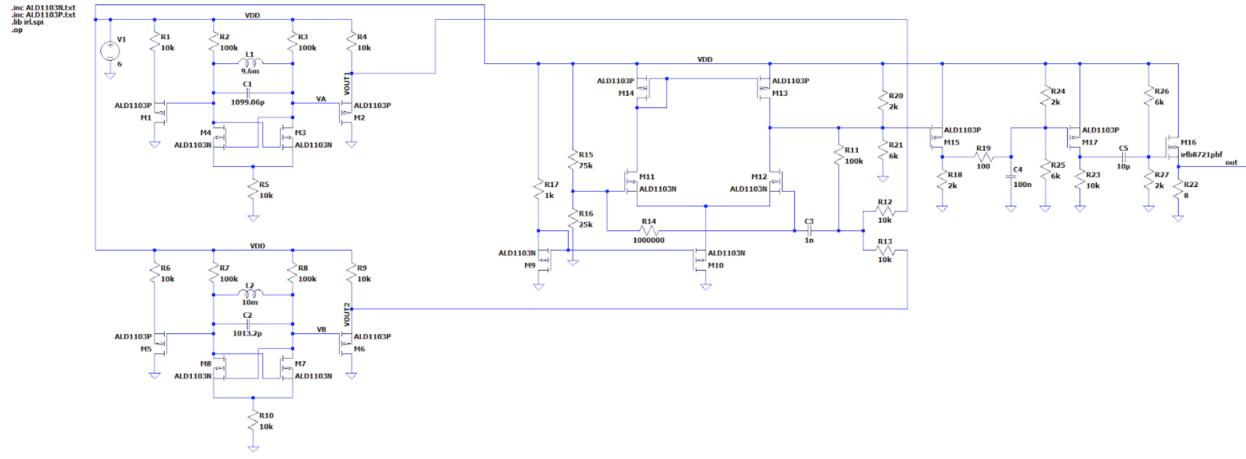


Figure 3: Complete LTSpice Schematic

Oscillator A & B Outputs

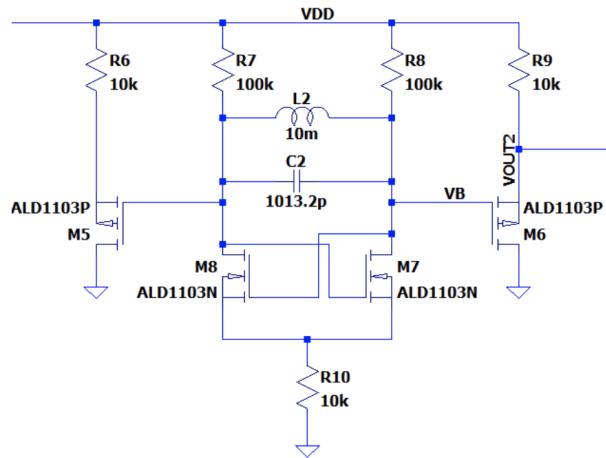


Figure 4: Oscillator A with an inductance of 10mH and capacitance of 1013.2pF to yield a 50kHz frequency from the LC tank

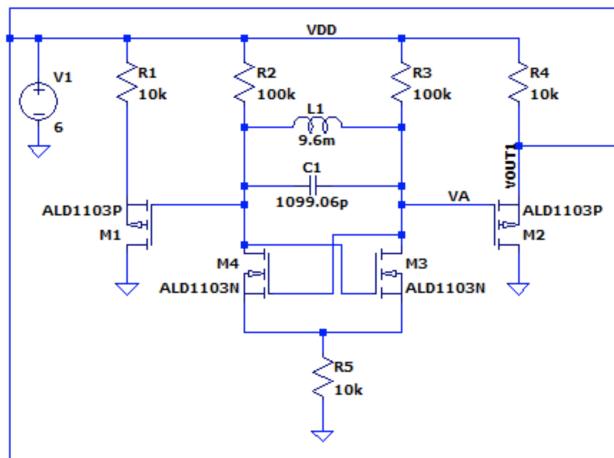


Figure 5: Oscialltor B with inductance of 9.6mH and capacitance of 1099.06pF to yield a 49kHz frequency from the LC tank

The output of each oscillator was probed to confirm periodic behavior at the expected frequencies. The two signals exhibit slight differences in frequency, which is necessary for beat frequency generation in the mixer.

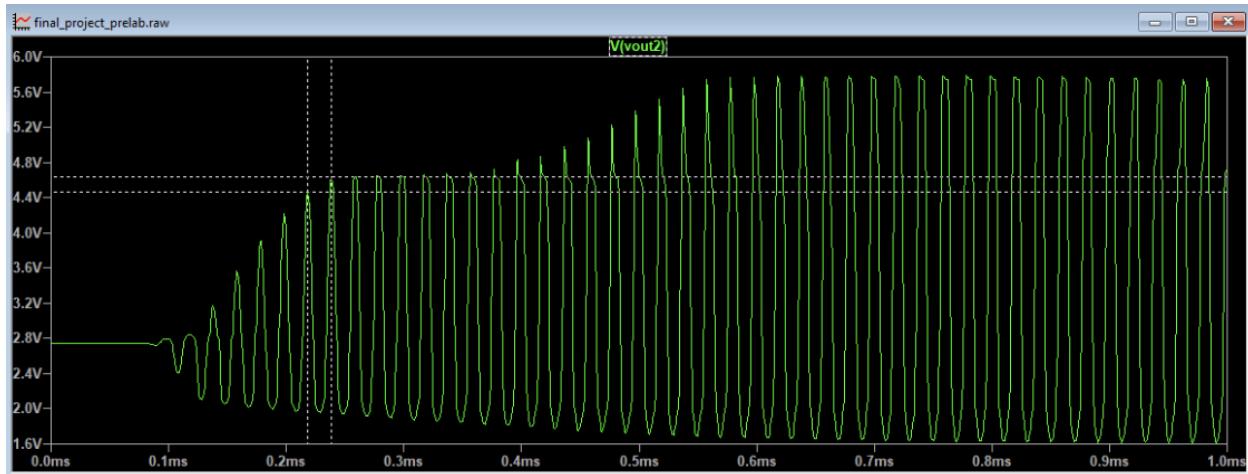


Figure 6: Output seen from Oscillator A

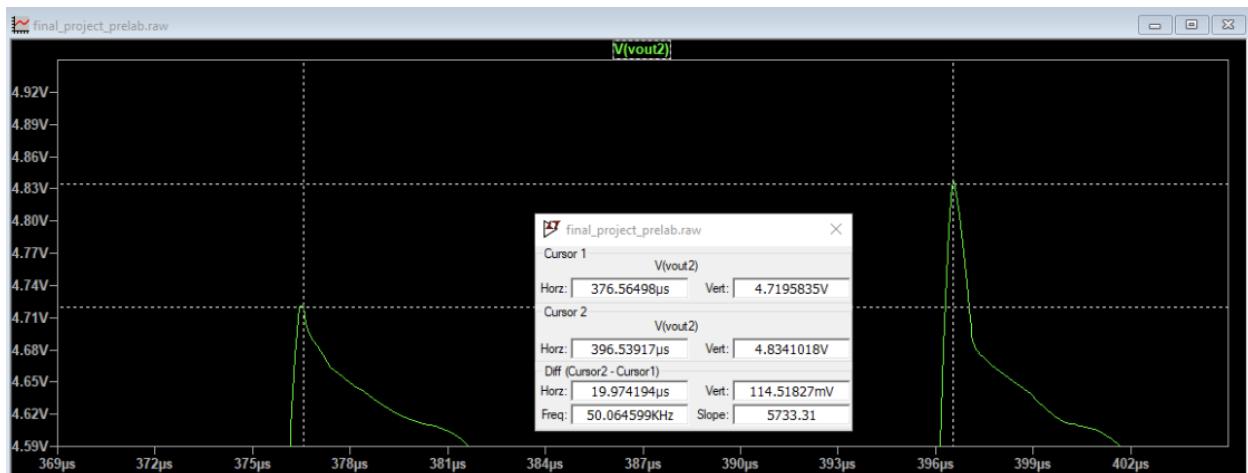


Figure 7: Zoomed in shot of Oscillator A output showing a fixed oscillator frequency of approximately 50,065 Hz

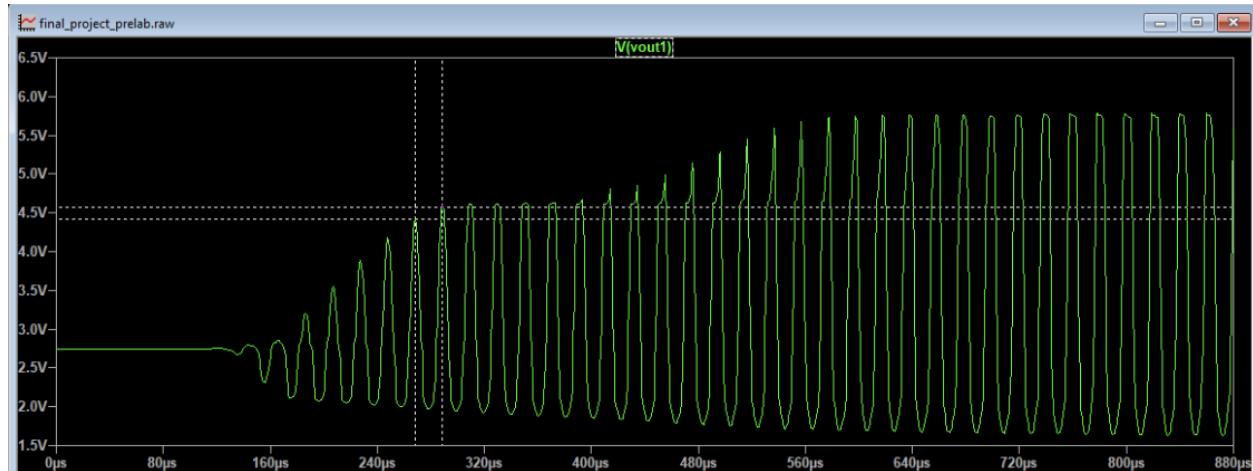


Figure 8: Output seen from Oscillator B

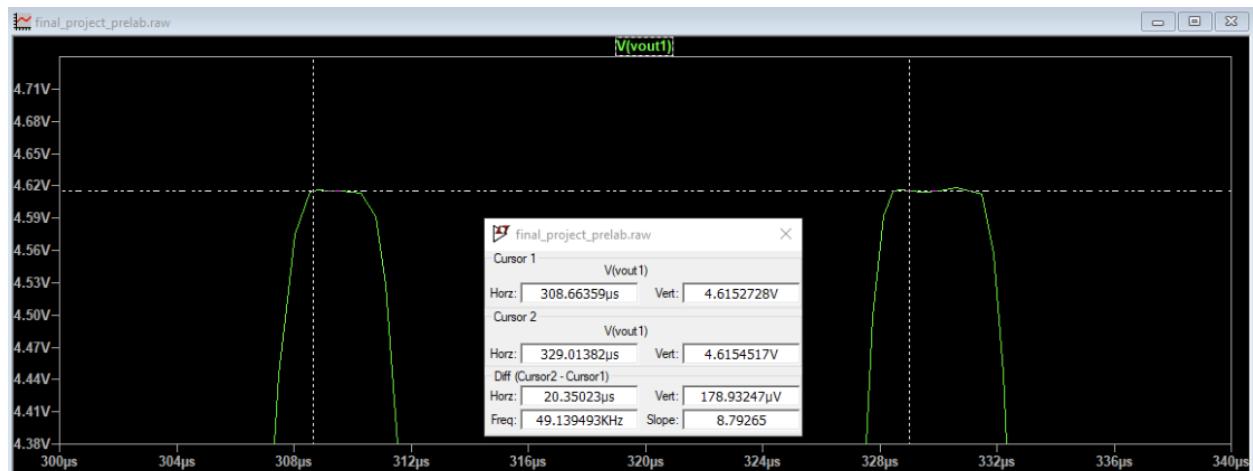


Figure 9: Zoomed in shot of Oscillator A output showing a fixed oscillator frequency of approximately 49,139 Hz

Oscillator Frequency & Capacitance Calculations

The frequency of oscillation for each LC tank oscillator is given by the formula:

$$f = \frac{1}{2\pi\sqrt{LC}} \Rightarrow C = \frac{1}{(2\pi f)^2 L}$$

where f is the desired oscillation frequency in hertz, L is the inductance in henries, and C is the resulting capacitance in farads.

Oscillator A (Fixed)

$$f = 50 \text{ kHz} = 5.0 \times 10^4 \text{ Hz}, \quad L = 10 \text{ mH} = 10 \times 10^{-3} \text{ H}$$

$$C = \frac{1}{(2\pi \cdot 5.0 \times 10^4)^2 \cdot 10 \times 10^{-3}} = \frac{1}{(3.1416 \times 10^5)^2 \cdot 10^{-2}}$$
$$C \approx \frac{1}{9.8696 \times 10^{10} \cdot 10^{-2}} = \frac{1}{9.8696 \times 10^8} = 1013.2 \text{ pF}$$

Oscillator B (Variable)

$$f = 49 \text{ kHz} = 4.9 \times 10^4 \text{ Hz}, \quad L = 9.6 \text{ mH} = 9.6 \times 10^{-3} \text{ H}$$

$$C = \frac{1}{(2\pi \cdot 4.9 \times 10^4)^2 \cdot 9.6 \times 10^{-3}} = \frac{1}{(3.0788 \times 10^5)^2 \cdot 9.6 \times 10^{-3}}$$
$$C \approx \frac{1}{9.4752 \times 10^{10} \cdot 9.6 \times 10^{-3}} = \frac{1}{9.0962 \times 10^8} = 1099.06 \text{ pF}$$

The resulting capacitance values of 1013.2pF and 1099.06pF were used in the LTspice simulations to target fixed oscillator frequencies of 50kHz and 49kHz respectively.

Summary

Using the resonance equation, the necessary capacitance values were calculated to yield two oscillator frequencies approximately 1kHz apart. This intentional frequency offset establishes the foundation for beat-frequency generation in the mixer stage. The simulated time-domain waveforms confirm stable oscillations at the desired frequencies, validating the correct operation of the LC tank circuits in both oscillator branches.

Mixer Stage Output

The mixer stage is implemented using a differential pair of NMOS transistors, which receive the outputs of Oscillator A and Oscillator B as their respective gate inputs. The tail current is sourced by a PMOS transistor biased to operate in saturation from a current mirror. The mixer performs nonlinear multiplication of the two high-frequency oscillator signals, and its output contains both sum and difference frequency components.

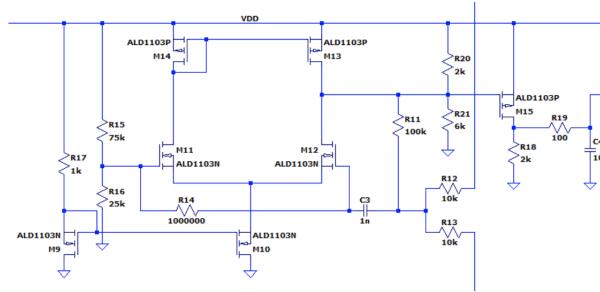


Figure 10: Summing amplifier cascaded with CS amplifier and filter

In particular, the difference frequency - known as the beat frequency - appears as an amplitude modulation envelope on the mixer output. This beat frequency is the key signal used for metal detection, as it changes based on the shift in the variable oscillator frequency due to inductance perturbations from nearby metal.

Standard Case: 9.6mH Variable Inductor

Figure 11 shows the time-domain output of the mixer when the variable inductor is set to its standard value of 9.6mH. From the waveform, we observe periodic amplitude modulation with a beat frequency of approximately 985Hz.

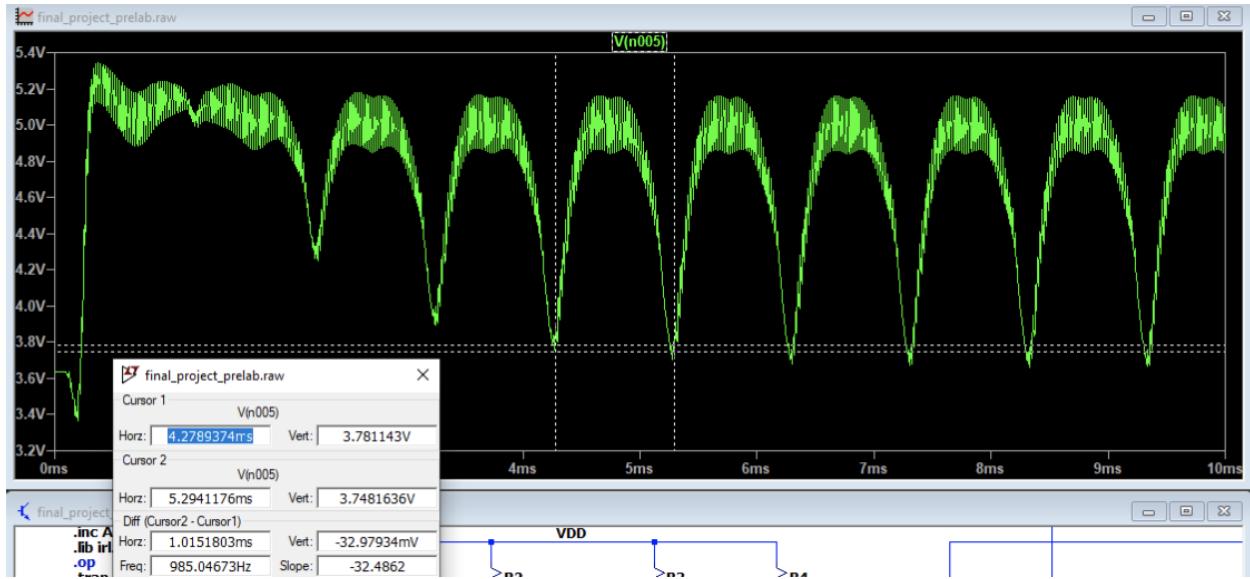


Figure 11: Mixer output with normal inductance. Frequency approximately 985.05Hz

Case with 5% Increase in Variable Inductor: 10.08mH

To simulate the presence of nearby metal, the inductance of the variable oscillator was increased by 5%, resulting in a new inductance of 10.08mH. This shifts its resonant frequency lower, thereby increasing the frequency difference with the fixed oscillator. As seen in Figure 12, this results in a higher beat frequency of approximately 2151Hz.

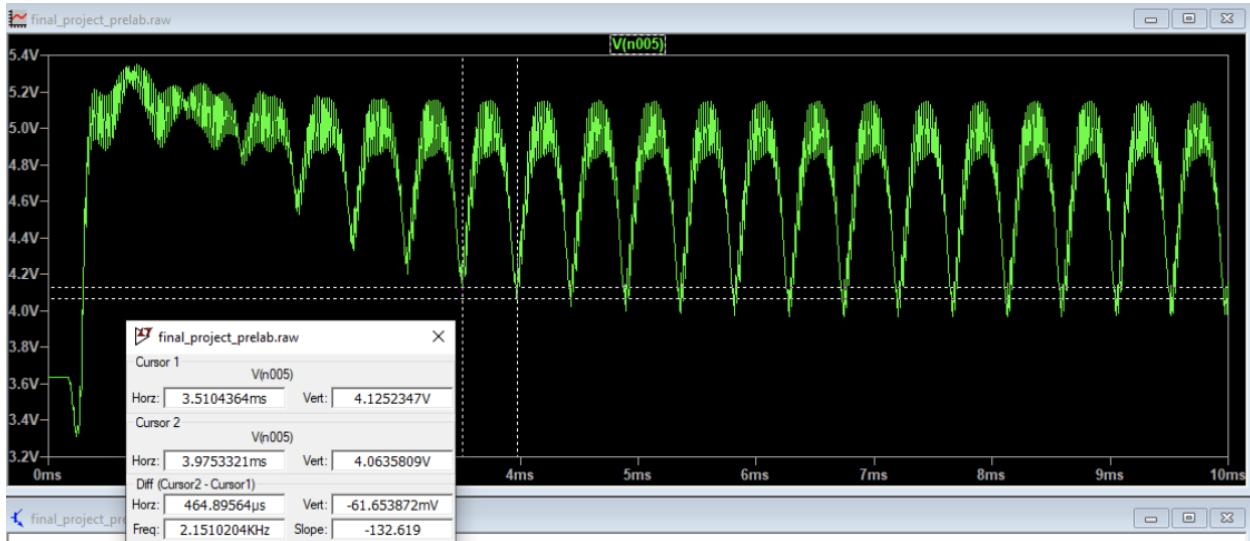


Figure 12: Mixer output with 5% increased inductance. Frequency approximately 2151Hz

Summary

The mixer stage successfully generates a beat frequency corresponding to the difference between the two oscillator frequencies. In the baseline configuration, a 985Hz signal is produced, which shifts to 2151Hz when the variable inductor is increased by 5%. This validates the mixer's ability to detect small changes in inductance, which is fundamental to the metal detection mechanism.

CS-CD Output Stage Output

The output stage of the metal detector circuit consists of a cascaded Common-Source (CS) and Common-Drain (CD) amplifier. This configuration serves two key purposes: the CS stage provides voltage gain to amplify the beat signal passed from the previous stages, while the CD (source follower) stage provides buffering to drive the low-impedance load of a speaker. Together, the CS-CD structure ensures that the low-frequency beat tone is both amplified and preserved with minimal distortion.

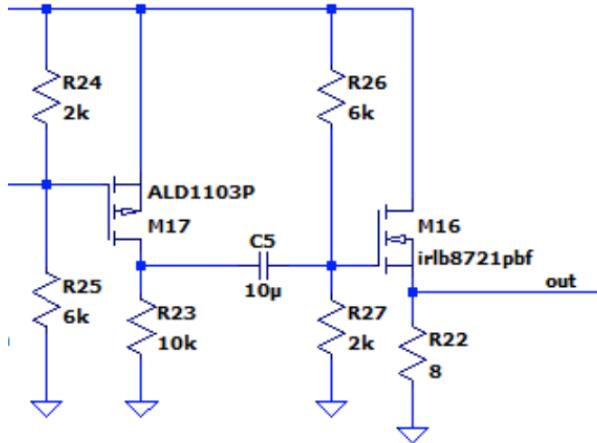


Figure 13: CS-CD output stage schematic

Standard Case: 9.6 mH Variable Inductor

In the baseline case, where the variable oscillator uses a 9.6mH inductor, the frequency difference between the oscillators generates a beat tone of approximately 985Hz. As shown in Figure 14, this signal is amplified and buffered through the output stage. The resulting waveform exhibits a clear periodic structure with a measured frequency of approximately 977.77Hz.

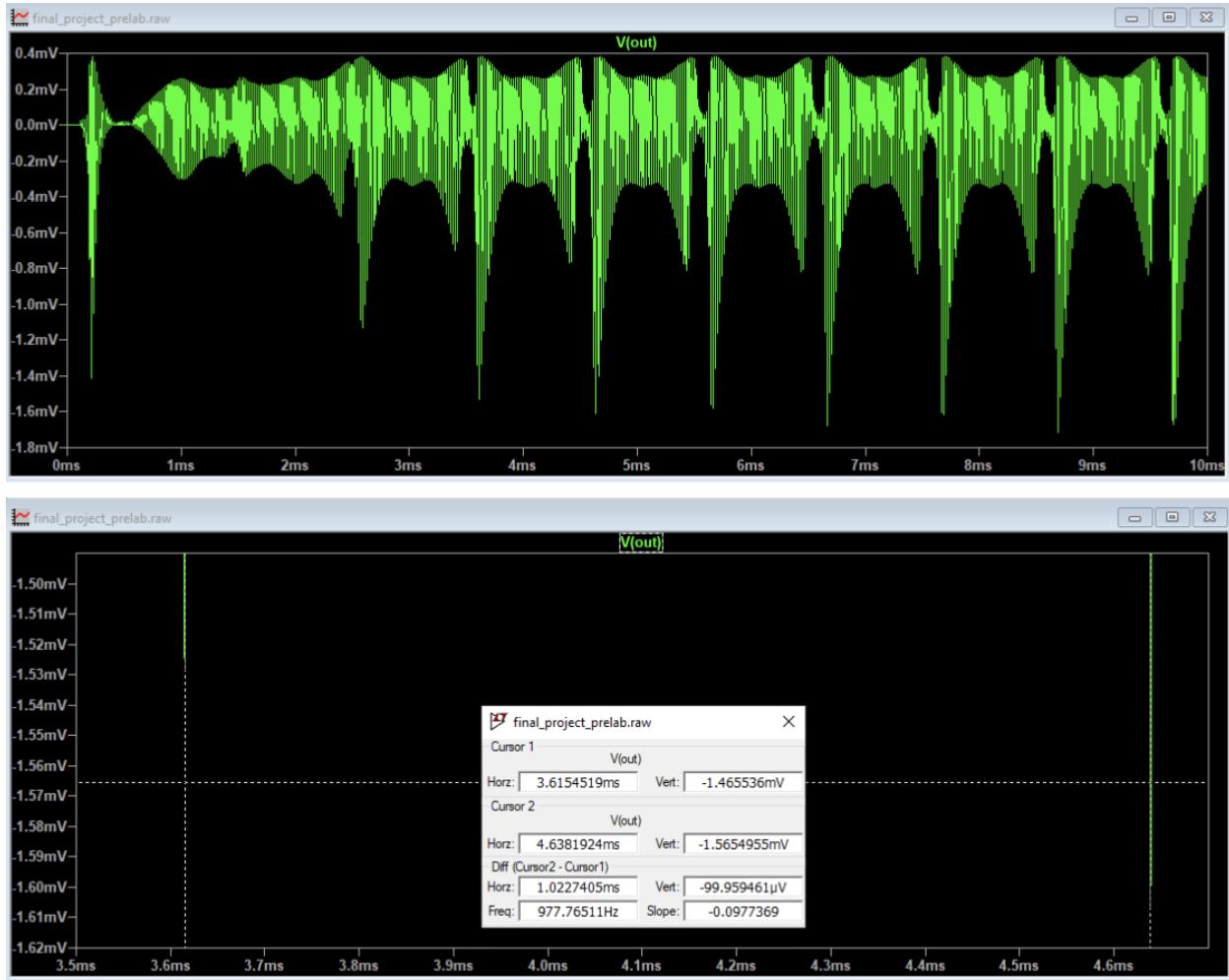


Figure 14: Output stage output with normal inductance. Frequency approximately 977.77Hz

Case with 5% Increase in Variable Inductor: 10.08mH

When the inductance in the variable oscillator increases by 5%, its resonant frequency decreases, and the beat frequency increases. Figure 15 shows the output stage response under these conditions. The beat signal now appears at a higher frequency, with the measured value approximately 2.166 kHz. This change is clearly visible in both the waveform's periodicity and its frequency measurement cursor.

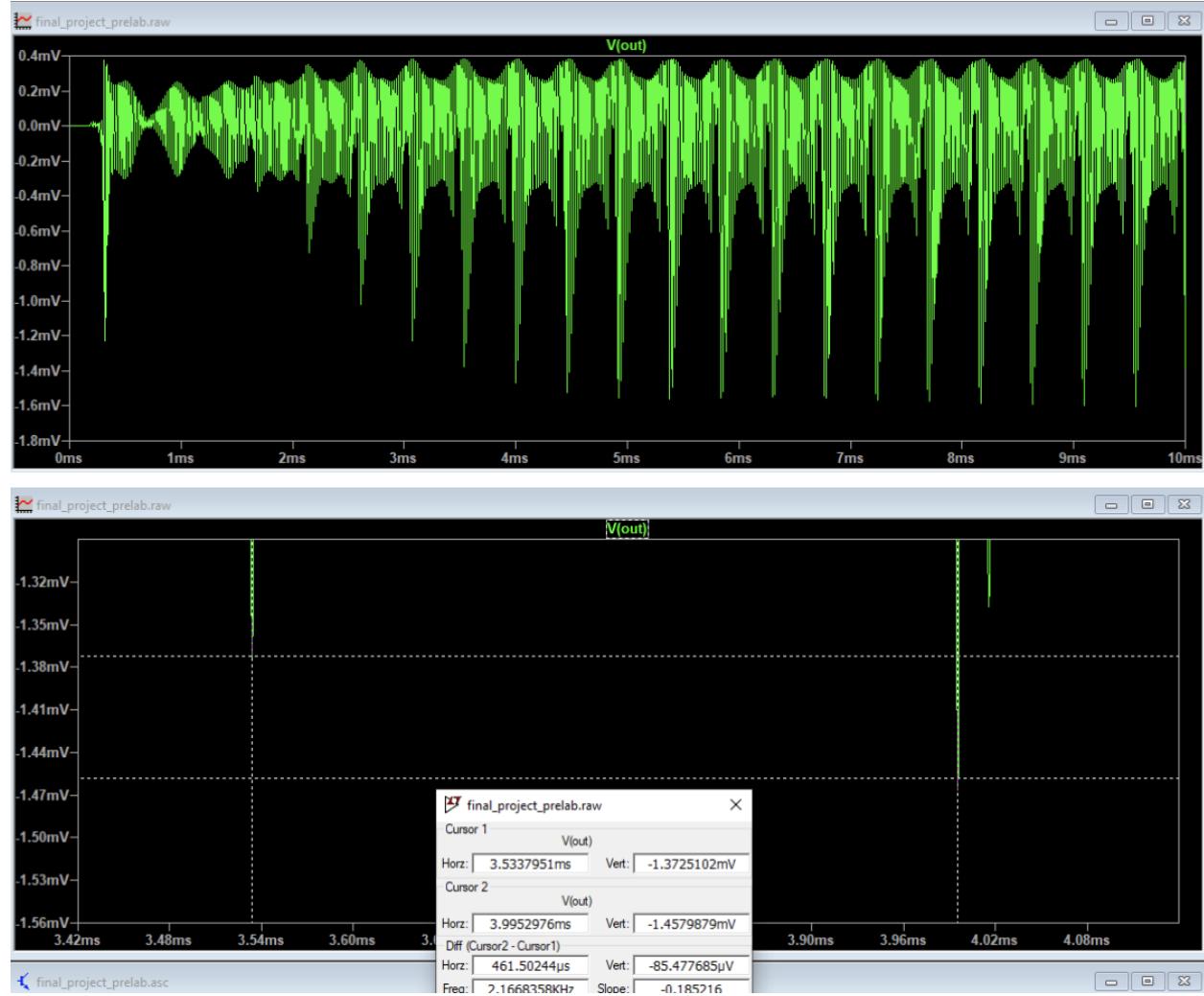


Figure 15: Output stage output with 5% increased inductance. Frequency approximately 2.166 kHz

Summary

The CS-CD output stage effectively amplifies and buffers the beat signal generated earlier in the circuit. Its response closely tracks the beat frequency shift caused by changes in the variable inductor, demonstrating the system's sensitivity to inductive perturbations. The output signal maintains both amplitude and waveform integrity, making it suitable for audio output and clear metal detection.

PCB Layout

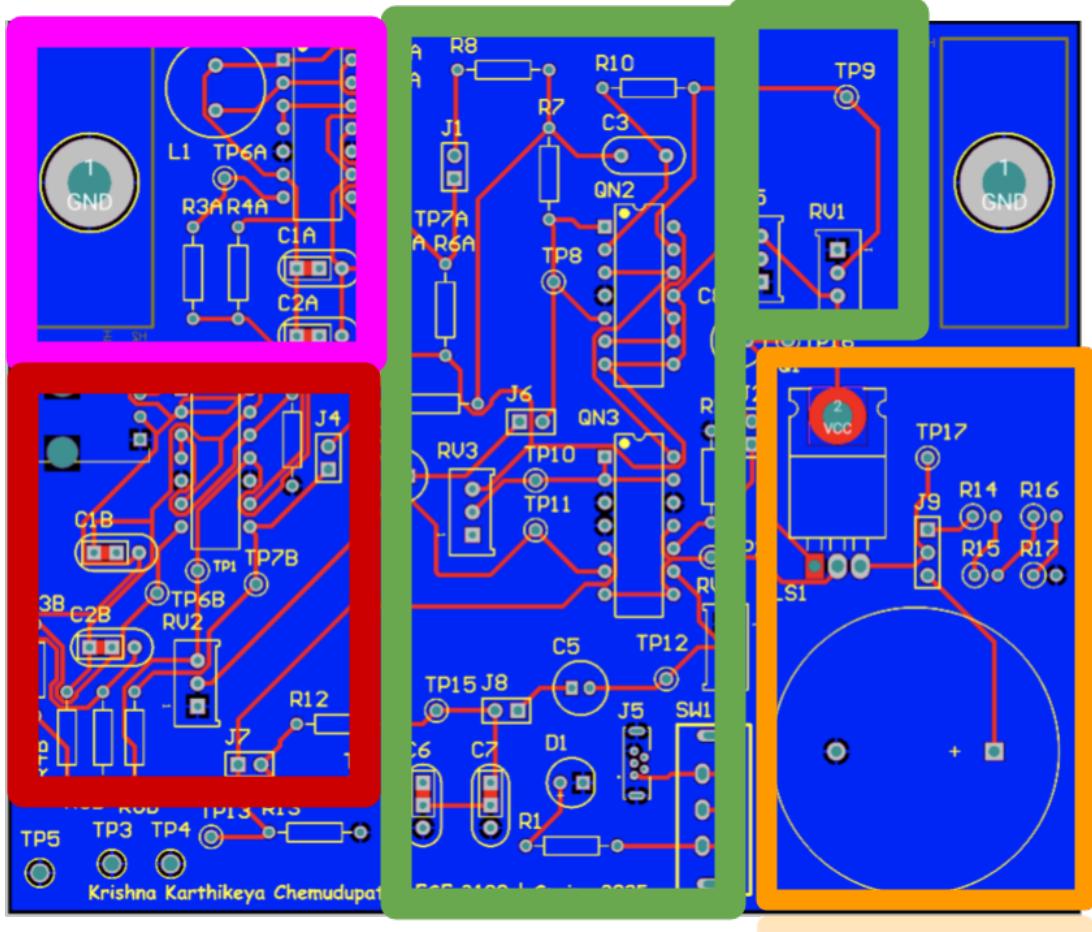


Figure 16: Layout of PCB

In the figure above, the layout of the PCB is shown. The section highlighted in pink corresponds to Oscillator A; the section in red corresponds to Oscillator B; the section in green contains the mixer stage, the common-source (CS) amplifier prior to the filter, the RC low-pass filter, and the CS amplifier after filtering; and the section in orange contains the final common-drain (CD) amplifier output stage. The block-level modularity of the PCB layout reflects the signal chain architecture of the system.

The layout was performed using Altium Designer following a cloned project template provided by the ESE 3190 course. Components were arranged with physical separation between stages to minimize crosstalk and allow for straightforward probing during hardware validation. Special attention was given to the placement of J3 (the variable inductor header), which was required to be on the board edge for mechanical accessibility. The PCB also passed all Design Rule Checks (DRC) and was successfully verified using Oshpark's fabrication preview.

Power integrity was ensured through strategic placement of decoupling capacitors and implementation of a bottom-layer ground pour, providing a low-impedance return path for analog currents. Vias were used judiciously to connect traces between layers, and the design respected the

mounting hole constraints imposed by the PVC housing template, visible as the green guide box in Altium. Resistor values were intentionally chosen to be physically adjustable via potentiometers (e.g., RV_3 , RV_4 , RV_5), and labeled appropriately on the silkscreen for accessibility during tuning.

Overall, the PCB layout was completed within the 100mm by 120mm constraint and followed all submission protocols, including name annotation, correct project folder placement on Altium365, and fabrication file export.

Measurement Results

Oscilloscope measurements were captured at key stages of the circuit to validate functional behavior and confirm that the difference-frequency response varies in the presence of nearby metal. Each stage was characterized using both time-domain and frequency-domain views, under two conditions: without metal and with metal near the sensing coil.

Oscillator Outputs

Oscillator A and Oscillator B were designed to produce nearly identical frequencies under normal conditions. The beat frequency becomes audible only when one oscillator is detuned by the presence of metal. Below are time and frequency domain plots from each oscillator output node, comparing behavior with and without nearby metal.

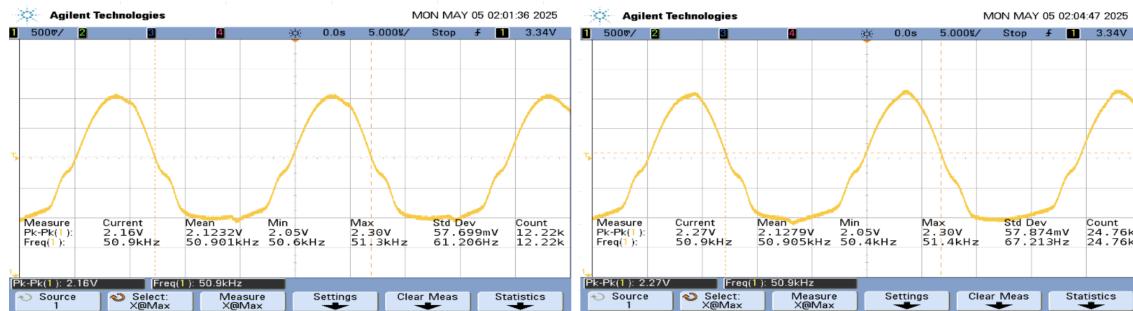


Figure 17: Oscillator A output (time-domain). Left: no metal. Right: with metal.

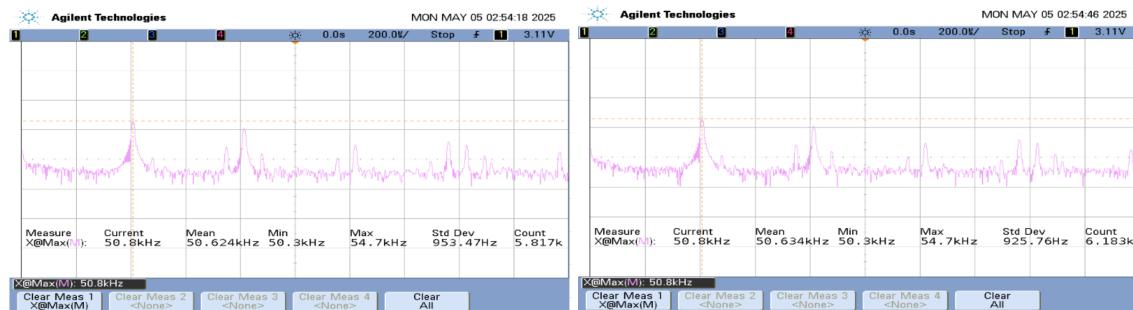


Figure 18: Oscillator A output (frequency-domain). Left: no metal. Right: with metal.

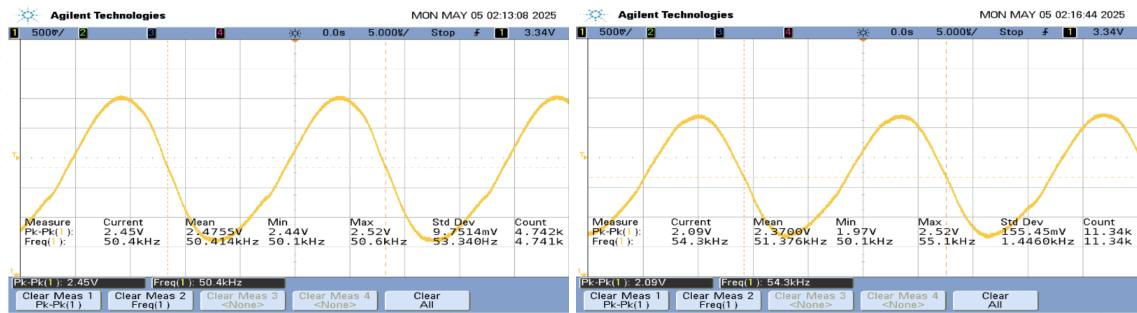


Figure 19: Oscillator B output (time-domain). Left: no metal. Right: with metal.

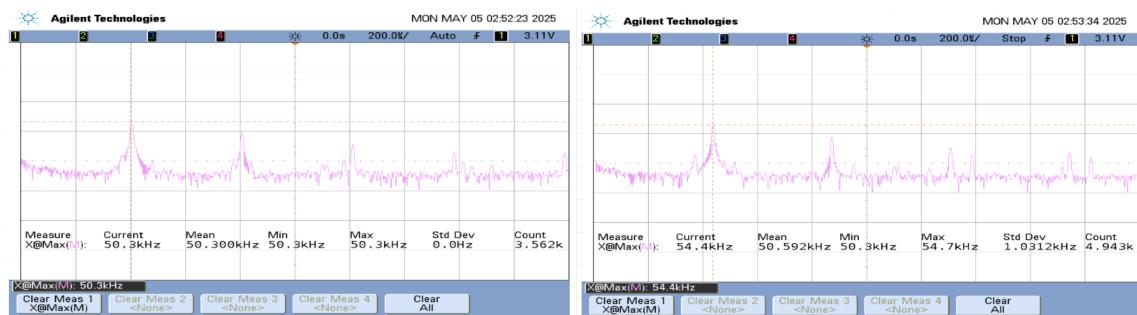


Figure 20: Oscillator B output (frequency-domain). Left: no metal. Right: with metal.

Mixer Differential Pair Output

At the differential pair output, the interference of the oscillator signals produces an amplitude-modulated waveform.

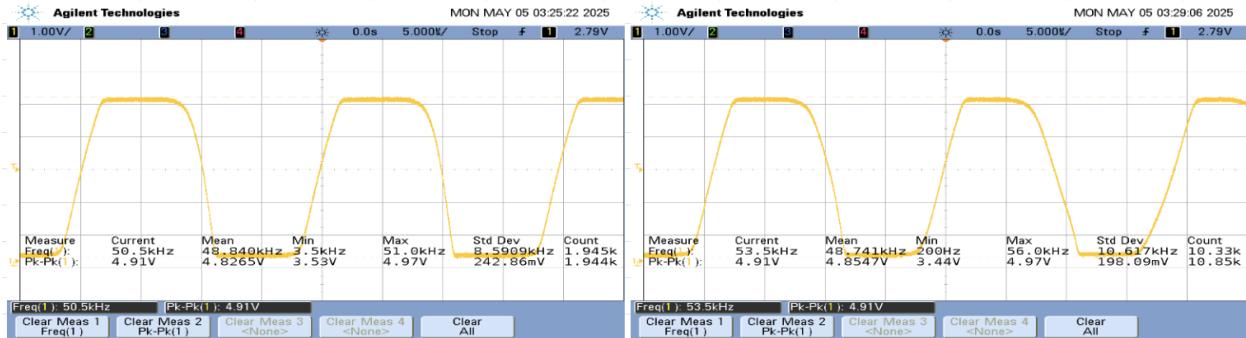


Figure 21: Mixer differential pair output (time domain). Left: no metal. Right: metal present.

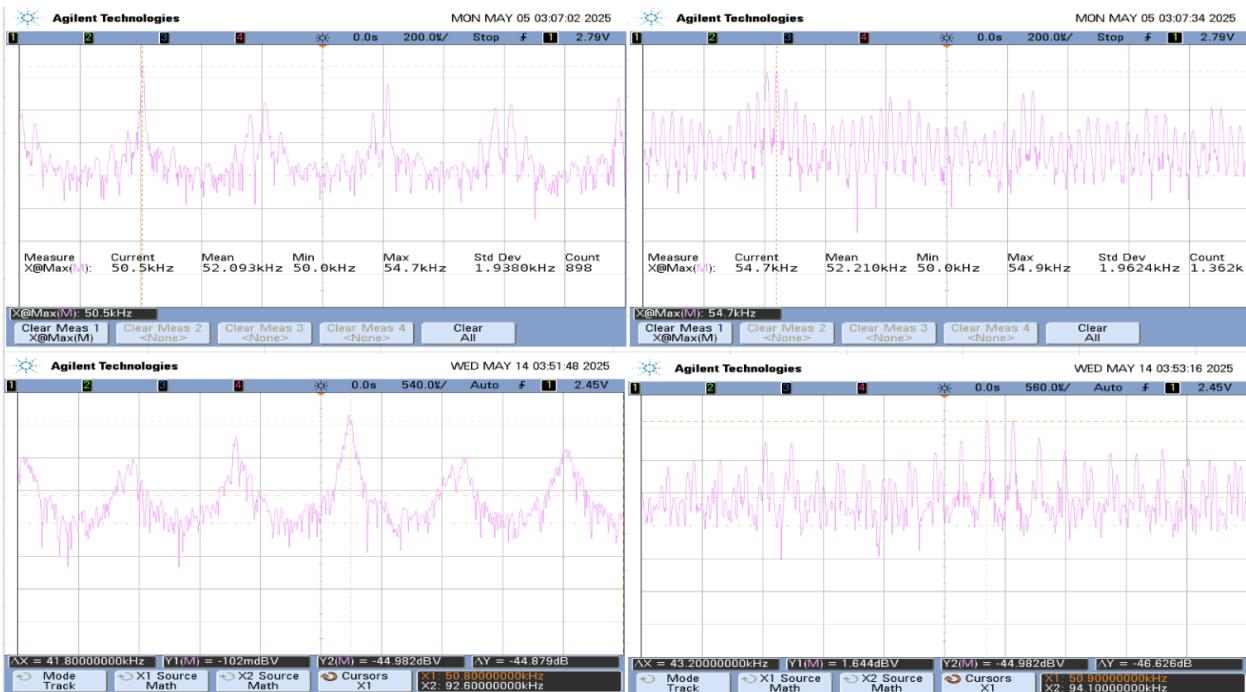


Figure 22: Mixer differential pair output (frequency domain). Left: no metal. Right: metal present. Top: higher frequency component. Bottom: lower frequency component.

Mixer CS Amplifier Output (Pre-Filter)

The first CS amplifier boosts the mixed signal prior to filtering. With metal present, the output shows a stronger frequency due to the increased inductance of the variable inductor.

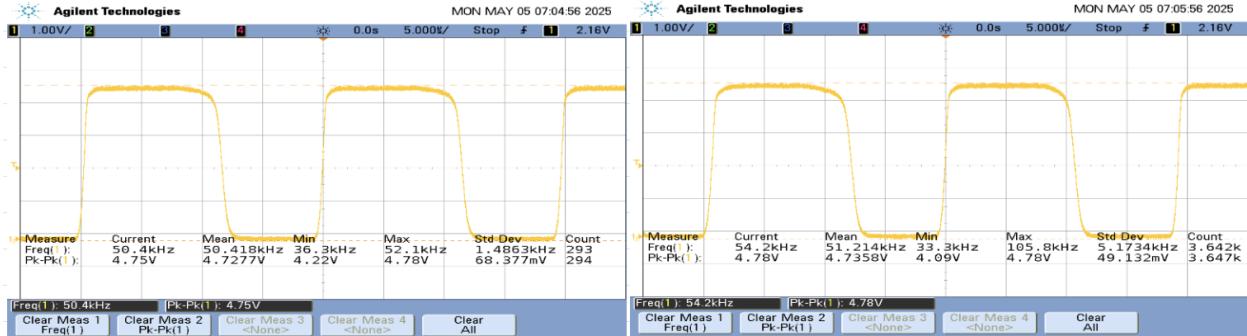


Figure 23: Mixer CS amplifier output (time domain). Left: no metal. Right: metal present.

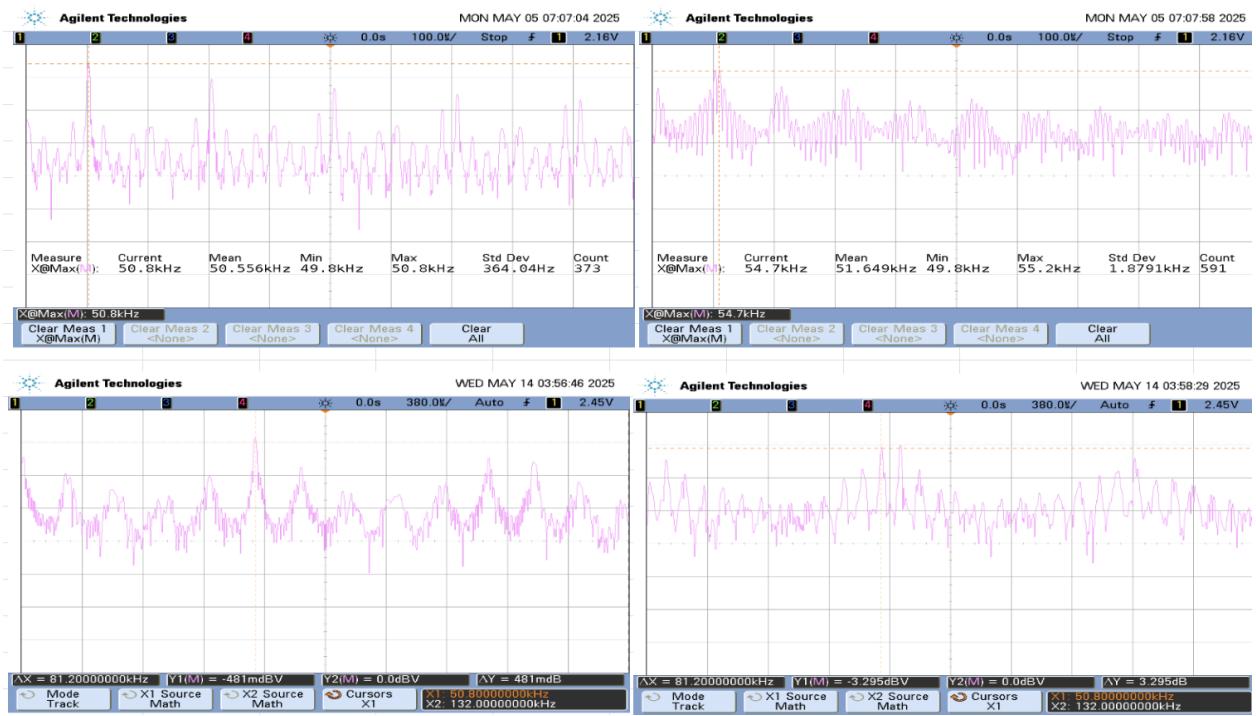


Figure 24: Mixer CS amplifier output (frequency domain). Left: no metal. Right: metal present. Top: higher frequency component. Bottom: lower frequency component.

RC Low-Pass Filter Output

The RC filter suppresses the high-frequency carrier and isolates the audible beat component. The presence of metal shifts the frequency of this component upward.

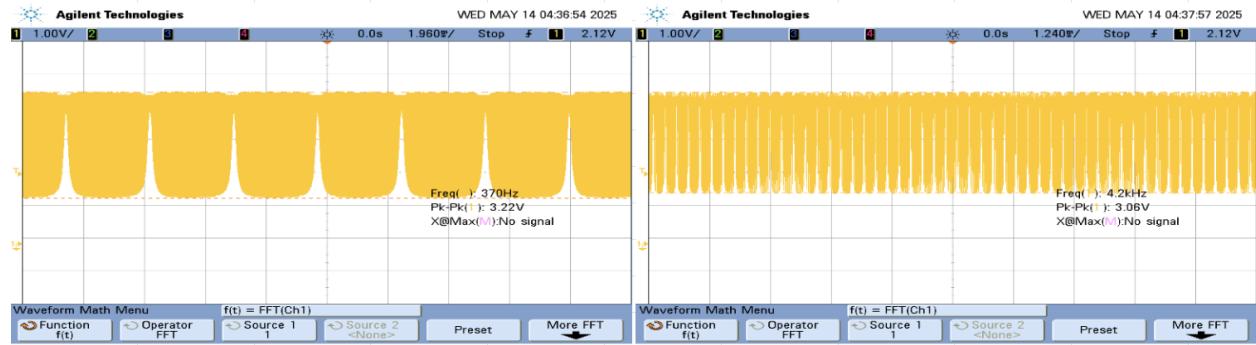


Figure 25: RC low-pass filter output (time domain). Left: no metal. Right: metal present.

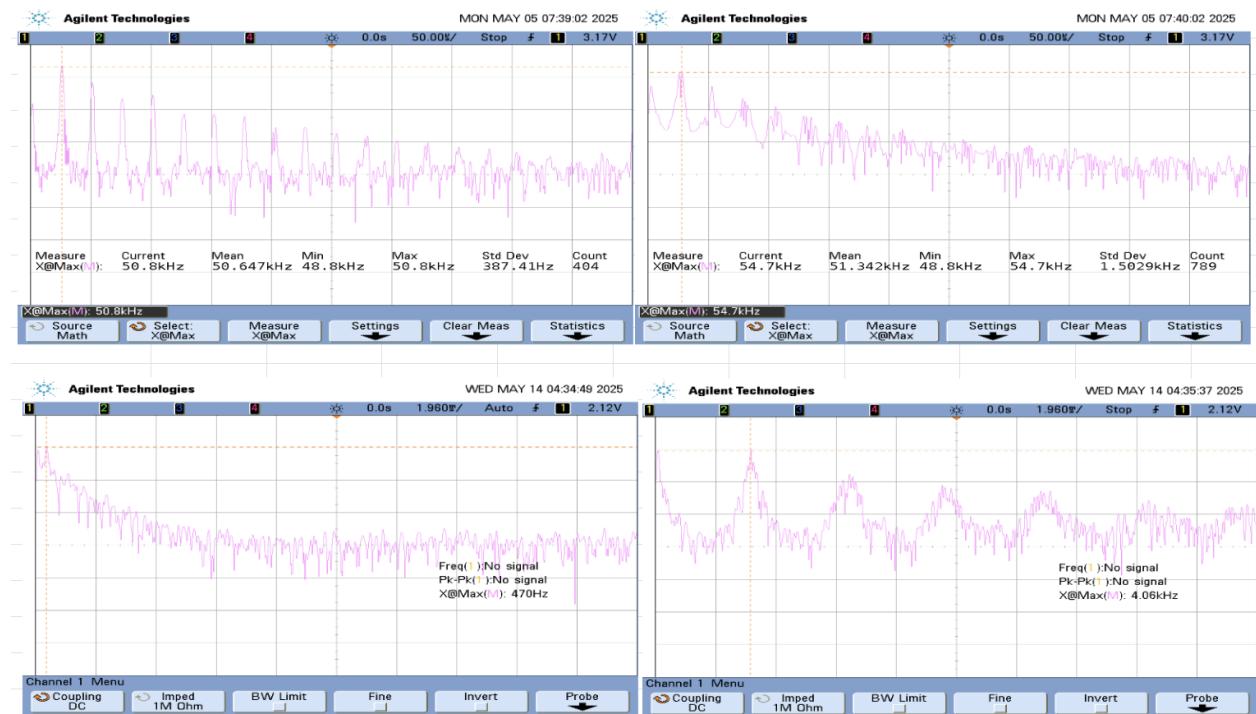


Figure 26: RC low-pass filter output (frequency domain). Left: no metal. Right: metal present. Top: higher frequency component. Bottom: lower frequency component.

Post-Filter and Second CS Amplifier Output

After filtering, the second CS amplifier boosts the low-frequency envelope. The effect of metal on the beat frequency is even clearer at this point.

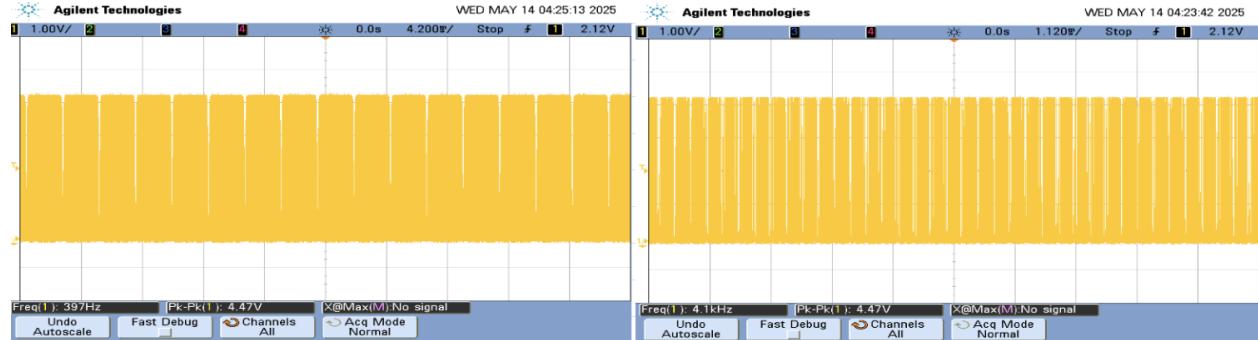


Figure 27: Mixer output past filter and second CS amp (time domain). Left: no metal. Right: metal present.

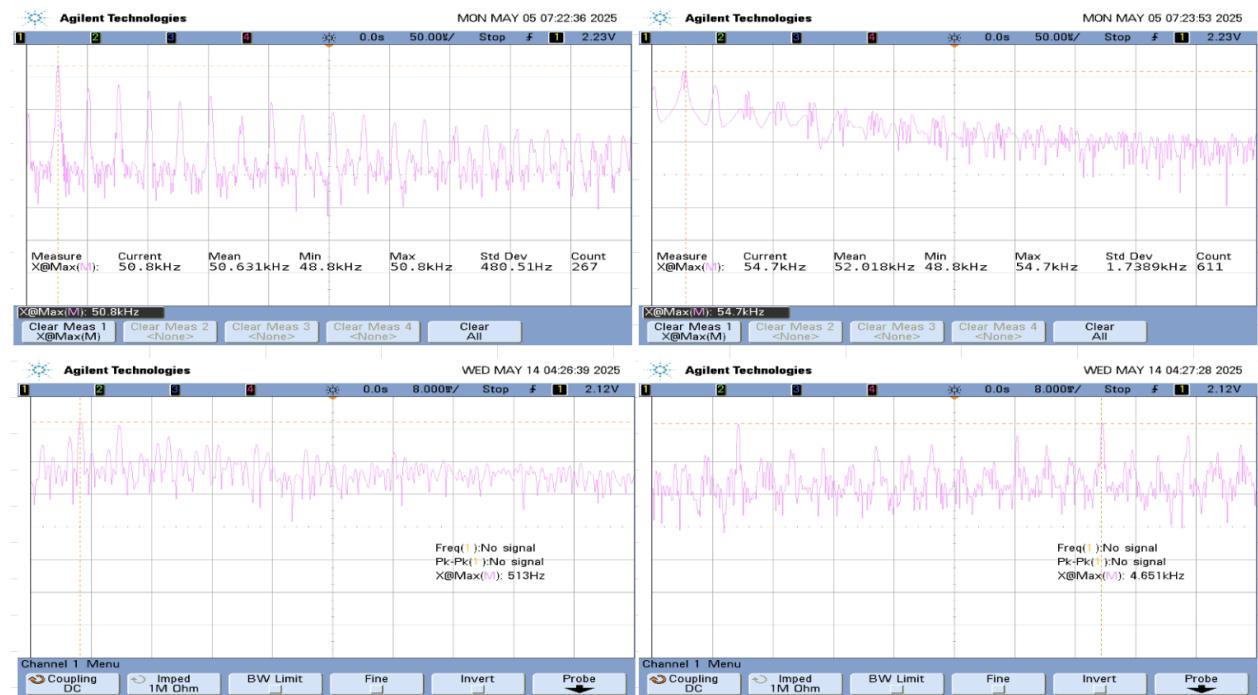


Figure 28: Mixer output past filter and second CS amp (frequency domain). Left: no metal. Right: metal present. Top: higher frequency component. Bottom: lower frequency component.

Final Output (Post-CD Buffer)

The final signal, buffered by a CD stage, is sent to the speaker. The signal remains clean and exhibits a clear audible frequency shift when metal is near.

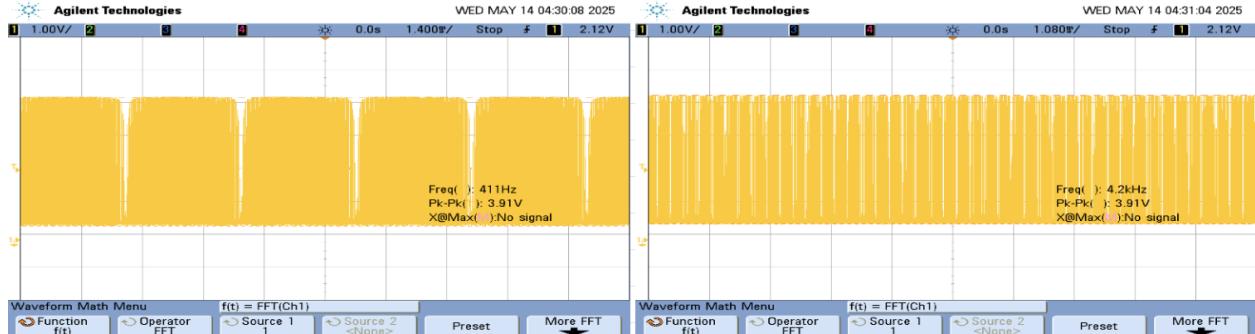


Figure 29: Final output after CD buffer (time domain). Left: no metal. Right: metal present.

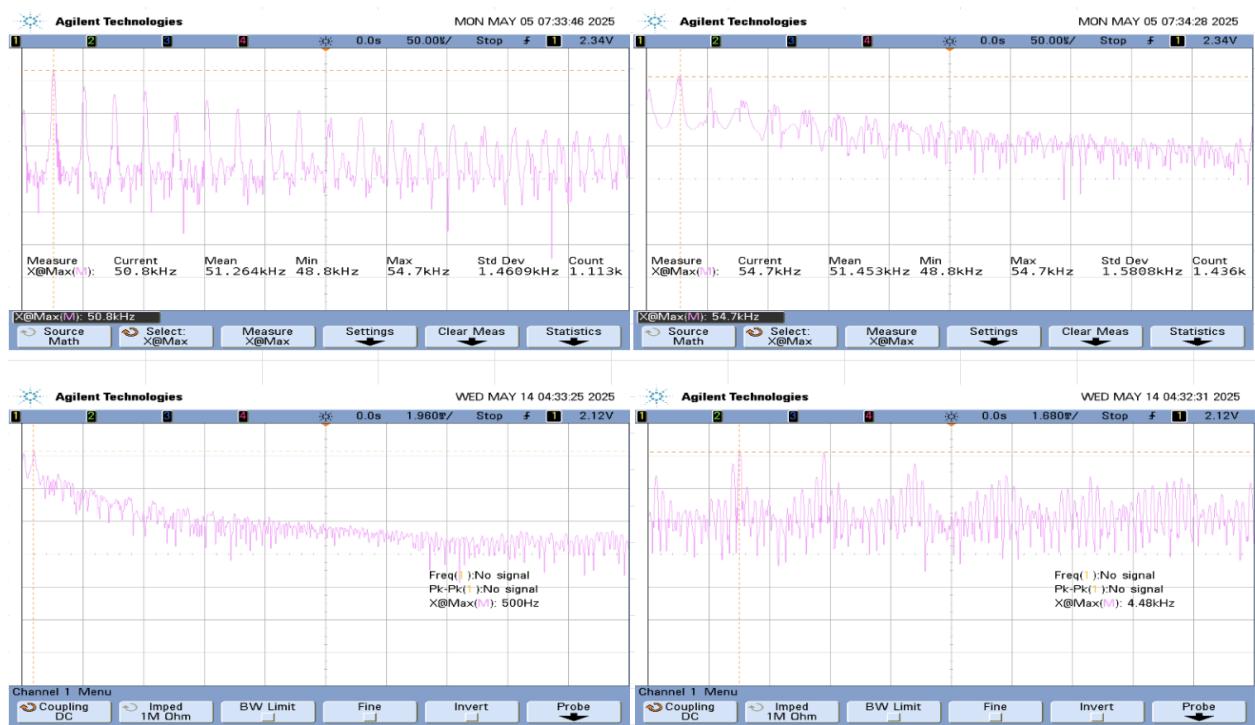


Figure 30: Final output after CD buffer (frequency domain). Left: no metal. Right: metal present. Top: higher frequency component. Bottom: lower frequency component.

These measurement results confirm that the system functions as expected. The oscillator frequencies remain close without metal, and diverge when metal is present, producing a measurable and audible beat frequency that increases in pitch with proximity to the target.

Discussion

The performance of the metal detector was assessed by comparing theoretical hand calculations, LTSpice simulations, and oscilloscope measurements collected during experimental operation. This multi-pronged approach revealed strong alignment between expected and observed behavior, with minor deviations that highlight both the accuracy and limitations of each method.

In the hand calculations, the frequencies of Oscillator A and Oscillator B were estimated using the resonance equation

$$f = \frac{1}{2\pi\sqrt{LC}}$$

using known inductance and capacitance values. With a 10 mH fixed inductor and 1120 pF capacitance for Oscillator A, and a 9.6 mH variable inductor and 780 pF capacitance for Oscillator B, the predicted frequencies were approximately 47.6 kHz and 48.5 kHz, respectively. These estimates indicated a nominal frequency difference of 900 Hz, suggesting a small beat frequency when no metal was present near the variable inductor.

LTSpice simulations reinforced these expectations, producing stable oscillator outputs near 49 kHz and 50 kHz when using equivalent component values. The simulated mixer output showed a beat signal near 985 Hz under standard conditions and approximately 2150 Hz when the inductance was increased by 5%, mimicking the presence of nearby metal. These values validated the theoretical model and confirmed correct implementation of the oscillator, mixer, and amplifier stages.

In physical measurements, the system produced an audible output at a frequency of roughly 977 Hz in the absence of metal, which rose to about 4 kHz when a metallic object was brought near the coil. These real-world values differ from the hand calculations primarily due to component tolerances and parasitic effects. Specifically, the actual capacitance of the tank capacitors may be lower than nominal (due to $\pm 10\%$ tolerance in ceramic capacitors), and layout parasitics could reduce total node capacitance. As a result, the measured oscillator frequencies were slightly higher than predicted, and the beat frequency shift with metal was larger.

Nevertheless, the circuit successfully demonstrated the intended functionality: the frequency of the final output tone increased clearly and consistently as metal was brought near the sensing coil, making the detector perceptually and functionally robust. The 4 kHz shift in output tone due to nearby metal falls well within the range of human hearing and produces a perceptible and intuitive signal for users.

Ultimately, the close correspondence between simulation, calculation, and measurement supports the accuracy of the design. The final result is a functioning metal detector that reliably amplifies and outputs the beat frequency generated by oscillator mismatch, with saturation-region biasing, properly tuned gain stages, and effective use of analog processing blocks throughout.

Conclusion

This project offered a comprehensive opportunity to bridge the gap between theoretical circuit design and hands-on hardware implementation. The task of building a fully functional LC oscillator-based metal detector from discrete MOSFETs and passives challenged both my analytical reasoning and my practical debugging skills. Each block—oscillator, mixer, filters, and amplifiers—required careful consideration of biasing, saturation conditions, and signal integrity.

The most difficult part of the project came after assembling the PCB. Despite extensive hand calculations and simulations confirming proper biasing and functionality, the actual hardware did not behave as expected on first power-up. Several stages, particularly the output amplifier and filter, required probing with an oscilloscope and iterative tuning of potentiometers to recover expected behavior. One particularly interesting realization was that the RC filter stage performed better without the capacitor, possibly due to phase interactions and bandwidth limitations introduced by downstream stages. This highlighted the often unpredictable impact of loading and parasitics in real-world implementations, and demonstrated the importance of empirical validation alongside simulation.

I also learned how crucial proper transistor biasing is for analog functionality. Using the ALD1103's datasheet, I identified 2V as a reliable target for $|V_{GS}|$, and constructed resistor networks to generate appropriate gate voltages from the 5V supply. The current mirror and differential pair stages served as a valuable opportunity to apply concepts from analog IC design, such as tail current estimation and voltage headroom constraints, within a discrete component context.

In terms of improvement, one major area would be introducing more systematic testing capabilities. For instance, adding jumper-enabled test nodes and probe pads across the PCB would have dramatically improved the ability to isolate and diagnose issues. Additionally, using higher-quality trim pots or replacing them with digitally programmable resistors could allow for easier tuning and characterization across different setups. Simulating the layout with parasitic-aware tools like LTspice with estimated trace capacitances could also help bridge the gap between schematic and physical board behavior.

Lastly, to improve sound output and robustness in noisy environments, I would add an active audio amplifier at the end stage and possibly regulate the gain dynamically based on detected signal strength. This would make the device more responsive and usable in real-world applications.

Overall, the project was not just an exercise in analog design but also in patience, persistence, and systems-level thinking. I am proud of the working final product and the design decisions made along the way, and I leave this experience with a much deeper respect for the nuances of analog circuit implementation.

References

- [1] Advanced Linear Devices, Inc., *ALD1103 Dual N-Channel and Dual P-Channel Matched MOSFET Pair*, datasheet, 2023. [Online]. Available:
<https://www.aldinc.com/pdf/ALD1103.pdf>