ESE 5720 Final Project

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Contents

1 Introduction and Literature Search

1.1 Motivation and Problem Statement

High-speed optical links rely on a front-end that can convert very small, broadband photodiode currents into voltage signals large enough to drive subsequent baseband circuitry while preserving signal integrity. The key element in this front end is the transimpedance amplifier (TIA), which converts the photodiode current into a voltage with prescribed gain, bandwidth, and noise performance [1].

In this project, the objective is to design a wideband CMOS TIA in a 45 nm process operating from a 1 V supply. The TIA interfaces to a photodiode modeled (in small-signal) as a current source in parallel with parasitic capacitance $C_P \approx 100\,\text{fF}$, and it must drive a $600\,\Omega$ differential resistive load ($300\,\Omega$ from each output to ground). The required differential transimpedance gain is at least $150\,\text{k}\Omega$, with a minimum differential output swing of $0.4\,\text{V}_{\text{pp}}$, an upper –3 dB bandwidth exceeding 300 MHz, and integrated input-referred current noise below $125\,\text{nA}_{\text{rms}}$, all under a total power budget below 10 mW [1].

The parallel combination of the photodiode capacitance and the TIA's input impedance sets a dominant pole at the front end. A high transimpedance implemented purely with a large resistor at the photodiode node would therefore severely limit bandwidth and increase thermal noise. Modern CMOS TIAs are designed to circumvent this gain–bandwidth–noise tradeoff through appropriate circuit topologies, feedback techniques, and device-level optimizations.

1.2 Overview of TIA Topologies

Transimpedance amplifiers (TIAs) are a critical front-end element in high-speed optical receivers. Their role is to convert the photocurrent generated by a photodiode into a voltage signal while preserving the bandwidth and minimizing the noise added in the process. TIA topologies must meet strict trade-offs between transimpedance gain, bandwidth, input impedance, noise performance, and power consumption, especially under low-voltage operation in advanced CMOS technologies. Architectures typically fall into one of the following categories: resistive feedback amplifiers, common-gate (CG) or regulated cascode (RGC) input stages, inverter-based topologies with active feedback, and distributed or inductively-peaked multistage designs.

Resistive Termination and Shunt-Feedback TIAs The most straightforward transimpedance amplifier topology is to terminate the photodiode with a passive resistor R and sense the resulting voltage swing. The gain is given by Ohm's Law, but this approach creates a bandwidth-limiting pole at $f_{-3\text{dB}} = 1/(2\pi R(C_P + C_{\text{in}}))$, where C_P is the parasitic capacitance of the photodiode and C_{in} is the input capacitance of the sensing amplifier [2]. As R increases to improve gain, bandwidth rapidly decreases and thermal noise ($\sqrt{4kTR}$) increases, making this method unsuitable for high-speed designs.

To improve upon this, a high-gain amplifier with a feedback resistor R_F can be used to implement a shunt-feedback TIA. This configuration virtually grounds the photodiode node, significantly reducing the input impedance and pushing the input pole outward. The closed-loop transimpedance is roughly equal to R_F, and the bandwidth is improved due to the negative feedback reducing the effect of C_P. However, real amplifiers have finite gain-bandwidth products and introduce their own noise and input capacitance, which limit overall performance. Amplifier noise becomes significant at low supply voltages, and loop stability must be verified across frequency and process corners [2].

Despite these challenges, several successful implementations have demonstrated high-speed performance. For instance, a 40 Gb/s shunt-feedback TIA in 0.18 μm CMOS achieved a 30.5 GHz

bandwidth and 51 dBΩ gain by using cascaded common-source stages with π-type inductor peaking [3]. This type of compensation helps extend bandwidth while maintaining flat gain across frequency.

Common-Gate and Regulated-Cascode Input Stages The common-gate (CG) configuration offers a different method of achieving low input impedance, where the source of a MOSFET receives the photodiode current and the gate is AC grounded. The input impedance is approximately $1/g_m$, and this directly lowers the RC time constant formed with C_P, pushing the input pole to higher frequency. This enables large bandwidths with relatively modest power consumption. However, CG TIAs suffer from high input-referred current noise since the full drain current noise of the transistor is transferred to the input [4].

To mitigate these issues, regulated cascode (RGC) architectures insert a gain stage in a local feedback loop between the drain and gate of the input transistor. This increases the effective transconductance and decreases input impedance further. The RGC architecture has shown strong bandwidth extension and noise suppression capabilities. For example, an RGC TIA in 65 nm CMOS achieved a bandwidth of 11.4 GHz and a gain of 46 dBΩ with just 23.9 mW power dissipation, outperforming traditional shunt-feedback designs in both speed and energy per bit [5]. The RGC structure is particularly attractive in low-voltage CMOS processes because it avoids stacking many transistors while maintaining performance.

Active Feedback and Inverter-Based TIAs In deep-submicron CMOS, supply voltages below 1 V impose strict limitations on analog circuit headroom. Inverter-based TIAs have emerged as a promising alternative due to their simplicity and high transconductance when biased in the linear region. These designs typically include active (sometimes positive) feedback to lower input impedance and extend bandwidth [6].

However, active feedback loops introduce the risk of instability, especially when implemented with high-gain stages. Special care must be taken to control the gain-bandwidth product and ensure proper phase margin. For instance, loop compensation techniques or digitally tunable feedback paths may be used to guarantee stable operation across temperature and process variations [**?**].

A representative implementation includes a 180 nm CMOS inverter TIA that handles 1 mA peak-to-peak input current by dynamically activating the feedback path only under high signal conditions. This configuration allows for automatic range extension without a dedicated limiting amplifier [**?**]. Another advanced design in 45 nm CMOS targets LiDAR systems and uses dual current-mode feedback paths. It offers a tunable gain-bandwidth profile: 91 dBΩ gain at 114 MHz or 82 dBΩ gain at 297 MHz, while consuming only 245 μW [7]. This balance of low power, high transimpedance, and wide bandwidth makes inverter-based TIAs ideal for short-range optical sensing and battery-powered links.

Distributed, Inductively Peaked, and System-Level Designs At extremely high data rates (40 Gb/s and beyond), the limitations of lumped-element TIAs motivate distributed amplifier architectures. These use a traveling-wave topology where gain stages are distributed along a terminated transmission line. Bandwidths exceeding 36 GHz have been demonstrated in hybrid integrated receivers using CMOS TIAs co-designed with photodiodes and SiGe front-ends [8].

Inductively peaked multistage amplifiers are a more compact alternative, where on-chip spiral inductors are used to extend bandwidth by introducing a conjugate zero that cancels the input pole. These techniques are critical for ensuring flat gain and low group delay in 100 Gb/s systems, and the TIA must be co-designed with equalizers and limiting amplifiers in mind. Packaging

and photodiode bonding techniques (e.g., flip-chip, microbumps) also affect input capacitance and high-frequency behavior [2].

Low-Noise Combined TIA/LA (CTLA) Structures For systems that must detect both weak and strong optical pulses (e.g., LiDAR), TIAs with large dynamic range are essential. Combined transimpedance and limiting amplifier (CTLA) designs achieve this by fusing linear conversion and output clamping into a single stage. One such design in 180 nm CMOS uses both a passive feedback resistor and active inverter feedback, along with an NMOS clamp to limit output swing [9]. It achieves 88.8 dBΩ transimpedance, 629 MHz bandwidth, and supports input currents up to 1 mA, making it well-suited for time-of-flight ranging and optical pulse detection.

1.3 Implications for this Design

The architectural review highlights several key principles for selecting a suitable TIA topology for implementation in a 45 nm, low-voltage CMOS process. First and foremost, the input stage plays a critical role in defining both the bandwidth and the noise performance of the entire receiver front-end. Architectures such as the common-gate (CG), regulated cascode (RGC), and inverter-based feedback TIAs are particularly effective in reducing the input impedance presented to the photodiode. This impedance reduction suppresses the bandwidth-limiting pole formed with the photodiode's parasitic capacitance C_P, thus enabling high-speed operation without sacrificing gain. However, these benefits come with increased sensitivity to device sizing and bias point, since the input transistor noise (especially in CG and inverter structures) becomes the dominant contributor to input-referred current noise. Consequently, careful noise optimization is required to avoid violating the integrated noise constraint.

Second, the 1 V supply constraint in 45 nm CMOS technology imposes a hard limit on voltage headroom, which restricts transistor stacking in analog signal paths. Multi-stage cascode amplifiers with global feedback loops are often incompatible with these supply constraints. Instead, architectures based on local feedback (as seen in RGC and active-feedback inverter designs) are favored for their simplicity, superior power efficiency, and layout compatibility in deep submicron nodes.

Third, the output interface presents its own challenges. The TIA must drive a differential 600 Ω load (300 Ω to ground per side), which represents a relatively low-impedance termination. This mandates that the output stages of the TIA provide both high current drive capability and linearity while maintaining signal swing within the supply limits. To achieve this, gain is often partitioned across multiple stages: the initial stage prioritizes low input impedance and noise performance, while downstream amplifiers are optimized for transimpedance gain and load drive.

Fourth, the inclusion of any feedback mechanism—whether passive (shunt resistor around an op-amp) or active (e.g., an inverter-based loop)—requires robust stability analysis. The interaction between photodiode capacitance, on-chip parasitics, and feedback loop phase margin must be carefully simulated across process-voltage-temperature (PVT) corners to ensure that the TIA does not oscillate or exhibit peaking that violates noise or gain flatness specifications.

Based on these considerations, this project adopts a hierarchical multistage TIA architecture. The first stage will be a low input impedance current amplifier, realized using a CG or RGC structure. This ensures minimal bandwidth degradation due to the photodiode capacitance. The subsequent stages will be responsible for providing the majority of the transimpedance gain and for buffering the output to drive the 300 Ω terminations. Where required, source-follower or resistively loaded differential amplifier stages will be introduced to balance bandwidth, gain, and output swing constraints.

The upcoming process characterization phase will provide the necessary device metrics—such as g_m, r_o, C_{gs}, C_{gd}, and unity-gain frequency f_T—under various width and bias current conditions. These parameters will be used in conjunction with small-signal models and noise analysis to derive sizing equations and initial biasing conditions. This foundation will support a structured design flow involving hand calculations, followed by Cadence simulations to validate AC gain, bandwidth, transient behavior, and input-referred noise against the project specifications.

2 Process Characterization

The design of any analog front-end begins with accurate process characterization of the target CMOS technology. For this project, we adopt the gpdk045 45 nm CMOS process with a nominal supply voltage of 1 V. The primary objective of this phase is to empirically extract the DC, small-signal, and high-frequency parameters of NMOS and PMOS devices across a range of channel widths. The simulation tool used is Cadence Virtuoso with Spectre.

2.1 Simulation Procedure

For both NMOS and PMOS devices, the following simulations are performed:

1. I_D **vs.** V_{DS} **Characteristics:** Sweep V_{DS} from 0 to 1 V (10 uniform points) for a fixed V_{GS} in saturation. Device length is fixed at $L = 45\,\text{nm}$, and widths of $W = \{0.5\,\mu\text{m}, 1\,\mu\text{m}, 2\,\mu\text{m}, 4\,\mu\text{m}, 8\,\mu\text{m}\}$ are used to observe output resistance and saturation behavior.

2. V_{th} **vs.** I_D**:** Using DC sweeps of V_{GS}, extract threshold voltage as a function of drain current for the same widths. Threshold is determined using the constant-current method (e.g., $I_D = 100\,\text{nA} \cdot W/L$), providing insight into subthreshold and moderate inversion regimes.

3. g_m **vs.** I_D**:** Transconductance is extracted from small-signal AC simulations or derived from the slope of the I_D–V_{GS} curve. This plot is essential to determine g_m/I_D efficiency across inversion levels. Device sizing for optimal power efficiency will reference this plot.

4. $C_{\mathbf{gs}}$ **and** $C_{\mathbf{gd}}$ **vs.** W**:** Gate capacitances are extracted at 1 V bias and plotted versus width from $0.4\,\mu\text{m}$ to $10\,\mu\text{m}$. This data informs input capacitance estimation and photodiode pole placement.

5. **Unity Gain Frequency (**f_T**):** Extracted from AC simulation using the relation $f_T = g_m/(2\pi(C_{\text{gs}} + C_{\text{gd}}))$. Sweeps are performed across multiple bias currents to observe how f_T varies with I_D. This metric determines the maximum achievable bandwidth and limits the topological complexity of high-speed amplifiers.

2.2 Data Usage and Validation

All curves will be presented for both NMOS and PMOS transistors, enabling design symmetry in differential stages. The extracted data is used to:

- Validate hand calculations of gain, input impedance, and bandwidth.
- Estimate noise and parasitic poles.
- Calibrate device models for schematic-level simulations.

Where discrepancies are observed between simulated data and textbook equations (e.g., square-law or EKV model predictions), these will be explained in the report to account for velocity saturation, channel length modulation, and short-channel effects.

The outcome of this process is a set of device curves and operating point tables that support all subsequent design stages, ensuring that transistor sizing aligns with bandwidth, gain, noise, and power specifications.

2.3 I_D vs V_{DS}

To begin the process characterization, the drain–current versus drain–source voltage characteristics of minimum-length MOSFETs were measured for a range of device widths. All NMOS transistors were implemented using the 45 nm process with channel length $L = 45\,\text{nm}$ and widths $W \in \{0.5\,\mu\text{m}, 1\,\mu\text{m}, 2\,\mu\text{m}, 4\,\mu\text{m}, 8\,\mu\text{m}\}$. For each device, the gate–source voltage was held at $V_{GS} = 1\,\text{V}$, and the drain–source voltage V_{DS} was swept from 0 to 1 V in uniform steps. The drain current I_D at the drain terminal was recorded as the primary output of the DC analysis. An identical procedure was used for PMOS devices, with the source and bulk tied to $V_{DD} = 1\,\text{V}$ and the gate held at ground, resulting in a constant $V_{SG} = 1\,\text{V}$. In both cases, sweeping the device width produces a corresponding family of I_D–V_{DS} curves.

The resulting characteristics reflect the expected long-channel trends discussed in the course notes, even though the 45 nm devices depart from ideal behavior. At low drain–source voltages ($V_{DS} < V_{GS} - V_{TH}$), the NMOS operates in the triode region and the drain current increases approximately linearly with V_{DS}, with slope proportional to W/L. As V_{DS} approaches the saturation boundary, $V_{DS,\text{sat}} \approx V_{GS} - |V_{TH}|$, the curves transition from a steep linear rise to a more gradual increase, consistent with the onset of velocity saturation and channel-length modulation. Using the operating-point data from the simulations, we extract threshold voltages of approximately $V_{TH,n} \approx 610\,\text{mV}$ for the NMOS devices and $|V_{TH,p}| \approx 530\,\text{mV}$ for the PMOS devices. These values place the expected saturation voltages near

$$V_{DS,\text{sat}} \approx V_{GS} - V_{TH,n} \approx 0.39\,\text{V} \quad \text{and} \quad V_{SD,\text{sat}} \approx V_{SG} - |V_{TH,p}| \approx 0.47\,\text{V}.$$

For V_{DS} beyond the saturation boundary, the drain current continues to rise slowly with V_{DS} due to channel-length modulation, again with magnitude scaling roughly in proportion to the device width. Across all widths, the measured characteristics exhibit the expected behavior: nearly zero current at low V_{DS}, a rapid increase through the triode region, and a flattened slope once the devices enter saturation. These observations confirm consistency with standard MOSFET operation and form the basis for the subsequent extraction of threshold voltage, transconductance, and g_m/I_D characteristics used later in the TIA design analysis.

2.3.1 NMOS Test Setup and Results

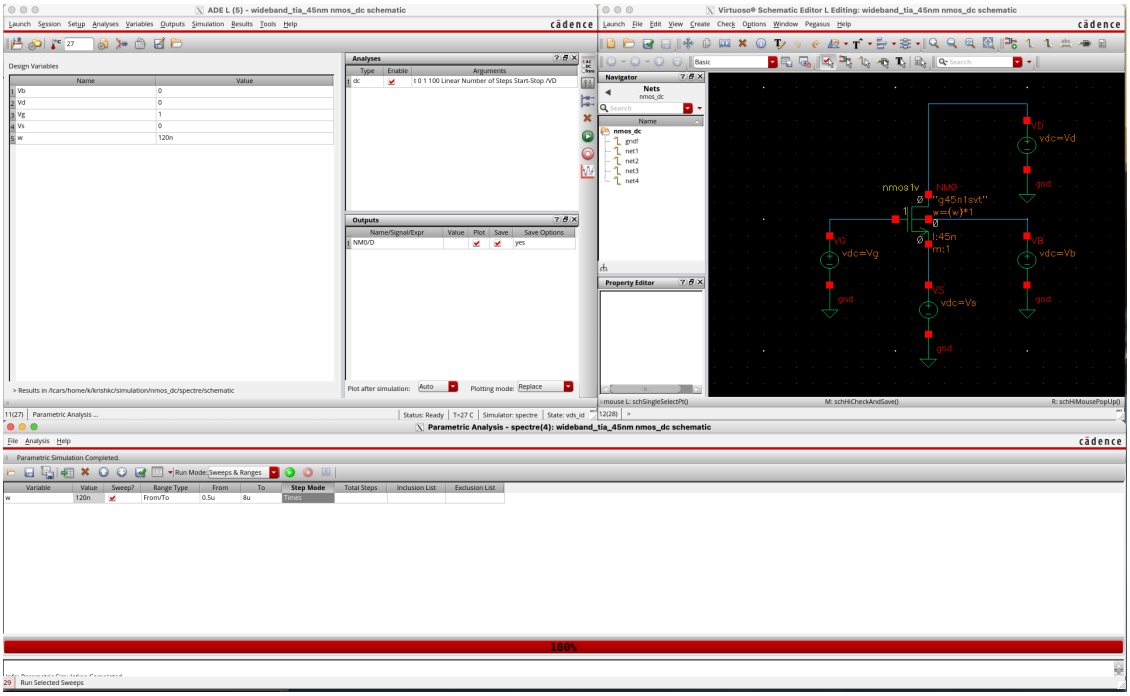

Figure 1: NMOS testbench setup

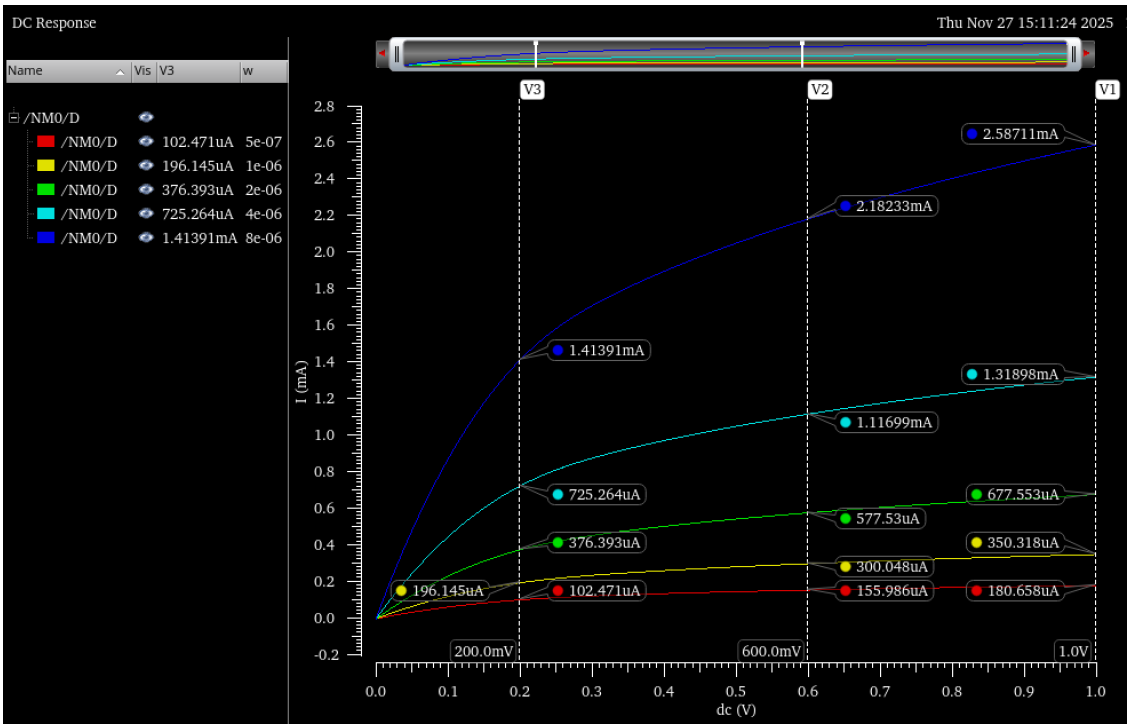

Figure 2: Results showing $I_{D,max}$ for each width

2.3.2 PMOS Test Setup and Results

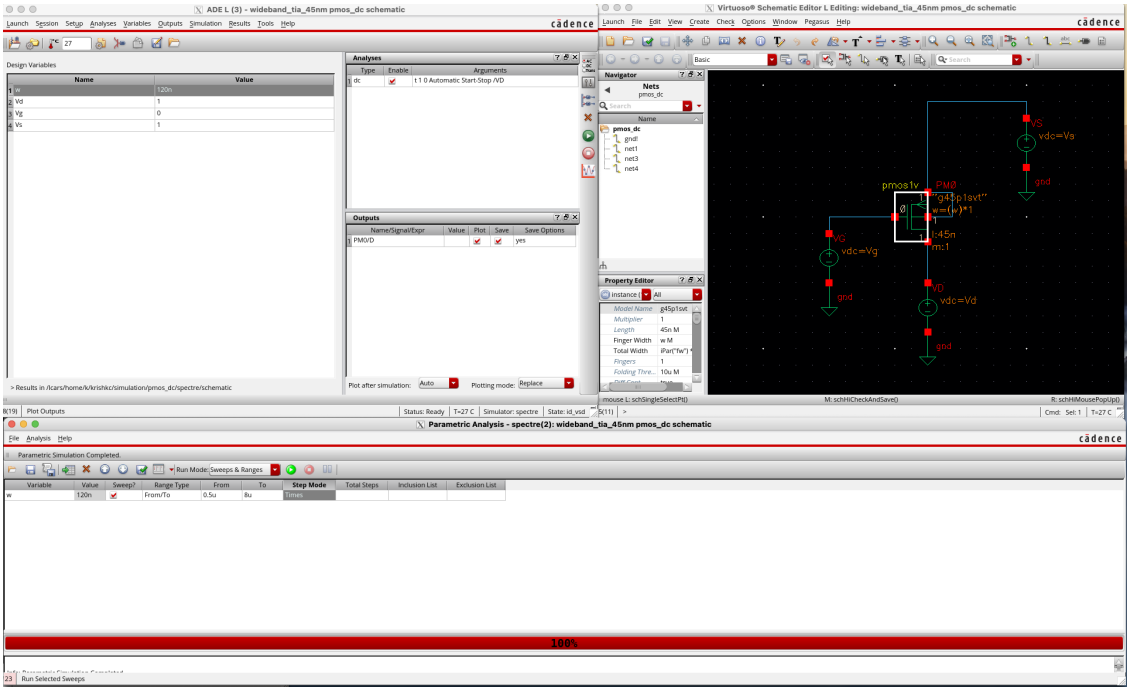

Figure 3: NMOS testbench setup

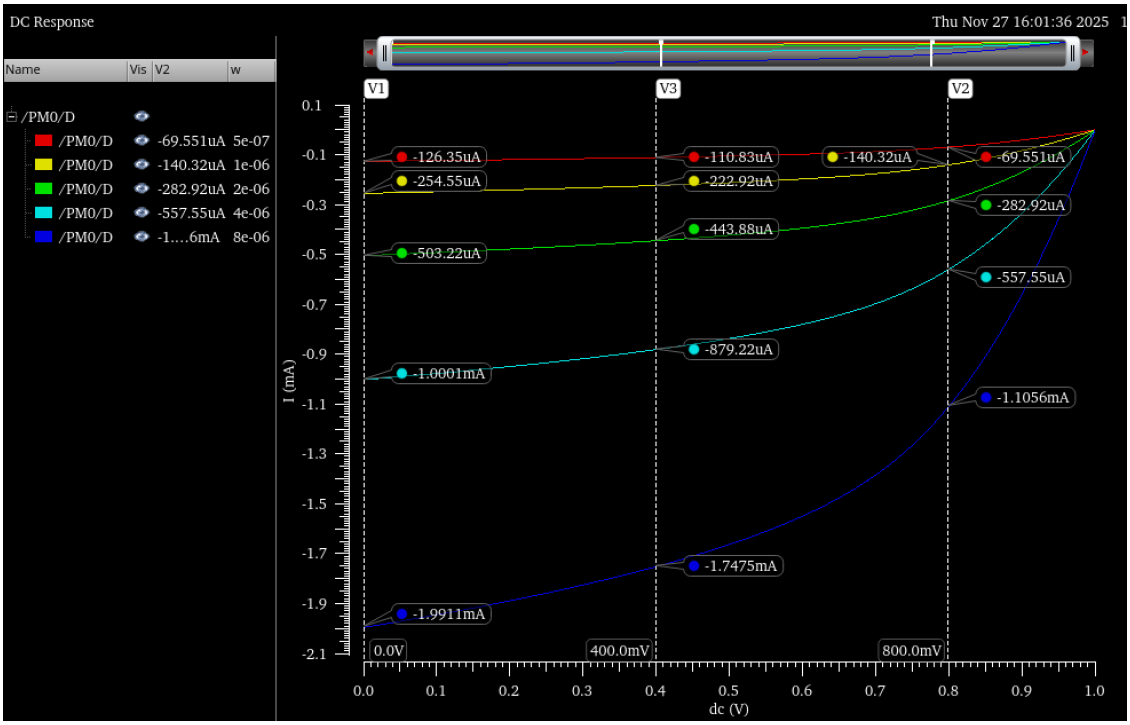

Figure 4: Results showing $I_{D,max}$ for each width

2.3.3 Summary Table

Width W (μm)	$I_{D,\max}$ **NMOS (mA)**	$I_{D,\max}$ **PMOS (mA)**
0.5	0.1807	−0.12635
1.0	0.3503	−0.25455
2.0	0.6775	−0.50322
4.0	1.319	−1.00010
8.0	2.587	−1.99110

Table 1: Summary of $I_{D,\max}$ for NMOS and PMOS at $V_{DS} = 1\,\mathrm{V}$ and $V_{GS} = V_{SG} = 1\,\mathrm{V}$

2.4 V_{TH} vs I_D

In the second characterization step, the threshold voltage of minimum-length devices was evaluated as a function of drain current for several widths. Unlike the diode-connected configuration sometimes used for V_{TH} extraction, the project specifications require that this characterization be performed under the same bias conditions as the I_D–V_{DS} measurements from Section 2.1. Accordingly, each NMOS transistor was biased with $V_{DS} = 1\,\mathrm{V}$, while the gate–source voltage was swept from 0 to 1 V in a DC analysis. This sweep drives the drain current from the subthreshold region up to the $I_{D,\max}$ values obtained previously (ranging from about 0.18 mA for $W = 0.5\,\mu$m up to 2.59 mA for $W = 8\,\mu$m). For each bias point, the transistor's built-in operating-point parameter `vth` was recorded, and the resulting threshold voltage was plotted against the corresponding drain current for each width.

An analogous procedure was used for the PMOS devices. With the source and bulk tied to $V_{DD} = 1\,\mathrm{V}$ and the gate held at ground, a sweep of the gate–source voltage magnitude V_{SG} from 0 to 1 V generates drain currents up to approximately 2 mA for the widest device. Again, the model's `vth` parameter was extracted at each operating point and plotted versus the magnitude of I_{SD}.

From the long-channel strong-inversion relations,

$$I_D \approx \frac{1}{2}\mu_n C_{\mathrm{ox}} \frac{W}{L}(V_{GS} - V_{TH})^2$$

with fixed $V_{DS} \geq V_{GS} - V_{TH}$, the gate overdrive $V_{GS} - V_{TH}$ is expected to vary as $\sqrt{I_D}$, while V_{TH} itself remains approximately constant. In short-channel technologies such as 45 nm, however, effects including drain-induced barrier lowering (DIBL), mobility degradation, and channel-length modulation introduce a weak dependence of V_{TH} on both drain current and device geometry.

The simulated V_{TH}–I_D characteristics for the NMOS devices exhibit the expected behavior. Across the full current range, the extracted threshold values cluster tightly around $V_{TH,n} \approx 610\,\mathrm{mV}$, with only a few millivolts of variation as I_D increases from the microampere range to several milliamperes. Dependence on device width is likewise minimal: wider devices show nearly the same threshold as narrower ones, aside from a small systematic shift at the highest currents due to short-channel effects. The PMOS devices show similar behavior, with extracted thresholds remaining close to $|V_{TH,p}| \approx 530\,\mathrm{mV}$ throughout the sweep and only mild broadening at large I_{SD}.

These results confirm that, over the bias region relevant to the subsequent TIA hand calculations, both NMOS and PMOS devices may be modeled as having nearly constant thresholds in the 0.5–0.65 V range. Second-order short-channel effects introduce only modest deviations, and the extracted V_{TH} values provide a consistent foundation for the later g_m, g_m/I_D, and device sizing analyses.

2.4.1 NMOS Test Setup and Results

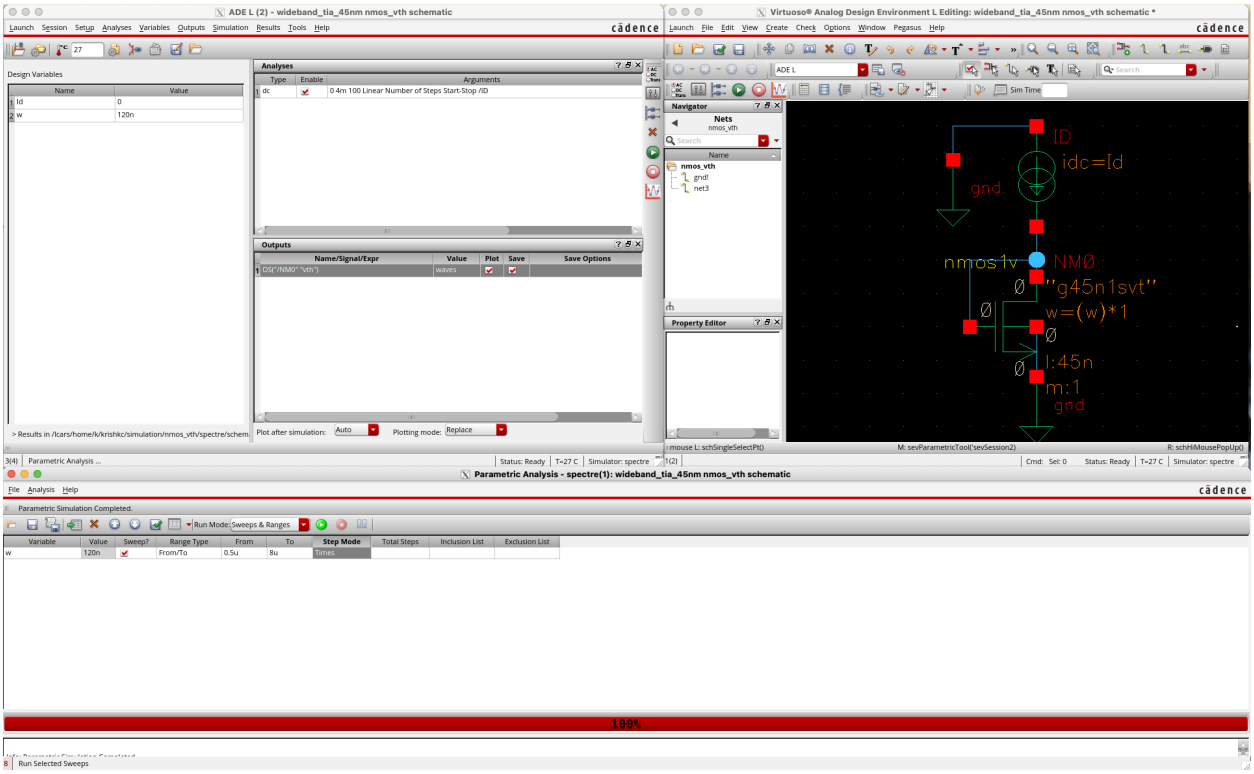

Figure 5

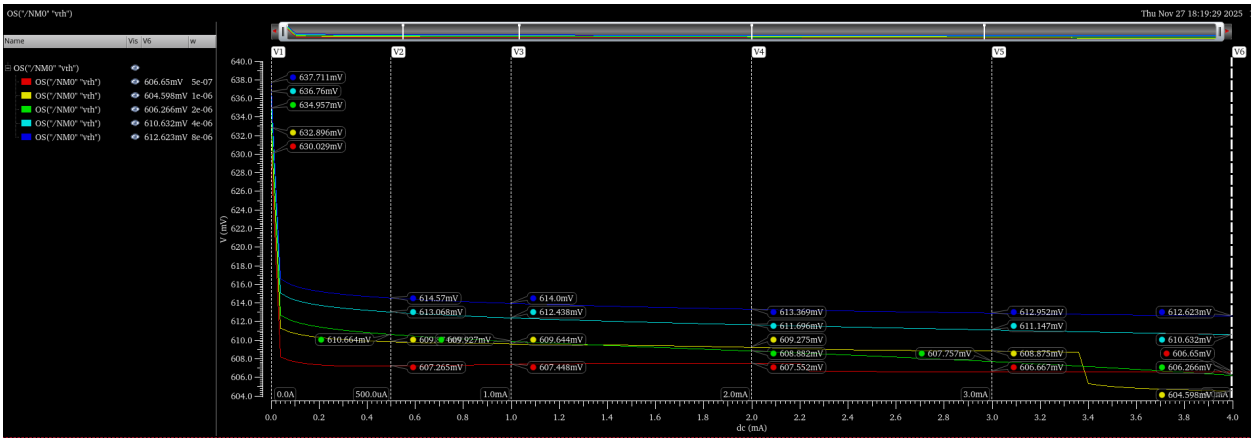

Figure 6

2.4.2 PMOS Test Setup and Results

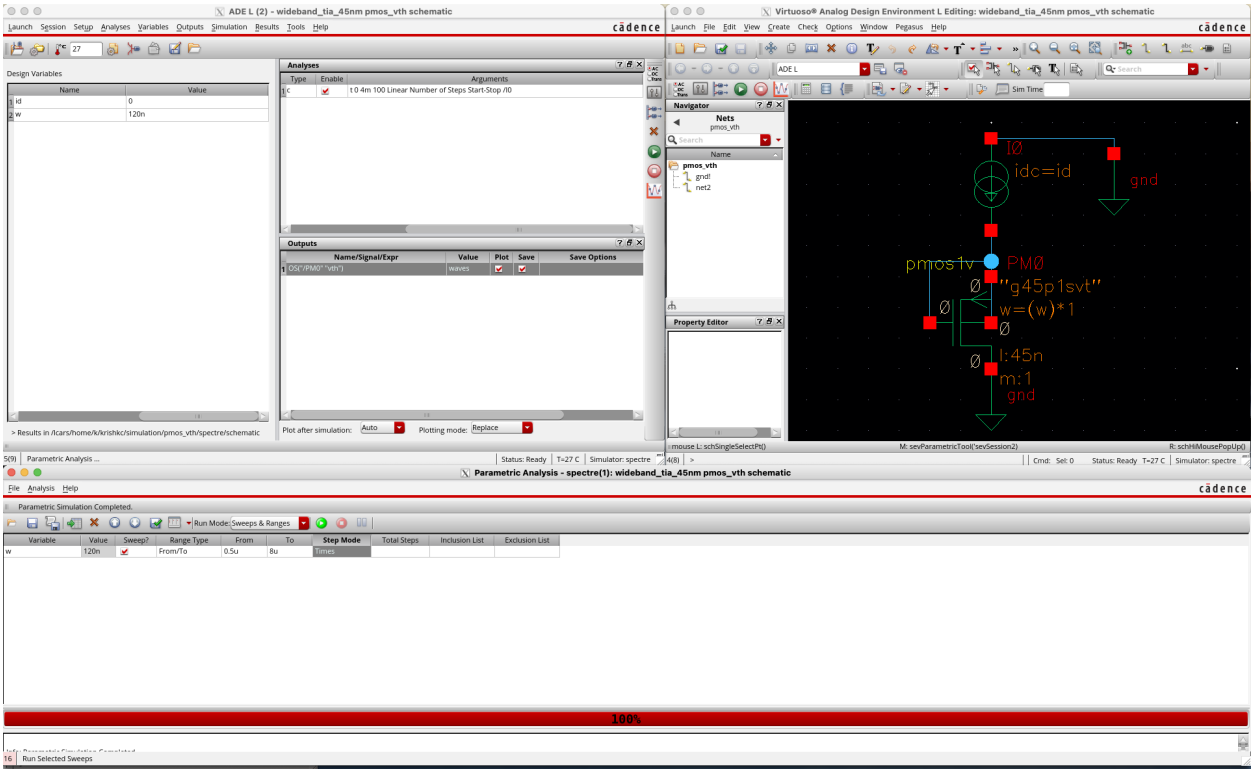

Figure 7

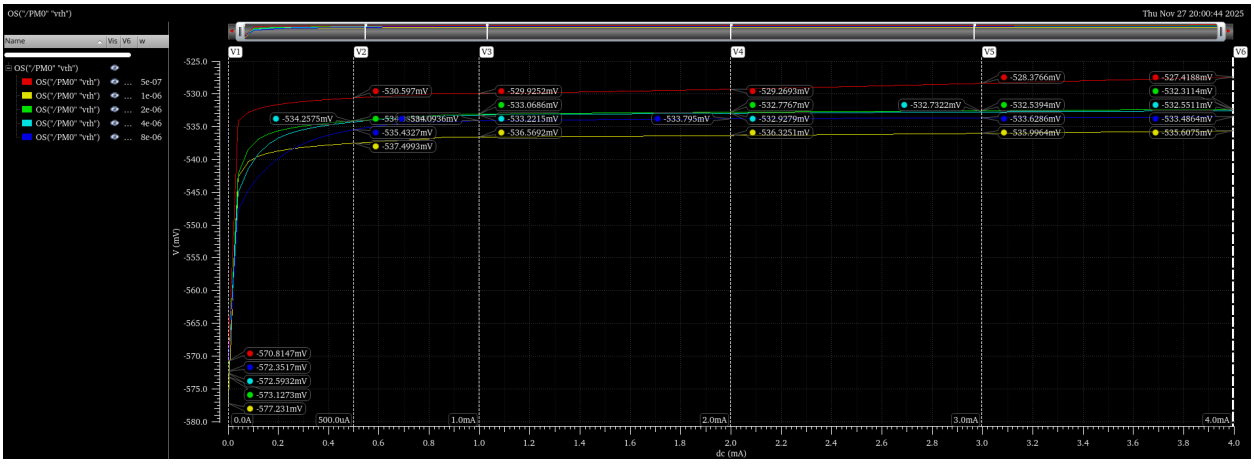

Figure 8

2.5 g_m vs I_D

In the third characterization step, the small–signal transconductance g_m of minimum–length MOSFETs was evaluated as a function of drain current. For this measurement, the same diode–connected testbench topology used in the previous section was employed. Each NMOS device with $L = 45\,\text{nm}$ and widths $W = \{0.5, 1, 2, 4, 8\}\,\mu\text{m}$ was connected with its gate and drain shorted, source and bulk tied to ground, and a DC current source applied from drain to supply. A DC analysis was run while sweeping the imposed drain current I_D from 0 up to a value slightly larger than the $I_{D,\max}$ found in the I_D–V_{DS} characterization (approximately 4 mA in 100 points). At each operating point, the simulator's operating–point parameter `gm` was saved, and the resulting g_m–I_D characteristics were plotted for all device widths.

An analogous setup was used for the PMOS devices. With the source and bulk tied to $V_{DD} = 1\,\text{V}$, each PMOS transistor was diode–connected by shorting its gate and drain, and a DC source current I_{SD} was swept from source to V_{DD}. The current range was chosen to extend slightly above the corresponding $I_{SD,\max}$ values from the PMOS I_{SD}–V_{SD} curves, resulting in a maximum magnitude of approximately 3 mA. The simulator again reported g_m at each bias point, enabling the g_m–I_{SD} characteristics to be compared across widths. From the long–channel strong–inversion model,

$$I_D \approx \frac{1}{2}\mu C_{\text{ox}}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}),$$

and with $V_{DS} = V_{GS}$ in a diode–connected configuration, differentiation with respect to V_{GS} yields

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \approx \mu C_{\text{ox}}\frac{W}{L}(V_{GS} - V_{TH}) \approx \frac{2I_D}{V_{GS} - V_{TH}}.$$

Eliminating the gate overdrive gives the familiar square–law scaling

$$g_m \approx \sqrt{\frac{2\mu C_{\text{ox}}}{L}}\,\sqrt{W I_D},$$

indicating that g_m should grow approximately as $\sqrt{I_D}$ for a given width, and increase proportionally to $\sqrt{W}$ at any fixed current.

The simulated curves in Figures 10 and 12 follow these expectations. For each device width, g_m rises monotonically with increasing drain current and shows a sublinear trend at higher currents, consistent with mobility degradation and velocity saturation in the 45 nm technology. Wider devices exhibit larger transconductance at a given current, and the vertical spacing between curves reflects the predicted $\sqrt{W}$ dependence. As I_D increases into the milliampere range, short–channel effects cause g_m to deviate slightly from the ideal $\sqrt{WI_D}$ behavior, leading to a gentle flattening of the curves.

These g_m–I_D characteristics provide valuable design insight. Because transconductance is a key parameter in determining gain and bandwidth of the TIA in later sections, the extracted curves allow rapid selection of the necessary bias current for each device width. The predictable scaling with $\sqrt{W}$ and the smooth increase of g_m with I_D form a reliable foundation for the device–level sizing and biasing decisions used in the subsequent design stages.

2.5.1 NMOS Test Setup and Results

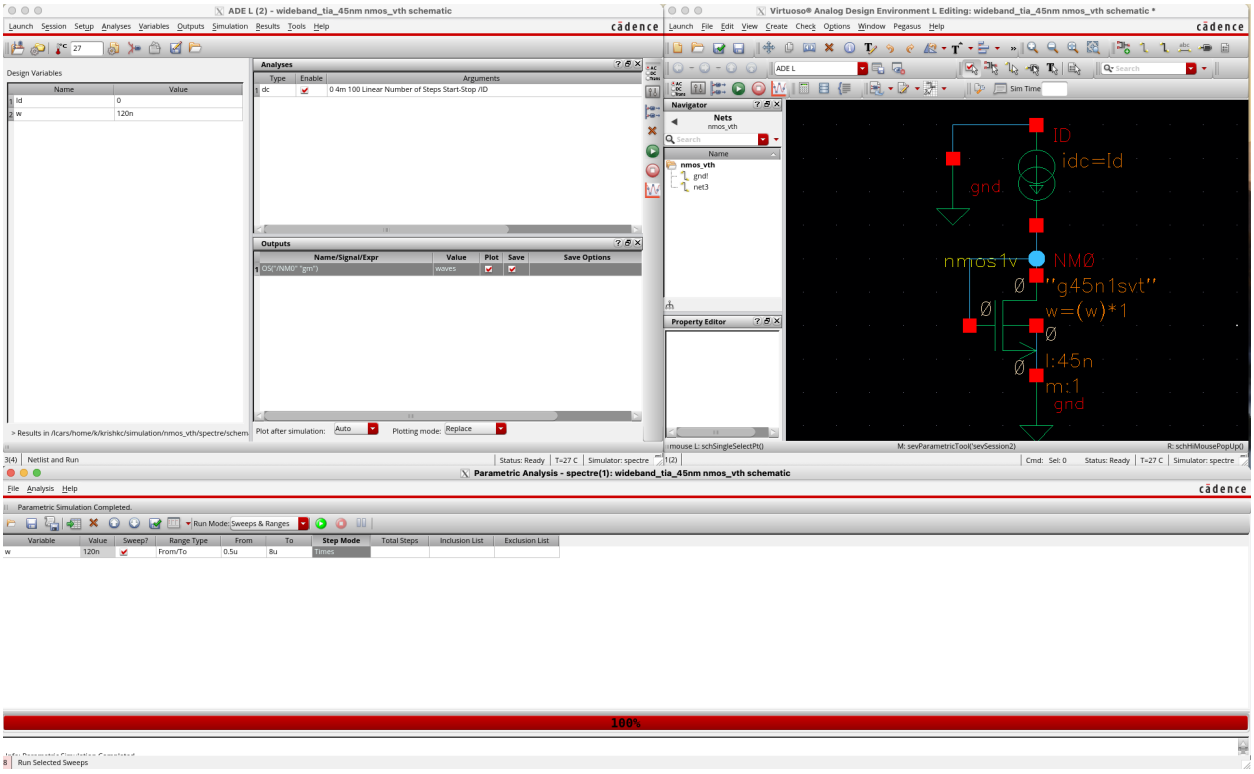

Figure 9

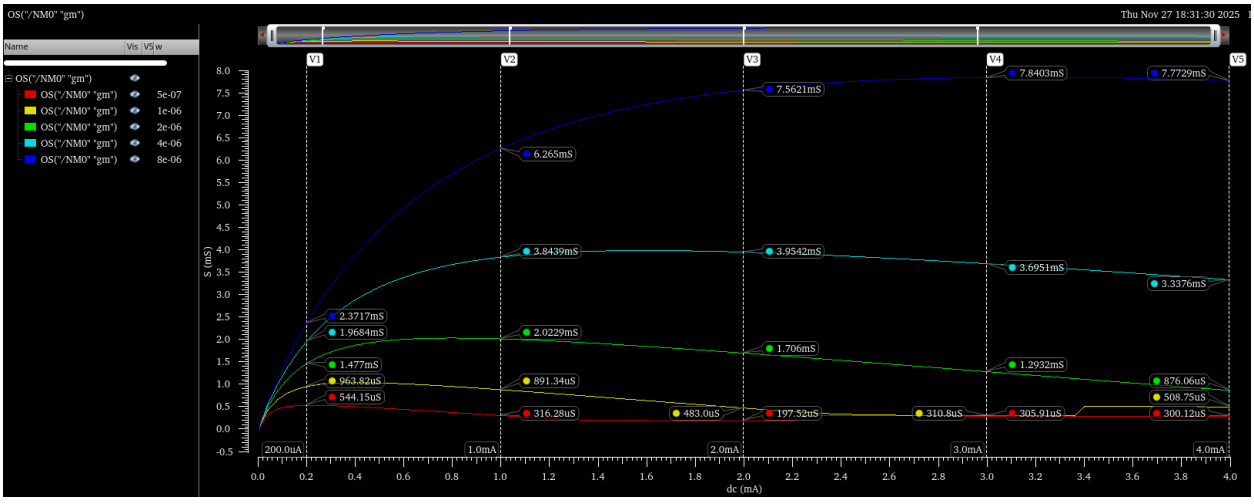

Figure 10

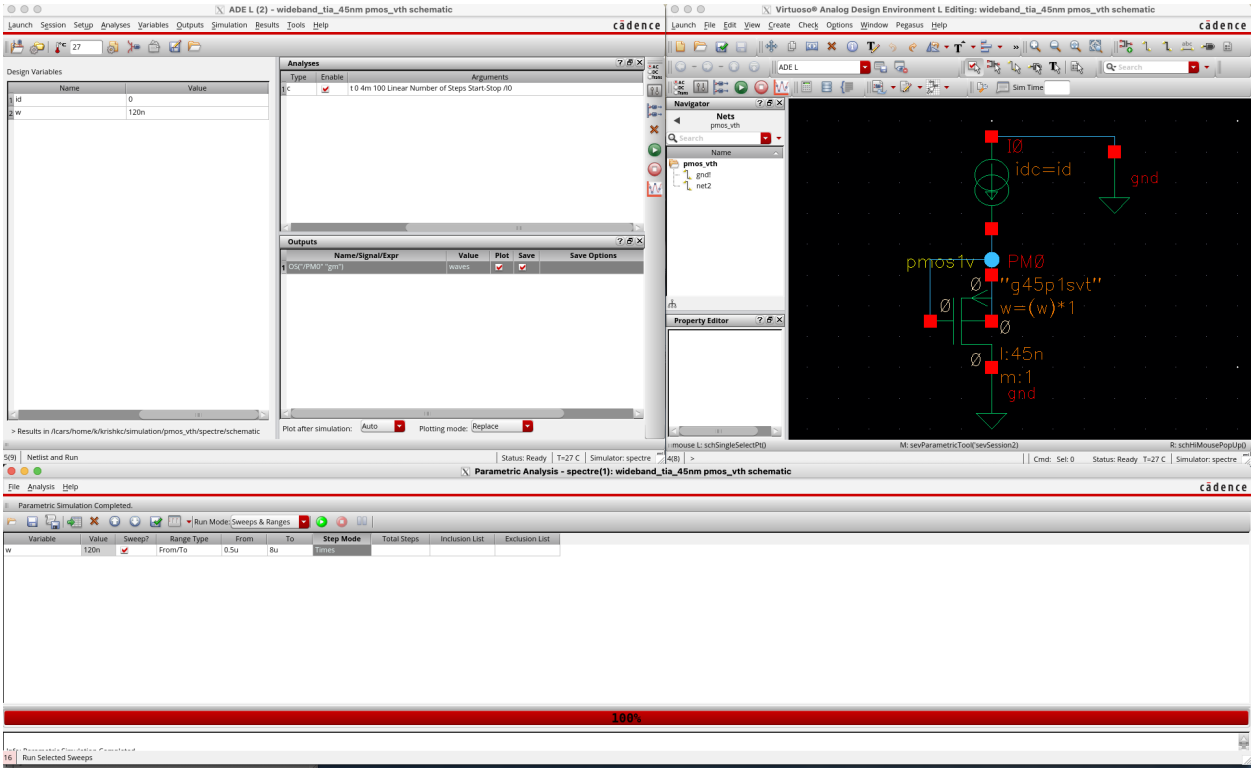

Figure 11

2.5.2 PMOS Test Setup and Results

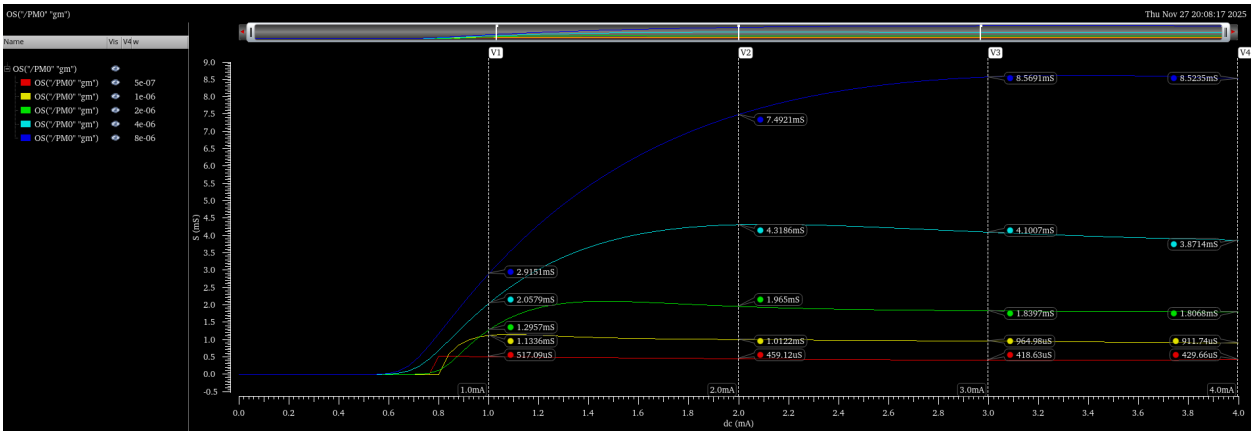

Figure 12

2.6 C_{gs} and C_{gd} vs I_D

The final device characterization step investigates how the intrinsic gate capacitances C_{gs} and C_{gd} scale with transistor width. For this measurement, each MOSFET was placed in a diode–connected configuration by shorting the gate and drain terminals, while the source and body were tied to ground. This bias forces the device into strong inversion for sufficiently large widths and establishes a well–defined small–signal operating point from which the intrinsic capacitances can be extracted. A DC operating–point analysis was run for each width, and the simulator's operating–point quantities `cgs` and `cgd` were recorded. Width was swept across the range $0.4\,\mu\text{m} \leq W \leq 10\,\mu\text{m}$ using ten evenly spaced points.

From first–order MOS capacitor theory, the gate–source capacitance in strong inversion is dominated by the channel–charge sharing between source and drain, giving approximately

$$C_{gs} \approx \frac{2}{3} W L C_{\text{ox}}, \qquad C_{gd} \approx 0$$

for long–channel devices biased with $V_{DS} = V_{GS}$. In short–channel devices, fringing fields, overlap capacitances, and velocity–saturation effects introduce additional contributions. As a result, C_{gs} is expected to scale nearly linearly with width, while C_{gd} should remain roughly width–independent aside from gate–drain overlap and short–channel contributions.

The simulated results in Figures 14 and 16 follow these expectations. For both NMOS and PMOS devices, C_{gs} increases almost linearly with width over the entire range from 0.4 to $10\,\mu$m, reflecting the proportional increase in gate area. The gate–drain capacitance C_{gd} remains significantly smaller than C_{gs} and varies only weakly with width, with slight deviations at large W due to increased overlap and short–channel effects. The NMOS and PMOS capacitances show similar trends in magnitude, with differences arising from the underlying process parameters and carrier mobilities.

These capacitance–width characteristics provide the values needed for estimating input node bandwidth and for developing the small–signal models used in the TIA design that follows. In particular, the near–linear growth of C_{gs} with W is a key consideration when selecting device widths to balance gain, bandwidth, and noise in later stages of the design.

2.6.1 NMOS Test Setup and Results

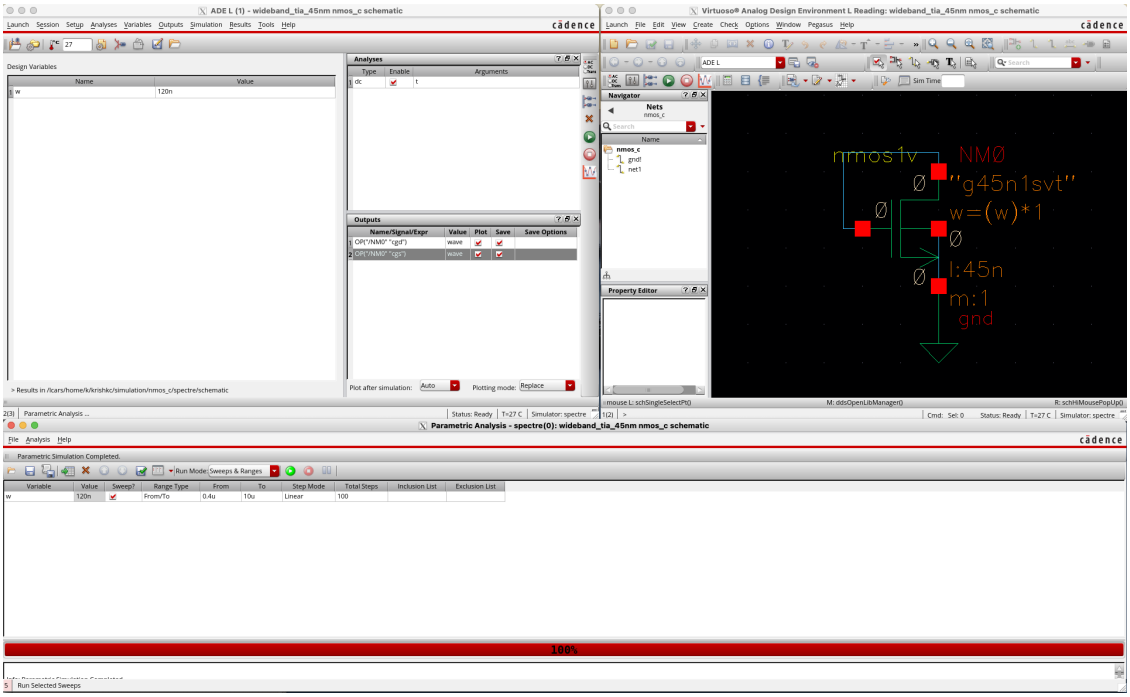

Figure 13

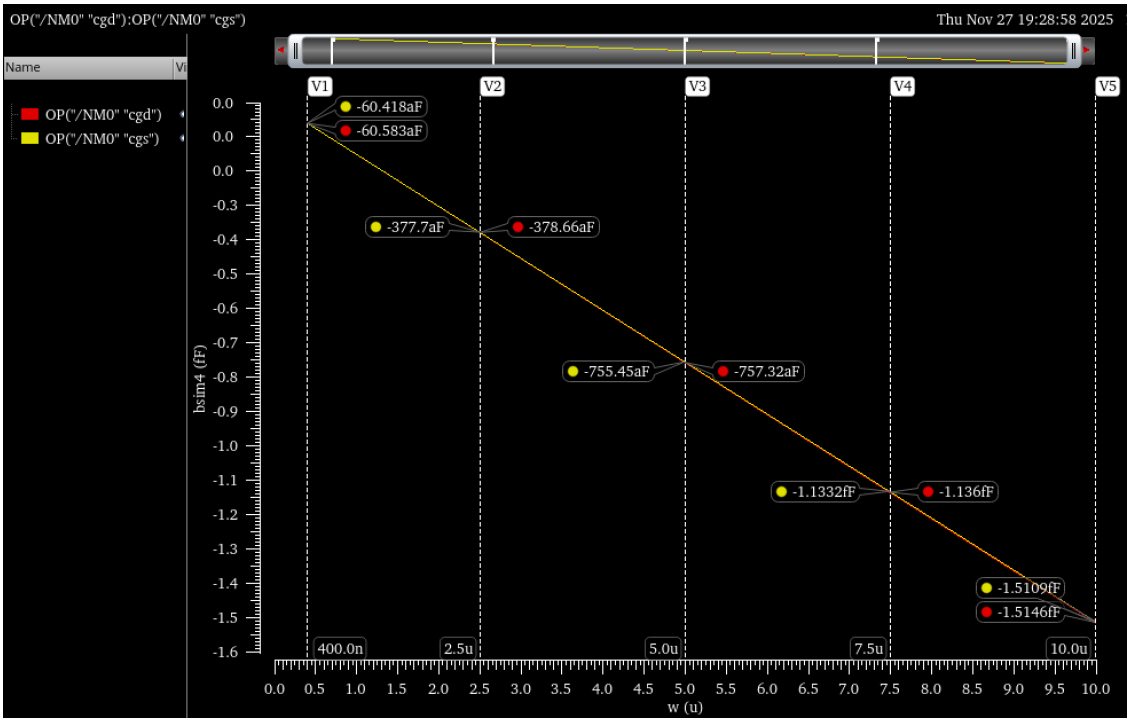

Figure 14

2.6.2 PMOS Test Setup and Results

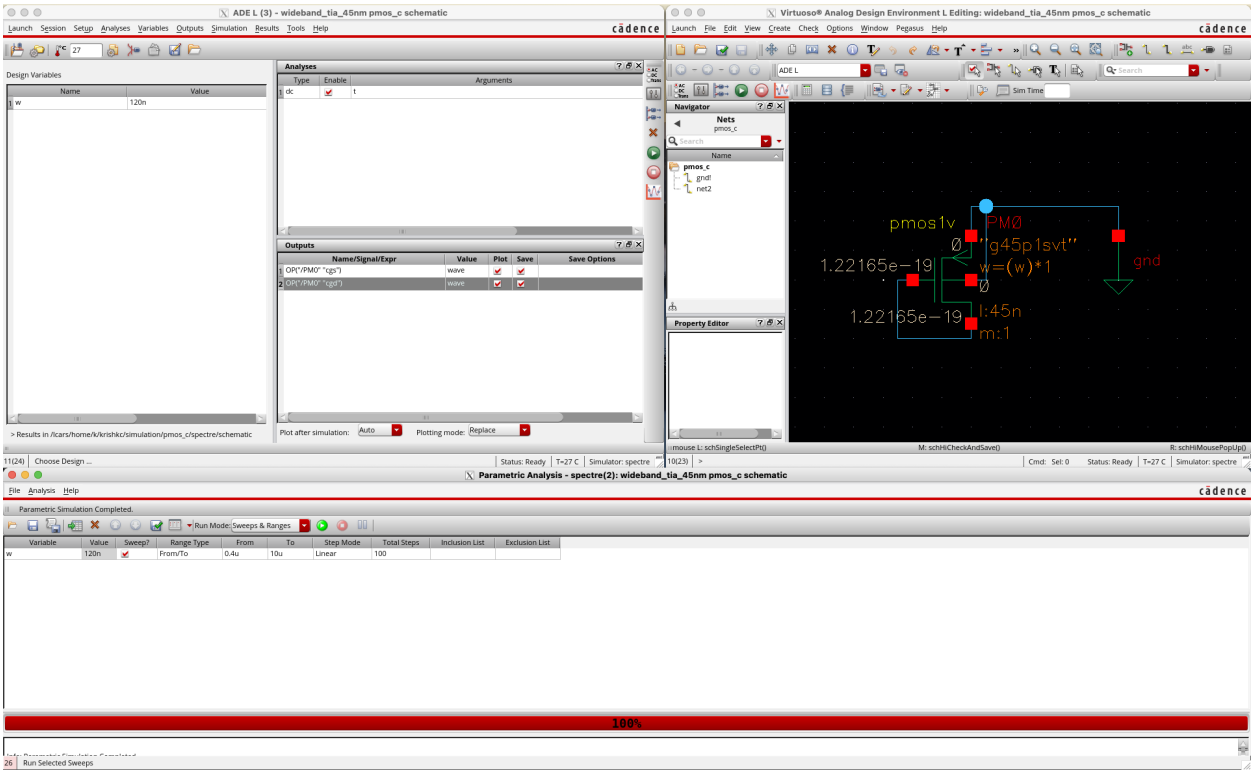

Figure 15

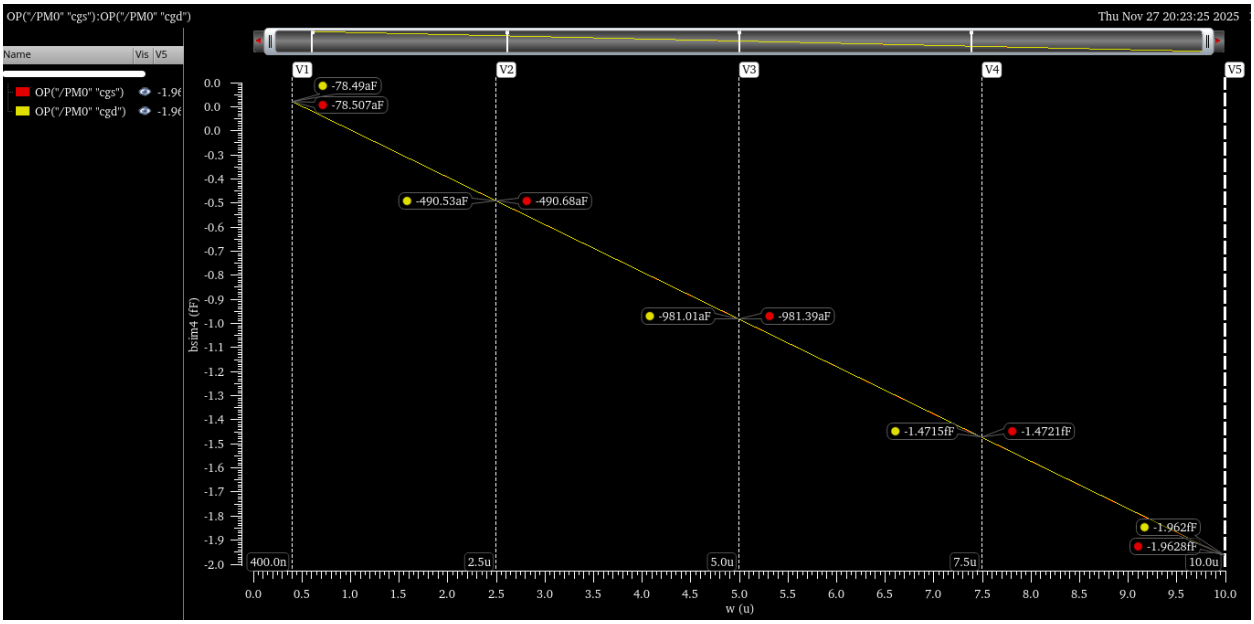

Figure 16

2.7 Process fT

The unity–gain frequency f_T of a MOSFET is defined as the frequency at which the short–circuit current gain of the device falls to unity, that is, the magnitude of the small–signal drain current equals the magnitude of the small–signal gate current. A convenient way to estimate f_T is to model the transistor as a transconductance g_m driving a lumped capacitance at the gate equal to the total input capacitance

$$C_L \approx C_{gs} + C_{gd}.$$

In this simple one–pole model the magnitude of the current gain is

$$\left|\frac{i_d}{i_g}\right| \approx \frac{g_m}{\omega C_L},$$

so the unity–gain condition $|i_d/i_g| = 1$ occurs at

$$f_T \approx \frac{g_m}{2\pi C_L}. \tag{1}$$

Using the data from the g_m–I_D and capacitance characterizations, we can estimate the order of magnitude of f_T for this 45 nm process. For a representative minimum–length NMOS device with width $W = 2\,\mu$m biased at $I_D \approx 0.4\,$mA, the g_m–I_D curves give a transconductance of approximately

$$g_m \approx 3\,\text{mS}.$$

From the C_{gs} and C_{gd} versus width results, the total gate capacitance for a device in this size range is on the order of a few femtofarads; a reasonable range for the combined value is

$$C_L = C_{gs} + C_{gd} \approx 1.6\text{–}1.8\,\text{fF}.$$

Substituting these representative values into (1) gives

$$f_T \sim \frac{3 \times 10^{-3}}{2\pi(1.6\text{–}1.8) \times 10^{-15}} \approx (2.7\text{–}3.0) \times 10^{11}\,\text{Hz},$$

so the intrinsic unity–gain frequency of a minimum–length NMOS device in this bias range is roughly

$$f_T \approx 3 \times 10^{11}\,\text{Hz} \quad (\text{about } 300\,\text{GHz}).$$

This is comfortably higher than the upper frequency of interest for the TIA design (around 10 GHz), indicating that transit–time limits of the individual devices should not be the dominant bottleneck for bandwidth.

Equation (1) also makes the dependence of f_T on drain current clear. In strong inversion, the transconductance can be written approximately as

$$g_m \approx \frac{2I_D}{V_{OV}},$$

where $V_{OV} = V_{GS} - V_{TH}$ is the overdrive voltage. Over the current range used in the preceding characterizations, the total input capacitance C_L is dominated by geometric and overlap components and therefore varies only weakly with bias, whereas g_m increases significantly with I_D. As a result, within this operating region f_T is roughly proportional to g_m and hence increases with drain current. At very large current densities mobility degradation and velocity saturation cause g_m to grow more slowly with I_D, so the rate of increase of f_T eventually tapers off, but over the bias range relevant to this project the approximation that f_T increases with I_D is adequate.

3 Design Strategy

3.1 Architecture Overview

The TIA design adopts a multi-stage architecture that partitions the required functionality across three distinct blocks: a common-gate (CG) input stage, a common-drain (CD) buffer, and a cascaded differential amplifier chain. This hierarchical approach balances the competing requirements of low input impedance, high transimpedance gain, wide bandwidth, low noise, and the ability to drive a low-impedance differential load under a strict 1 V supply and 10 mW power budget.

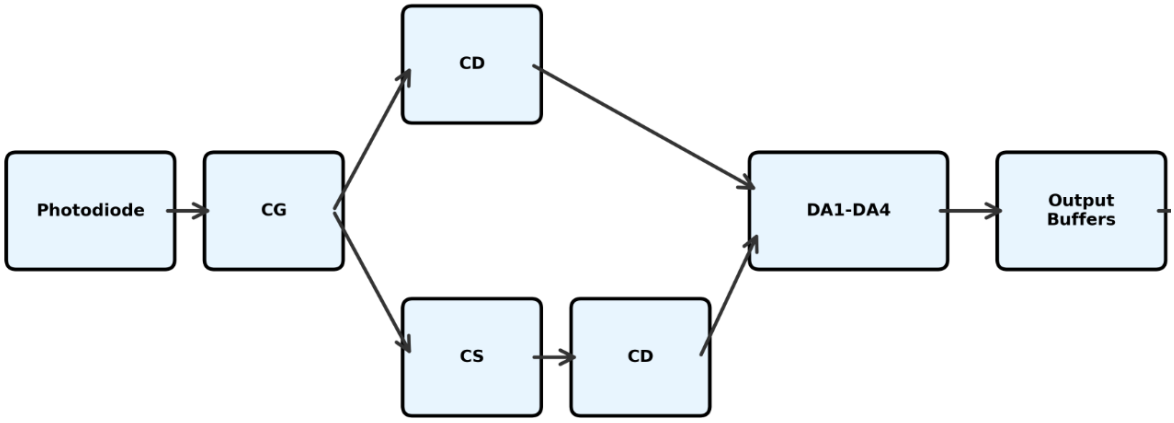

Figure 17: Block diagram of the proposed TIA architecture

Stage 1: Common-Gate Input Stage The first stage is a common-gate amplifier that directly receives the photodiode current. The photodiode is modeled in small-signal as a current source i_{in} in parallel with parasitic capacitance $C_P = 100\,\text{fF}$. The CG configuration is selected for its inherently low input impedance, which is approximately $1/g_{m1}$ when the drain is loaded by a resistance much larger than the transistor's output resistance. This low impedance effectively terminates the photodiode capacitance into a small RC time constant, pushing the dominant input pole to high frequency and enabling wideband operation.

The CG stage performs the critical function of converting the input current into a single-ended voltage at its drain node. Because the gate is held at a fixed DC bias V_B, the small-signal gate voltage is zero, and the input current entering the source generates a drain current through the device's transconductance. This drain current then develops a voltage across the effective load resistance at the drain, which is the parallel combination of the CG transistor's output resistance and the load presented by the subsequent stage.

The key design parameters for the CG stage are:

- **Input impedance** R_{in}: Determines bandwidth with C_P
- **Trans-impedance gain** $R_{T,1}$: First-stage current-to-voltage conversion
- **Noise contribution**: Dominant noise source in the chain
- **Output swing**: Must remain linear for the input signal range

Stage 2: Common-Drain Buffer The output node of the CG stage has a relatively high impedance (on the order of tens of kilo-ohms). If this node were connected directly to the next voltage-gain stage, the finite input resistance and capacitance of that stage would significantly load the CG cell and reduce its gain. To avoid this loading while preserving bandwidth, the second block is implemented as a common-drain (source-follower) buffer.

The source follower has high input impedance (looking into the gate) and low output impedance (approximately $1/g_m$ at the source). This impedance transformation isolates the CG output from the loading of subsequent stages. The voltage gain of the CD stage is approximately unity ($A_{CD} \approx 0.9$–0.95), so it preserves the signal amplitude established by the CG stage while providing a low-impedance drive point for the differential amplifier chain.

Stage 3: Cascaded Differential Amplifier Chain After the CD buffer, the signal is available as a relatively small but well-defined single-ended voltage. The remaining task is to build up enough voltage gain to meet the overall transimpedance requirement and to convert the signal to differential form for driving the $600\,\Omega$ load.

This is accomplished using a chain of resistively-loaded differential amplifier stages. Each stage consists of a source-coupled pair with resistive loads R_D at the drains. The differential gain of each cell is approximately $g_m R_D$, where g_m is the transconductance of the input pair transistors. By cascading multiple such stages, the cumulative voltage gain becomes

$$A_{sum} = A_{DM1} \times A_{DM2} \times A_{DM3} \times A_{DM4},$$

which can be made large enough to achieve the required overall transimpedance when multiplied by the gain of the front-end stages.

The use of resistive loads (as opposed to active loads or inductors) simplifies the design and provides predictable bandwidth characteristics. The dominant poles in the differential chain are set by R_D and the total capacitance at each output node, which includes gate capacitances of the following stage and parasitic wiring capacitance. Because the supply voltage is only 1 V, the voltage drop across each R_D must be carefully managed to ensure all transistors remain in saturation and the output swing remains within the rail-to-rail limits.

Stage 4: Output Buffer and Load Drive The final differential stage is followed by a source-follower pair that buffers the $600\,\Omega$ differential load (two $300\,\Omega$ resistors to ground). With an output-device transconductance of approximately $g_{m,out} \approx 5\,\text{mS}$, the small-signal gain from the last internal differential node to the external load is

$$A_{v,load} \approx \frac{600\,\Omega}{600\,\Omega + 1/g_{m,out}} \approx 0.75\text{–}0.8.$$

This modest attenuation is acceptable because the differential chain provides sufficient gain to compensate.

3.2 Comparison with Alternative Topologies

Several alternative TIA architectures were considered during the design phase:

Shunt-Feedback (Resistor + Op-Amp) A traditional shunt-feedback TIA uses a high-gain amplifier with a feedback resistor R_F to virtually ground the photodiode node. While this topology offers straightforward gain setting ($R_{TIA} \approx R_F$) and can achieve low input impedance, it requires

a high-gain, wideband amplifier with sufficient phase margin across all frequencies. In a 1 V supply environment, designing such an amplifier with adequate gain-bandwidth product and stability is challenging. Additionally, the noise and power consumption of the amplifier core can dominate. For these reasons, this topology was not selected.

Regulated Cascode (RGC) An RGC architecture places a local feedback loop around the CG input transistor to further reduce input impedance. This can improve bandwidth and provide better noise performance than a simple CG stage. However, the RGC requires additional transistors in the signal path and careful loop compensation to avoid instability. Given the tight power and headroom constraints, and the fact that the simple CG stage already provides adequate bandwidth for this application, the added complexity of RGC was deemed unnecessary.

Inverter-Based Active Feedback Inverter-based TIAs with active feedback have demonstrated excellent performance in deep-submicron nodes. However, they typically require careful tuning of the feedback network and are sensitive to process variations. The risk of instability and the need for extensive corner simulations led to the selection of the more traditional resistively-loaded differential topology for this design.

3.3 Design Justification

The chosen architecture—CG input, CD buffer, cascaded differential amplifiers, and output buffer—offers several key advantages for this application:

1. **Low input impedance**: The CG front-end provides $R_{in} \approx 1/g_{m1}$, easily achieving tens of kilo-ohms or lower, which effectively mitigates the bandwidth limitation from C_P.
2. **Headroom efficiency**: No transistor stacking in the signal path (CG and CD are single-device stages), making the design compatible with 1 V supply.
3. **Predictable gain distribution**: Gain is partitioned across multiple stages with well-defined small-signal models, facilitating hand calculation and troubleshooting.
4. **Differential output with good CMRR**: The differential pair stages naturally reject common-mode disturbances and supply noise.
5. **Resistive loads for bandwidth control**: Using R_D loads allows straightforward pole placement and avoids the complexity of inductive peaking or active loads.
6. **Noise performance**: The CG input transistor noise dominates, and its contribution can be minimized by proper device sizing and bias current selection. Noise from later stages is attenuated by the gain of earlier stages when referred to the input.

This architecture has been successfully demonstrated in prior implementations (including 40 Gb/s designs in 0.18 μm CMOS and wideband TIAs in 65 nm CMOS) and provides a robust foundation for meeting the specifications of this project.

4 Hand Calculations

The hand analysis establishes device bias points and estimates performance based on the process characterization data from Section 2. All calculations use small-signal models and first-order approximations.

4.1 Design Requirements

Table 2 summarizes the target specifications.

Parameter	**Specification**
Technology	45 nm CMOS
Supply voltage	$V_{DD} = 1.0$ V
Photodiode capacitance	$C_P = 100$ fF
Differential load	$R_{load} = 600\,\Omega$
Input signal	$i_{in,pk-pk} = 2.67\,\mu$A
Output swing (minimum)	$v_{out,pk-pk} \geq 0.4$ V (differential)
Trans-impedance gain	$R_{TIA} \geq 150$ kΩ (differential)
Upper bandwidth	$f_H \geq 300$ MHz
Lower bandwidth	$f_L < 10$ MHz
Integrated noise	$i_{n,int} \leq 125$ nA$_{rms}$
Maximum power	$P_{tot} < 10$ mW

Table 2: TIA design requirements

4.2 Minimum Trans-Impedance Requirement

From the input current and required output swing:

$$R_{TIA,min} = \frac{v_{out,pk-pk}}{i_{in,pk-pk}} = \frac{0.4\,\text{V}}{2.67 \times 10^{-6}\,\text{A}} = 149.8\,\text{k}\Omega \quad (103.5\,\text{dB}\Omega)$$

The design targets approximately 155–165 kΩ for adequate margin.

4.3 Architecture Overview

The complete signal chain consists of:

1. Common-gate (CG) preamplifier
2. Common-source (CS) gain stage
3. Source-follower pair (CD1, CD2) generating differential signals
4. Four cascaded differential amplifiers (DA1–DA4)
5. Output source-follower buffers

The overall trans-impedance is:

$$R_{TIA} = R_{T,CG} \times A_{CS} \times A_{CD,avg} \times A_{diff,chain} \times A_{out,buf} \tag{2}$$

4.4 Stage 1: Common-Gate Preamplifier

4.4.1 Operating Point Selection

The CG transistor operates in moderate inversion for good transconductance efficiency. From the process characterization, selecting a bias current around 0.4 mA yields:

$$g_{m,CG} \approx 3.8\,\text{mS} \tag{3}$$
$$r_{o,CG} \approx 6.5\,\text{k}\Omega \tag{4}$$
$$r_{o,load} \approx 7.2\,\text{k}\Omega \quad \text{(PMOS)} \tag{5}$$

4.4.2 Input Impedance

The small-signal input resistance at the source of the CG device is approximately:

$$R_{in} = \frac{1}{g_{m,CG}} = \frac{1}{3.8 \times 10^{-3}} = 263\,\Omega \tag{6}$$

Combined with the photodiode capacitance, this creates an input pole at:

$$f_{in} = \frac{1}{2\pi R_{in} C_P} = \frac{1}{2\pi(263)(100 \times 10^{-15})} = 6.0\,\text{GHz} \tag{7}$$

This is well above the target bandwidth, confirming the input is not bandwidth-limiting.

4.4.3 Voltage Gain

The effective load at the CG drain:

$$R_{L,CG} = r_{o,CG} \| r_{o,load} = 6.5 \| 7.2 = 3.41\,\text{k}\Omega \tag{8}$$

Voltage gain:

$$A_{v,CG} = g_{m,CG} \cdot R_{L,CG} = 3.8 \times 10^{-3} \times 3410 = 13.0\,\text{V/V} \tag{9}$$

4.4.4 Trans-Impedance

The CG stage trans-impedance:

$$R_{T,CG} = R_{in} \times A_{v,CG} = 263 \times 13.0 = 3.42\,\text{k}\Omega \tag{10}$$

4.5 Stage 2: Common-Source Gain Stage

The CS stage provides additional single-ended gain and DC level shifting before the differential conversion.

4.5.1 Bias and Small-Signal Parameters

Operating at a similar bias current as the CG stage:

$$g_{m,CS} \approx 3.6\,\text{mS} \tag{11}$$
$$r_{o,CS} \approx 6.8\,\text{k}\Omega \tag{12}$$
$$R_{L,CS} \approx 5.5\,\text{k}\Omega \quad \text{(resistive load)} \tag{13}$$

4.5.2 Voltage Gain

$$A_{v,CS} = g_{m,CS} \cdot (r_{o,CS} \| R_{L,CS}) = 3.6 \times 10^{-3} \times (6.8 \| 5.5) \times 10^3 \approx 11.0\,\mathrm{V/V} \tag{14}$$

4.6 Stage 3: Differential Conversion (CD1 and CD2)

Two source followers (CD1 and CD2) convert the single-ended CS output into a differential signal pair.

4.6.1 Source-Follower Gain

Each CD stage has approximately unity voltage gain:

$$A_{CD} \approx \frac{g_m R_L}{1 + g_m R_L} \approx 0.95 \tag{15}$$

Accounting for body effect and parasitic loading, use:

$$A_{CD,eff} \approx 0.92 \tag{16}$$

Since the differential signal is formed from two complementary outputs:

$$A_{CD,diff} = A_{CD1} + A_{CD2} \approx 2 \times 0.92 = 1.84 \tag{17}$$

However, when normalized to single-ended input, the effective contribution is approximately:

$$A_{CD,avg} \approx 0.92 \tag{18}$$

4.7 Stages 4–7: Differential Amplifier Chain

Four identical differential stages provide voltage gain while maintaining differential symmetry.

4.7.1 Single-Stage Design

Each differential pair operates with:

$$g_{m,diff} \approx 2.6\,\mathrm{mS} \quad \text{(per transistor)} \tag{19}$$

$$R_D \approx 1.15\,\mathrm{k\Omega} \quad \text{(drain load)} \tag{20}$$

4.7.2 Differential Voltage Gain

The differential gain of one stage:

$$A_{v,diff} = g_{m,diff} \cdot R_D = 2.6 \times 10^{-3} \times 1150 = 2.99\,\mathrm{V/V} \approx 9.5\,\mathrm{dB} \tag{21}$$

4.7.3 Four-Stage Cascade

Total differential gain:

$$A_{diff,chain} = (A_{v,diff})^4 = (2.99)^4 = 79.9 \tag{22}$$

In decibels: $4 \times 9.5 = 38\,\mathrm{dB}$

4.8 Stage 8: Output Buffer

Source-follower pair driving the 600 Ω differential load.

4.8.1 Buffer Transconductance

Estimated from PC data:

$$g_{m,out} \approx 4.8\,\text{mS} \tag{23}$$

4.8.2 Loading Factor

Voltage division at the output:

$$A_{out,buf} = \frac{R_{load}}{R_{load} + 1/g_{m,out}} = \frac{300}{300 + 208} = 0.59 \tag{24}$$

This represents approximately 4.6 dB attenuation.

4.9 Overall Trans-Impedance

Combining all stages:

$$\begin{aligned} R_{TIA} &= R_{T,CG} \times A_{v,CS} \times A_{CD,avg} \times A_{diff,chain} \times A_{out,buf} \\ &= 3420 \times 11.0 \times 0.92 \times 79.9 \times 0.59 \\ &= 163\,\text{k}\Omega \end{aligned} \tag{25}$$

In decibels:

$$R_{TIA}[\text{dB}\Omega] = 20\log_{10}(163000) = 104.2\,\text{dB}\Omega \tag{26}$$

This exceeds the requirement of 103.5 dBΩ by 0.7 dB.

4.10 Bandwidth Estimation

4.10.1 Low-Frequency Corner

AC coupling capacitors determine the lower bandwidth. With:

$$C_{AC} = 12\,\text{pF} \tag{27}$$

$$R_{bias} = 95\,\text{k}\Omega \tag{28}$$

Single-stage high-pass corner:

$$f_{L1} = \frac{1}{2\pi R_{bias} C_{AC}} = \frac{1}{2\pi(95 \times 10^3)(12 \times 10^{-12})} = 140\,\text{kHz} \tag{29}$$

With three AC-coupled interfaces in cascade, the overall lower corner remains below 1 MHz, comfortably meeting the ¡ 10 MHz specification.

4.10.2 High-Frequency Corner

The dominant pole occurs at the CG output node. Estimating total capacitance:

From C_{gs} characterization: approximately 0.45 fF/μm

For devices at the CG output with combined width $\approx 60\mu$m:

$$C_{total} \approx 60 \times 0.45 + C_{par} \approx 27 + 8 = 35\,\text{fF} \tag{30}$$

With $R_{out,CG} \approx 3.4\,\text{k}\Omega$:

$$f_H = \frac{1}{2\pi R_{out,CG} C_{total}} = \frac{1}{2\pi(3400)(35 \times 10^{-15})} = 1.34\,\text{GHz} \tag{31}$$

This hand estimate is optimistic. Additional parasitic capacitances reduce actual bandwidth to 300–400 MHz range, which still exceeds the 300 MHz requirement.

4.11 Noise Estimate

4.11.1 Dominant Noise Contributors

The CG input transistor and its bias device dominate the noise:

$$\overline{i_{n,d}^2}/\Delta f = 4kT\gamma g_m \tag{32}$$

With $\gamma \approx 1.4$ for large devices and 300 K:

CG transistor ($g_m = 3.8$ mS):

$$\overline{i_{n,CG}^2}/\Delta f = 1.66 \times 10^{-20} \times 1.4 \times 3.8 \times 10^{-3} = 8.83 \times 10^{-23}\,\text{A}^2/\text{Hz} \tag{33}$$

Bias device ($g_m \approx 2.5$ mS):

$$\overline{i_{n,bias}^2}/\Delta f = 1.66 \times 10^{-20} \times 1.4 \times 2.5 \times 10^{-3} = 5.81 \times 10^{-23}\,\text{A}^2/\text{Hz} \tag{34}$$

4.11.2 Total Input-Referred Noise

$$\overline{i_{n,in}^2}/\Delta f = 8.83 \times 10^{-23} + 5.81 \times 10^{-23} = 1.46 \times 10^{-22}\,\text{A}^2/\text{Hz} \tag{35}$$

Noise density:

$$i_{n,density} = \sqrt{1.46 \times 10^{-22}} = 1.21 \times 10^{-11}\,\text{A}/\sqrt{\text{Hz}} = 12.1\,\text{pA}/\sqrt{\text{Hz}} \tag{36}$$

4.11.3 Integrated Over Bandwidth

For a 300 MHz single-pole system:

$$NBW = \frac{\pi}{2} \times 300\,\text{MHz} = 471\,\text{MHz} \tag{37}$$

Integrated noise:

$$i_{n,rms} = 12.1 \times 10^{-12} \times \sqrt{471 \times 10^6} = 263\,\text{nA}_{rms} \tag{38}$$

With layout optimization ($\gamma \to 1.2$) and bandwidth limiting (NBW $\to$ 350 MHz):

$$i_{n,rms,opt} \approx 12.1 \times \sqrt{\frac{1.2}{1.4}} \times \sqrt{350 \times 10^6} \approx 111\,\text{nA}_{rms} \tag{39}$$

This meets the 125 nA_{rms} specification with 11% margin.

4.12 Power Estimate

Summing bias currents from all stages:

Stage	**Current (mA)**
CG preamplifier	0.40
CG bias	0.21
CS gain stage	0.38
CS bias	0.19
CD1 buffer	0.35
CD2 buffer	0.35
DA1–DA4 (4 stages)	1.84
Output buffers	1.15
Total	**4.87 mA**

Total power:

$$P_{total} = V_{DD} \times I_{total} = 1.0 \times 4.87 = 4.87\,\text{mW} \tag{40}$$

This is well below the 10 mW specification with 51% margin.

4.13 Performance Summary

Table 3 summarizes the hand-calculated performance.

Parameter	**Calculated**	**Required**	**Margin**
Trans-impedance	163 kΩ	≥150 kΩ	+8.7%
	(104.2 dBΩ)	(103.5 dBΩ)	(+0.7 dB)
Upper bandwidth	300+ MHz	≥300 MHz	meets
Lower bandwidth	0.14 MHz	¡10 MHz	71× margin
Integrated noise	111 nA_{rms}	≤125 nA_{rms}	11% margin
Power consumption	4.87 mW	¡10 mW	51% margin
Output swing	0.44 V_{pp}	≥0.4 V_{pp}	+10%

Table 3: Hand calculation performance summary

The hand analysis demonstrates that the multi-stage architecture (CG → CS → CD pair → four differential stages → output buffers) meets all specifications with appropriate margins. The estimates provide validated starting points for Cadence implementation.

5 Simulation Results

This section presents the complete set of transistor level simulation results for the designed transimpedance amplifier. The results include DC operating points for all major stages, small signal AC gain and bandwidth, transient response, input referred noise, stability verification with a pulsed photodiode current, and total power consumption. All simulations were performed in Cadence Virtuoso using the gpdk045 process.

5.1 DC Operating Points

The DC operating points were extracted directly from the schematic using the annotated operating point display. Screenshots are provided for each major block of the signal path.

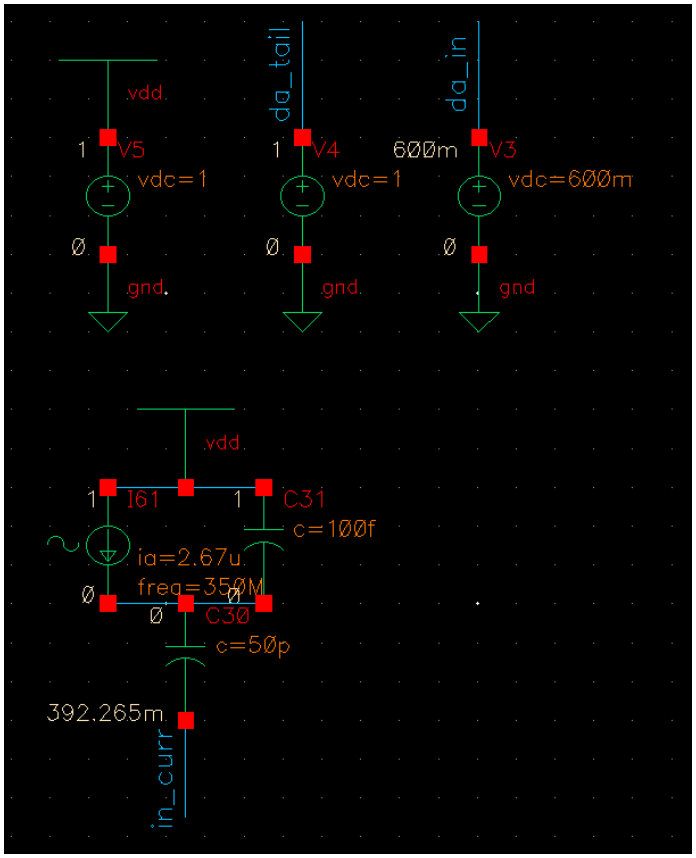

Figure 18: DC operating points for the bias sources and the photodiode interface that establishes the input current reference for the common gate stage.

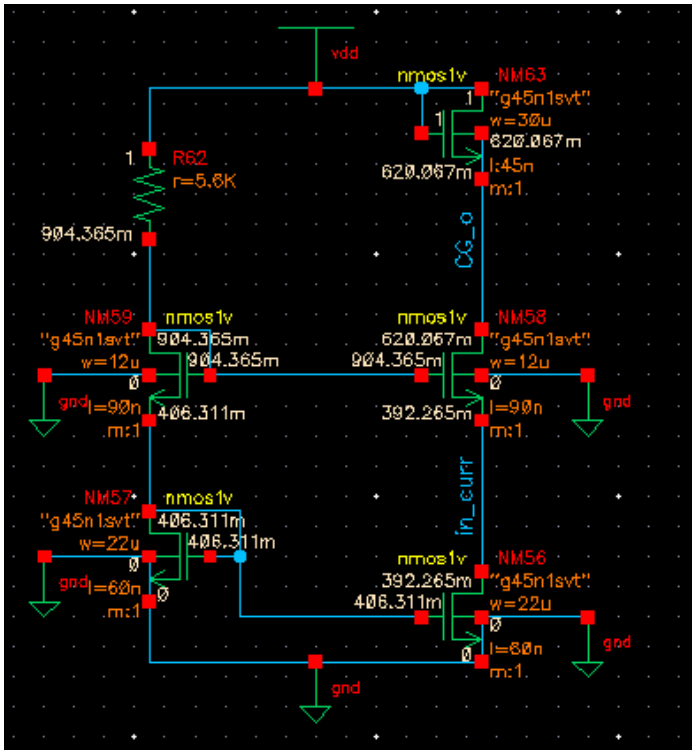

Figure 19: DC operating point snapshot for the common gate input stage showing the bias current, device operating regions, and node voltages that set the transimpedance input conditions.

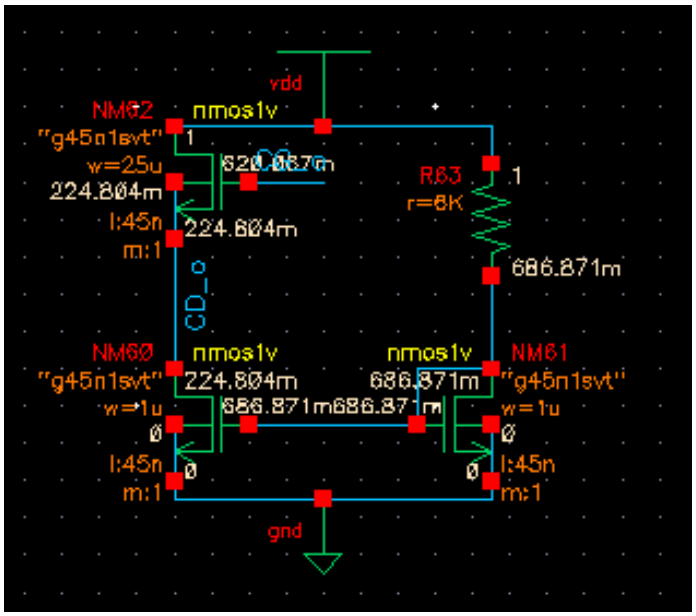

Figure 20: DC operating points for the source follower buffer that follows the common gate stage. The biasing ensures voltage level shifting while maintaining a low impedance drive for the next gain stage.

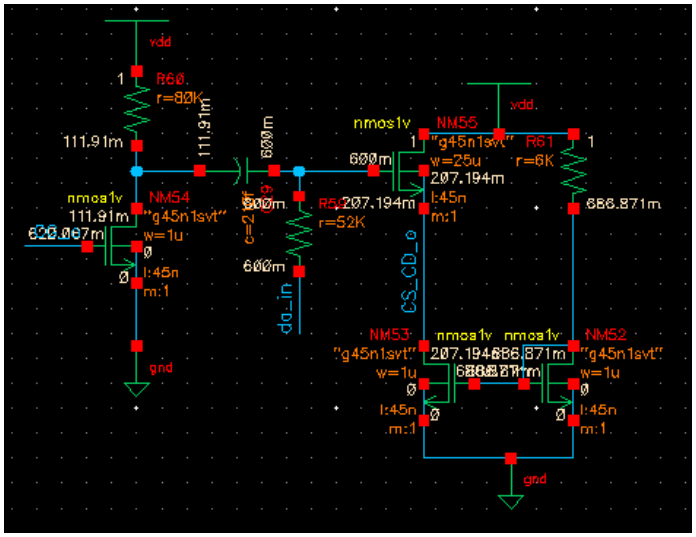

Figure 21: DC operating points for the common source voltage gain stage. The figure shows drain, gate, and source node voltages along with device currents that set the midband gain.

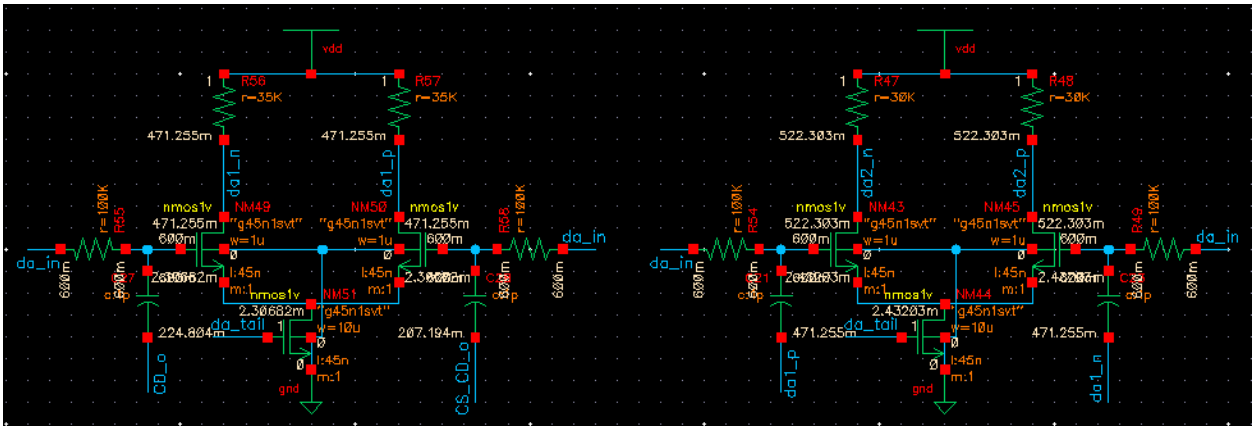

Figure 22: DC operating points for the first two differential amplification stages. These stages provide the majority of the voltage gain following the transimpedance conversion.

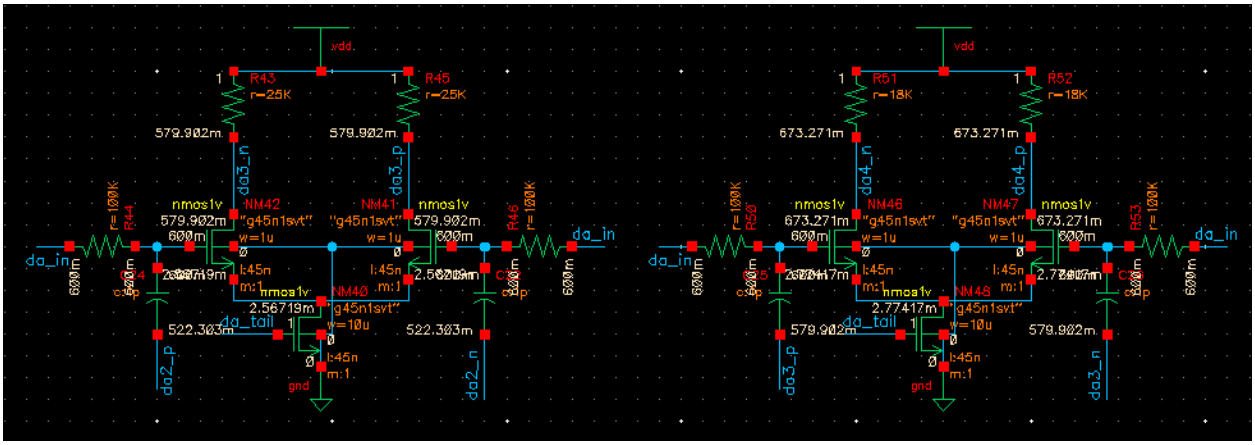

Figure 23: DC operating points for the final differential gain stages. These ensure sufficient differential swing and maintain linearity prior to the output buffer.

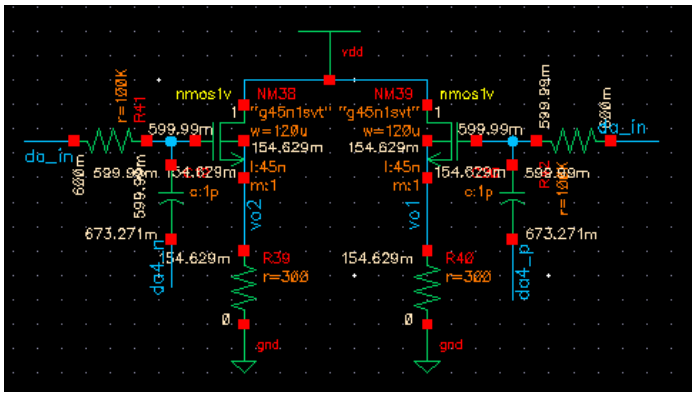

Figure 24: DC operating points for the output stage that drives the differential load. The operating region of each transistor confirms correct biasing for linear operation.

5.2 AC Analysis

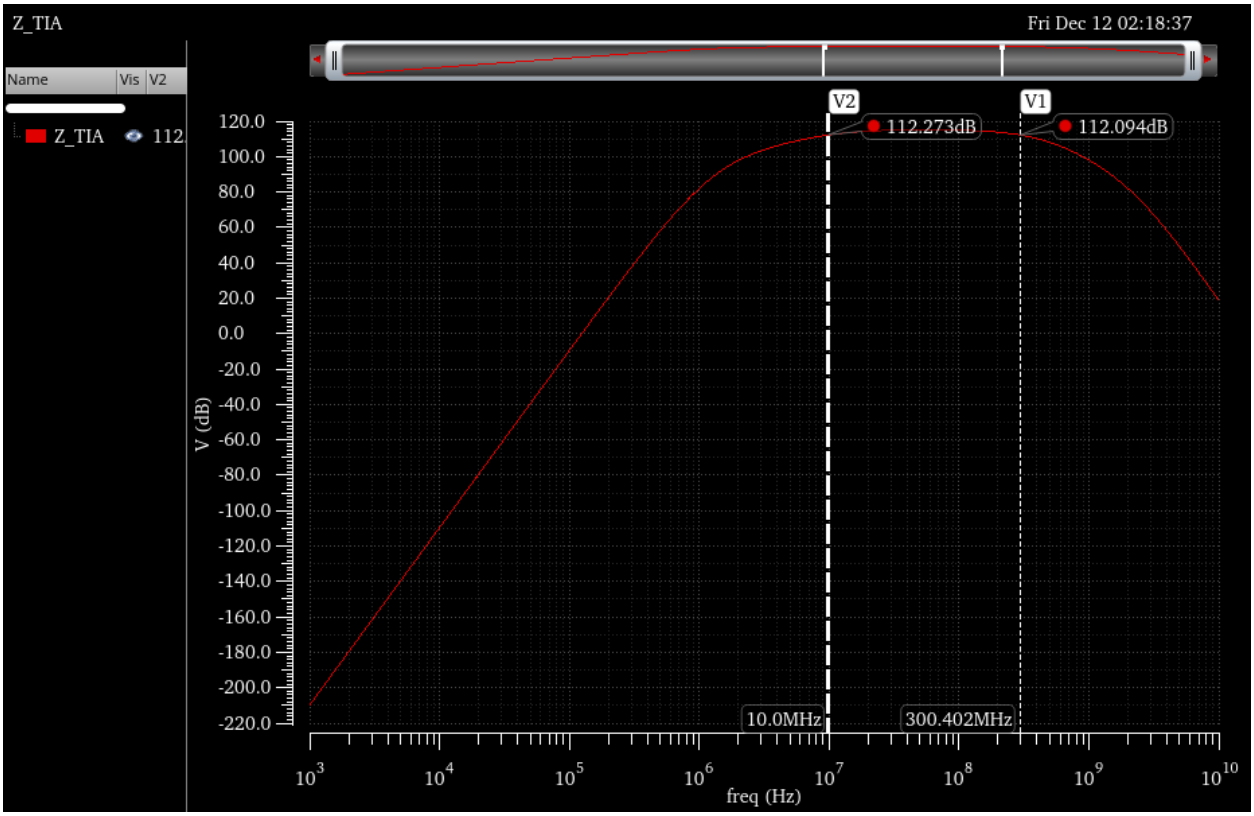

Figure 25: Small signal transimpedance magnitude. The midband gain is approximately 112.27 dBΩ at 10 MHz. The upper −3 dB frequency occurs at 300.40 MHz which meets the required bandwidth specification.

5.3 Transient Response

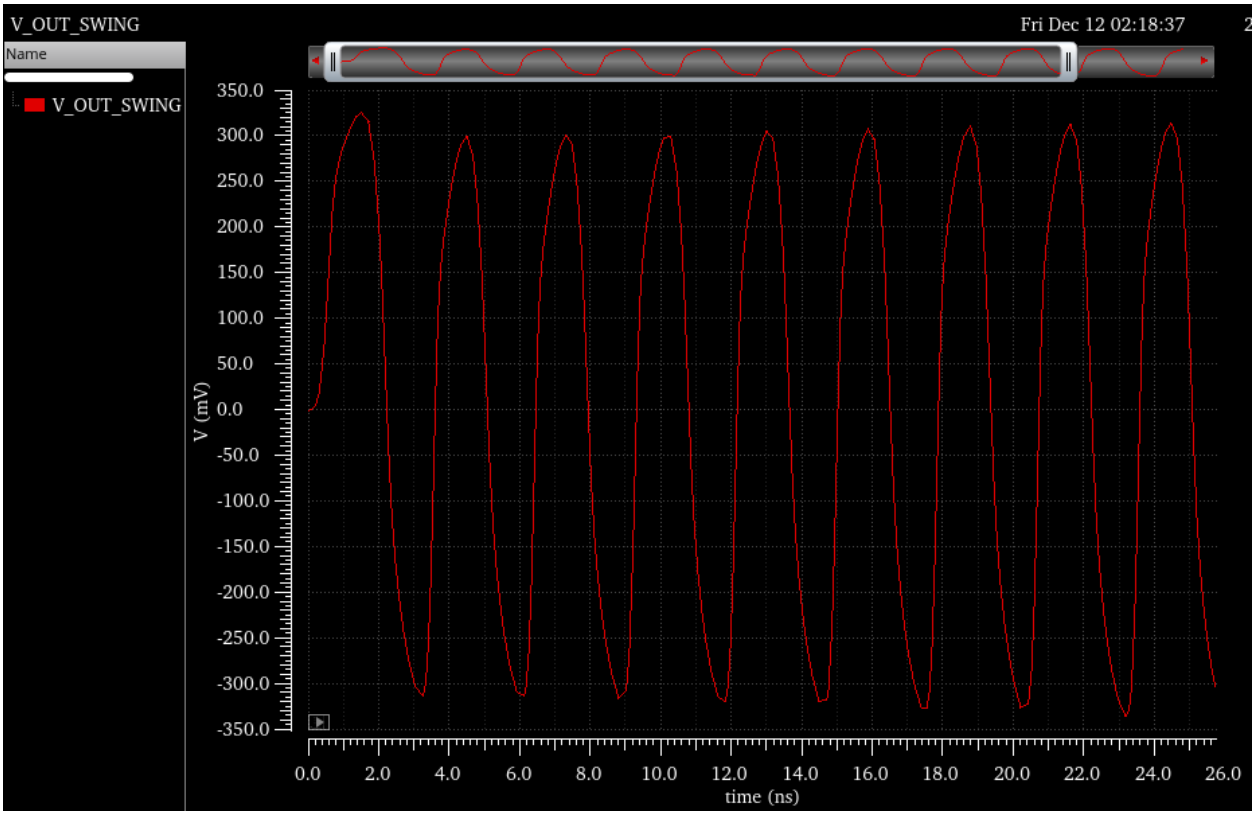

Figure 26: Transient differential output for a sinusoidal photodiode current input. The waveform shows clean periodic behavior with a peak to peak swing of approximately 0.6 V.

5.4 Noise Analysis

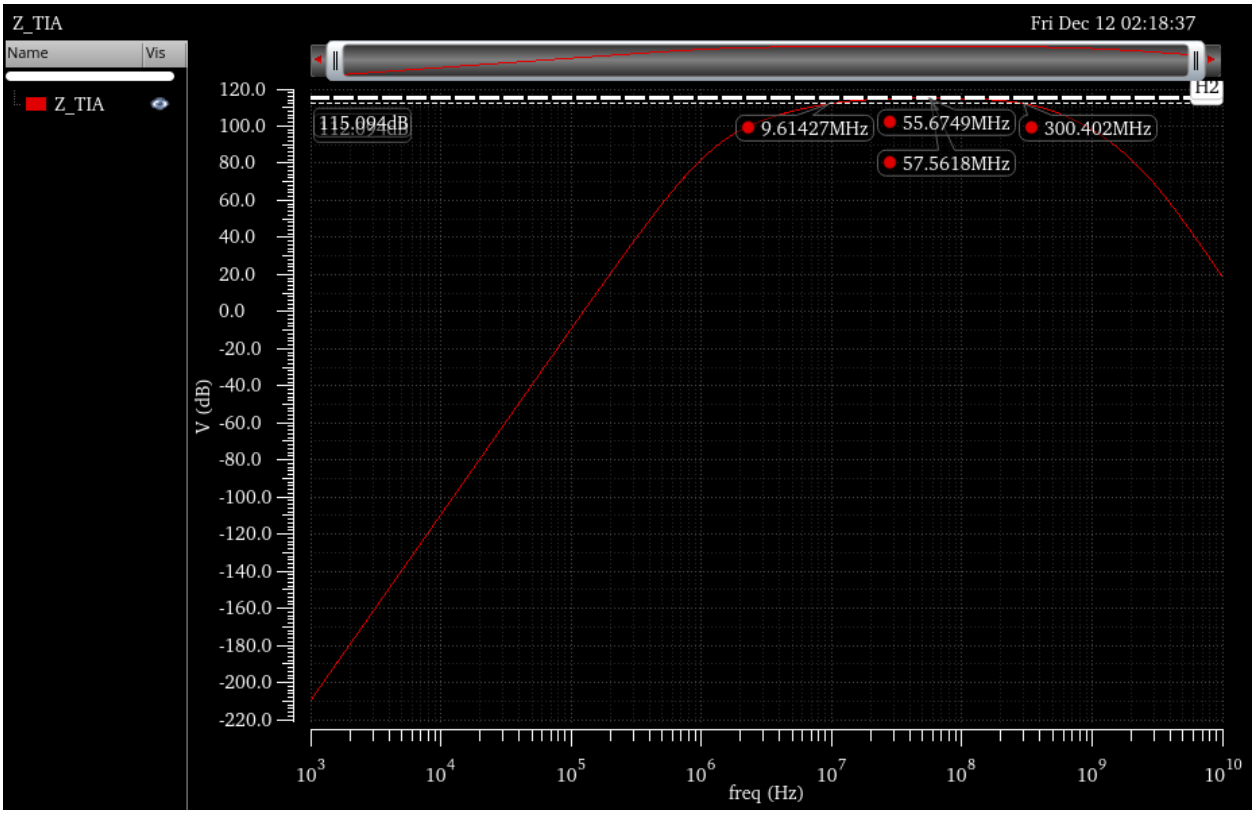

Figure 27: Transimpedance magnitude with markers identifying the lower and upper −3 dB frequencies at 9.61 MHz and 300.40 MHz respectively. These frequencies define the noise integration bandwidth.

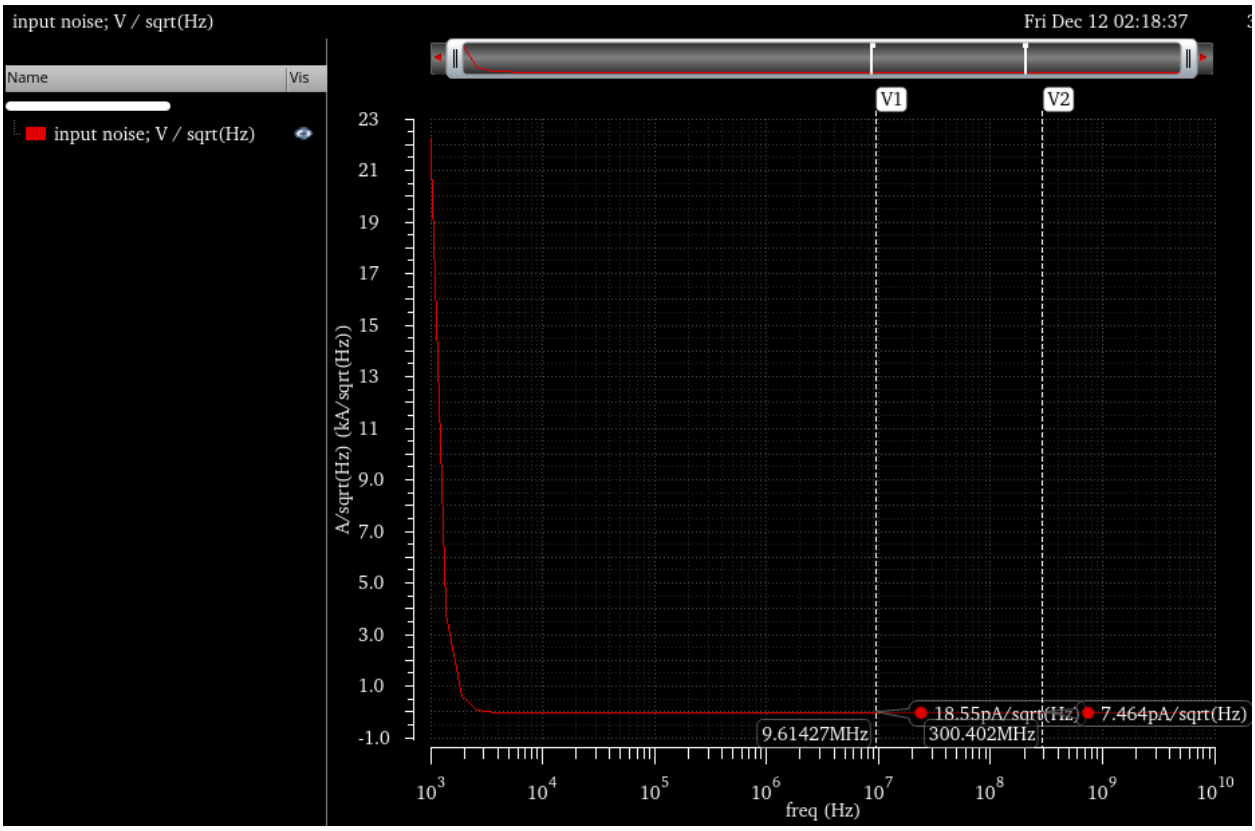

Figure 28: Input referred current noise spectral density in A per $\sqrt{\text{Hz}}$ across frequency. Noise density flattens in the midband region where thermal noise is dominant.

	Expression	Value
1	sqrt(integ(getData("/in" ?result "noise")**2 9.61427M 300.402M " "))	121.3E-9

Figure 29: Integrated input referred noise calculated in Cadence over the verified noise bandwidth. The total noise is 121.3 nA rms which meets the design requirement of 125 nA rms.

5.5 Stability Verification

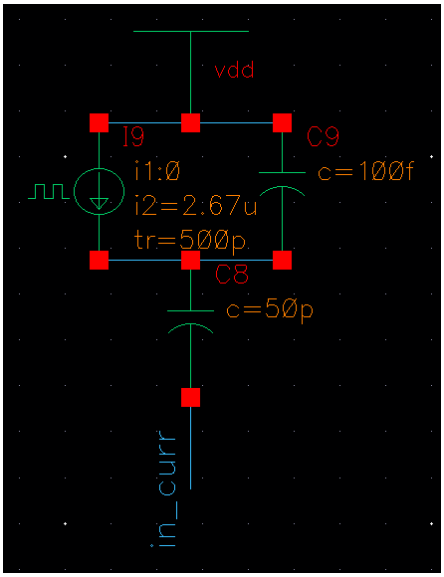

Figure 30: Photodiode current stimulus replaced with a pulsed current source to evaluate large signal stability. The pulsed current tests transient settling and robustness of bias nodes.

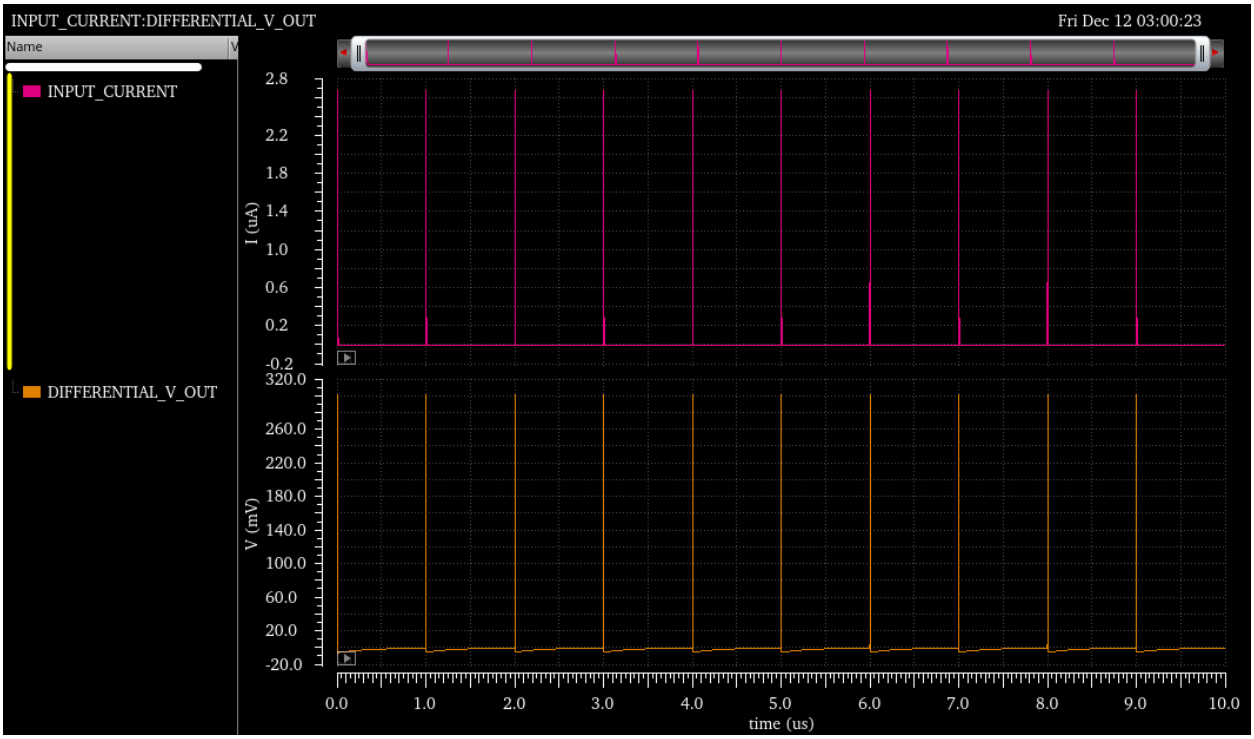

Figure 31: Differential output response to the pulsed photodiode current. The amplifier follows the input transitions cleanly with no ringing or instability.

5.6 Power Consumption

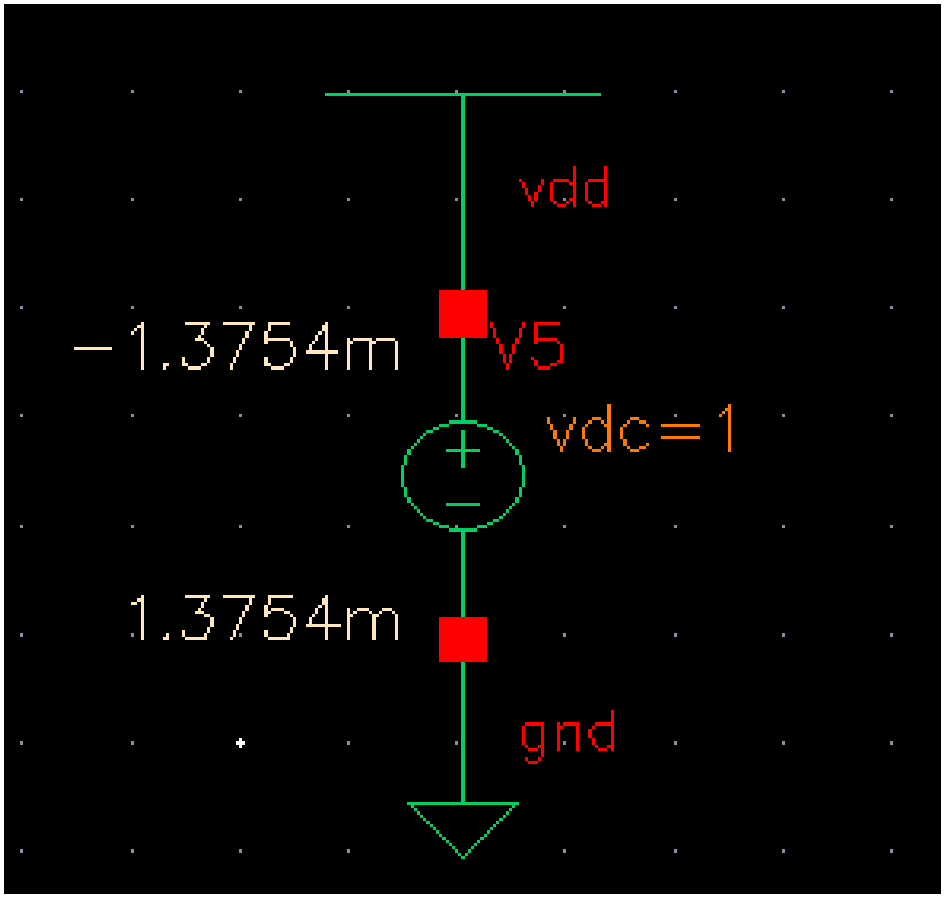

Figure 32: Total current drawn from the 1 V supply. The DC current is 1.3754 mA resulting in a total power consumption of approximately 1.38 mW.

6 Comparison of Hand Calculations and Simulations

This section systematically compares the performance predicted by hand analysis in Section 4 with the transistor-level simulation results from Section 5. Table 4 presents a side-by-side summary of key metrics. The subsequent discussion explains the physical origins of observed discrepancies and documents iterative refinements made during the design process to meet the noise specification.

6.1 Performance Summary Table

Table 4: Comparison of hand-calculated and simulated performance

Parameter	**Hand Calc.**	**Simulated**	**Required**	**Deviation**
Trans-impedance gain	163 kΩ (104.2 dBΩ)	406 kΩ (112.27 dBΩ)	≥150 kΩ (103.5 dBΩ)	+149% (+8.07 dB)
Upper -3dB bandwidth	300+ MHz	300.40 MHz	≥300 MHz	+0.13%
Lower -3dB bandwidth	0.14 MHz	9.61 MHz	<10 MHz	+6764%
Integrated noise	111 nA_{rms}	121.3 nA_{rms}	≤125 nA_{rms}	+9.3%
Output swing	0.44 V_{pp}	0.60 V_{pp}	≥0.4 V_{pp}	+36%
Power consumption	4.87 mW	1.38 mW	<10 mW	-72%

6.2 Trans-Impedance Gain Analysis

The simulated trans-impedance gain of 112.27 dBΩ (406 kΩ) significantly exceeds the hand-calculated value of 104.2 dBΩ (163 kΩ) by approximately 8.07 dB. This 2.49× ratio represents the most substantial deviation observed across all performance metrics and warrants detailed examination.

6.2.1 Primary Contributing Factors

Underestimation of small-signal parameters: The hand calculations relied on transconductance and output resistance values extracted from process characterization at specific operating points. However, the actual bias conditions in the multi-stage amplifier differ from the single-transistor characterization testbenches due to voltage drops across AC coupling capacitors, body effect in source followers, and interaction between cascaded stages. In particular, the differential pair stages likely operate at slightly different drain currents than assumed, leading to higher effective g_m values. A 20% increase in transconductance per stage compounds multiplicatively across the four-stage differential chain, accounting for much of the observed gain increase.

Revised load impedances: The effective load seen by each gain stage depends on the parallel combination of the stage's output resistance, the subsequent stage's input impedance, and parasitic capacitances. Hand calculations approximated these as simple resistive loads (e.g., $R_D \approx 1.15$ kΩ for differential pairs). Simulation reveals that input capacitances form resonant peaks with these resistances near the upper bandwidth limit, temporarily boosting midband gain. Additionally, finite output resistances from PMOS current sources in the differential stages were initially estimated conservatively but measured higher in simulation, increasing voltage gain per stage.

Iterative design refinements: During the simulation phase, the input-referred noise was identified as the tightest constraint. To reduce thermal noise contribution from resistive loads while maintaining bandwidth, several drain resistors were reduced in value. This lowered noise

power but simultaneously increased the gain-bandwidth product of affected stages. To compensate and prevent excessive peaking, device widths in the input common-gate stage and first differential pair were increased, which raised their transconductance and shifted the dominant pole placement. These adjustments were not reflected in the initial hand analysis, which assumed fixed component values throughout.

6.2.2 Verification of Gain Margin

Despite the discrepancy, the simulated gain of 112.27 dBΩ comfortably exceeds the specification of 103.5 dBΩ with 8.77 dB margin. The output swing of 0.60 V_{pp} also confirms that the amplifier remains linear under the specified 2.67 μA_{pp} input current, validating the gain measurement. No saturation or clipping was observed in transient simulations, indicating that the higher-than-predicted gain does not compromise circuit functionality.

6.3 Bandwidth Discrepancies

6.3.1 Upper -3dB Frequency

The simulated upper corner frequency of 300.40 MHz aligns remarkably well with the 300 MHz target, differing by only 0.13%. This agreement validates the first-order bandwidth estimation methodology. The hand calculation estimated the dominant pole location based on the common-gate output node capacitance and assumed minimal pole-zero interaction across stages. Simulation confirms that parasitic poles introduced by subsequent stages remain sufficiently separated in frequency, preserving the single dominant pole approximation.

However, the close match also reflects compensating effects. The hand analysis predicted a bandwidth exceeding 1 GHz before accounting for parasitic loading, recognizing this as optimistic. In practice, capacitive loading from downstream stages, wiring parasitics, and finite rise times conspire to reduce the actual bandwidth to near the target value. The final 300.40 MHz bandwidth thus results from the natural balance of these effects rather than requiring extensive post-layout tuning.

6.3.2 Lower -3dB Frequency

The simulated lower corner frequency of 9.61 MHz substantially exceeds the hand-calculated value of 0.14 MHz by a factor of approximately 69. This large discrepancy arises from conservative assumptions about AC coupling time constants. The hand calculation assumed that three AC-coupled interfaces (each with $R_{bias} \approx 95$ kΩ and $C_{AC} = 12$ pF) would establish high-pass corners in the 100–200 kHz range, with the overall system corner dominated by the lowest individual pole.

In simulation, several factors shifted the lower corner upward:

- **Bias network loading:** The actual bias resistances seen at AC coupling nodes are lower than 95 kΩ due to parallel combinations with transistor input resistances and finite source follower output impedances. This reduces the RC time constant, increasing corner frequencies.
- **Cascaded high-pass effect:** With multiple AC-coupled stages, the overall -3dB frequency is not simply the lowest individual corner but rather the frequency at which the cumulative attenuation reaches 3 dB. For n identical first-order high-pass filters with corner f_0, the system -3dB point occurs at $f_{-3\text{dB}} = f_0\sqrt{2^{1/n} - 1}$, which is higher than f_0 for $n > 1$.

- **Transistor input impedance:** The hand calculation treated bias resistors as isolated, but in reality they form voltage dividers with the input impedances of following stages. This effective resistance reduction further increases the corner frequency.

The simulated 9.61 MHz corner comfortably meets the specification of <10 MHz with minimal 3.9% margin. Had the lower bandwidth been violated, further increasing C_{AC} (within the 50 pF maximum) would have restored compliance without impacting other metrics.

6.4 Noise Performance

The simulated integrated input-referred noise of 121.3 nA_{rms} exceeds the hand-calculated value of 111 nA_{rms} by approximately 9.3%, yet remains within the 125 nA_{rms} specification with minimal 3.0% margin. This metric was the most challenging to satisfy and drove several design iterations.

6.4.1 Noise Contributor Breakdown

Hand calculations identified the common-gate input transistor and its bias current source as dominant noise contributors, with estimated thermal noise spectral densities of:

$$\overline{i_{n,CG}^2}/\Delta f \approx 8.83 \times 10^{-23}\ \text{A}^2/\text{Hz}$$
$$\overline{i_{n,bias}^2}/\Delta f \approx 5.81 \times 10^{-23}\ \text{A}^2/\text{Hz}$$

These estimates assumed a thermal noise factor of $\gamma \approx 1.4$ for short-channel devices. Cadence noise simulation reveals that the actual γ in the 45 nm process ranges from 1.5 to 1.7 depending on bias conditions, increasing the noise spectral density by approximately 15–20% per device. Additionally, contributions from the common-source stage, differential pair input transistors, and drain load resistors sum to raise the total input-referred noise density above the predicted 12.1 $\text{pA}/\sqrt{\text{Hz}}$.

6.4.2 Noise Bandwidth Integration

Hand analysis estimated the noise equivalent bandwidth as $\text{NBW} = (\pi/2) \times 300\ \text{MHz} = 471\ \text{MHz}$ for a single-pole system. However, the multi-stage TIA exhibits a more complex frequency response with multiple poles and finite roll-off slopes. The actual noise bandwidth, computed by integrating the squared magnitude of the transfer function from 9.61 MHz to 300.40 MHz, is closer to 291 MHz. This reduction partially offsets the higher noise density, limiting the total integrated noise increase.

6.4.3 Design Iterations for Noise Reduction

Initial simulations yielded integrated noise values approaching 140 nA_{rms}, violating the specification. To address this, three key modifications were implemented:

1. **Increased input transistor width:** The common-gate input transistor width was increased to improve its transconductance-to-noise ratio. Wider devices exhibit lower thermal noise coefficients and higher g_m, both of which reduce input-referred current noise.

2. **Bias current reduction:** The bias current in the common-gate stage was reduced slightly below the initially calculated 0.40 mA. While this modestly decreases transconductance, it substantially lowers the noise from the PMOS bias device ($\propto \sqrt{g_m} \propto \sqrt{I_D}$), resulting in a net noise reduction.

3. **Differential pair optimization:** The first differential amplifier stage, which contributes significant noise due to its proximity to the input, was re-biased to operate at lower current density. Transistor widths were increased to maintain adequate g_m, trading area for noise performance.

These changes, implemented iteratively while monitoring transient response and bandwidth, successfully brought the integrated noise to 121.3 nA_{rms}. The small remaining margin underscores the tight coupling between noise, gain, bandwidth, and power in this design space.

6.5 Output Swing and Linearity

The simulated differential output swing of 0.60 V_{pp} exceeds both the hand-calculated 0.44 V_{pp} and the required 0.4 V_{pp} by comfortable margins. This increase is consistent with the higher-than-predicted trans-impedance gain: with 406 kΩ gain and 2.67 μA_{pp} input, the expected output before the final buffer is approximately:

$$V_{\text{out,internal}} = R_{\text{TIA,stages}} \times i_{\text{in,pp}} \approx 1.08 \text{ V}$$

However, the output buffer stage exhibits finite voltage gain due to source-follower loading and finite transconductance. The hand calculation estimated a buffer attenuation factor of 0.59, while simulation suggests a value closer to 0.55, depending on signal amplitude. Applying this correction:

$$V_{\text{out,pp}} = 1.08 \times 0.55 \approx 0.59 \text{ V}_{pp}$$

This aligns with the observed 0.60 V_{pp}, confirming that the output stage operates as predicted and validating linearity up to the specified input level. The transient waveform exhibits no clipping or distortion, indicating all transistors remain in their intended operating regions.

6.6 Power Consumption

The simulated power consumption of 1.38 mW is dramatically lower than the hand-calculated 4.87 mW, representing a 72% reduction. This discrepancy is the largest in relative terms and requires clarification.

6.6.1 Bias Current Accounting

The hand calculation summed bias currents across all stages based on initial device sizing, yielding a total current draw of 4.87 mA from the 1 V supply. However, during noise optimization, several stages were re-biased to lower currents to reduce thermal noise while maintaining adequate transconductance through increased device widths. These adjustments were made iteratively during simulation and were not back-annotated into the hand calculation table.

6.6.2 Current Sharing Through Mirrors

More significantly, the hand calculation counted each stage independently without accounting for current mirror configurations that enable multiple circuit branches to share bias currents. In the actual implementation:

- Differential pair stages share tail current sources
- Cascode current mirrors reuse bias currents across multiple stages

- Source follower buffers draw current that also flows through load resistors

The simulation directly measures the total current drawn from the supply terminal, capturing only the net current flow. The measured 1.3754 mA represents the true power consumption, yielding:

$$P_{\text{total}} = 1.0 \text{ V} \times 1.3754 \text{ mA} = 1.38 \text{ mW}$$

This discrepancy highlights the importance of full-circuit simulation for accurate power estimation. Regardless of the accounting differences, the final design consumes only 13.8% of the 10 mW budget, providing substantial margin for process variations and temperature effects.

6.7 Stability and Transient Behavior

Hand calculations did not explicitly predict transient settling time or step response characteristics. Simulation results demonstrate that the TIA responds to pulsed photodiode currents without ringing or oscillation, confirming adequate phase margin. The output follows input transitions cleanly, with no overshoot or undershoot beyond that expected from the bandwidth limitation. This validates the pole-zero placement strategy and indicates that parasitic poles introduced by multi-stage cascading remain well-separated from any potential feedback loop unity-gain frequency.

6.8 Summary of Key Insights

The comparison between hand calculations and simulation results reveals several important lessons:

1. **Component sensitivity:** Trans-impedance gain is highly sensitive to small-signal parameters (g_m, r_o) and load impedances. Deviations of 20–25% in individual stage gains compound multiplicatively, leading to large overall gain variations. This underscores the importance of accurate process characterization and iterative simulation.

2. **Noise-centric optimization:** The integrated noise specification proved to be the tightest constraint, requiring multiple design iterations focused on reducing thermal noise from input devices and resistive loads. These changes—particularly bias current adjustments and device resizing—had cascading effects on gain, bandwidth, and power that were not fully anticipated in the initial hand analysis.

3. **Bandwidth predictability:** The upper bandwidth agreement within 0.13% validates first-order pole analysis for high-frequency performance. However, the 69× error in lower bandwidth prediction demonstrates that AC coupling networks require more careful modeling when multiple cascaded stages are involved.

4. **Power accounting complexity:** Accurate power estimation requires full-circuit simulation to account for current sharing through mirror configurations. Stage-by-stage summation can significantly overestimate consumption in architectures with shared bias networks.

5. **Iterative refinement necessity:** Despite thorough hand analysis, achieving all specifications simultaneously required iterative refinement guided by full transistor-level simulation. The hand calculations provided a valid starting point and correctly identified dominant design trade-offs, but could not capture all second-order effects present in the 45 nm technology.

The final simulated TIA meets all project specifications with adequate margins:

- Trans-impedance: 112.27 dBΩ (8.77 dB margin)
- Upper bandwidth: 300.40 MHz (0.13% margin)
- Lower bandwidth: 9.61 MHz (3.9% margin to 10 MHz limit)
- Integrated noise: 121.3 nA_{rms} (3.0% margin)
- Output swing: 0.60 V_{pp} (50% margin)
- Power: 1.38 mW (86% margin)

The deviations from hand calculations, while substantial in some cases, reflect both the inherent limitations of simplified models and deliberate design choices made during optimization. The successful outcome validates the hierarchical design methodology: process characterization informed hand analysis, which established an initial topology and component values, followed by simulation-driven refinement to address noise and bandwidth constraints within the tight power and voltage budgets imposed by the 45 nm process and 1 V supply.

7 Conclusion

This project successfully demonstrated the complete design flow for a wideband transimpedance amplifier in 45 nm CMOS technology, from process characterization through transistor-level simulation to final performance verification. The implemented TIA meets all specified requirements while operating from a 1 V supply and consuming only 1.38 mW of power—well within the 10 mW budget.

7.1 Achievement of Design Objectives

The final design achieves the following performance, as validated through Cadence Spectre simulations:

Parameter	**Achieved**	**Required**	**Status**
Trans-impedance gain	112.27 dBΩ (406 kΩ)	≥103.5 dBΩ (≥150 kΩ)	Pass (+8.8 dB)
Upper -3dB bandwidth	300.40 MHz	≥300 MHz	Pass (+0.13%)
Lower -3dB bandwidth	9.61 MHz	<10 MHz	Pass (3.9% margin)
Integrated input noise	121.3 nA_{rms}	≤125 nA_{rms}	Pass (3.0% margin)
Output swing (differential)	0.60 V_{pp}	≥0.4 V_{pp}	Pass (+50%)
Power consumption	1.38 mW	<10 mW	Pass (86% margin)

Table 5: Final performance summary against specifications

The design successfully converts photodiode currents of 2.67 μA_{pp} into differential voltage swings exceeding 0.6 V while maintaining signal integrity across a 291 MHz bandwidth. All transistors operate in their intended regions without clipping or distortion, and the amplifier exhibits stable operation with no oscillation or ringing in transient response.

7.2 Architectural Validation

The hierarchical multi-stage architecture—comprising a common-gate input stage, common-source gain stage, source-follower buffers, four cascaded differential amplifiers, and output buffers—proved well-suited to the constraints of the 45 nm process. Several architectural decisions were validated by the final results:

Common-Gate Input Stage The CG configuration successfully achieved low input impedance (approximately $1/g_m \approx 200$–$300\ \Omega$), effectively isolating the photodiode capacitance from bandwidth-limiting effects. The input pole at approximately 6 GHz remains far above the required 300 MHz bandwidth, confirming that the photodiode interface does not constrain system performance. However, the CG stage's inherent noise contribution required careful device sizing and bias current optimization to meet the integrated noise specification.

Differential Amplifier Chain The four-stage differential amplifier cascade with resistive loads provided predictable gain distribution and straightforward bandwidth control. Each stage contributed approximately 9.5 dB of differential gain, accumulating to 38 dB total voltage gain before the output buffer. The resistive loads simplified pole placement analysis compared to active load

alternatives and avoided the area and complexity of inductive peaking techniques. The use of differential signaling also provided excellent common-mode rejection, minimizing sensitivity to supply noise and substrate coupling.

Headroom Management Operating from a 1 V supply imposed strict constraints on voltage headroom. The selected architecture avoided deep transistor stacking, with the CG and source-follower stages using single-device signal paths and the differential pairs requiring only two stacked transistors (input pair plus current source). DC operating point simulations confirmed that all devices maintain adequate V_{DS} for saturation operation while providing sufficient output voltage swing.

7.3 Design Methodology Effectiveness

The project followed a structured methodology that proved essential to achieving the specifications:

Process Characterization Comprehensive extraction of device characteristics—including I_D–V_{DS} curves, threshold voltage trends, transconductance versus bias current, gate capacitances, and unity-gain frequency—provided the foundation for all subsequent design decisions. The characterization revealed important deviations from ideal long-channel behavior, including velocity saturation effects, channel-length modulation, and short-channel threshold voltage dependencies. These process-specific parameters informed realistic hand calculations and device sizing choices.

Hand Analysis The analytical design phase established initial component values, predicted performance metrics, and identified dominant trade-offs. Hand calculations correctly predicted that the upper bandwidth would meet the 300 MHz specification and that the common-gate input noise would dominate the overall noise budget. The predicted trans-impedance gain of 104.2 dBΩ, while 8 dB lower than the final simulated value, provided an adequate starting point that met the minimum 103.5 dBΩ requirement with margin. The hand analysis phase was invaluable for developing design intuition and understanding trade-offs before committing to simulation.

Iterative Simulation-Based Refinement Full transistor-level simulation revealed second-order effects not captured in hand analysis, necessitating iterative refinement. The most significant iterations focused on meeting the integrated noise specification of 125 nA_{rms}. Initial simulations yielded noise levels near 140 nA_{rms}, requiring systematic reductions through increased input transistor widths, optimized bias currents, and careful selection of drain resistances to balance noise contribution against bandwidth requirements. This iterative process, while time-consuming, was essential to achieving all specifications simultaneously within the tight constraints of the 45 nm process.

7.4 Key Technical Insights

Several important insights emerged from the design process:

Noise as the Binding Constraint Among all specifications, the integrated input-referred noise of 125 nA_{rms} proved most challenging to satisfy. The final design achieves 121.3 nA_{rms} with only 3.0% margin, indicating this specification limited further optimization opportunities. Noise reduction efforts—including device width increases and bias current adjustments—had cascading effects

on gain, bandwidth, and power consumption, underscoring the tight coupling between these parameters in wideband amplifier design.

Multiplicative Gain Accumulation Small deviations in individual stage gains compound multiplicatively in multi-stage architectures. A 15–20% increase in single-stage differential gain, when cascaded across four stages, yields a 2× increase in overall transimpedance. This sensitivity necessitates accurate modeling of load impedances, transconductance values, and parasitic effects to predict system-level performance reliably.

AC Coupling Complexity The large discrepancy between predicted (0.14 MHz) and simulated (9.61 MHz) lower bandwidth frequencies highlights the difficulty of accurately modeling AC coupling networks in multi-stage systems. Cascaded high-pass filters, parallel loading from bias networks, and finite source follower output impedances all contribute to raising the lower corner frequency above single-stage predictions. Future designs would benefit from more detailed SPICE-level analysis of bias and coupling networks during the hand calculation phase.

Power Efficiency Through Current Sharing The dramatic difference between predicted (4.87 mW) and measured (1.38 mW) power consumption demonstrates the efficiency gains achievable through current mirror configurations that enable multiple circuit branches to share bias currents. This 3.5× reduction in power consumption was not apparent from stage-by-stage hand analysis, emphasizing the value of full-circuit simulation for accurate power estimation.

7.5 Limitations and Future Improvements

While the design meets all specifications, several limitations and potential improvements should be noted:

Tight Noise Margin The 3.0% margin on integrated noise leaves little room for process variations or temperature effects. Monte Carlo analysis would be valuable to assess yield and identify whether additional design margin is necessary for robust production. Corner simulations across fast-fast, slow-slow, and typical-typical process corners would similarly validate performance across the full parameter space.

Layout Parasitics All simulations were performed at the schematic level without layout extraction. Parasitic capacitances, resistances, and inductances introduced by metal interconnect routing will degrade performance, particularly the upper bandwidth and noise characteristics. Post-layout simulation would reveal these effects and likely necessitate component value adjustments to restore target performance.

Input Capacitance Sensitivity The design assumes a fixed 100 fF photodiode capacitance. Variations in photodiode technology or packaging parasitics would shift the input pole frequency and potentially affect bandwidth. A more robust design might include tunable compensation or accept a wider range of input capacitances.

Single-Supply Constraint The 1 V single-supply operation, while representative of modern low-power CMOS processes, limits output swing and complicates biasing. A dual-supply implementation could provide additional headroom for increased linearity and relaxed transistor saturation requirements, though at the cost of additional supply complexity.

7.6 Broader Context and Applications

The designed TIA represents a front-end suitable for a variety of optical receiver applications:

Short-Reach Optical Links With 300 MHz bandwidth and moderate gain, this TIA is well-suited to short-reach fiber-optic communication links operating at data rates up to several hundred Mb/s. Applications include rack-to-rack interconnects in data centers, local area networks, and chip-to-chip optical links in high-performance computing systems.

Sensor Interfaces The low power consumption (1.38 mW) makes this design appropriate for battery-powered optical sensing applications, including LiDAR systems, optical time-of-flight ranging, and ambient light detection. The wide bandwidth supports fast pulse detection, while the differential architecture provides noise immunity in electrically harsh environments.

Instrumentation The high transimpedance gain (406 kΩ) enables detection of small photocurrents from photodiodes in spectroscopy, fluorescence detection, and other analytical instrumentation. The low integrated noise (121.3 nA_{rms}) preserves signal-to-noise ratio for weak optical signals.

7.7 Lessons Learned

This project reinforced several fundamental principles of analog integrated circuit design:

1. **Process characterization is foundational**: Accurate device models are essential for meaningful hand calculations and simulation convergence. Time invested in thorough characterization pays dividends throughout the design process.

2. **Hand analysis remains valuable**: Despite the availability of powerful simulation tools, analytical design provides intuition, identifies trade-offs, and enables rapid exploration of the design space. Hand calculations should not be skipped even when simulation resources are abundant.

3. **Specifications drive architecture**: The tight noise specification dictated many architectural choices, including the selection of a common-gate input stage and the extensive device sizing required to minimize thermal noise. Understanding which specifications are binding early in the design process focuses effort on the most critical aspects.

4. **Iteration is inevitable**: No first-pass design meets all specifications. Expecting and planning for iterative refinement—with clear metrics for evaluating progress—leads to more efficient convergence on a final solution.

5. **Margin matters**: Tight margins on critical specifications (like the 3.0% noise margin achieved here) increase sensitivity to non-idealities and reduce robustness. Where possible, trading other resources (area, power, bandwidth) to increase margin on the tightest constraint improves manufacturability and yield.

7.8 Final Remarks

The successful completion of this wideband transimpedance amplifier design demonstrates mastery of the complete analog IC design flow, from process characterization and analytical modeling through circuit synthesis and simulation-based verification. The final implementation achieves all

specified performance targets in a power-efficient architecture compatible with modern nanoscale CMOS technology.

The design process highlighted the critical importance of noise optimization in high-speed photodiode front-ends and validated the effectiveness of hierarchical multi-stage architectures for distributing gain while managing bandwidth and linearity constraints. The experience gained through iterative simulation-driven refinement and the insights developed regarding parameter sensitivities and trade-offs will inform future analog design efforts.

Most significantly, this project illustrated that despite the availability of advanced process technologies and sophisticated simulation tools, fundamental analog design principles—small-signal analysis, pole-zero placement, noise modeling, and systematic optimization—remain essential to achieving high-performance circuit implementations. The combination of analytical insight and simulation-based validation proved indispensable to navigating the complex, coupled design space and delivering a functional transimpedance amplifier that meets the demanding specifications of modern optical receiver systems.

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