Design Verification Of Nand Flash Memory Controller of Lattice semiconductor corporation

Members -

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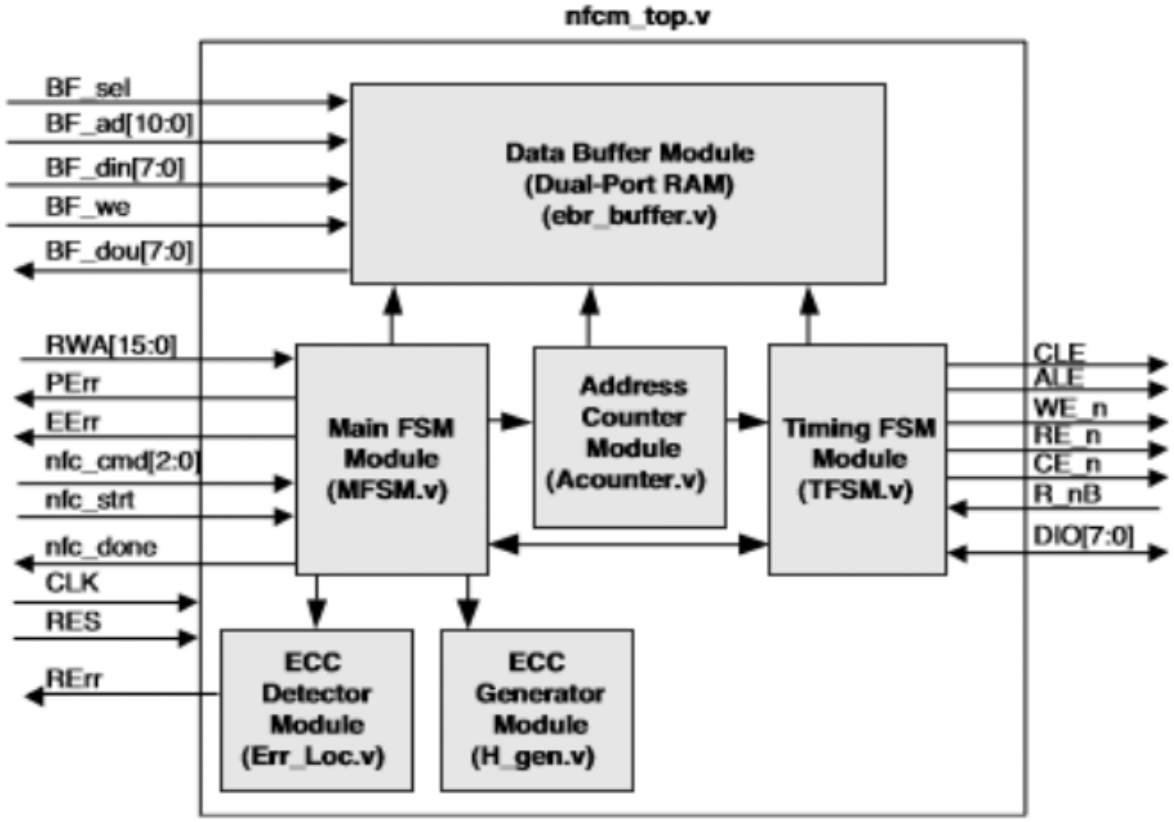
Design diagram with specifications

RTL Implementation



- Data Buffer Module—This Module is implemented as Dual Port RAM which facilitates storing of data when the host writes data into the Flash and Reads data from the Flash.

- Main FSM-This FSM works together with timing FSM where the module interprets command from the host and passes control signals to the timing FSM which creates all the necessary controls for NAND flash to execute the repeated task with strict timing requirements.

- Address Counter Module-Generates Address control signals required for the data buffer module based state machine in the main FSM.
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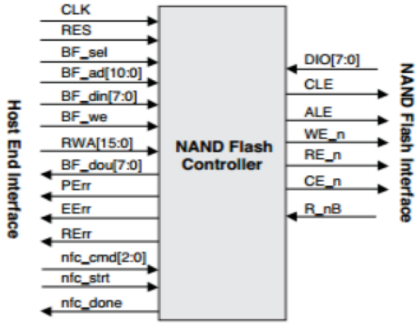
- ECC Generator Module-Generates Error correction code during program operation and stores the ECC code in Flash memory.
- ECC Detector Module-Makes use of this ECC code in Flash memory to detect errors in the data during host read operation.

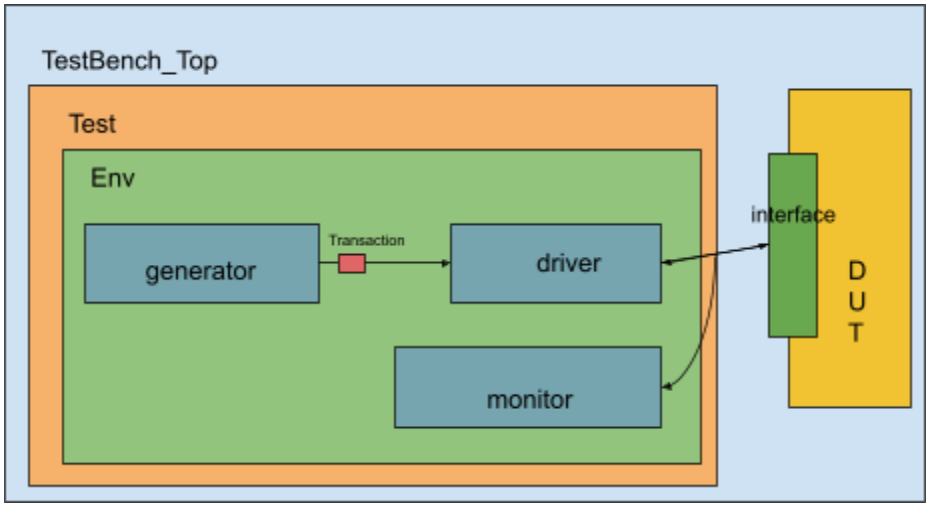
Signal Name	Signal Direction	Active State	Definition
Host End interface			
CLK	Input	N/A	Clock signal.
RES	Input	High	Reset signal.
BF_sel	Input	High	Dual-port RAM clock enable signal.
BF_ad[10:0]	Input	N/A	Dual-port RAM address signal.
BF_din[7:0]	Input	N/A	These lines are used to pass data to the dual-port RAM.
BF_we	Input	High	Dual-port RAM write signal.
RWA[15:0]	Input	N/A	These address signals are used by the Flash device.
BF_dou[7:0]	Output	N/A	These lines are used to pass data to host.
PErr	Output	High	Page program operation error signal.
EErr	Output	High	Block erase operation error signal.
RErr	Output	High	Page read operation error signal.
nfc_cmd[2:0]	Input	N/A	Command code signal.
nfc_strt	Input	High	When asserted, indicates the host initiates a operation.
nfc_done	Output	High	When asserted, indicates an operation is done.
NAND Flash Interface			
DIO[7:0]	In/Out	N/A	I/O pins used to send commands, address, and data to the Flash, and receive data during read operations.
CLE	Output	High	Command Latch Enable.
ALE	Output	High	Address Latch Enable.
WE_n	Output	Low	Write Enable.
RE_n	Output	Low	Read Enable.
CE_n	Output	Low	Chip Enable.
R_nB	Input	N/A	When this signal is high, the Flash is ready for the next operation. When it is low, an internal operation is in progress.



Basic Operations -

- Reset
- Read ID
- Program page(copy content of data buffer into Flash Memory)
- Read page(content of Flash page is copied into the data buffer)

Verification Methodology



Basic Tests -

- Performed type_id, Read page , program page , reset.

- Data to be written, block and page address were generated randomly.

Stress test

- Consecutive writes to flash memory at consecutive pages followed by consecutive reads .

- Consecutive writes at random addresses followed by reads.

- Check for the design behavior with system reset and read/write command operation applied simultaneously.
- Check for the design behavior with a read followed by write operation with the same address.

- Check for the design behavior with a write followed by read with the same address.
- Check for 5 successive read operations with the same address.
- Check for 5 successive read operations with different addresses.
- Check for 3 successive write operations with the same address.
- Check for 3 successive write operations with different addresses.
- Check for read and write operation with invalid address.
- Check for read ID operation if it is reading the correct ID of the device.
- Check for the read/write operation followed by erase operation.
- Check for the response of the design by driving the command port without driving the start signal.
- Check if the design raises any error flag if any erroneous data is received while read operation.
- (Raise a flag).
- Check for the signal protocol from the memory controller:
- Check for the nfc_done signal when the intended operation is done from memory stub.
- Check for the valid address and command generated by the memory controller as per the specification.

Results Achieved:

- Achieved 96% coverage on the design under test which indicates that most of our test cases have been exercised.

- Verified the design completely and found the design to be bug free and the design is now ready for tape out