BEEE assignment 5.

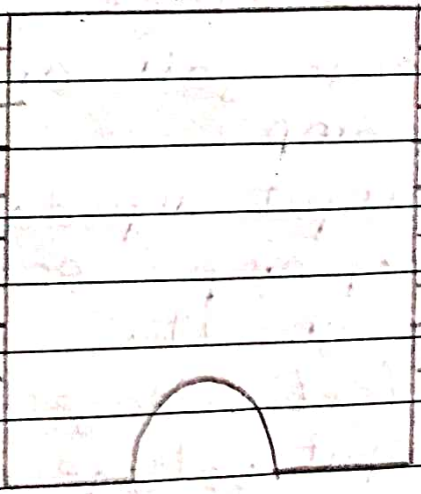
Name - Neet Kaushik His No - 612410080 Div-I Batch-B

Q1 An op-Amp is a high gain DC coupled voltage amplifier with differential inputs and a single output. It is a versatile analog circuit building block used in a wide arrgay of applications

Applications.

1) Amplifiers: Used for both voltage and current amplification
2) Filters: Used in various types of filters.
3) Comparators: Used as a comparator to compare two input voltages.
4) oscillators: Can be used to build oscillators.

2. Pin Diagram of Op-Amp.



Function

1) Pin 4 and Pin 7 are the negative and positive voltage power supply terminals The power which is required for the IC to function is received from these pins
2) Output pin 6. , the output which is delivered from opamp is received from this pin.
3) Input pins 2 and 3.
Pin 3 is considered as the inverting input. and Pin 2 is the non inverting pin. Provides the input.
4) ~~out~~ offset Null pins 1 and 5
Even slight variation in input voltages (Both at Inverting, non inverting) can show an impact on the output. In order to overcome this p offset value of voltage are applied to these pins.

The characteristics ~~are~~ of ideal op-amp is.
1) Infinite voltage gain: It is the differential open loop gain and is infinite for an ideal opamp
2). Infinite input impedance: It is infinite for an ideal op amp ensuring that no current flows Through it.
3) zero offset voltage: The presence of small output voltage though $V_1 = V_2 = 0$ is called offset voltage. It is zero for an ideal op-amp

4) Zero output impedance: This ensures that output voltage of op-amp remains the same.

It is essential for ~~sev~~ several reasons.

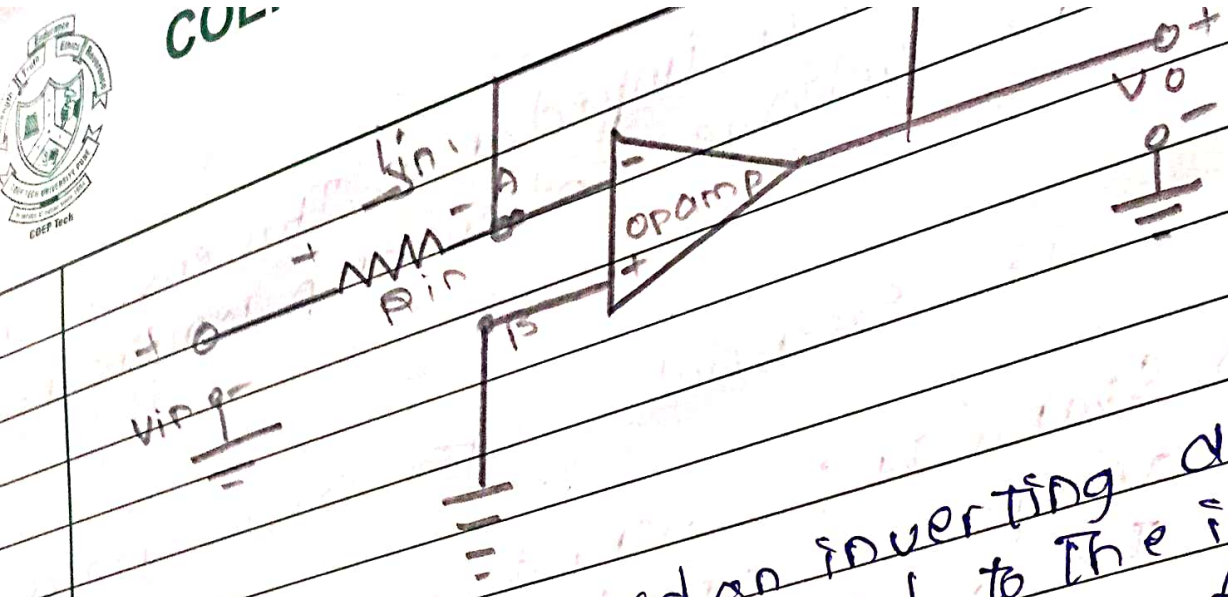
1) Stability: without negative feedback. an op amp can oscillate causing unstable output. Also reduces distortion in output signal)

2) Control
i) Negative feedback allows for precise control over the op amps gain, making it easier to design.
ii) Also increases the input impedance.

3) Common applications.

1) Inverting Amplifier: use negative feedback to invert and amplify the input signal
2) Non inverting: used to amplify input without inverting it.
3) Voltage follower: to provide a buffered output ~~to~~ of input signal.

Op-amp as an ~~non negative~~ inverting amplifier.



Op-amp can be used an inverting amplifier by connecting input signal to the inverting input and applying a negative feedback to the non inverting input.

Derivation of gain ie: V_o/V_{in}.

As node B is grounded, node A is also at ground potential, $\therefore V_A = 0$.

$$I = \frac{V_{in} - V_A}{R_1} \Rightarrow I = \frac{V_{in}}{R_1} \quad \text{①}$$

Now from output side, considering direction of I we can write

$$I = \frac{V_A - V_o}{R_f}$$

$$I = \frac{-V_o}{R_f} \quad \text{②}$$

From ① and ②

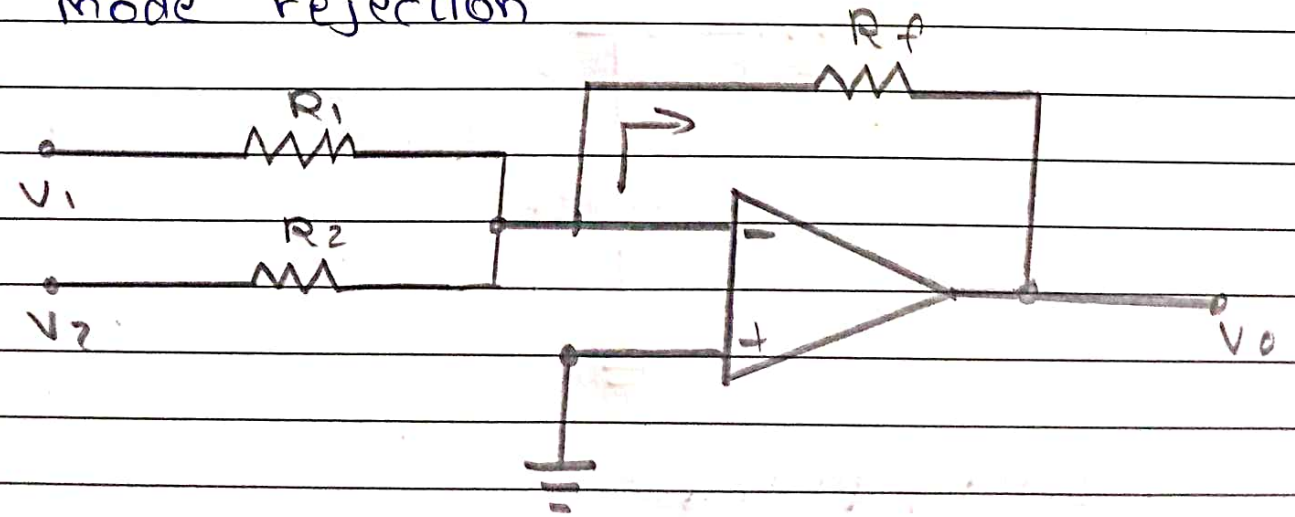
$$\frac{V_{in}}{R_1} = \frac{-V_o}{R_f}$$

$$\Rightarrow \frac{V_o}{V_{in}} = -\frac{R_f}{R_1}$$

$$\text{Gain} = -\frac{R_f}{R_1}$$

The following are uses of an op amp as a non inverting amplifier

1) Buffer amplifiers: To isolate circuits and drive low-impedance loads without significant loss.
2) High impedance Input stages:- In systems where high input impedance is essential to avoid loading effects.
3) Audio amplifiers:: For preamplifiers where ~~input impedance~~ phase preservation is important.
4) Active filters.: Part where the high input impedance minimizes loading effects on passive components
5) Instrumentation amplifiers: To amplify differential signals with high common mode rejection

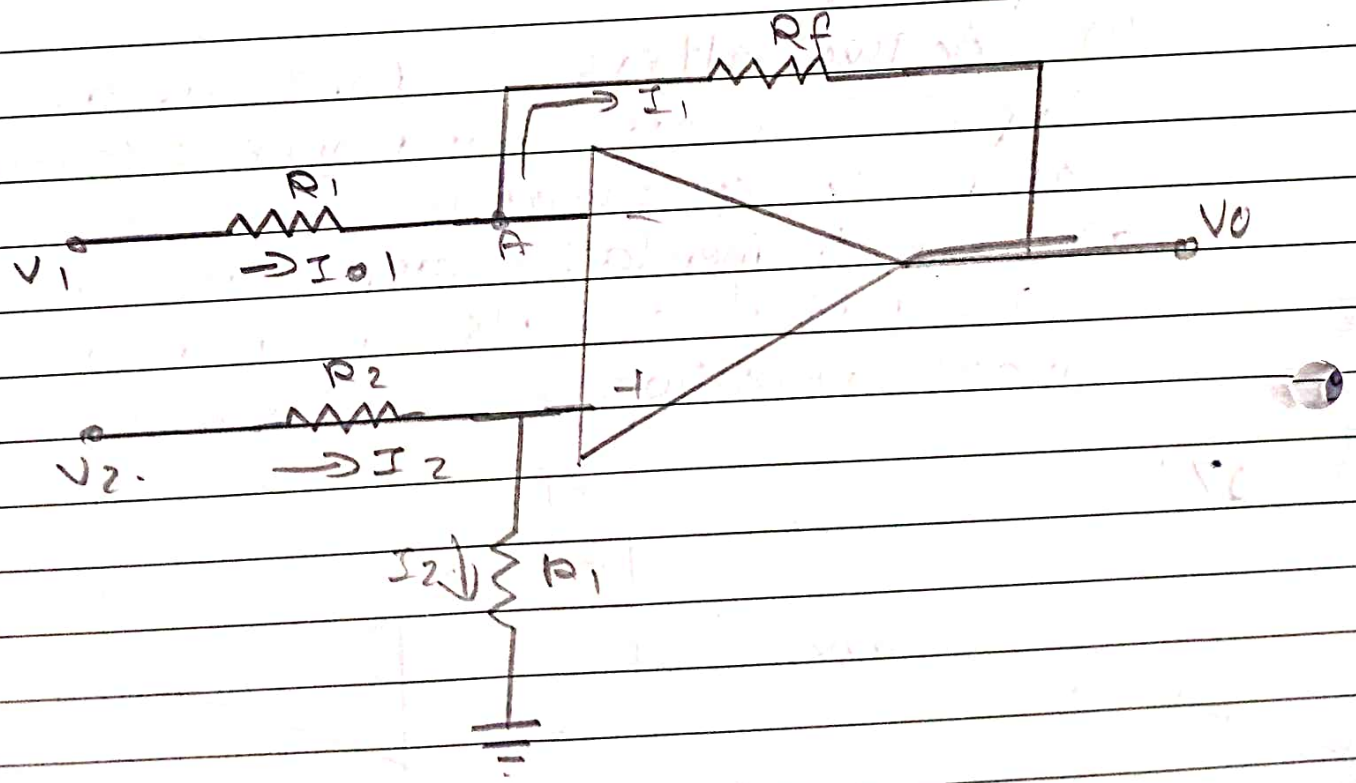


working

> Multiple inputs: The circuit has multiple input voltages (V_1, V_2, V_3 ... etc) connected to inverting / non inverting input through their respective resistors.

2) virtual ground: Due to high gain and negative feedback, the inverting input of op-amp is held at virtual ground. Same potential as non inverting input
3) Current flow: Each source contributes a current to the input
4) Output voltage: This is determined by total current flowing through the feedback resistor and its resistance value.

Difference amplifier.



working principle.

1. differential input: Two voltages input v_1 and v_2, applied to the inverting and non inverting input of op-amp

2) Virtual ground : Due to ~~hai~~ high gain and negative feedback, inverting pain is held at virtual ground.

3) Current flow: Input voltages create currents flowing through the input resistors. These currents are amplified by op-amp

4) Output voltage: The output voltage is proportional to the difference between the input voltages.

$$V_{out} = \frac{R_2}{R_1} \times (V_2 - V_1)$$

29 Given.

Inverting amplifier circuit.

$R_f = 80k\Omega$, $R_i = 16k\Omega$.

$V_{in} \Rightarrow$ i) 0.4 V, ii) 2 V, iii) 3.5 V, iv) -0.6V, v) ~~-2.4V~~ -1.6 vi) -2.4 V

Formula.

$$\frac{V_o}{V_{in}} = -\frac{R_f}{R_1}$$

i) $\frac{V_o}{0.4} = \frac{-80 \times 10^3}{16 \times 10^3}$ $V_o \Rightarrow -2V$.

ii) $\frac{V_o}{2} = \frac{-80 \times 10^3}{16 \times 10^3} V_o \Rightarrow -10V$.

iii) $\frac{V_o}{3.5} = \frac{-80 \times 10^3 V_o}{16 \times 10^3} \Rightarrow V_o = -17.5V$

iv) $\frac{V_o}{-0.6} = \frac{-80 \times 10^3}{16 \times 10^3} \Rightarrow V_o = +3V$.

v) $\frac{V}{-1.6} = \frac{-80\times10^3}{16\times10^3} = +80\,V$

vi) $\frac{V}{-2.4} = \frac{-80\times10^3}{16\times10^3} = +12\,V$

Given

Inverting summer amplifier circuit.

$V_1 = 0.1\,V$, $V_2 = 0.25\,V$, $V_3 = 0.5\,V$

$R_f = 250\,k\Omega$, $R_1 = 5\,k\Omega$, $R_2 = 25\,k\Omega$.

$R_3 = 50\,k\Omega$.

To find V_o.

Formula.

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

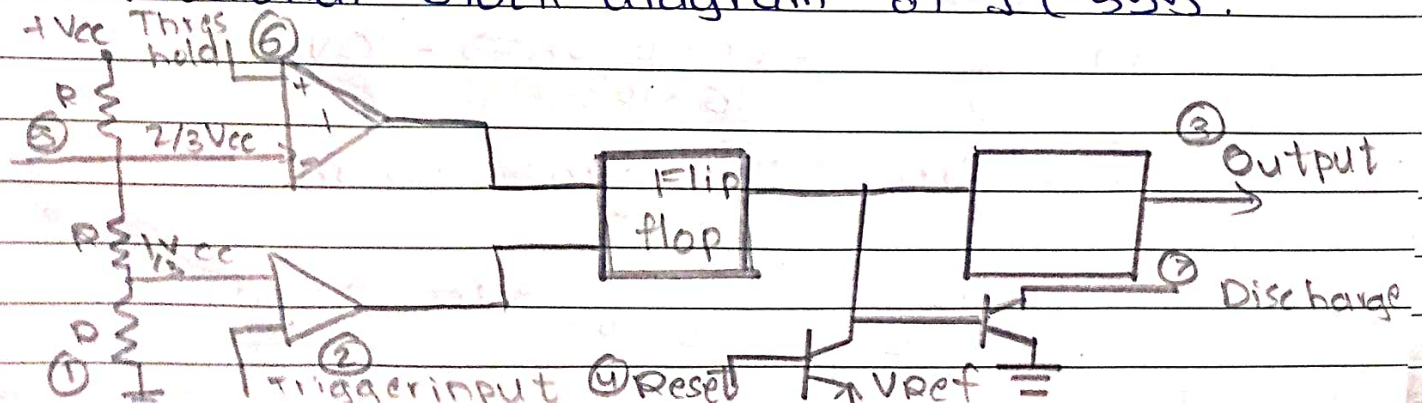
$$\Rightarrow V_o = -\left(\frac{250\times10^3}{5\times10^3}\times 0.1 + \frac{250\times10^3}{25\times10^3}\times 0.25 + \frac{250\times10^3}{50\times10^3}\times 0.5\right)$$

$$\Rightarrow V_o = -(50\times0.1 + 10\times0.25 + 5\times0.5)$$

$$V_o = -(5 + 2.5 + 2.5)\,V$$

$$V_o = -10\,V.$$

Functional block diagram of IC555.

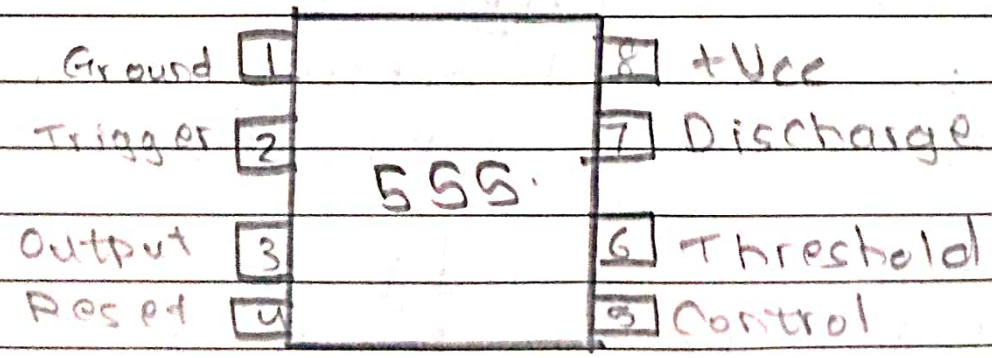


As d shown in block diagram, a 555 timer consists of two comparators, an RS flip flop, two transistors and a resistive network.

Resistive network acts as a voltage divider, comparator 1 compares threshold voltage with $+2/3\ V_{cc}$ volt reference, comparator 2 compares trigger voltage with $+1/3\ V_{cc}$ reference voltage. output of both comparators is given to flip flop, it assumes its state as per the output of comparators one of the transistor is discharge transistor connected to pin 7. This saturates according to output state of flip flop

Base of another transistor is connected to a Reset terminal. A pulse applied to this terminal resets the whole timer irrespect -ive of any input.

912 Pin diagram of IC 555 timer.



Functions of all pins.

Pin 1 (Ground).
- Provides the ground reference for circuit

Pin 2 (Trigger)
- Detects voltage below of 1/3 Vcc (supply voltage) to trigger the timer and start the timer

Pin 3 (Output)
- Delivers the output signal, which can be either high (close to Vcc) or low (close to ground) depending on timers mode of operation.

Pin 4 (Reset).
To reset the timer a negative pulse is applied to this pin, which resets the timer irrespective of input.

~~for~~ Pin 5 (Control).
Allows external control of threshold voltage, affecting the timing of output pulses

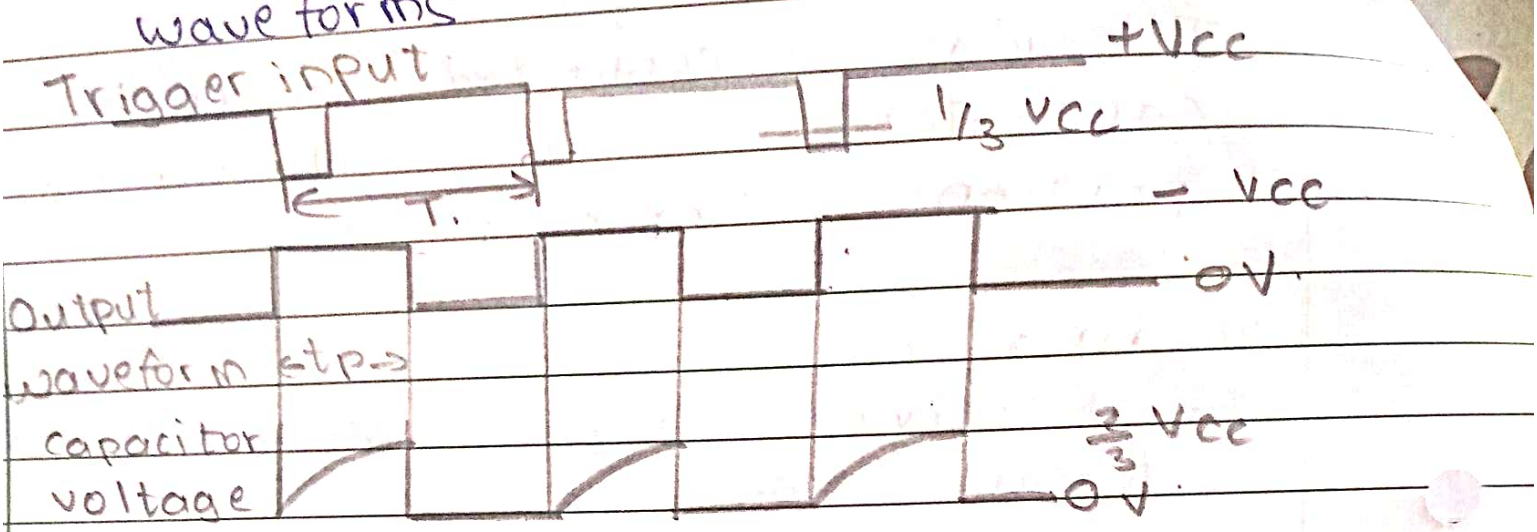
Pin 6 (Threshold).
When the voltage at this pin exceeds 2/3Vcc, the output transitions to ~~to~~ low state.

7) Pin 7 (Discharge)
The pin is connected to the timing capacitor to discharge it during the low portion of the output cycle.

8) Pin 8 (Vcc).
- Receives the positive supply voltage for the IC.

Monostable operation.
1) Initially when the output at pin 3 is low The circuit is in stable state, the transistor is on and the capacitor C is shorted to ground.
2) when negative pulse is applied to pin 2, the trigger input falls below 1/3 Vcc the output of comparator goes high which resets the flip-flop and consequently turns the transistor off.
3) This is the transition from stable to quasi stable state., as discharge transistor is cutoff, the capacitor C begins charging towards +Vcc through resistance RA, with a time constant equal to RAC.
4) when the increasing capacitor voltage becomes slightly greater than +2/3 Vcc, the output of comparator 1 goes high. which sets the flip flop.
Thus output returns to stable state from quasi stable state.

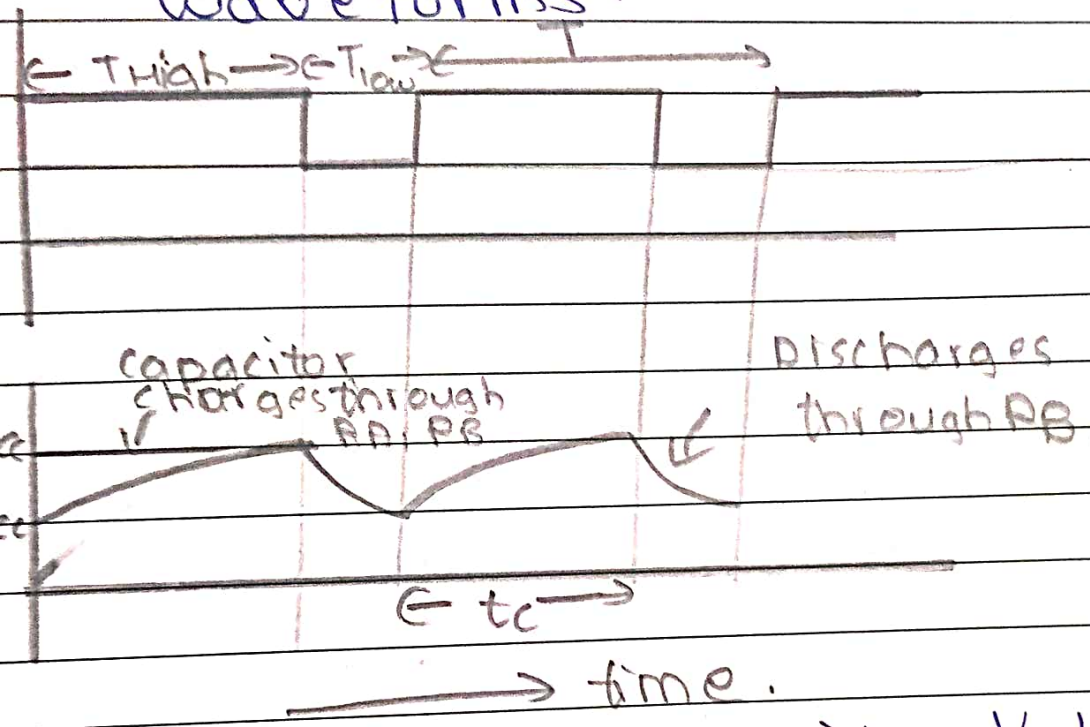
Wave forms



~~Ab~~ Astable Operation.

1) When Vout is high, the discharging transistor is cutoff and capacitor begins charging toward V_{cc} through resistance R_A and R_B., charging time constant is $(R_A + R_B)C$.
2) Eventually, the threshold voltage exceeds $+\frac{2}{3}V_{cc}$, the comparator 1 has high output and triggers flip flop so that timer output is low
3) The discharge transistor saturates and pin 7 grounds so ~~through~~ that capacitor discharges through resistance R_B
4) With discharging of capacitor, trigger inpute of comparator 2, decreases. when its below $\frac{1}{3}V_{cc}$, the output of comparator 2 goes high and this resets the flip flop so that timer output is high.

waveforms.



Output and Capacitor Voltage waveforms.