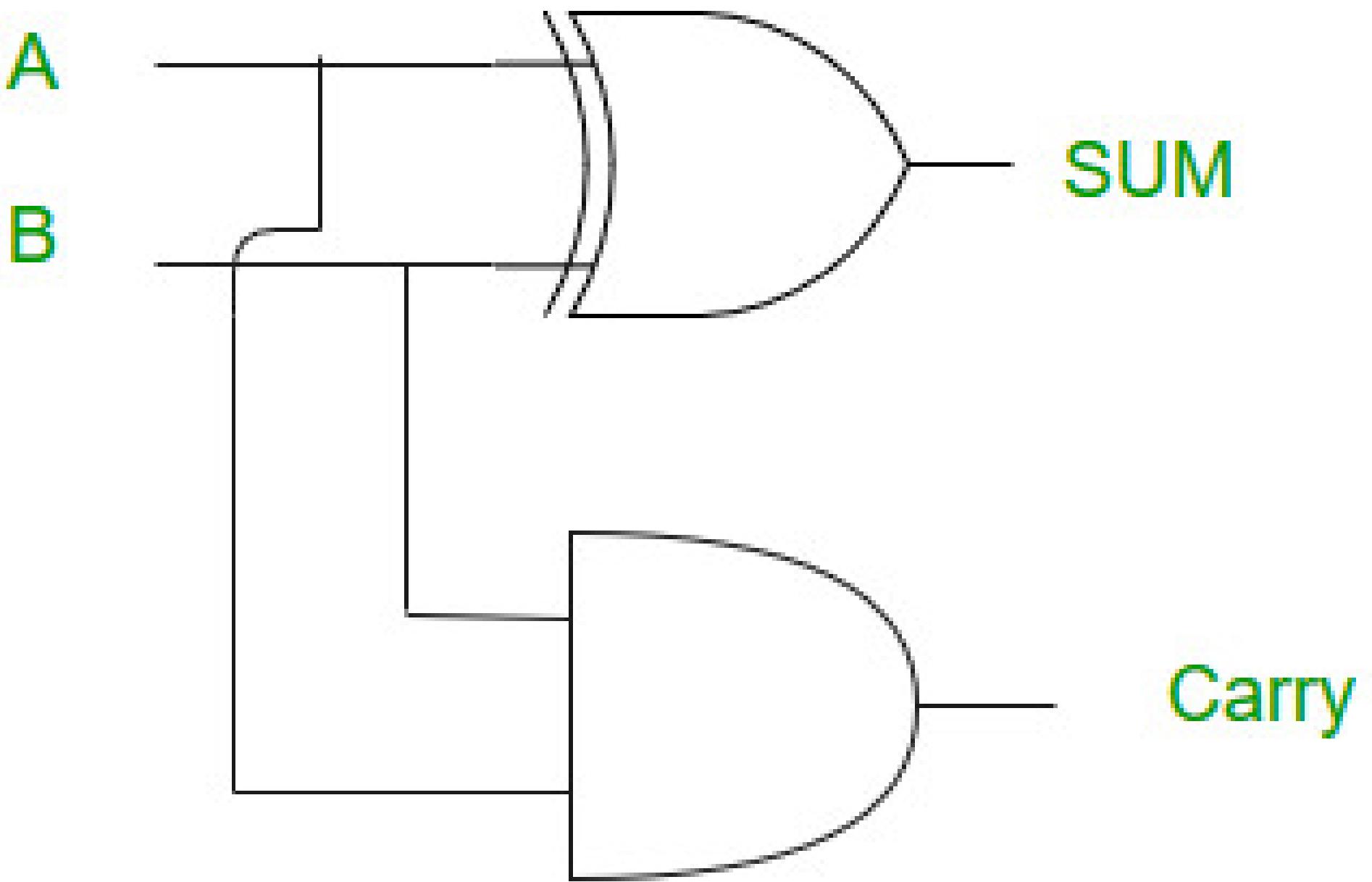


A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

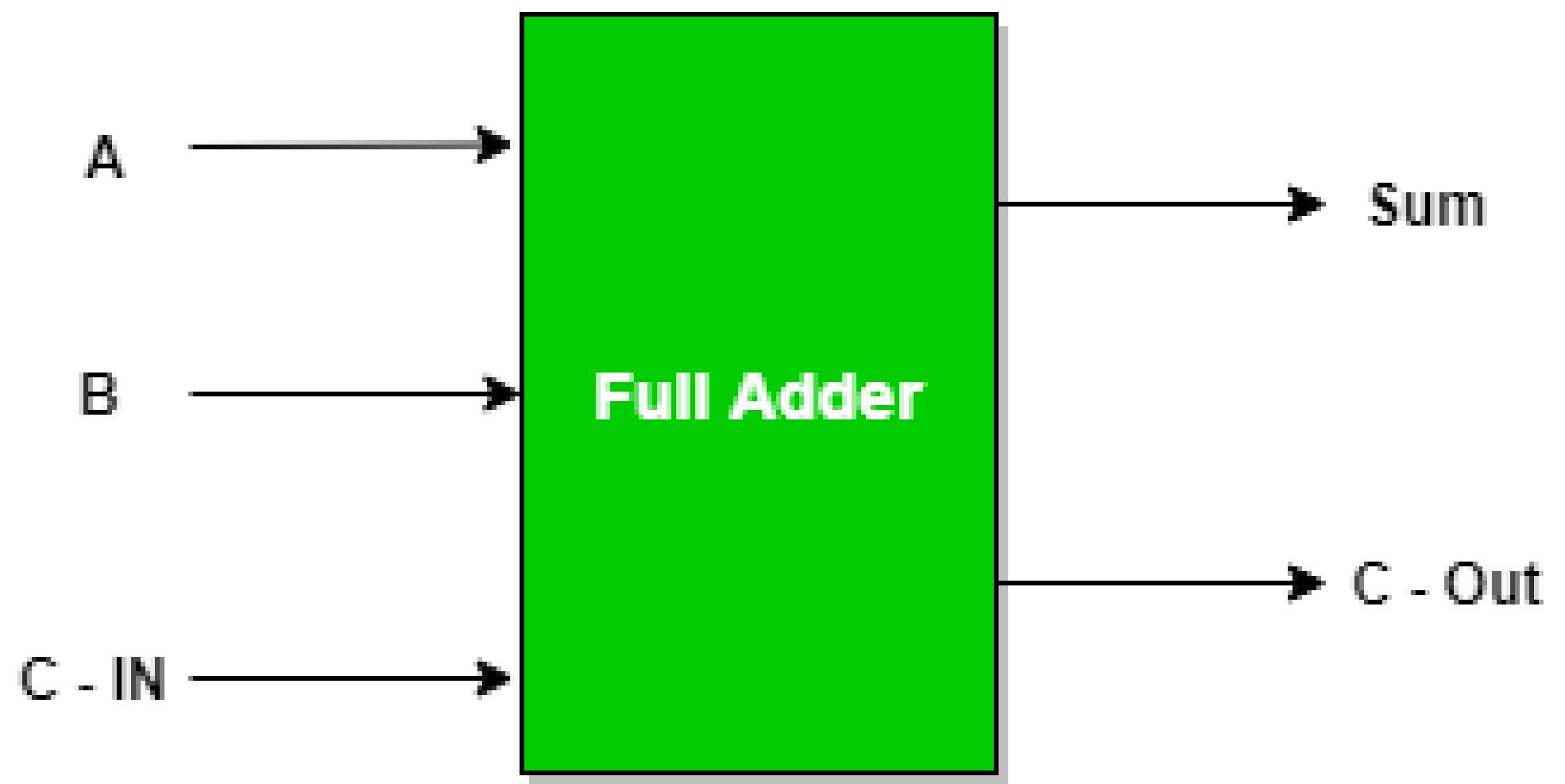
$$\text{Sum} = A \text{ XOR } B$$

$$\text{Carry} = A \text{ AND } B$$



half adder

full adder

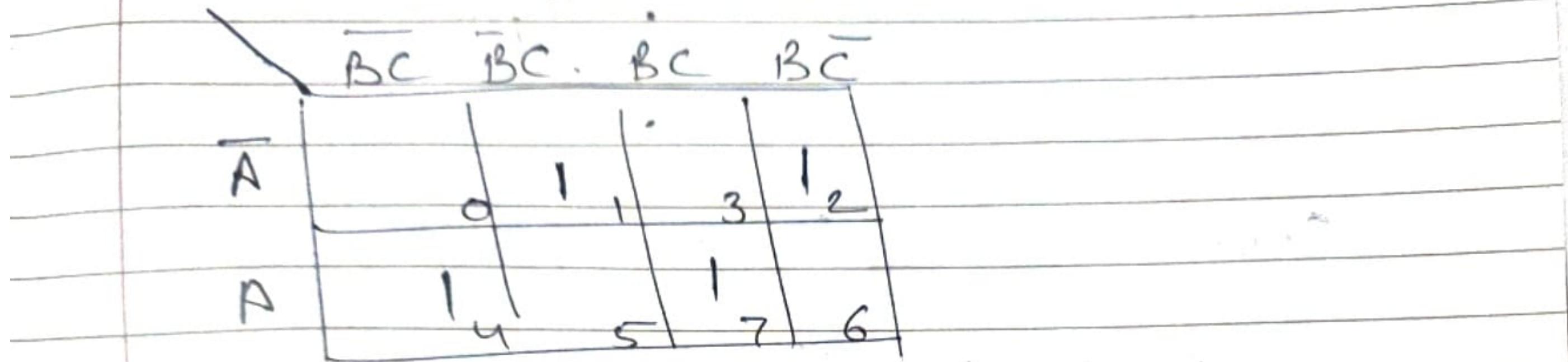


Logical Expression for SUM: =(1,2,4,7)

$$1+1+1 = \underbrace{1}_{10}$$

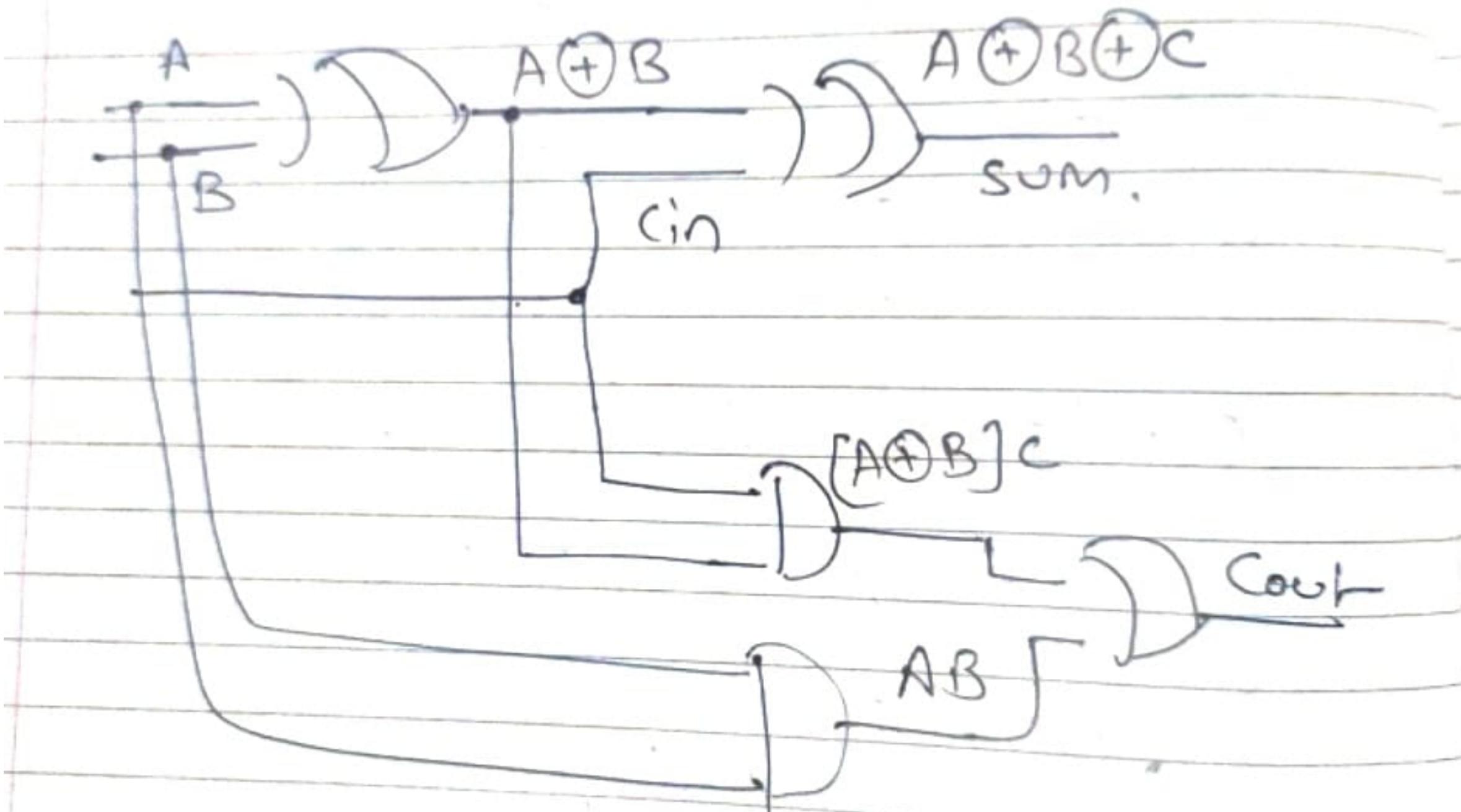
Logical Expression for C-OUT: =(3,5,6,7)

Inputs			Outputs	
A	B	C-IN	Sum	C-Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



$$\begin{aligned}
 \text{Sum} &= \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}C + AB\overline{C} \\
 &= A \oplus B \oplus C.
 \end{aligned}$$

$$\begin{aligned}
 \text{Note: } A \oplus B \oplus C &= (A'B + AB')C' + (A'B + AB')C \\
 &= A'B'C' + AB'C' + (\cancel{A'B})(A+B')(A'+B)C \\
 &= A'B'C' + AB'C' + [AA'C + A'BC + A'B'C + BB'C]
 \end{aligned}$$



$$c_{out} = \Sigma(3, 5, 6, 7)$$

	$\bar{B}c$	$\bar{B}c$	Bc	$B\bar{C}$
\bar{A}	0	1	$\frac{1}{3}$	2
A	1	1	1	1
	Carry = $Bc + A\bar{c} +$			

$$\text{carry out} = AB + BC + CA = AB + \underline{(A \oplus B)C}$$

$$AB + (A \oplus B)C = AB + [AB' + A'B]C$$

$$= AB + [AB'C + A'BC]$$

$$= AB + AB'C + A'BC$$

$$= A[B + B'C] + A'BC$$

$$= A[(B + B')(B + C)] + A'BC$$

$$= A(B + C) + A'BC$$

$$= AB + AC + A'BC$$

$$= AB + [A + A'B]C$$

$$= AB + [(A + A')(A + B)]C$$

$$= AB + (A + B)C$$

$$= AB + AC + CA$$

$$\text{Carry} = [A \oplus B]C + AB$$

$$[A \oplus B]C + AB = A'B'C + \underline{\underline{AB'C + AB}}$$

$$= A'B'C + A[B + B'C]$$

↓

$$= \text{---} A \left[\underbrace{(B + B')}_{\text{Distributive law}} (B + C) \right]$$

$$= A'B'C + A[B + C]$$

$$= A'B'C + \underline{\underline{AB + AC}}$$

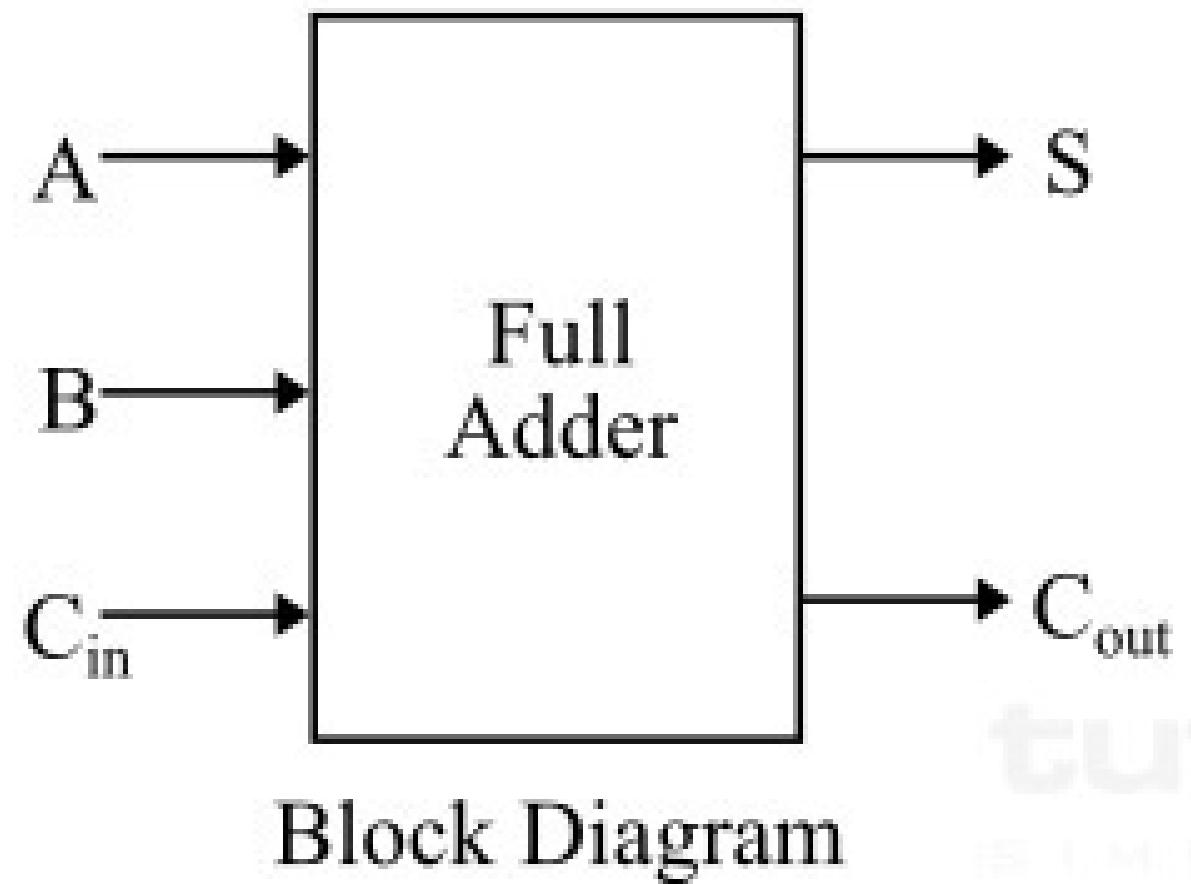
$$= B[A + A'C] + AC$$

$$= B[(A + A')(A + C)] + AC$$

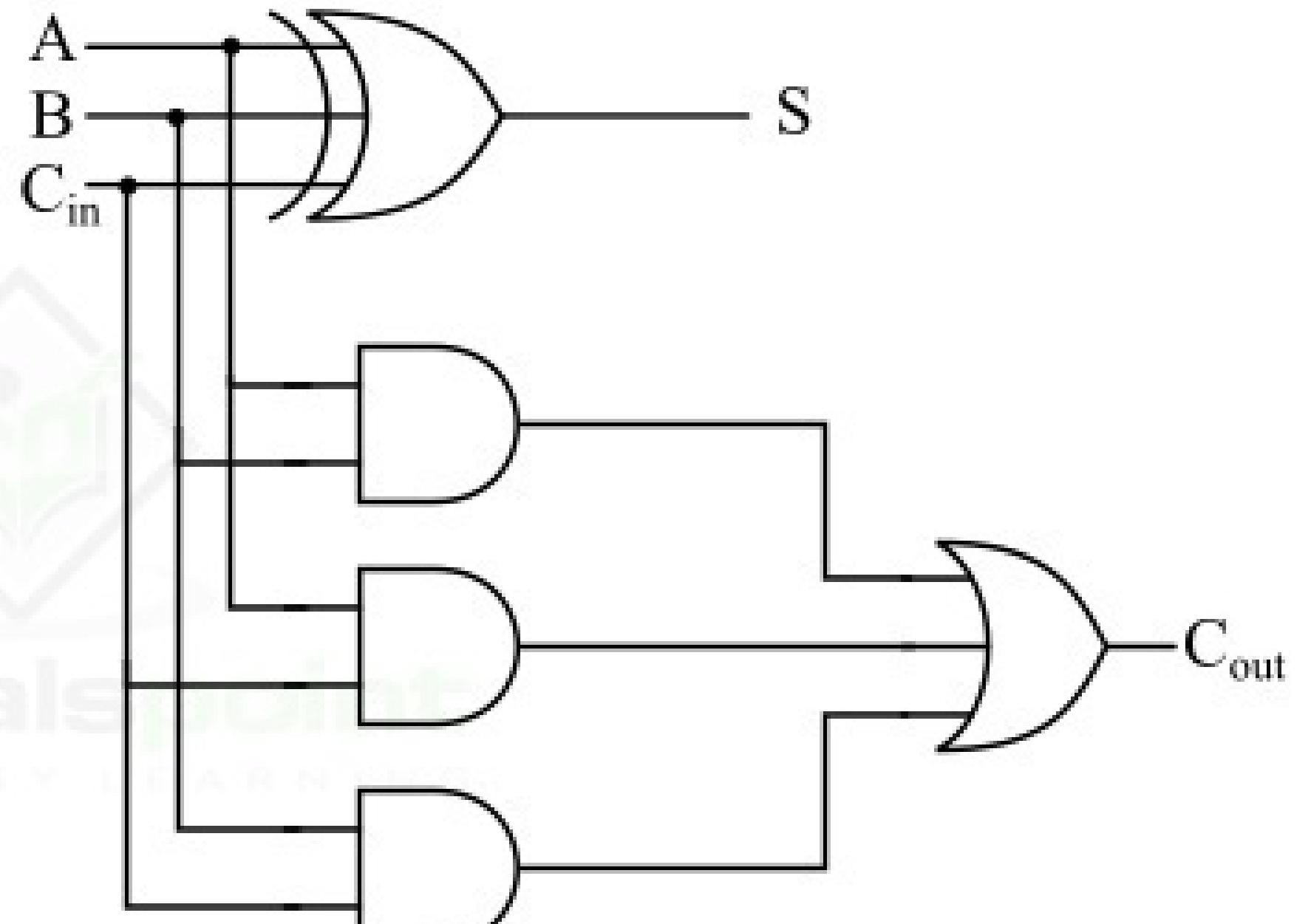
$$= B[A + C] + AC$$

$$= AB + BC + AC \quad \checkmark$$

$$[A \oplus B]C + AB = AB + BC + AC$$



Block Diagram



Circuit Diagram

Figure 2 - Full Adder

$$\text{cout} = AB + BC + CA$$

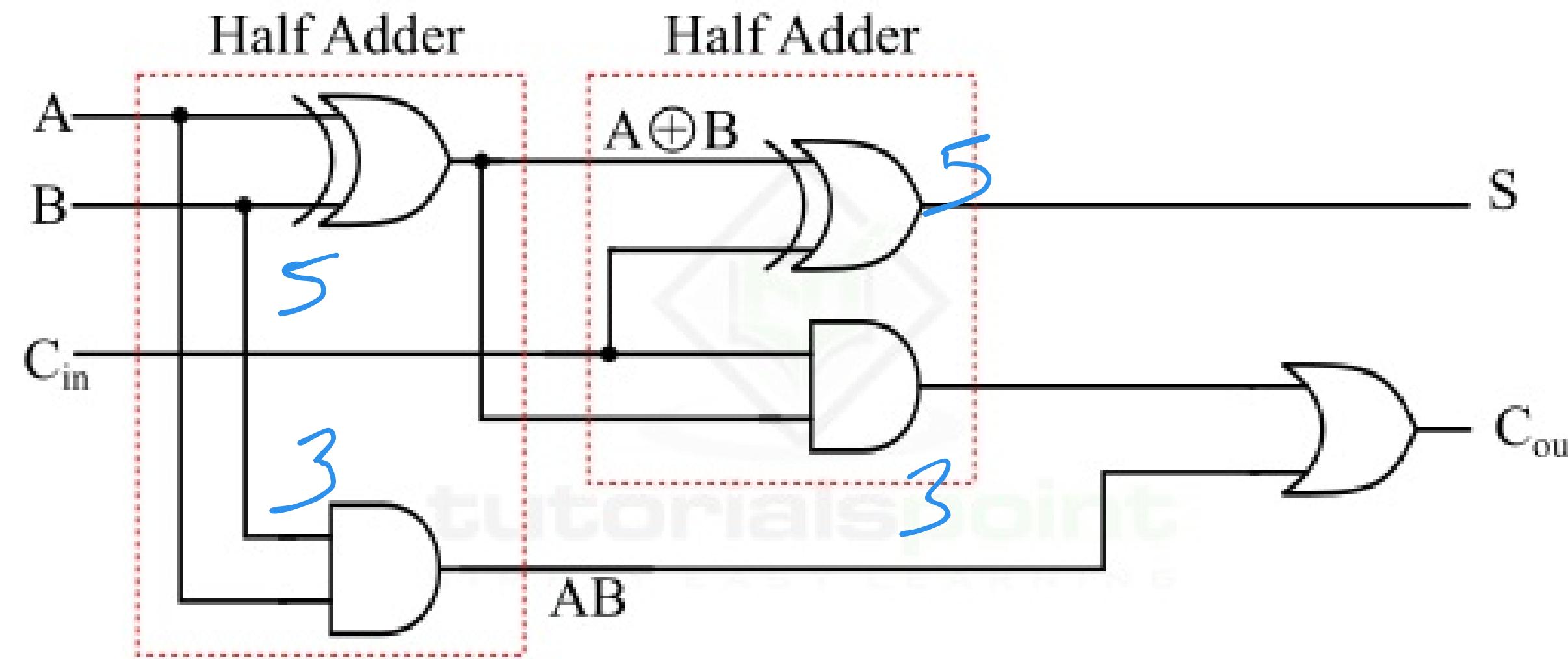
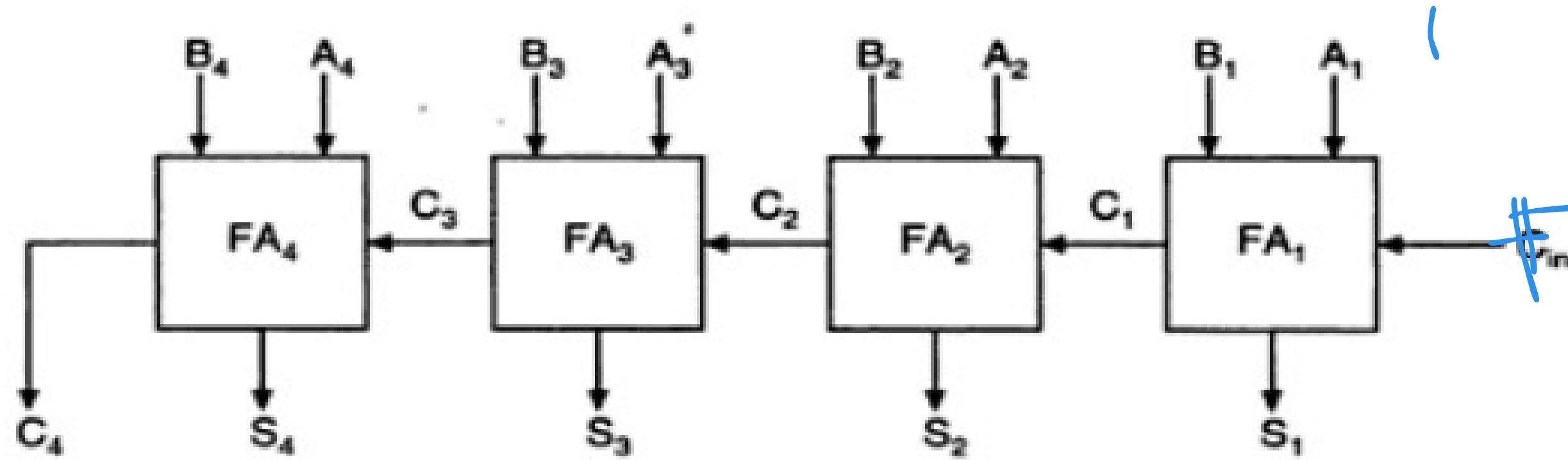


Figure 3 - Logic Diagram of Full Adder using Half Adder

$$C_{out} = (A \oplus B)C + AB$$

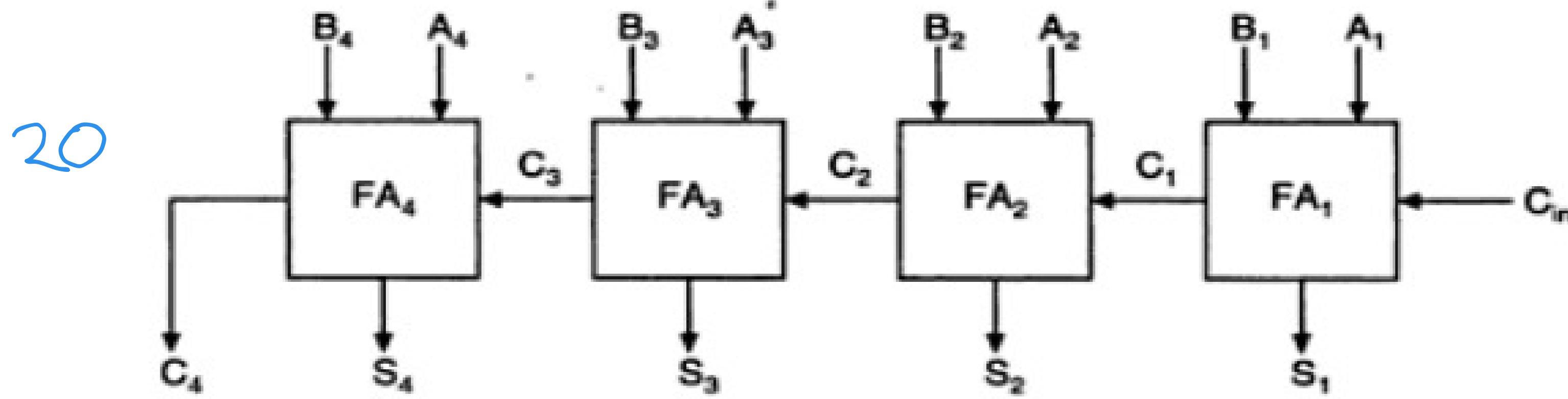
$$SUM = A \oplus B \oplus C$$

Propagation delay of FA = $2 \times$ Propagation delay of HA + Propagation delay of OR



4 bit ripple carry adder = 3 full adder + 1 half adder(for LBS)
 $= (N-1) \text{ FULL ADDER} + 1 \text{ AND GATE}$
 $= (N-1) (2 \text{ AND GATE} + 1 \text{ OR GATE}) + 1 \text{ AND GATE}$
 $= (2N-2)\text{AND} + (N-1) \text{ OR GATE} + 1 \text{ AND GATE}$

N BIT RIPPLE ADDER= $(2N-1)$ AND GATES + $(N-1)$ OR GATES



$$c_1 = (A_1 \text{ XOR } B_1) C_0 + A_1 B_1$$

$$C_2 = (A_2 \text{ XOR } B_2) C_1 + A_2 B_2$$

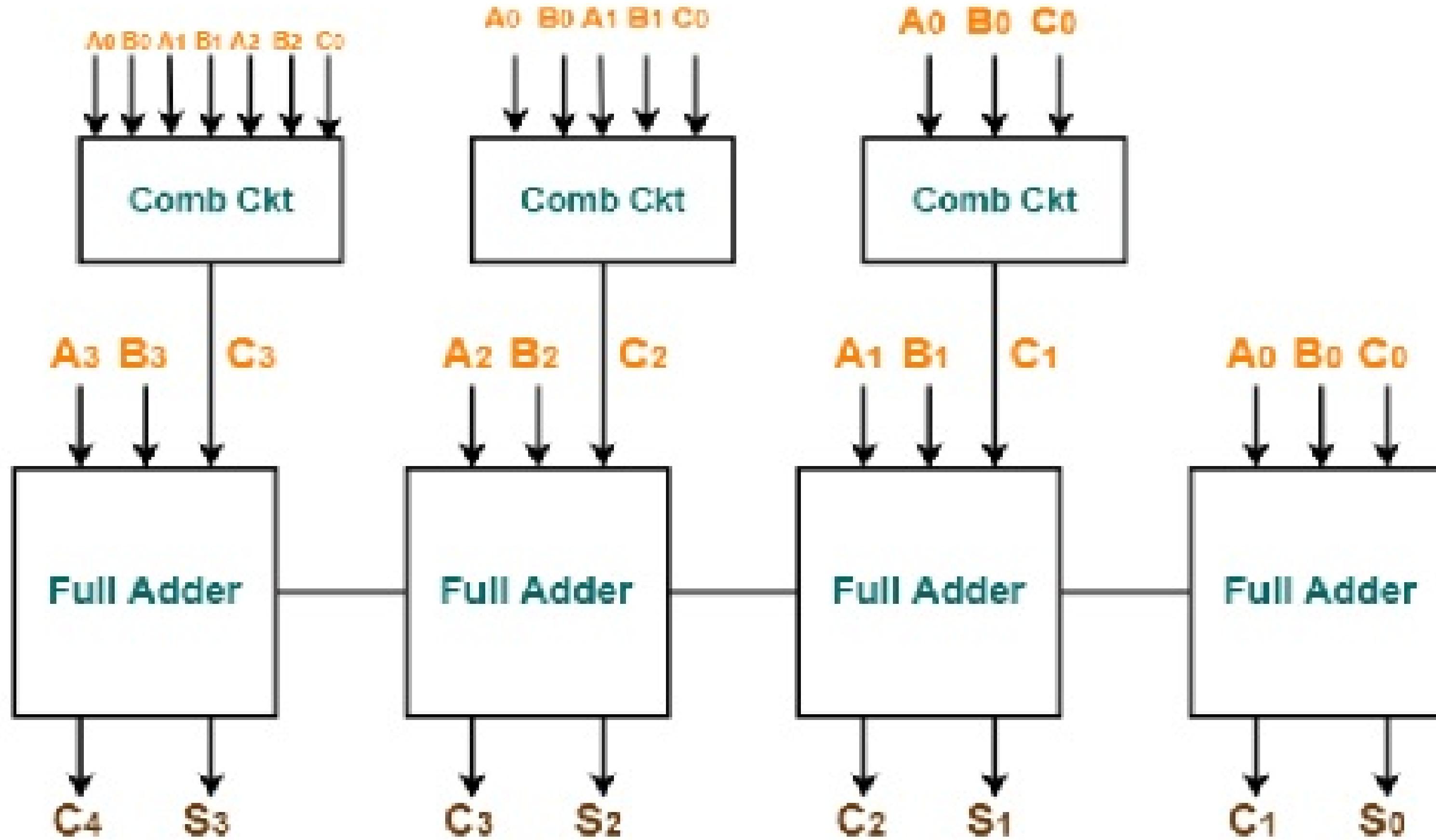
$$C_3 = (A_3 \text{ XOR } B_3) C_2 + A_3 B_3$$

$$C_4 = (A_4 \text{ XOR } B_4) C_3 + A_4 B_4$$



CARRY LOOK AHEAD ADDER

Carry Look-ahead Adder is the faster adder circuit. It reduces the propagation delay, which occurs during addition, by using more complex hardware circuitry. It is designed by transforming the ripple-carry Adder circuit such that the carry logic of the adder is changed into two-level logic.



$$Q = A \oplus B, \quad G = AB$$

Using the Gi and Pi terms the Sum Si and Carry Ci+1 are given as below –

$$Pi \text{ (carry propagate)} = A_i \text{ xor } B_i$$

$$Gi \text{ (carry generate)} = A_i B_i$$

$$S_{i+1} = Pi \oplus Ci.$$

$$Ci+1 = Ci \cdot Pi + Gi.$$

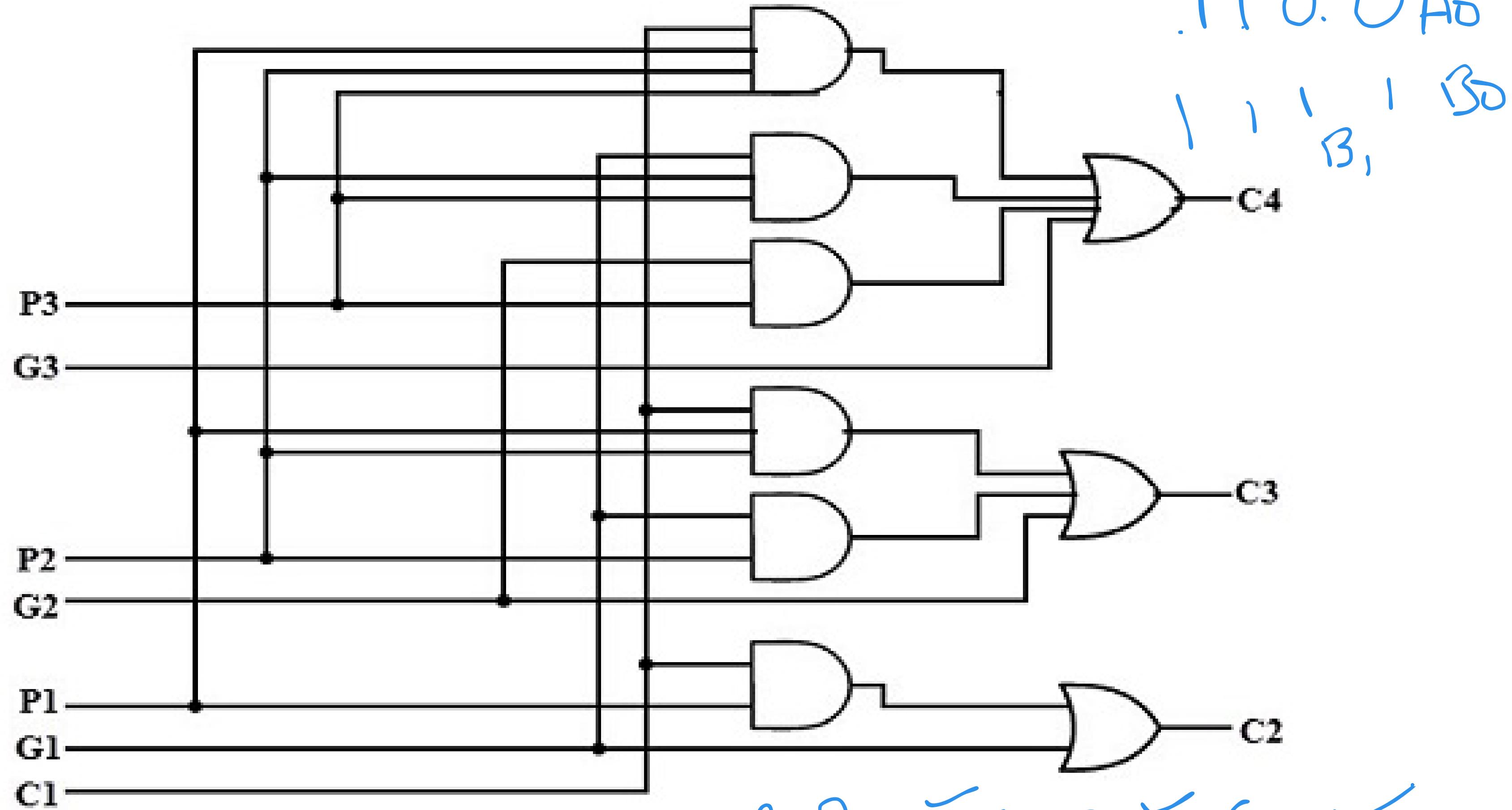
Therefore, the carry bits C1, C2, C3, and C4 can be calculated as

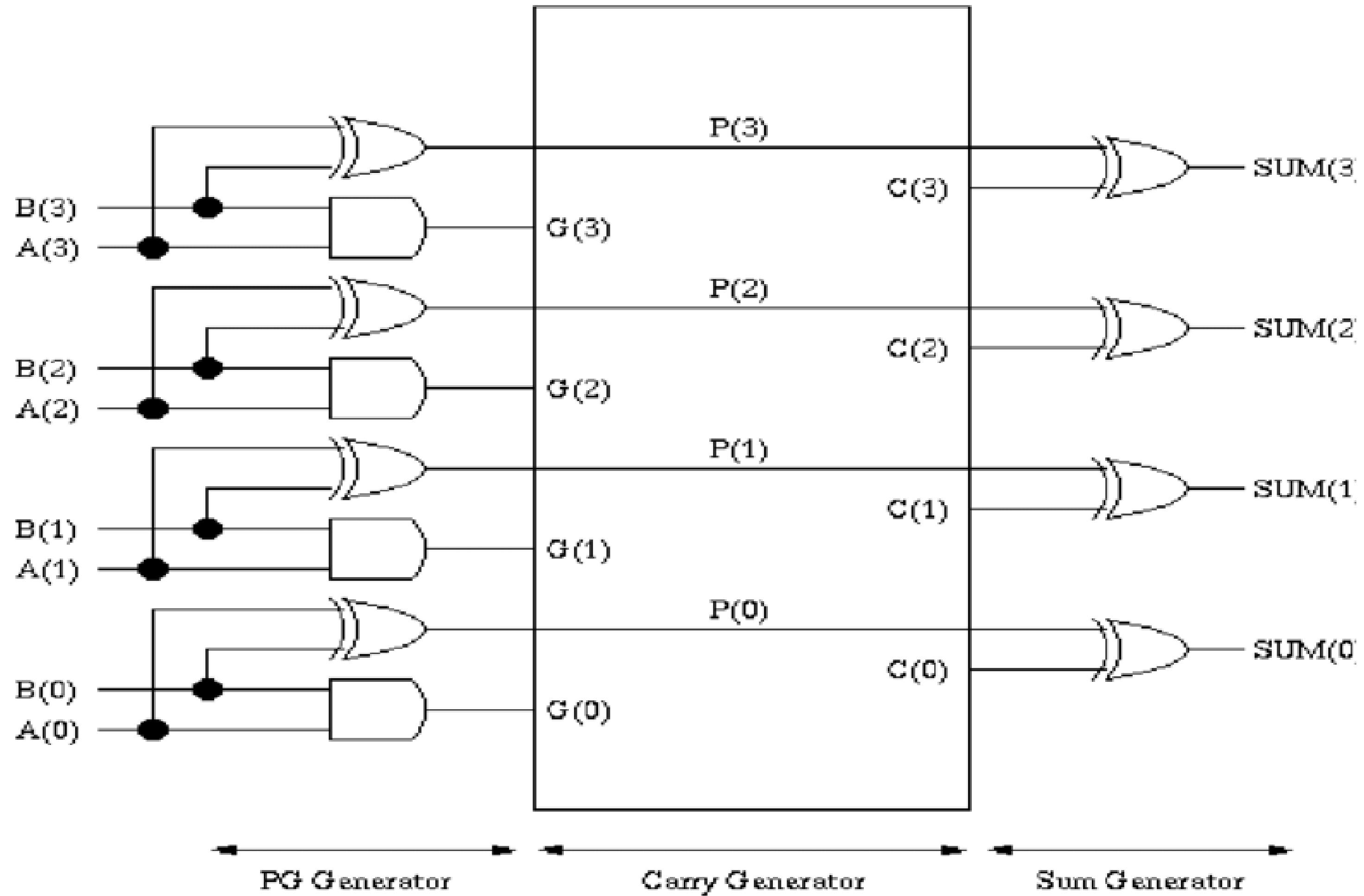
$$C1 = C0.P0+G0.$$

$$C2 = C1.P1+G1 = (C0.P0+G0).P1+G1 = C0 P0 P1+G0 P1+G1$$

$$C3 = C2.P2+G2 = (C1.P1+G1).P2+G2 = C0 P0 P1 P2 + G0 P1 P2 + G1 P2 + G2$$

$$C4 = C3.P3+G3 = C0.P0.P1.P2.P3 + P3.P2.P1.G0 + P3.P2.G1 + G2.P3 + G3.$$



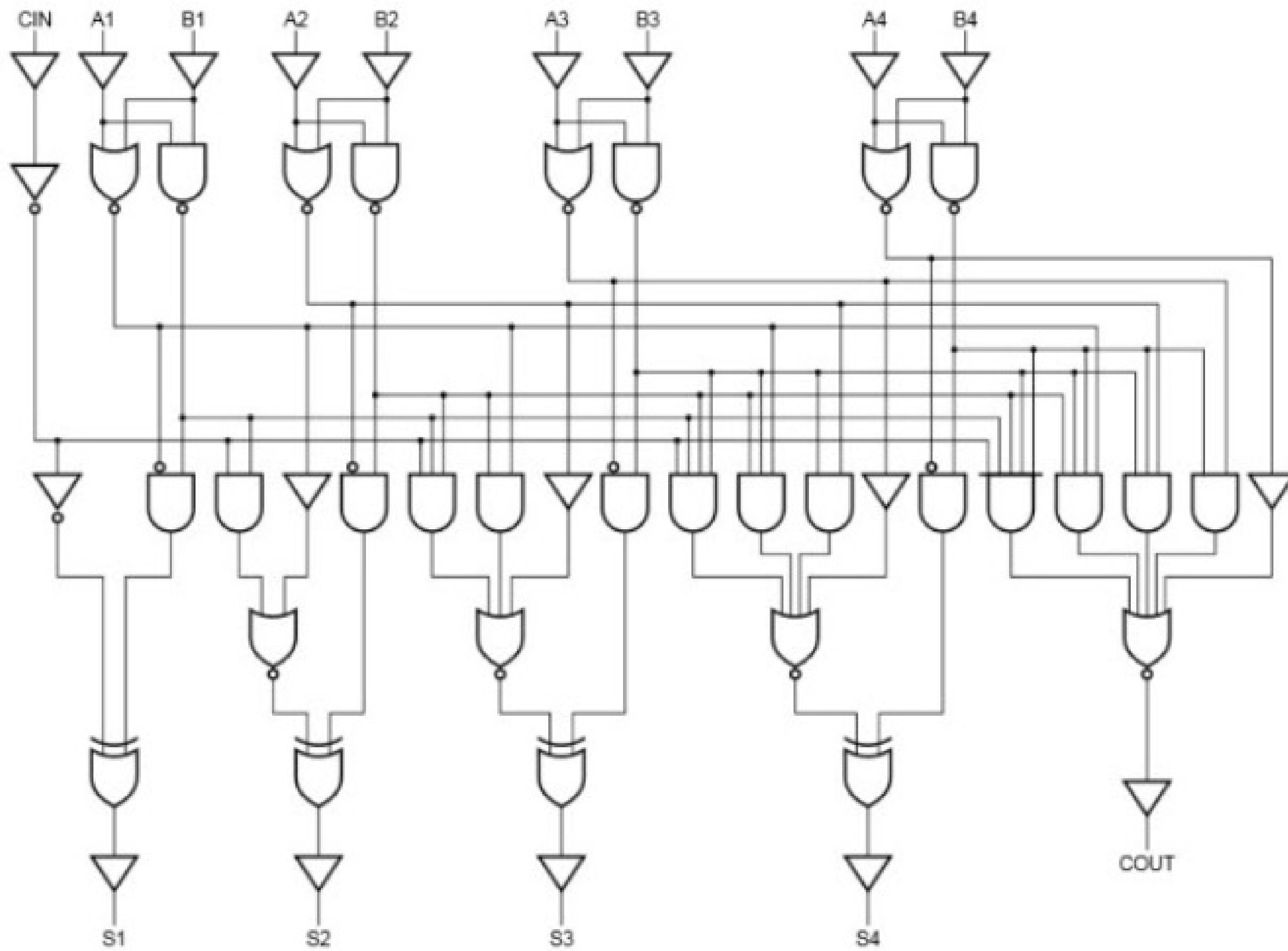


	A	B	C_{in}	C_{out}	
	0	0	0	0	No Carry
	0	0	1	0	Generate.
$G_i^o = 0$	0	1	0	0	Carry fro
$P_i^o = 1$	0	1	1	1	No Carry Propagate.
	1	0	0	0	
	1	0	1	1	
	1	1	0	1	Carry Generate
	1	1	1	1	as $G_i^o = 1$.

$$C_{i+1}^o = G_i^o + P_i^o C_i^o$$

$$= G_i^o + (A \oplus B) C_i^o$$

$$= AB + (A \oplus B) C_i^o$$



A 4 bit Carry Look Ahead (CLA) adder can be constructed with the help of following steps (Assuming T as the delay of a single 2-Input gate):

1. Generate All P and G internal signals.
These can be generated simultaneously as C0 and all inputs are available.
2. Generate all carry output signals (C1, C2, C3, C4). These will be valid after 3T time
3. Generate Sum signals $S = P \text{ xor } C$. It will be valid after 4T time.

Thus, Sum signals will be valid after a delay of 4T. On the other hand, delay expression in case of ripple carry adder = $(2n+2)T$. Thus, for n =4, i.e. for 4 bit ripple carry adder, delay will be 10T.

No. of OR gates = n

No. of AND Gates = $n(n+1)/2$

$$c_1 = 1$$

$$c_2 = 2$$

$$c_3 = 3$$

$$\Rightarrow [1 + 2 + 3 + \dots] = n(n+1)/2$$

\Rightarrow Carry look ahead Adder has
4 stages \rightarrow .

① stage $\rightarrow P_i^o, G_i^o$.

② & ③ stage - Carry Generate

④ stage - Sum Generate.

$$S_{i+1}^o = P_i^o \oplus C_i^o$$

Q.1. Time complexity of n bit Adder

(look ahead) is 3.

Assuming ($n+1$) input or and gates
are available.

Ans. No. of stages = 4.

for carry there are 3 stages.

4th stage only for sum.

Ans. Time Comx = $O(1)$.

$A_{n-1} \dots A_2 A_1 A_0$

$B_{n-1} \dots B_2 B_1 B_0$

$S_{n-1} \dots S_2 S_1 S_0$

PRACTICE PROBLEMS

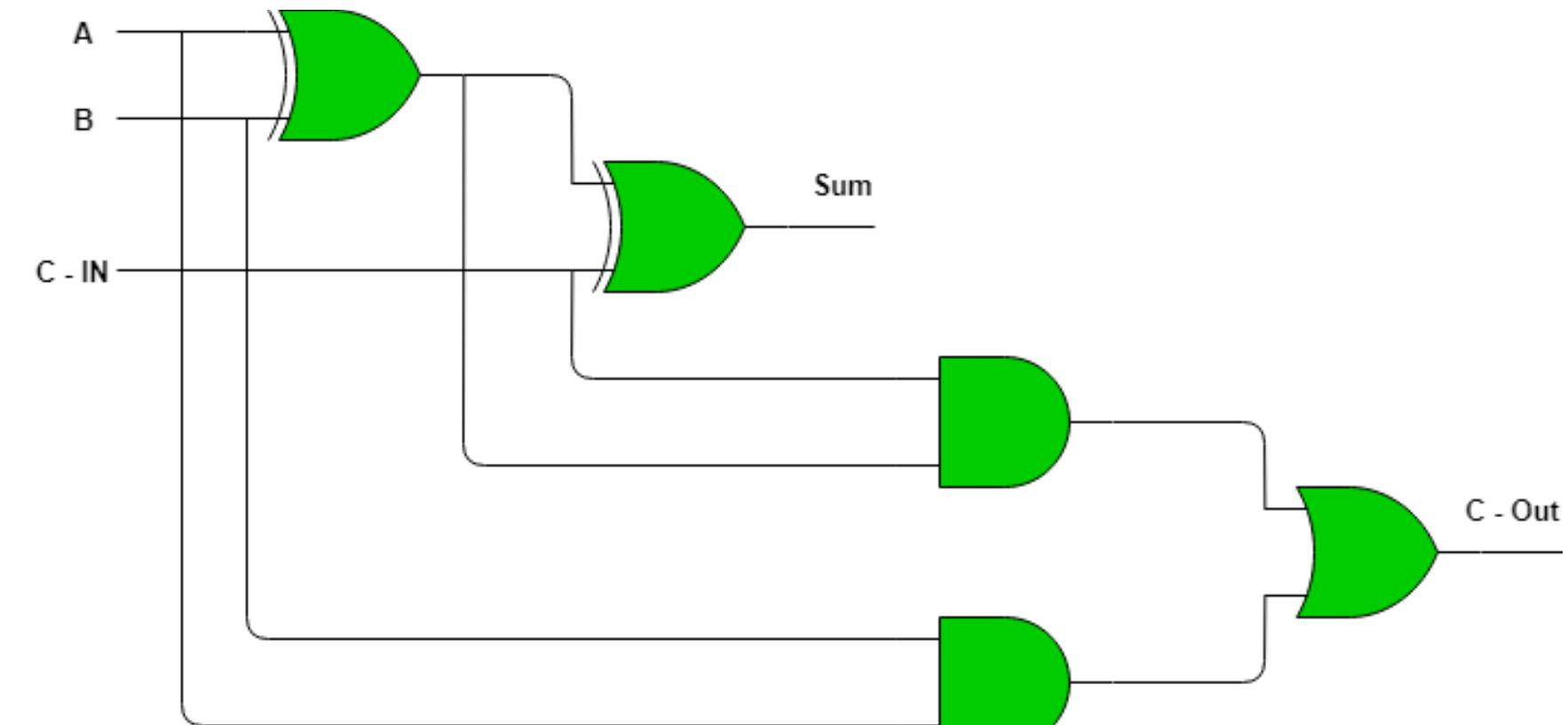
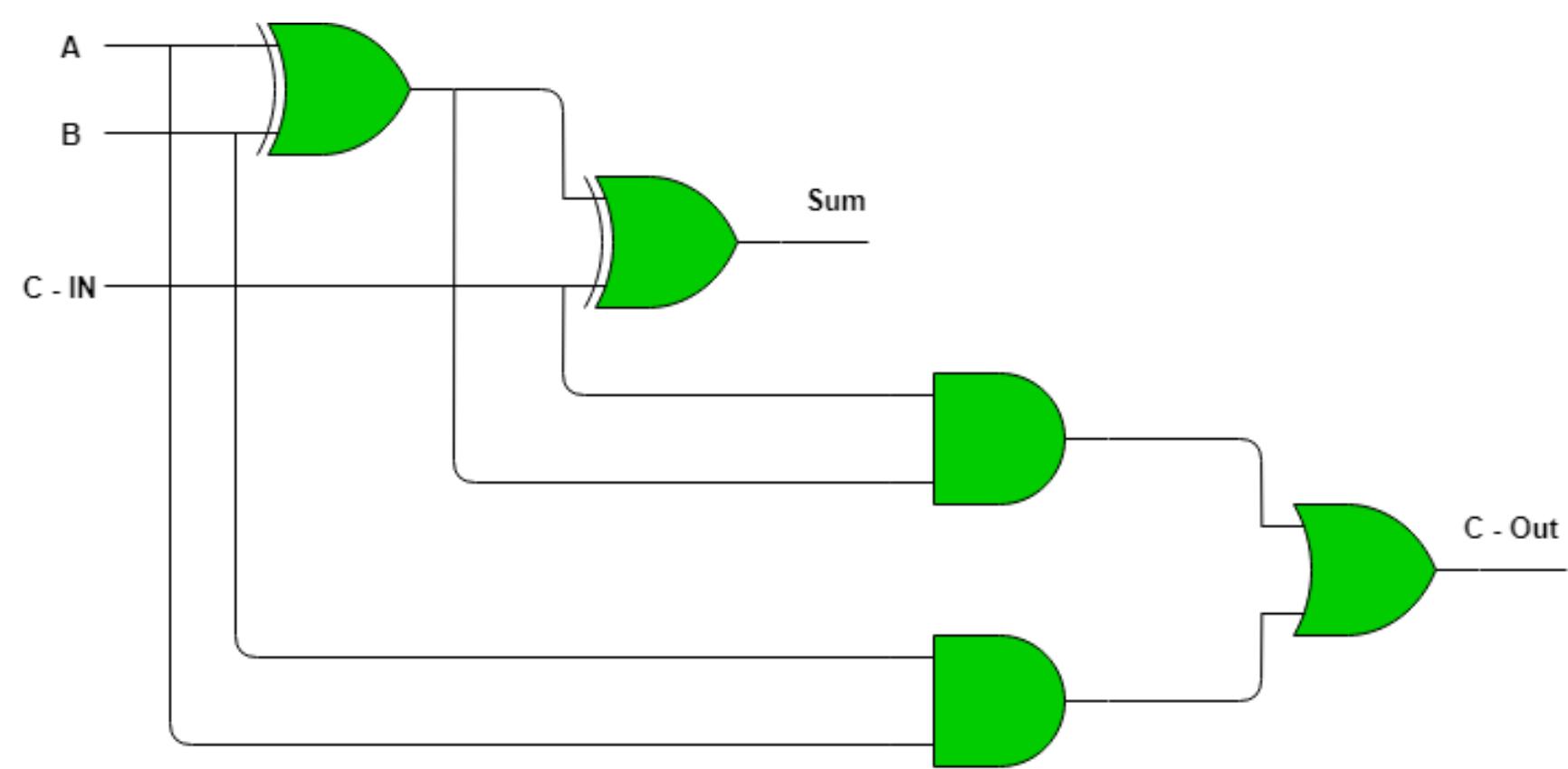
1 DESIGN FULL ADDER USING NAND GATE AND NOR GATE

2 DESIGN SUBTRACTOR USING NAND AND NOR GATE

3 CONVERT BCD TO GREY CODE ,MAKE A CIRCUIT AND TRUTH TABLE

How many gate delays are there in overflow for ripple carry adder?

- If LSB also uses FULL Adder,(we can use Half Adder for LSB because we don't need carry-in).
- For the first carry out, there will be 3 GATE DELAY: 1 AND, 1 EX-OR, 1 OR
- For the next $(n-1)$ bit , only 2 Gate Delay will be considered: 1 OR and 1 AND because EX-OR Operation will happen at parallel.
- So total gate delay will be = $2*(n-1) + 3 = 2n+1$ Gate Delay



Half Adder is implemented with XOR and AND gate. A. FA is implemented with 2 HA and 1 OR gate The propagation delay of XOR -gate is twice that of AND / OR gate. Propagation delay of AND/OR is 1.2 ms. A 4-bit ripple carry binary adder is implemented using 4 full adder. the total propagation time of this 4 bit binary adder in micro second is _____?

full adder needs

carrytime delay = Xor gate delay + and gate delay+ or gate delay =
 $2.4 +1.2+1.2= 4.8\text{msec}$

sum delay = 2 Xor gate delay = 4.8 msec

total propa. time for 4 bit adder = $3*\text{carry time} + \max(\text{sum}, \text{carry time})$
 $= 3*4.8 +4.8$

In a 4 bit carry look ahead adder, the propagation delay of EX-OR gate is 20 NSEC, AND and OR gates is 10nsec. The sum and carry output of full adder takes 20nsec and 10nsec respectively. The total propagation delay of the above adder is ?

solution : 20ns (External Ex-OR GATE) + 10ns (Internal AND GATE) + 10ns (Next level OR GATE + 20ns (External Ex_OR GATE)

$$\text{Total : } 20\text{ns} + 10\text{ns} + 10\text{ns} + 20\text{ns} = 60\text{ns}$$

4 stages ;

1 STAGE : $G_i = A_i B_i$, $P_i = A_i \text{ xor } B_i$ g_i and p_i in parallel ... 20 NSEC

2 AND 3RD STAGE : c_4 generate using OR AND GATE $10+10$ NSEC..

STAGE 4 : SUM GENERATE: $P_i \text{ xor } C_i$ 20 nsec