COEP Technological University

(COEP Tech)
A Unitary Public University of Government of Maharashtra
w.e.f 21st June 2022
(Formerly College of Engineering Pune)

END SEM Examination

Programme: B.Tech FY | **Semester: II**

Course Code: CT 23006 | **Course Name: Digital Logic Design**

Branch: Computer Engineering & IT | **Academic Year: 2023-2024**

Duration: 3 Hr | **Max Marks: 60**

Student PRN No :

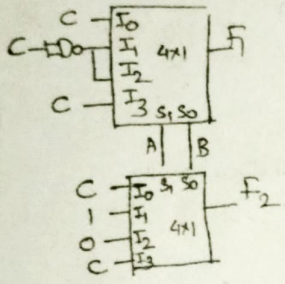
Instructions :

1. Figures to the right indicate the full marks.
2. Mobile phones and programmable calculators are strictly prohibited.
3. Writing anything on question paper is not allowed.
4. Exchange/Sharing of stationery, calculator etc. not allowed.
5. Write your PRN Number on Question paper.

	Marks	CO	PO
Q.1 Consider the Boolean function, $F(A,B,C\ D) = \sum(0,2,3,8,9,10,11,13,15)$ Find the following:	[06]	[1]	[2,3]
A. Complete set of Prime and Essential prime implicants.			
B. Simplified sum of product and product of sum.			
Q.2 Design a BCD to Excess 3 code converter. Draw the truth table, simplified form and logic gates.	[08]	[1,3]	[2,3]
Q.3 Design a 4 to 2 bit priority encoder for inputs Y3, Y2, Y1, Y0 (Y3 having highest priority and Y0 having lowest priority) and outputs A1 AND A0 with truth table, logic equations and logic gates diagram.	[06]	[1,3]	[2,3]

Q.4 In a 10-bit parallel adder setup, the propagation delay of EX-OR gate is 20 ns, AND & OR gates is 10 ns. Find out the total propagation delay of the Carry look ahead adder. Assume multi-input gates. [06] [1,2] [3]

Q.5 Realize the following multiplexer using Min no of NAND GATES: Implement both f1 and f2 [08] [3] [3]



Q.6 Convert SR flip flop into JK flip flop by drawing suitable diagram, table and equations. [06] [2] [2,4]

Q.7 Explain Master Slave flip flop and its working. [08] [4] [3,4]

Q.8 Explain the difference between Ring AND Johanson counter [06] [4] [1,4]

Q.9 Explain the Algorithmic State Machine. [06] [2] [1,4]