COEP Technological University

(COEP Tech)
A Unitary Public University of Government of Maharashtra
w.e.f 21st June 2022
(Formerly College of Engineering Pune)

Test 2 Examination

Programme: B.Tech | **Semester: II**

Course Code: : CT 23006 | **Course Name: Digital Logic Design**

Branch: Computer Engineering & IT | **Academic Year: 2023-2024**

Duration: 1 Hr | **Max Marks: 20**

6	1	2	3	0	3	0	4	3

Student PRN No :

Instructions :

1. Figures to the right indicate the full marks.
2. Mobile phones and programmable calculators are strictly prohibited.
3. Writing anything on question paper is not allowed.
4. Exchange/Sharing of stationery, calculator etc. not allowed.
5. Write your PRN Number on Question Paper.

	Marks
Q.1 Design Carry look ahead generator for 4 bit additon .	[05]
Q.3 Design a JK FLIP FLOP using NAND gates. Write all of its tables.	[04]
Q.4 Design 8 to3 priority encoder with 1 valid (v) output.	[04]
Q.5 Why latches are not considered the perfect choice for sequential circuits design. Design the SR LATCH.	[04]
Q.6 Design a Full Adder using 3 to 8 Decoder.	[03]