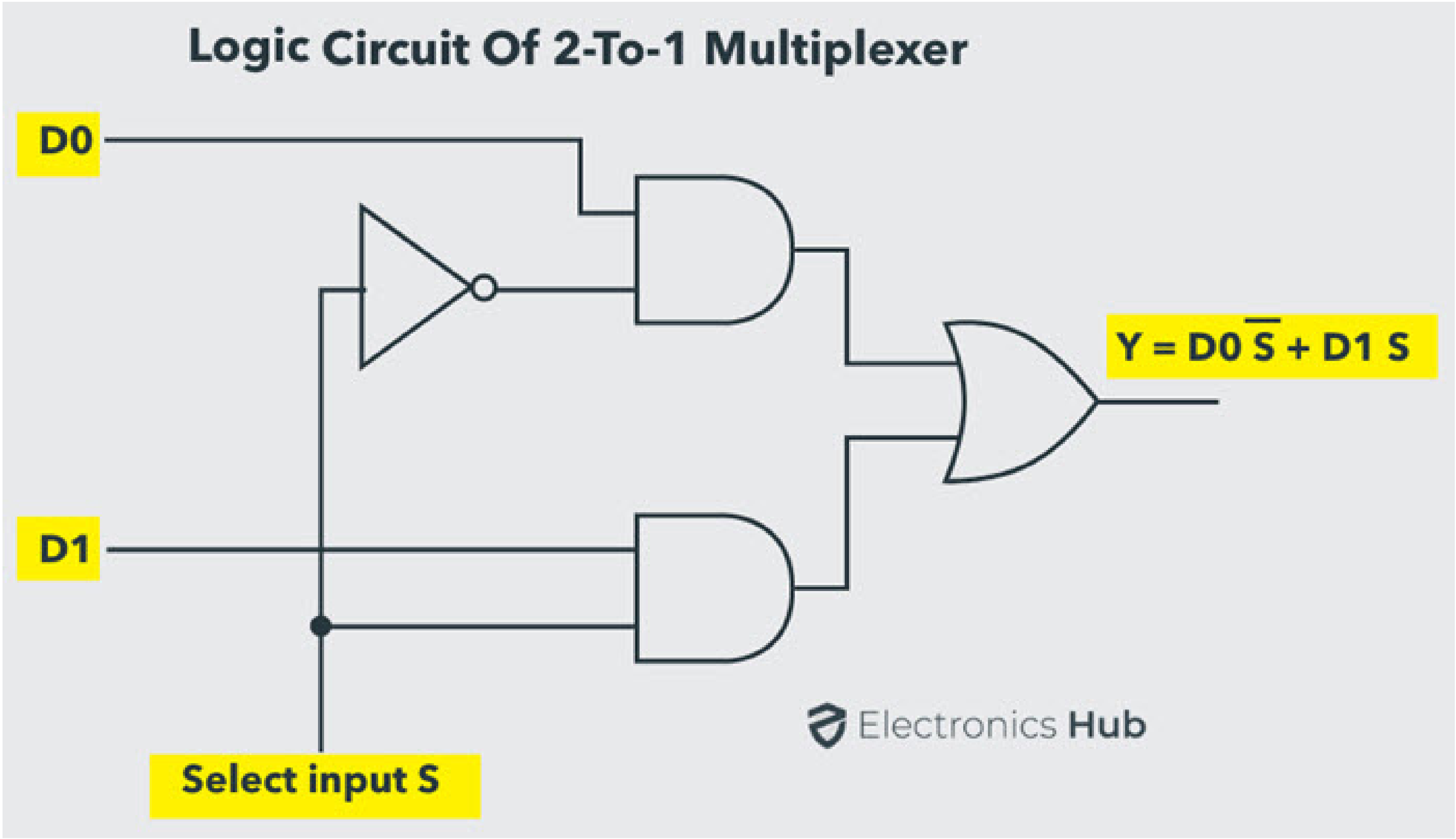
Multiplexers in Digital Logic

It is a combinational circuit which have many data inputs and single output depending on control or select inputs

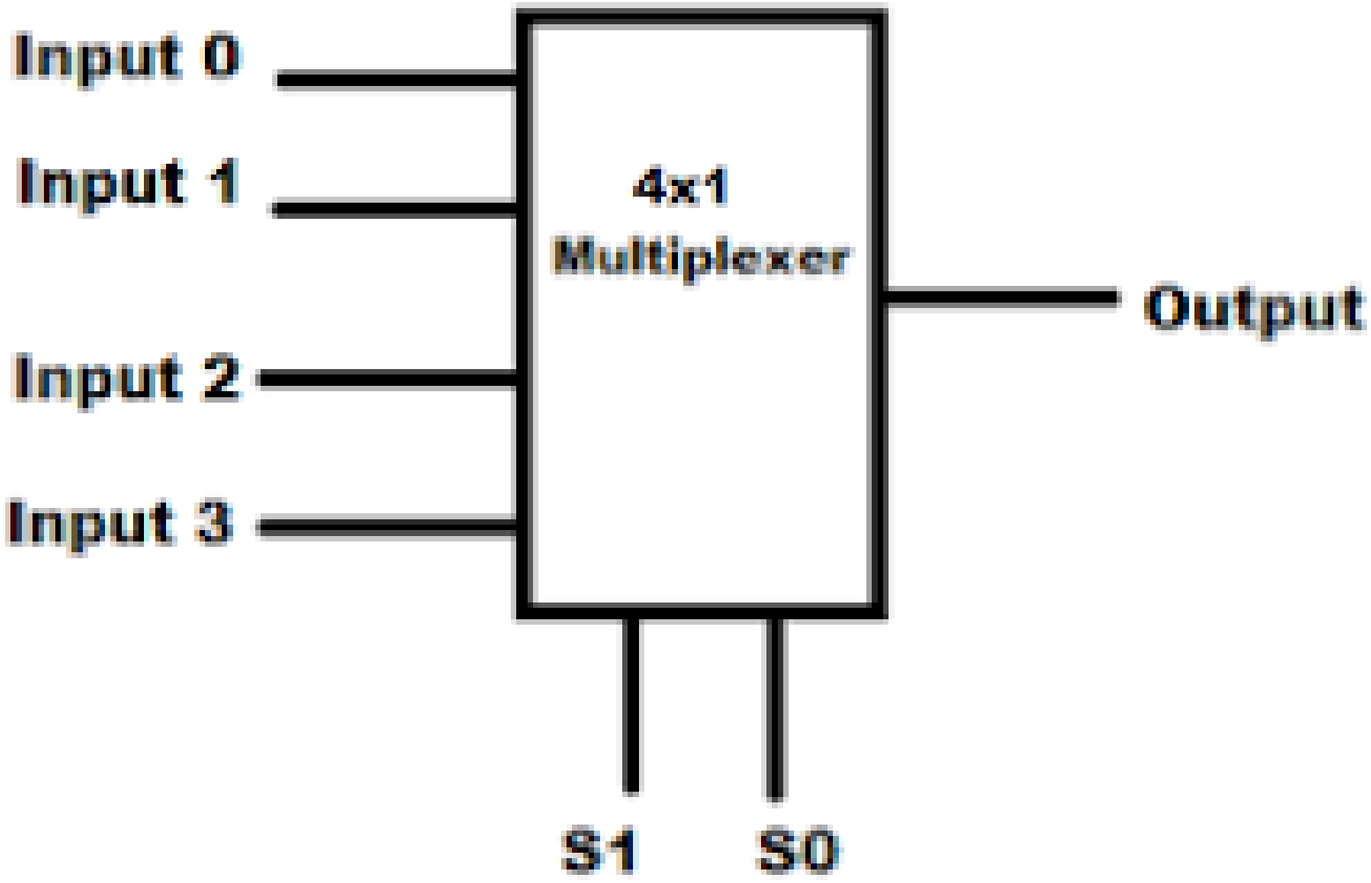
for 2n input lines, n selection lines are required.

Multiplexers are also known as n selector, parallel to serial convertor, many to one circuit, universal logic circuit

Multiplexer can act as universal combinational circuit. All the standard logic gates can be implemented with multiplexers.


Logic Circuit Of 2-To-1 Multiplexer
D0
D1
Y = D0 S̄ + D1 S
Select input S
Electronics Hub

4 to 1 multiplexer



Truth Table

S0	S1	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

So, final equation,

$$Y = S0'.S1'.I0 + S0'.S1.I1 + S0.S1'.I2 + S0.S1.I3$$

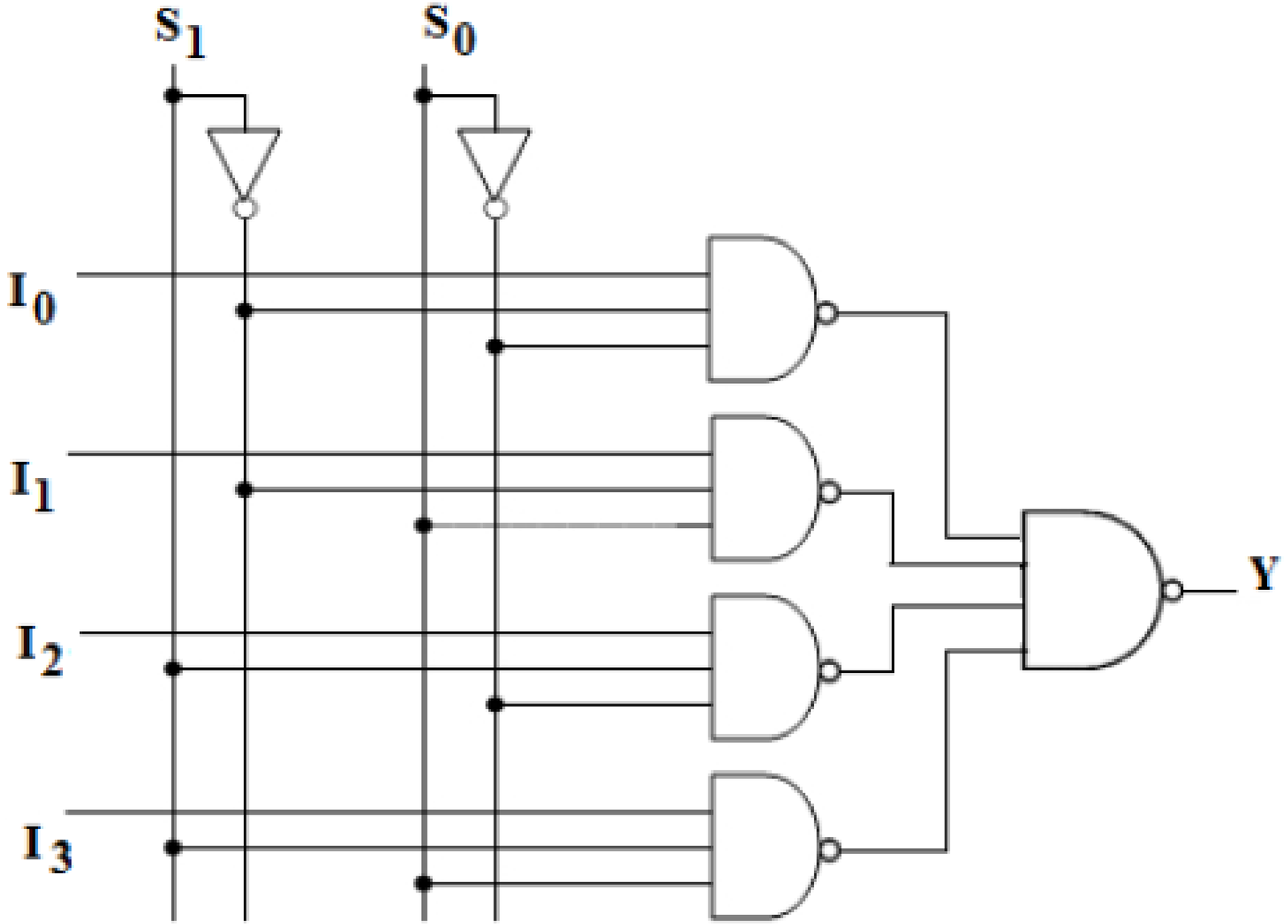
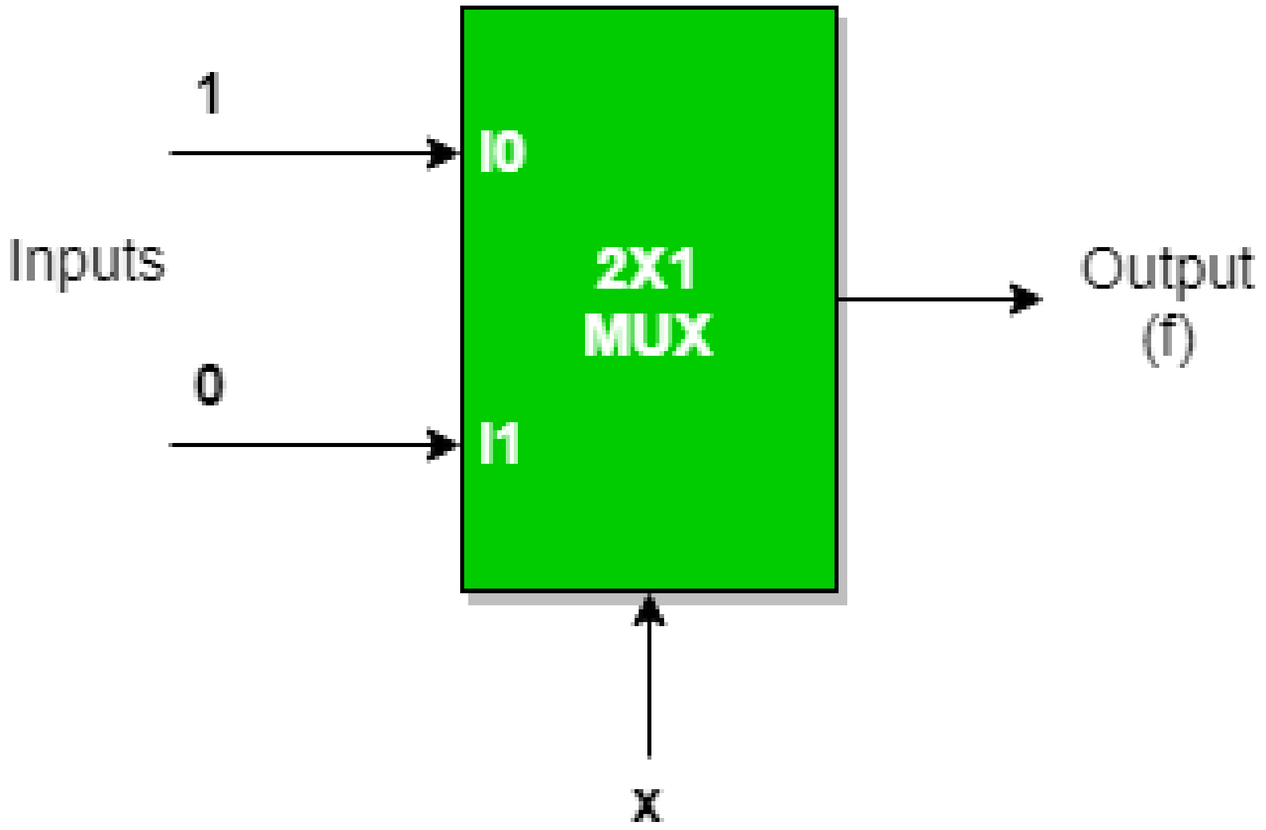


Fig. 1: 4x1 Multiplexer

Implementation of NOT gate using 2 : 1 Mux



Truth Table

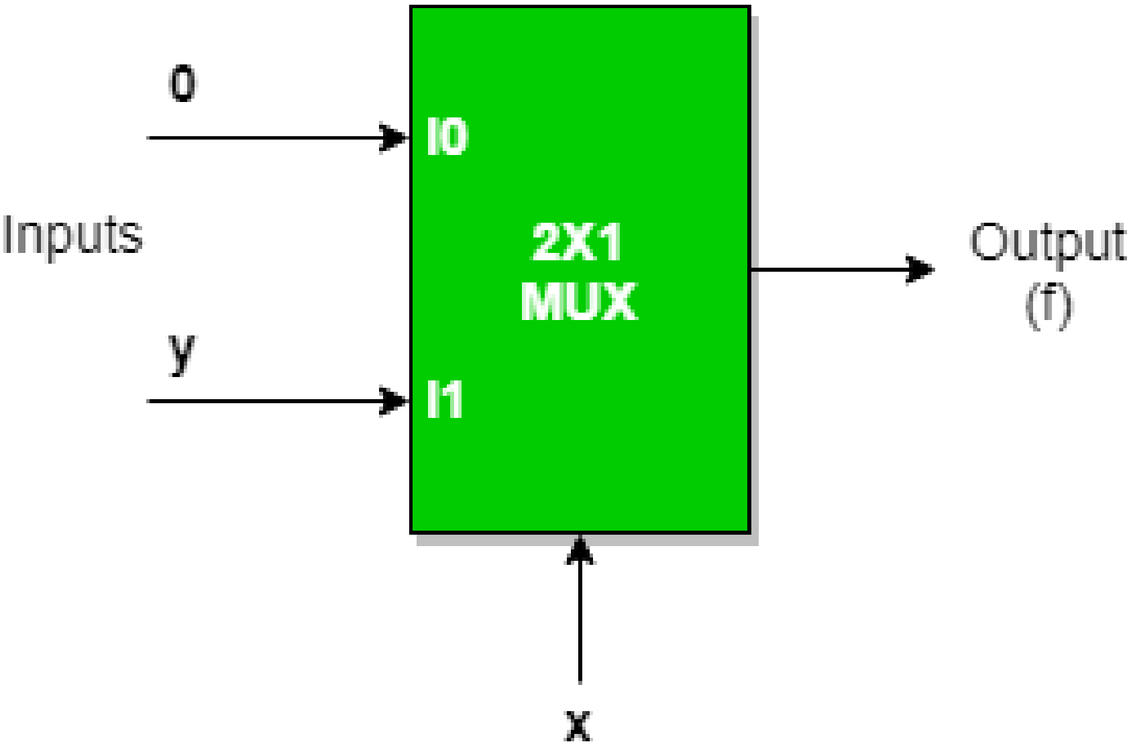
x	f
0	1
1	0

We can analyze it

Y = x'.1 + x.0 = x'

It is NOT Gate using 2:1 MUX.

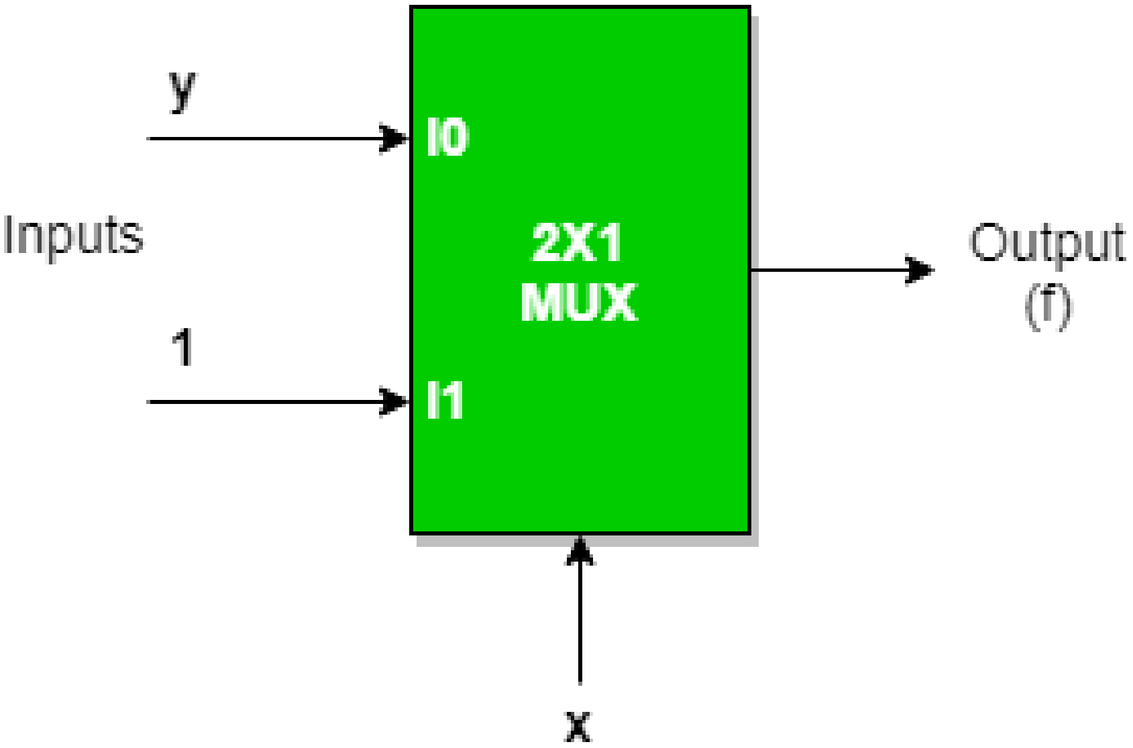
Implementation of AND gate using 2 : 1 Mux



Truth Table

x	y	f	f→y
0	0	0	f = 0
0	1	0	
1	0	0	f = y
1	1	1	

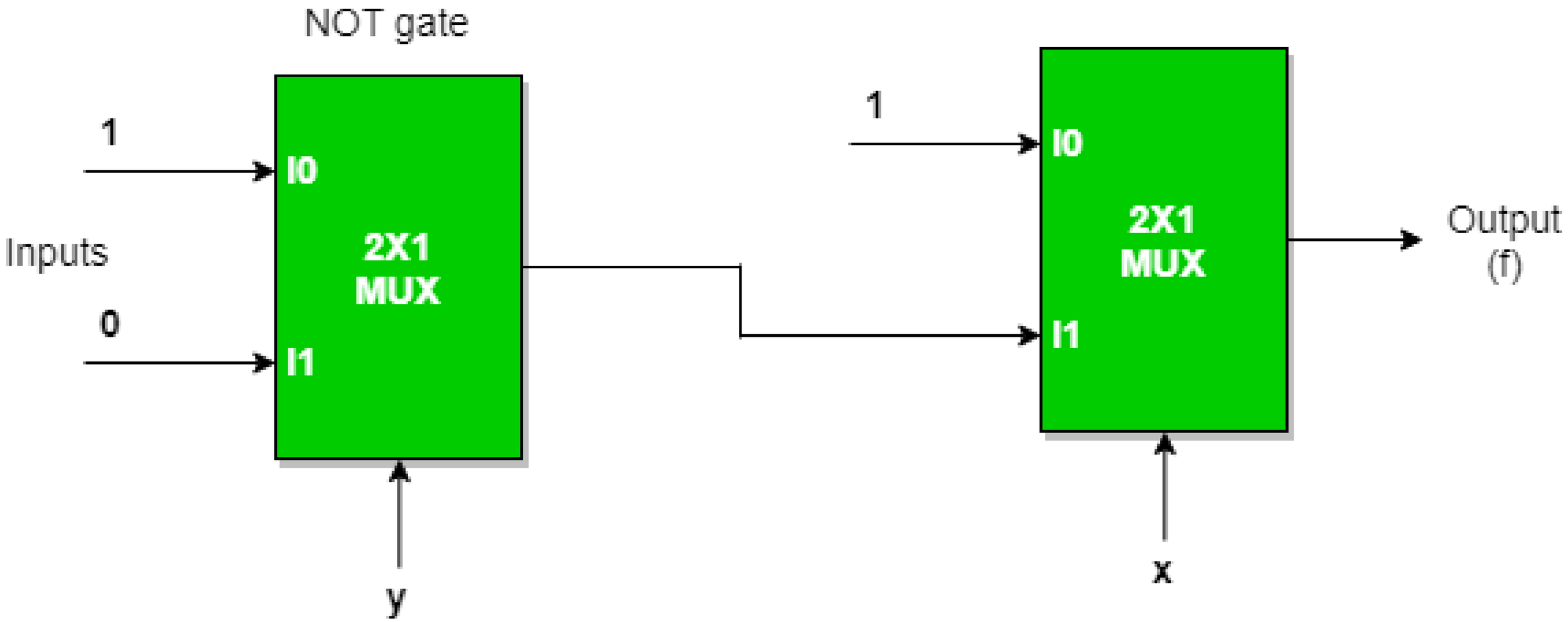
Implementation of OR gate using 2 : 1 Mux



Truth Table

x	y	f	f→y
0	0	0	f = y
0	1	1	
1	0	1	f = 1
1	1	1	

Implementation of NAND gate using 2 : 1 Mux



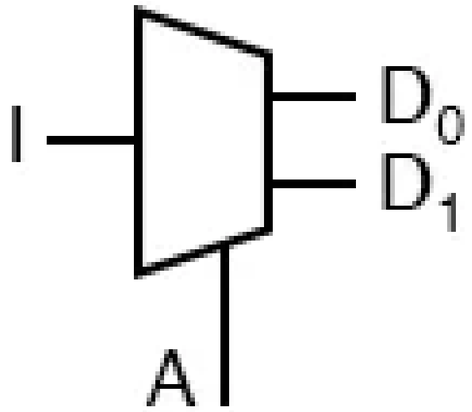
nand gate using 4 to 1 multiplexer

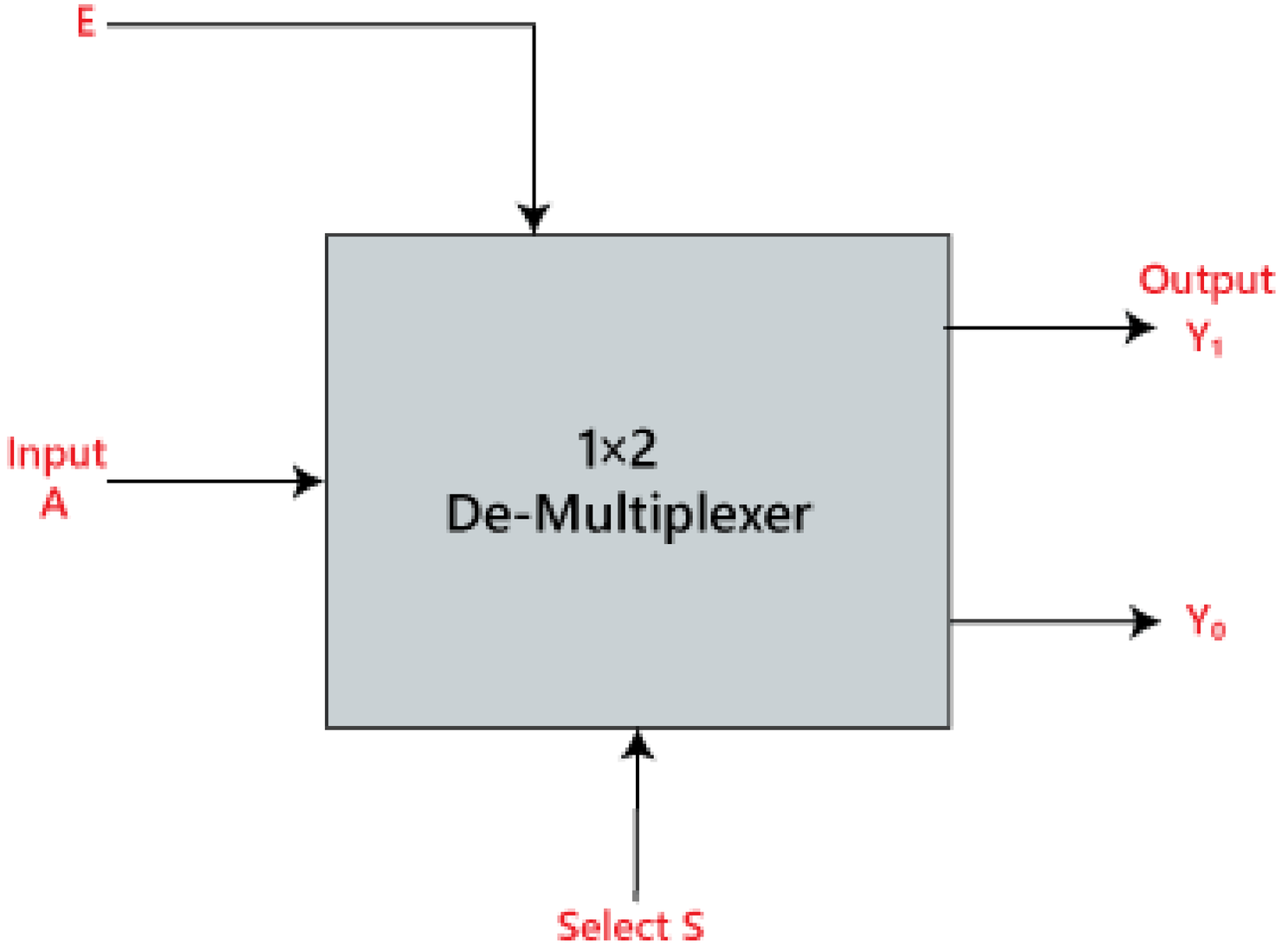
xor gate using multiplexer

xnor gate using 4 to 1 multiplexer

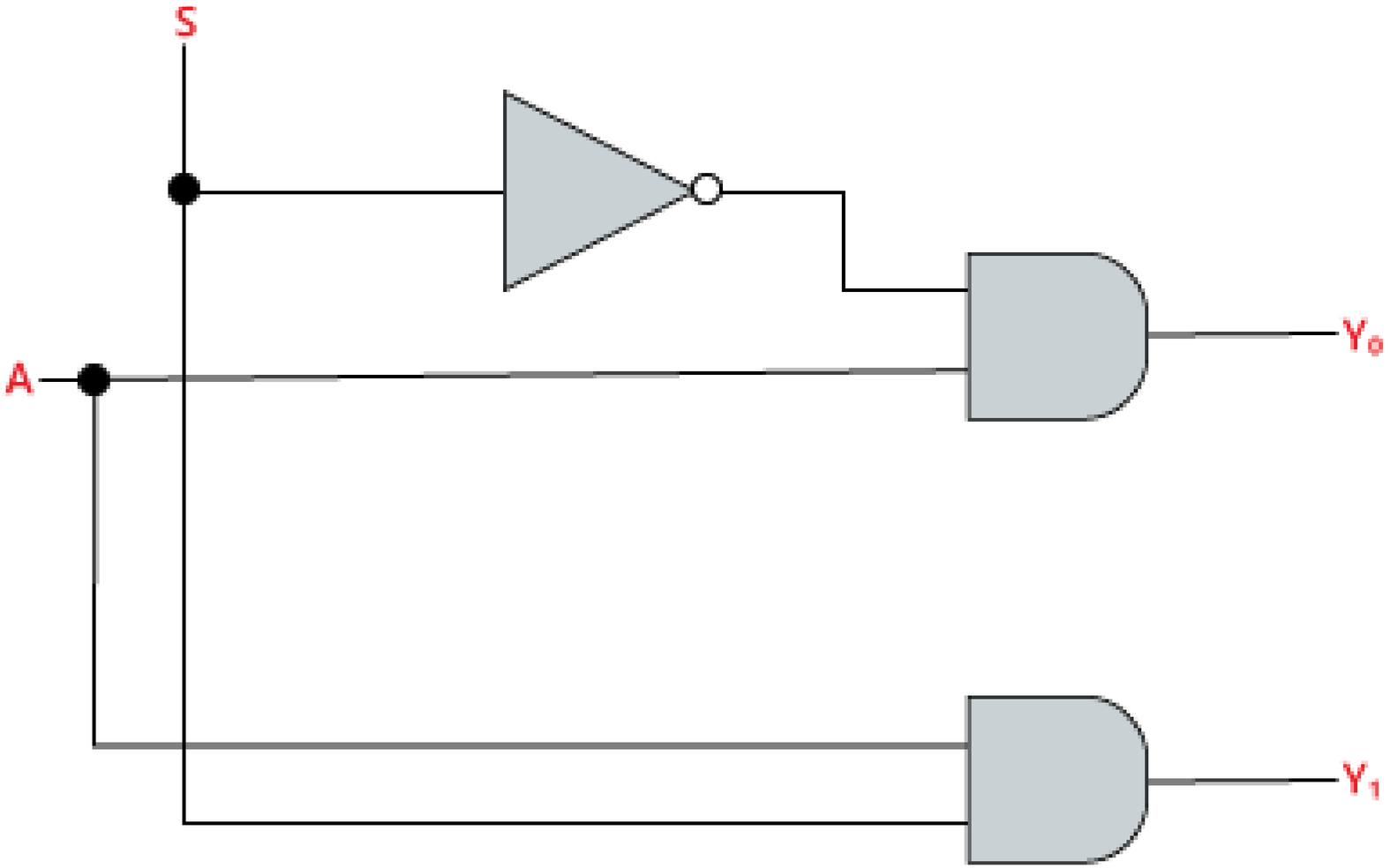
Demultiplexers

A demultiplexer, sometimes abbreviated dmux, is a circuit that has one input and more than one output. It is used when a circuit intends to send a signal to one of many devices.





INPUTS	Output	
S_0	Y_1	Y_0
0	0	A
1	A	0



The logical expression of the term Y is as follows:

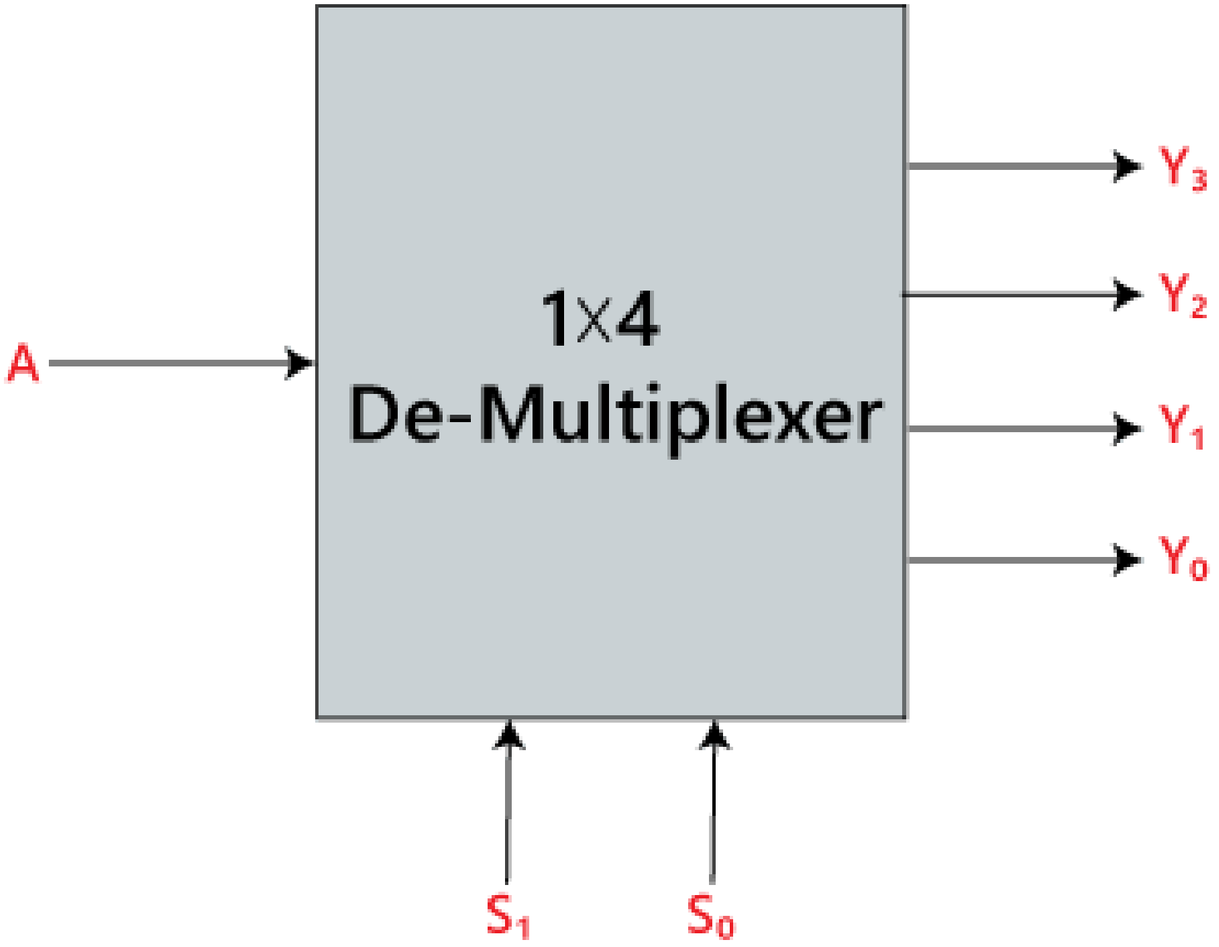
Y0=S0'.A

Y1=S0.A

1×4 De-multiplexer:

In 1 to 4 De-multiplexer, there are total of four outputs, i.e., Y0, Y1, Y2, and Y3, 2 selection lines, i.e., S0 and S1 and single input, i.e., A.

On the basis of the combination of inputs which are present at the selection lines S0 and S1, the input be connected to one of the outputs.


1×4
De-Multiplexer
A
Y_3
Y_2
Y_1
Y_0
S_1
S_0

INPUTS		Output			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	A
0	1	0	0	A	0
1	0	0	A	0	0
1	1	A	0	0	0

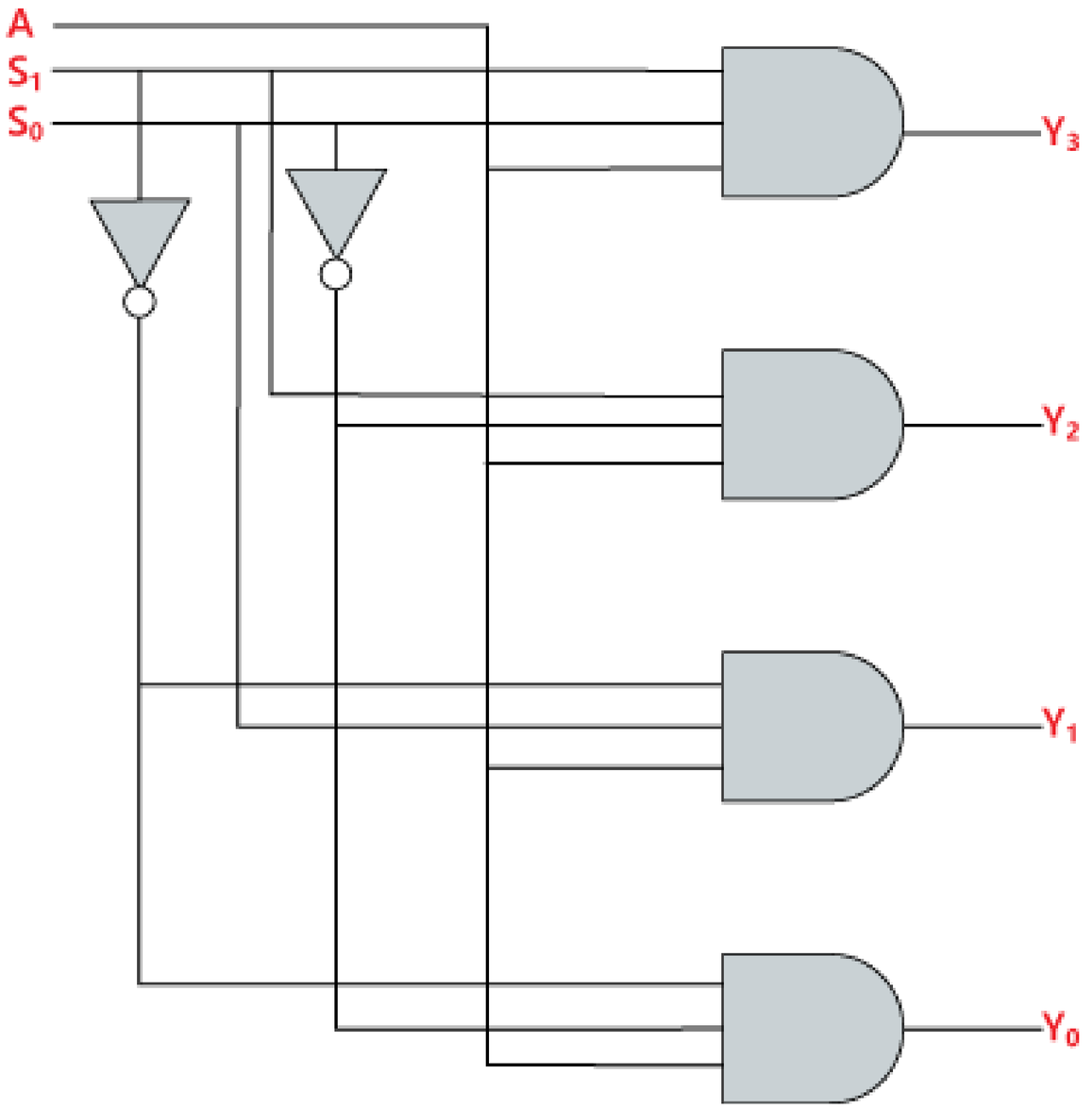
The logical expression of the term Y is as follows:

Y0=S1' S0' A

y1=S1' S0 A

y2=S1 S0' A

y3=S1 S0 A


A
S1
S0
Y3
Y2
Y1
Y0