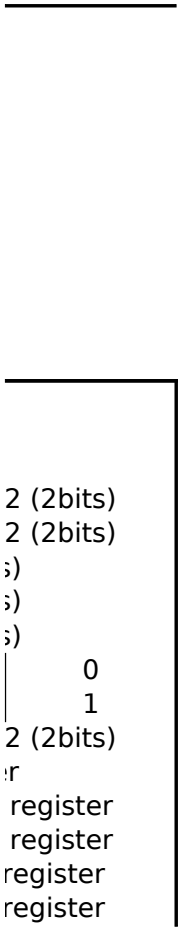
Register	Address	Comments
r0	000	
r1	001	
r2	010	
r3	011	
zero	100	always reads 0
one	101	always reads 1
dst low	110	
dst high	111	

Instruction	Command	Comments
halt	hlt	
branch less than	blt	
branch greater equal	bge	
addition	add	writes to reg1 if not $zero or $one, else writes to reg2
subtraction	sub	writes to dst low
shift right logical / 16	srl4	read/write from same register
shift right logical / 2	srl	read/write from same register
shift left logical * 16	sll4	read/write from same register
increment dst high	inch	add flag bit to destination high
set r3 to 3	Set3	writes 3 to $r3
bitwise and	and	
move	mov	
load	ld	loads D[address] into destination register
load next	ldn	loads D[address + 1] into destination register
store	st	stores source register into D[address]
store next	stn	stores source register into D[address + 1]

Opcode				
000	0	0000		
000	0	offset (4 bits)		
000	1	offset (4 bits)		
001	register 1 (3bits)		register	
010	register 1 (3bits)		register	
011	0	0	register (3 bits	
011	0	1	register (3 bits	
011	1	0	register (3 bits	
011	1	1	0	0
011	1	1	0	0
100	register 1 (3bits)		register	
101	destination register		source registe	
110	1	destination register	address	
101	0	destination register	address	
111	0	address register	source r	
111	1	address register	source r	


2 (2bits)
2 (2bits)
s)
s)
s)
0
1
2 (2bits)
r
register
register
register
register