ECE111 Winter 2007 Project 1

- Due Thursday, January 18.
- Read Tutorial 1 before starting Project 1.
- Project 1 is the design of a Fibonacci calculator using Verilog HDL.
- Accepts as input a number n on an input port, and a clock, and outputs the nth Fibonacci number, some number of clocks later.

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 The nth Fibonacci number is the sum of the (n-1)th and (n-2)th Fibonacci number, and the first two numbers, the 0th and 1st Fibonacci numbers, are 1 and 1.

So the Fibonacci sequence is:

1,1,2,3,5,8,13,21,...