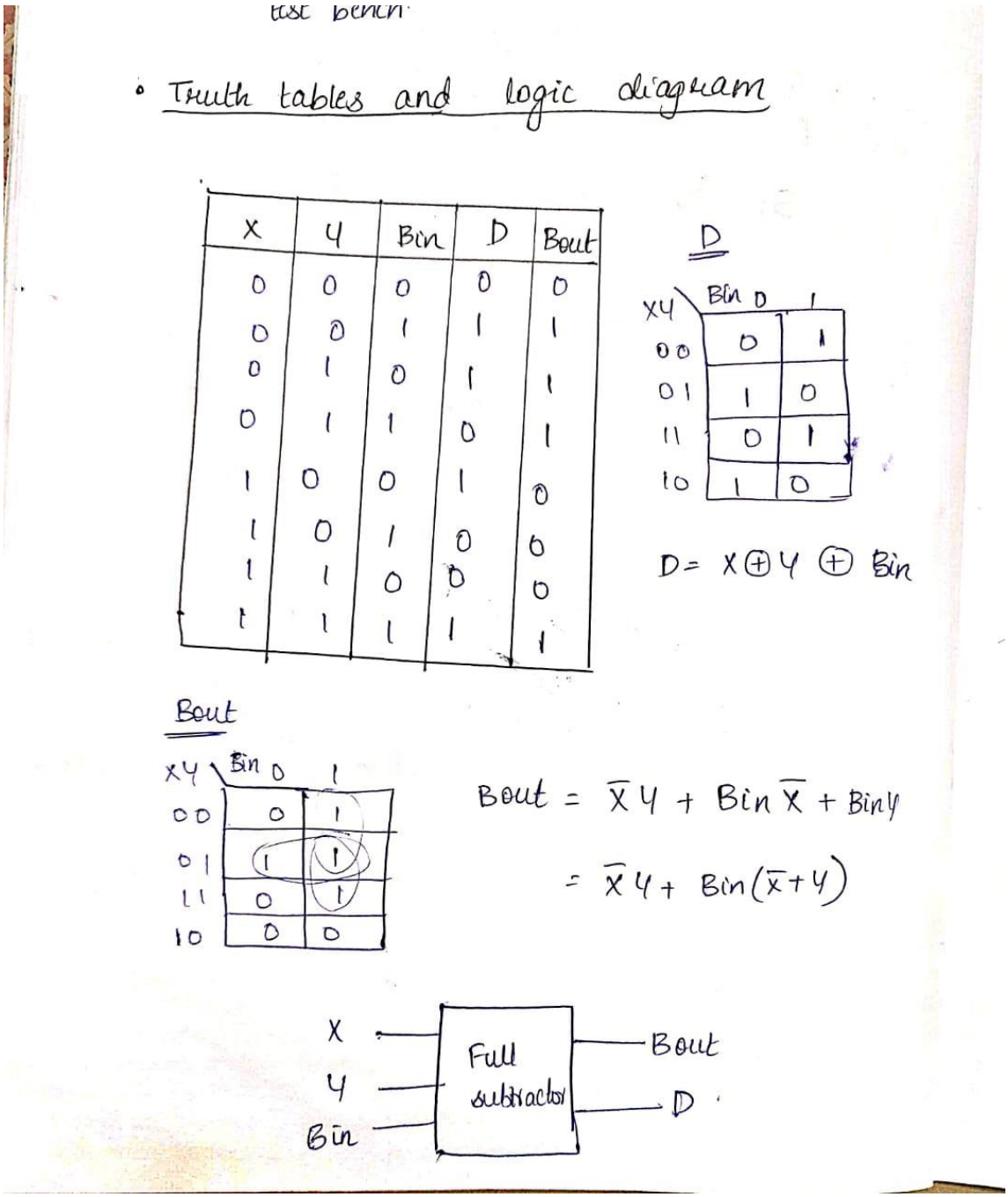
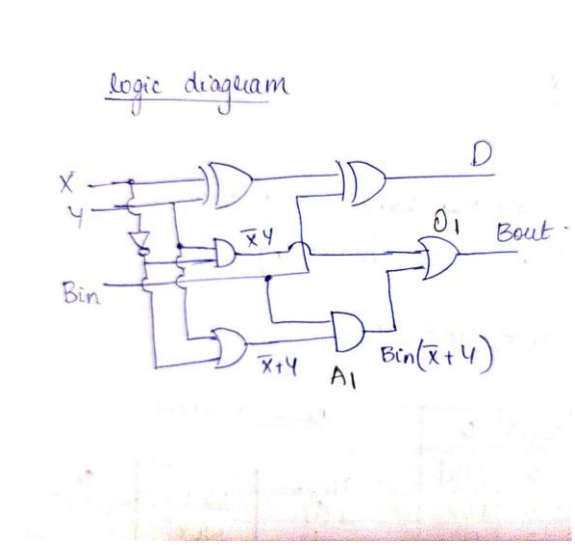
1. Verilog code and testbench to design and simulate a Full subtractor using a) data flow, b) behavioral and c) mixed style modelling.

We design a full adder with 1-bit inputs X,Y and borrow from previous unit, Bin and outputs difference D and borrow out Bout. The truth table and Boolean equations are given below:



According to the Boolean equations, the logic diagram of a full adder circuit is drawn as:

Full subtractor circuit using logic gates:

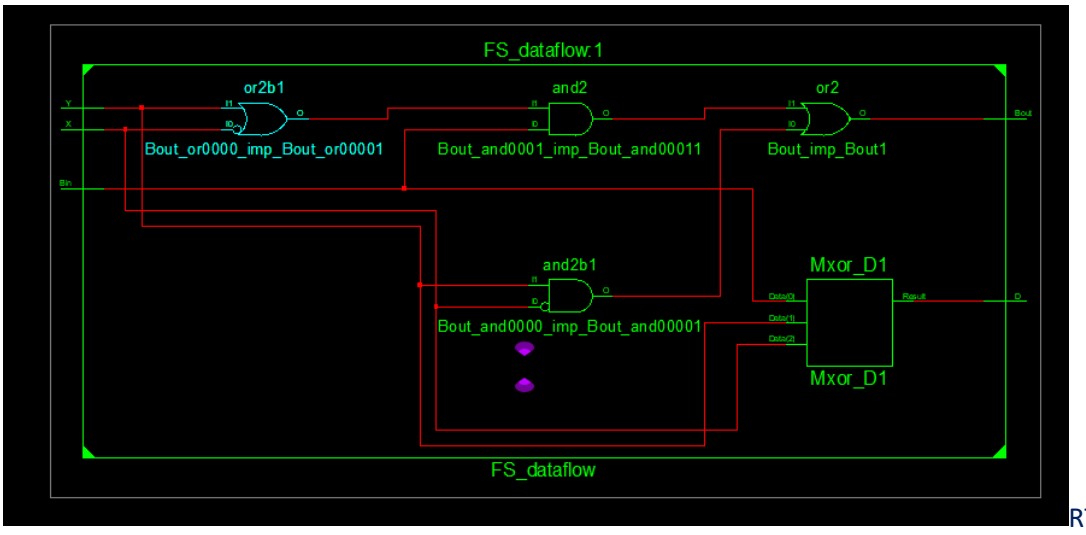


(a) Data Flow modelling

In data flow modelling, we design the Verilog module using the assign statements

(i)Code:

```
`timescale 1ns / 1ps
module FS_dataflow(input X, input Y,input Bin,output D, output Bout );
assign #1 D=(X^Y)^Bin;
assign #2 Bout=(~X&Y)|(Bin&(~X|Y));
endmodule
```



RTL Schematic

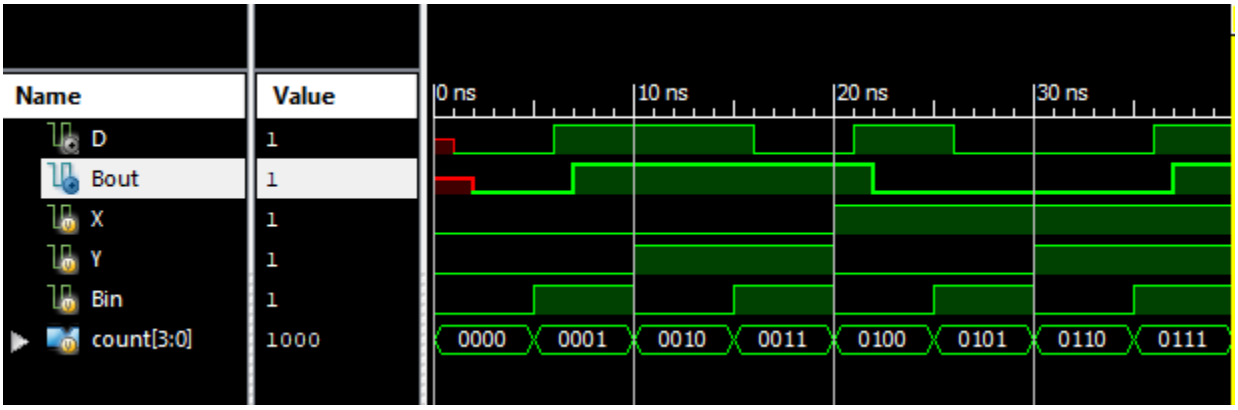
(ii)Test bench

```
`timescale 1ns / 1ps
module FS_test;
// Inputs
reg X;
reg Y;
reg Bin;
reg [3:0]count;
// Outputs
wire D;wire Bout;
// Instantiate the Unit Under Test (UUT)
FS_mixed uut (.X(X), .Y(Y), .Bin(Bin), .D(D), .Bout(Bout));

	initial begin
	// Initialize Inputs
	X = 0;Y = 0;Bin = 0;
		for(count=0;count<8;count=count+1)
		begin
		{X,Y,Bin}=count;
		#5
		$display("$Time:%t::X=%b,Y=%b,Bin=%b::D=%b,Bout=%b",$time,X,Y,Bin,D,Bout);
		end
	$finish;
	end
endmodule
```

(iii) Results

```
Console
ISim P.58f (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
$Time:          5000::X=0,Y=0,Bin=0::D=0,Bout=0
$Time:          10000::X=0,Y=0,Bin=1::D=1,Bout=1
$Time:          15000::X=0,Y=1,Bin=0::D=1,Bout=1
$Time:          20000::X=0,Y=1,Bin=1::D=0,Bout=1
$Time:          25000::X=1,Y=0,Bin=0::D=1,Bout=0
$Time:          30000::X=1,Y=0,Bin=1::D=0,Bout=0
$Time:          35000::X=1,Y=1,Bin=0::D=0,Bout=0
$Time:          40000::X=1,Y=1,Bin=1::D=1,Bout=1
Stopped at time : 40 ns : File "I:/xilinxfiles/FS_dataflow/FS_test.v" Line 57
ISim>
```

Discussion: The below is the waveforms of the full adder circuit constructed using data flow modelling .It can be observed that the delays given to D (1 unit time delay) and Bout (2 units time delay) are reflectef in the waveform. For example at t=5ns Bin becomes 1, however the same is reflected in D at t=6ns and in Bout at t=7ns.

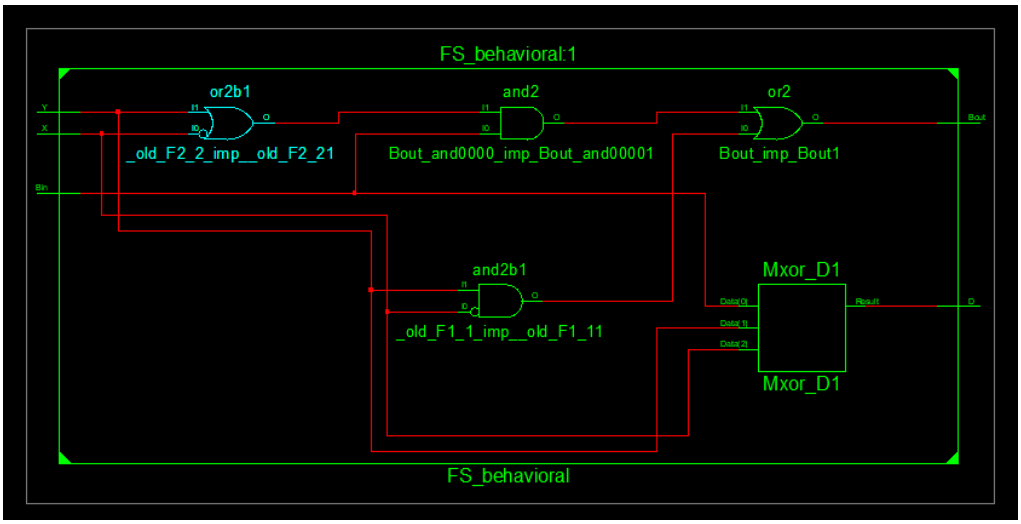


(b)Behavioral modelling

(i)CODE

```
`timescale 1ns / 1ps
module FS_behavioral(input X,  input Y, input Bin,output reg d, output reg Bout  );
reg F1,F2;
always@(X,Y,Bin)
```

```
begin
d= #1(X^Y)^Bin;
F1=~X&Y;
F2=~X|Y;
Bout= #1 F1|(Bin&F2);
end
endmodule
```

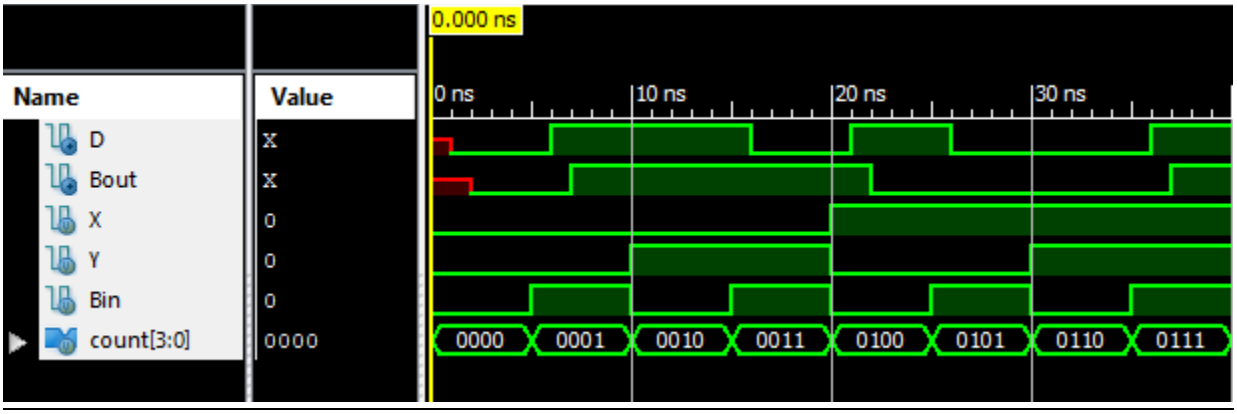


RTL SChematic

The same test bench used for data flow modelling is used for behavior modelling. Only the module name is modified. The results are as follows:

(ii)RESULTS

```
Console
ISim P.58f (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
$Time:          5000::X=0,Y=0,Bin=0::D=0,Bout=0
$Time:         10000::X=0,Y=0,Bin=1::D=1,Bout=1
$Time:         15000::X=0,Y=1,Bin=0::D=1,Bout=1
$Time:         20000::X=0,Y=1,Bin=1::D=0,Bout=1
$Time:         25000::X=1,Y=0,Bin=0::D=1,Bout=0
$Time:         30000::X=1,Y=0,Bin=1::D=0,Bout=0
$Time:         35000::X=1,Y=1,Bin=0::D=0,Bout=0
$Time:         40000::X=1,Y=1,Bin=1::D=1,Bout=1
Stopped at time : 40 ns : File "I:/xilinxfiles/FS_dataflow/FS_test.v" Line 5
ISim>
```

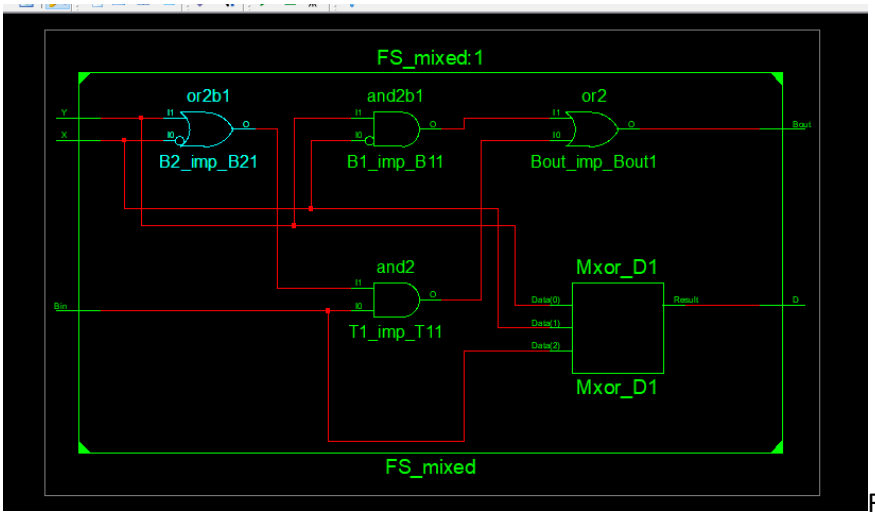


Discussion:It can be observed from the waveforms that, though D is given a delay of 1ns and Bout is given a delay of 1 ns, due to the use of blocking statements, Bout changes after a delay of 2ns as the delay of D also gets added since D preceeds Bout.

(c) Mixed Modelling

(i)CODE:

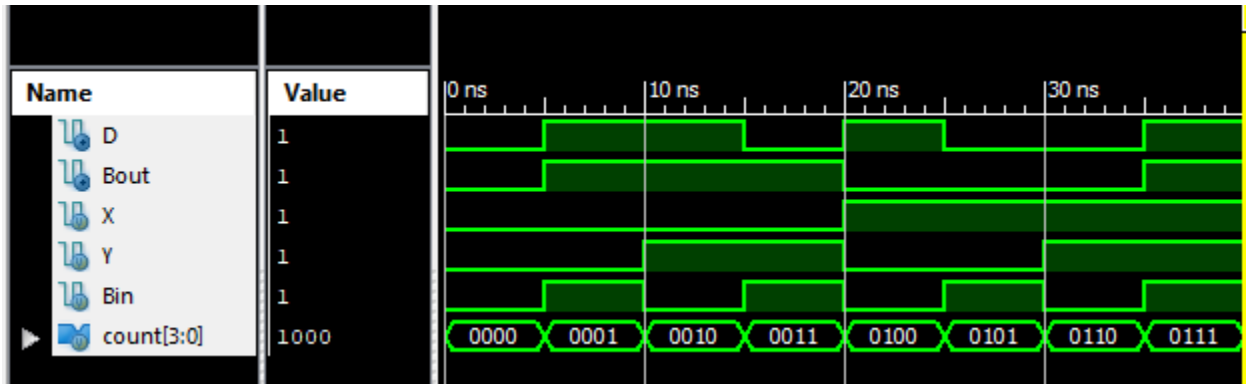
```
module FS_mixed(  input X, input Y,input Bin,output D,output Bout );
        reg B1,B2,D1;
        wire T1;
        always@(X,Y,Bin)
        begin
                D1=X^Y;
                B1=~X&Y;
                B2=~X|Y;
        end
        assign D=D1^Bin;
        and A1 (T1,Bin,B2);
        or O1 (Bout,T1,B1);
        endmodule
```



RTL Schematic

The simulation results after using the same test bench after modifying the module name are as follows:

```
Console
ISim P.58f (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
$Time:          5000::X=0,Y=0,Bin=0::D=0,Bout=0
$Time:          10000::X=0,Y=0,Bin=1::D=1,Bout=1
$Time:          15000::X=0,Y=1,Bin=0::D=1,Bout=1
$Time:          20000::X=0,Y=1,Bin=1::D=0,Bout=1
$Time:          25000::X=1,Y=0,Bin=0::D=1,Bout=0
$Time:          30000::X=1,Y=0,Bin=1::D=0,Bout=0
$Time:          35000::X=1,Y=1,Bin=0::D=0,Bout=0
$Time:          40000::X=1,Y=1,Bin=1::D=1,Bout=1
Stopped at time : 40 ns : File "I:/xilinxfiles/FS_dataflow/FS_test.v" Line 57
ISim>
```

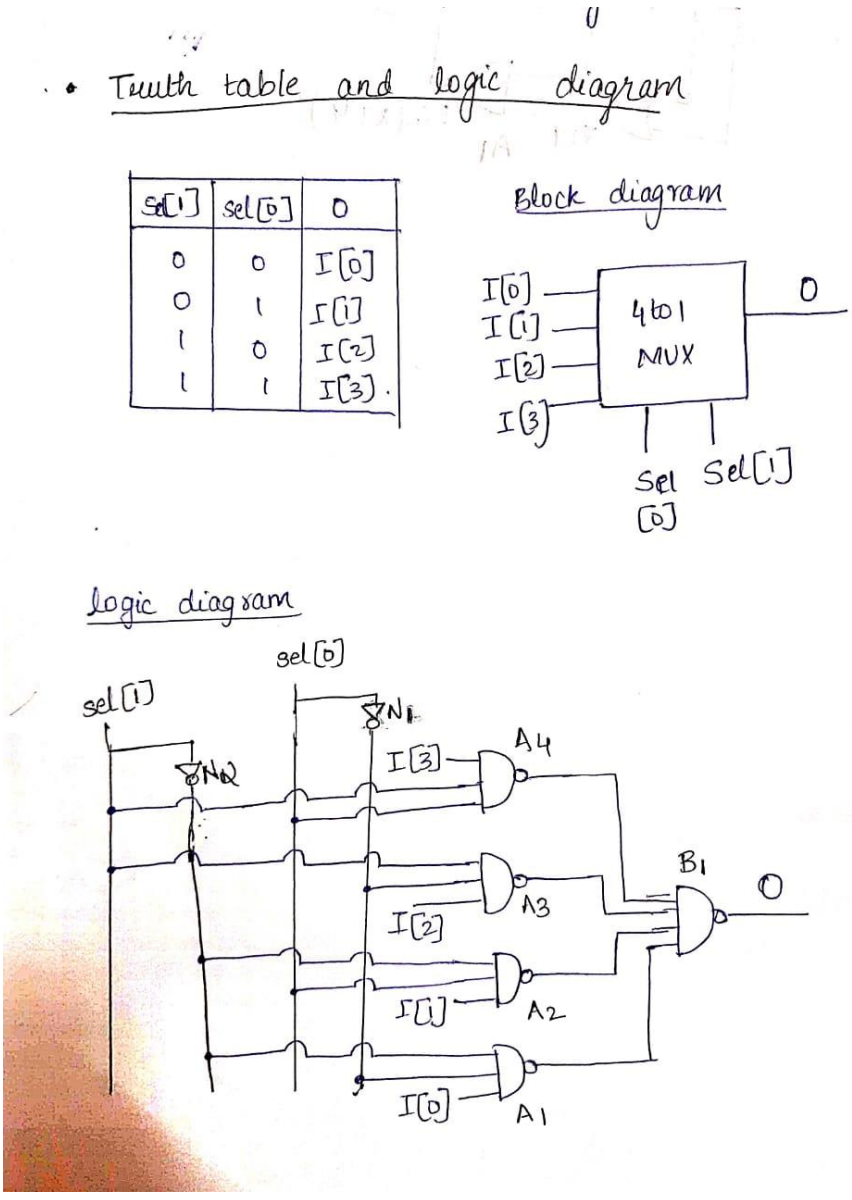


Discussion: As we do not introduce any delay to the module implementation, the delay is taken as 0 as default by the simulation tool.However, while implementing on hardware delays depend on the technology used and the implementation. It can also be observed that the schematic is different from

data flow modelling as in mixed, we have defined intermediate steps using behavioral modelling and structural modelling. Hence RTL schematic is generated accordingly

2. Verilog code and testbench to design and simulate 4:1 mux using a) data flow and b) structural (gate level) modelling.

Inputs are an input bus with three inputs I[0], I[1], I[2] and I[3] , slelect lines sel[1] and sel[0] and output O

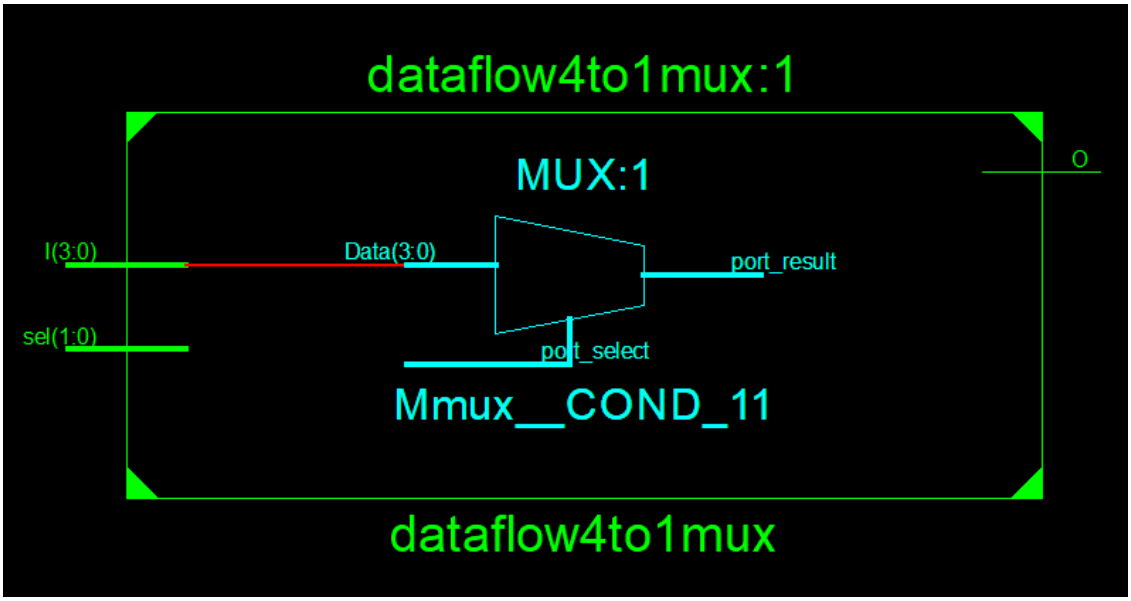


(a) Data Flow modelling

(i) CODE

```
`timescale 1ns / 1ps
module dataflow4to1mux(
    input [3:0] I,
    output O,
    input [1:0] sel
    );
assign O = I[sel];
endmodule
```

RTL Schematic:



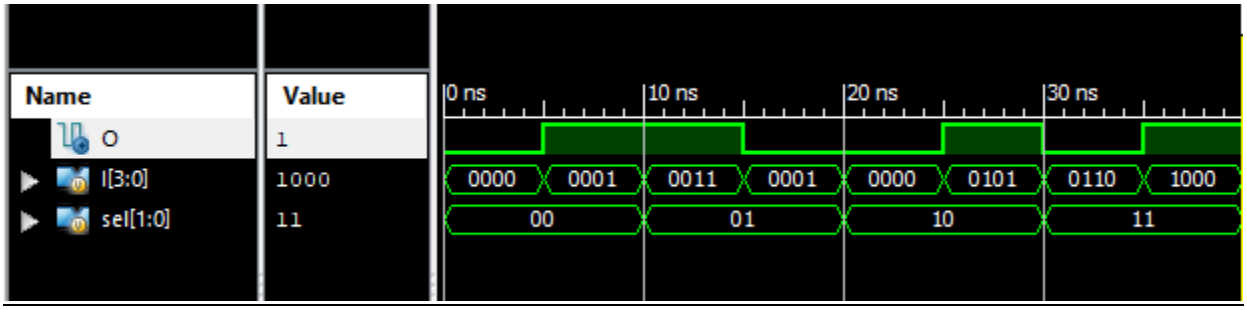
(II)TESTBENCH

```
`timescale 1ns / 1ps
module mux4to1test;
// Inputs
reg [3:0] I;reg [1:0] sel;
```

```
// Outputs
wire O;
// Instantiate the Unit Under Test (UUT)
MUX4to1structural uut (.I(I), .O(O), .sel(sel));
Initial begin
// Initialize Inputs
I = 0;sel = 0;
#5 I = 1;sel = 0;
#5 I = 3;sel = 1;
#5 I = 1;sel = 1;
#5 I = 0;sel = 2;
#5 I = 5;sel = 2;
#5 I = 6;sel = 3;
#5 I = 8;sel = 3;
end
initial
$monitor ("I1=%b,I2=%b,I3=%b,I4=%b,sel=%d, O=%b",I[0],I[1],I[2],I[3],sel,O);
Initial begin
#40 $finish;
end
endmodule
```

RESULTS:

```
Console
ISim P.58f (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
I1=0,I2=0,I3=0,I4=0,sel=0, O=0
I1=1,I2=0,I3=0,I4=0,sel=0, O=1
I1=1,I2=1,I3=0,I4=0,sel=1, O=1
I1=1,I2=0,I3=0,I4=0,sel=1, O=0
I1=0,I2=0,I3=0,I4=0,sel=2, O=0
I1=1,I2=0,I3=1,I4=0,sel=2, O=1
I1=0,I2=1,I3=1,I4=0,sel=3, O=0
I1=0,I2=0,I3=0,I4=1,sel=3, O=1
Stopped at time : 40 ns : File "I:/xilinxfiles/MUX4to1/mux4to1test.v" Line 62
ISim>
```

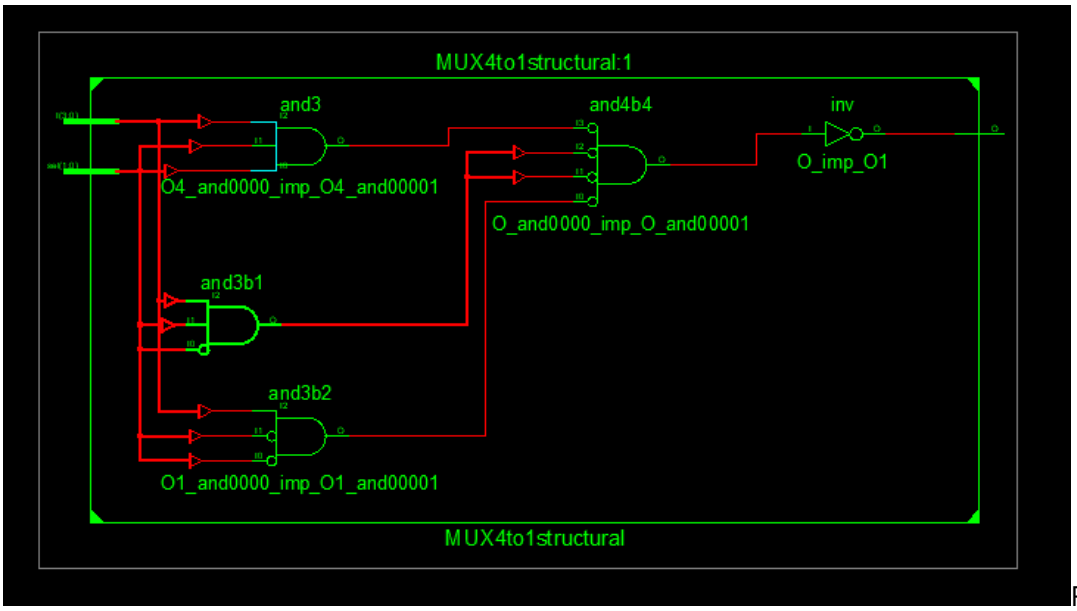


Discussion: As no delays have been mentioned, zero delay is assumed by the simulator. Also when variable input is assigned to the output in data flow modelling, a MUX is implemented by ISE tool.

(a) Structural modelling

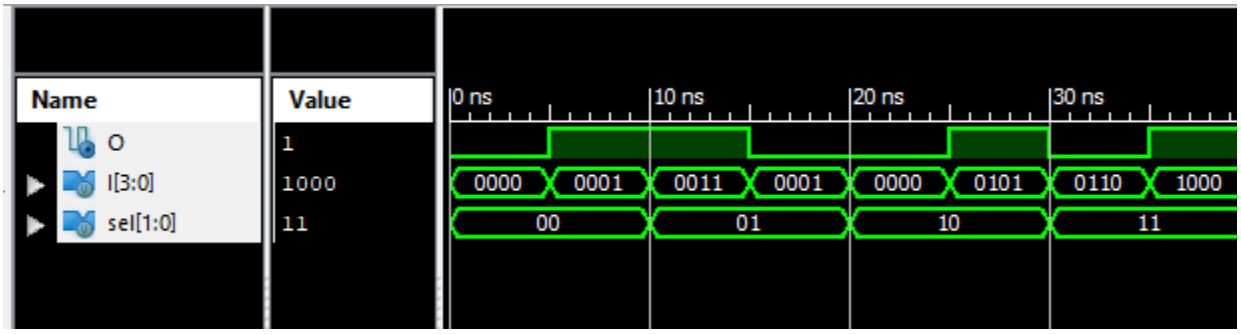
(i) CODE

```
`timescale 1ns / 1ps

module MUX4to1structural(input [3:0] I,  input [1:0] sel, output O  );

wire O1,O2,O3,O4,NS0,NS1;

not N1(NS0,sel[0]);

not N2(NS1,sel[1]);

nand A1 (O1,NS0,NS1,I[0]);

nand A2 (O2,sel[0],NS1,I[1]);

nand A3 (O3,NS0,sel[1],I[2]);

nand A4 (O4,sel[0],sel[1],I[3]);

nand B1 (O,O1,O2,O3,O4);

endmodule
```



RTL Schematic

```
ISim P.58f (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
I1=0,I2=0,I3=0,I4=0,sel=0, O=0
I1=1,I2=0,I3=0,I4=0,sel=0, O=1
I1=1,I2=1,I3=0,I4=0,sel=1, O=1
I1=1,I2=0,I3=0,I4=0,sel=1, O=0
I1=0,I2=0,I3=0,I4=0,sel=2, O=0
I1=1,I2=0,I3=1,I4=0,sel=2, O=1
I1=0,I2=1,I3=1,I4=0,sel=3, O=0
I1=0,I2=0,I3=0,I4=1,sel=3, O=1
```



Discussion: The delays are again considered to be zero. However in structural modelling, since gates are specified, it can be observed that the RTL schematic is as specified in the module. Hence structural modelling gives more control to the designer.

CONCLUSION:

Full subtractor was designed using dataflow, behavioral and mixed modelling and the results have been verified using a test bench. The outputs for different inputs have been listed in the console and

the waveforms have been generated along with RTL schematic for each. The delays have been discussed along with the schematics for the different modelling techniques.

4 to 1 MUX has been generated using data flow and structural modelling. Results were verified by generating output to selected inputs. RTL schematics for the both techniques have been compared. It is found that structural modelling creates a schematic as specified by the programmer and hence gives more control to the designer.