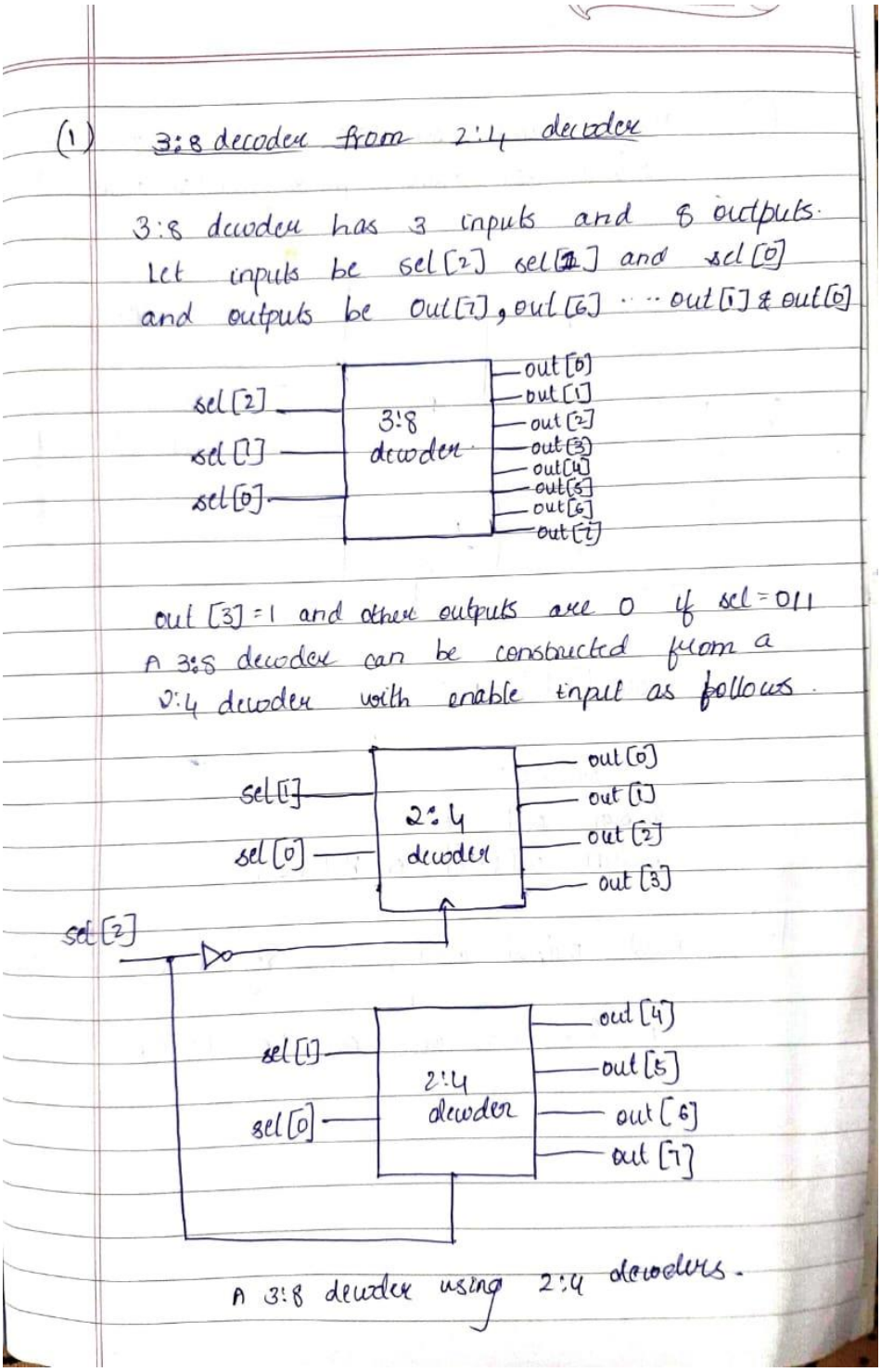
1)3:8 Decoder from 2:4 decoder



Codes:

Module 1: 2to4 decoder

```
`timescale 1ns / 1ps
module decoder_2to4(
    input en,
    input [1:0] sel,
    output [3:0] out
    );
assign out[0]=en&~sel[0]&~sel[1];
assign out[1]=en&sel[0]&~sel[1];
assign out[2]=en&~sel[0]&sel[1];
assign out[3]=en&sel[0]&sel[1];
endmodule
```

Module 1: 3to8 decoder

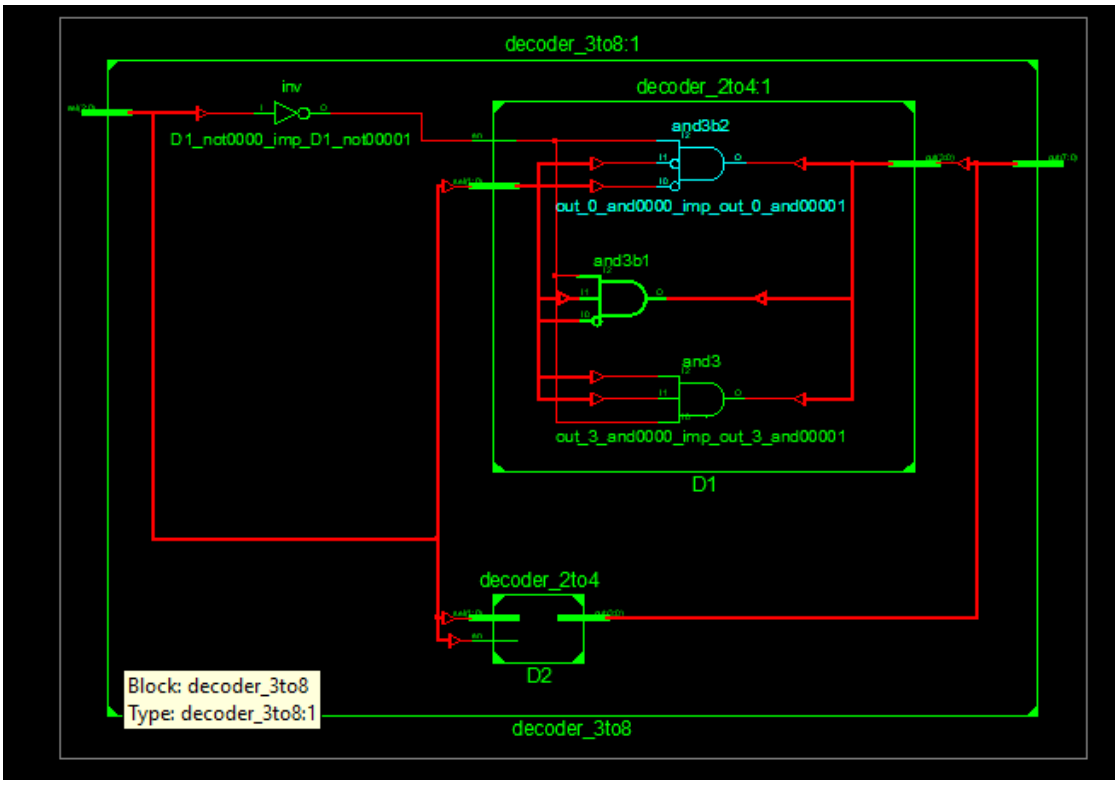
```
`timescale 1ns / 1ps
module decoder_3to8(  input [2:0] sel,
    output [7:0] out );
decoder_2to4 D1(~sel[2],sel[1:0],out[3:0]);
decoder_2to4 D2(sel[2],sel[1:0],out[7:4]);

endmodule
```

Module Testbench:

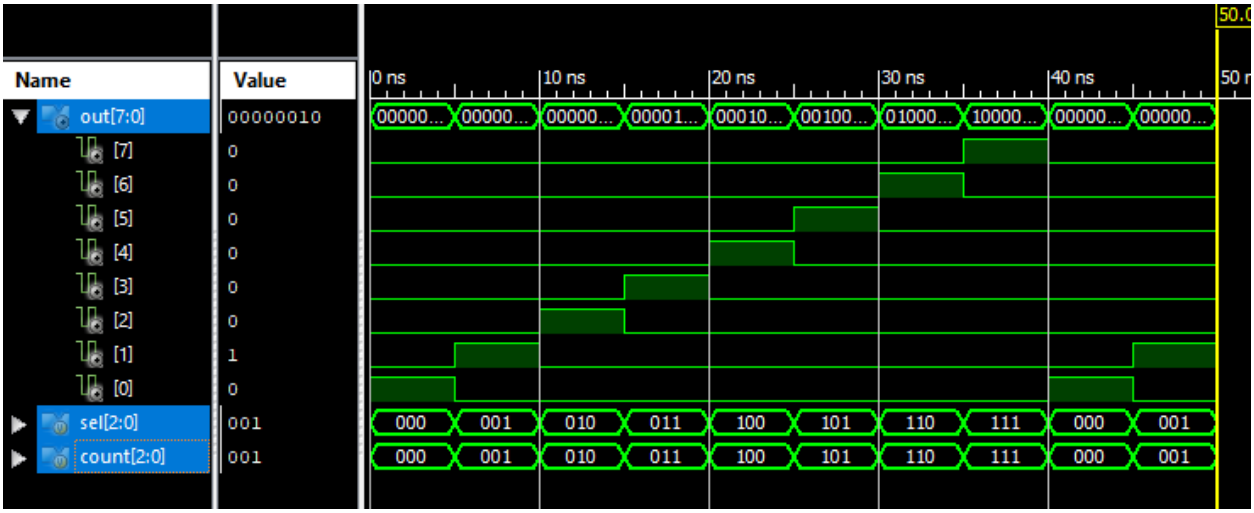
```
`timescale 1ns / 1ps
module test_3to8;
// Inputs
            reg [2:0] sel;reg [2:0] count;
// Outputs
```

```
        wire [7:0] out;
// Instantiate the Unit Under Test (UUT)
        decoder_3to8 uut ( .sel(sel), .out(out));

        initial begin
                // Initialize Inputs
                for(count=0;count<8;count=count+1)
                        begin
                        sel=count;
                        #5;
                        end
        end

        //monitoring output
        initial
        $monitor("sel=%b,out=%b",sel,out);
        initial
        #50 $finish;

endmodule
```

RTL Schematic:




```
ISim P.58f (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
sel=000,out=00000001
sel=001,out=00000010
sel=010,out=00000100
sel=011,out=00001000
sel=100,out=00010000
sel=101,out=00100000
sel=110,out=01000000
sel=111,out=10000000
sel=000,out=00000001
sel=001,out=00000010
Stopped at time : 50 ns : File "I:/xilinxfiles/decoder_3to8_from2to4/test_3to8.v" Line 53
ISim>
```



Discussion: In the above circuit, en is used as the third input to build a 3:8 decoder form 2:4 decoders. Output follows select according to the equation out[sel]=en .However the same assignment could not be used in the module as Verilog generates an error when output is assigned a variable index. So we assign each bit of input seperately using data flow assignment.