Design Implementation of Compound Subthreshold Source-Coupled Logic

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28 February 2022

Abstract

In this paper, I am going to design and Implement compound Source-Coupled Logic gates with merging an AND gate and an XOR gate in a

single gate which can provide the possibility of reducing the circuit power consumption and improving the speed of

$$\tau_{\text{tot},A} \approx N \times \frac{V_{\text{SW}} C_L}{I_{\text{SS}}}$$

operation simultaneously. Using this technique, it is possible to have only one pair of output load devices and also only one single tail bias transistor, and hence reduce the area in addition to halving the total current consumption. Assuming that the time constant at the output nodes of each SCL gate is equal to then the total equivalent time constant of a simple N stage SCL gate will be:

$$\tau_L = R_L C_L = \frac{V_{\text{SW}} C_L}{I_{\text{SS}}}$$

Reference Circuit Details

Implementation of Compound STSCL gate (AND operation followed by XOR gate). In this approach, it is necessary to make sure that the stacking of *M* differential pair stages will not affect the correct current switching behaviour of the circuit. In other words, with *M* stacked transistors, the differential pair transistors should be able to switch the current completely to one of the output branches with the specified input voltage swing, VSW. As in this case, there are M series transistors, it is possible to show that the inversion coefficient, IC, of ON

$$IC = \frac{I_{\text{SS}}}{2n_n \mu_n C_{\text{ox}} \frac{W_N}{M \times L_N} U_T^2} = \frac{M \times I_{\text{SS}}}{2n_n \mu_n C_{\text{ox}} \frac{W_N}{L_N} U_T^2}.$$

transistors based on the EKV model would be:

This equation implies that W_N /L_N (aspect ratio of differential NMOS transistors) should be large enough to keep their inversion coefficients small and make sure that VSW is sufficient to switch the tail bias current to one of the output branches: which puts an upper limit on M and should be taken into

$$M \leq IC \cdot \frac{2n_n \mu_n C_{\text{ox}} \frac{W_N}{L_N} U_T^2}{I_{\text{SS}}}$$

account in design of stacked topologies.

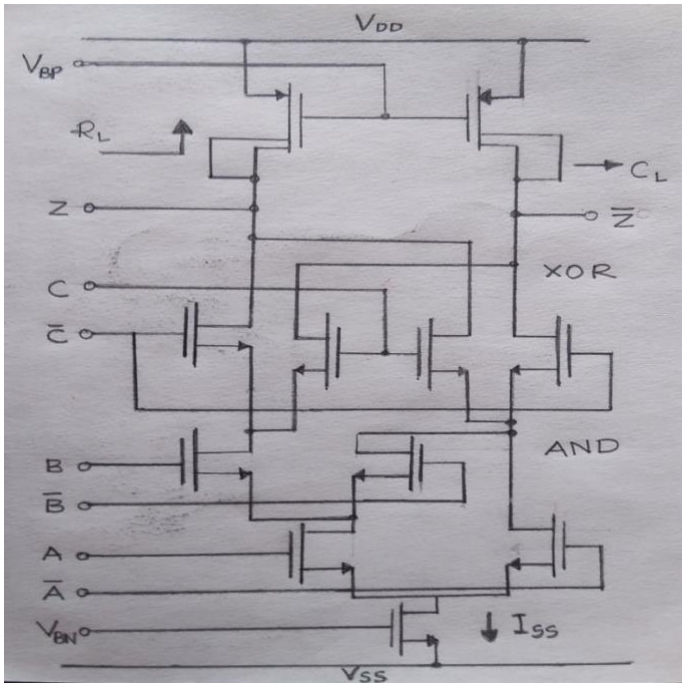

Figure 01 : Reference Circuit Diagram

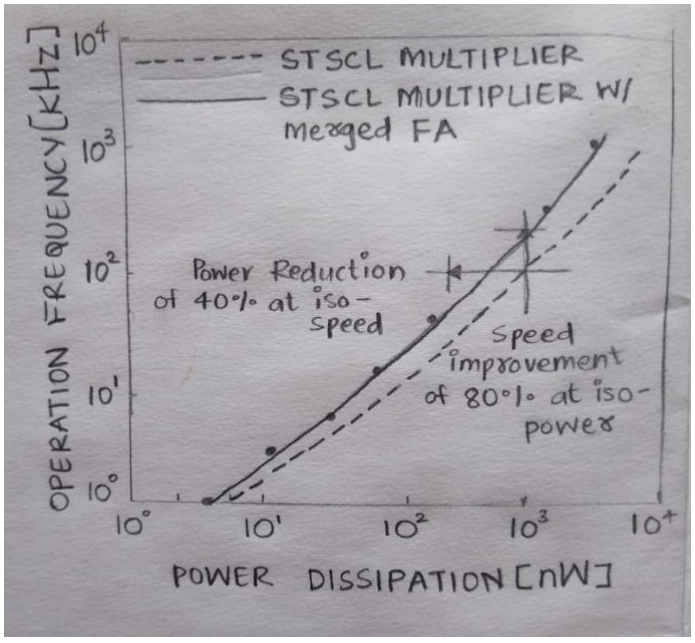

Figure 02 : Reference Waveform

References

A. Tajalli and Y. Leblebici, Extreme Low-Power Mixed Signal IC Design: Subthreshold Source-Coupled Circuits, DOI 10.1007/978-1-4419-6478-6 11, -c Springer Science + Bussiness Media, LLC 2010