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ARTICLE

An Optimisation Based Study of Underlap Architecture of Sub 16 nm Double Gate MOSFET for Enhanced Analog Performance

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ABSTRACT

This paper shows a comparative study of 14 nm Underlap Double Gate (U-DG) NMOSFET with gate stack (GS) with varying underlap length. In highly scaled devices underlap is used to minimize Short Channel Effects (SCEs) as a cost of reduced on current. Hence underlap length has been optimized with the help of on current to off current ratio (I_{ON}/I_{OFF}) and Drain Induced Barrier Lowering (DIBL). In this paper the Analog performance comparison of devices with various underlap length has been shown, considering the drain current (I_D), the transconductance (g_m), the transconductance generation factor (g_m/I_D), the intrinsic gain (g_mR_0). It is observed that the device with lowest underlap offers 35.4% better drain current but provides poor SCE performances than that of the device with highest underlap. The later offers 41% less DIBL and 85% better I_{ON}/I_{OFF}. The performance of single stage amplifier using the devices is also analyzed with the help of Voltage Transfer Characteristics (VTC) and Gain Bandwidth product (GBW) in this paper.

KEYWORDS: Underlap, GateStack, DIBL, Analog Performance, Single Stage Amplifier, Gain Bandwidth Product (GBW).

1. INTRODUCTION

The present VLSI trend has got a new wing as it is stormed into nanometerrealm. Scaling down of the device although increase the on current (I_{ON}) but it also leads to Short Channel Effects (SCEs)[1] such as Drain Induced Barrier Lowering (DIBL), Gate Induced Drain Leakage (GIDL) etc.[2–4] The Symmetric Underlap Double Gate NMOSFET (U-DG NMOSFET) has emerged as a potential solution for the SCEs. It minimizes the GIDL as well as fringing capacitances though DIBL is high for the lesser underlap lengths. Underlap also produces channel resistance which in turn reduces the I_{ON}. Hence, the underlap length must be optimized for desired functioning of the device.[5]

Demands of speed with low power consumption for System on Chip (SoC) applications have been the prime focus of today's research. Hence high I_{ON} is the essential to achieve the aforementioned objective. Therefore, the gate oxide thickness (t_{ox}) scaling is required to increase the gate oxide capacitance (C_{ox}), which in turn increases the I_{ON} of the device. However, with the decreasing of t_{ox}, gate quantum mechanical tunnelling phenomenon comes into effect for thin gates which leads to gate leakage[1, 6, 7] as oxide thickness of about 1.2 nm is necessary for proper control of gate tunnelling.[8] This problem is mitigated by replacing silicon dioxide (SiO_2) with *high-k* dielectrics like HfO_2, Al_2O_3 as gate insulators.[9] However, the presence of interface traps and severe scattering at the *high-k* silicon junction causes a decrease in the mobility of the carriers, thus in the I_{ON} as well.[10] This setback is eliminated by the usage of a thin layer of SiO_2 padding since the junction between silicon and its oxide provides minimum interface traps and hence, resulting in minimum scattering. This arrangement is known as GateStack (GS).[6, 11]

This paper shows analog performance studies of 14 nm U-DG-GS NMOSFET for varying underlap length with respect to the drain current (I_D), the transconductance (g_m), the transconductance generation factor (g_m/I_D), the intrinsic gain (g_mR_0), and performance of single stage amplifier circuit implementing the abovementioned devices has studied. In the Section 2 the device specification and simulation undertaken will be discussed. In the Section 3 the analog comparisons has been presented. In the Section 4

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