	Marwadi University **Faculty of Engineering & Technology** **Department of Information and Communication Technology**	
Subject: Digital Electronics (01EC0102)	**Aim:** Configure various code converters. a)Binary to Gray code b) Gray to Binary code	
Experiment No: 7	**Date:12/03/2025**	**Enrollment No:92400120535**

Aim: Configure various code converters. a) Binary to Gray code b) Gray to Binary code

Software: Deldsim

https://www.deldsim.com/circuit/C58/design--implement-3-bit-binary-to-gray-code-converter-using-ic--74ls138--using-74ls138-74ls20/

https://www.deldsim.com/circuit/C71/3-bit-gray-to-binary-code-conversion-using-74ls86/

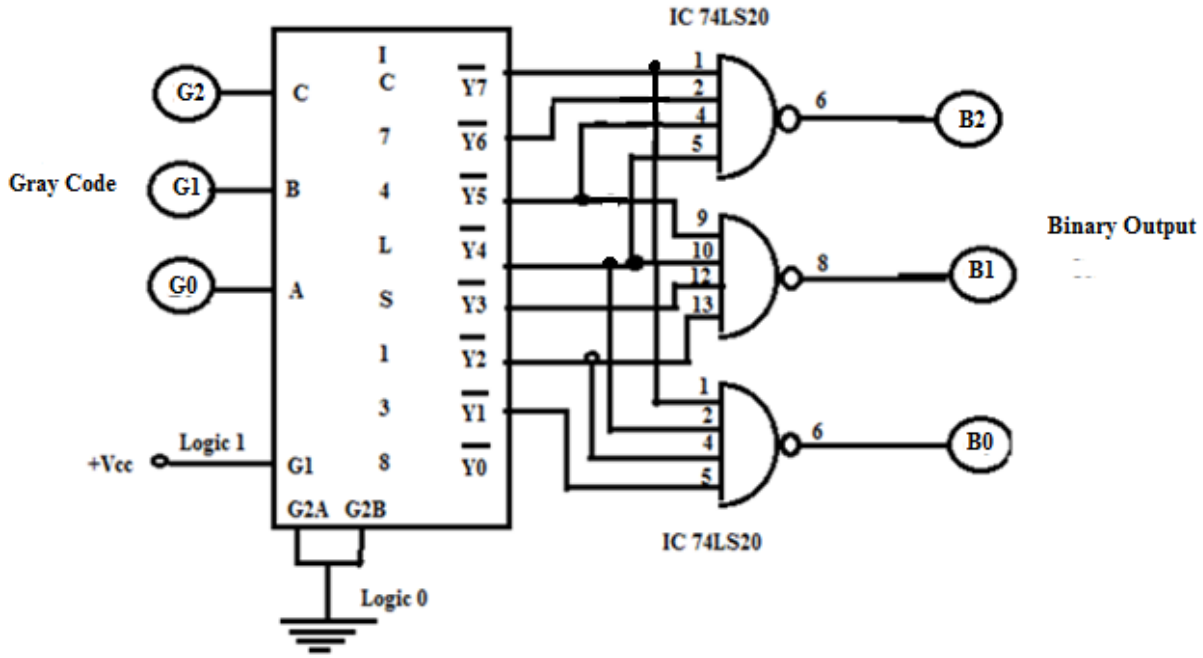
Theory:

The formula for converting a 3-bit binary number to Gray code is:

G2=B2
G1=B2⊕B1
G0=B1⊕B0

Where:

B2,B1,B0 are the binary bits.
G2,G1,G0 are the corresponding Gray code bits.



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The 74LS138 is a 3-to-8 line decoder with three binary inputs. It decodes the 3-bit binary input into one of 8 output lines. Each output line corresponds to one possible combination of the binary input. Here's how the IC works:

- The 3 binary input lines (let's call them B2,B1,B0) determine which one of the 8 output lines gets activated.
- The outputs of the IC will correspond to the Gray code combination.

However, the 74LS138 doesn't directly output Gray code, so we'll need to manipulate the decoded lines from the IC using logic gates (XOR gates) to generate the Gray code output.

Procedure:

Step 1: Open DELDSim

- Open DELDsim and create a new project for the design.

Step 2: Place IC-74LS138 Decoder

- From the component library in DELDSim, select the 74LS138 IC (3-to-8 line decoder).
- Place the IC on the workspace.

Step 3: Connect the Binary Inputs (B2, B1, B0)

- Use 3 input switches to simulate the 3-bit binary input.
- Connect these switches to the input pins of the 74LS138 IC.
  - B2 connects to pin 6 (A).
  - B1 connects to pin 7 (B).
  - B0 connects to pin 8 (C).

Step 4: Use Logic Gates (XOR gates) for Gray Code Conversion

- You need to implement the Gray code logic using XOR gates:
  - Gray code bit G2 is directly the same as B2.
  - Gray code bit G1 is $B2 \oplus B1$
  - Gray code bit G0 is $B1 \oplus B0$
- Place 2 XOR gates on the workspace:
  - The first XOR gate takes B2 and B1 as inputs to generate G1.
  - The second XOR gate takes B1 and B0 as inputs to generate G0.

  The outputs of the XOR gates will be the Gray code bits G1 and G0.

Step 5: Connect IC-74LS138 Outputs

- The 74LS138 IC will decode the 3-bit binary input into one of the 8 output lines:
  - Y0 to Y7 are the output lines.
- Since the IC decodes the binary inputs, you can use outputs Y2,Y3,Y6,Y7 to help generate the Gray code bits for G2,G1,G0. The output lines will correspond to the different combinations of the binary input.

Step 6: Display the Gray Code Output

- Use LEDs or 7-segment displays to show the Gray code output (G2, G1, G0).
  - Connect the Gray code outputs (G2, G1, G0) to the LEDs.

Step 7: Run the Simulation

- Once everything is connected (inputs, IC, XOR gates, and outputs), you can now run the simulation.
- Flip the input switches to different binary values and check the corresponding Gray code output on the LEDs.

Gray to Binary Code Conversion Logic

The logic to convert a 3-bit Gray code G2,G1,G0 to a Binary code B2,B1,B0 is as follows:

- B2=G2 (The most significant bit of the binary is the same as the most significant bit of the Gray code)
- B1=G1⊕B (The second binary bit is the XOR of the second Gray code bit and the first binary bit)
- B0=G0⊕B1 (The least significant binary bit is the XOR of the third Gray code bit and the second binary bit)

In this conversion, the 74LS86 XOR gates will be used to implement the XOR logic required for B1 and B0.

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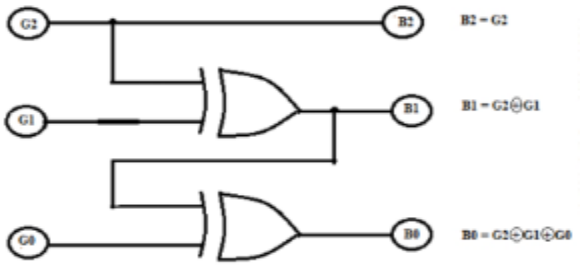

Procedure:

Step 1: Start DELDSim

- Open DELDsim and create a new project for the design.

Step 2: Place the 74LS86 IC

- From the component library in DELDSim, select the 74LS86 IC (Quad 2-input XOR gate).
- Place the IC on the workspace.

Step 3: Create the 3-bit Gray Code Input

- Use 3 input switches to simulate the 3-bit Gray code inputs.
  - Label these switches as G2, G1, and G0 for the 3-bit Gray code input.

Step 4: Connect the Gray Code Inputs to XOR Gates

- For Gray to Binary Conversion:
  - B2=G2,B2=G2: The most significant bit of binary is directly the same as the Gray code MSB.
  - B1=G1⊕B2 Use the XOR gate to calculate B1, which is the XOR of G1 and B2.
  - B0=G0⊕B1 Use another XOR gate to calculate B0, which is the XOR of G0 and B1.

Step 5: Implement XOR Gate Logic Using 74LS86

- The 74LS86 IC has 4 XOR gates, each with 2 inputs. You can use these gates for the conversion logic.
  - Gate 1: Connect G2 to B2. This is direct, so no XOR needed.
  - Gate 2: Connect G1 and B2 (from Gate 1 output) to calculate B1.
  - Gate 3: Connect G0 and B1 (from Gate 2 output) to calculate B0.

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Step 6: Connect the XOR Gates

- For B2: Directly connect G2 to the output.
- For B1: Connect G1 to one input of the second XOR gate and the output of the first XOR gate (which is B2) to the other input.
- For B0: Connect G0 to one input of the third XOR gate and the output of the second XOR gate (which is B1) to the other input.

Step 7: Display the Binary Code Output

- Use 3 LEDs or 7-segment displays to show the resulting Binary output B2, B1, and B0.
    - Connect the outputs from the XOR gates (B2, B1, and B0) to the LEDs.

Step 8: Run the Simulation

- After connecting all the components (Gray code inputs, XOR gates, and binary output displays), run the simulation.

Flip the Gray code input switches

- o different values and observe the corresponding Binary code output on the LEDs.

Screenshots

Marwadi University Marwadi Chandarana Group NAAC A+	**Marwadi University** **Faculty of Engineering & Technology** **Department of Information and Communication Technology**	
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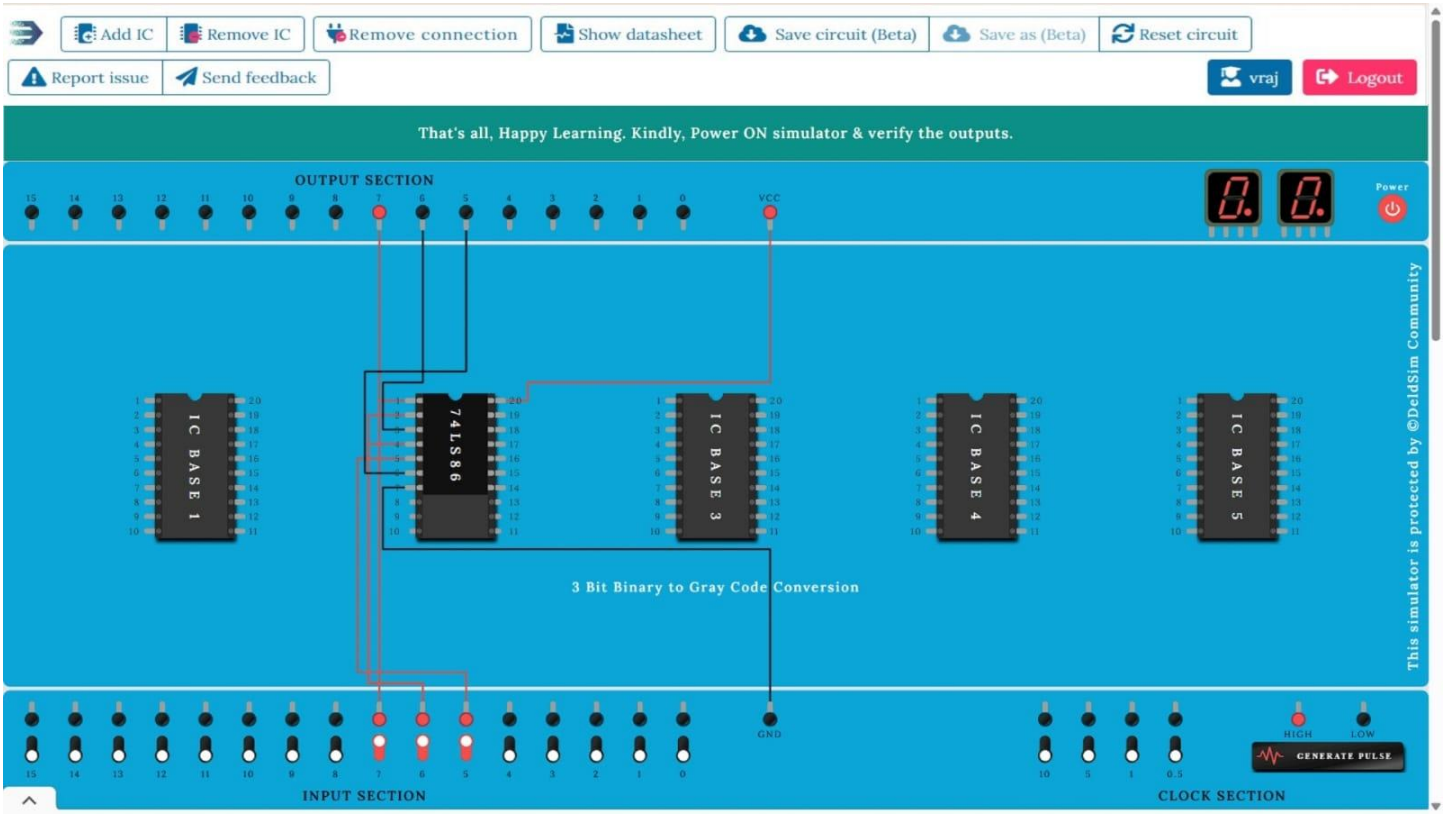
a) Binary to Gray code



Marwadi University Marwadi Chandarana Group NAAC A+	**Marwadi University** **Faculty of Engineering & Technology** **Department of Information and Communication Technology**	
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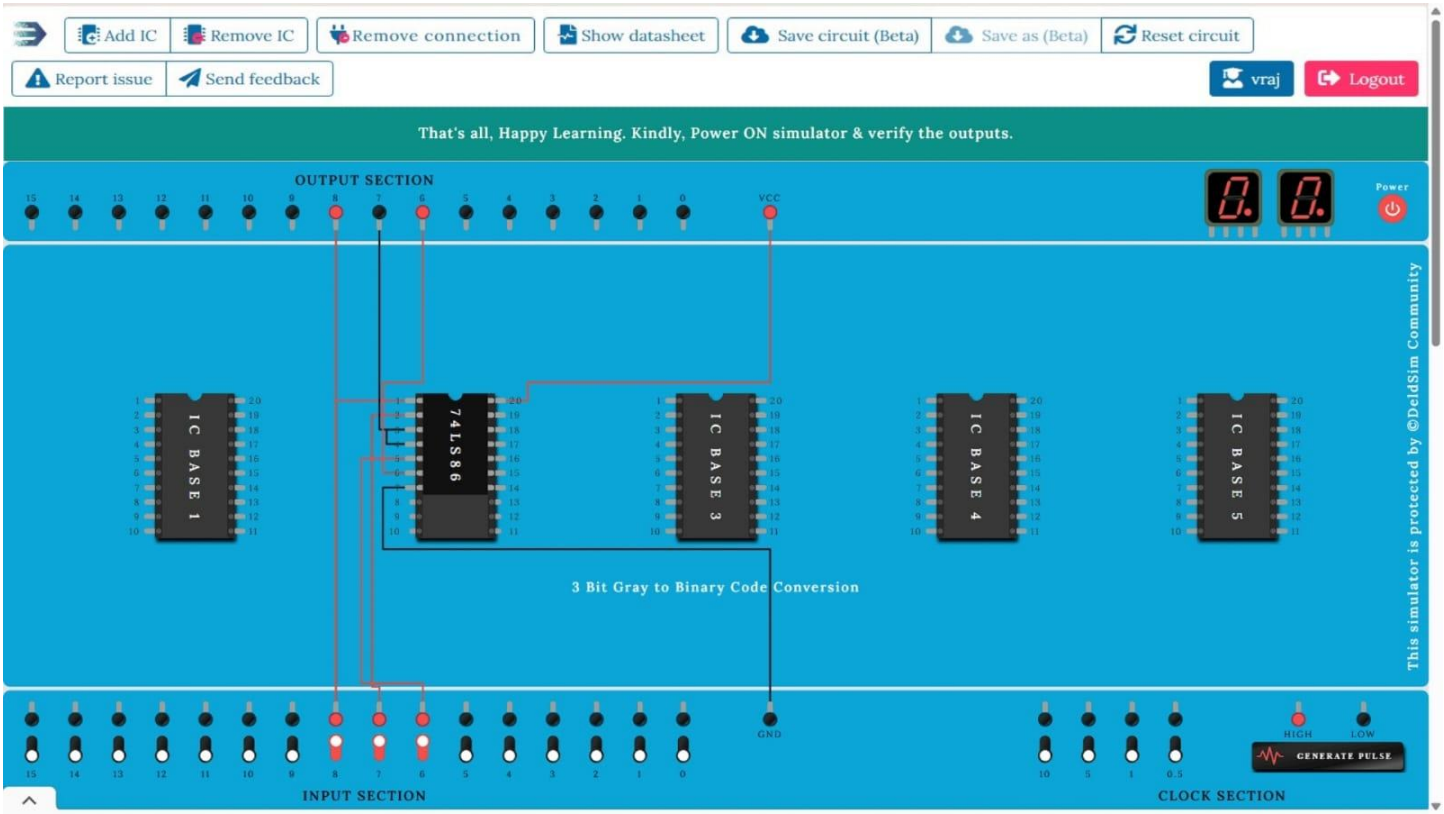
b) Gray to Binary code



Conclusion:

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POST LAB EXERCISE

1. What is the Gray code equivalent of the 3-bit binary number 101?

a) 111
b) 100
c) 110
d) 101

Answer: b) 100

2. In a 3-bit Gray code, what is the Gray code equivalent of the binary number 011?

a) 010
b) 011
c) 100
d) 001

Answer: a) 010

3. What is the binary equivalent of the 3-bit Gray code 110?

a) 111
b) 101
c) 100
d) 010

Answer: b) 101

4. Which of the following is true for converting binary to Gray code?

a) Gray code is obtained by applying XOR operation between consecutive bits of binary.
b) Gray code is the same as binary code.
c) Gray code is obtained by applying AND operation between consecutive bits of binary.
d) The most significant bit of Gray code is always 1.

Answer: a) Gray code is obtained by applying XOR operation between consecutive bits of binary.

5. In the Gray code to binary conversion process, which XOR gate inputs correspond to the conversion of the least significant bit?

a) G0⊕B1

b) G1⊕B2
c) G0⊕B2
d) G0⊕B0

Answer: a) G0⊕B1

6. Which of the following correctly represents the Gray code for the binary number 111?

a) 101
b) 110
c) 011
d) 100

Answer: a) 101

7. In a 3-bit Gray code to binary conversion, how is the most significant bit of binary calculated?

a) XOR of the first and second Gray code bits
b) It is the same as the most significant Gray code bit
c) XOR of all Gray code bits
d) It is always 0

Answer: b) It is the same as the most significant Gray code bit

8. If the binary number is 010, what is the Gray code equivalent?

a) 011
b) 101
c) 110
d) 100

Answer: c) 110

9. Which logic gate is primarily used to convert between binary and Gray code?

a) AND gate
b) OR gate
c) XOR gate
d) NAND gate

Answer: c) XOR gate

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10. If the Gray code number is 011, what is the binary equivalent?

a) 010
b) 001
c) 100
d) 101

Answer: d) 101

Marwadi University Marwadi Chandarana Group NAAC A+	**Marwadi University** **Faculty of Engineering & Technology**	
Subject: Digital Electronics (01EC0102)	**Aim: Construction of 4 x 1 Multiplexer and 1 x 4 demultiplexer using logic gates**	
Experiment No: 8	**Date:21/3/2025**	**Enrollment No:92400194055**

Aim: Construction of 4 x 1 Multiplexer and 1 x 4 demultiplexer using logic gates

Software: Deldsim

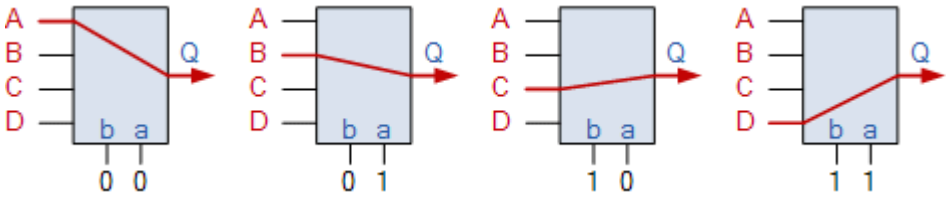
Theory:

Construction of 4 x 1 Multiplexer

Multiplexer - Multiplexing is the generic term used to describe the operation of sending one or more analogue or digital signals over a common transmission line at different times or speeds and as such, the device we use to do just that is called a Multiplexer.

The multiplexer , shortened to "MUX" or "MPX", is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal. Multiplexers operate like very fast acting multiple position rotary switches connecting or controlling multiple input lines called "channels" one at a time to the output. Multiplexers, or MUX's, can be either digital circuits made from high speed logic gates used to switch digital or binary data or they can be analogue types using transistors, MOSFET's or relays to switch one of the voltage or current inputs through to a single output.

Basic Multiplexing Switch



The rotary switch, also called a wafer switch as each layer of the switch is known as a wafer, is a mechanical device whose input is selected by rotating a shaft. In other words, the rotary switch is a manual switch that you can use to select individual data or signal lines simply by turning its inputs "ON" or "OFF". So how can we select each data input automatically using a digital device.

In digital electronics, multiplexers are also known as data selectors because they can "select" each input line, are constructed from individual Analogue Switches encased in a single IC package as opposed to the "mechanical" type selectors such as normal conventional switches and relays.

They are used as one method of reducing the number of logic gates required in a circuit design or when a single data line or data bus is required to carry two or more different digital signals. For example, a single 8-channel

multiplexer.

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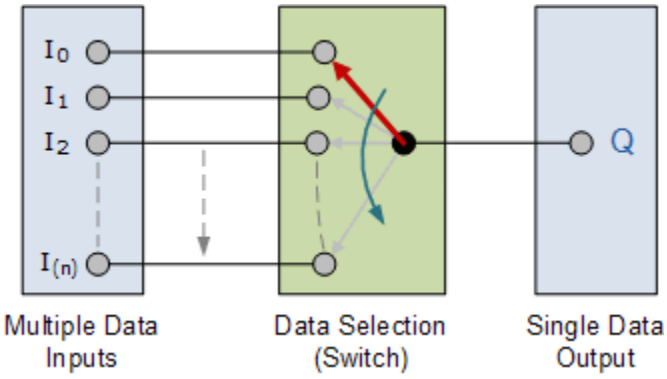
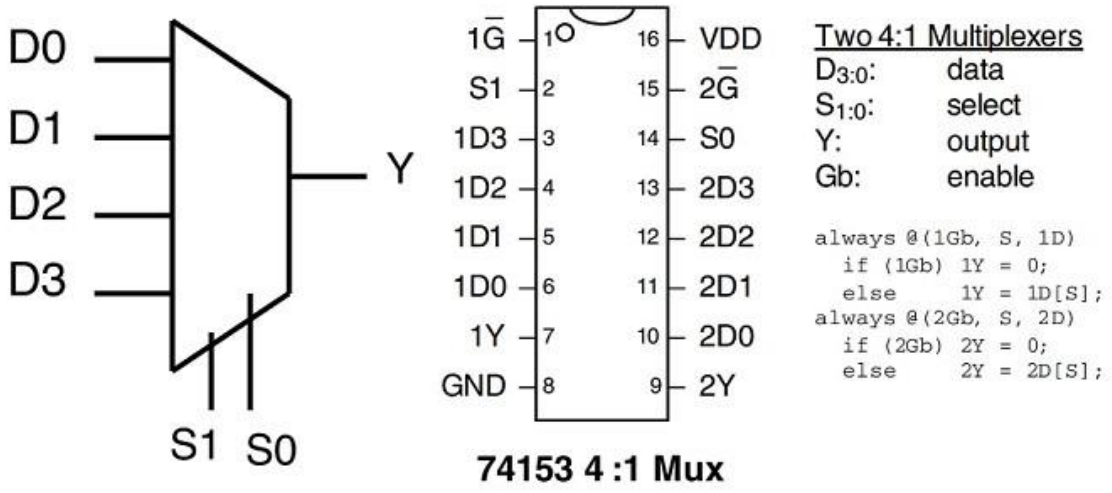


Generally, the selection of each input line in a multiplexer is controlled by an additional set of inputs called control lines and according to the binary condition of these control inputs, either "HIGH" or "LOW" the appropriate data input is connected directly to the output. Normally, a multiplexer has an even number of 2 n data input lines and a number of "control" inputs that correspond with the number of data inputs.

Block Diagram



1 x 4 demultiplexer

Theory

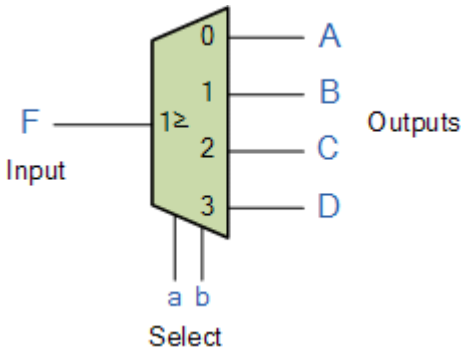
De-Multiplexer - The demultiplexer is a combinational logic circuit designed to switch one common input line to one of several separate output lines. The data distributor, known more commonly as a Demultiplexer or "Demux" for short, is the exact opposite of the Multiplexer we saw in the previous tutorial. The demultiplexer

takes one single input data line and then switches it to any one of a number of individual output lines one at a time. The demultiplexer converts a serial data signal at the input to a parallel data at its output lines as shown

below.

The function of the Demultiplexer is to switch one common data input line to any one of the 4 output data lines A to D in our example above. As with the multiplexer the individual solid state switches are selected by the binary input address code on the output select pins “a” and “b” as shown.

Demultiplexer Output Line Selection :

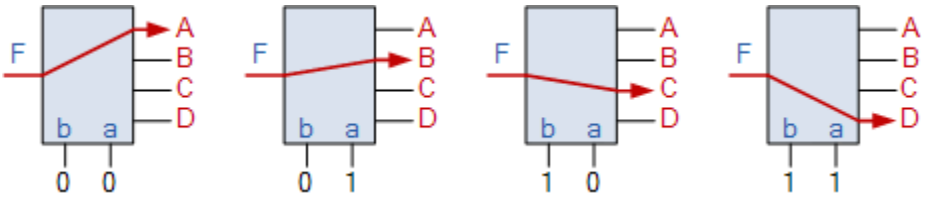


As with the previous multiplexer circuit, adding more address line inputs it is possible to switch more outputs giving a 1-to-2n data line outputs.

Some standard demultiplexer IC´s also have an additional “enable output” pin which disables or prevents the input from being passed to the selected output. Also some have latches built into their outputs to maintain the output logic level after the address inputs have been changed.

However, in standard decoder type circuits the address input will determine which single data output will have the same value as the data input with all other data outputs having the value of logic “0”.

The Demultiplexer Symbol



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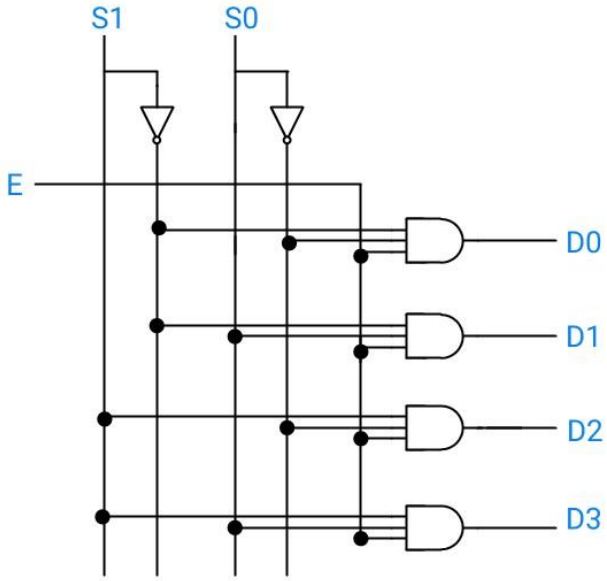
Block Diagram



Procedure:

Place the IC on IC Trainer on Deldsim.

Connect VCC and ground to respective pins of IC Trainer.

Implement the circuit as shown in the circuit diagram.

Connect the inputs to the input switches provided in the IC Trainer Kit.

Connect the outputs to the switches of O/P LEDs

Apply various combinations of inputs according to the truth table and observe the condition of LEDs.

Note down the corresponding output readings for various combinations of inputs.

Power Off Trainer Kit, disconnect all the wire connections and remove IC's from IC-Base.

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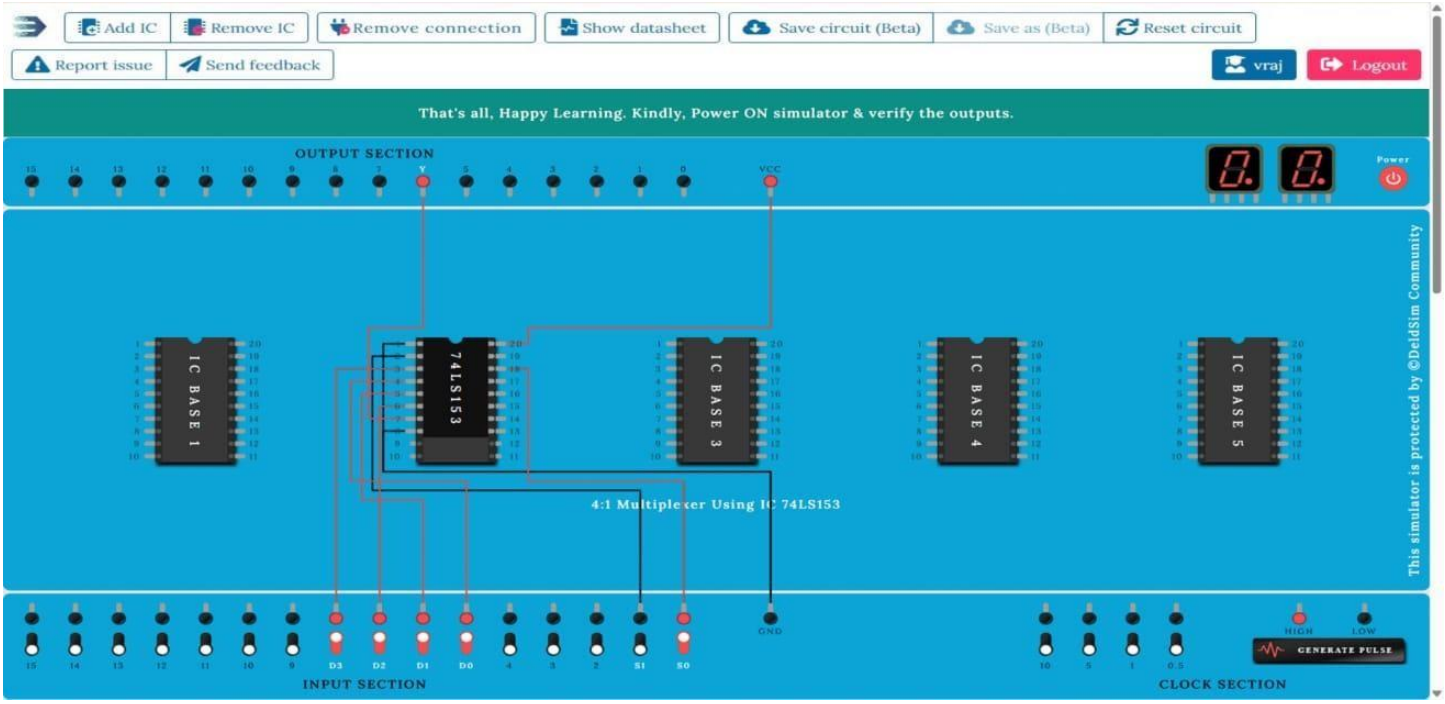
4 x 1 Multiplexer



1 x 4 demultiplexer

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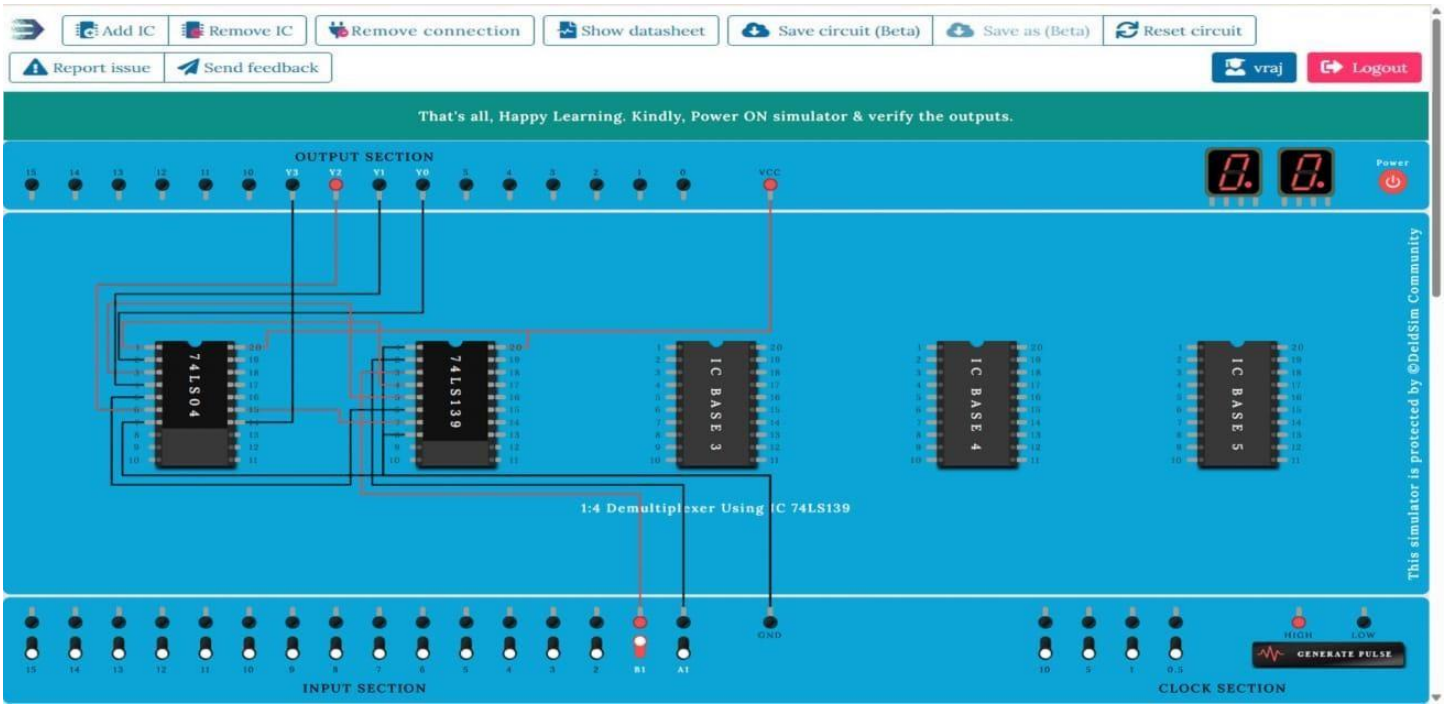

Conclusion:

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POST LAB EXERCISE

1. **How many NOT gates are required for the construction of a 4-to-1 multiplexer?**

a: 3

b: 4

c: 2

d: 5

2. **In 1-to-4 demultiplexer, how many select lines are required?**

a: 2

b: 3

c: 4

d: 5

3. **How many select lines are required for a 1-to-8 demultiplexer?**

a: 2

b: 3

c: 4

d: 5

4. Which IC is used for the implementation of 1-to-16 DEMUX?

a: IC 74154

b: IC 74155 c:

IC 74139 d:

IC 74138

5. The enable input is also known as _____ a: Select input b: Decoded input c: Strobe d: Sink

6. A demultiplexer accepts ..... inputs.

a: Single

b: Multiple

c: Two d:

Three

7. In a multiplexer, the selection of a particular input line is controlled by _____ a: Data controller

b: Selected lines c: Logic gates d: Both data controller and selected lines

8. If the number of n selected input lines is equal to 2^m then it requires _____ select lines.

a: 2 b:

m

c: n

d: 2^n

9. Which of the following circuit can be used as parallel to serial converter?

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a: Multiplexer b:

Demultiplexer c:

Decoder d:

Digital counter

10. How many select lines would be required for an 8-line-to-1-line multiplexer?

a: 2

b: 4

c: 8

d: 3

Marwadi University Marwadi Chandarana Group NAAC A+	**Marwadi University** **Faculty of Engineering & Technology** **Department of Information and Communication Technology**	
Subject: Digital Electronics (01EC0102)	**Aim:** Verify the truth table of RS, JK, T and D flip-flops using NAND and NOR gates	
Experiment No: 9	**Date**	**ENROLLMENT No: 92400194055**

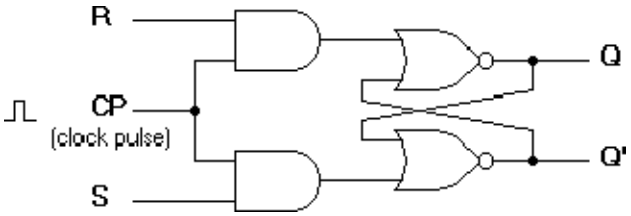
Aim: Verify the truth table of RS, JK, T and D flip-flops using NAND and NOR gates

Software: DEEDS Theory:

A flip flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

RS flip flop

The basic NAND gate RS flip flop circuit is used to store the data and thus provides feedback from both of its outputs again back to its inputs. The RS flip flop actually has three inputs, SET, RESET and clock pulse.



INPUTS			OUTPUT	STATE
CLK	S	R	Q	
X	0	0	No Change	Previous
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	-	Forbidden

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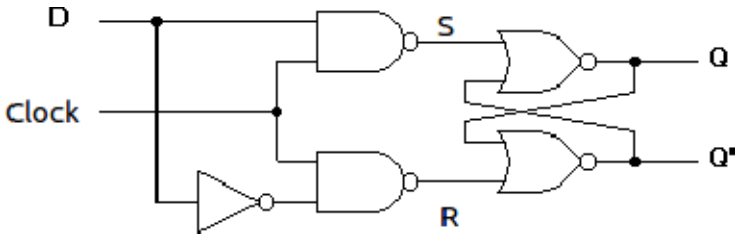
D flip flop

Experiment No: 9 **Date:** **Enrollment No: 92400120535**

A D flip flop has a single data input. This type of flip flop is obtained from the SR flip flop by connecting the R input through an inverter, and the S input is connected directly to data input. The modified clocked SR flip-flop is known as D-flip-flop and is shown below. From the truth table of SR flip-flop we see that the output of the SR flip-flop is in unpredictable state when the inputs are same and high. In many practical applications, these input conditions are not required. These input conditions can be avoided by making them complement of each other.



Input			Output	
D	reset	clock	Q	Q'
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

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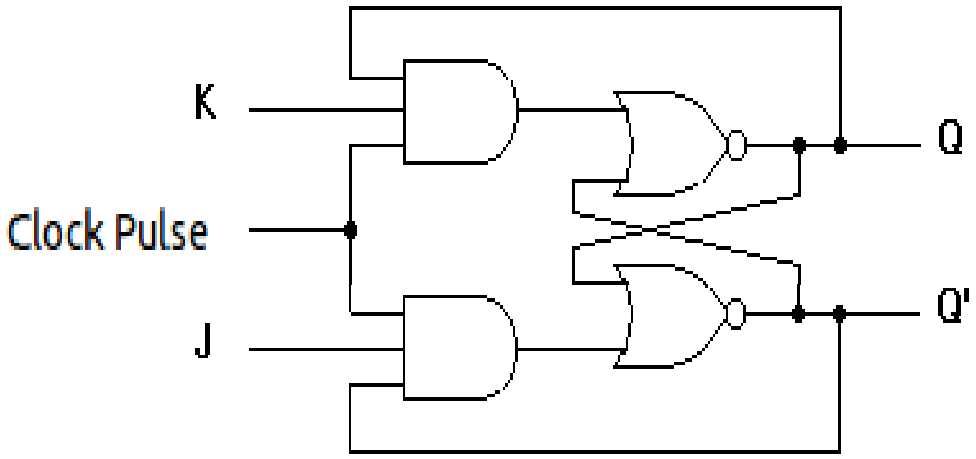
Experiment No: 9	**Date**	**ENROLLMENT No: 92400194055**

J-K flip flop

In a RS flip-flop the input R=S=1 leads to an indeterminate output. The RS flip-flop circuit may be re-joined if both inputs are 1 than also the outputs are complement of each other as shown in characteristics table below.

Experiment No: 9 **Date:** **Enrollment No: 92400120535**



Marwadi University Marwadi Chandarana Group NAAC A+	**Marwadi University** **Faculty of Engineering & Technology** **Department of Information and Communication Technology**
Subject: Digital Electronics (01EC0102)	**Aim:** Verify the truth table of RS, JK, T and D flip-flops using NAND and NOR gates

Trigger	Inputs		Output				Inference
			Present State		Next State		
CLK	J	K	Q	Q'	Q	Q'	
⊠	x	x	-		-		Latched
⊓	0	0	0	1	0	1	No Change
⊓			1	0	1	0	
⊓	0	1	0	1	0	1	Reset
⊓			1	0	0	1	
⊓	1	0	0	1	1	0	Set
⊓			1	0	1	0	
⊓	1	1	0	1	1	0	Toggles
⊓			1	0	0	1	

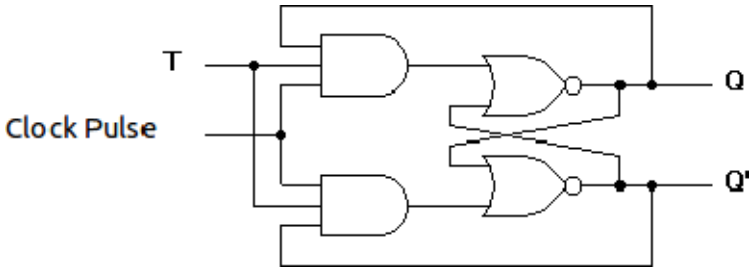
T flip flop

T flip-flop is known as toggle flip-flop. The T flip-flop is modification of the J-K flip-flop. Both the JK inputs of the JK flip – flop are held at logic 1 and the clock signal continuous to change as shown in table below.

Marwadi University Marwadi Chandarana Group NAAC A+	**Marwadi University** **Faculty of Engineering & Technology** **Department of Information and Communication Technology**	

Subject: Digital Electronics **Aim:** Verify the truth table of RS, JK, T and D flip-flops using NAND and

(01EC0102) NOR gates **Experiment No: 9** **Date:** **Enrollment No: 92400120535**



T flip-flop

T	Clock	Q	Q'
0	↑	Q	Q'
1	↑	Q'	Q
X	↓	Q	Q'

Procedure: 1. Connect Nand gate in cross coupled manner

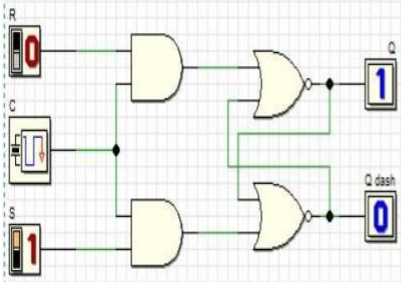
2. Label the inputs and the outputs as Q and Q'

3. Continue with the different cases as 00,01,10,11 to get the output for RS,JK,D and T flip flop

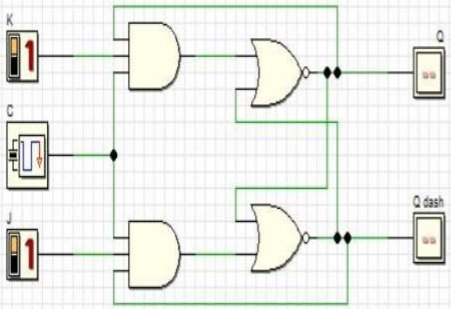
Marwadi University Marwadi Chandarana Group NAAC A+	**Marwadi University** **Faculty of Engineering & Technology** **Department of Information and Communication Technology**	
Subject: Digital Electronics	**Aim:** Verify the truth table of RS, JK, T and D flip-flops using NAND and	

Paste your simulation result screen shots here:

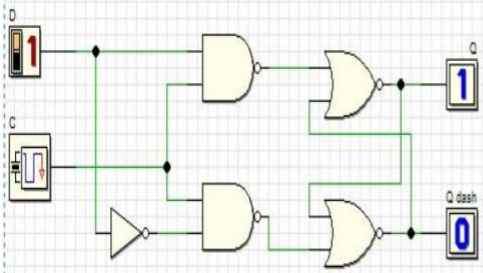
SR FLIP FLOP



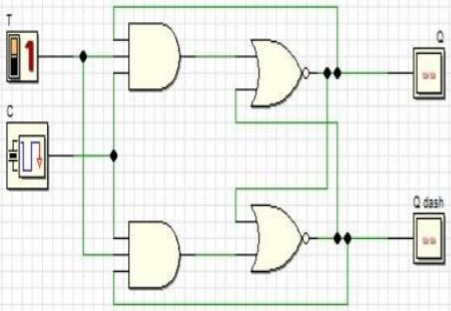
JK FLIP FLOP



D FLIP FLOP



T FLIP FLOP



Conclusion:

Experiment No: 9 **Date:** **Enrollment No: 92400120535**

Marwadi University Marwadi Chandarana Group NAAC A+	**Marwadi University** **Faculty of Engineering & Technology** **Department of Information and Communication Technology**	

Subject: Digital Electronics **(01EC0102)**

Aim: Verify the truth table of RS, JK, T and D flip-flops using NAND and NOR gates

Experiment No: 9 **Date:** **Enrollment No: 92400120535**

POST LAB EXERCISE

1. What is the primary function of the flip-flop in digital circuits?

A) To store binary data
B) To convert analog signals to digital
C) To generate clock pulses
D) To act as a gate for logical operations

2. Which of the following flip-flops can be implemented using only NAND gates?

A) JK flip-flop
B) D flip-flop
C) RS flip-flop
D) All of the above

3. In the DEEDS software, which feature allows the user to simulate and verify flip-flop truth tables?

A) Gate-level simulation
B) Boolean equation solver
C) Truth table analysis
D) Logic probe tool

4. What is the primary difference between RS and JK flip-flops?

A) RS flip-flop has an invalid state while JK does not
B) JK flip-flop cannot store data
C) RS flip-flop has a clock input
D) JK flip-flop only works with NAND gates

Marwadi University Marwadi Chandarana Group NAAC A+	**Marwadi University** **Faculty of Engineering & Technology** **Department of Information and Communication Technology**	
Subject: Digital Electronics	**Aim:** Verify the truth table of RS, JK, T and D flip-flops using NAND and	

5. Which gates are commonly used to implement an RS flip-flop?

A) AND and OR gates
B) NAND and NOR gates
C) XOR and XNOR gates D) NOT and AND gates
6. In a T flip-flop, the output toggles when the input is:

A) High

(01EC0102) NOR gates **Experiment No: 9** **Date:** **Enrollment No: 92400120535**

B) Low
C) Zero
D) One

7. How can the truth table of the D flip-flop be simplified in DEEDS?

A) By applying the correct input-output combinations
B) By using only NOR gates
C) By using an AND gate in place of a NOT gate
D) By testing for all edge cases

8. Which flip-flop type has no invalid states, making it suitable for reliable use in counters?

A) RS flip-flop
B) T flip-flop
C) JK flip-flop
D) D flip-flop

9. What is the effect of the "Set" and "Reset" inputs in the RS flip-flop when using NOR gates?

A) They change the output only when the clock pulse is high
B) They lead to an invalid state if both are high
C) They always produce the same output
D) They toggle the state of the flip-flop

10. When simulating flip-flops in DEEDS, what outcome would indicate an error in the truth table?

Marwadi University Marwadi Chandarana Group NAAC A+	**Marwadi University** **Faculty of Engineering & Technology** **Department of Information and Communication Technology**	

Subject: Digital Electronics **Aim:** Verify the truth table of RS, JK, T and D flip-flops using NAND and

A) The output does not change when inputs are altered
B) The outputs match the expected values for each input combination
C) The simulation runs without any delays
D) The circuit outputs a constant high signal

Marwadi University **Faculty of Engineering & Technology**		
Subject: Digital Electronics (01EC0102)	**Aim: Design and verify 4-bit Serial In – In-Parallel Out (SIPO) shift registers.**	
Experiment No: 10	**Date: 03/04/25**	**Enrollment No: 92400194055**

Aim: Design and verify 4-Bit Serial In – Parallel Out (SIPO) shift registers.

Software: Deeds (Digital Circuit Simulator)

Theory: In Serial In Parallel Out (SIPO) shift registers, the data is stored into the register serially while it is retrieved from it in parallel-fashion. Figure 1 shows an n-bit synchronous SIPO shift register sensitive to positive edge of the clock pulse. Here the data word which is to be stored (Data in) is fed serially at the input of the first flip-flop (D1 of FF1). It is also seen that the inputs of all other flip-flops (except the first flip-flop FF1) are driven by the outputs of the preceding ones like the input of FF2 is driven by the output of FF1. In this kind of shift register, the data stored within the register is obtained as a parallel-output data word (Data out) at the individual output pins of the flip-flops (Q1 to Qn).

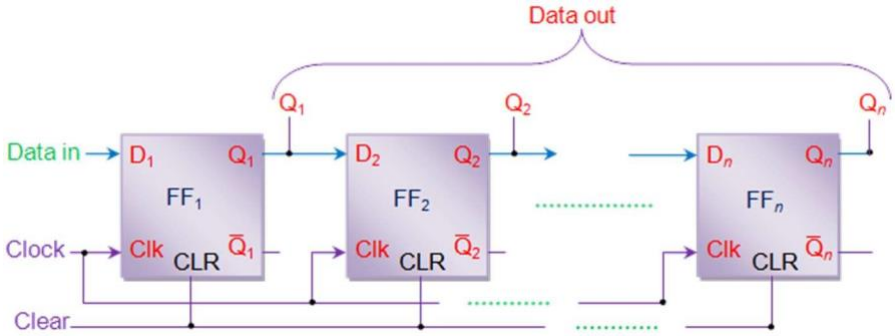


Figure 1. n-bit Serial In-Parallel Out shift register

In general, the register contents are cleared by applying high on the clear pins of all the flip-flops at the initial stage. After this, the first bit, B1 of the input data word is fed at the D1 pin of FF1.This bit (B1) will enter into FF1, get stored and thereby appears at its output Q1 on the appearance of first leading edge of the clock. Further at the second clock pulse, the bit B1 right-shifts and gets stored into FF2 while appearing at its output pin Q2 while a new bit, B2 enters into FF1. Similarly at each clock pulse the data within the register moves towards right by a single bit while a new bit of the input word enters into the register. Meanwhile one can extract the bits stored within the register in parallel-fashion at the individual flip-flop outputs.

Analyzing on the same grounds, one can note that the n-bit input data word is obtained as an n-bit output data word from the shift register at the rising edge of the nth clock pulse. This working of the shift-register can be summarized as in Table I and the corresponding waveforms are given by figure 2.

Marwadi University Marwadi Chandarana Group NAAC A+	Marwadi University Faculty of Engineering & Technology	
Subject: Digital Electronics (01EC0102)	Aim: Design and verify 4-Bit Serial In – Parallel Out (SIPO) shift registers.	
Experiment No: 10	Date: 03/04/25	Enrollment No: 92400120535

Table 1. Data movement in Right-Shift SIPO Shift Register

Clock Cycle	Data in	Q_1	Q_2	...	Q_n
1	B_1	B_1	0	...	0
2	B_2	B_2	B_1	...	0
3	B_3	B_3	B_2	...	0
4	B_4	B_4	B_3	...	0
5	B_5	B_5	B_4	...	0
6	B_6	B_6	B_5	...	0
.	.	.	.	...	.
.	.	.	.		.
.	.	.	.		.
n	B_n	B_n	B_{n-1}	...	B_1

Output of SIPO (right-shift) Shift Register

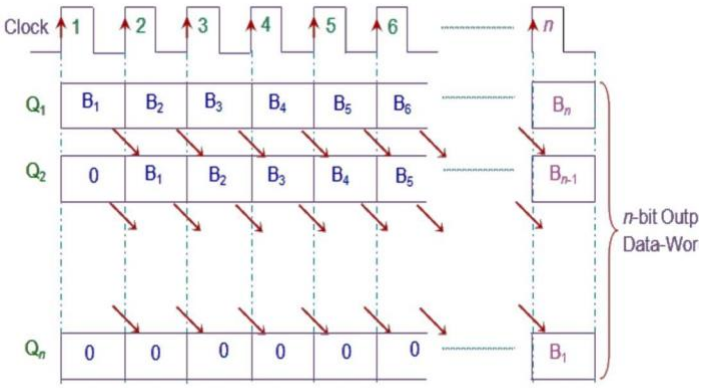


Figure 2. Output waveform of n-bit Right Shift SIPO Shift Register

Procedure:

Step 1: Open DEEDS and Create a New Circuit

- Launch DEEDS (Digital Electronics Education and Design Suite).
- Create a new circuit schematic.

Step 2: Add Components

- Flip-Flops: Add four D-type flip-flops (D-FFs) to the circuit.
- Input Pins: Add an input pin for serial data input.
- Clock Signal: Add a clock signal to control shifting.
- Enable and Clear Signals: Add Enable and Clear input pins.
- Output Display: Place four output displays to observe the parallel output.

Marwadi University Marwadi Chandarana Group NAAC A+	Marwadi University Faculty of Engineering & Technology	
Subject: Digital Electronics (01EC0102)		
Experiment No: 10	Date: 03/04/25	Enrollment No: 92400120535

Step 3: Connect the Circuit

- Connect the serial data input to the D input of the first flip-flop.
- Connect the Q output of each flip-flop to the D input of the next flip-flop.
- Connect a common clock signal to the clock (Ck) inputs of all flip-flops.
- Connect the Enable signal to all flip-flops.
- Connect the Clear signal to the reset (CL) inputs of all flip-flops.
- Connect the Q outputs of each flip-flop to the parallel output displays.

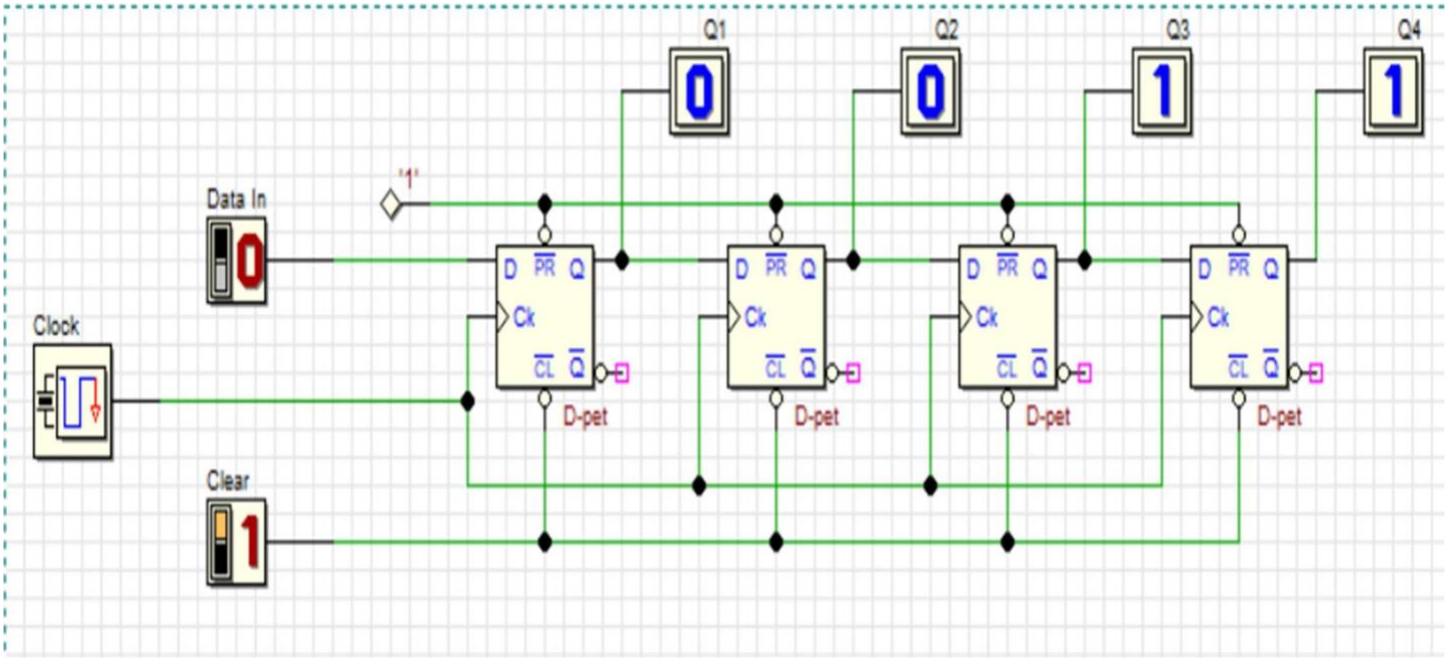
Step 4: Configure Flip-Flops

- Set each D-FF to trigger on the clock edge.
- Ensure the Enable signal is active high to allow shifting.
- Set the Clear signal to reset all flip-flops when needed.

Step 5: Simulate the Circuit

- Apply a serial data sequence to the input.
- Toggle the clock signal to shift data through the register.
- Observe the parallel outputs updating with each clock pulse.

Simulation:



Marwadi University Marwadi Chandarana Group NAAC A+	Marwadi University Faculty of Engineering & Technology	
Subject: Digital Electronics (01EC0102)	Aim: Design and verify 4-Bit Serial In – Parallel Out (SIPO) shift registers.	
Experiment No: 10	Date: 03/04/25	Enrollment No: 92400120535

Conclusion:

POST LAB EXERCISEB) 3

C) 5

D) 5

1. What is the primary function of a 4-bit Serial-In Parallel-Out (SIPO) shift register?

A) Convert parallel data to serial data
B) Convert serial data to parallel data
C) Store data permanently
D) Perform arithmetic operations

2. How many D flip-flops are required to implement a 4-bit SIPO shift register?

A) 2

3. What is the role of the clock signal in a shift register?

A) It controls the shifting of data

B) It resets the register
C) It holds the data constant
D) It converts data from serial to parallel

4. What happens when a new bit is shifted into a 4-bit SIPO shift register?

A) The last bit is lost
B) The register remains unchanged
C) All bits move one position forward
D) The register resets

5. What is the purpose of the "Enable" signal in a shift register?

A) It controls whether data shifting occurs
B) It resets the register
C) It controls output voltage
D) It stores the input permanently

Marwadi University Marwadi Chandarana Group NAAC A+	Marwadi University Faculty of Engineering & Technology	
Subject: Digital Electronics (01EC0102)	Aim: Design and verify 4-Bit Serial In – Parallel Out (SIPO) shift registers.	
Experiment No: 10	Date: 03/04/25	Enrollment No: 92400120535

6. In a 4-bit SIPO shift register, how many clock pulses are required to fully load 4 bits of data?

A) 1
B) 2
C) 3
D) 4

7. Which type of flip-flop is commonly used in SIPO shift registers?

A) SR Flip-Flop
B) JK Flip-Flop
C) D Flip-Flop D) T Flip-Flop

8. If the input sequence is 1011, what will be the final output of a 4-bit SIPO shift register after four clock pulses?

A) 1101
B) 1011
C) 0110
D) 1001

9. What happens to the existing bits in a shift register when a new bit is shifted in?

A) They move one position to the right
B) They move one position to the left
C) They remain unchanged
D) They get erased

10. Which of the following applications uses SIPO shift registers?

A) Serial-to-parallel data conversion
B) Multiplication
C) Analog signal processing
D) Data encryption