Marwadi University **Faculty of Engineering & Technology**		
Subject: Digital Electronics (01EC0102)	**Aim: Design and verify 4-bit Serial In – In-Parallel Out (SIPO) shift registers.**	
Experiment No: 10	**Date: 03/04/25**	**Enrollment No: 92400194055**

Aim: Design and verify 4-Bit Serial In – Parallel Out (SIPO) shift registers.

Software: Deeds (Digital Circuit Simulator)

Theory: In Serial In Parallel Out (SIPO) shift registers, the data is stored into the register serially while it is retrieved from it in parallel-fashion. Figure 1 shows an n-bit synchronous SIPO shift register sensitive to positive edge of the clock pulse. Here the data word which is to be stored (Data in) is fed serially at the input of the first flip-flop (D1 of FF1). It is also seen that the inputs of all other flip-flops (except the first flip-flop FF1) are driven by the outputs of the preceding ones like the input of FF2 is driven by the output of FF1. In this kind of shift register, the data stored within the register is obtained as a parallel-output data word (Data out) at the individual output pins of the flip-flops (Q1 to Qn).

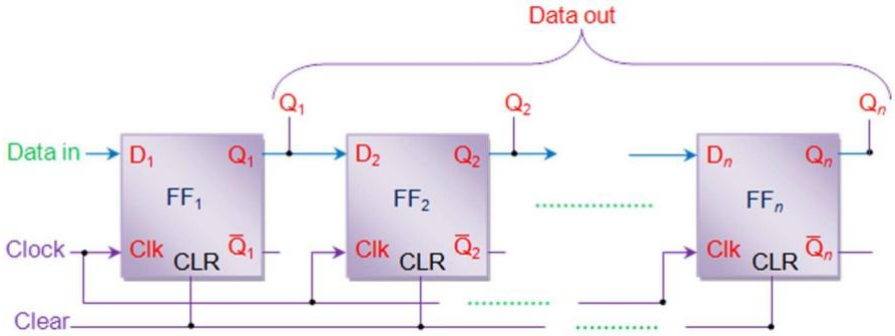

Figure 1. n-bit Serial In-Parallel Out shift register

In general, the register contents are cleared by applying high on the clear pins of all the flip-flops at the initial stage. After this, the first bit, B1 of the input data word is fed at the D1 pin of FF1.This bit (B1) will enter into FF1, get stored and thereby appears at its output Q1 on the appearance of first leading edge of the clock. Further at the second clock pulse, the bit B1 right-shifts and gets stored into FF2 while appearing at its output pin Q2 while a new bit, B2 enters into FF1. Similarly at each clock pulse the data within the register moves towards right by a single bit while a new bit of the input word enters into the register. Meanwhile one can extract the bits stored within the register in parallel-fashion at the individual flip-flop outputs.

Analyzing on the same grounds, one can note that the n-bit input data word is obtained as an n-bit output data word from the shift register at the rising edge of the nth clock pulse. This working of the shift-register can be summarized as in Table I and the corresponding waveforms are given by figure 2.

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Table 1. Data movement in Right-Shift SIPO Shift Register

Clock Cycle	Data in	Q_1	Q_2	...	Q_n
1	B_1	B_1	0	...	0
2	B_2	B_2	B_1	...	0
3	B_3	B_3	B_2	...	0
4	B_4	B_4	B_3	...	0
5	B_5	B_5	B_4	...	0
6	B_6	B_6	B_5	...	0
.	.	.	.	...	.
.	.	.	.		.
.	.	.	.		.
n	B_n	B_n	B_{n-1}	...	B_1

Output of SIPO (right-shift) Shift Register

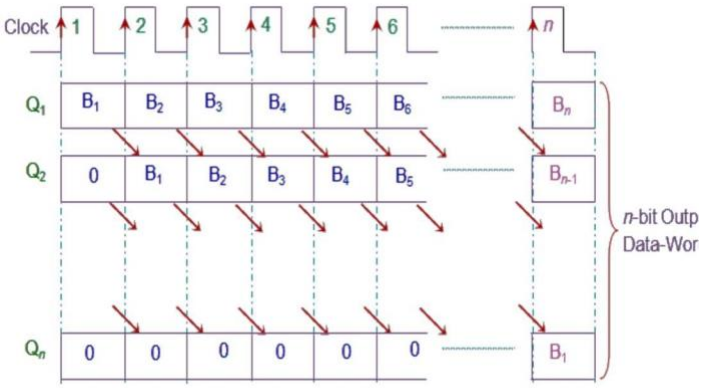

Figure 2. Output waveform of n-bit Right Shift SIPO Shift Register

Procedure:

Step 1: Open DEEDS and Create a New Circuit

- Launch DEEDS (Digital Electronics Education and Design Suite).
- Create a new circuit schematic.

Step 2: Add Components

- Flip-Flops: Add four D-type flip-flops (D-FFs) to the circuit.
- Input Pins: Add an input pin for serial data input.
- Clock Signal: Add a clock signal to control shifting.
- Enable and Clear Signals: Add Enable and Clear input pins.
- Output Display: Place four output displays to observe the parallel output.

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Step 3: Connect the Circuit

- Connect the serial data input to the D input of the first flip-flop.
- Connect the Q output of each flip-flop to the D input of the next flip-flop.
- Connect a common clock signal to the clock (Ck) inputs of all flip-flops.
- Connect the Enable signal to all flip-flops.
- Connect the Clear signal to the reset (CL) inputs of all flip-flops.
- Connect the Q outputs of each flip-flop to the parallel output displays.

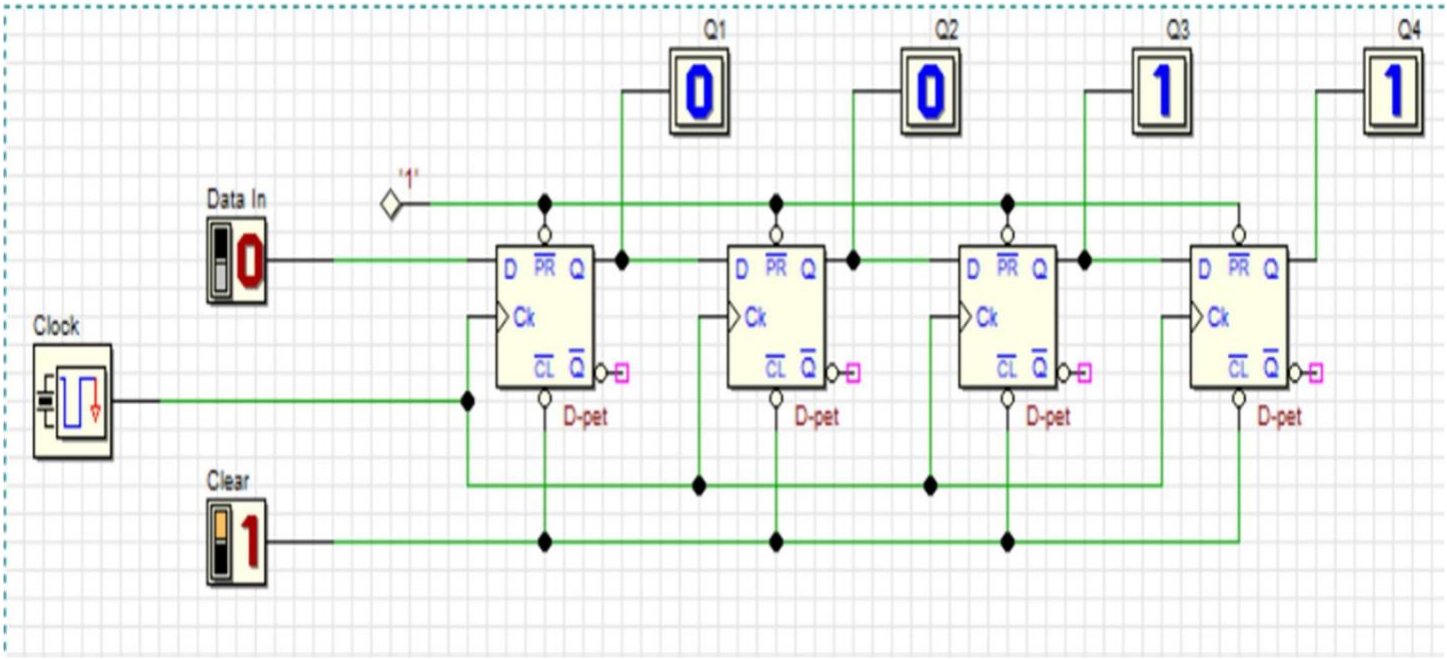
Step 4: Configure Flip-Flops

- Set each D-FF to trigger on the clock edge.
- Ensure the Enable signal is active high to allow shifting.
- Set the Clear signal to reset all flip-flops when needed.

Step 5: Simulate the Circuit

- Apply a serial data sequence to the input.
- Toggle the clock signal to shift data through the register.
- Observe the parallel outputs updating with each clock pulse.

Simulation:



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Conclusion:

POST LAB EXERCISEB) 3

C) 5

D) 5

1. What is the primary function of a 4-bit Serial-In Parallel-Out (SIPO) shift register?

A) Convert parallel data to serial data
B) Convert serial data to parallel data
C) Store data permanently
D) Perform arithmetic operations

2. How many D flip-flops are required to implement a 4-bit SIPO shift register?

A) 2

3. What is the role of the clock signal in a shift register?

A) It controls the shifting of data

B) It resets the register
C) It holds the data constant
D) It converts data from serial to parallel

4. What happens when a new bit is shifted into a 4-bit SIPO shift register?

A) The last bit is lost
B) The register remains unchanged
C) All bits move one position forward
D) The register resets

5. What is the purpose of the "Enable" signal in a shift register?

A) It controls whether data shifting occurs
B) It resets the register
C) It controls output voltage
D) It stores the input permanently

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6. In a 4-bit SIPO shift register, how many clock pulses are required to fully load 4 bits of data?

A) 1
B) 2
C) 3
D) 4

7. Which type of flip-flop is commonly used in SIPO shift registers?

A) SR Flip-Flop
B) JK Flip-Flop
C) D Flip-Flop D) T Flip-Flop

8. If the input sequence is 1011, what will be the final output of a 4-bit SIPO shift register after four clock pulses?

A) 1101
B) 1011
C) 0110
D) 1001

9. What happens to the existing bits in a shift register when a new bit is shifted in?

A) They move one position to the right
B) They move one position to the left
C) They remain unchanged
D) They get erased

10. Which of the following applications uses SIPO shift registers?

A) Serial-to-parallel data conversion
B) Multiplication
C) Analog signal processing
D) Data encryption