Krish Patel

www.krishpatel.com • kdpatel@wpi.edu • 703.629.0921

EXPERIENCE

DRAPER SCHOLAR PROGRAM | AI-Driven Researcher
June 2024 – Present | Cambridge, MA

- Leading a 2-year AI-driven thesis project on Technical Debt in Systems Engineering lifecycles.
- Developing a Retrieval-Augmented Generation (RAG) system with LLMs to analyze SEMP documents.

ARCFIELD | IT Intern
July 2023 – August 2023 | Chantilly, VA

- Engineered a network monitoring dashboard using Icinga in an Azure GCC-H environment.
- Integrated Grafana and Prometheus for real-time system health visualization.

ABBVIE | Grafana Prometheus Developer
June 2022 – March 2023 | Chicago, IL

- Designed network monitoring solutions for EMR clusters using Grafana and Prometheus.
- Integrated legacy applications with cloud infrastructure for improved data visualization.

PROJECTS

SYSTEMVERILOG ASSERTIONS LIBRARY | Open-Source Verification Project
github.com/krishpatel1077/sv_assertion_library

- Developed a comprehensive SVA library for verifying sequential logic and protocol compliance.
- Created reusable assertion modules for bus protocols, handshakes, and clock-domain crossing.
- Open-sourced with documentation and usage examples for the hardware verification community.

PYTHON RTL TESTBENCH GENERATOR | Functional Verification Automation
github.com/krishpatel1077/rtl-testbench-gen

- Created a Python-based SystemVerilog testbench generator using Jinja2 templating.
- Supports multiple module types (ALU, FSM, Memory, UART) with specialized test patterns.
- Reduces testbench development time by up to 80% for standard RTL modules.

RISC-V CPU DESIGN | Custom Processor Implementation

- Designed and implemented a single-cycle RISC-V processor supporting the RV32I instruction set.
- Developed register file, ALU, control unit, and memory interfaces in SystemVerilog.
- Validated instruction execution and control flow with comprehensive verification.

EDUCATION

WORCESTER POLYTECHNIC INSTITUTE

M.S. in Electrical and Computer Engineering
2024 – 2025

B.S. in Electrical and Computer Engineering
2021 – 2024

SKILLS

HARDWARE VERIFICATION
SystemVerilog • UVM • Assertions • Formal Verification
RTL Design • FPGA Simulation • Testbench Development • Coverage Metrics

PROGRAMMING
C, Python, Java, Verilog, VHDL, SystemVerilog

CLOUD TECHNOLOGIES
AWS, Microsoft Azure, Kubernetes, Docker

CERTIFICATIONS

AWS Certified Machine Learning Specialty (AWS MLS-C01) (2025 - 2028)
AWS Certified Solutions Architect Professional (AWS SAP-C02) (2024 - 2027)
Microsoft Certified: Azure Solutions Architect Expert (AZ-305) (2022 - 2024)
Certified Kubernetes Application Developer (CKAD) (2021 - 2024)

COURSEWORK

GRADUATE
On-Device Deep Learning
Computer Architecture
Machine Learning in Cybersecurity

UNDERGRADUATE
Computer Architecture
Real-time Embedded Systems
Microelectronic Circuits I, II
Advanced Digital System Design with FPGA
Embedded Computing in Engineering Design

LINKS

Github:// **krishpatel1077**
LinkedIn:// **krishpatel9999**