



VIJAYA KRISHNA KASULA

Principal Engineer, Processor Verification @ Synopsys Jul 2010 - Present

Worked as a contractor from SoCronics from Jul 2010 - Feb 2014 ([details](#))

KEY PROJECTS (all)

Random Program Generators (RPGs) ([details](#))

Dec 2011 - Present

Lead Developer & Product Manager, Synopsys

- Designed and developed multiple RPGs: Offline RPG, Online RPG (Stepping), Python Environment, C-based Environment
- Managed product lifecycle end-to-end, supporting 50+ verification engineers across multiple product lines
- Developed SystemVerilog-based generator with coverage-driven features (Cov2gen)
- Impact: Enabled comprehensive processor feature coverage, reduced test development time significantly

AI-ML Log Anomaly Detector ([details](#))

Nov 2021 - Feb 2022

Master's Thesis Project, BITS Pilani, Deployed in production at Synopsys

- Developed intelligent log analyzer using scikit-learn, NLP, and unsupervised learning
- Evaluated on 10 datasets with 400M+ reference log lines, tested 36 model combinations
- Deployed in production at Synopsys, automating verification failure log triaging

Co-Simulation Environment ([details](#))

Dec 2012 - Mar 2014

Sole Developer, Synopsys

- Designed and implemented robust co-simulation environment for processor-level verification
- Enabled seamless integration between testbenches and golden reference models

C-Forge ([details](#))

2025

Sole Developer, Synopsys

- Efficient configuration generator for configuration space verification of ARC Processor IP
- Presented at Purple Poster event (Synopsys) 2025

PUBLICATIONS & PRESENTATIONS (all)

Kasula, V. K. (2025). *C-Forge, Efficient Configuration Generator for Configuration Space Verification of ARC Processor IP*. Purple Poster, Synopsys.

Kasula, V. K., & Chedella, S. S. (2016). *Barrier Insertion in Test Programs for Controlled Verification of Cache Coherency*. SITC, Bangalore.

Kasula, V. K. (2016). *Reverse Generation Technique for Functional Verification of Processor Cores*. SITC, Bangalore.

Kasula, V. K., & Tadiboina, G. K. (2016). *Test Generation for Processors with Extended Address Capability*. SITC, Bangalore.

OPEN SOURCE CONTRIBUTIONS (all)

argparse-enh ([details](#))

Active

Python Library, PyPI

- Enhanced argparse with API, shell, and automatic GUI generation modes

txt2flow ([details](#))

Active

Python Library, PyPI

- Automatically generates flowcharts from pseudo-code written in C-like languages

CONTACT

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📞 +91 92931 94921
LinkedIn • GitHub • GitLab
🌐 Detailed Resume / CV

PROFESSIONAL SUMMARY

15+ years of experience in processor-level verification. Led development of critical verification infrastructure supporting 50+ engineers.

TECHNICAL SKILLS

Languages: SystemVerilog, Python, Perl, C/C++, SQL

Verification: UVM, Processor Verification, Coverage-Driven

ML/AI: scikit-learn, NLP, Unsupervised Learning, Anomaly Detection

Tools: Grafana, GitLab CI/CD, Docusaurus, Sphinx, Doxygen, Verdi

Infrastructure: Git, GitLab, Regression Automation, Monitoring

EDUCATION (full)

M.Tech in Data Science & Engineering
BITS Pilani (WILP)
Nov 2019 - Feb 2022 | CGPA: 8.75

B.Tech in Electronics & Communication
SVIT (JNTU Hyderabad)
Jun 2006 - Jun 2010 | 71.40%

AWARDS & RECOGNITION

Received a certificate of recommendation from HARVARD University, Cambridge, MA, USA, acknowledging my performance in an online coding competition held in collaboration with NASA on TopCoder (2012)

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