KLE Technological University

Creating Value
Leveraging Knowledge

School

of

Electronics and Communication Engineering

Course Project Report

on

Implementation of Programmable digital delay timer in Verilog hdl

By:

1. **Sandesh.R.C** USN: 01FE20BEC330
2. **Krishnareddy.H.M** USN: 01FE20BEC305

Semester: VI, 2022-2023

Under the Guidance of

Dr.Saroja.V.S

0.1 Problem statement

Implementation of Programmable digital delay timer in Verilog hdl.

0.2 Introduction

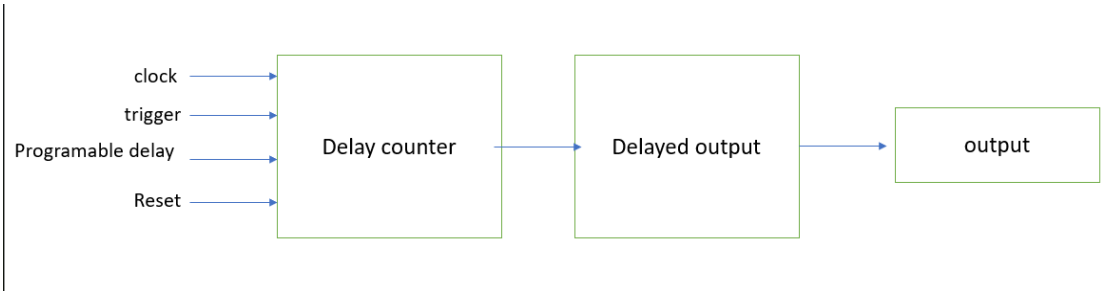
A digital delay timer is an electronic circuit or device that is used to introduce a time delay in a digital signal. It can be used for a variety of applications, such as timing control, synchronization, signal processing, and communication systems.

A digital delay timer typically consists of a clock signal input, a delay time input, and a delay signal output. The clock signal is used to trigger the delay timer, and the delay time input specifies the duration of the delay. When the delay timer is triggered, it waits for the specified amount of time and then generates a delay signal output. The delay signal output can be used to control the timing of other circuits or devices in the system.

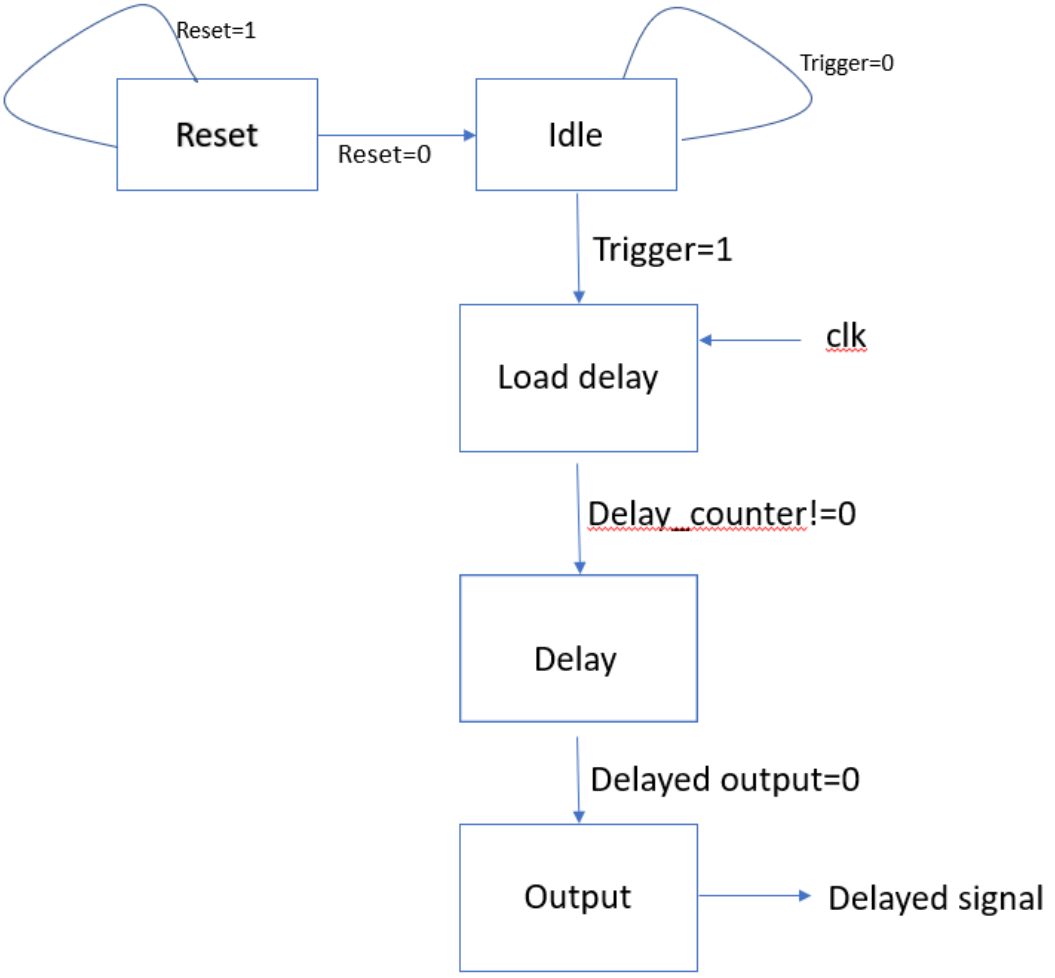
Digital delay timers can be implemented using digital logic circuits, such as counters, shift registers, and flip-flops. In modern digital systems, digital delay timers are often implemented using programmable logic devices, such as FPGAs.

Digital delay timers are widely used in a variety of applications, including audio and video processing, telecommunications, data transmission, radar systems, and industrial control systems. They are also used in scientific and engineering applications, such as time-domain reflectometry, pulse shaping, and signal propagation analysis.

0.3 Architecture



0.4 Architecture



1)clk: The clock input signal.
2)trigger: The trigger input signal used to start the delay.
3)reset: The reset input signal is used to reset the delay timer.
4)delay input: An 8-bit input signal representing the duration of the delay.
5)delayed output: A registered output signal that goes high after the specified delay duration has passed.

An 8-bit register called a delay counter. It is used to count the delay duration. If the reset signal is asserted (high), the delay counter and delayed output are both resets to 0.

The clock signal (clk) drives the sequential behavior of the module. On each positive edge of the clock, the delay timer module checks the state of the reset and trigger signals and updates the delay counter and delayed output accordingly. The reset signal resets the delay counter and delayed output to 0, effectively resetting the delay timer. The trigger signal starts the delay timer by loading the delay counter with the value of the delay input and setting the delayed output to 0. The delay counter counts down from the loaded delay input value on each clock cycle, as long as it is not zero and neither the reset nor trigger signals are asserted. Once the delay counter reaches 0, the delayed output signal is set to 1, indicating that the specified delay has elapsed.

The maximum delay that the delay timer module can generate depends on the maximum value that can be represented by the delay input, as well as the clock frequency. Assuming an 8-bit delay input, the maximum delay time that can be achieved with various clock frequencies is:
For a 1 MHz clock frequency, the maximum delay time is $(2^8 - 1 + 1) * 1microsecond = 256microseconds$.
For a 10 MHz clock frequency, the maximum delay time is $(2^8 - 1 + 1) * 100ns = 25.6microseconds$.
For a 100 MHz clock frequency, the maximum delay time is $(2^8 - 1 + 1) * 10ns = 2.56microseconds$.
For a 1 GHz clock frequency, the maximum delay time is $(2^8 - 1 + 1) * 1ns = 256ns$

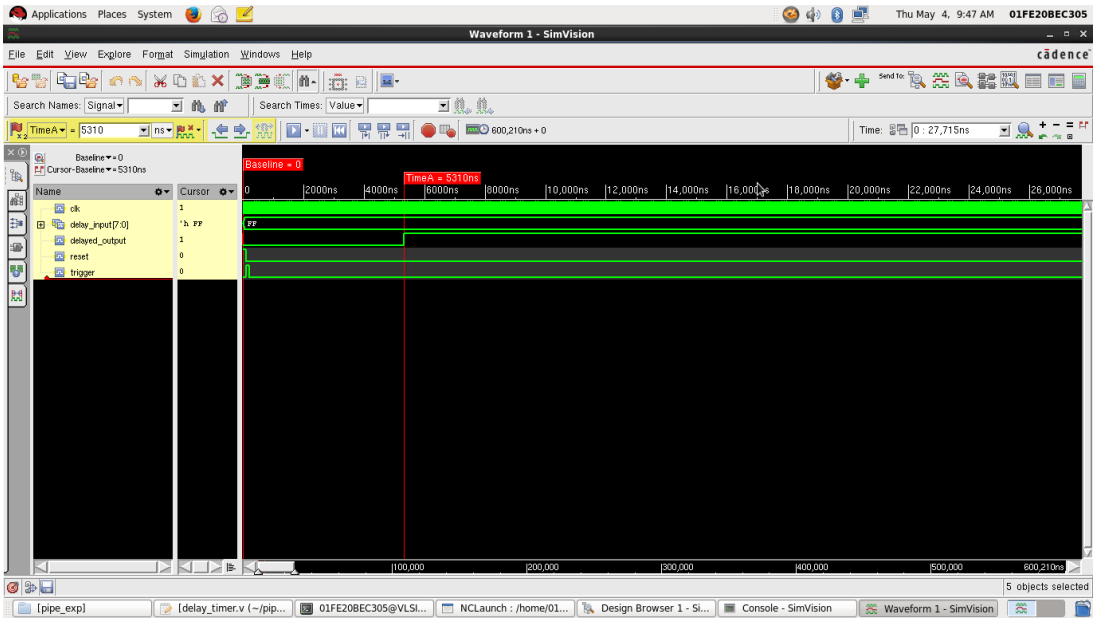
Note that the actual maximum delay time may be slightly longer than these theoretical values due to propagation delays in the logic gates and wires.
In the Verilog module delay timer, the delayed output signal is set to 1 after a certain delay specified by the delay input signal, which is a user-defined 8-bit value.
The delay is generated using a counter (delay counter) that is incremented every clock cycle when the trigger signal is high. Once the counter value reaches the delay input value, the delayed output signal is set to 1.
The time delay generated by the counter can be calculated as follows:

Delay time = (delay input + 1) * (clock period)

Here, delay input is the user-defined value for the delay, and clock period is the time period of the input clock signal (clk).
The +1 term in the equation accounts for the fact that the counter starts from 0 and counts up to the delay input value.

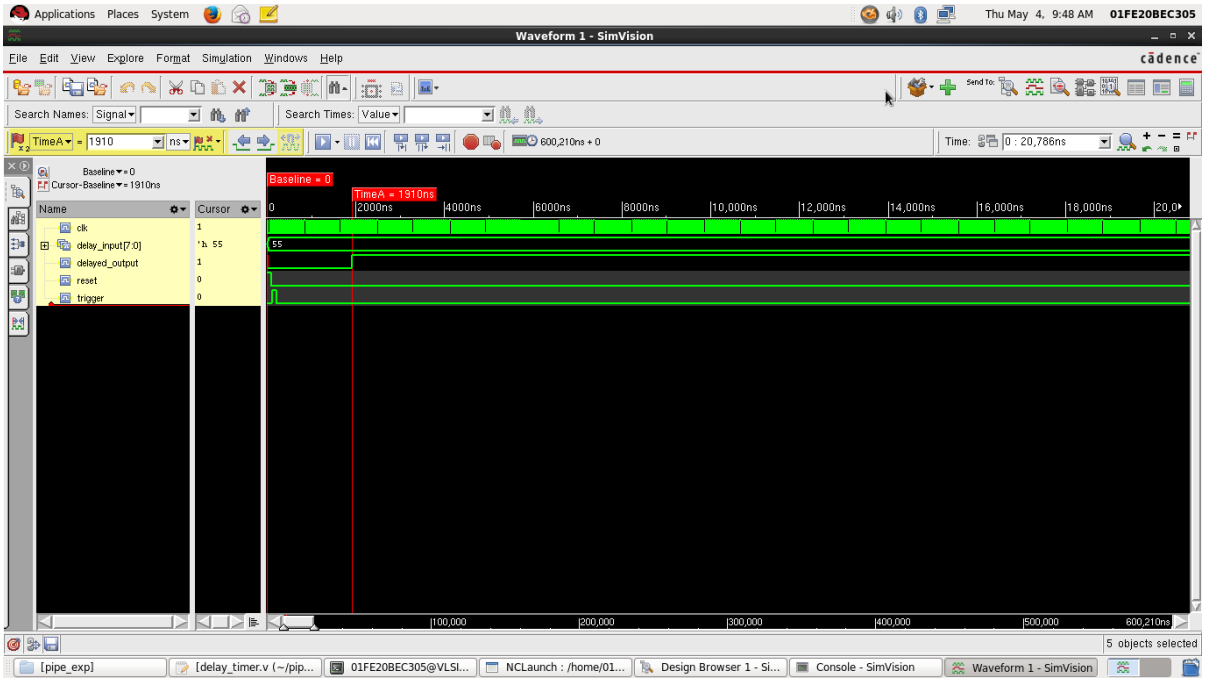
0.5 Result

1)



when we give h'ff as input we get 3150ns as output delay

2)



when we give h'55 as input we get 1910ns as output delay

0.6 Conclusion

In conclusion, the provided Verilog code represents a simple delay timer module. It features inputs for the clock signal, trigger signal, reset signal, and delay duration. The module utilizes a delay counter and a registered output to generate a delayed output signal.

This delay timer module can be used in various digital designs that require timed operations or synchronization. By incorporating this module, designers can introduce delays and time-controlled behaviors into their designs.

Understanding the functionality and behavior of this delay timer module provides a foundation for designing more complex systems that involve time-based operations and precise synchronization.