CHAPTER 4

MOS Field-Effect Transistors (MOSFETs)

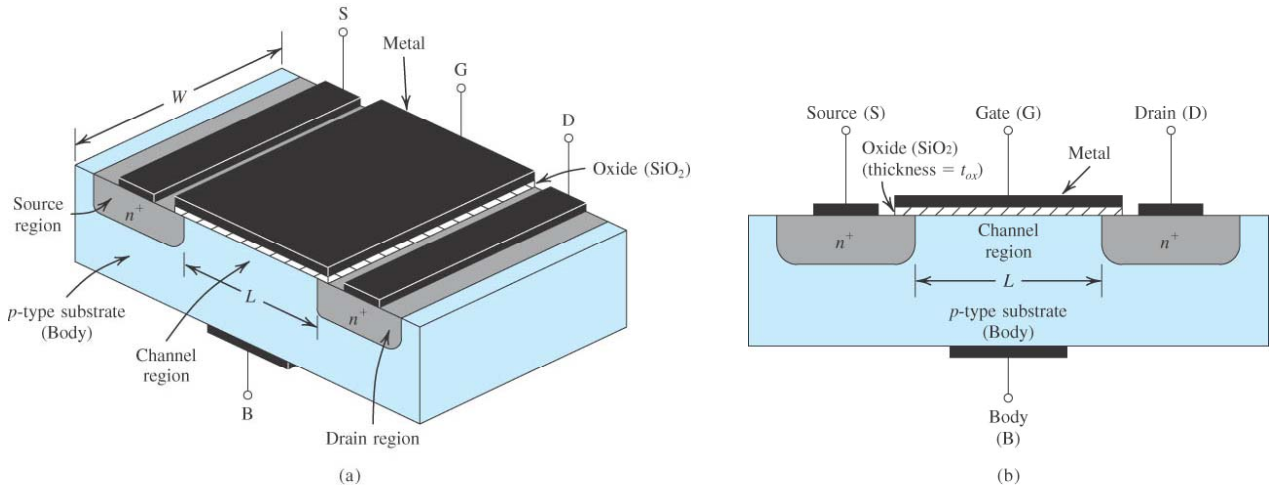


Figure 4.1 Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross-section. Typically L = 0.1 to 3 μm, W = 0.2 to 100 μm, and the thickness of the oxide layer (t_{ox}) is in the range of 2 to 50 nm.

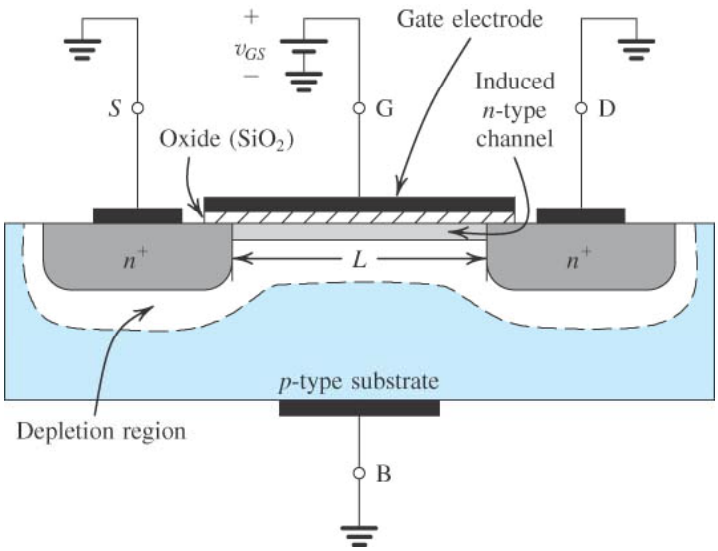


Figure 4.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

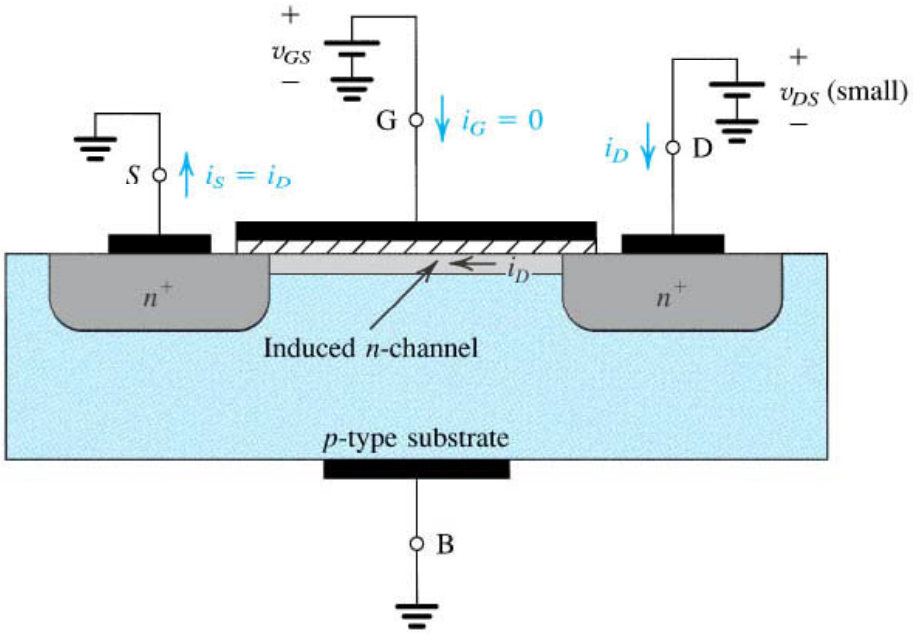


Figure 4.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)\, v_{DS}$. Note that the depletion region is not shown (for simplicity).

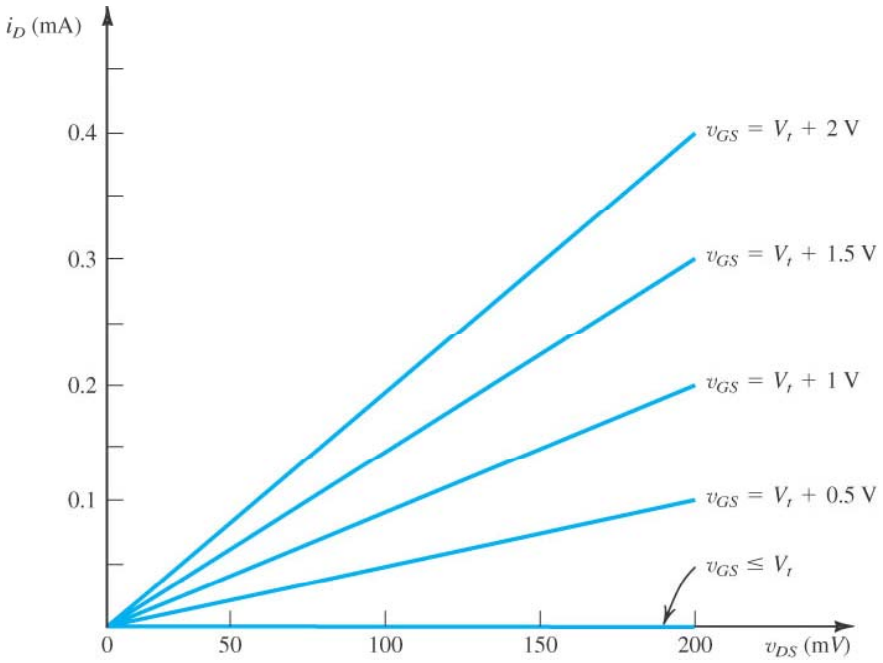


Figure 4.4 The i_D–v_{DS} characteristics of the MOSFET in Fig. 4.3 when the voltage applied between drain and source, $v_{DS,}$ is kept small. The device operates as a linear resistor whose value is controlled by v_{GS}.

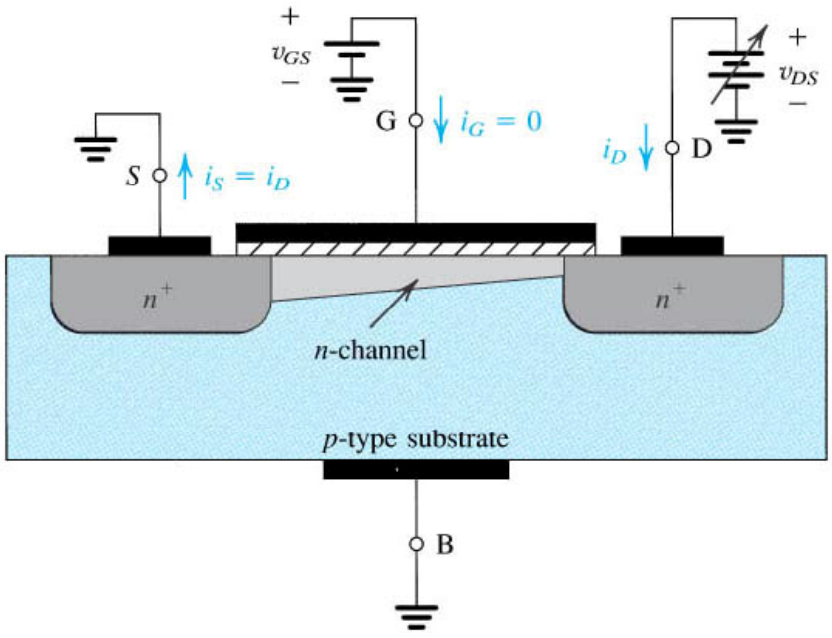


Figure 4.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t.

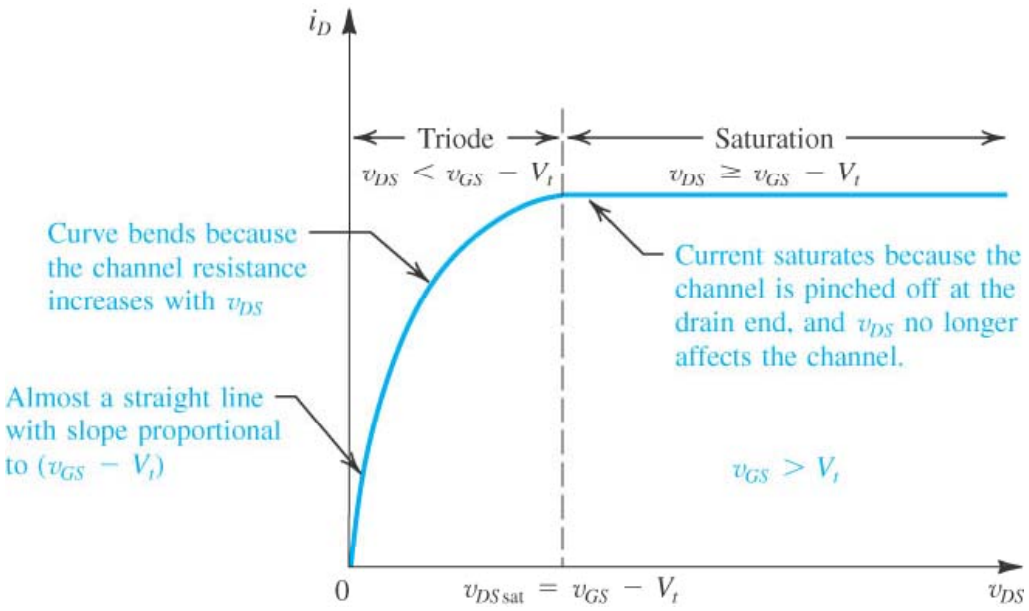


Figure 4.6 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$.

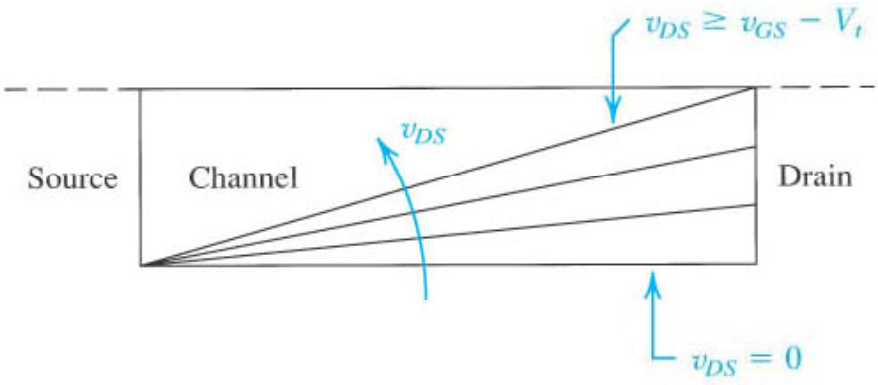


Figure 4.7 Increasing v_{DS} causes the channel to acquire a tapered shape. Eventually, as v_{DS} reaches $v_{GS} - V_t$, the channel is pinched off at the drain end. Increasing v_{DS} above $v_{GS} - V_t$ has little effect (theoretically, no effect) on the channel's shape.

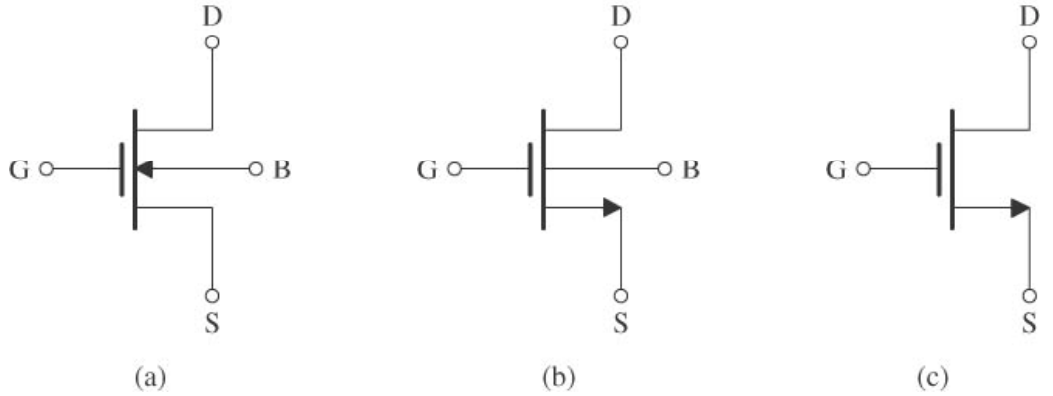


Figure 4.10 **(a)** Circuit symbol for the *n*-channel enhancement-type MOSFET. **(b)** Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). **(c)** Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

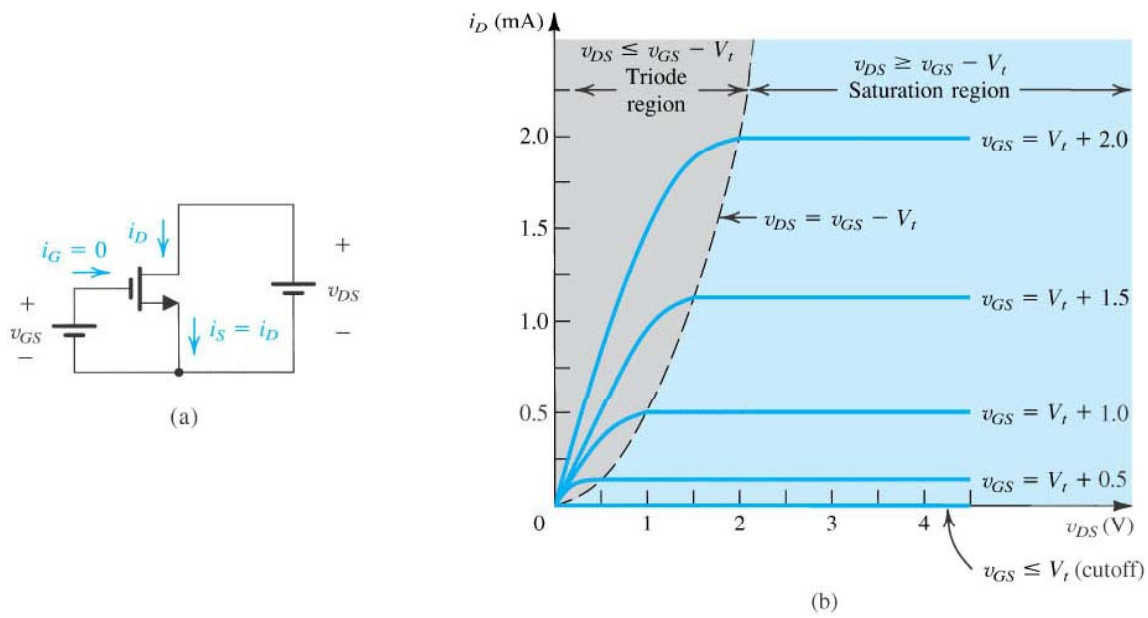


Figure 4.11 **(a)** An *n*-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. **(b)** The i_D–v_{DS} characteristics for a device with $k'_n(W/L) = 1.0$ mA/V^2.

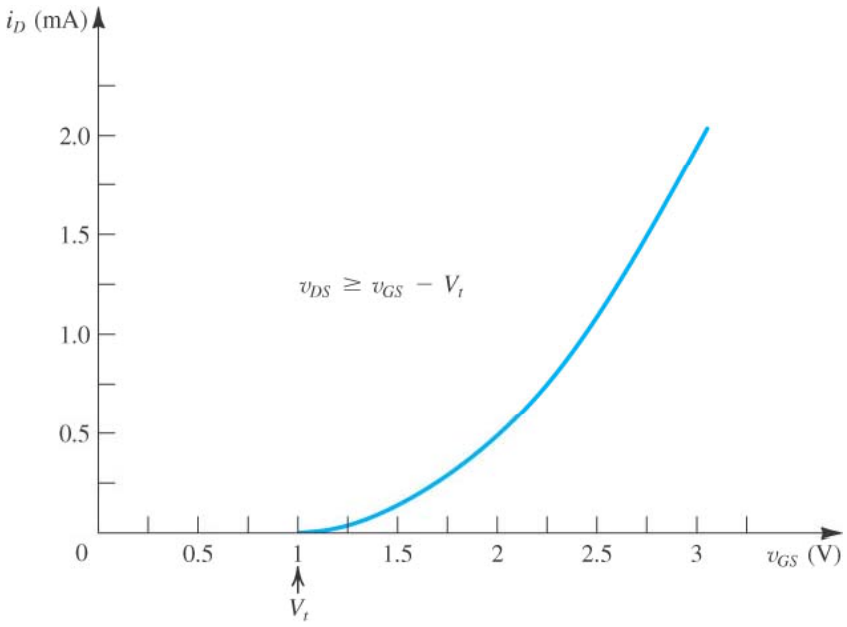


Figure 4.12 The i_D–v_{GS} characteristic for an enhancement-type NMOS transistor in saturation (V_t = 1 V, $k'_n W/L$ = 1.0 mA/V^2).

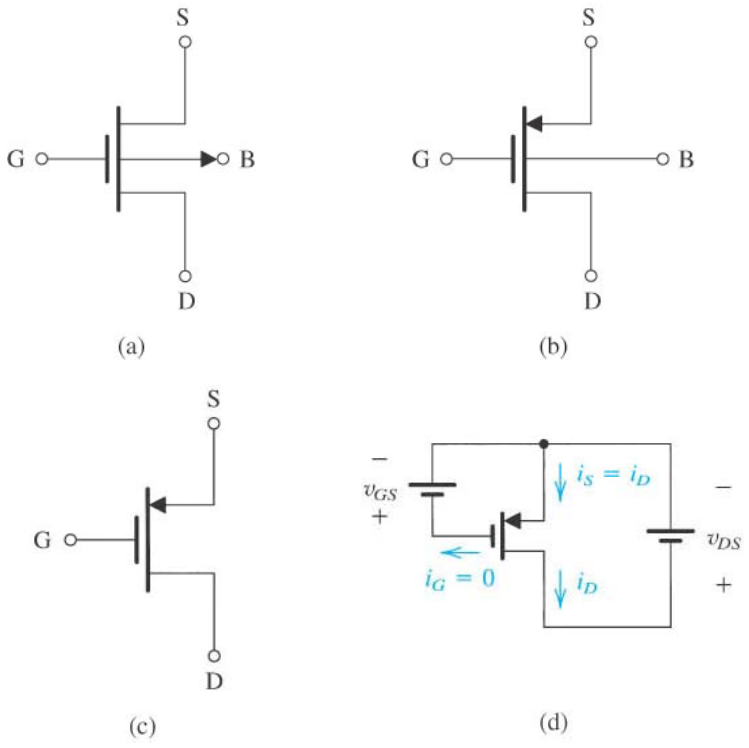


Figure 4.18 **(a)** Circuit symbol for the *p*-channel enhancement-type MOSFET. **(b)** Modified symbol with an arrowhead on the source lead. **(c)** Simplified circuit symbol for the case where the source is connected to the body. **(d)** The MOSFET with voltages applied and the directions of current flow indicated. Note that v_{GS} and v_{DS} are negative and i_D flows out of the drain terminal.

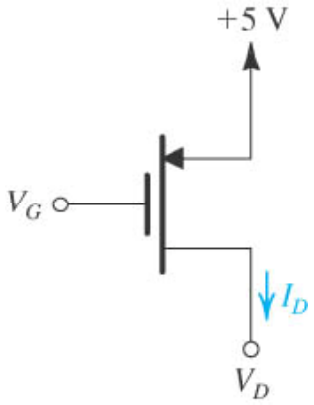


Figure E4.8

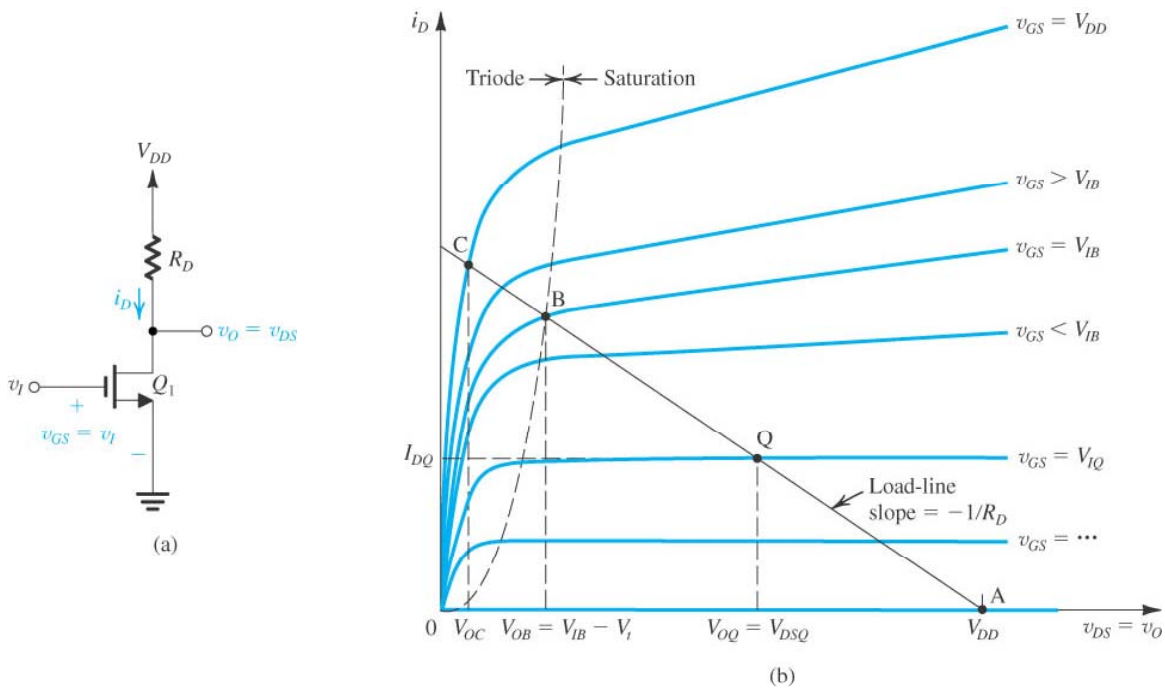


Figure 4.26 (a) Basic structure of the common-source amplifier. **(b)** Graphical construction to determine the transfer characteristic of the amplifier in (a).

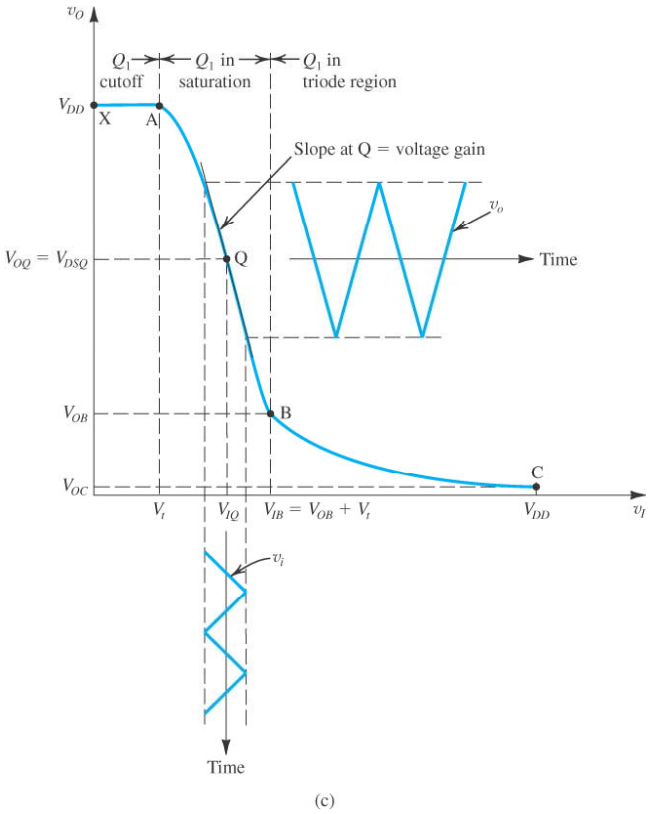


Figure 4.26 *(Continued)* **(c)** Transfer characteristic showing operation as an amplifier biased at point Q.

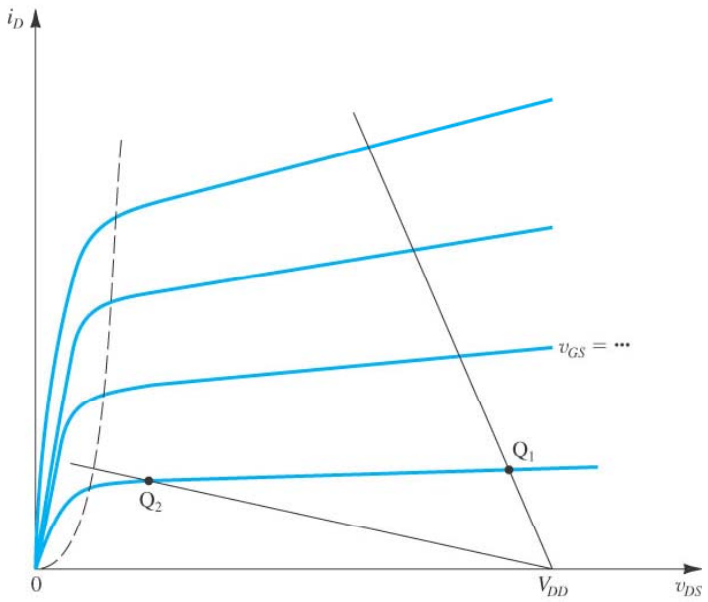


Figure 4.27 Two load lines and corresponding bias points. Bias point Q_1 does not leave sufficient room for positive signal swing at the drain (too close to V_{DD}). Bias point Q_2 is too close to the boundary of the triode region and might not allow for sufficient negative signal swing.

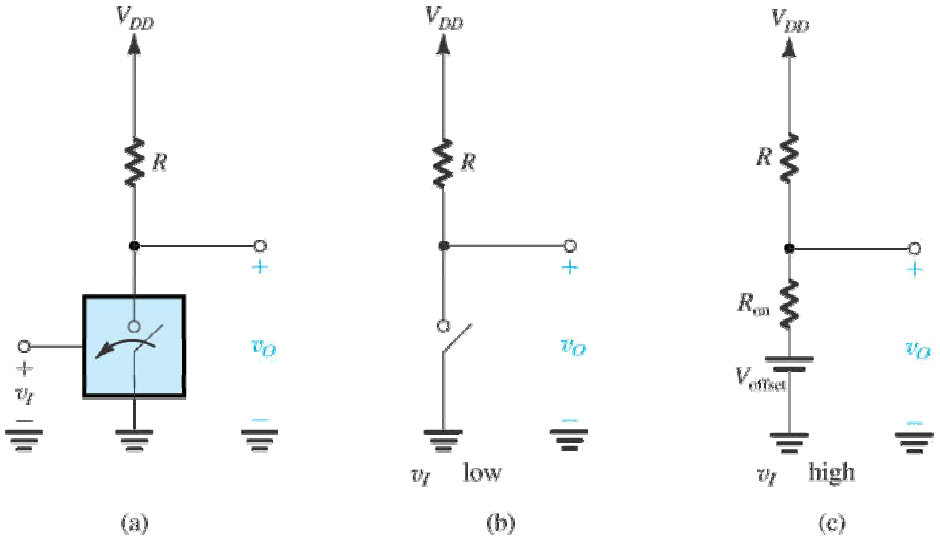


Figure 1.31 **(a)** The simplest implementation of a logic inverter using a voltage-controlled switch; **(b)** equivalent circuit when v_I is low; and **(c)** equivalent circuit when v_I is high. Note that the switch is assumed to close when v_I is high.

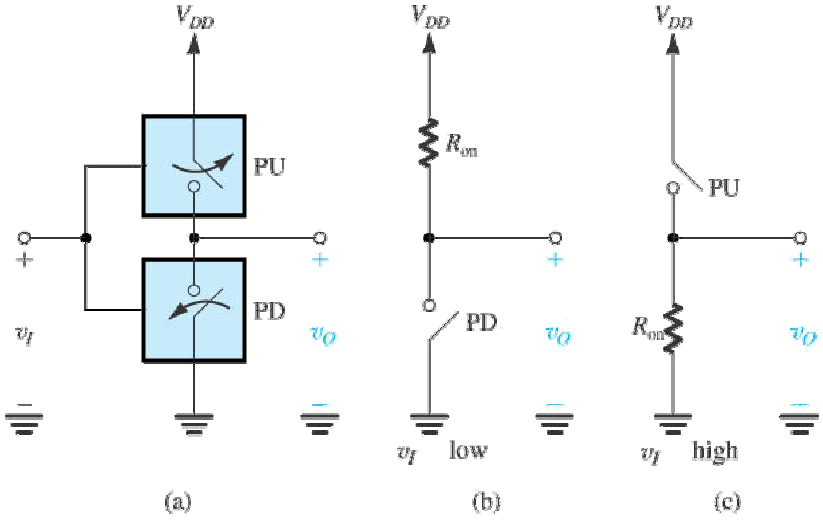


Figure 1.32 A more elaborate implementation of the logic inverter utilizing two complementary switches. This is the basis of the CMOS inverter studied in Section 4.10.

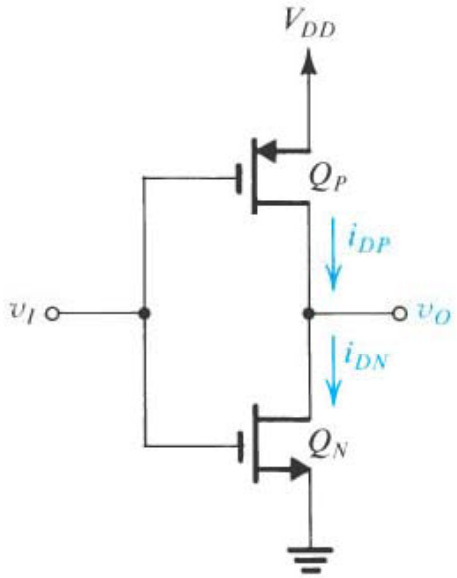


Figure 4.53 The CMOS inverter.

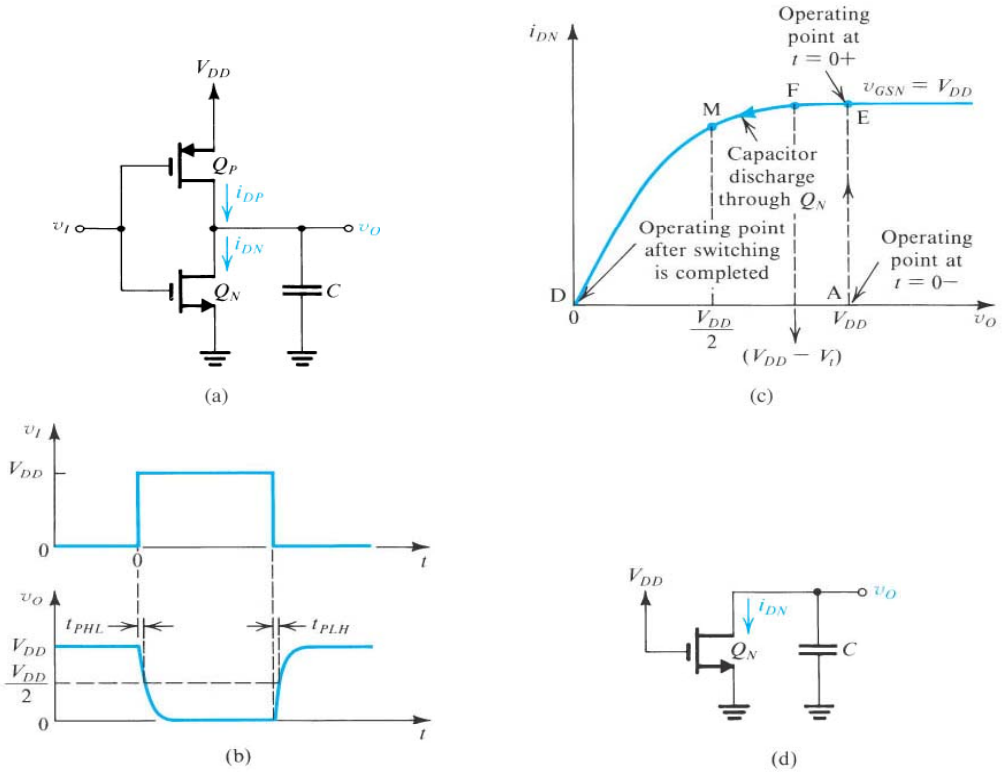


Figure 4.57 Dynamic operation of a capacitively loaded CMOS inverter: **(a)** circuit; **(b)** input and output waveforms; **(c)** trajectory of the operating point as the input goes high and C discharges through Q_N; **(d)** equivalent circuit during the capacitor discharge.

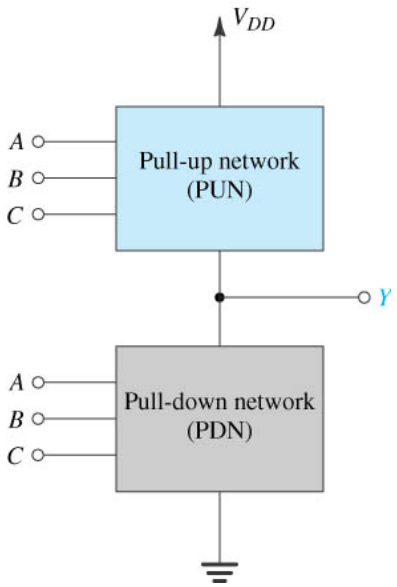


Figure 10.8 Representation of a three-input CMOS logic gate. The PUN comprises PMOS transistors, and the PDN comprises NMOS transistors.

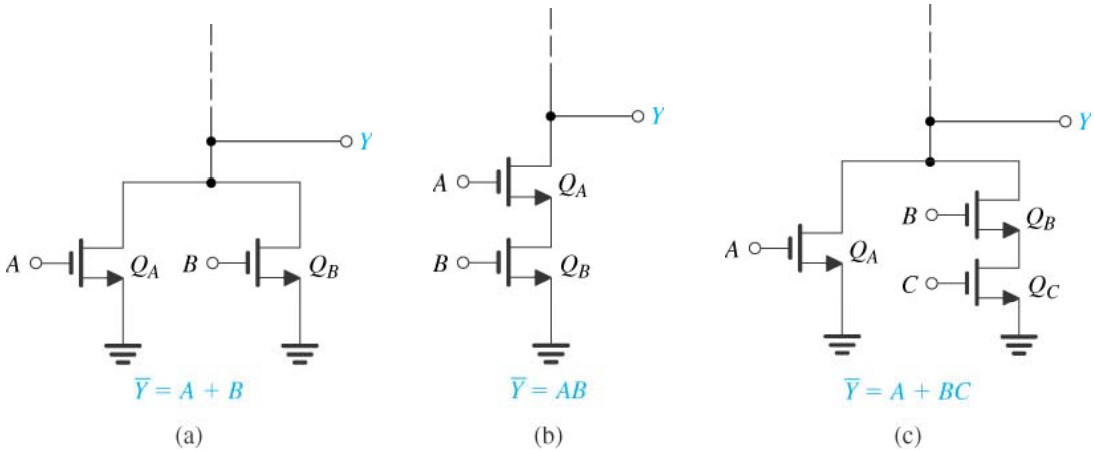


Figure 10.9 Examples of pull-down networks.

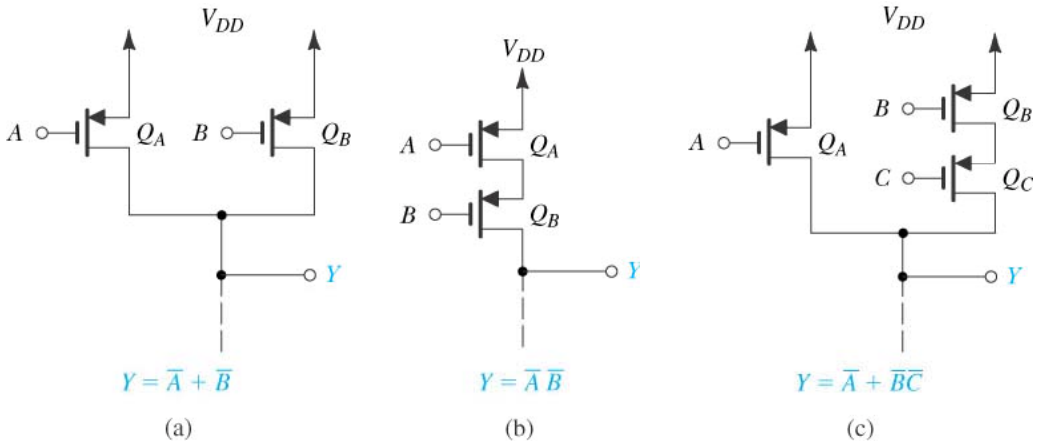


Figure 10.10 Examples of pull-up networks.

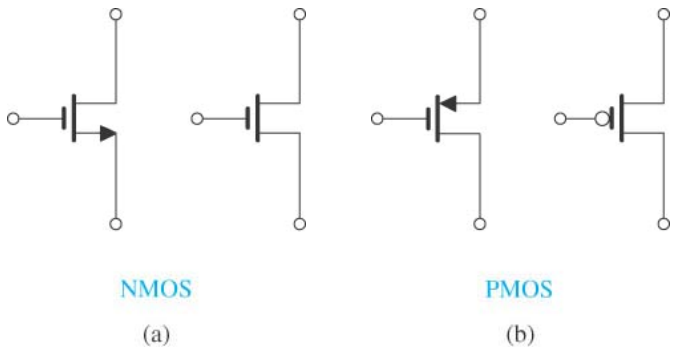


Figure 10.11 Usual and alternative circuit symbols for MOSFETs.

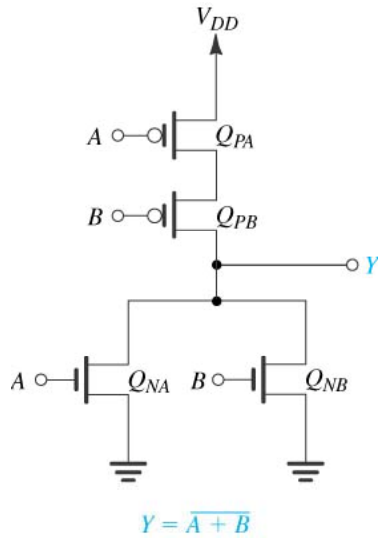


Figure 10.12 A two-input CMOS NOR gate.

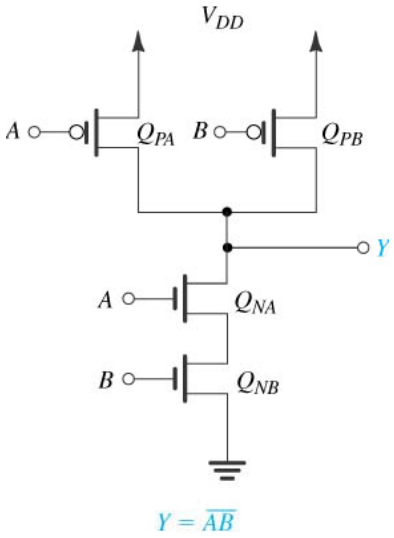


Figure 10.13 A two-input CMOS NAND gate.

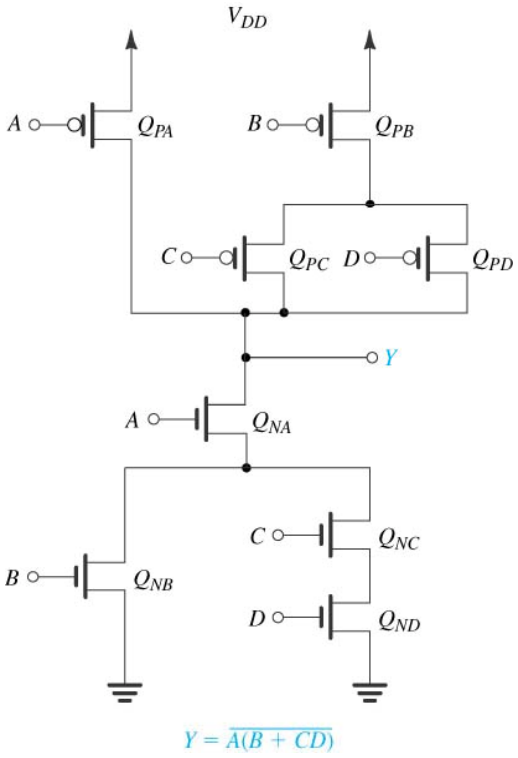


Figure 10.14 CMOS realization of a complex gate.

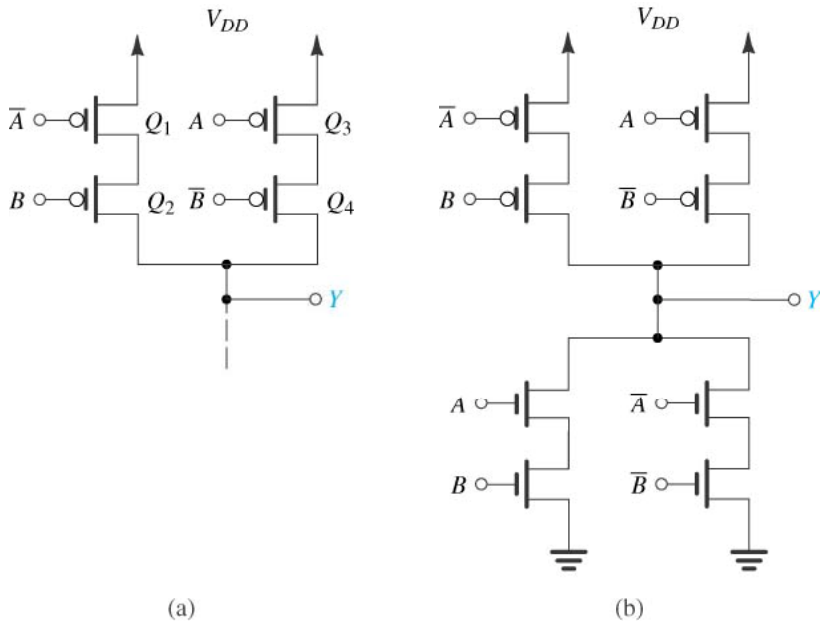


Figure 10.15 Realization of the exclusive-OR (XOR) function: **(a)** The PUN synthesized directly from the expression in Eq. (10.25). **(b)** The complete XOR realization utilizing the PUN in (a) and a PDN that is synthesized directly from the expression in Eq. (10.26). Note that two inverters (not shown) are needed to generate the complemented variables. Also note that in this XOR realization, the PDN and the PUN are not dual networks; however, a realization based on dual networks is possible (see Problem 10.27).

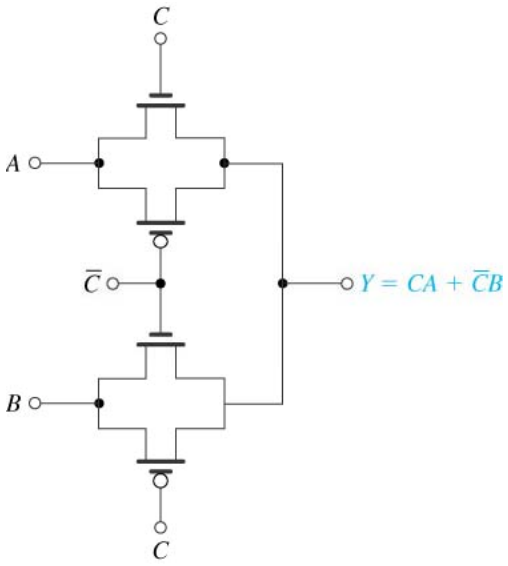


Figure 10.30 Realization of a two-to-one multiplexer using pass-transistor logic.

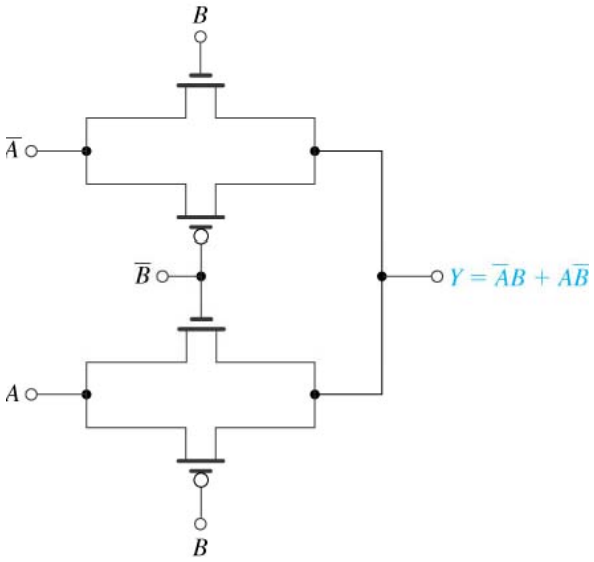
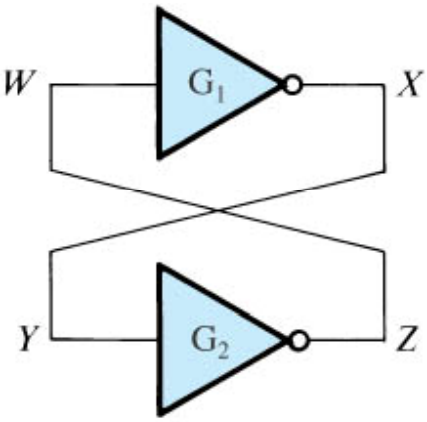
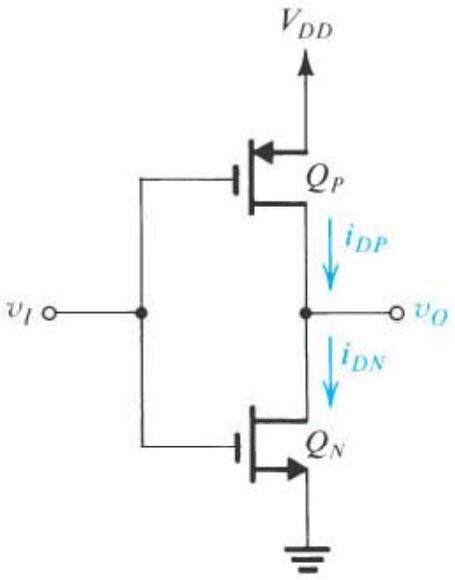


Figure 10.31 Realization of the XOR function using pass-transistor logic.

Basic Latch

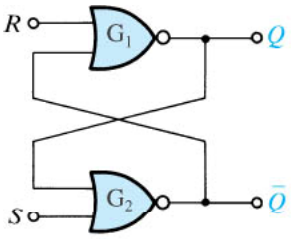


(a)



NOT gate

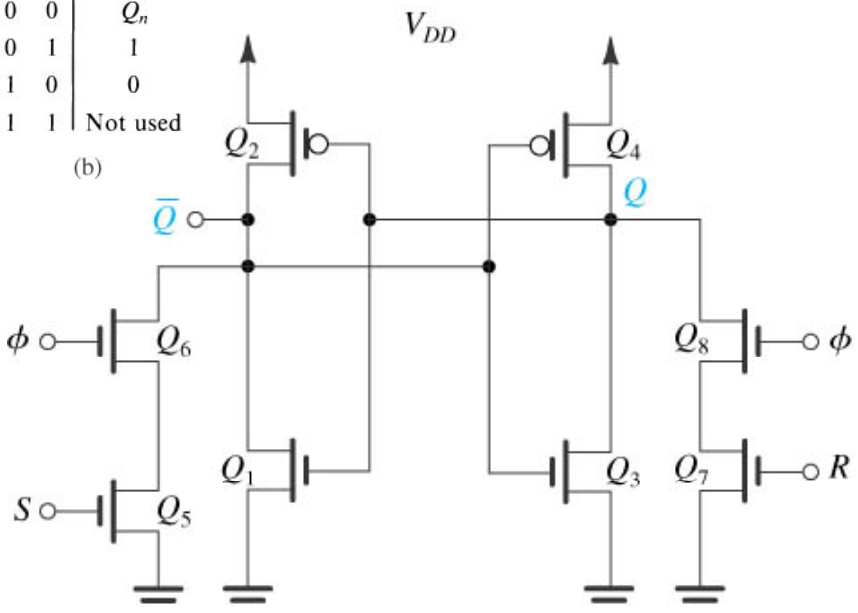
SR Flip-flop



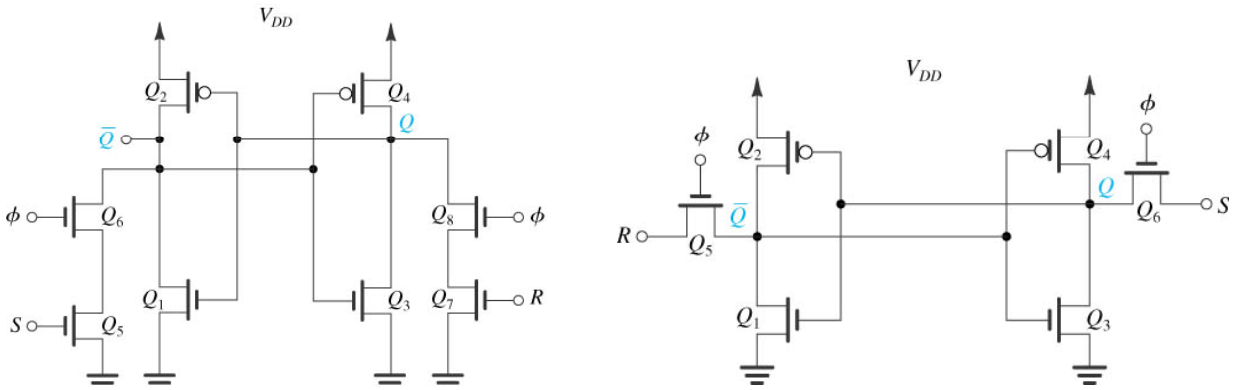
(a)

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	Not used

(b)



SR Flip-flop



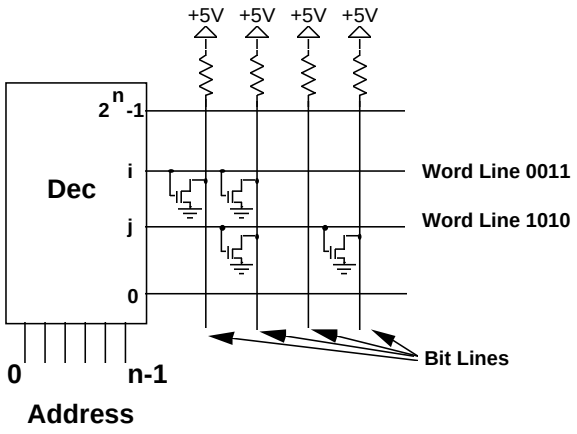
Read-Only Memories

ROM: Two dimensional array of 1's and 0's

Row is called a "word"; index is called an "address"

Width of row is called *bit-width* or *wordsize*

Address is input, selected word is output



Internal Organization

Taken from Katz's Contemporary Logic Design

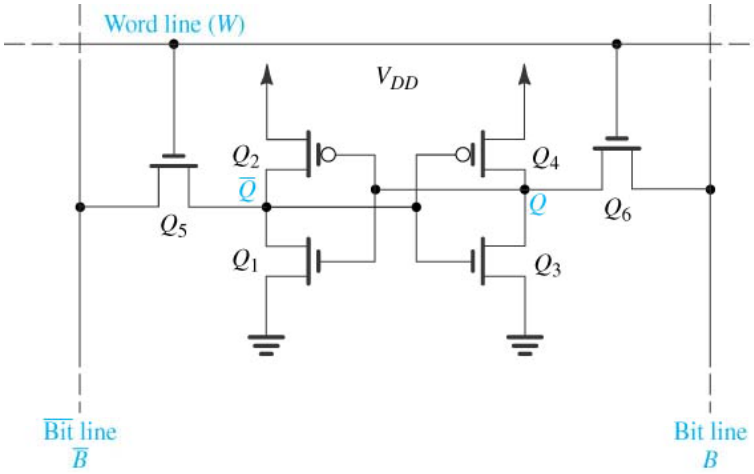


Figure 11.18 A CMOS SRAM memory cell.

Random Access Memories

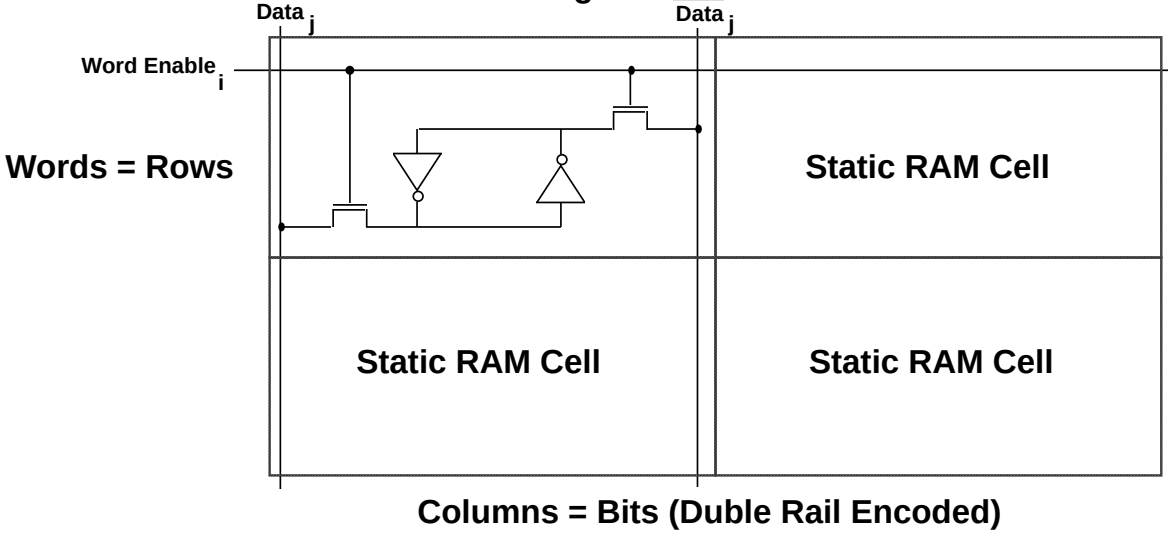
Static RAM

Transistor efficient methods for implementing storage elements

Small RAM: 256 words by 4-bit

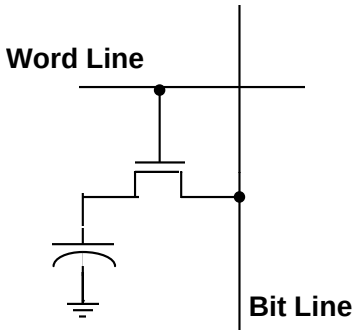
Large RAM: 4 million words by 1-bit

We will discuss a 1024 x 4 organization



Random Access Memories

Dynamic RAMs



1 Transistor (+ capacitor) memory element

Read: Assert Word Line, Sense Bit Line

Write: Drive Bit Line, Assert Word Line

Destructive Read-Out

Need for Refresh Cycles: storage decay in ms

Internal circuits read word and write back