1. Description

1.1. Project

Project Name	stm_config_official
Board Name	custom
Generated with:	STM32CubeMX 6.9.1
Date	05/10/2024

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration

3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Output	CAN_EN
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Output	RELAY_EN
9	PC1	I/O	TIM1_CH2	DRV2_IN1
10	PC2	I/O	TIM1_CH3	DRV2_IN2
11	PC3	I/O	ADC1_IN9	DRV2_VIP
12	VSSA	Power		
13	VDDA	Power		
16	PA2	I/O	TIM15_CH1	DRV1_IN1
17	PA3	I/O	TIM15_CH2	DRV1_IN2
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC2_IN1	DRV1_VIP
21	PA5	I/O	GPIO_EXTI5	END_SW
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	IMU_INT2
34	PB13 *	I/O	GPIO_Output	IMU_INT1
37	PC6	I/O	TIM8_CH1	ENC2B
38	PC7	I/O	TIM8_CH2	ENC2A
40	PC9	I/O	I2C3_SDA	
41	PA8	I/O	I2C3_SCL	
42	PA9	I/O	GPIO_EXTI9	USB_VB
43	PA10 *	I/O	GPIO_Output	USB_DP_DRV
44	PA11	I/O	USB_DM	
45	PA12	I/O	USB_DP	
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
50	PA15	I/O	GPIO_EXTI15	END_SW_BAK
51	PC10	I/O	GPIO_EXTI10	OPT_SW2
52	PC11	I/O	GPIO_EXTI11	OPT_SW1

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
53	PC12	I/O	UART5_TX	
54	PD2	I/O	UART5_RX	
56	PB4	I/O	TIM3_CH1	ENC1A
57	PB5	I/O	TIM3_CH2	ENC1B
58	PB6	I/O	I2C1_SCL	
59	PB7	I/O	I2C1_SDA	
60	BOOT0	Boot		
61	PB8	I/O	CAN_RX	
62	PB9	I/O	CAN_TX	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration
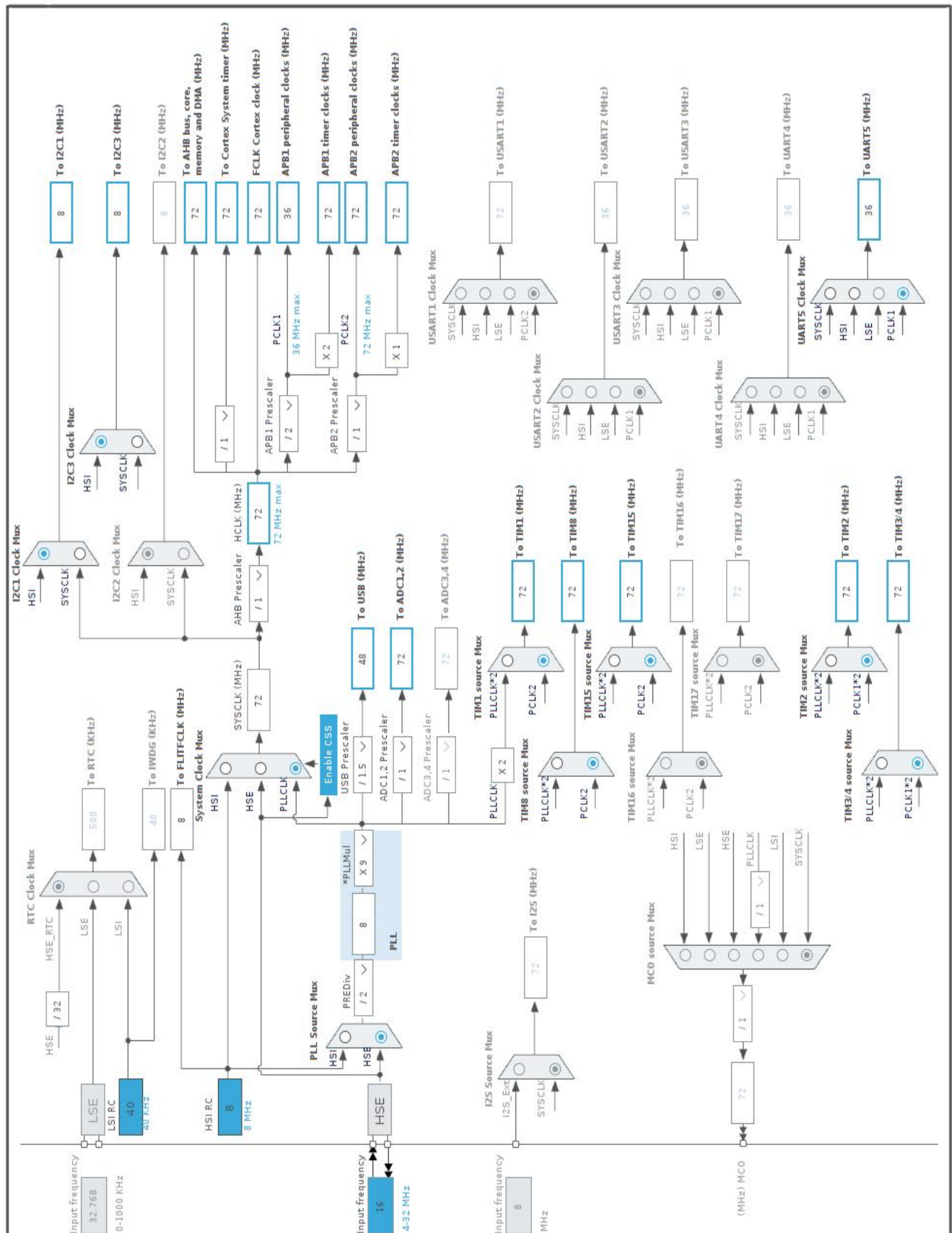
5. Software Project

5.1. Project Settings

Name	Value
Project Name	stm_config_official
Project Folder	/home/ov_robotarm/TTK4900_Masteroppgave/code/stm_config_official
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F3 V1.11.4
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	No
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC2_Init	ADC2
4	MX_CAN_Init	CAN
5	MX_TIM3_Init	TIM3
6	MX_TIM8_Init	TIM8
7	MX_TIM15_Init	TIM15
8	MX_I2C1_Init	I2C1
9	MX_UART5_Init	UART5
10	MX_I2C3_Init	I2C3
11	MX_TIM1_Init	TIM1

Rank	Function Name	Peripheral Instance Name
12	MX_USB_DEVICE_Init	USB_DEVICE
13	MX_TIM2_Init	TIM2
14	MX_ADC1_Init	ADC1
15	MX_TIM4_Init	TIM4
16	MX_TIM7_Init	TIM7

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303RETx
Datasheet	DS10362_Rev5

1.2. Parameter Selection

Temperature	25
Vdd	3.6

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSEBYP PLL	Regulator_LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	33.24 mA	9.8 µA
Duration	0.1 ms	0.9 ms
DMIPS	63.0	0.0
Ta Max	99.5	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	3.33 mA
Battery Life	1 month, 12 days, 1 hour	Average DMIPS	63.0 DMIPS

1.6. Chart
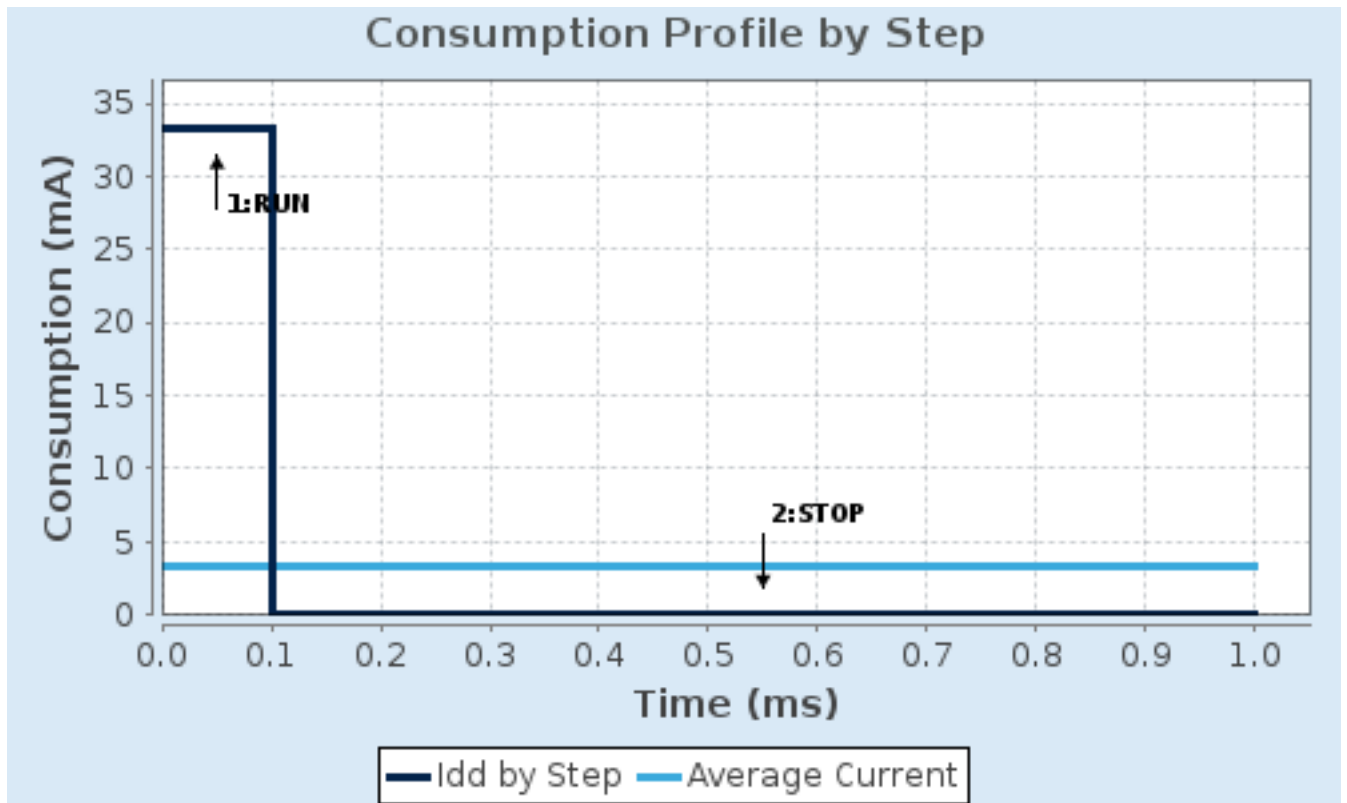
2. Peripherals and Middlewares Configuration

2.1. ADC1

mode: IN9

2.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
SequencerNbRanks	1
Rank	1
Channel	Channel 9
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	**true ***
Watchdog Mode	Single regular channel
Analog WatchDog Channel	Channel 9
High Threshold	**4000 ***
Low Threshold	0
Interrupt Mode	**Enabled ***

Analog Watchdog 2:

Enable Analog WatchDog2 Mode   false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode   false

2.2. ADC2
IN1: IN1 Single-ended
2.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
SequencerNbRanks	1
<u>Rank</u>	1
Channel	Channel 1
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	**true ***
Watchdog Mode	Single regular channel

Analog WatchDog Channel	Channel 1
High Threshold	**4000 ***
Low Threshold	0
Interrupt Mode	Disabled

Analog Watchdog 2:

| Enable Analog WatchDog2 Mode | false |

Analog Watchdog 3:

| Enable Analog WatchDog3 Mode | false |

2.3. CAN
mode: Activated
2.3.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**9 ***
Time Quantum	**250.0 ***
Time Quanta in Bit Segment 1	**2 Times ***
Time Quanta in Bit Segment 2	1 Time
Time for one Bit	1000
Baud Rate	**1000000 ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

| Operating Mode | Normal |

2.4. I2C1
I2C: I2C
2.4.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x2000090E

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

2.5. I2C3

I2C: I2C

2.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x0000020B ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

2.6. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

2.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

2.7. SYS
Debug: Serial Wire
Timebase Source: SysTick

2.8. TIM1
Clock Source   : Internal Clock
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
2.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2880 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High

BRK2 Filter (4 bits value)   0

Break And Dead Time management - Output Configuration:

Automatic Output State   Disable

Off State Selection for Run Mode (OSSR)   Disable

Off State Selection for Idle Mode (OSSI)   Disable

Lock Configuration   Off

Clear Input:

Clear Input Source   Disable

PWM Generation Channel 2:

Mode   PWM mode 1

Pulse (16 bits value)   0

Output compare preload   Enable

Fast Mode   Disable

CH Polarity   High

CH Idle State   Reset

PWM Generation Channel 3:

Mode   PWM mode 1

Pulse (16 bits value)   0

Output compare preload   Enable

Fast Mode   Disable

CH Polarity   High

CH Idle State   Reset

2.9. TIM2
Clock Source   : Internal Clock
2.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)   **7199 ***

Counter Mode   Up

Counter Period (AutoReload Register - 32 bits value)   **29 ***

Internal Clock Division (CKD)   No Division

auto-reload preload   Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)   Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO   Reset (UG bit from TIMx_EGR)

2.10. TIM3

Combined Channels: Encoder Mode

2.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
_____ Parameters for Channel 1 _____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
_____ Parameters for Channel 2 _____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

2.11. TIM4

Clock Source   : Internal Clock

2.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**719 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

2.12. TIM7

mode: Activated

2.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**7199 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**200 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

2.13. TIM8

Combined Channels: Encoder Mode

2.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
_____ Parameters for Channel 1 _____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
_____ Parameters for Channel 2 _____	
Polarity	Rising Edge

IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

2.14. TIM15

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

2.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2880 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable

Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

2.15. UART5
Mode: Asynchronous
2.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.16. USB
mode: Device (FS)
2.16.1. Parameter Settings:

Basic Parameters:

Speed	Full Speed 12MBit/s
Physical interface	Internal Phy

Power Parameters:

Low Power	Disabled
Link Power Management	Disabled

2.17. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

2.17.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message

Class Parameters:

USB CDC Rx Buffer Size	1024
USB CDC Tx Buffer Size	1024

2.17.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

* User modified value

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC3	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	DRV2_VIP
ADC2	PA4	ADC2_IN1	Analog mode	No pull-up and no pull-down	n/a	DRV1_VIP
CAN	PB8	CAN_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PB9	CAN_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	**High ***	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	**High ***	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	**High ***	
	PA8	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	**High ***	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PC1	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	DRV2_IN1
	PC2	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	DRV2_IN2
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENC1A
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENC1B
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENC2B
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENC2A
TIM15	PA2	TIM15_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	DRV1_IN1
	PA3	TIM15_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	DRV1_IN2
UART5	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
USB	PA11	USB_DM	n/a	n/a	n/a	
	PA12	USB_DP	n/a	n/a	n/a	
GPIO	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CAN_EN
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RELAY_EN
	PA5	GPIO_EXTI5	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	END_SW
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_INT2
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_INT1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA9	GPIO_EXTI9	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USB_VB
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_DP_DRV
	PA15	GPIO_EXTI15	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	END_SW_BAK
	PC10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	OPT_SW2
	PC11	GPIO_EXTI11	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	OPT_SW1

3.2. DMA configuration

nothing configured in DMA service

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
ADC1 and ADC2 interrupts	true	0	0
USB low priority or CAN_RX0 interrupts	true	0	0
EXTI line[9:5] interrupts	true	0	0
TIM2 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
UART5 global interrupt / UART5 wake-up interrupt through EXTI line 35	true	0	0
TIM7 global interrupt	true	0	0
USB low priority interrupt remap	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USB high priority or CAN_TX interrupts	unused		
CAN_RX1 interrupt	unused		
CAN_SCE interrupt	unused		
TIM1 break and TIM15 interrupts	unused		
TIM1 update and TIM16 interrupts	unused		
TIM1 trigger, commutation and TIM17 interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
I2C1 event global interrupt / I2C1 wake-up interrupt through EXTI line 23	unused		
I2C1 error interrupt	unused		
TIM8 break global interrupt	unused		
TIM8 update interrupt	unused		
TIM8 trigger and commutation interrupt	unused		
TIM8 capture compare interrupt	unused		
I2C3 event interrupt / I2C3 wake-up interrupt through EXTI line 27	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
I2C3 error interrupt	unused		
USB high priority interrupt remap	unused		
Floating point unit interrupt	unused		

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
ADC1 and ADC2 interrupts	false	true	true
USB low priority or CAN_RX0 interrupts	false	true	true
EXTI line[9:5] interrupts	false	true	true
TIM2 global interrupt	false	true	true
TIM4 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
UART5 global interrupt / UART5 wake-up interrupt through EXTI line 35	false	true	true
TIM7 global interrupt	false	true	true
USB low priority interrupt remap	false	true	true

* User modified value

4. System Views

4.1. Category view

4.1.1. Current

5. Docs & Resources

Type   Link