INF3410 — Fall 2015

Book Interrupt: Linear Circuit- and Small Signal Analysis

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Linear Circuits

Thévenin Equivalent Circuit

Small Signal Analysis

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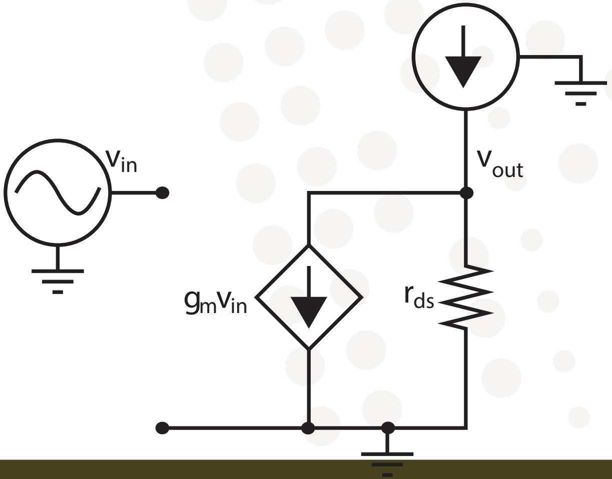
Linear Circuits: Definition

Linear circuits are circuits made up of linear elements, i.e. resistors, capacitors, inductors, and possibly 'artificial' elements such as voltage- or current-dependent voltage- or current-sources. The dynamics of linear circuits can be described by linear differential equations. For a DC analysis (capacitors are open circuits and inductors short circuits), this simplifies to linear equations (i.e. without 'differential').

Linear Circuits Analysis

If one defines an input and an output node of a linear circuit one can compute the total impedance/admittance or generally its transfer function $H(s)$ or $H(j\omega)$ (i.e. $\frac{O(s)}{I(s)}$ where I stands for 'input' and O for output) between those two points. That's simple in the DC case, e.g. by applying Kirchhoff to get a set of equations and solve them. The transfer function is a constant, i.e. the DC gain then. It gets more tricky if one has elements such as capacitors and inductors and non-DC signals. Then we will resort to an analysis in the s-plane resulting in a transfer function that shows the gain to be dependent on the frequency of the input signal... but more of that later.

Linear Circuit Example: Intrinsic MOS FET Gain



Example Analysis: Intrinsic MOS FET Gain

$$v_{out}\frac{1}{r_{ds}} - g_m v_{in} = 0$$

$$\frac{v_{out}}{v_{in}} = g_m r_{ds}$$

Linear Circuit Analysis s-Plane

Once you do have capacitors and inductors in your circuit it gets more complicated. Let us first learn about how to do this by applying s-plane analysis by just learning some rules without actually knowing why they work.

s-Plane Manipulation Rules

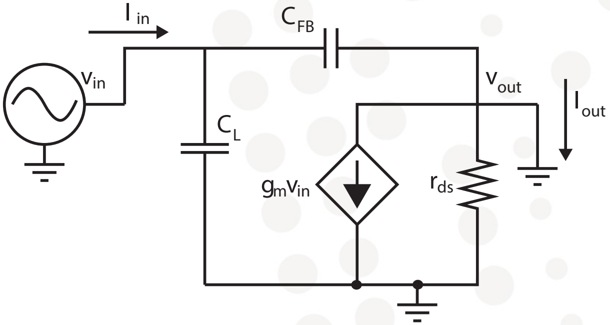
Use Kirchhoff again to obtain a set of equations, but use the s-plane notation impedances and/or admittances for capacitors and inductors (next slide). At the very end you substitute s with $j\omega$, where j is the imaginary unit and ω is the frequency in rad of a sinusoidal input signal. Then the transfer function can be solved for a given ω and the absolute value of that complex solution is the gain of the output at that frequency and the and the angle of the complex solution is the phase of the output.

Impedances/Admittances of Linear Circuit Elements

	impedance	admittance
resistor:	R	$\frac{1}{R}$
capacitor:	$\frac{1}{sC}$	sC
inductor:	sL	$\frac{1}{sL}$

Ideal sources (e.g. the $i_d = g_m v_{gs}$ sources in small signal models of FETs) are left as they are.

Linear Circuit Example: Intrinsic MOS FET Speed



Example Analysis: Intrinsic MOS FET Speed

$$I_{in} - V_{in}s(C_{FB} + C_L) = 0 \quad I_{in} = V_{in}s(C_{FB} + C_L)$$

$$I_{out} + V_{in}sC_{FB} - g_m V_{in} = 0 \quad I_{out} = g_m V_{in} - V_{in}sC_{FB}$$

$$\frac{I_{out}}{I_{in}} = \frac{g_m V_{in} - V_{in}sC_{FB}}{V_{in}s(C_{FB}+C_L)}$$

$$\frac{I_{out}}{I_{in}} = \frac{g_m - sC_{FB}}{s(C_{FB}+C_L)} \approx \frac{g_m}{s(C_{FB}+C_L)}$$

$$\left|\frac{I_{out}(j\omega)}{I_{in}(j\omega)}\right| \approx \frac{g_m}{\omega(C_{FB}+C_L)}$$

$$\left|\frac{I_{out}(j\omega)}{I_{in}(j\omega)}\right| \stackrel{!}{=} 1 \Rightarrow \omega_t \approx \frac{g_m}{C_{FB}+C_L}$$

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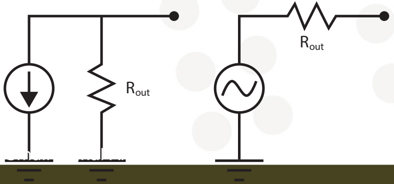
Small Signal Analysis

Thévenin equivalent circuit

Linear circuits when probed at two points can be replaced with the Thevenin equivalent circuit: with a voltage source (equivalent to the voltage accross those two points when they are open circuit) in series with an impedance (the impedance between those two points when all independent voltage sources are short circuited and all independent current sources are open circuited). Typically for this course one of the two nodes is Gnd, as we'll mainly talk about output resistance.



Testing Thévenin equivalent output resistance

The Thévenin equivalent resistance (let's stick with resistance for now, i.e. no capacitors/inductors) at the output node of a linear circuit is the rate of change of voltage when forcing a current into that node.

$$R_{out} = \frac{\partial V_{out}}{\partial I_{out}}$$

An ideal voltage source has a zero output resistance and an ideal current source has infinite output resistance. Input and output resistance are important when connecting circuits together: a large output resistance and small input resistance keep current signals unaffected, and the opposite is good for voltage signals.

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Small Signal Analysis: Why?

Small Signal Analysis is most commonly used to analyse amplifiers to determin such parameters as output resistance r_{out} and voltage gain A at either DC or frequency dependent. It translates a rather complicated non-linear circuit into a linear approximation around a point of operation which then can be analyzed using linear circuit analysis methods.

Small Signal Analysis: How? (1/2)

1. Compute Large signal operation point and all relevant small signal parameters at that point, e.g. g_m, r_{ds} ...
2. Replace Large Signal Schematics with the corresponding small signal circuits.
3. Decide where you want to put a probing input and where you want to measure an output, e.g. you might have a probing voltage input at the input node and measure the voltage at the output node to compute a transfer function, or you might put a probing current input at the output node and measure the output voltage to determine the output resistance.

Small Signal Analysis: How? (2/2)

4. Replace all constant voltage sources with a short circuit and all constant current sources with an open circuit. Note: when measuring output resistance a current source $V_{in}g_m$ actually becomes constant as V_{in} is constant and can thus be replaced with an open circuit.
5. Perform a linear circuit analysis. For DC/low frequency analysis, capacitors can be replaced by open circuits and inductors by short circuit. For a frequency dependent/high frequency analysis use s-plane analysis, i.e. complex impedances. For the transfer function, get the resulting expression into root form and use the rules pertaining zeros and poles to draw a bode plot (later in chapter 4).