

INF3410, fall 2013, Final Exam Solution

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January 13, 2014

Chapter 1

Task 1 (4p): Compute the intrinsic gain and speed of NMOS Transistors with $W/L=1$ and L equal to three times the minimum length for the 0.35um in table 1 for a drain current of $20\mu A$.

Intrinsic gain:

$$A_i = g_m r_{ds}$$

NMOS:

$$g_{mn} = \sqrt{2\mu_n C_{ox}(W/L)I_D} = \sqrt{2 * 190\mu A/V^2 * 1 * 20\mu A} = 8.72 * 10^{-5} S$$

PMOS:

$$g_{mp} = \sqrt{2\mu_n C_{ox}(W/L)I_D} = \sqrt{2 * 55\mu A/V^2 * 1 * 20\mu A} = 4.69 * 10^{-5} S$$

NMOS & PMOS:

$$r_{ds} \approx \frac{1}{\lambda I_D} = \frac{3 * 0.35 * 10^{-6}}{0.16 * 10^{-6} * 20 * 10^{-6}} = 328 k\Omega$$

NMOS:

$$A_i = 28.60$$

PMOS:

$$A_i = 15.39$$

Table 1.5 MOSFET parameters representative of various CMOS technologies and used for rough hand calculations in this text.

	0.8 μm		0.35 μm		0.18 μm		45 nm	
Technology	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
μC_{ox} ($\mu\text{A}/\text{V}^2$)	92	30	190	55	270	70	280	70
V_{t0} (V)	0.80	-0.90	0.57	-0.71	0.45	-0.45	0.45	-0.45
$\lambda \cdot L$ ($\mu\text{m}/\text{V}$)	0.12	0.08	0.16	0.16	0.08	0.08	0.10	0.15
C_{ox} ($\text{fF}/\mu\text{m}^2$)	1.8	1.8	4.5	4.5	8.5	8.5	25	25
t_{ox} (nm)	18	18	8	8	5	5	1.2	1.2
n	1.5	1.5	1.8	1.7	1.6	1.7	1.85	1.85
θ ($1/\text{V}$)	0.06	0.135	1.5	1.0	1.7	1.0	2.3	2.0
m	1.0	1.0	1.8	1.8	1.6	2.4	3.0	3.0
$C_{ov}/W = L_{ov}C_{ox}$ ($\text{fF}/\mu\text{m}$)	0.20	0.20	0.20	0.20	0.35	0.35	0.50	0.50
$C_{db}/W \approx C_{sb}/W$ ($\text{fF}/\mu\text{m}$)	0.50	0.80	0.75	1.10	0.50	0.55	0.45	0.50

Table 1.5
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Table 1: Typical process parameters

Intrinsic Speed (unity gain frequency):

$$f_t \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

$$C_{gs} \approx 2/3 * WLC_{ox} + WL_{ov}C_{ox} = 2/3 * 4.5e-15 * 9 * 0.35^2 + 3 * 0.35 * 0.2e-15 = 3.52\text{fF} \quad (1.91)$$

$$C_{gd} = C_{ov} = 0.2 * 10^{-15} * 3 * 0.35 = 0.21\text{fF}$$

NMOS:

$$f_t \approx \frac{g_{mn}}{2\pi(C_{gs} + C_{gd})} = \frac{8.72 * 10^{-5} \text{A/V}}{2\pi * 3.73\text{fF}} = 3.72\text{GHz}$$

Without overlapps (slightly wrong):

$$f_t \approx \frac{g_{mn}}{2\pi(2/3 * WLC_{ox})} = \frac{8.72 * 10^{-5} \text{A/V}}{2\pi * 3.31\text{fF}} = 4.19\text{GHz}$$

Others have used the equations:

$$A_i \approx \frac{2}{\lambda V_{eff}}$$

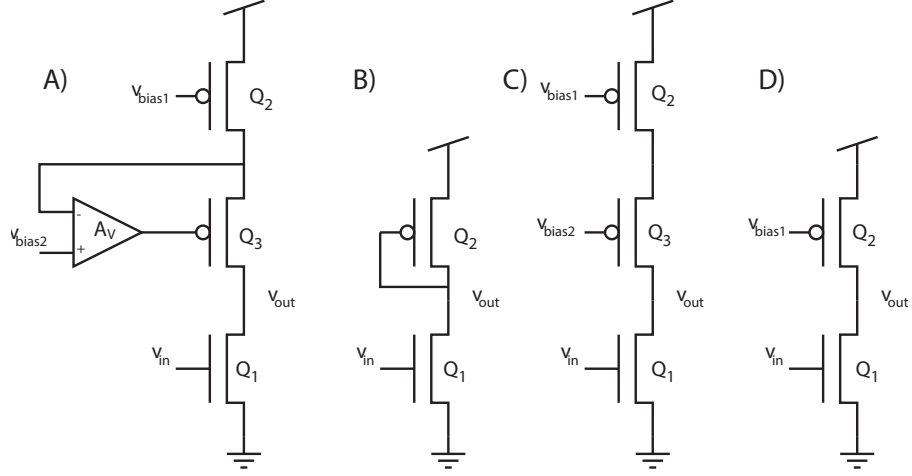


Figure 1: Common source gain stages with different loads

$$g_m = \mu C_{ox} \frac{W}{L} * V_{eff}$$

$$V_{eff} = \sqrt{\frac{2I_D}{\mu C_{ox} \frac{W}{L}}}$$

Which can be used to get a simple expression when neglecting C_{gd} and the overlap term for C_{gs} :

$$f_t \approx \frac{6\mu}{4\pi L^2 * A_i}$$

PMOS:

$$f_t \approx \frac{g_{mp}}{2\pi(C_{gs} + C_{gd})} = \frac{4.69 * 10^{-5} \text{A/V}}{2\pi 3.73 \text{fF}} = 2.00 \text{GHz}$$

Without overlaps (slightly wrong):

$$f_t \approx \frac{g_{mn}}{2\pi(2/3 * WLC_{ox})} = \frac{4.69 * 10^{-5} \text{A/V}}{2\pi 3.31 \text{fF}} = 2.25 \text{GHz}$$

Chapter 3

Task 2 (2p): Figure 1 shows common source gain stages with different loads. Assume that all transistors are in saturation and in strong inversion and biased at the same DC current. Please order them according to how much small signal low frequency voltage gain you assume they will have, i.e. make a list beginning with the circuit with the highest gain and ending with the lowest.

The load with the highest resistance leads to the highest output resistance and gain

$$A = g_{m1}r_{out} = g_{m1}(r_{ds1} \parallel R_L)$$

A) C) D) B)

Task 3 (4p): Find small signal low frequency expressions for output resistance and voltage gain for all the circuits in fig. 1. Ignore the body effect.

As already stated:

$$A = g_{m1}r_{out} = g_{m1}(r_{ds1} \parallel R_L)$$

Expressions for R_L :

A)

$$R_L \approx g_{mp}r_{dsp}^2(1 + A) \quad (6.82)$$

C)

$$R_L = g_{mp}r_{dsp}^2 \quad (3.37)$$

D)

$$R_L = r_{dsp} \quad (3.2) \& Fig. 3.3$$

B)

$$R_L = \frac{1}{g_{mp}} \quad Fig. 3.2$$

1 Chapter 4

Task 4 (4p): Complete the bode plots in figure 2. Sketch the expected corresponding magnitude/phase plot. Indicate all important points and explicitly give their phase and rad/s values! Write down the corresponding transfer function. If there are several solutions, sketch all of them! (Note that the phase plots are piece-wise linear approximations where 90° phase transitions are assumed to be linear in a log-log plot and complete during one decade. Please use a similar convention for your sketches!)

See Fig, 3

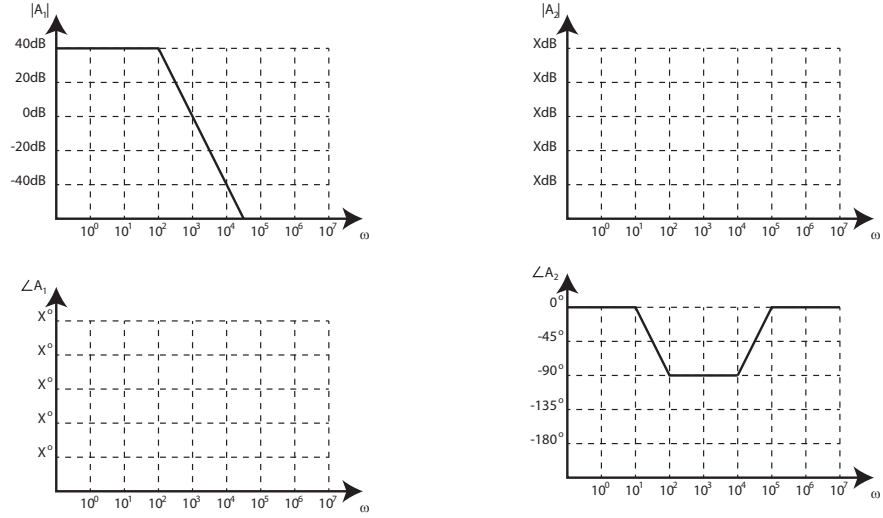


Figure 2: Incomplete Bode plots

Task 5 (4p): Write down the corresponding transfer functions for the Bode plots. If there are several solutions, write all of them!

A_0 shall be 100

$$A_1(s) = A_0 \frac{1}{(1 + \frac{s}{\omega_0})^2}$$

where $\omega_0 = 100\text{rad/s}$

$$A_{2a}(s) = A_0 \frac{1 + \frac{s}{z_0}}{1 + \frac{s}{\omega_0}}$$

where $\omega_0 = 10^{1.5} = 31.623\text{rad/s}$ and $z_0 = 10^{4.5} = 31623\text{rad/s}$

OR

$$A_{2b}(s) = A_0(1 - \frac{s}{z_0})(1 + \frac{s}{z_1})$$

where $z_0 = 10^{1.5} = 31.623\text{rad/s}$ and $z_1 = 10^{4.5} = 31623\text{rad/s}$

2 Chapter 5

Task 6 (4p): Figure 4 shows the small signal model of a two stage amplifier with negative feedback. The given parameters are $g_{m1} = g_{m2} = 3\text{mA/V}$,

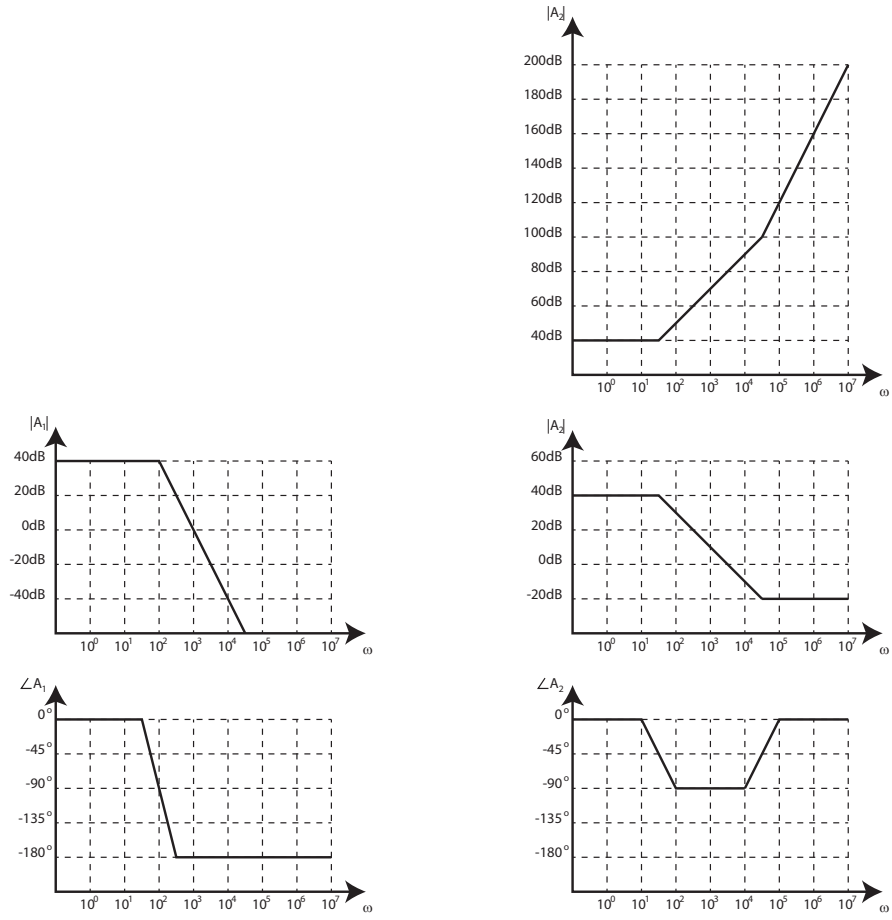


Figure 3: Completed Bode plots

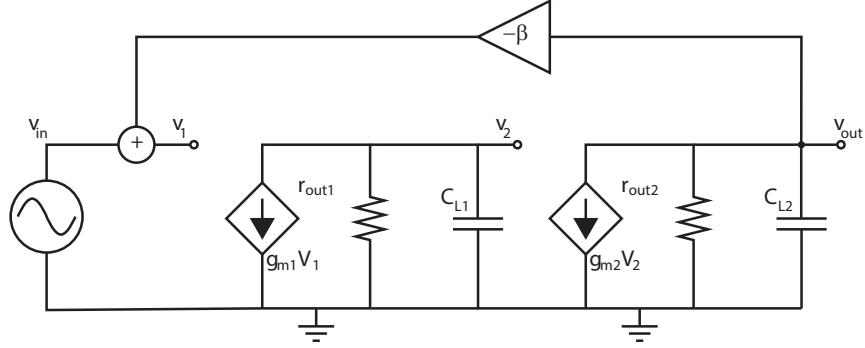


Figure 4: Small signal model of a two stage amplifier with negative feedback

$r_{out1} = r_{out2} = 10\text{k}\Omega$, $C_{L1} = 100\text{pF}$, $C_{L2} = 1\text{pF}$. What is the open loop transfer function (i.e. ignoring the feedback $-\beta$)?

$$\begin{aligned}
 A(s) &= \frac{g_{m1}r_{out1}}{1 + sr_{out1}C_{L1}} \frac{g_{m2}r_{out2}}{1 + sr_{out2}C_{L2}} \\
 &= \frac{3\text{mA/V}10\text{k}\Omega}{1 + s10\text{k}\Omega100\text{pF}} \frac{3\text{mA/V}10\text{k}\Omega}{1 + s10\text{k}\Omega1\text{pF}} \\
 &= \frac{30}{1 + \frac{s}{1\text{Mrad/s}}} \frac{30}{1 + \frac{s}{100\text{Mrad/s}}}
 \end{aligned}$$

thus

$$\begin{aligned}
 \omega_1 &= \frac{1}{10e3 * 100e-12} = 1\text{Mrad/s} \\
 \omega_2 &= \frac{1}{10e * 1e-12} = 100\text{Mrad/s}
 \end{aligned}$$

and

Task 7 (4p): Find the value for β that will make the second pole frequency the exact same as the unity loop gain frequency ω_t . What will be the phase margin of this circuit?

To find the unity loop gain frequency ω_t set:

$$|A(j\omega_2)| = \frac{1}{\beta}$$

$$\beta = \frac{1}{|A(j\omega_2)|}$$

A trick:
 $|A(j\omega_2)|$ will be:

$$|A(j\omega_2)|[dB] = |A(0)|[dB] - (\omega_2[decade] - \omega_1[decade]) * 20 - 3dB = |A(0)|[linear] / 100 * 0.7079 = 9 * 0.7079 = 6.37$$

$$\beta = \frac{1}{|A(j\omega_2)|} = \frac{1}{6.37} = 0.1569$$

(neglecting the -3dB is also close and would yield

$$\beta = \frac{1}{|A(j\omega_2)|} = \frac{1}{9} = 0.1111$$

The phase margin shall be 45°

3 Chapter 6

Task 8 (4p): Figure 5 depicts a variant of a current mirror implemented with the $0.35\mu\text{m}$ process parameters from table 1. All transistors are $2\mu\text{m}$ wide 1μ long. Assume an input current of $20\mu\text{A}$. Compute the optimal V_{bias} for that particular input current that allows for maximal output swing while still keeping all transistors in saturation!

$$V_{eff} = \sqrt{\frac{2I_D}{\mu_n C_{ox} W/L}} = 0.32V$$

$$V_{bias} = 2 * V_{eff} + V_{tn} = 1.21V$$

4 Chapter 9

Task 9 (4p): An inverter is implemented with MOS FETs of the $0.35\mu\text{m}$ process described in table 1, where both the pMOS and nMOS transistors have $W=L=1\mu\text{m}$. Find the operation point where the inverter acts as an amplifier (i.e. an input voltage where the drain currents of both transistors are the same. Compute the individual transconductances g_{mn} and g_{mp} for the transistors and the inverter's voltage gain A .

$$190(V_x - 2 * 0.57V_x + 0.57^2) = 55(V_x - 2 * 2.59V_x + 2.59^2) \quad (1)$$

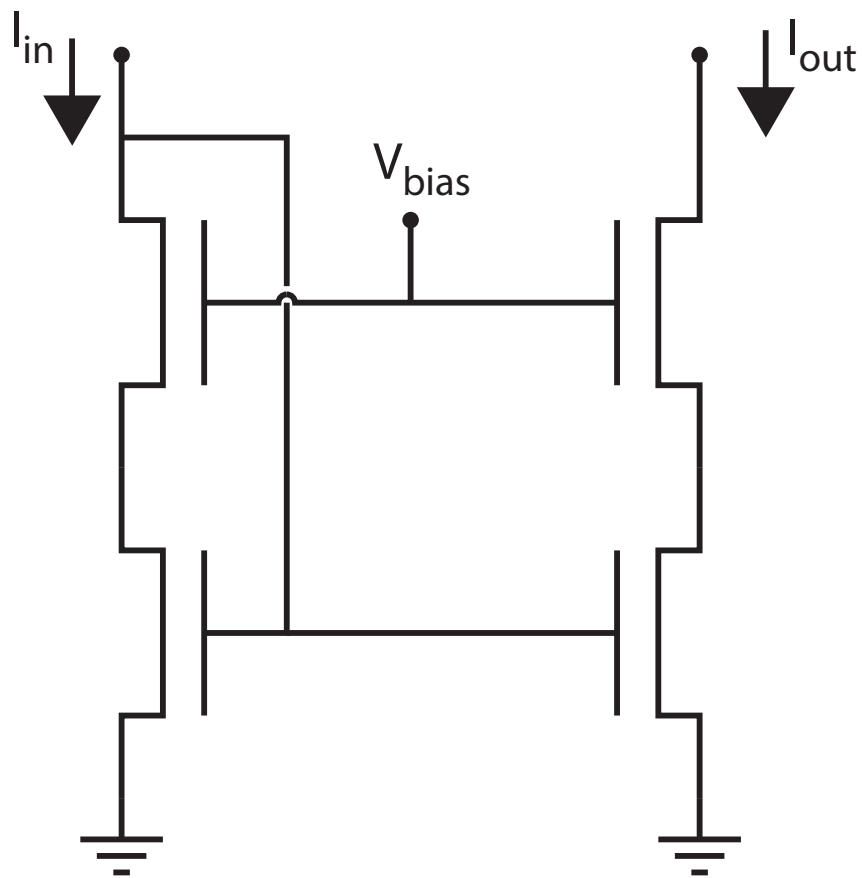


Figure 5: Current mirror variant


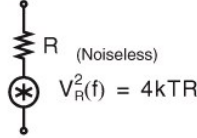
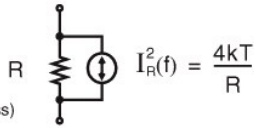

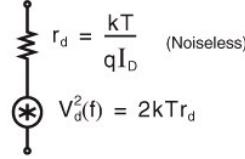
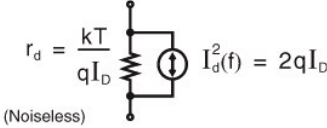

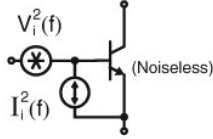

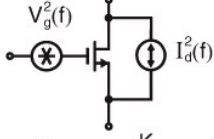
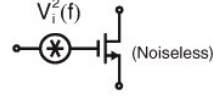
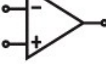
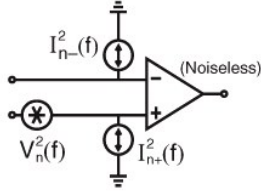
Element	Noise Models	
Resistor 		
Diode  (Forward biased)		
BJT  (Active region)		$V_i^2(f) = 4kT \left(r_b + \frac{1}{2g_m} \right)$ $I_i^2(f) = 2q \left(I_B + \frac{KI_B}{f} + \frac{I_C}{ \beta(f) ^2} \right)$
MOSFET  (Active region)	 $V_g^2(f) = \frac{K}{WLC_{ox}f}$ $I_d^2(f) = 4kT \left(\frac{2}{3} \right) g_m$	 $V_i^2(f) = 4kT \left(\frac{2}{3} \right) \frac{1}{g_m} + \frac{K}{WLC_{ox}f}$ <p>Simplified model for low and moderate frequencies</p>
Opamp 		$V_n(f), I_{n-}(f), I_{n+}(f)$ <p>— Values depend on opamp — Typically, all uncorrelated</p>

Figure 9.11
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Table 2: Device noise models

$$(190 - 55)V_x - 2 * (190 * 0.57 - 55 * 2.59)V_x + 190 * 0.57^2 - 55 * 2.59^2 = 0 \quad (2)$$

$$V_x = (\underline{1.28}, -1.78) \quad V_{effn} = 1.28 - 0.57 = 0.71V \quad V_{effp} = 2.59 - 1.28 = 1.31V \quad (3)$$

$$I_D = 0.5 * 190 * 0.71^2 \mu A = 48 \mu A \quad (4)$$

$$I_D = 0.5 * 55 * 1.31^2 \mu A = 47 \mu A \quad (5)$$

$$r_{dsn} = r_{dsp} = \frac{1}{\lambda I_D} = \frac{L}{L \lambda I_D} = \frac{1 \mu m}{0.16 \mu m/V} * 47 \mu A = 0.133V/\mu A = 133k\Omega \quad (6)$$

$$r_{out} = r_{dsn}/2 = \quad (7)$$

$$g_{mn} = 190 \mu A/V^2 * 0.71 = 135 \mu A/V \quad (8)$$

$$g_{mp} = 55 \mu A/V^2 * 1.31 = 72 \mu A/V \quad (9)$$

$$A = (135 + 72) \mu A/V * (133/2kV/A) = 14 \quad (10)$$

Task 10 (4p): By considering the transistor noise model in table 2 and neglecting the $V_g^2(f)$ noise component only considering the thermal noise component $I_d^2(f)$ at room temperature ($T=300^\circ K$), what is the output noise spectral density (sketch a graph!) and what is the input referred root mean square value considering a noise bandwidth of 1MHz?

$$V_{no}(f) = \sqrt{I_{np}^2 + I_{nn}^2} * r_{out} \quad (11)$$

$$= \sqrt{4kT \frac{2}{3} (g_{mp} + g_{mn})} * r_{out} \quad (12)$$

$$= \sqrt{4kT \frac{2}{3} (135 + 72) \mu A/V * 66k\Omega} \quad (13)$$

$$= 0.3 \mu V / \sqrt{Hz} \quad (14)$$

$$V_{ni(rms)}^2 = (V_{no}(f)/A)^2 * 1MHz = 459 \mu V^2 \quad (15)$$

$$V_{ni(rms)} = 21 \mu V_{rms} \quad (16)$$

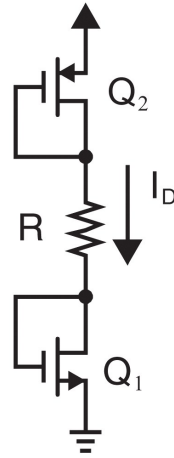


Figure P7.2
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Figure 6: A simple circuit to produce a bias current

5 Chapter 7

Special Master syllabus only!

The circuit in figure 6 is implemented in the $0.35\mu\text{m}$ technology of table 1 with $L_{1,2}=1\mu\text{m}$.

Task 11 (3p): Find W_1 , W_2 and R so that $V_{eff1,2}=300\text{mV}$ and $I_D=25\mu\text{A}$

$$\begin{aligned}
 V_{eff} &= \sqrt{\frac{2I_D L}{\mu C_{ox} W}} \\
 V_{eff}^2 &= \frac{2I_D L}{\mu C_{ox} W} \\
 W &= \frac{2I_D L}{\mu C_{ox} V_{eff}^2} \\
 W_n &= \frac{2 * 25e-6 - 61e-6}{190e-6 * 300e-3^2} = 2.92\mu\text{m} \\
 W_p &= \frac{2 * 25e-6 - 61e-6}{55e-6 * 300e-3^2} = 10.10\mu\text{m}
 \end{aligned}$$

$$V_R = V_{dd} - V_{tn} - V_{tp} - V_{effn} - V_{effp} = 3.3 - 0.71 - 0.57 - 0.3 - 0.3 = 1.42\text{V}$$

$$R = V_R / I = 1.42 / 25e-6 = 56.8\text{k}\Omega$$

Task 12 (3p): How much will I_D change if both V_{tn} and $|V_{tp}|$ increase by 20%?

$$V_{tn} = 1.2 * 0.57 = 0.68$$

$$V_{tp} = 1.2 * 0.71 = 0.85$$

Since $\mu C_{ox} \frac{W}{L} = 5.555e - 4 \text{A/V}^2 := \beta$ is the same for PMOS and NMOS for the same current also:

$$V_{eff} = V_{effn} = V_{effp}$$

The equations needed are:

$$\begin{aligned} I &= \frac{1}{2} \mu C_{ox} \frac{W}{L} V_{eff}^2 := \frac{1}{2} \beta V_{eff}^2 \\ I &= \frac{V_R}{R} \\ 2V_{eff} &= V_{dd} - V_{tn} - V_{tp} - V_R \end{aligned}$$

Solving for V_{eff} :

$$0 = \frac{R\beta}{4} V_{eff}^2 + V_{eff} - \frac{V_{dd} - V_{tn} - V_{tp}}{2}$$

$$V_{eff} = (-0.4037, \underline{0.2769})$$

Control:

$$I = \frac{1}{2} \beta V_{eff}^2 = 21.30 \mu\text{A}$$

$$I = (V_{dd} - V_{tn} - V_{tp} - 2V_{eff})/R = 21.30 \mu\text{A}$$