Oblig 1 - INF3410

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0.1 Task1

In matlab we coded a simple modell and ploted the results. The code:

```
function [ Ids ] = nmosmodel(Vgs)
%nmos-model plotting vds as function of Vgs
%
%%
% $W/L=10m/0.4um$
% $uC_{ox}W/Lm=beta =190*10/0.4$
%   V_{tn}=0.57
%   C_{ox}=4.5

%  $ 0.35 um prosess$
%   V_T=kT/q=26mV at 300 degree Kelvin
%   n=1.5 for weak inversion
%   n=1.7 for strong ionversion
%   no length modulation lambda
W=10;
L=0.4;
vt=1.7;
bolt=1.38e-23;
beta=190*W/L;
Veff=Vgs-vt;
Vds=Veff;

if Vgs<vt
    Ids=0;
%triode region
else if (Vgs>vt && Vds<=Veff);
    vt=vt;
    Ids=beta*(Veff)*Vds-(Vds^2/2);
%active region
else % (Vgs>vt && Vds>=Veff)
    Ids=0.5*beta*Veff^2;
end


end
```

the plotting code:

```
Vgs=linspace(0, 5, 100);
Ids=zeros(length(Vgs),1)';
for n= 1:length(Vgs);
    Ids(n)=nmosmodel(Vgs(n));
end
figure();
title('I_{ds} as funtion of V_{gs}')
xlabel('V_{gs}')
ylabel('V_{ds}')
plot (Vgs,Ids)
figure()
title('logaritmic I_{ds} as funtion of V_{gs}')
```

```
xlabel('V_{gs}')
ylabel('I_{ds}')
plot (Vgs,log(Ids))
```

See fig1 and 2.

0.2 Task2

Comparing cadence plot ofV_{gs} andI_{ds} and adjusting modelparameters so the simple nmosmodel is more accurate.

See fig 3 and 4.

0.3 Task3

Measuring the current through a $47k\Omega$ resistor. Using Matlab and GPIB-interface to the Agilent voltage suply. and agilent multimeter-

see fig 5

0.4 Task4

We soldered on the mc1400qb to a perfboard and measured the current of the drain node. We used both channels on the Agilent Voltagesuply, one chanell for the V_{gs}-sweep and one channel to suply a sufficiently large V_{ds}

```
function [ iout ] = gpib_function( vinmin,vinmax, steps )

HPE3631_Init;
HPE3631_SetILimit(1,0.1);
%HPE3631_SetVolt(1,1);
HPE3631_Operate;


K617_Init;
iout=zeros(1,steps)';
K617_SetRange(0);
K617_SetMode('A');

i=linspace(vinmin,vinmax,steps);
for k=1:length(i)
   HPE3631_SetVolt(1,i(k));

   pause(0.5);
   iout(k) = K617_ReadQuick();
end
plot(i,iout)
return

end
```

0.5 Task5

See Figure 10

0.6 Task6

We didn't take the gnd-connection of V_{gs} into account when we ran the script. Therefor the we plot from zero. We have also connected the Keithley reversed so the values are negative.

0.7 Task7

The difference between nMOS and pMOS is that the nMOS when the V_{gsn} is high the I_{dsn} is high. The pMOS is inverted: When the V_{gsp} is high the I_{dsp} is low.

0.8 Task8

See fig 13

0.9 Task9

```
0.0000
0.0000
0.0000
0.0000
0.0000
0.0000
0.0000
0.0000
0.0000
0.0000
0.0000
0.0000
0.0000
0.0000
0.0000
0.0000
0.0000
0.0001
0.0005
0.0008
0.0007
0.0006
0.0006
0.0010
0.0017
0.0031
0.0045
0.0060
0.0077
0.0096
0.0118
0.0140
0.0163
0.0188
0.0211
0.0233
0.0257
0.0277
```

```
0.0294
0.0310
0.0326
0.0337
0.0344
0.0350
0.0348
0.0341
0.0334
0.0315
0.0289
0.0257
0.0219
0.0165
```

Dette er relativ error mellom nmosmodel.m og mc14007ub.

0.10 Task10

```
close all
figure
hold on

plot(Vgs,cadence)
legend('Cadence');
plot(Vgs,ans)
```

Data fra cadence:

```
0.0000
0.0000
0.0000
0.0000
0.0000
0.0002
0.0016
0.0056
0.0123
0.0211
0.0319
0.0443
0.0581
0.0733
0.0896
0.1069
0.1250
0.1435
0.1620
0.1796
0.1960
0.2109
0.2240
0.2356
0.2448
```

```
0.2527
0.2590
0.2635
0.2664
0.2674
0.2670
0.2650
0.2612
0.2561
0.2497
0.2415
0.2323
0.2219
0.2101
0.1967
0.1824
0.1670
0.1500
0.1323
0.1137
0.0934
0.0727
0.0510
0.0284
0.0046
0.0193
```

see fig 14 - viser cadence og transistoren i samme plot.

0.11 Task11

her skal vi trekke ut $/Beta$ fra nMOS-transistoren.

```
function [ betas ] = calcBeta( )
%calcBeta finds beta for a cmos transistor.
iout=zeros(1,1,100)';
iout=gpib_function(0,5,100)
vgs=linspace(0,5,100);
betas=zeros(1,1,100)';
for K= i:length(iout)
    betas(K)=sqrt(iout(K)-sqrt(K+1))/(vgs(K)-vgs(K+1))
end
return

end
```

0.12 Task12

0.13 Pictures

And nnow the logaritmic I_{ds} Logaritmic scaling of I_{ds}

Figure 1: Task 1

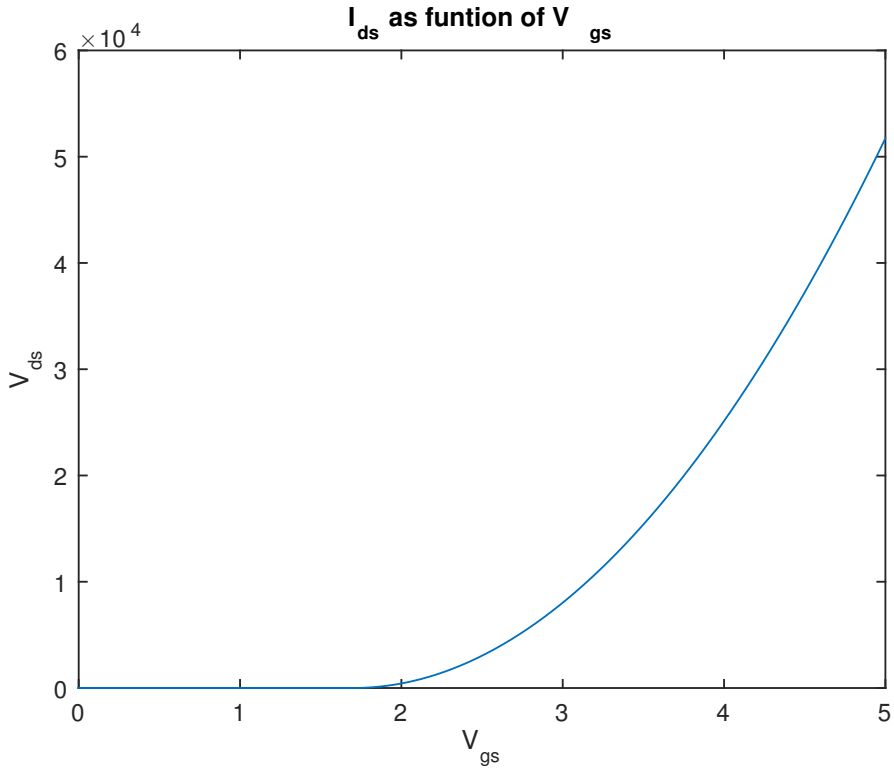

Figure 2: Task 1 log

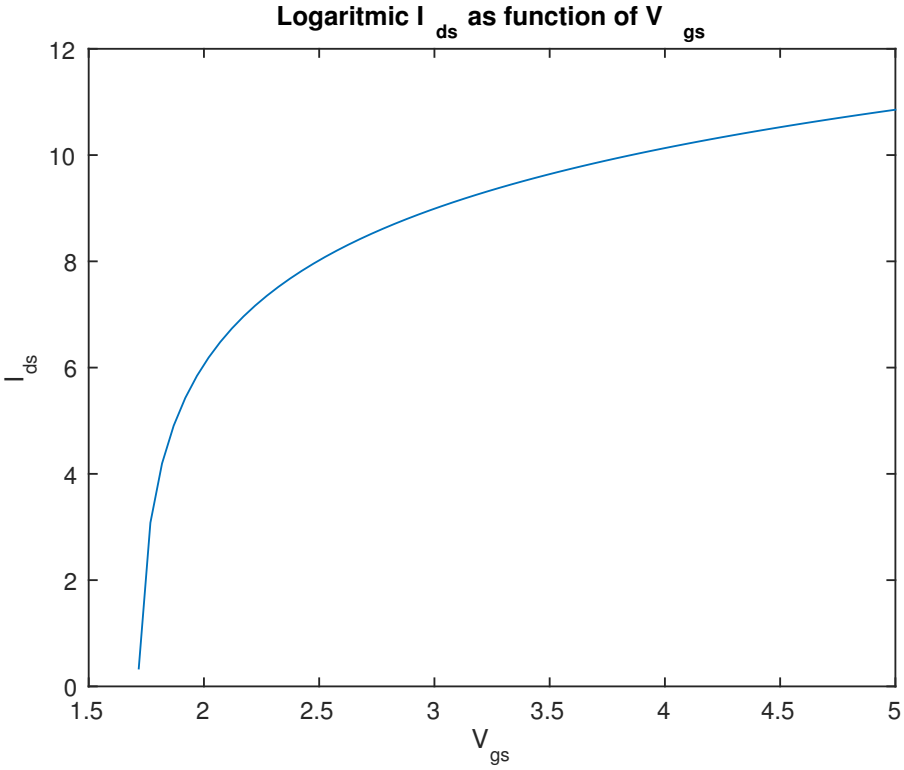

Figure 3: Task 2 not Matched parameters

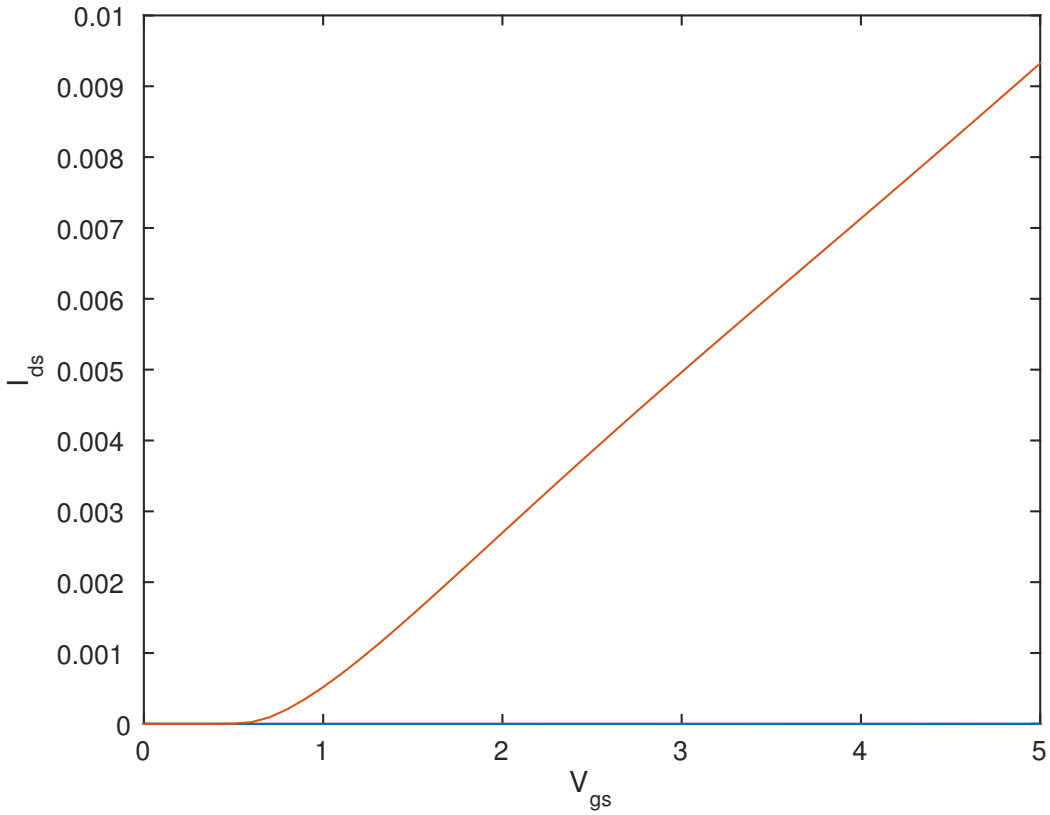

Figure 4: task 2 Matched parameters

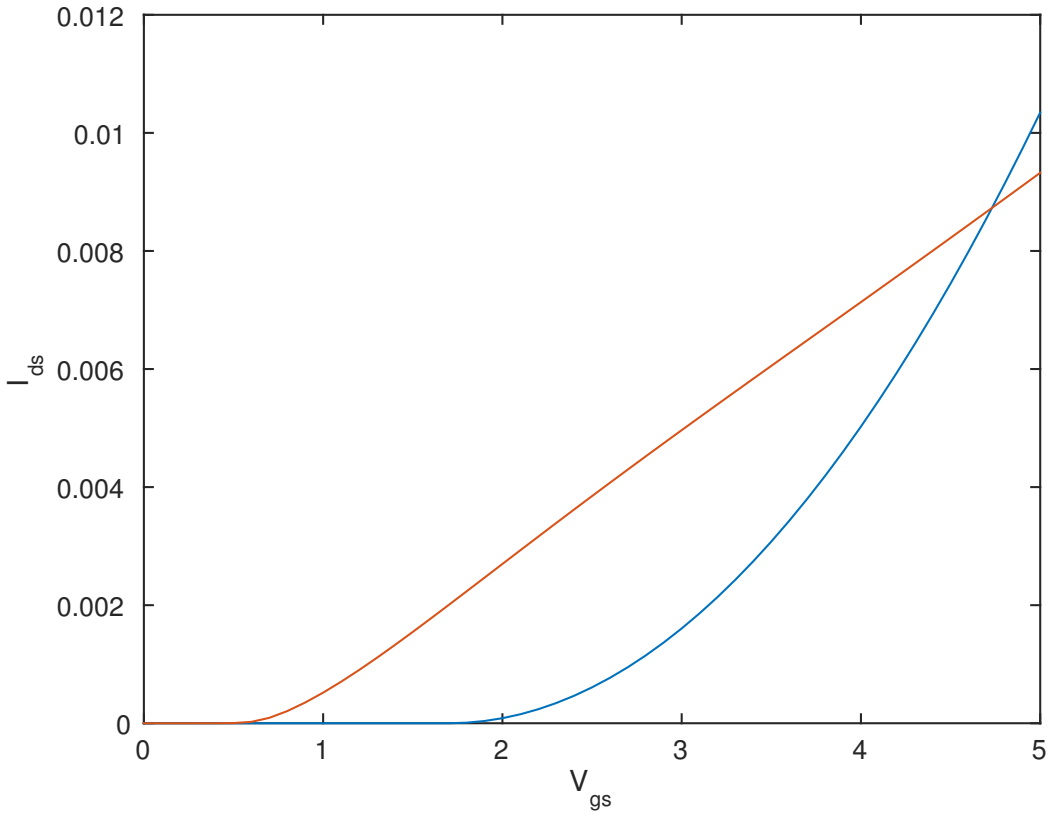

Figure 5: Task2 nMOS Not matched parameters

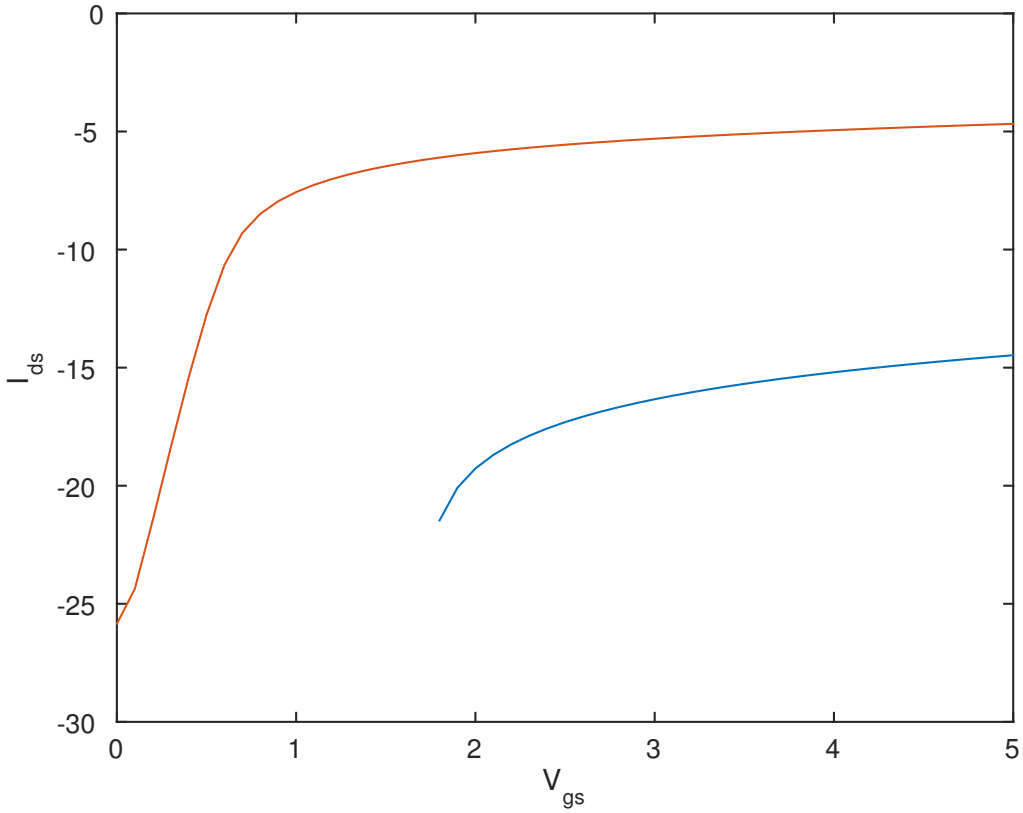

Figure 6: Task 2 nMOSMatched parameters

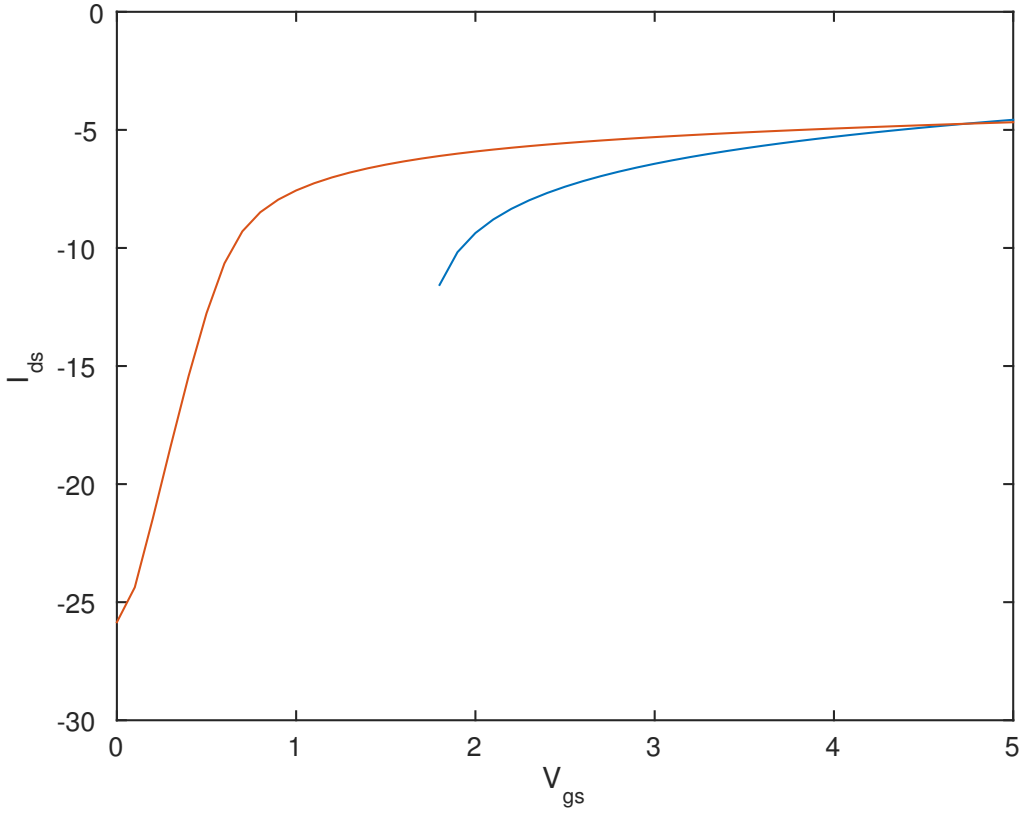

Figure 7: Task 3 Resistor I_{out}

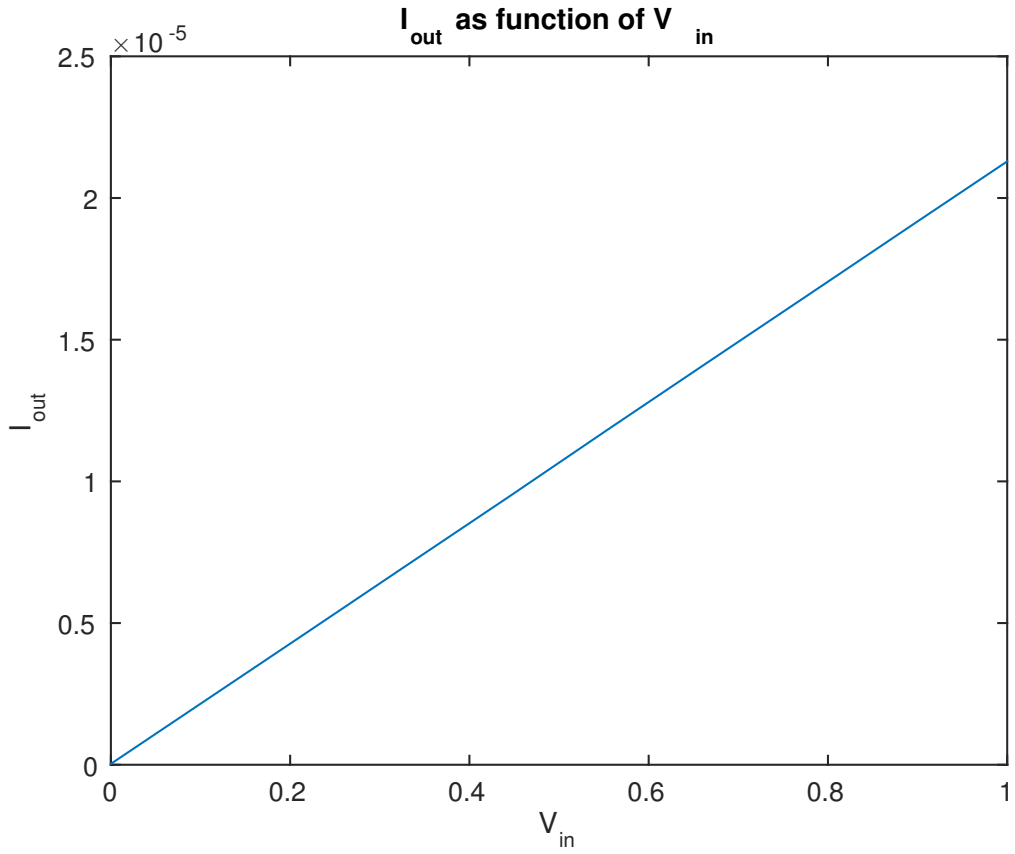

Figure 8: Task 4

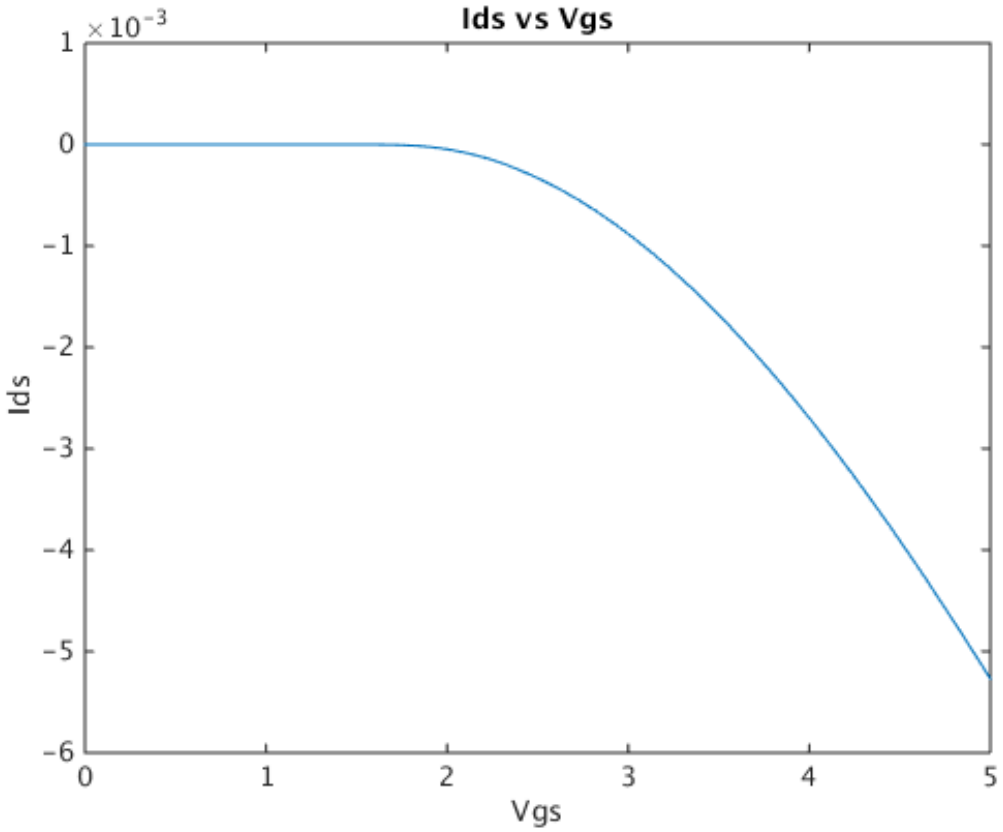

Figure 9: task 4 log

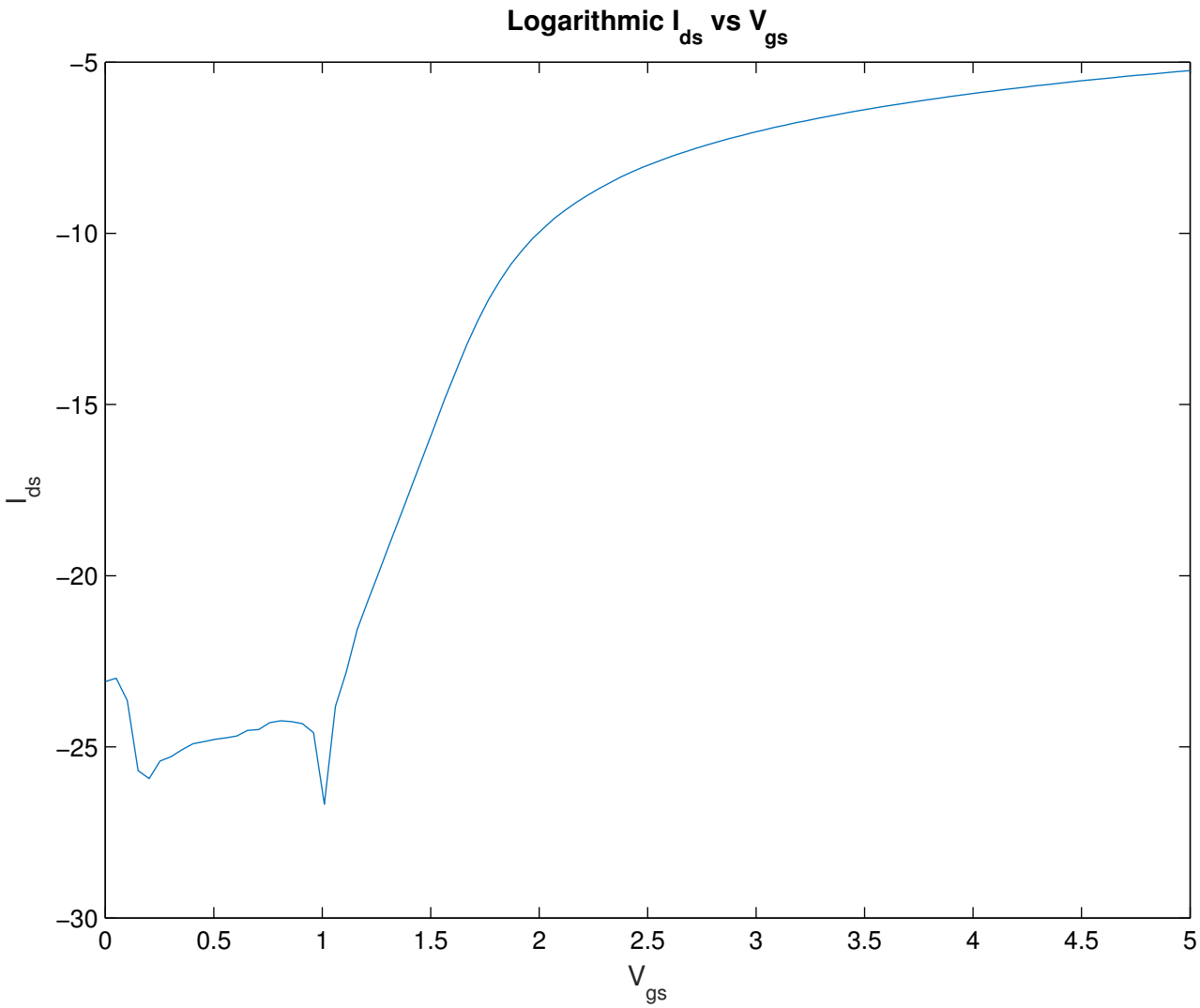

Figure 10: Task 5: Circuit for measuring the cmos's

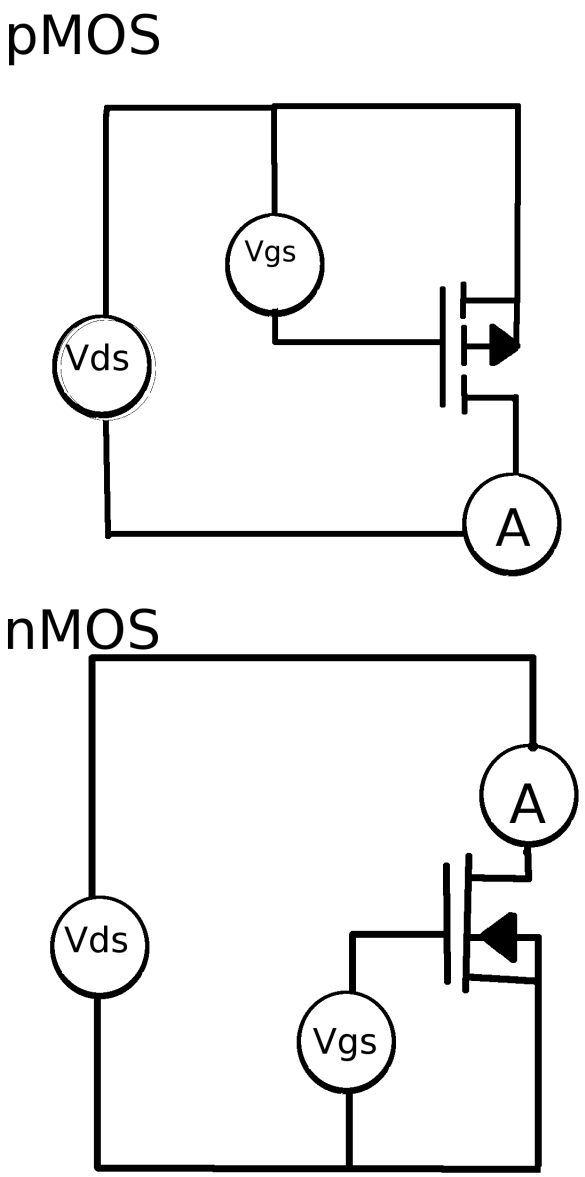

Figure 11: task6: pMOS

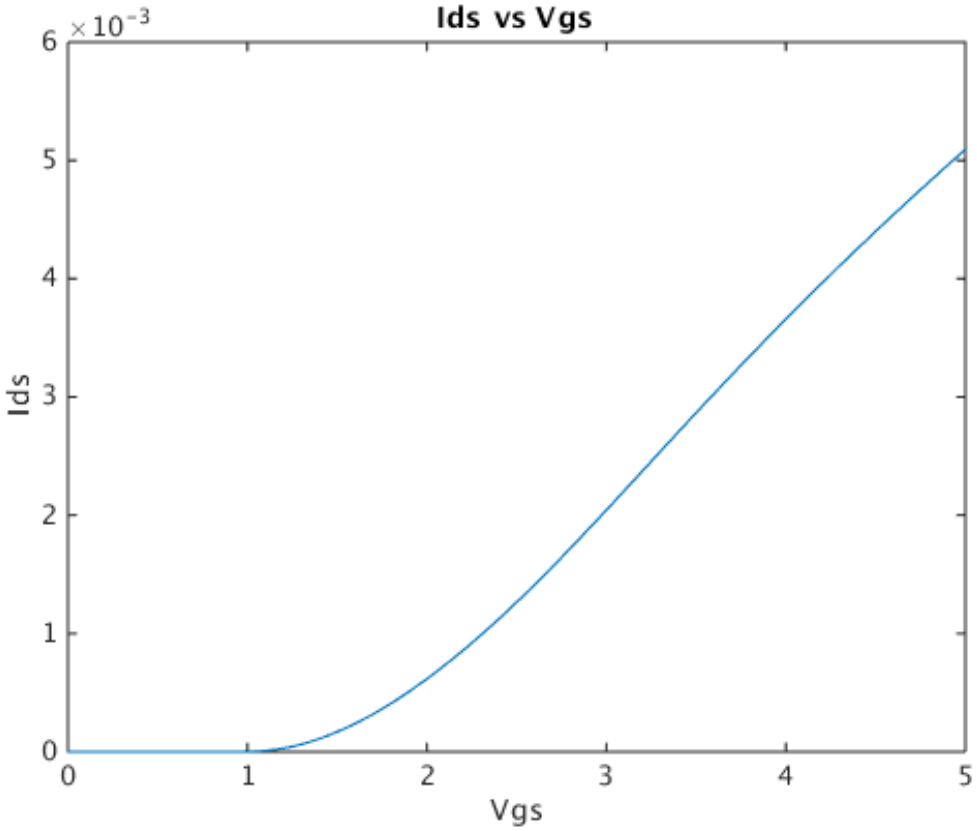

Figure 12: Task6: pMOS logaritmic

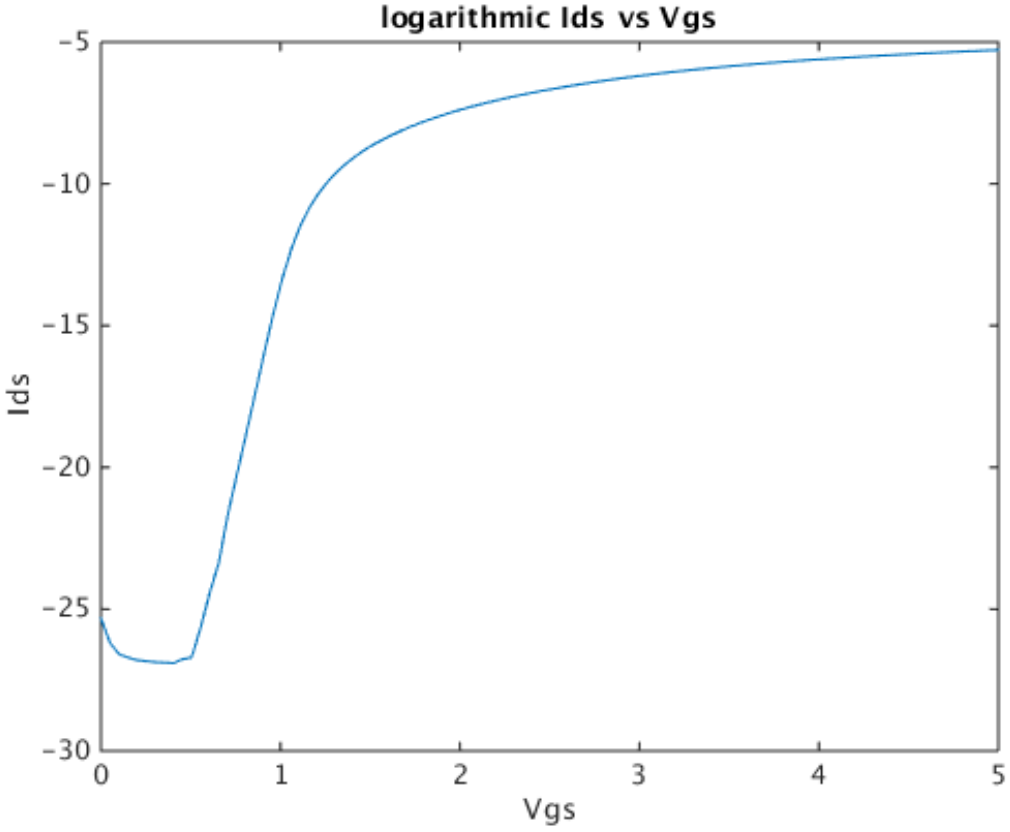

Figure 13: Task8:

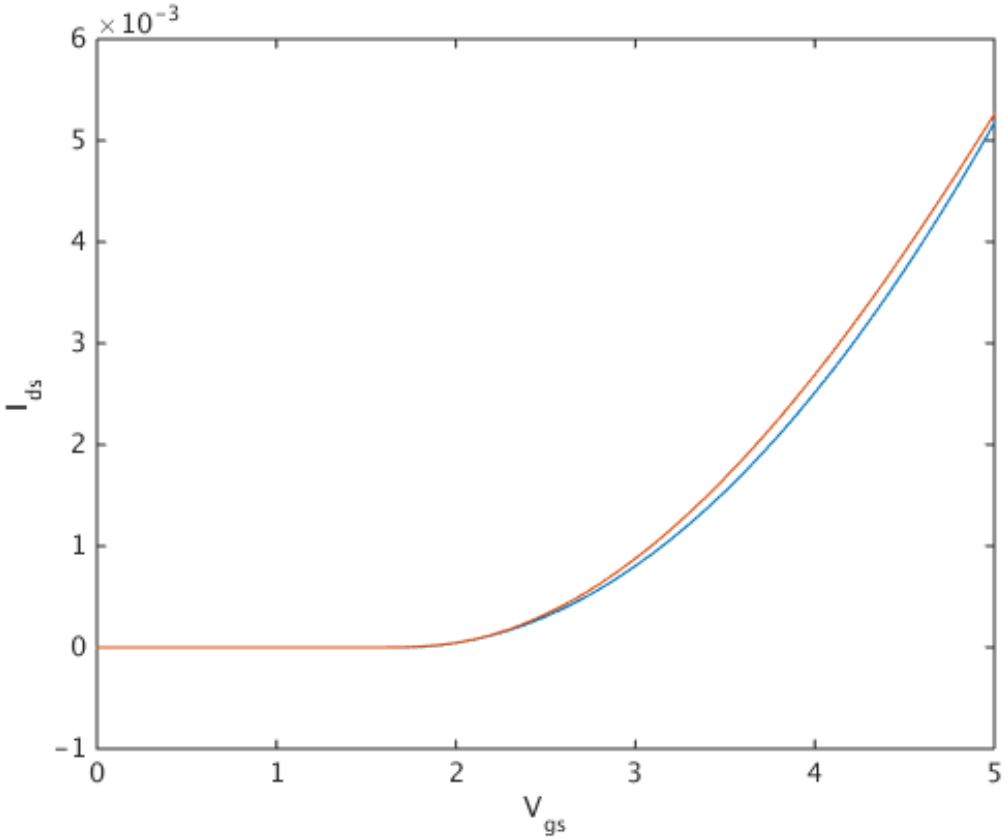

Figure 14: Task10: