University of Oslo
Faculty of Mathematics and Natural Sciences

Final Exam in: INF3410, fall 2013 Date of exam: 18-Dec-2013
Time: 9:00-13:00
This examination paper consists of 6 page(s)
Permitted materials: All printed and written including approved (!) calculator

Make sure that your copy of this examination paper is complete before answering.

Read Carefully:

This is the final exam of INF3410, fall 2013. It will contribute 60% towards the final grade, while the other 40% are contributed by the mandatory labs 2 and 3 of the course.

It is recommended that you read all the tasks before starting with the exam. A good strategy thereafter is to start with the tasks you feel most comfortable with and leave the most difficult ones for last.

It is also recommended to read through all the tasks once more once you have finished, to make sure you have not overlooked anything.

Start a new page for every task you are answering and write your name and task number on the top of all pages you submit. If you use several pages per task also mark the page number next to the task number. Make sure to answer all questions and follow all instructions. Clearly mark your final answers and results (all that are explicitly asked for or instructed to find in a task) with a double underline. Document your deduction of those results and any assumptions you may have had to make.

Note that you may not hand in the original task papers that you are holding now, i.e. do not write any results here but use exclusively the separate sheets of paper that you are going to hand in.

Each question is graded indicating the weight when grading.

Chapter 1

Task 1 (4p): Compute the intrinsic gain and intrinsic speed of an NMOS and PMOS transistor with W/L=1 and L equal to three times the minimum length for the 0.35μm processes in table 1 for a drain current of 20μA.

Chapter 3

Task 2 (2p): Figure 1 shows common source gain stages with different loads. Assume that all transistors are in saturation/in the active region and in strong

Table 1.5 MOSFET parameters representative of various CMOS technologies and used for rough hand calculations in this text.

	0.8 μm		0.35 μm		0.18 μm		45 nm	
Technology	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
μC_{ox} ($\mu A/V^2$)	92	30	190	55	270	70	280	70
V_{t0} (V)	0.80	–0.90	0.57	–0.71	0.45	–0.45	0.45	–0.45
$\lambda \cdot L$ (μm/V)	0.12	0.08	0.16	0.16	0.08	0.08	0.10	0.15
C_{ox} ($fF/\mu m^2$)	1.8	1.8	4.5	4.5	8.5	8.5	25	25
t_{ox} (nm)	18	18	8	8	5	5	1.2	1.2
n	1.5	1.5	1.8	1.7	1.6	1.7	1.85	1.85
θ (1/V)	0.06	0.135	1.5	1.0	1.7	1.0	2.3	2.0
m	1.0	1.0	1.8	1.8	1.6	2.4	3.0	3.0
$C_{ov}/W = L_{ov}C_{ox}$ (fF/μm)	0.20	0.20	0.20	0.20	0.35	0.35	0.50	0.50
$C_{db}/W \approx C_{sb}/W$ (fF/μm)	0.50	0.80	0.75	1.10	0.50	0.55	0.45	0.50

Table 1.5

Table 1: Typical process parameters

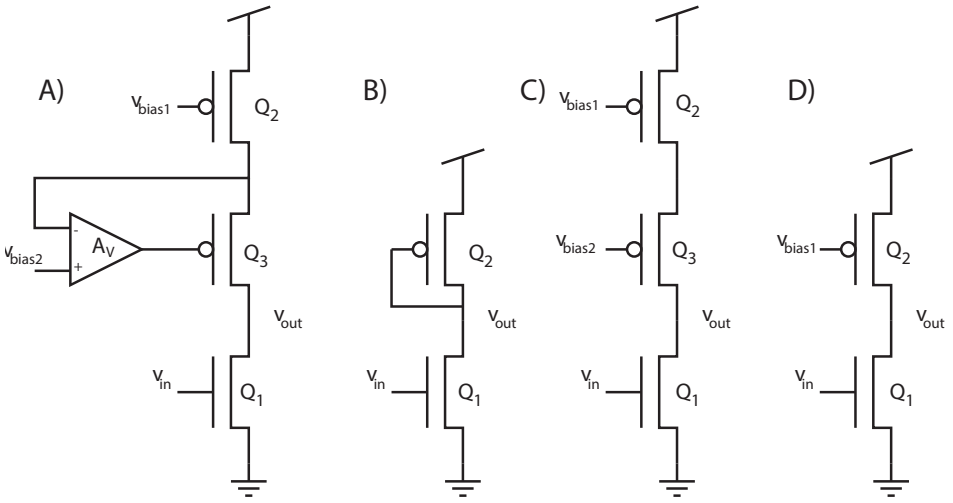

Figure 1: Common source gain stages with different loads

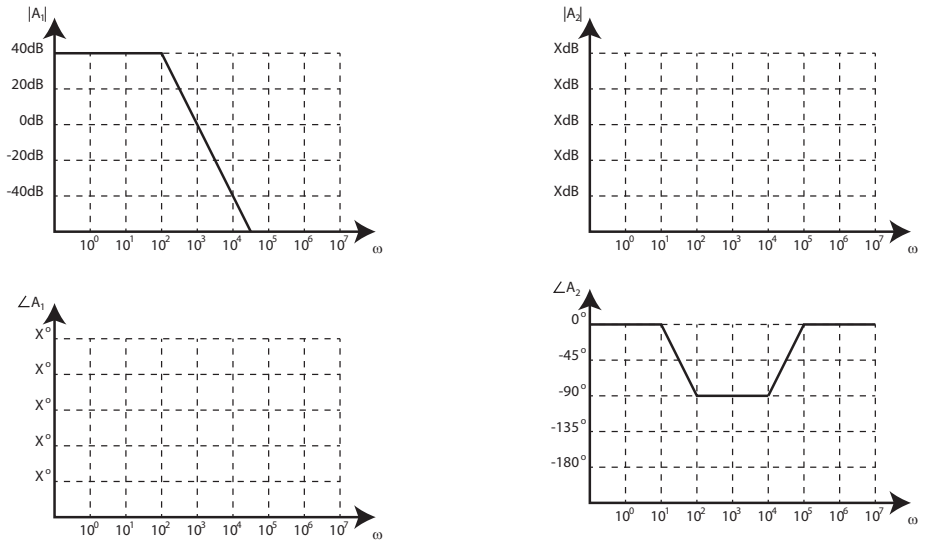

Figure 2: Incomplete Bode plots

inversion and biased at the same DC current. Please order them according to how much small signal low frequency voltage gain you assume they will have, i.e. make a list beginning with the circuit with the highest gain and ending with the lowest.

Task 3 (4p): Find small signal low frequency expressions for output resistance and voltage gain for all the circuits in fig. 1. Ignore the body effect.

Chapter 4

Task 4 (4p): Complete the Bode plots in figure 2. Copy them to the sheets of paper that you will hand in (!!!) as you may not hand in the exam task papers! Sketch the expected corresponding magnitude/phase plot. Indicate all important points and explicitly give their phase, dB and rad/s values! Assume all filters involved have a DC gain of 100. If there are several solutions, sketch all of them! (Note that the plots are piece-wise linear approximations. In the phase plots 90^o phase transitions are assumed to be completed during one decade. Please use the same convention for your sketches!)

Task 5 (4p): Write down the corresponding transfer functions for the Bode plots. If there are several solutions, write all of them!

Chapter 5

Task 6 (4p): Figure 3 shows the small signal model of a two stage amplifier with negative feedback. The given parameters are $g_{m1} = g_{m2} = 3\text{mA/V}$, $r_{out1} = r_{out2} = 10\text{k}\Omega$, $C_{L1} = 100\text{pF}$, $C_{L2} = 1\text{pF}$. What is the open loop transfer function (i.e. ignoring the feedback $-\beta$)?

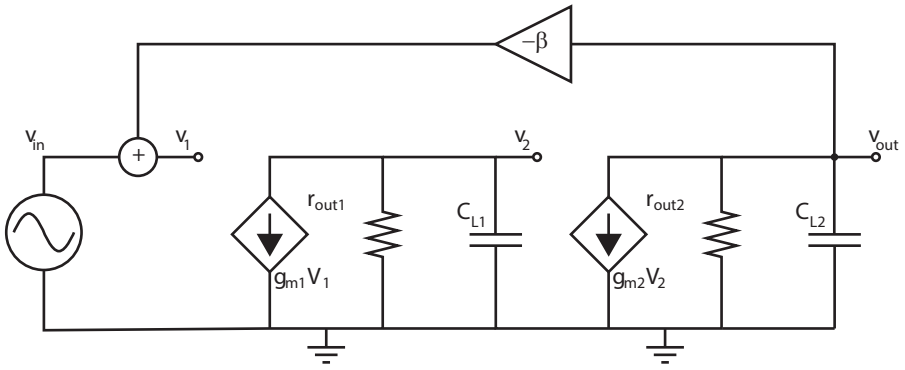

Figure 3: Small signal model of a two stage amplifier with negative feedback

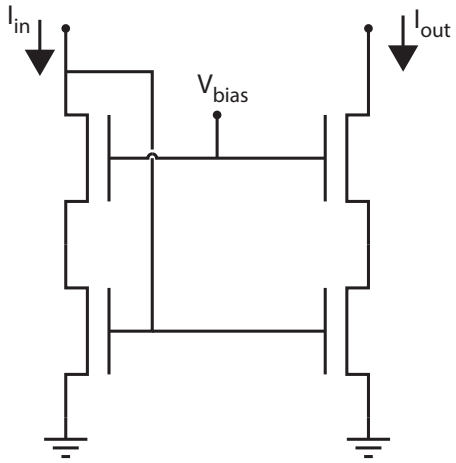

Figure 4: Current mirror variant

Task 7 (4p): Find the value for β that will make the second pole frequency the exact same as the unity loop gain frequency ω_t. What will be the phase margin of this circuit?

Chapter 6

Task 8 (4p): Figure 4 depicts a variant of a current mirror implemented with the 0.35μm process parameters from table 1. All transistors are 2μm wide 1μ long. Assume an input current of 20μA. Compute the optimal V_{bias} for that particular input current that allows for maximal output swing while still keeping all transistors in saturation/in the active region!

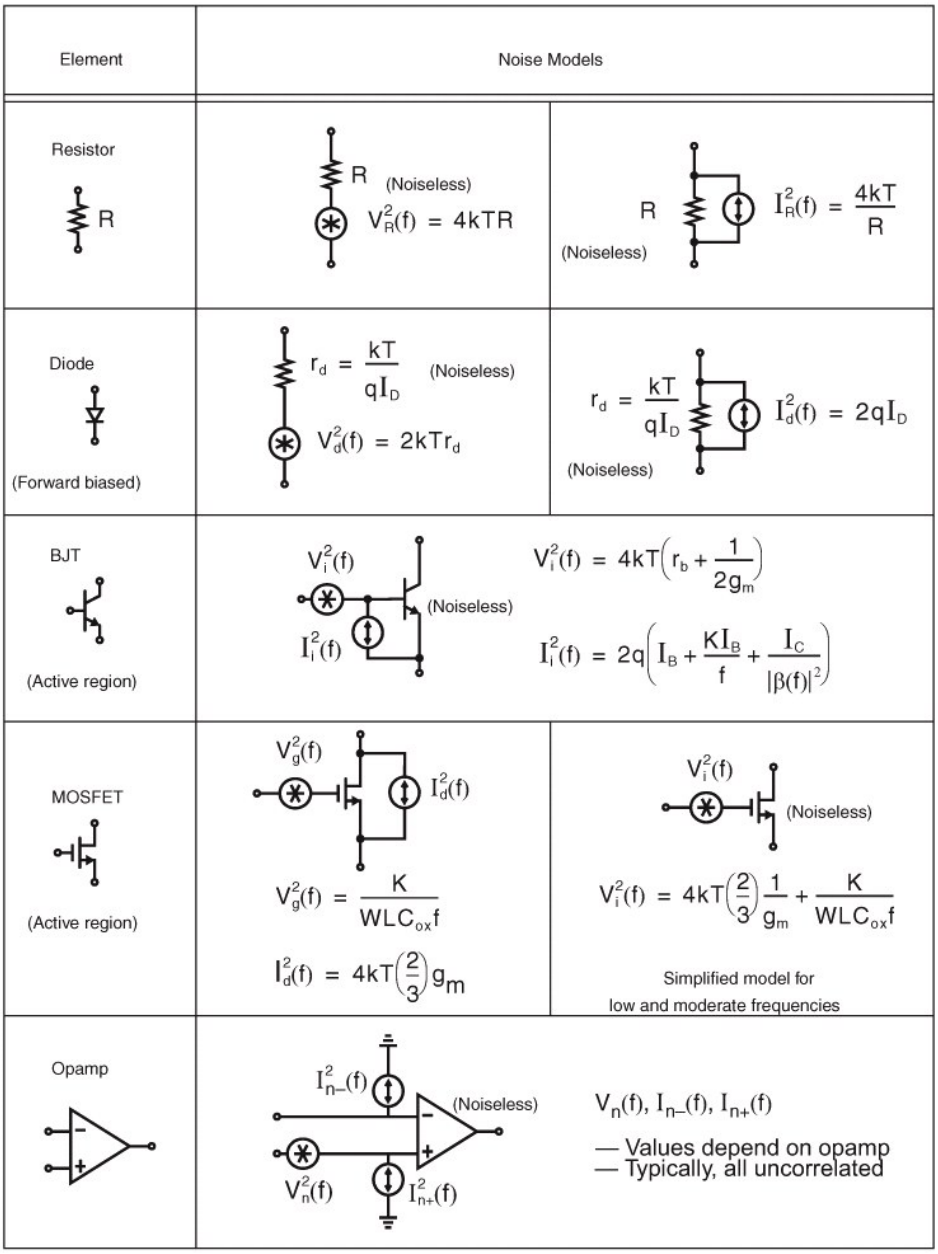

Figure 9.11

Table 2: Device noise models

Chapter 9

Task 9 (4p): An inverter is implemented with MOS FETs of the 0.35μm process described in table 1, where both the pMOS and nMOS transistors have W=L=1μm and where the supply voltage Vdd is 3.3V. Find the operation point where the inverter acts as an amplifier, i.e. an input voltage where the drain currents of both transistors are the same. Compute the drain current, individual transconductances g_{mn} (nMOS) and g_{mp} (pMOS) for the transistors and the inverter's voltage gain A.

Task 10 (4p): By considering the transistor noise model in table 2 and neglecting the $V_g^2(f)$ noise component, i.e. only considering the thermal noise component $I_d^2(f)$ at room temperature (T=300^{o}K), what is the output noise spectral density (sketch a graph!) and what is the input referred root mean square value considering a noise bandwidth of 1MHz?