INF3410 — Fall 2015

Book Chapter 1: Devices and Modelling

UNIVERSITETET I OSLO

Content

PN Junction Properties

Field Effect Transistor Large Signal Models

Field Effect Transistor Small Signal Models

Field Effect Transistor ‘Second Order’ Properties

Short Remark on Passive Devices

Summary

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Built in Potential/Junction Capacitance

$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{\Phi_0}}} \quad (1.17)$$

$$C_{j0} = \sqrt{\frac{qK_S\varepsilon_0}{2\Phi_0}\frac{N_A N_D}{N_A + N_D}} \quad (1.18)$$

$$\Phi_0 = U_T \ln\left(\frac{N_A N_D}{n_i^2}\right) \quad (1.6)$$

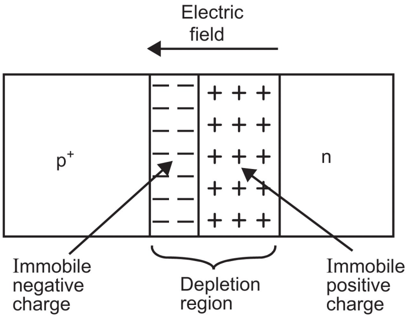

Figure 1.2

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nFET cross section and symbols

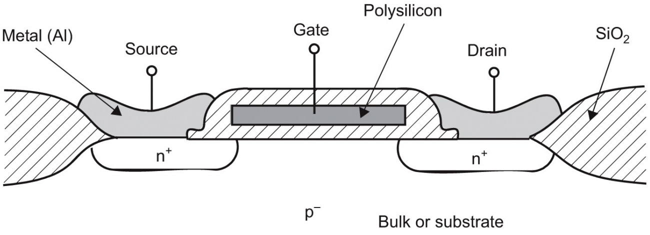


Figure 1.6

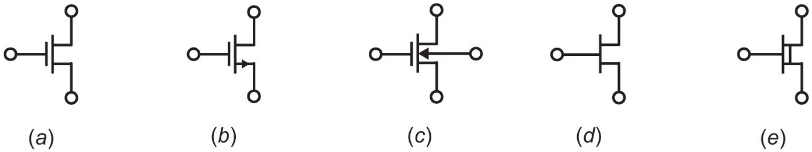


Figure 1.7

EKV Model

$$I_{DS} = I_F - I_R$$

for an NFET:

$$I_{F(R)} = I_S \ln^2\left[1 + e^{\frac{V_G - V_{T0} - nV_{S(D)}}{2nU_T}}\right]$$

where $I_S = 2n\beta U_T^2 \;\; \beta = \mu C_{OX}\frac{W}{L}$

Active region/in saturation: $I_F >> I_R$
Triode region/linear region: $I_F \approx I_R$

EKV Simplified in Weak Inversion

Weak inversion/subthreshold:

$$(I_F << I_S) = (V_G - nV_S < V_{T0})$$

$$\Rightarrow$$

$$I_F = 2n\beta U_T^2 e^{\frac{V_G - V_{T0} - nV_S}{nU_T}}$$

Book model (in saturation):

$$I_D = (n-1)\beta U_T^2 e^{\left(\frac{(V_G - V_{tn})}{nU_T}\right)} \quad (1.121)$$

EKV Simplified in Strong Inversion

Strong inversion/above threshold:

$$(I_F >> I_S) = (V_G - nV_S > V_{T0})$$

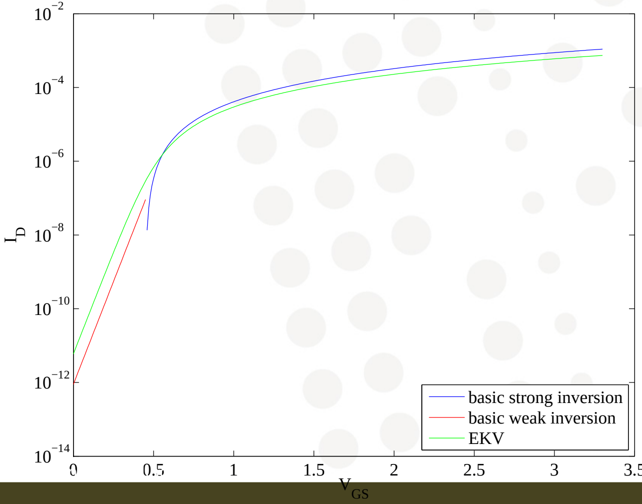
$$\Rightarrow$$

$$I_{F(R)} = \frac{\beta}{2n}\left(V_G - V_{T0} - nV_{S(D)}\right)^2$$

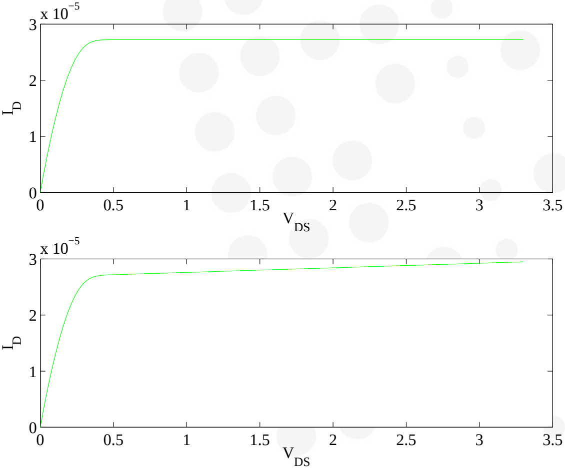
Book model (in saturation/active region):

$$I_D = \frac{\beta}{2}(V_G - V_S - V_{tn})^2 \quad (1.63)$$

Basic Equation vs. EKV



Channel Modulation/Early Effect Illustration



Channel Modulation/Early Effect Formula

Strong Inversion

$$I_D = \frac{\beta}{2}(V_{eff})^2\left[1+\lambda(V_D - V_S - V_{eff})\right] \quad (1.67)$$

$$\lambda = \frac{k_{ds}}{2L\sqrt{V_{DS} - V_{eff} + \Phi_0}}$$

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Small Signal Models

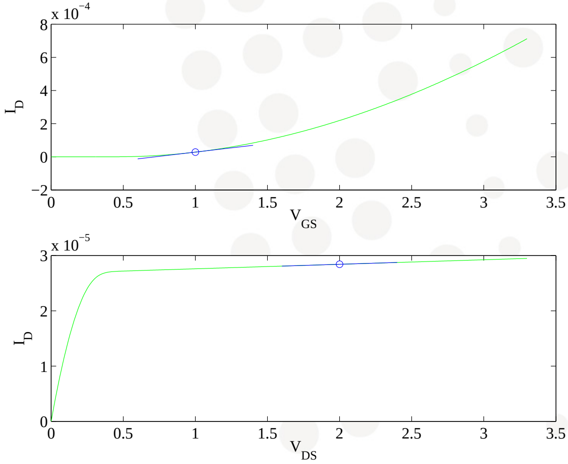
A linearized model that applies to a certain point of operation. All small signal variables (e.g. $\mathrm{i_d}$) are thus only the offset to the variables at this point of operation (e.g. $\mathrm{I_D}$). Sometimes the total of the two is refered to as $\mathrm{i_D}$ (though not in the Carusone book!).

$$\mathrm{i_D} = \mathrm{I_D} + \mathrm{i_d}$$

Those so inclined may think of it as a first order Taylor expansion:

$$i_D(\vec{X} + \vec{x}) \approx I_D(\vec{X}) + \nabla I_D(\vec{X})\vec{x}^T = I_D(\vec{X}) + i_d(\vec{x})$$

Linear Approximation/Small Signal Model



Low Frequency Small Signal Model nFET

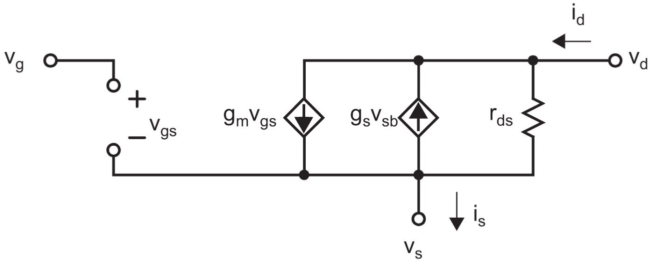


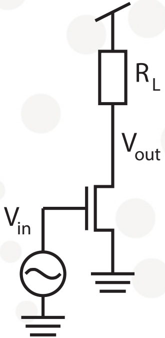
Figure 1.17

Small Signal Model Parameters

$$
\begin{aligned}
g_m &= \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} \text{ (1.77)(strong inversion)} \\
r_{ds} &\approx \frac{1}{\lambda I_D} \text{ (1.86)}
\end{aligned}
$$

Example

In a simple common source amplifier with resistive load and a sine wave input with DC value 1.0V and an amplitude of 50mV, how does the output voltage look like? Use the parameters from the book in table 1.5 for a 0.35μm process and a W=L=1μm. R_L=100kΩ.

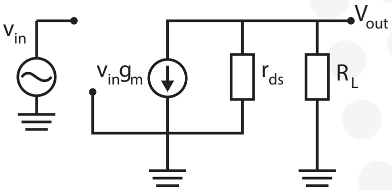


Large Signal Model for Point of Operation

$$\begin{aligned} I_D &= \frac{1}{2}190\frac{\mu\mathrm{A}}{\mathrm{V}^2}\frac{1\mu m}{1\mu m}0.2^2\mathrm{V}^2 \\ &= 3.8\mu A \end{aligned}$$

$$\begin{aligned} V_{out} &= Vdd - R_L I_D = 3.3V - 7.6 * 10^{-6}\mathrm{A} * 100 * 10^3\Omega \\ &= 3.3 - \mathrm{V}0.38\mathrm{V} = 2.92\mathrm{V} \end{aligned}$$

Small Signal Model (1/2)

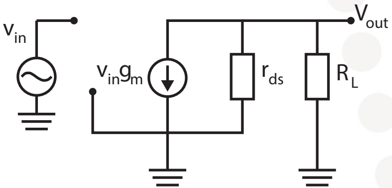


For a summary of the MOS FET equations see section 1.3.3, p42

$$
\begin{aligned}
g_m &= 190\frac{\mu\mathrm{A}}{\mathrm{V}^2}\frac{1\mu m}{1\mu m}0.2\mathrm{V} \\
&= 38\frac{\mu\mathrm{A}}{\mathrm{V}}
\end{aligned}
$$

$$
\begin{aligned}
r_{ds} &= \frac{1}{\lambda I_D} \\
&= \frac{1}{\lambda\frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{eff}^2} \\
&= \frac{1}{\frac{0.16\frac{\mu\mathrm{m}}{\mathrm{V}}}{1\mu m}190\frac{\mu\mathrm{A}}{\mathrm{V}^2}\frac{1\mu m}{1\mu m}0.2^2\mathrm{V}^2} \\
&= 0.82\frac{\mathrm{V}}{\mu\mathrm{A}} = 820k\Omega
\end{aligned}
$$

Small Signal Model (2/2)



$$
\begin{aligned}
v_{out} &= -v_{in} g_m (R_L \parallel r_{ds}) \\
&= -v_{in} 38 * 10^{-6} \left(\frac{820 * 100 * 10^6}{820 * 10^3 + 100 * 10^3} \right) \\
&= -v_{in} * 38 * 10^{-6} * 89 * 10^3 \\
&= -v_{in} * 3.38\text{V}
\end{aligned}
$$

$$A = \frac{v_{out}}{v_{in}} = 3.38$$

Check Error: Large Signal Model for Max and Min

Large signal model:

$$V_{out}^{min,max} = (2.71\text{V}, 3.09\text{V})$$

Small Signal Model:

$$V_{out}^{min,max} = 2.92 \pm 3.38 * 0.05 = (2.75\text{V}, 3.09\text{V})$$

Why the discrepancy?

High Frequency Small Signal Model nFET

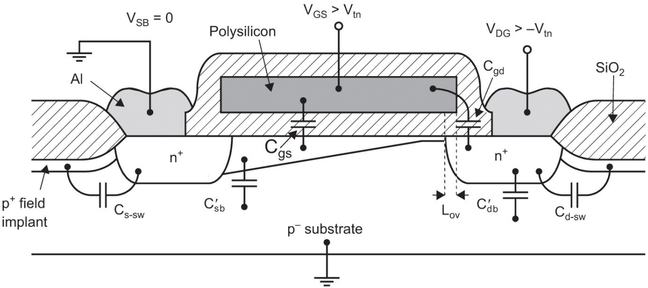


Figure 1.22

High Frequency Small Signal Model nFET

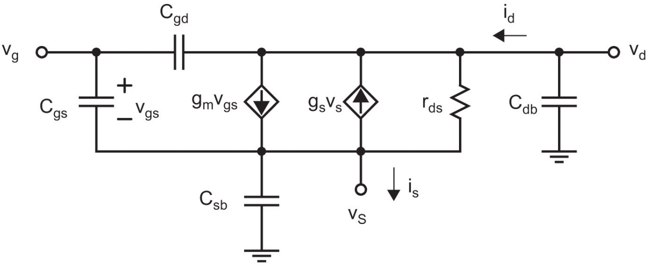


Figure 1.21

High Frequency Small Signal Model nFET

$$\begin{aligned} C_{gs} &\approx \frac{2}{3} W L C_{ox} \quad (1.89) \\ C_{sb} &\approx (A_S + A_{CH}) C_{js} \quad (1.92) \\ C_{gd} &\approx C_{ox} W L_{ov} \quad (1.96) \end{aligned}$$

Intrinsic (Voltage) Gain

Maximal voltage gain, no external load, common source amplifier with ideal current source as 'load'

$$A_i = \left| \frac{\partial V_{out}}{\partial V_{in}} \right| = g_m r_{ds} \approx \frac{2}{\lambda V_{eff}} \quad (1.114/115)$$

$\Rightarrow$ Higher for long transistors (large L) and small V_{eff}

Unity-Gain Frequency (Intrinsic Speed)

Unity current gain ($\frac{\partial I_{out}}{\partial I_{in}} = 1$), no external load, common source amplifier with ideal voltage source as 'load'

$$f_t \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} \approx \frac{3\mu_n V_{eff}}{4\pi L^2} \quad (1.116/117)$$

$\Rightarrow$ Higher speed for shorter transistors (small L) and large V_{eff}

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Field Effect Transistor ‘Second Order’ Properties
- Mobility-Degradation
- Short-Channel Effects
- Leakage Currents

Short Remark on Passive Devices

Summary

Mobility-Degradation/Velocity Saturation

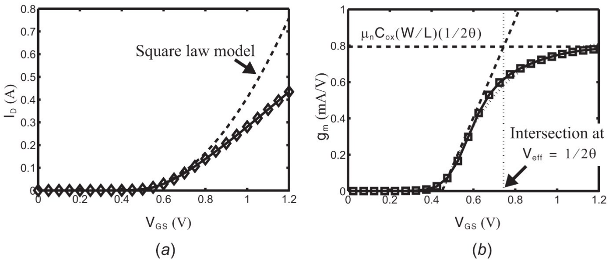

Figure 1.30

$$I_D = \frac{1}{2}\beta V_{eff}^2 \frac{1}{[1+(\theta V_{eff})^m]^{\frac{1}{m}}}, \quad g_m = \frac{1}{2}\beta\frac{1}{\theta} \text{ for } V_{eff} > \frac{1}{2\theta}$$

Short-Channel Effects

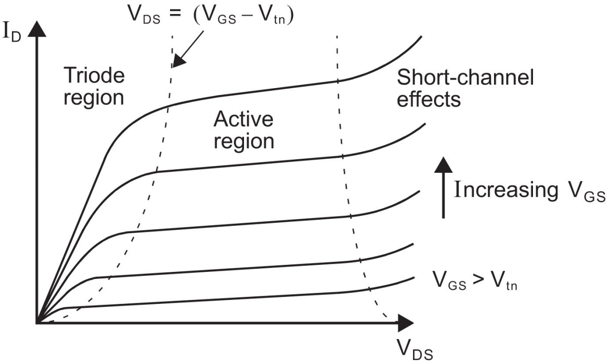

Figure 1.16

Leakage Currents

- subthreshold leakage
- junction leakage (strongly temperature dependent)
- gate leakage (depends on t_{ox} < 2nm: new technologies!)

Leakage Currents

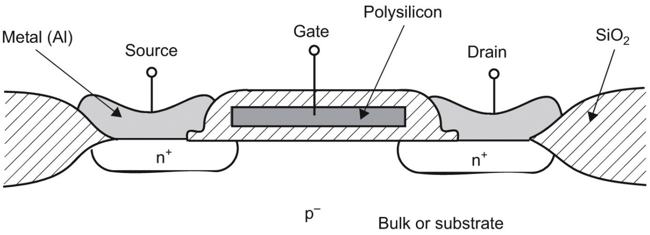

Figure 1.6

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MOS capacitors, a word of caution

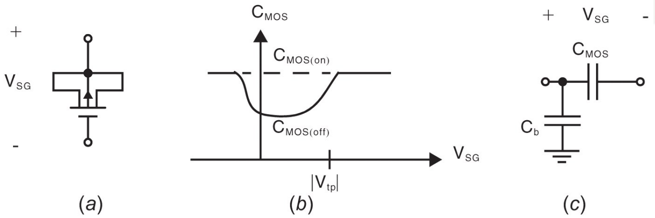

Figure 1.36

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Summary

All equations are summarized in the book section 1.3, starting from page 39.
Realistic parameters for a few technology nodes can be found on in table 1.5 on page 54.