University of Oslo
Faculty of Mathematics and Natural Sciences

Final Exam in: INF4411, fall 2014
Date of exam: 17-Dec-2014
Time: 14:30-18:30
This examination paper consists of 6 page(s)
Permitted materials: All printed and written including approved (!) calculator

Make sure that your copy of this examination paper is complete before answering.

Read Carefully:

This is the final exam of INF3410, fall 2014. It will contribute 60% towards the final grade, while the other 40% are contributed by the mandatory labs 2 and 3 of the course.

It is recommended that you read all the tasks before starting with the exam. A good strategy thereafter is to start with the tasks you feel most comfortable with and leave the most difficult ones for last.

It is also recommended to read through all the tasks once more once you have finished, to make sure you have not overlooked anything.

Start a new page for every task you are answering and write your ID-number and task number on the top of all pages you submit. If you use several pages per task also mark the page number next to the task number. Make sure to answer all questions and follow all instructions. Clearly mark your final answers and results (all that are explicitly asked for or instructed to find in a task) with a double underline. Document your deduction of those results and any assumptions you may have had to make.

Note that you may not hand in the original task papers that you are holding now, i.e. do not write any results here but use exclusively the separate sheets of paper that you are going to hand in.

Each question is graded indicating the weight when grading.

Chapter 1

Task 1 (3p): Compute the small signal transconductance g_m and drain to source resistance r_{ds} for a minimum length nFET of the 0.18μm processes in table 1 for a drain current of 100μA and a width to length ratio (W/L) of 10. What is the transistor's large signal gate to source voltage V_{GS}?

Chapter 3

Task 2 (3p): Figure 1 shows common gate gain stages with different loads and different serial resistances at the input. Derive small signal low frequency

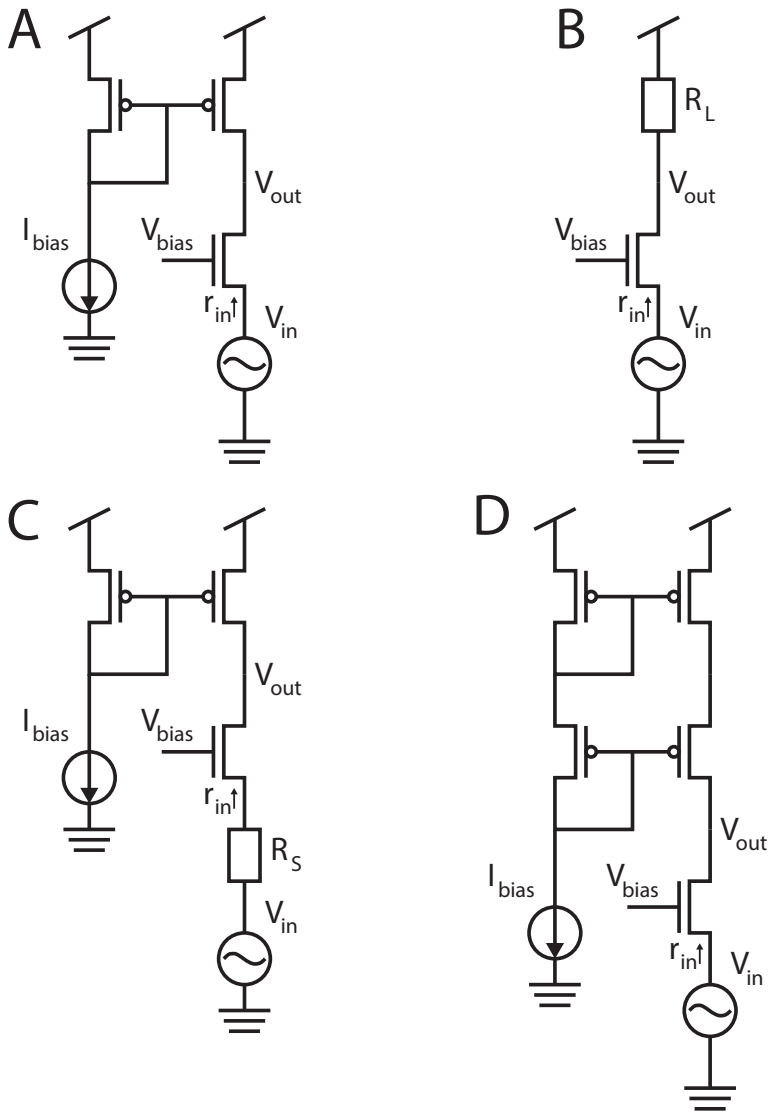

Figure 1: Common gate gain stages with different loads, and with input sources with different serial/output resistances

Table 1.5 MOSFET parameters representative of various CMOS technologies and used for rough hand calculations in this text.

	0.8 μm		0.35 μm		0.18 μm		45 nm	
Technology	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
μC_{ox} ($\mu A/V^2$)	92	30	190	55	270	70	280	70
V_{t0} (V)	0.80	–0.90	0.57	–0.71	0.45	–0.45	0.45	–0.45
$\lambda \cdot L$ (μm/V)	0.12	0.08	0.16	0.16	0.08	0.08	0.10	0.15
C_{ox} ($fF/\mu m^2$)	1.8	1.8	4.5	4.5	8.5	8.5	25	25
t_{ox} (nm)	18	18	8	8	5	5	1.2	1.2
n	1.5	1.5	1.8	1.7	1.6	1.7	1.85	1.85
θ (1/V)	0.06	0.135	1.5	1.0	1.7	1.0	2.3	2.0
m	1.0	1.0	1.8	1.8	1.6	2.4	3.0	3.0
$C_{ov}/W = L_{ov}C_{ox}$ (fF/μm)	0.20	0.20	0.20	0.20	0.35	0.35	0.50	0.50
$C_{db}/W \approx C_{sb}/W$ (fF/μm)	0.50	0.80	0.75	1.10	0.50	0.55	0.45	0.50

Table 1: Typical process parameters

expressions for their gain $\frac{v_{out}}{v_{in}}$ in dependence of g_m and r_{ds}, R_L and R_S. Assume that pFETs and nFETs have the same g_m and r_{ds} and that all the circuits' point of operation is at the same large signal current through the common gate transistor. Neglect the body effect g_s and assume the transistors are in their active region/in saturation and that $g_m >> \frac{1}{r_{ds}}$.

Task 3 (3p): In addition to the above task's assumptions also assume that $R_L = 0.5 * r_{ds}$ and $R_S = r_{in}$. Write down the resulting even more simplified (where possible) transfer functions and order the circuits from the previous task according to their small signal low frequency voltage gain, i.e. make a list beginning with the circuit with the highest gain and ending with the one with the lowest gain.

Chapter 4

Task 4 (3p): Consider the inverter in figure 2 with W=4μm and L=0.35μm. Assume the parameters of the 0.35μm process and a Vdd of 3.3V. Compute the large signal point of operation, i.e. the input voltage for which the large signal source drain currents for both nFET and pFET are equal. Also note down that source-drain current.

Task 5 (3p): What is the frequency dependent transfer function (state the DC gain and draw a Bode plot!) and the -3dB bandwidth of the inverter of the previous task, if you consider C_{db} as a load capacitance and neglect other parasitic capacitances like C_{gs} and C_{gd}?

Task 6 (3p): Consider a simple current mirror as depicted in figure 3. Derive and draw a small signal model, including relevant capacitances of the transistors among C_{db}, C_{gs} and C_{gd}. Also derive the 'current-mode' transfer function $H(s) = \frac{i_{out}(s)}{i_{in}(s)}$, i.e. where the input and output signals are currents. The

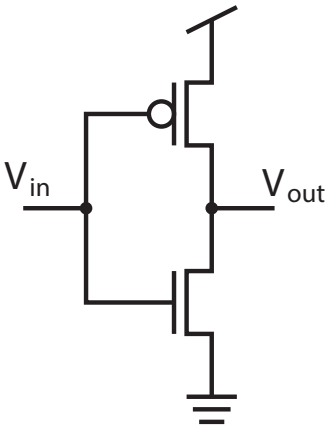

Figure 2: Large signal schematics of an inverter

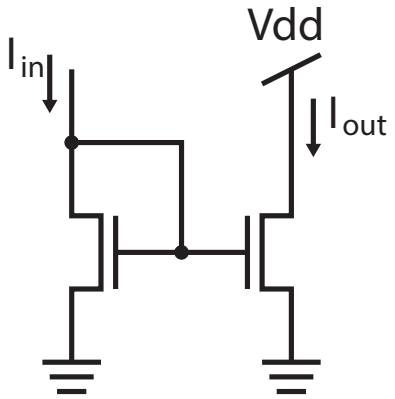

Figure 3: Large signal schematics of a simple current mirror

output node is at a constant voltage (e.g. Vdd) that assures that the output transistor is in the active region/saturation .

Task 7 (3p): For the current mirror in the previous task, use the parameters of the 0.35μm process, W=L=1 um, and a point of operation $I_{in} = 20\mu$A. Compute the -3dB cut-off frequency and draw a Bode plot of the current mode transfer function.

Chapter 5

Task 8 (4p): Consider the two stage transconductance amplifier small signal model of figure 4. At first, assume that the ideal switches are open (not conducting), i.e. that there is no external feedback loop and $V_1 = V_{in}$. In this model, there are no capacitors other than the feedback capacitor between the output of the first and second stage. Derive the transfer function H(s) and explicitly write down the expressions for all poles and zeros.

Task 9 (2p): In continuation of the previous task you may safely assume that the first pole is at a lower frequency than any zeros and sketch a Bode-plot for the H(s) with all important points marked and their values indicated in dependency of g_{m*}, R_*, C_C.

Task 10 (4p): Continuing from the previous task: if you consider a negative feedback network with gain β (i.e. with the switches conducting and $V_1 = V_{in} - \beta V_{out}$), for which values of β would you expect a phase margin bigger than 45^o? Write an expression for the limit of β in terms of the DC gain and the zero(s) and pole(s)! Can you indicate this somehow graphically in your Bode-plot?

Chapter 6

Task 11 (4p): Figure 5 shows an adaption of the wide-swing current mirror with enhanced output impedance from the book. All transistors shall have the same length, and the widths are noted proportional to each other. Write

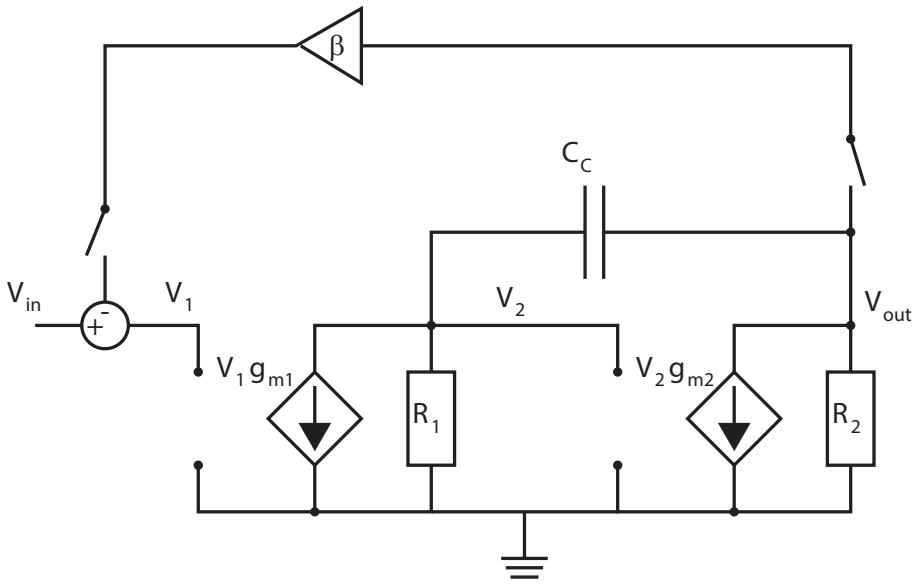

Figure 4: Two stage transconductance amplifier with capacitive feedback but neither load- nor parasitic capacitances.

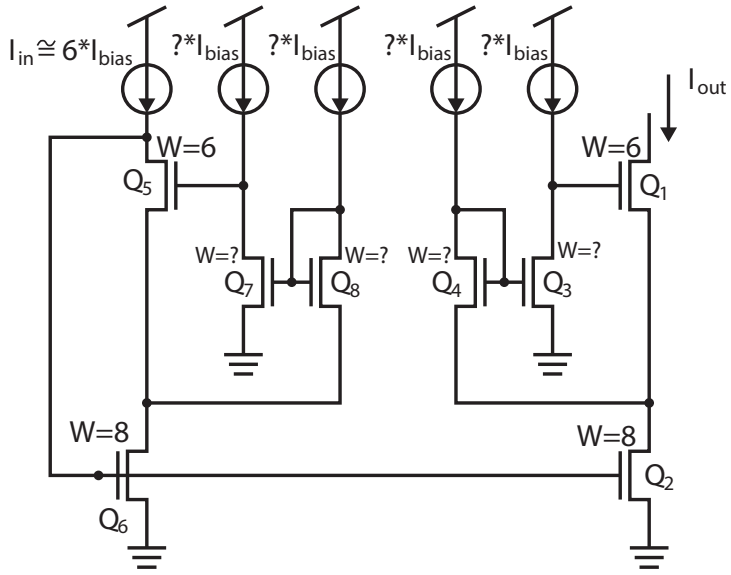

Figure 5: Advanced current mirror with wide-swing at the output and enhanced output impedance.

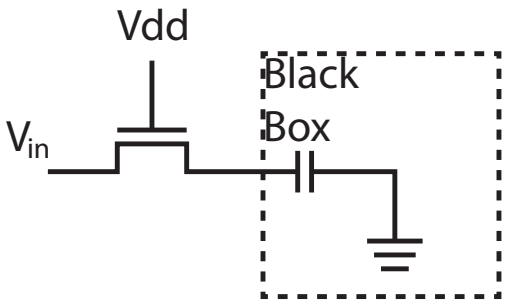

Figure 6: Pass transistor

down the values for the parameters noted with '?' in the figure, i.e. what the relative widths of Q_7, Q_8, Q_4, and Q_3, and what the bias currents to those transistors will have to be! The goal is that the output voltage swing at which the current mirror works (i.e. all transistors are in saturation/in their active region) shall be in the range from $2V_{eff}$ to Vdd.

Chapter 9

Task 12 (4p) Often transistors are used as pass-transistors to connect or disconnect an input, i.e. like a simple switch. Let us assume that an nFET of the 0.35μm process of table 1 with Vdd=3.3V is used as such a pass transistor and that it connects an input node at a point of operation of Vdd/2 to a black box circuit (with purely capacitive input impedance). It is set to be conducting, i.e. its gate voltage is at Vdd. Derive the noise spectral density function of the thermal noise *current* (ignore the flicker-noise!) through the pass transistor at room temperature. Hint: will this pass transistor operate in its triode- or active region? Note that there are different models for those two cases, one can be found in the table with noise models in the book and the other only in the text in the book! W=10μm, L=0.5μm. Sketch the noise spectral density function on a log-log plot, with the y-axis in dBm or V^2/Hz and the x-axis in $\log_{10}$(f). If you assume a noise bandwidth of 1MHz, what will be the total rms noise power?