INF3410 — Fall 2015

Book Chapter 6: Basic Opamp Design and Compensation

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Classic Uses of Opamps

An Operational Amplifier (Opamp) is a high gain voltage amplifier with differential input.
Classic applications are:

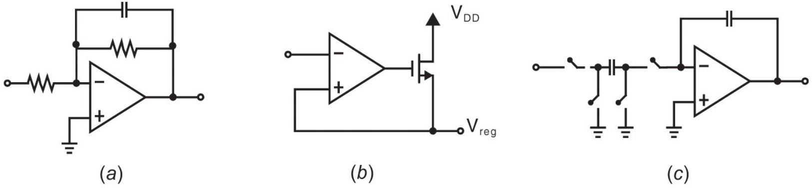


Figure 6.1

Content

Two Stage CMOS Opamps

The classic way of getting high gain is a two stage solution, also providing high output swing (as opposed to e.g. cascode gain stages).

General principle:

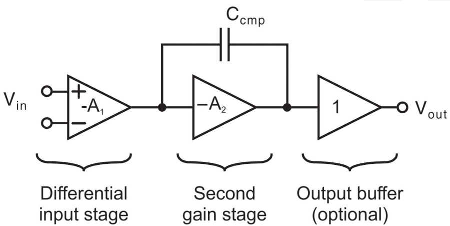


Figure 6.2

The *compensation* capacitor C_{cmp} in conjunction with the output resistance of the first stage limits the bandwidth, which can be handy to stabilize the circuit when employed in a feedback configuration.

Two Stage CMOS Opamp Example

A simple example:

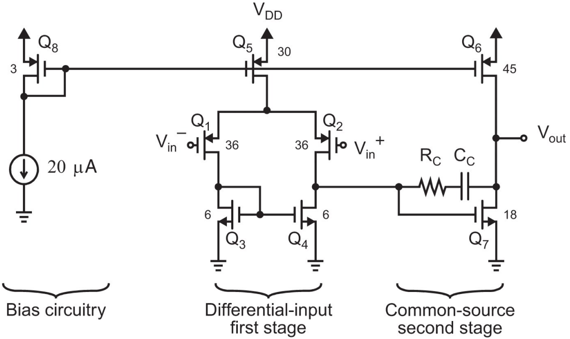


Figure 6.3

DC Gain (in a first, mostly valid approximation):

$$A = A_{v1}A_{v2}$$

First Order Approximation of Frequency Response

In mid range (only C_C matters) simplified to:

$$A_{v1} = -g_{m1} Z_{out1} \quad (6.5)$$

$$\approx -g_{m1} \left(r_{ds2} \parallel r_{ds4} \parallel \frac{1}{sC_C A_{v2}} \right) \quad ($$

$$A_v(s) \approx A_{v2} \frac{g_{m1}}{sC_C A_{v2}} = \frac{g_{m1}}{sC_C}$$

$$\omega_{ta} \lesssim \frac{g_{m1}}{C_C} \quad (6.9)$$

$$= \frac{I_{bias}}{V_{eff1} C_C} \quad (6.10, \text{strong inv.})$$

$$= \frac{q I_{bias}}{2nkTC_C} \quad (\text{weak inv.})$$

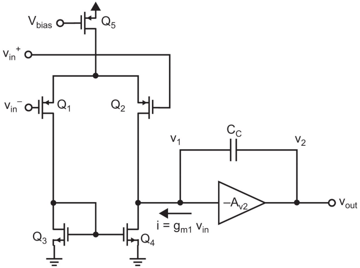


Figure 6.4

Second Order Approximation of Frequency Response (1/2)

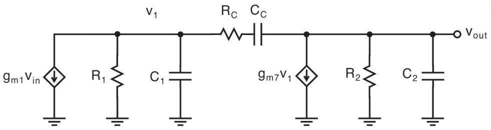


Figure 6.5

Second order becomes necessary for analysis close to ω_{ta}. Without R_C:

$$A_v(s) = \frac{g_{m1}g_{m7}R_1R_2\left(1 - \frac{sC_C}{g_{m7}}\right)}{1 + sa + s^2b} \quad (6.15)$$

Interrupt: Second Order Approximation Deduction 1

$$\begin{aligned}
v_1\left(\frac{1}{R_1} + sC_1 + sC_C\right) + v_{in} g_{m1} &= v_{out} sC_C \quad |1 \\
v_{out}\left(\frac{1}{R_2} + sC_2 + sC_C\right) + v_1 g_{m7} &= v_1 sC_C \quad |2
\end{aligned}$$

$$v_1 = v_{out} \frac{\frac{1}{R_2} + sC_2 + sC_C}{sC_C - g_{m7}} \quad | \rightleftharpoons 2 \rightarrow 3$$

Interrupt: Second Order Approximation Deduction 2

$$v_{out}\frac{\frac{1}{R_2}+sC_2+sC_C}{sC_C-g_{m7}}\left(\frac{1}{R_1}+sC_1+sC_C\right)+v_{in}g_{m1} \quad = \quad v_{out}sC_C \;\; |3\rightarrow 1=4$$

$$v_{out}\left[sC_C-\frac{\frac{1}{R_1R_2}+s\left(\frac{C_2+C_C}{R_1}+\frac{C_1+C_C}{R_2}\right)+s^2(C_1+C_C)(C_2+C_C)}{sC_C-g_{m7}}\right] \quad = \quad v_{in}g_{m1} \;\; |\rightleftharpoons 4=5$$

$$v_{out}\left[\frac{sC_C(sC_C-g_{m7})-\frac{1}{R_1R_2}-s\left(\frac{C_2+C_C}{R_1}+\frac{C_1+C_C}{R_2}\right)-s^2(C_1+C_C)(C_2+C_C)}{sC_C-g_{m7}}\right] \quad = \quad v_{in}g_{m1} \;\; |\rightleftharpoons 5=6$$

Interrupt: Second Order Approximation Deduction 3

$$v_{out}\frac{-\frac{1}{R_1R_2}-s(C_Cg_{m7}+\frac{C_2+C_C}{R_1}+\frac{C_1+C_C}{R_2})+s^2\left[C_C^2-(C_1+C_C)(C_2+C_C)\right]}{sC_C-g_{m7}} = v_{in}g_{m1} \quad |\rightleftharpoons 6=7$$

$$\frac{v_{out}}{v_{in}} = g_{m1}\frac{sC_C-g_{m7}}{-\frac{1}{R_1R_2}-s(C_Cg_{m7}+\frac{C_2+C_C}{R_1}+\frac{C_1+C_C}{R_2})+s^2\left[C_C^2-(C_1+C_C)(C_2+C_C)\right]} \quad |\rightleftharpoons 7=8$$

Interrupt: Second Order Approximation Deduction 4

$$\frac{v_{out}}{v_{in}} = \frac{R_1 R_2 g_{m1} g_{m7}(\frac{sC_C}{g_{m7}} - 1)}{-1 - s(C_C g_{m7} R_1 R_2 + R_2(C_2 + C_C) + R_1(C_1 + C_C)) + s^2\left[R_1 R_2(C_C^2 - (C_1 + C_C)(C_2 + C_C))\right]} \quad |\text{rearrangi}$$

And that's the same as (6.15) with minimal rearranging. Thus:

$$z_1 = -\frac{g_{m7}}{C_C}$$

Second Order Approximation of Frequency Response (2/2)

$$|\omega_1| \approx \frac{1}{g_{m7}R_1R_2C_C} (6.19)$$

$$|\omega_2| \approx \frac{g_{m7}}{C_1 + C_2} (6.20)$$

$$z_1 = \frac{g_{m7}}{C_C}$$

The problem with positive zeros is negative phase shift, here dependent on C_C: Increasing C_C will reduce ω_{ta} but also the frequency at which the phase shift becomes -180^o, making a feedback system no more stable.

Compensation Tools

Dominant pole compensation: Moving (only) the dominant pole of the open loop gain to a lower frequency. (Shifting ω_t to a frequency smaller than the second most dominant pole)

Lead compensation: Introducing a 'right hand side' zero that shifts the -180^o phase shift to higher frequencies.

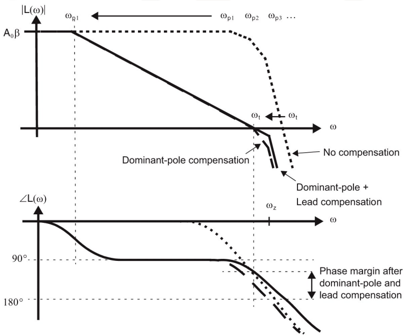


Figure 6.8

Interrupt: Second Order Approximation Deduction 5 (With R_C)

with R_C in series the admittance sC_C becomes $\frac{sC}{1+sC_CR_C}$ and thus the term $\frac{sC_C}{g_{m7}} - 1$ in the nominator of (6.15) becomes (neglecting influences of R_C elswhere):

$$\begin{aligned} \frac{sC_C}{g_{m7}} - 1 &\to \frac{sC_C}{(1+sC_CR_C)g_{m7}} - 1 \\ &\to \frac{sC_C - g_{m7} - sg_{m7}C_CR_C}{(1+sC_CR_C)g_{m7}} \end{aligned}$$

The nominator of that term becomes:

$$s(C_C - g_{m7}C_CR_C) - g_{m7} \stackrel{/g_{m7}}{\to} sC_C(\frac{1}{g_{m7}} - R_C) - 1 \text{ (Philipp 9)}$$

Lead compensation (1/2)

With R_C the zero becomes (without much influencing the poles!):

$$z_1 = \frac{-1}{C_C\left(\frac{1}{g_{m7}} - R_C\right)} \quad (6.43)$$

R_C can now be chosen to eliminate the zero (see equation(Philipp 9)!):

$$R_C = \frac{1}{g_{m7}} \quad (6.44)$$

or to negate the non-dominant pole ω_2 (using (6.20)):

$$R_C = \frac{1}{g_{m7}}\left(1 + \frac{C_1 + C_2}{C_C}\right) \quad (6.45)$$

Lead compensation (2/2)

Or to choose R_C even higher to not cancel phase shift due to $\omega_{2/eq}$ to -180^o entirely but to 'delay' it (create a phase lead), e.g. (dependent on a β in a closed loop application):

$$R_C \approx \frac{1}{1.7\beta g_{m1}}$$

IN all of the above R_C may conveniently be implemented as transistor Q_9 in triode region (this β is the EKV notation $\beta = \mu C_{ox}\frac{W}{L}$):

$$R_C = \frac{1}{\beta V_{eff9}}$$

Slew Rate Concept

The ’speed’ of an OpAmp output is not only limited by bandwidth but also by the bias current, as the output current cannot be bigger than the bias current. Thus, a big input step will get the transconductance out of its linear range and the output current saturates. Thus the maximum output gradient of an OpAmp is called *slew rate* (SR) in units [V/s].

Slew Rate Illustration

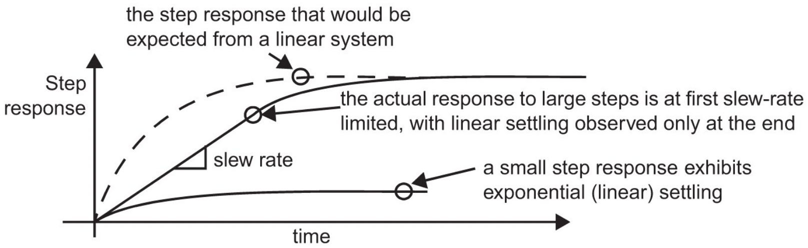


Figure 6.6

$$V_{step,max} < SR\dot{\tau}$$

Increasing the Slew Rate

The slew rate is dictated by the bias current and the compensation capacitor:

$$SR = \frac{I_{D5}}{C_C}$$

However, simply increasing the bias current or decreasing C_C will raise ω_{ta}, potentially making the circuit unstable. Thus, one needs also to increase ω_2 and/or V_{eff1} (i.e. reduce $(W/L)_1$) to maintain proper compensation, which the book says are the only ways to design for higher slew rate.

Systematic Offset

Basically the ’zero output’ of stage one has to closely match the ’zero input of stage two. (What happens oterwise?) ’Zero input’ of stage two means the currents in Q_6 and Q_7 need to be equal. ’Zero output’ from stage one means that Q_4 is sinking half the bias current (while Q_5 is sourcing the whole bias current). Thus, if for instance Q_5 and Q_6 have the same W/L, then Q_7 needs to have twice the W/L of Q_4. More generally:

$$\frac{W/L_7}{W/L_4} \stackrel{!}{=} 2\frac{W/L_6}{W/L_5} \quad (6.38)$$

Content

Cascode Current Mirror

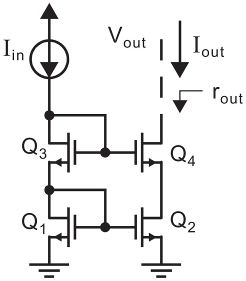


Figure 3.14

The cascode current mirror in chapter 3 reduces the output headroom by $V_{out} > 2V_{eff} + V_{t0}$ (3.42). The problem is that the sources of the transistor closest to the output is at $V_{eff} + V_{t0}$. There are alternatives that provide equally high output resistance with less loss of headroom/output-swing.

Wide-Swing Current Mirrors

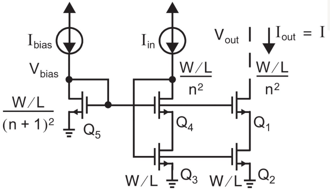


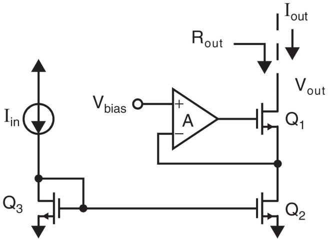
Figure 6.12

Think this circuit through for the case where $I_{bias} = I_{in}$. Then the current through all transistors is the same. For constant current in strong inversion (!) if you scale W/L by 1/a^2, V_{eff} scales with a.

$$V_{s1} = V_{g5} - V_{gs1} = (V_{eff}(n+1) + V_{t0}) - (V_{eff}n + V_{t0}) = V_{eff}$$

and thus $V_{out} > (n+1)V_{eff}$ (6.78) for all transistors to be saturated. For instance for n=1 the optimum $V_{out} > 2V_{eff}$ (6.79) is obtained. For $I_{in} < I_{bias}$, the minimum V_{out} will shrink in absolute terms, but will no longer be optimal in terms of V_{eff}. For $I_{in} > I_{bias}$ the output resistance drops dramatically as the transistors enter the triode region.

Enhanced Output Impedance Current Mirrors (1/2)



Similarly to the cascode current mirror V_{d2} (and thus the current through Q_2) is attempted to be kept as constant as possible. While V_{g1} is constant in the cascode current mirror, here it is actively moved to compensate the influence of V_{out} on V_{d2}

So while the a circuit with constant V_{g1} would have $R_{out} \approx g_{m1} r_{ds1} r_{ds2}$ (like a cascode current mirror), this circuit has:

$$R_{out} \approx (A+1) g_{m1} r_{ds1} r_{ds2} \quad (6.82)$$

Enhanced Output Impedance Current Mirrors (2/2)

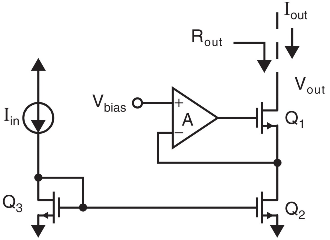


Figure 6.13

Note:

- V_{bias} needs to be big enough to keep Q_2 in saturation!
- Stability of feedback loop needs to be veryfied!
- Parasitic resistance from drain to bulk may become the actual limiting factor!

Enhanced Gain Cascode Gain Stage

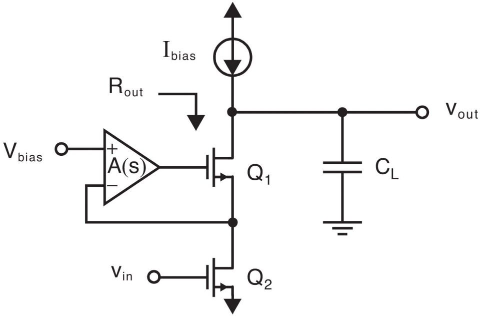


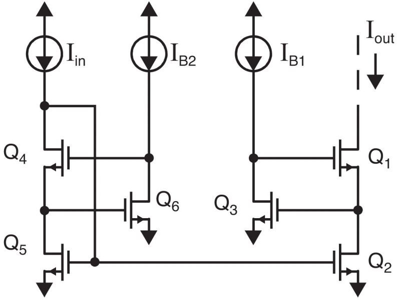
Figure 6.14

The same technique can be used to enhance the output resistance, and thus the gain of a cascode gain stage. **Note:** The current source needs a similarly enhanced output resistance!

$$A_V(s) = -g_{m2}\left(R_{out} \parallel \frac{1}{sC_L}\right) \qquad (6.83)$$

$$R_{out}(s) = g_{m1}r_{ds1}r_{ds2}\left(1 + A(s)\right) \qquad (6.84)$$

Enhanced Output Impedance Current Mirrors Implementation



The amplifier is a common source gain stage. **Note:** Again the output swing is quite limited by $V_{out} > V_{eff3} + V_{tn} + V_{eff1}$ (one way of looking at this is that the amp's $V_{bias} = V_{eff3} + V_{tn}$)

$$r_{out}(s) \approx g_{m1} r_{ds1} r_{ds2} (g_{m3} \frac{r_{ds3}}{2}) \quad (6.93)$$

Wide Swing AND enhanced impedance

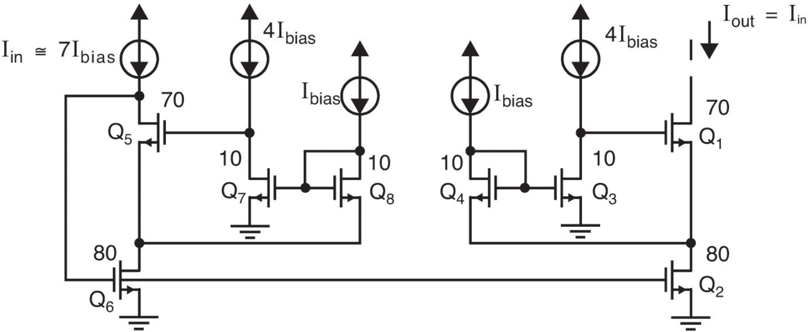


Figure 6.16

Space and Power Conserving Variant

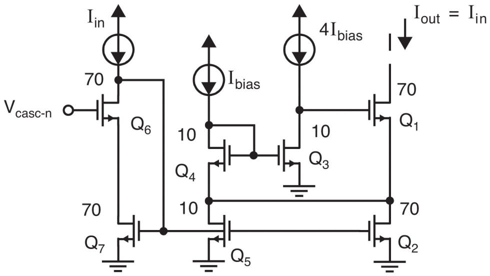


Figure 6.17

Quite equivalent with worse current matching but less power and layout space consumption. More modular with splitting Q_2 and presumably better stability.

Content

Operational Transconductance Amplifiers

These are operational amplifiers with high output impedance, limited in bandwith by the output load (and not in internal nodes that are low impedance nodes). Thus, mainly suited for capacitive output loads only!

Current Mirror Opamp

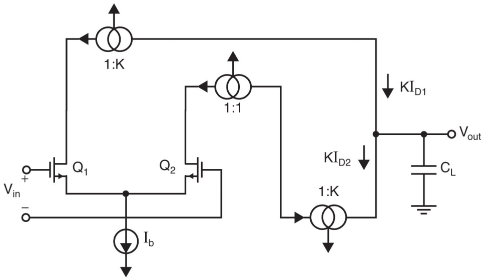


Figure 6.21

A simple concept boosting the output current resulting in good bandwidth and good slew rate assuming C_L is dominant.

$$A_V(s) = \frac{Kg_{m1}r_{out}}{1+sr_{out}C_L} \quad (6.119)$$

$$\omega_{ta} \approx \frac{Kg_{m1}}{C_L} = \frac{2KI_{D1}}{C_L V_{eff1}} \quad (6.121)$$

$$SR = \frac{KI_b}{C_L} \quad (6.124)$$

Folded Cascode Opamp

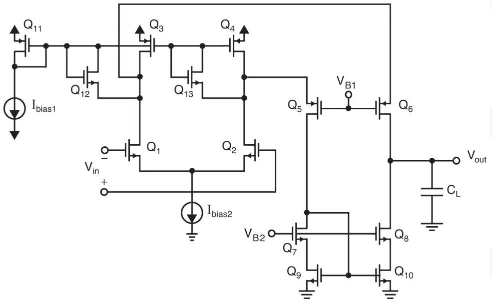


Figure 6.20

Ignore Q_{12} and Q_{13} for an initial analysis. Think of it as an extension of a differential pair: the cascodes simply increase the output resistance of the differential output current ⇒ higher voltage gain given the same transconductance.

Content

Interrupt: Common Mode Rejection Ratio

On the white board...

Basic TransAmp with Diff Output

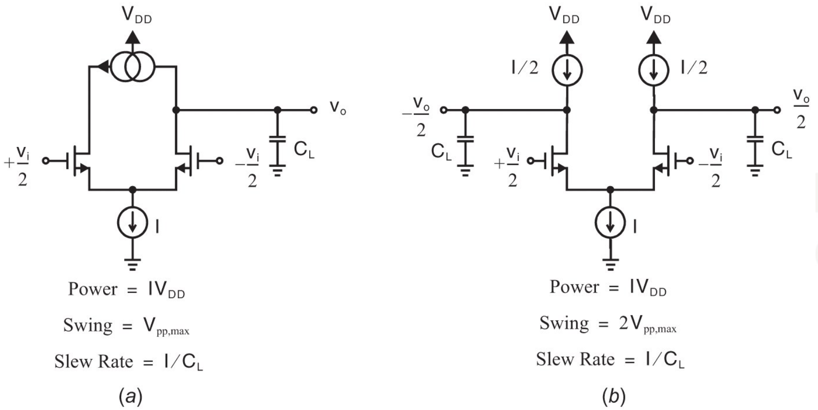
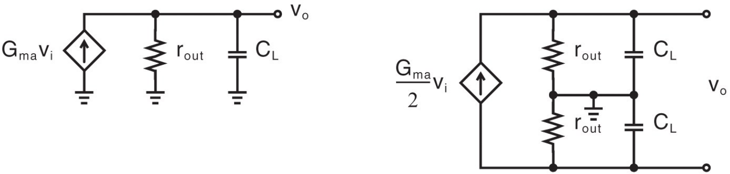


Figure 6.24

Small Signal Considerations



(a)	(b)
dc gain: $G_{ma}r_{out}$	dc gain: $\frac{G_{ma}}{2}2r_{out} = G_{ma}r_{out}$
$\omega_{-3\,dB} = 1/(r_{out}C_L)$	$\omega_{-3\,dB} = 1/(r_{out}C_L)$
$\omega_{ta} = G_{ma}/C_L$	$\omega_{ta} = G_{ma}/C_L$

Figure 6.25

Fully Differential Current Mirror Opamp

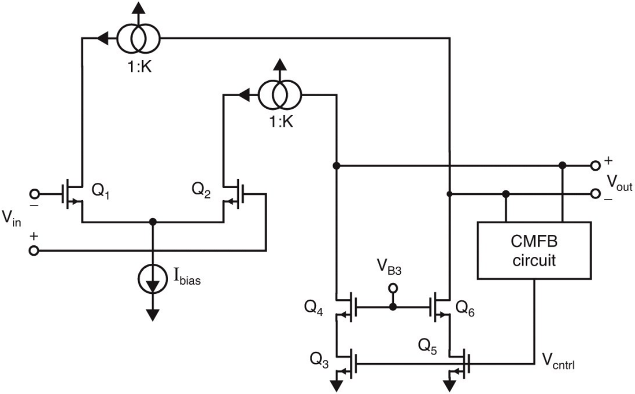


Figure 6.29

Dual Single Ended Structure

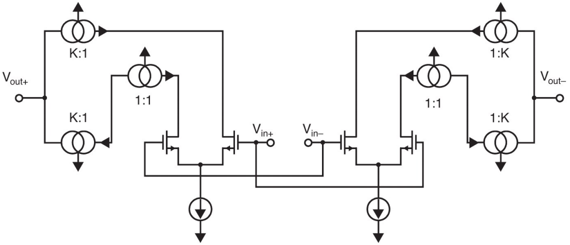


Figure 6.31

Actively pulling the output up *and* down. (Class AB amplifier as opposed to class A). Better symmetrical slew rate. CMFB needed!

Partially Dual Single Ended Structure

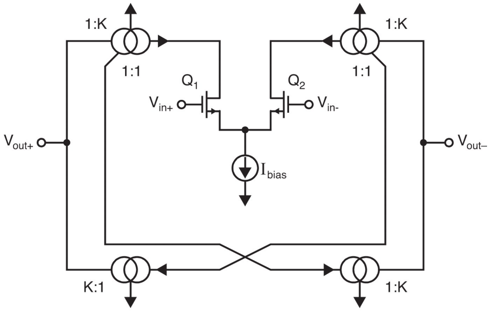


Figure 6.30

Actively pulling the output up *and* down. Also better (symmetrical) slew rate, but maybe worse bandwith (due to more capacitance in current mirrors). CMFB needed!

Wide Input Fully Differential Cascode OpAmp

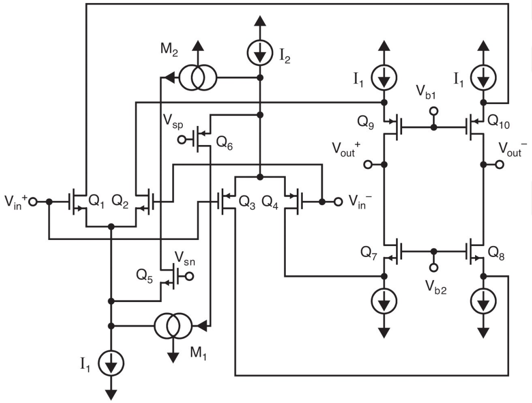


Figure 6.32

A problem with low supply voltage is the minimum requirement for the common mode voltage. Complementary input pairs help.

Two Stage Differential OpAmp

Another challenge with low supply voltage is the output swing. Common source output stages do comparatively well: just one V_{eff} away from the rails.

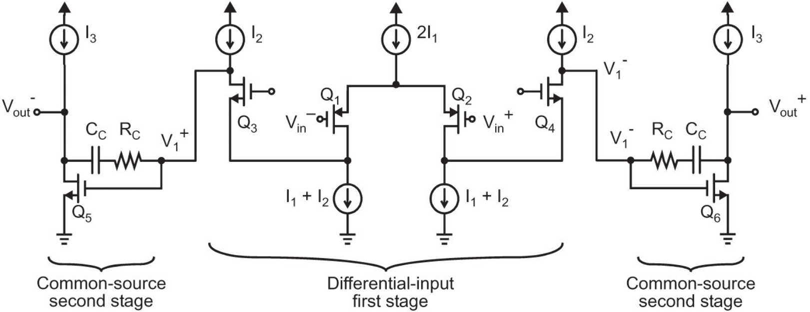


Figure 6.33

Common Mode Feedback Principle

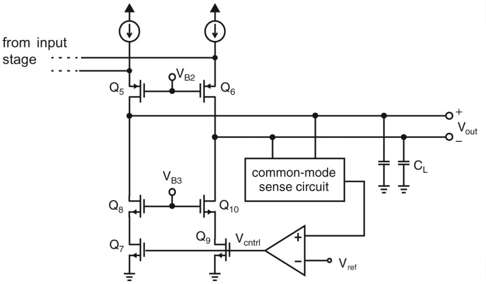


Figure 6.37

Carefull: A feedback loop that needs to be stable!

Continuous Common Mode Feedback Variant 1

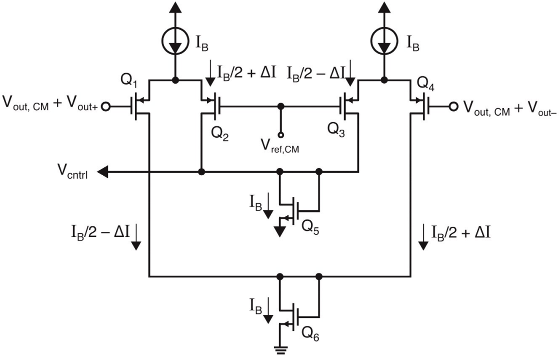


Figure 6.34

Continuous Common Mode Feedback Variant 2

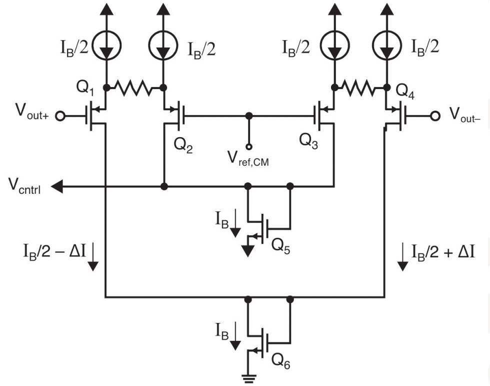
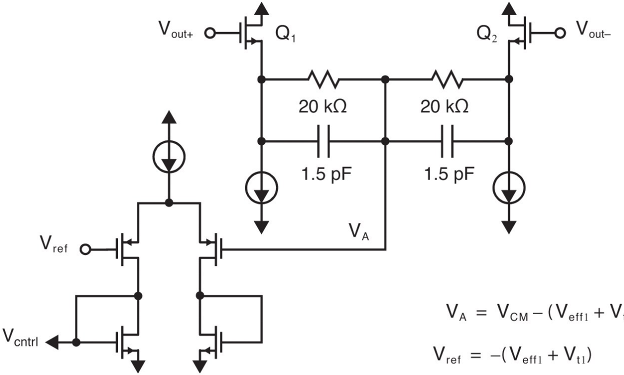


Figure 6.35

Saturation of the diff-pairs is a problem as the outputs swing much wider as the input ⇒ reduce gain.

Continuous Common Mode Feedback Variant 3



$$V_A = V_{CM} - (V_{eff1} + V_{t1})$$

$$V_{ref} = -(V_{eff1} + V_{t1})$$

Figure 6.36

Switched Cap Common Mode Feedback

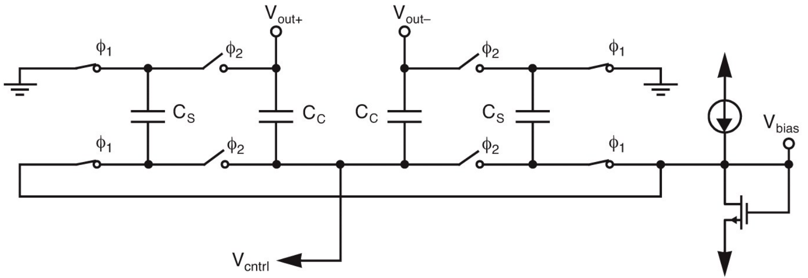


Figure 6.38

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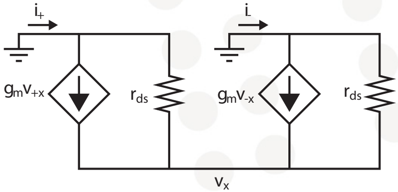
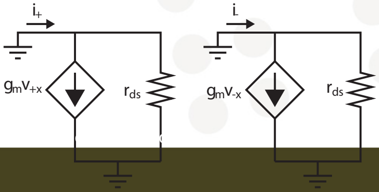
DiffPair

At the core of almost all differential CMOS amplifiers is the diff-pair. The diff-pair invariably translates a differential input voltage into a differential output current around a small signal operating point. (Interestingly this is true for any large signal monotonic function of $I_D(V_{GS})$...) From here on it is best to think in currents for a while rather than voltages.



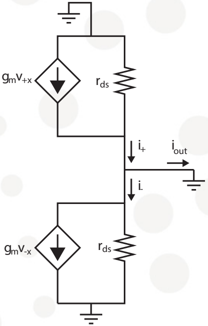
Differential Current Source

With complementary inputs ($v_{+x} = -v_{-x}$), v_x will be clamped to 0V, simplifying things considerably: two small signal current sources with a parallel output-resistance (common source gain stages, in fact). The simplification holds even for the large signal model where the output current is limited by $[0, I_B]$ and the DC $V_{x\pm}$ is the average of both inputs. The large signal model is a sinking(!) current source for an nFET pair: so practically you can only connect anything at the top terminal.



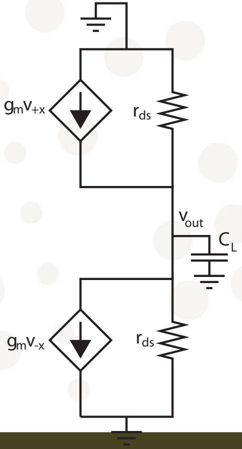
Differential Transconductance Amplifier

Using a current mirror you can turn one of your large signal sinking current sources into a sourcing current source. Thus, you can connect the two output currents in a single node thereby subtracting them: you get a single ended current output if you connect it to a low (input) impedance node.



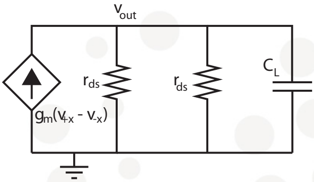
Differential Operational Transconductance Amplifier (1/2)

Or you get a single ended voltage output if you connect it to a high (input) impedance node.



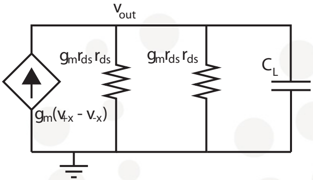
Differential Operational Transconductance Amplifier (2/2)

Rearranging the circuit yields a very simple small signal (DC) model. If the output is connected to a significant capacitive load, this model is even good enough for AC.



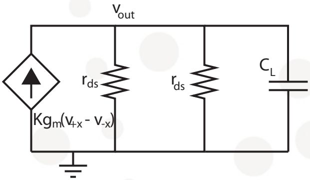
Folded Casode OpAmp

The only difference from a small signal perspective of the folded cascode opamp is an increased output resistance. Simply see the cascode gain stage in chapter 3 if you want to understand how this is achieved starting from two Differential Current Sources, or more precisely from two differntial common source gain stages.



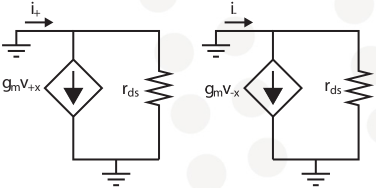
Current Mirror OpAmp

And the current mirror opamp simply increases the transconductance



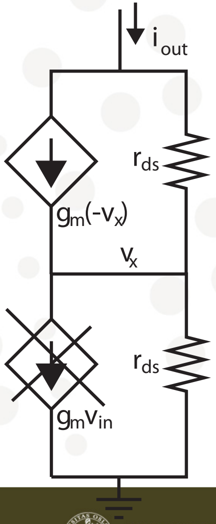
Fully Differential OpAmps

Fully Differential Opamps are in a way simpler, as one can go back to only considering the diff-pair small signal model with complementary inputs. The tricky bit is the large signal point of operation, as one needs to provide exactly matched current sources of $\frac{I_b}{2}$ for each branch of the diff pair to ensure zero output for zero input. Thus, the common mode feedback circuits.



Cascode Principle

This whole section deals (again) with the marvels of a cascode transistor that hugely enhances a common source stage output resistance, bringing it closer to a ideal current source. It basically adds a series resistance of $g_m r_{ds}$:



Advanced Current Mirrors

The rest of this section in the book introduces various ways to a) deduce an optimal V_{bias} to maximize the output swing and b) to make V_{bias} dynamic to increase the output resistance even more. The basic principle of b) is illustrated in:

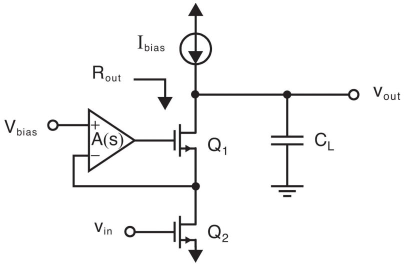


Figure 6.14

Cadence demonstrations live ...