A Design and Simulation for Dynamically Reconfigurable Systolic Array

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Abstract

Systolic array is known as an architecture that can process a large amount of data with high speed, by large scale parallel and pipeline processing. If dynamic reconfiguration of systolic array is realized, flexible circuit construction and reduction of circuit scale become possible, without sacrificing the processing speed.

Therefore, this paper proposes an architecture of dynamically reconfigurable systolic array (DRSA). The circuit was designed by using VHDL, and verified with a logic circuit simulator. The calculations of matrix such as 1-by-64 and 8-by-8 were simulated correctly with a lot of PEs (Processing Element). The effectiveness of proposed architecture is confirmed by circuit simulation results.

1. Introduction

Recently, reconfigurable circuits are attracting a lot of attention [1-3]. Dynamically reconfigurable circuits attempt speed up by large scale parallel and pipeline processing. Similarly, systolic array is known as an architecture that can process a large amount of data with high speed, by large scale parallel processing and pipeline processing. Therefore, systolic arrays are suitable for dynamically reconfigurable circuits for the above reasons.

Figure 1 shows typical systolic array types. Systolic array is constructed by uniform blocks which are connected to nearest blocks. The typical applications are matrix calculations, FFT, pattern matching, and so on. If reconfiguration of systolic arrays is realized, flexible circuit construction and reduction of circuit scale become possible, without sacrificing the processing speed.

Therefore, this paper proposes an architecture of dynamically reconfigurable systolic array (DRSA) and shows its effectiveness.

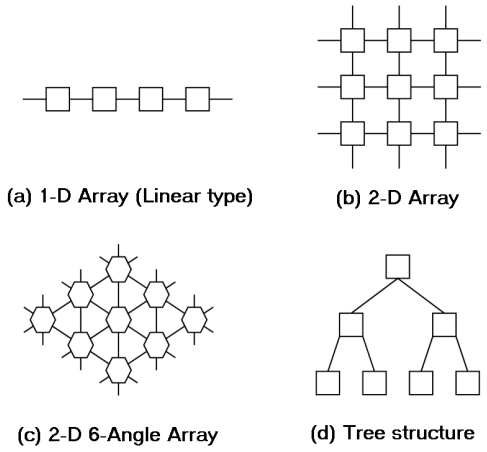

Figure 1 Systolic Array Types

2. Architecture

The proposed dynamically reconfigurable systolic array (DRSA) is composed of the array of the basic block called DRSAB (DRSA Block). The architecture of DRSAB is described as follows.

DRSAB: The DRSAB contains one reconfigurable systolic array block (RSAB), two connection blocks (CB) and one routing block (RB). Figure 2 shows the configuration of DRSAB.

RSAB: The RSAB (Reconfigurable Systolic Array Block) contains four processing elements (PE). Figure 3 shows the configuration of RSAB realized by connecting four PEs through multiplexers. The RSAB can configure 1-by-2 arrays (two sets), a 1-by-4 array or a 2-by-2 array, using multiplexers (Figure 4).

The reason why RSAB contains four PEs is to achieve hierarchical reconfiguration. As a result, the reconfiguration control signal of the entire systolic array can be decreased.

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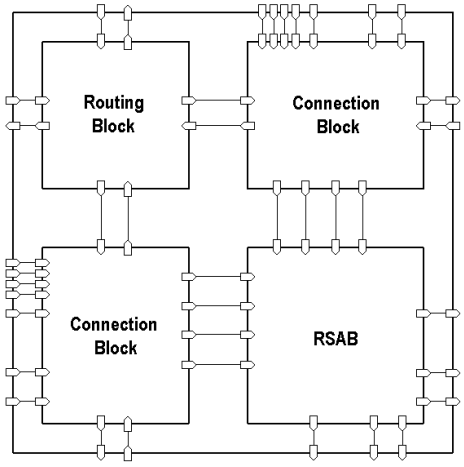


Figure 2 Configuration of DRSAB (DRSA Block)

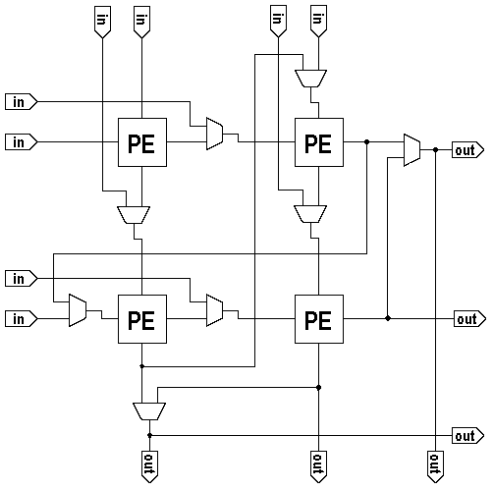


Figure 3 Configuration of RSAB (Reconfigurable Systolic Array Block)

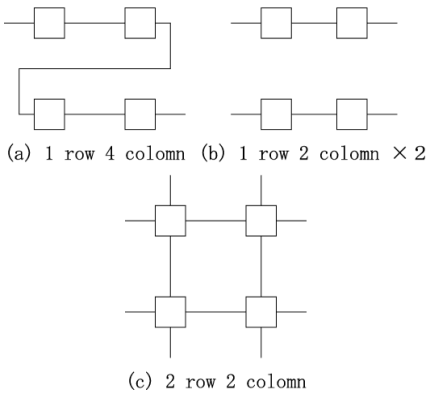


Figure 4 Shapes of PE-array composed by one DRSAB

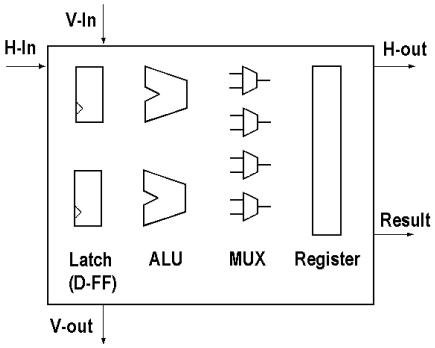


Figure 5 Configuration of PE (Processing Element)

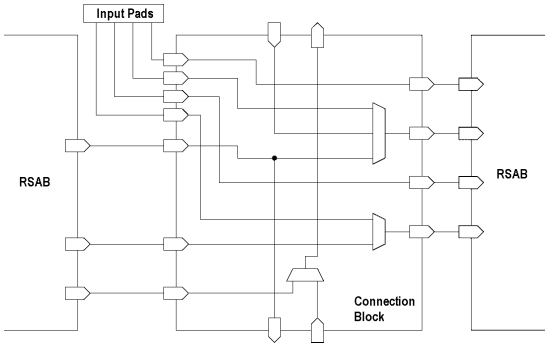


Figure 6 Configuration of CB (Connection Block)

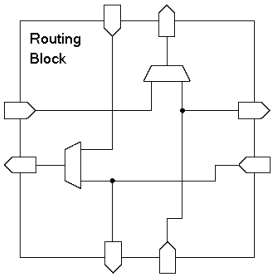


Figure 7 Configuration of RB (Routing Block)

PE: The PE (Processing Elements) is composed of two ALUs, a register, two latches and four multiplexers (Figure 5). The PE has two inputs (V-In, H-In), two latch-outputs (V-Out, H-Out), and an output of operation result (Result).

CB and **RB**: The CB (Connection Block) is used to connect adjoined RSAB. Figure 6 shows the configuration of CB. On the other hand, the RB (Routing Block) is used to connect CBs mutually. Figure 7 shows the configuration of RB. In the DRSAB unit, only systolic array up to size 4 can be constructed. However, RSAB in each DRSAB can be connected mutually by appropriately setting CBs and

RBs, then large scale systolic arrays can be constructed. In addition, dynamic reconfigurations of systolic array become possible by changing the setting of CBs and RBs dynamically. Figure 8 shows an example of PE-array composed by four DRSABs. Moreover, figure 9 shows two examples of arrays by 16 DRSABs.

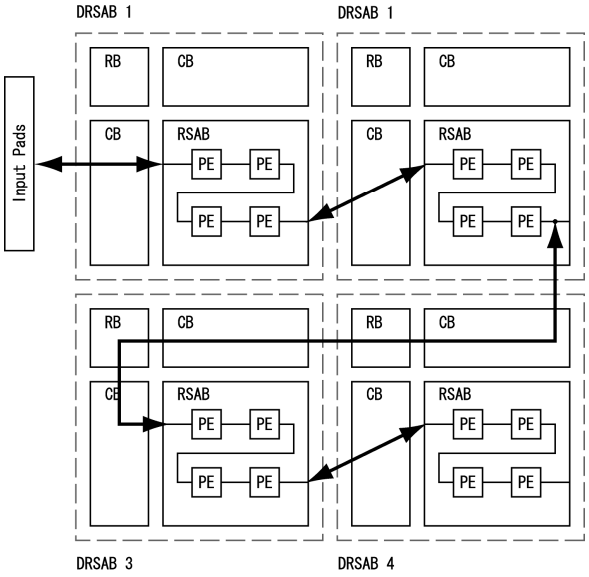
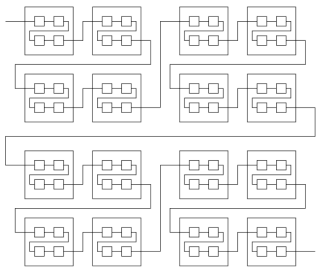
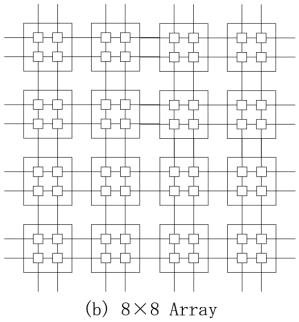


Figure 8 An example of PE-array by four DRSABs



(a) 1×64 Array



(b) 8×8 Array

Figure 9 Examples of PE-array by 16 DRSABs

3. Design

The circuit was designed by using VHDL, and verified by the FPGA design tool (ISE of Xilinx Corp.) and the logic simulator (ModelSim XE III of Mentor Graphics Corp.). To suppress the circuit scale, PE (Processing Element) has designed for addition and multiplication with 8-bit unsigned integer number.

Table 1 summarizes the logic synthesis results of proposed DRSA (Dynamically Reconfigurable Systolic Array). The target FPGA (Field Programmable Gate Array) is Spartan 3A of Xilinx Corp. (XC3S700A-FG484, 700K gate). Similarly, table 2 summarizes the logic synthesis results of conventional systolic array.

It is clarified that the proposed DRSA has larger scale and slower speed than conventional systolic array by the comparison of these two tables. The reason of these disadvantages is that the circuit scale of PE is too small. That is the ratio of overheads (CB, RB, multiplexer) is large in this case. If the PE was for 32-bit floating point operations, the differences between DRSA and usual systolic array would be small.

Table 1 Logic synthesis results of dynamically reconfigurable systolic array

	1	2×2	4×4
Slice	316	1,232	5,859
FF	122	478	1,930
4-input LUTs	567	2,288	10,816
Gate count	5,056	22,415	109,979
Max Freq. [MHz]	81.1	67.4	61.3

Table 2 Logic synthesis results of conventional systolic array

	4×4	8×8
Slice	399	1593
FF	304	1216
4-input LUTs	512	2048
Gate count	7,987	31,951
Max Freq. [MHz]	104.7	104.7

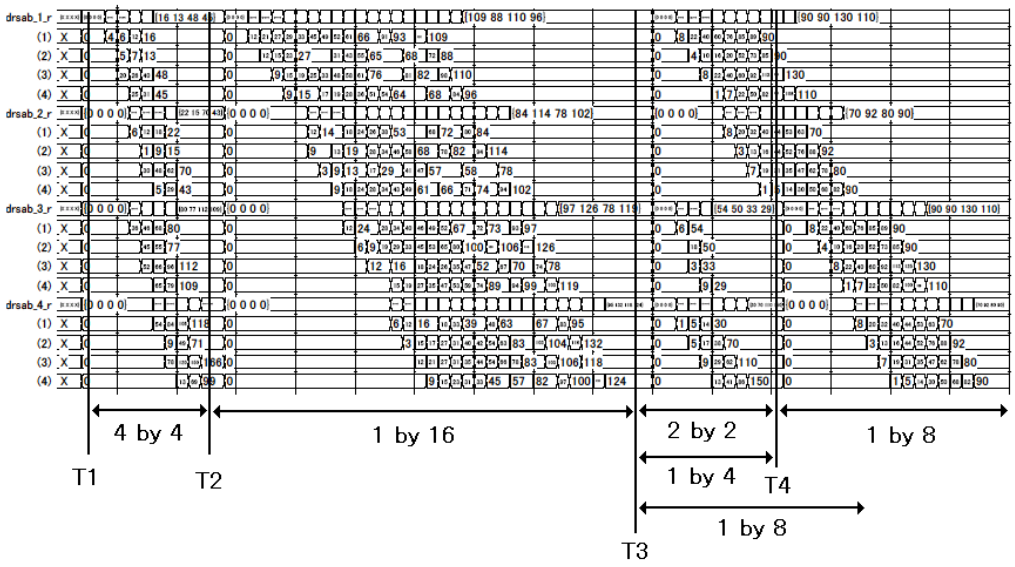


Figure 10 An example of parallel matrix calculations on proposed dynamic reconfigurable systolic array

4. Simulation

Figure 10 illustrates the parallel matrix calculations with various sizes and various types (1-D and 2-D array) on the proposed DRSA with four DRSAB (that is 16 PEs). From the time T1 to T2, the DRSA calculates the product of matrix of 4-by-4. Similarly, from the time T2 to T3, the DRSA calculates the product of matrix of 1-by-16. However, it is remarkable that the DRSA calculates the three matrixes in parallel, from the time T3 to T4. After the time T4, the DRSA calculates two matrixes in parallel by partial reconfiguration. The scheduling, assignments of PEs and control signals of CBs and RBs have to be prepared manually, unfortunately at the present. The effectiveness of proposed architecture is confirmed by the above circuit simulation results.

5. Conclusion

This paper proposed an architecture of dynamically reconfigurable systolic array (DRSA). The detailed design and simulation results were described. It was confirmed that the proposed DRSA can manage the various matrix calculations in parallel by dynamic reconfiguration.

The future works are automatic scheduling, generation of control signals, and compiler software.

Acknowledgements

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