Kristian Bugge (kribug)

IN3160 lab 3

a) The output data signal changes three clock cycles after indata is 1. This delay happens because signal variables after line 27 in delay.vhd(elsif rising_edge(mclk) then) are set three times, which takes up one cycle of the process each.

b) The output data signal changes at 100ns to 00000000, at 750 ns to 11110000 and at 850 to 00001111. The output data is equal to U at 50ns because reset is 1, so the signal isnt set to 0 and indata will not be updated to 00000000 until five clock cycles have passed, therefore the signal sits at U.

c)Because sig1 and sig2 are in the sensitivity, list line 23 (outdata(3 downto 2)<= sig2 & sig1;) are set as if lines 24-27 have ran. This means there is technically no difference between how line 23 and line 29 (outdata(7 downto 6)<= sig2 & sig1;) are set. That is why output(7 downto 6) is always equal to (3 downto 2). output(5 downto 4) is different from output(1 downto 0) because

d)First off, the signals are U initially because signals will not get set until after they are updated because they are removed from the sensitivity list, and only input is on the list triggering changes. In the next loop sig1 and sig2 are given the values from the previous loop and will be the equal because outdata is lagging one loop behind.