Lab 5

Backend

Systems On-Chip

Group nr.:	3
Student-ID-1: ist1112497	Kristian Guttormsen Gøystdal
Student-ID-2: ist1113000	Miki Tecle Hagos
Student-ID-3: ist1112548	Einar Bergslid

Electrical and Computer Engineering
IST-ALAMEDA

2024

1 Layout

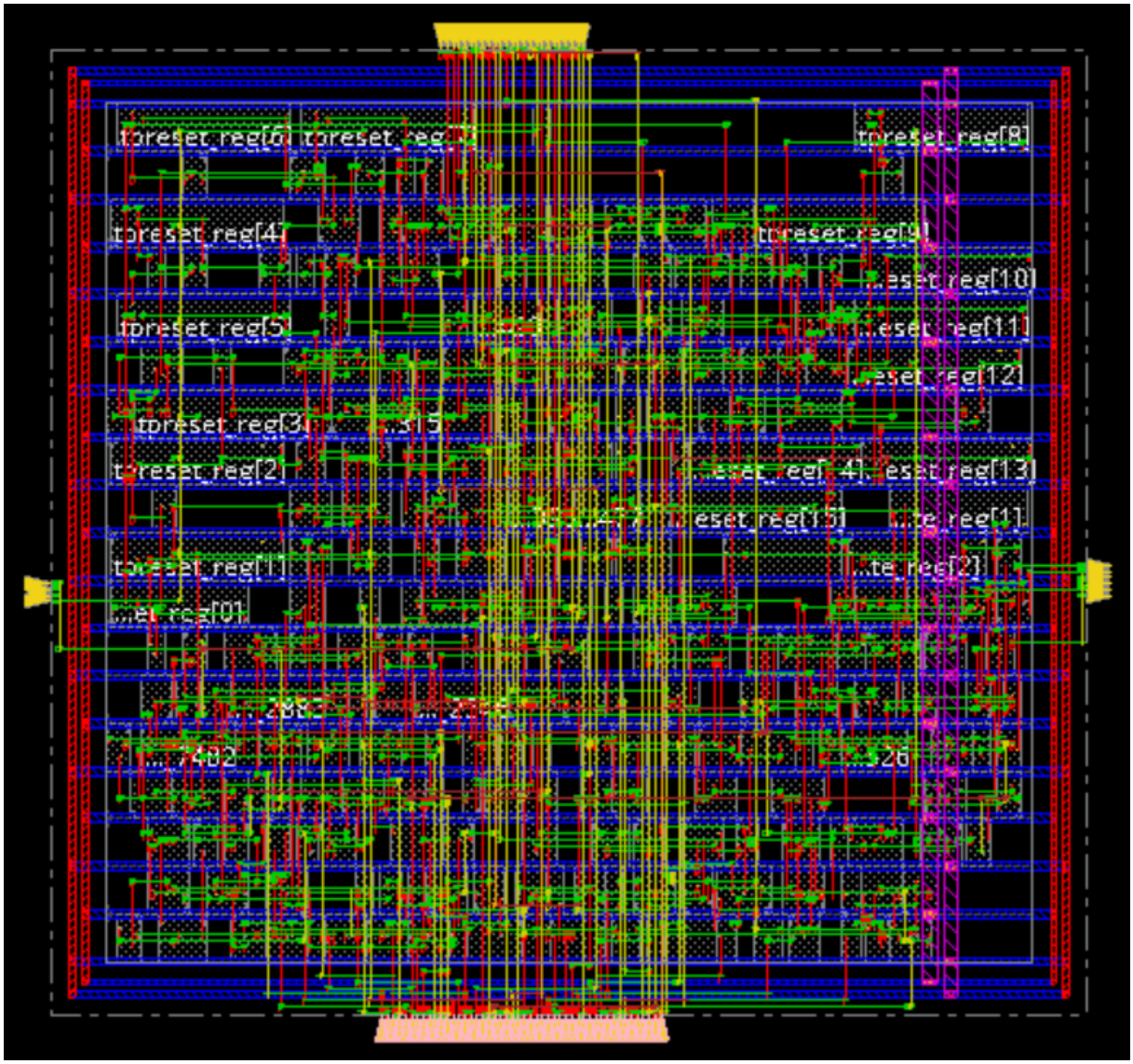

Figure 1: Post-place layout.

Figure 1 shows the layout after adding the PG rings, special route, vertical stripes, and placing the standard cells. Routing is temporary and incomplete. For the PG rings, the inner ring is dgnd and the outer ring is dvdd. The special route horizontal stripes and the added vertical stripes provide easy access to the PG rings from anywhere within the core.

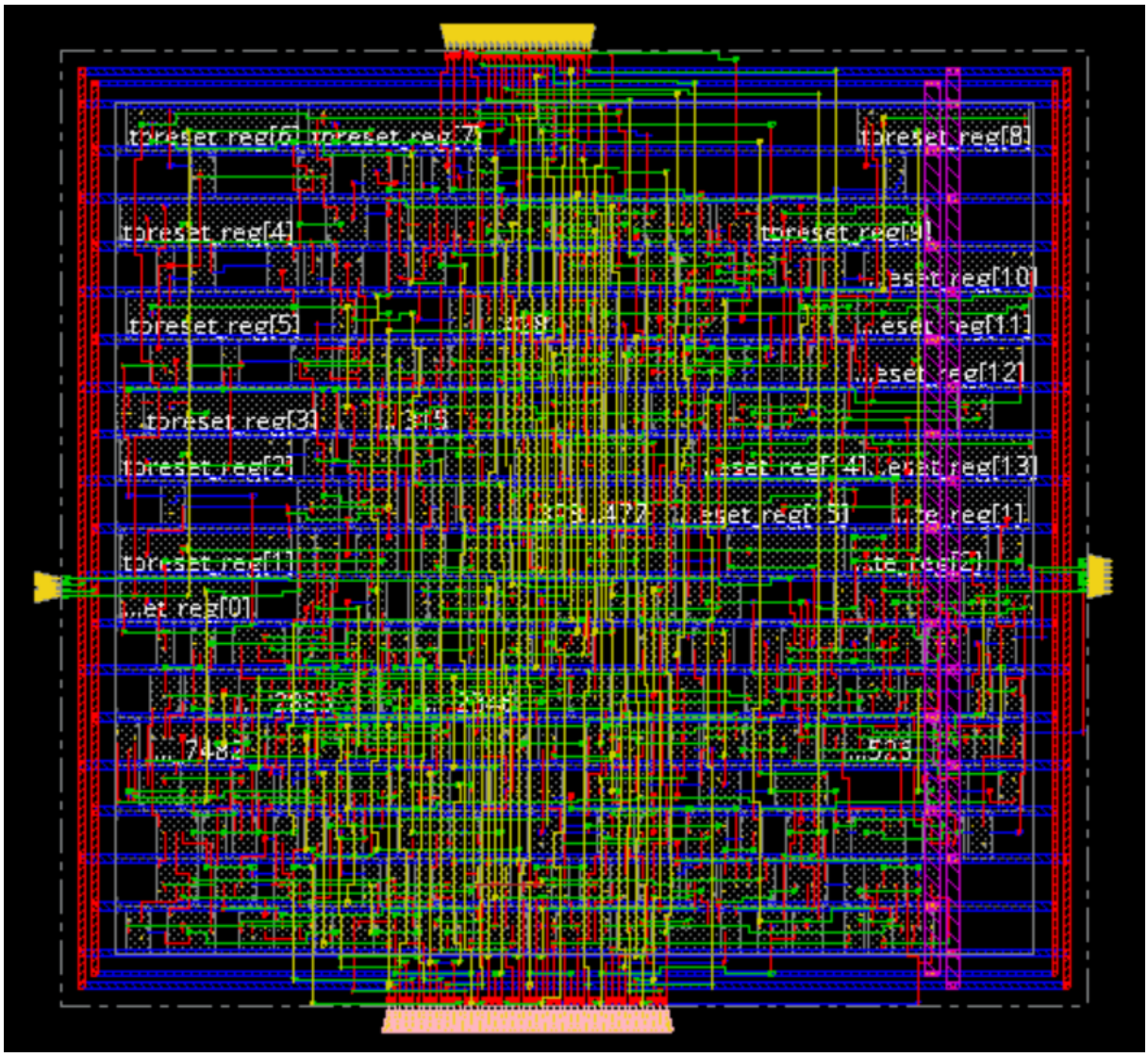

Figure 2: Post-route layout.

After routing, the resulting layout is shown in Figure 2. Here, the routing is optimized and subsequently verified to not contain any DRC errors.

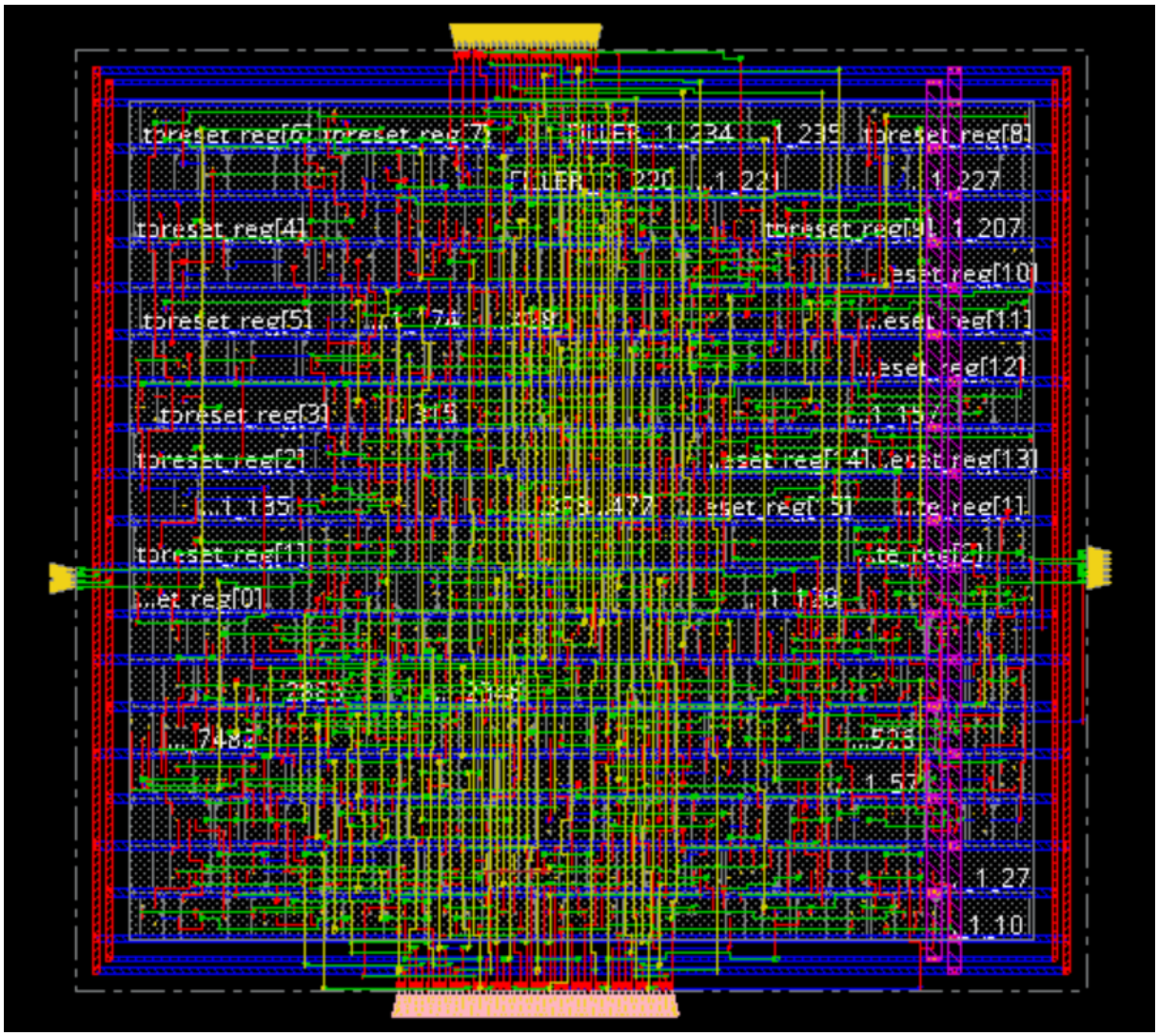

Figure 3: Post-fill layout

After adding filler cells, the placement of standard cells or routing does not change, and we make sure there is no empty space in the core. This is shown in Figure 3.

2 Validations

During the placing and routing of the layout, we perform timing reports between each stage of the process. As shown in Figure 4, each process has a timing requirement that checks if the worst negative slack (WNS) is positive.

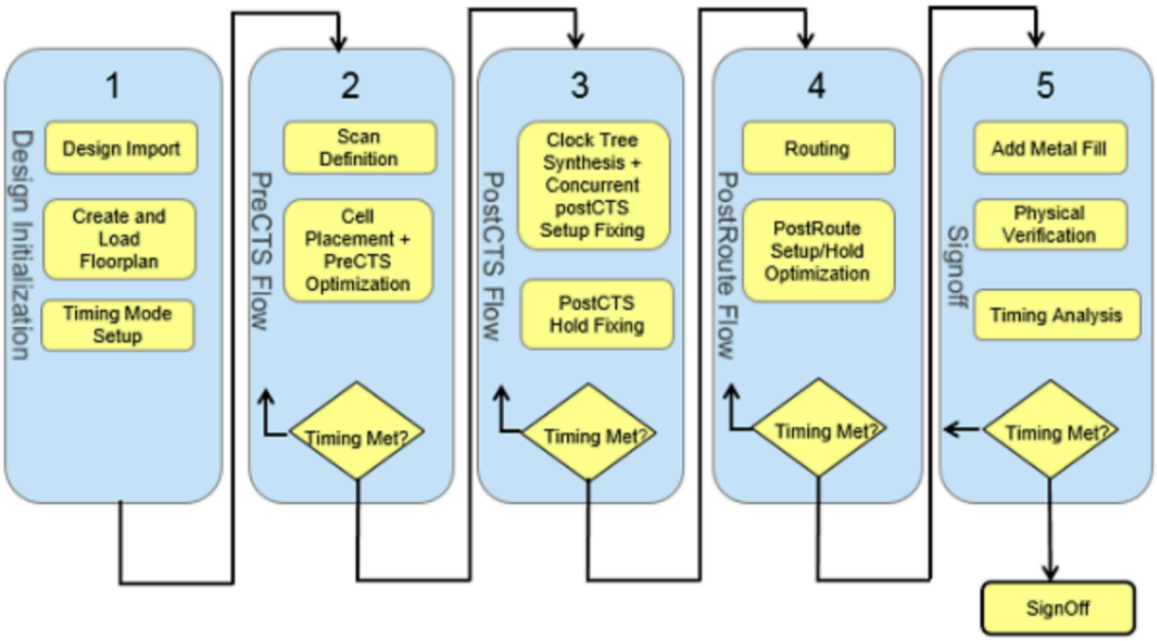

Figure 4: Process steps

If the WNS is negative, this means that the layout will not function properly with the current clock period, and some optimizations must be done.

Table 1 shows the timing report before the placement has been executed and we can see that the WNS is positive by a good margin.

Table 1: Timing report before placing

Setup mode	all	reg2reg	default
WNS (ns)	8.050	8.050	8.439
TNS (ns)	0.000	0.000	0.000
Violating Paths	0	0	0
All Paths	52	50	21

For the next step, we do a timing verification after initial placement and before Clock Tree Synthesis (CTS). Table 2 contains the values for WNS and shows them as less than pre-placement but still positive.

Table 2: Timing report before CTS

Setup mode	all	reg2reg	default
WNS (ns)	7.565	7.565	8.250
TNS (ns)	0.000	0.000	0.000
Violating Paths	0	0	0
All Paths	52	50	21

After CTS, the WNS decreased for all values except the default as shown in Table 3.

Table 3: Timing report after CTS

Setup mode	all	reg2reg	default
WNS (ns)	7.560	7.560	8.254
TNS (ns)	0.000	0.000	0.000
Violating Paths	0	0	0
All Paths	52	50	21

WNS after routing decreases on all counts, and this can be seen in Table 4.

Table 4: Timing report after routing

Setup mode	all	reg2reg	default
WNS (ns)	7.529	7.529	8.234
TNS (ns)	0.000	0.000	0.000
Violating Paths	0	0	0
All Paths	52	50	21

The final timing report is run during the sign-off and the WNS had a small increase as seen in Table 5.

Table 5: Timing report during sign off

Setup mode	all	reg2reg	default
WNS (ns)	7.553	7.553	8.264
TNS (ns)	0.000	0.000	0.000
Violating Paths	0	0	0
All Paths	52	50	21

For all of the timing reports, we have a positive WNS, which is crucial for the layout and the functionality.

Additional validations were performed to confirm that the layout was entirely operational and error-free. The final DRC was executed with the ***verify_drc*** command, resulting in zero violations. The ***verifyGeometry*** command confirms that the geometry of the layout has been validated without any errors, as indicated by the result: 'Verification Complete: 0 Viols. 0 Wrngs.'

3 LEF

The updated LEF file is different from the one in Lab 4 as the pins are now centered for each of the four edges of the IO boundary. This was not a requirement in Lab 4 and the pins were more or less randomly placed closer to the corners of the boundary, as this still fulfilled the requirement of pin spacing. The area is also larger (4510 μm^2 vs 3172 μm^2), mainly because we have now added the IO boundary with a certain distance from the core.