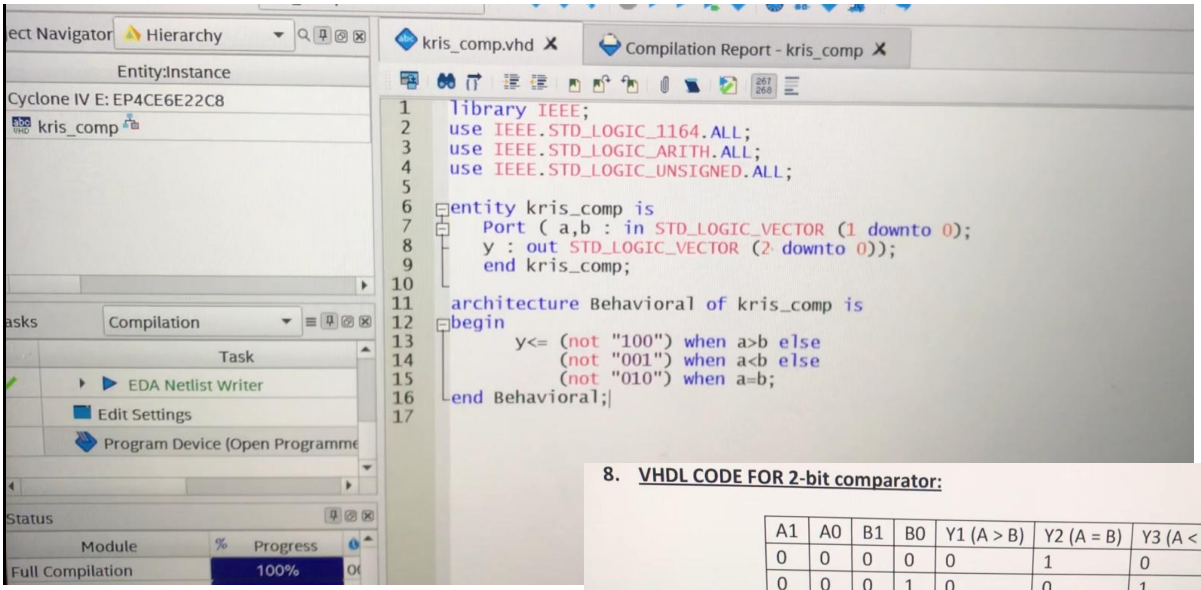
Kris M. Vallozo
BSCpE- 3A

2BIT COMPARATOR

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity kris_comp is
   Port ( a, b : in  STD_LOGIC_VECTOR (1 downto 0);
       y : out STD_LOGIC_VECTOR (2 downto 0));
end kris_comp;

architecture Behavioral of kris_comp is
begin
          y <= (not “100”) when a>b else
                (not “001”) when a<b else
                (not “010”) when a=b;
end Behavioral;
```



8. **VHDL CODE FOR 2-bit comparator:**

A1	A0	B1	B0	Y1 (A > B)	Y2 (A = B)	Y3 (A < B)
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0