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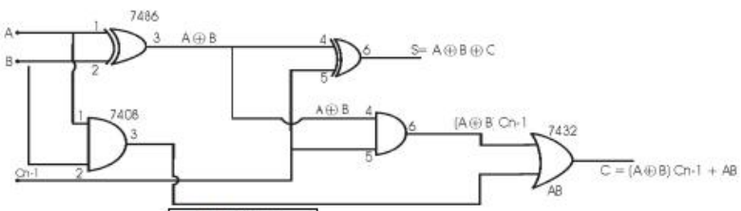
BSCpE - 3A

LABORATORY 8

1. VHDL CODE FOR FULL ADDER DATA FLOW:



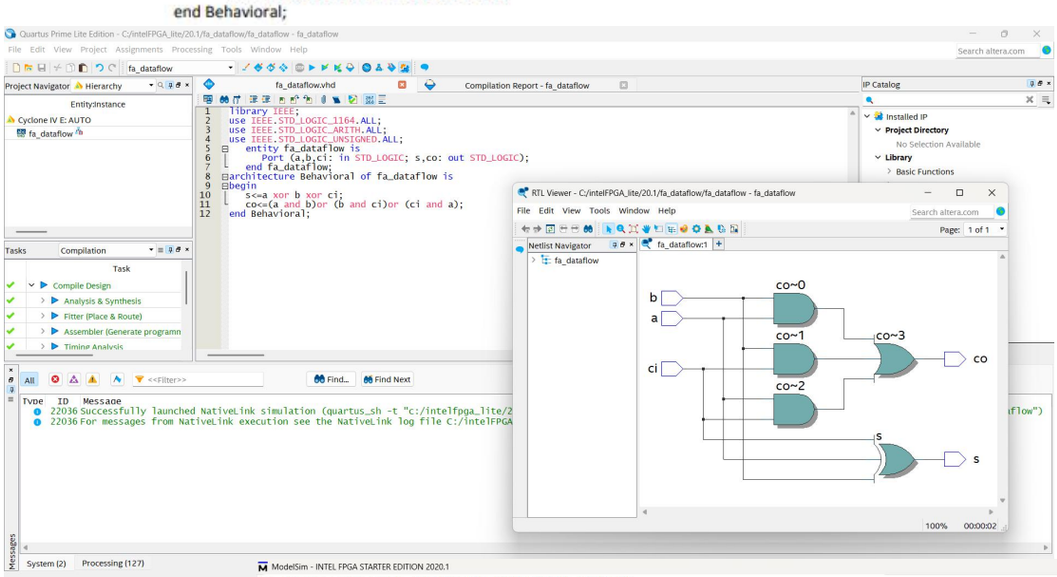
Full Adder				
A	B	Ci	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

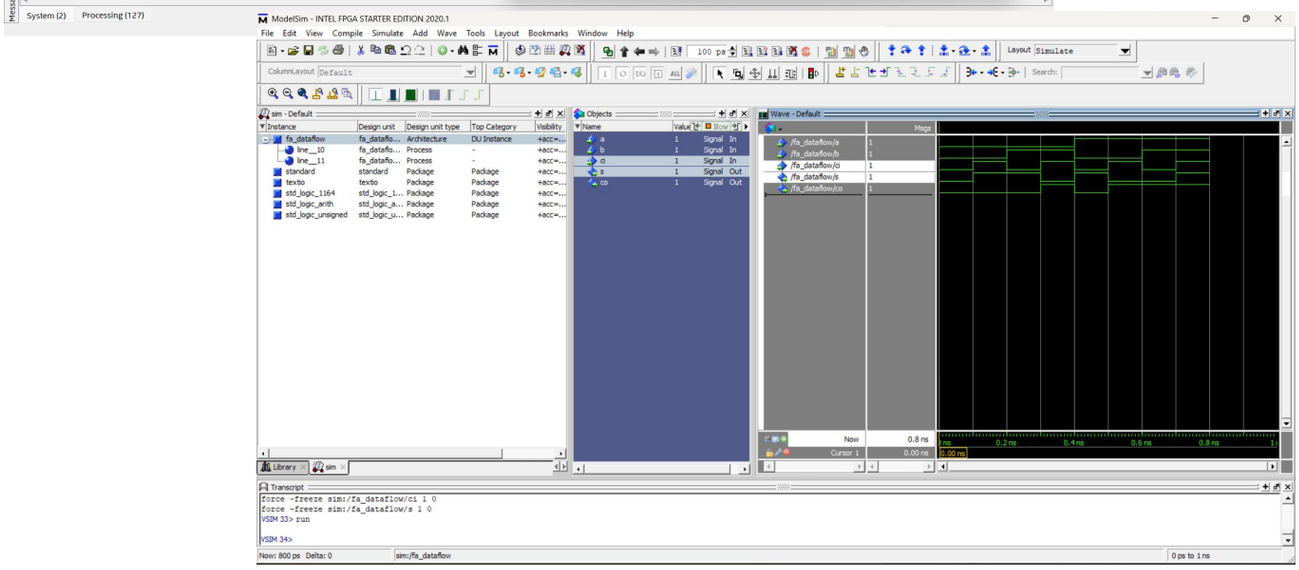
EXPRESSIONS:

$S = A \oplus B \oplus Ci$

$CO = (A \oplus B)Ci + AB$

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
        entity fa1 is
          Port ( a,b,ci : in  STD_LOGIC; s,co : out  STD_LOGIC);
        end fa1;
architecture Behavioral of fa1 is
begin
        s<=a xor b xor ci;
        co<=(a and b)or (b and ci)or (ci and a);
end Behavioral;
```





VHDL CODE FOR FULL ADDER BEHAVIORAL:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
        entity fa1 is
          Port ( a,b,ci : in  STD_LOGIC; s,co : out  STD_LOGIC);
        end fa1;
architecture Behavioral of fa1 is
begin
        process(a,b,ci)
begin
        s<=a xor b xor ci;
        co<=(a and b)or (b and ci)or (ci and a);
end process;
end Behavioral;
```