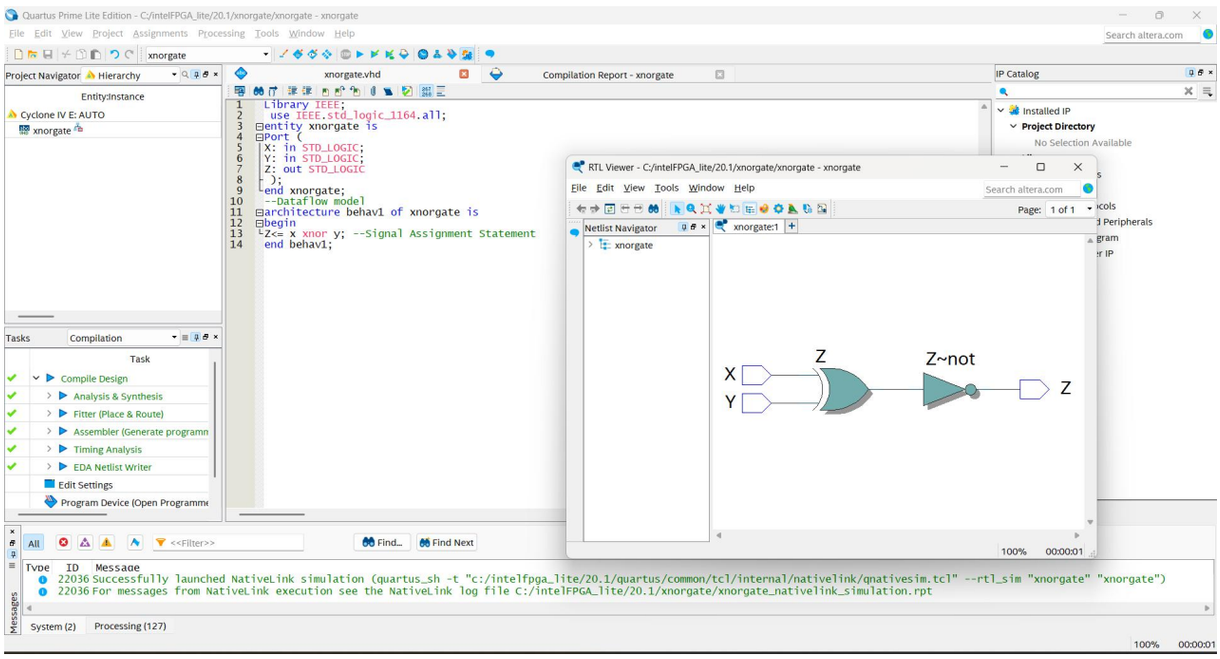
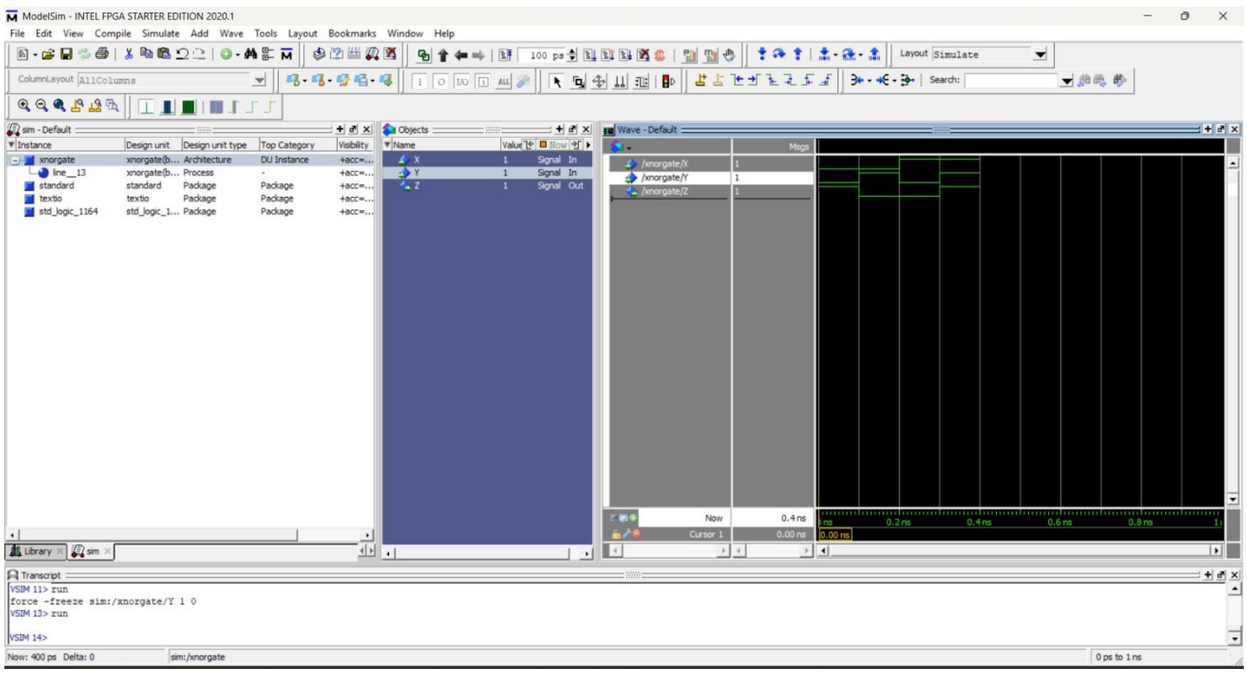
Kris M. Vallozo

BSCpE - 3A

LABORATORY 7 : EX-NOR GATE



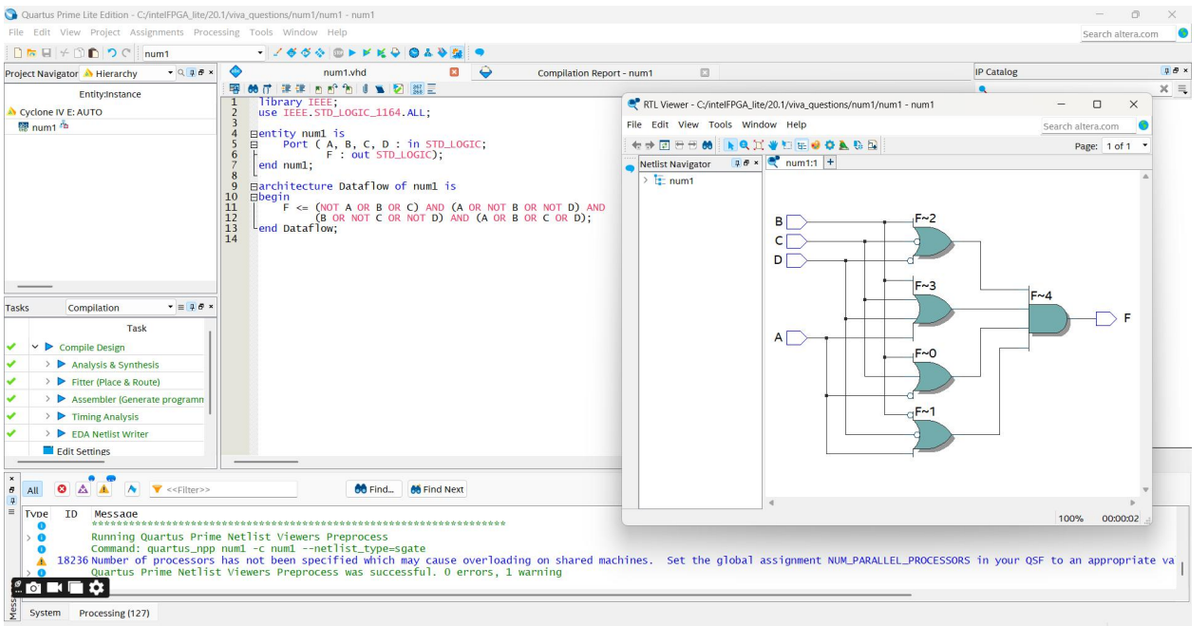


VIVA QUESTIONS:

1. Implement the following function using VHDL coding. (Try to minimize if you can).

$$F(A,B,C,D)=(A'+B+C)\ .\ (A+B'+D').\ (B+C'+D')\ .\ (A+B+C+D)$$

Answer:



2. What will be the no. of rows in the truth table of N variables?

Answer: The number of rows in a truth table of **N variables** is:

$$2^N$$

For example:

- If **N = 3**, then **8 rows** ($2^3 = 8$).
- If **N = 4**, then **16 rows** ($2^4 = 16$).

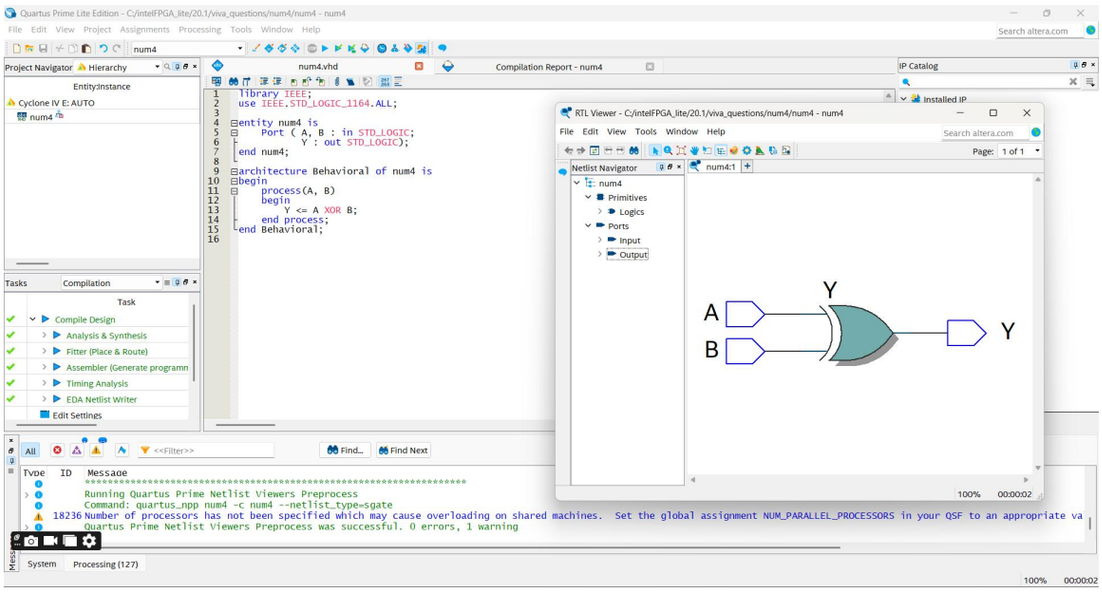
3. What are the advantages of VHDL?

Answer:

The advantages of VHDL include its ability to describe digital circuits in a structured, reusable, and technology-independent manner. It supports concurrent execution, making it ideal for modeling real hardware behavior. With strong simulation and verification capabilities, VHDL helps detect errors early, reducing costly rework. Its modularity and flexibility make it a preferred choice for FPGA and ASIC development.

4. Design Ex-OR gate using behavioral model?

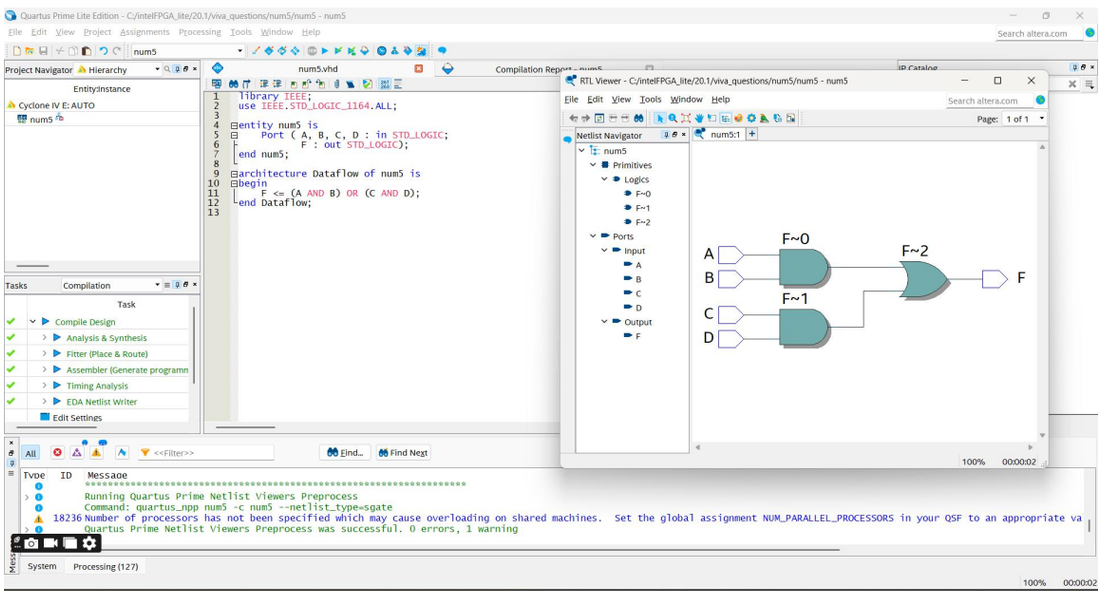
Answer:



5. Implement the following function using VHDL code

f=AB+CD.

Answer:



5. What are the differences between half adder and full adder?

Answer:

The differences between half adder and full adder lie in their functionality and inputs. A half adder adds two binary inputs (A and B) and produces a sum and a carry but does not handle carry input from a previous stage. In contrast, a full adder adds three inputs (A, B, and carry-in), making it suitable for multi-bit addition by considering carry propagation. This makes the full adder essential for building complex arithmetic circuits, whereas the half adder is limited to basic addition operations.

6. What are the advantages of minimizing the logical expressions?

Answer:

The advantages of minimizing the logical expressions are reduced hardware complexity, lower power consumption, and faster circuit operation. Simplified expressions require fewer gates, which decreases cost and improves efficiency. Additionally, minimized logic reduces propagation delay, enhancing the overall performance of digital circuits. This optimization is crucial in FPGA and ASIC design, where space and speed are essential.

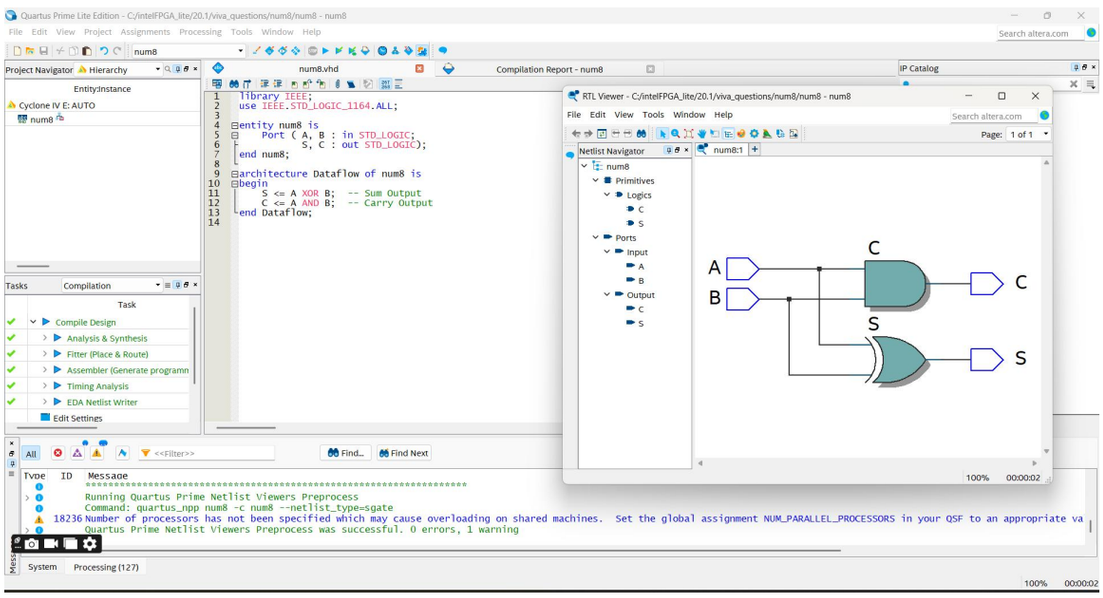
7. What does a combinational circuit mean?

Answer:

A combinational circuit is a type of digital circuit where the output depends only on the current input values and not on past inputs or memory. It consists of logic gates like AND, OR, and XOR, which perform operations based on Boolean algebra. Common examples include adders, multiplexers, and encoders. Since there is no feedback or storage, combinational circuits operate instantly, making them essential for fast computations in digital systems.

8. Implement the half adder using VHDL code?

Answer:



10. Implement the full adder using two half adders and write VHDL program in structural model?

Answer:

```
-- Include necessary IEEE library
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
```

```
-- Half Adder Entity
entity HalfAdder is
    Port ( A, B : in STD_LOGIC;
           S, C : out STD_LOGIC);
end HalfAdder;

architecture Dataflow of HalfAdder is
begin
    S <= A XOR B;  -- Sum Output
    C <= A AND B;  -- Carry Output
end Dataflow;

-- Full Adder Entity Using Two Half Adders
entity FullAdder is
    Port ( A, B, Ci : in STD_LOGIC;
           S, Co : out STD_LOGIC);
end FullAdder;

architecture Structural of FullAdder is
    -- Declare signals to connect components
    signal S1, C1, C2 : STD_LOGIC;

    -- Declare Half Adder Component
    component HalfAdder
        Port ( A, B : in STD_LOGIC;
               S, C : out STD_LOGIC);
    end component;

begin
    -- First Half Adder
    HA1: HalfAdder port map (A => A, B => B, S => S1, C => C1);
    -- Second Half Adder
    HA2: HalfAdder port map (A => S1, B => Ci, S => S, C => C2);

    -- OR Gate for Carry Out
    Co <= C1 OR C2;
end Structural;
```