DC MOTOR INTERFACE

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library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.NUMERIC STD.ALL;
entity DC MOTOR INTERFACE
Port (
  clk
        : in STD LOGIC;
  reset n: in STD LOGIC;
  start n : in STD LOGIC;
  dir n : in STD_LOGIC;
  pwm n : out STD LOGIC;
  motor n : out STD LOGIC VECTOR(1 downto 0);
    stat led n: out STD LOGIC
end DC MOTOR INTERFACE;
architecture Behavioral of DC MOTOR INTERFACE is
  signal pwm cnt : unsigned(7 downto 0) := (others \Rightarrow '0');
  signal clk div : unsigned(18 downto 0) := (others => '0');
  signal pwm clk : STD LOGIC := '0';
  signal enabled : STD LOGIC := '0';
  signal direction: STD LOGIC:='0';
begin
    process(clk)
  begin
    if rising edge(clk) then
      clk div \le clk div + 1;
      pwm clk \le clk \ div(18);
    end if;
  end process;
  process(pwm clk, reset n)
  begin
    if reset n = 0 then
      pwm cnt \leq (others \Rightarrow '0');
      pwm n \le '1';
    elsif rising edge(pwm clk) then
      pwm cnt \leq pwm cnt + 1;
      if enabled = '1' and pwm cnt < 128 then
         pwm n \le 0';
      else
         pwm n \le 11;
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end if;
     end if;
  end process;
  process(clk, reset_n)
  begin
     if reset_n = '0' then
        motor n \le "11";
        enabled \leq '0';
        direction <= '0';
     elsif rising edge(clk) then
        enabled <= not start n;</pre>
        direction <= not dir_n;</pre>
        if enabled = '1' then
          motor_n <= not (direction & not direction);</pre>
          motor_n <= "11";
        end if;
     end if;
  end process;
  stat_led_n <= not enabled;</pre>
end Behavioral;
```

