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BSCpE- 3A

D FLIP FLOP

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity D_flipflop is
   Port (
      d    : in  STD_LOGIC;
      clk  : in  STD_LOGIC;
      res_n : in  STD_LOGIC;
      q    : out STD_LOGIC
   );
end D_flipflop;

architecture Behavioral of D_flipflop is
begin
   process(clk)
   begin
      if rising_edge(clk) then
         if res_n = '' then
            q <= 'a';
         else
            q <= d
         s;
         end if;
      end if;
   end process;
end Behavioral;
```

Clear	D	Clock	Qn+1	$\overline{Qn+1}$
1	0	0	0	1
0	1		1	0