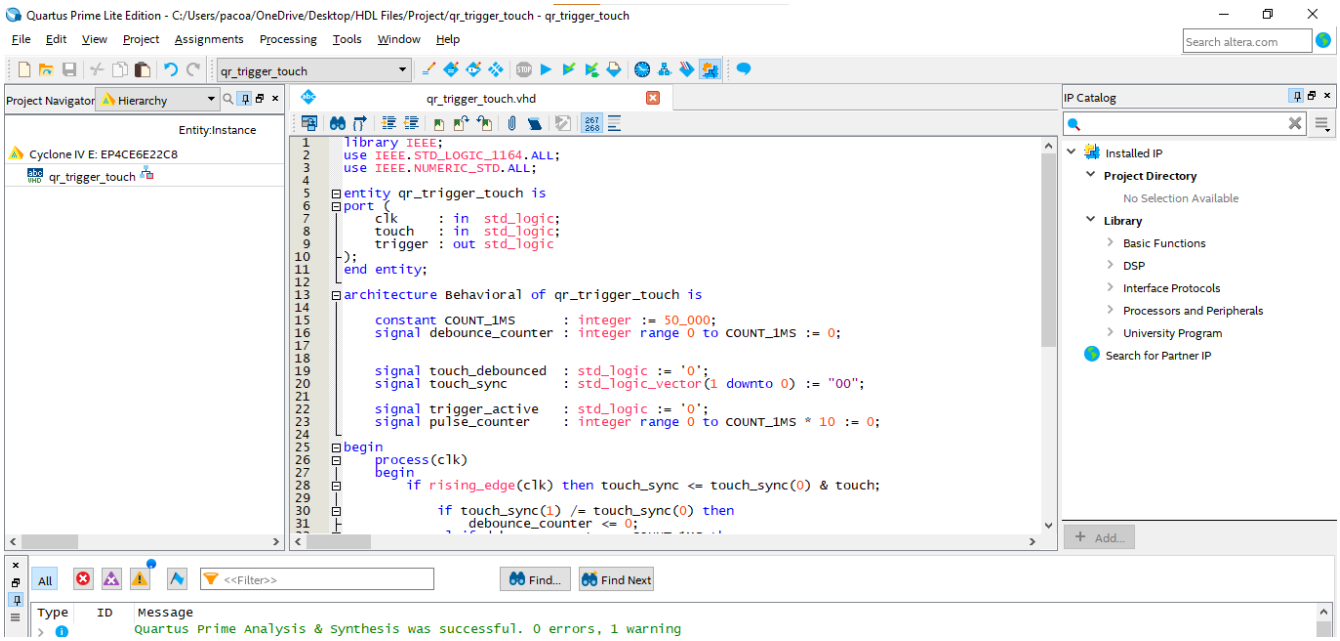
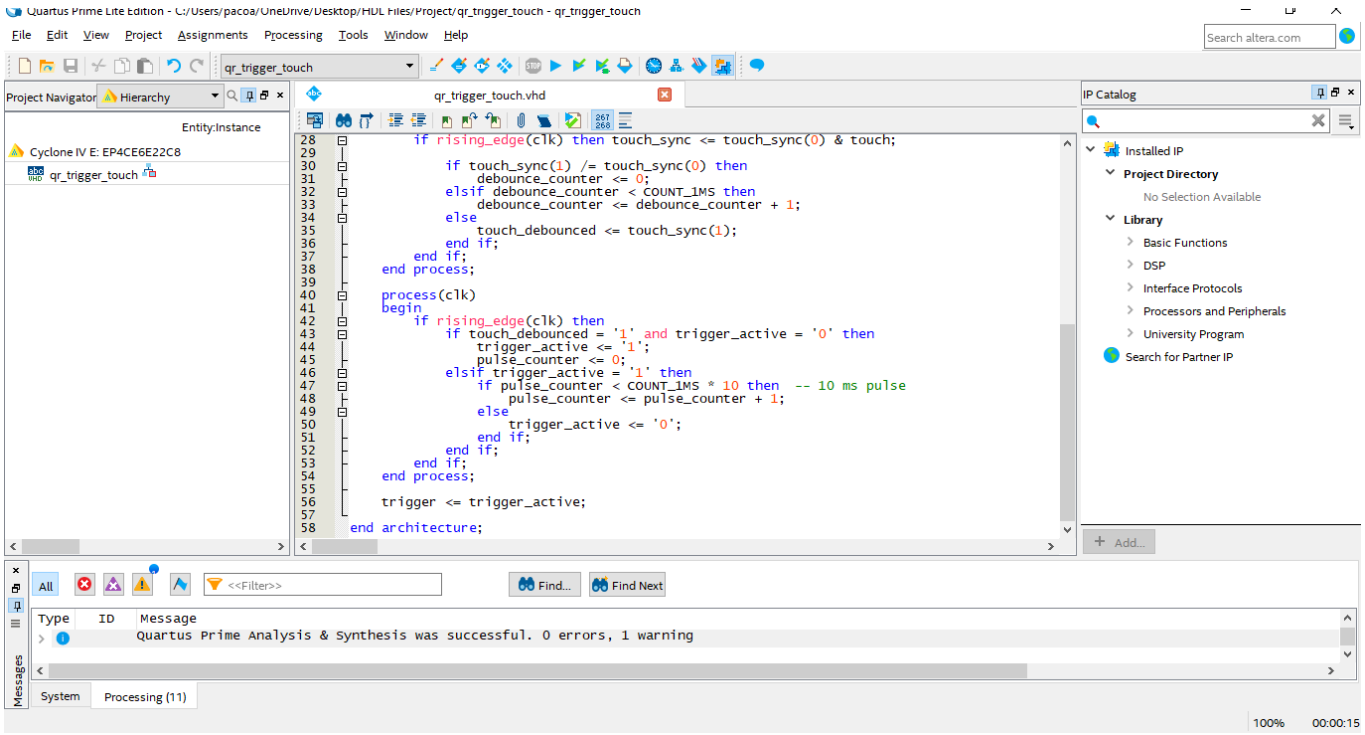
VHDL CODE:


Quartus Prime Lite Edition - C:/Users/pacoa/OneDrive/Desktop/HDL Files/Project/qr_trigger_touch - qr_trigger_touch
File Edit View Project Assignments Processing Tools Window Help
qr_trigger_touch
Project Navigator Hierarchy
Entity:Instance
Cyclone IV E: EP4CE6E22C8
qr_trigger_touch
qr_trigger_touch.vhd
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.NUMERIC_STD.ALL;
4
5 entity qr_trigger_touch is
6 port (
7 clk : in std_logic;
8 touch : in std_logic;
9 trigger : out std_logic
10);
11 end entity;
12
13 architecture Behavioral of qr_trigger_touch is
14
15 constant COUNT_1MS : integer := 50_000;
16 signal debounce_counter : integer range 0 to COUNT_1MS := 0;
17
18
19 signal touch_debounced : std_logic := '0';
20 signal touch_sync : std_logic_vector(1 downto 0) := "00";
21
22 signal trigger_active : std_logic := '0';
23 signal pulse_counter : integer range 0 to COUNT_1MS * 10 := 0;
24
25 begin
26 process(clk)
27 begin
28 if rising_edge(clk) then touch_sync <= touch_sync(0) & touch;
29
30 if touch_sync(1) /= touch_sync(0) then
31 debounce_counter <= 0;
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
University Program
Search for Partner IP
Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
Quartus Prime Analysis & Synthesis was successful. 0 errors, 1 warning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qr_trigger_touch
Project Navigator Hierarchy
Entity:Instance
Cyclone IV E: EP4CE6E22C8
qr_trigger_touch
qr_trigger_touch.vhd
28 if rising_edge(clk) then touch_sync <= touch_sync(0) & touch;
29
30 if touch_sync(1) /= touch_sync(0) then
31 debounce_counter <= 0;
32 elsif debounce_counter < COUNT_1MS then
33 debounce_counter <= debounce_counter + 1;
34 else
35 touch_debounced <= touch_sync(1);
36 end if;
37 end if;
38 end process;
39
40 process(clk)
41 begin
42 if rising_edge(clk) then
43 if touch_debounced = '1' and trigger_active = '0' then
44 trigger_active <= '1';
45 pulse_counter <= 0;
46 elsif trigger_active = '1' then
47 if pulse_counter < COUNT_1MS * 10 then -- 10 ms pulse
48 pulse_counter <= pulse_counter + 1;
49 else
50 trigger_active <= '0';
51 end if;
52 end if;
53 end if;
54 end process;
55
56 trigger <= trigger_active;
57
58 end architecture;
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
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Search for Partner IP
Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
Quartus Prime Analysis & Synthesis was successful. 0 errors, 1 warning
Messages
System
Processing (11)
100%
00:00:15