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U19CS076

CO_QUIZ

1. 1's complement of 11010
is
00101

d. 00101

2. Yes, ~~#~~ the 2s complement is adding 1 to 1s complement

a. TRUE

3 Booth's Algorithm is applied only on signed and unsigned binary numbers.

b. binary numbers

4. ~~a~~. Booth's Algorithm multiplies binary numbers (signed & unsigned).

b. Booth's Algorithm

5. It is denoted by Q (multiplier)
22 is multiplicand. and 3 is Q

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d. Multiplier

6. $(-2)*(-3)$

$M = (-2)_{10} = (1110)_2$

$-M = 0010$

$Q = (1101)_2$

count	AC	Q_0	Q_{-1}	Operation
4	0000	1101	0	AC→AC-M
	0010	1101	0	ASR
	0001	0110	1	
3	0001	0110	1	AC→AC+M
				0001
				+ 1110
	1111	0110	1	ASR
	1111	1011	0	
2.	0001	1011	0	AC→AC-M
				1111
				0010
				0001
	0000	1101	1	ASR

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ASR

1. 0000	1101	1	
0000	0110	1	

$n-1=0 \rightarrow$ end

since MSB→0

$(000001100) = \underline{+6}$

$-2 * -3 = 6$

option A)

0111
1000

A) 6

$(-7)*3$

(7)

$M = -7 = 2^s$ comp of $(0111)_2$

$= (11001)_2$

$-M = (00111)_2$

$Q = (00011)_2$

$n = 5$

(0001 0100)

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count	AC	Q_0	Q_{-1}	Operation
5	00000	00011	0	AC → AC-M
	00111	00011	0	ASR ~~Right~~
	00011	10001	1	
4	00011	10001	1	ASR
	00001	11000	1	
3	00001	11000	1	AC → AC+M 00001 +11001 11010
	11010	11000	1	
	11~~0~~101	01100	0	ASR
2	1110~~0~~1	01100	0	ASR
1	11110	10110	0	

0 → END

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① 1110 1011

Since its 1 we have to take 2s compliment

$(00001\,0100)_2$

$+ \quad 1$

$(00001\,0101)_2$

$= 16 + 4 + 1 = 21$

Since MSB it was 1 signed bit

$(-7) * (3) = -21$

c) -21

⑧

Arithmetic shift	logical shift
signed bit is preserved	signed bit is ignored
In left shift, 0s are shifted to left keeping sign bit	0s replaced by discarded bits

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In right shift, sign bit is kept as it is	In right logical shift, inserts value 0 to shifted bit.
Used for signed interpretation	Used for unsigned interpretation
Eficient to perform multiplication and division by left shift and right shift of n bits respectively using power of 2.	Just performs multiplication by left shift.
Eg: 1100 as right shift 1 is signed bit 1100 1110	Eg:- 1100 no signed bit 1100 0110

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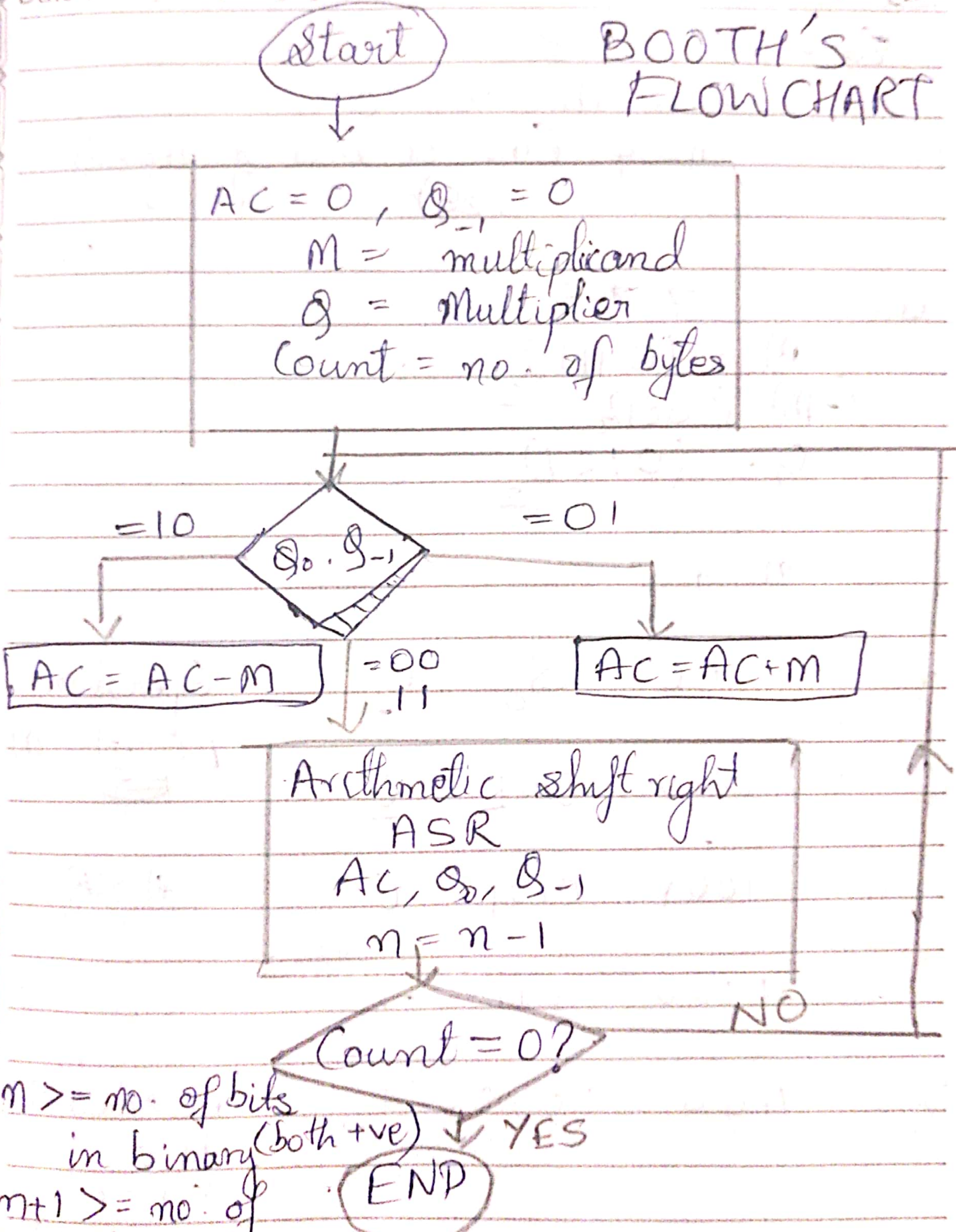
BOOTH'S FLOWCHART



n >= no. of bits in binary (both +ve)

n+1 >= no. of bits in binary (one −ve)

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Eg:- $7 * 3$

7 is M 3 is Q

$n = 4$ (no. of bits of register size)

1000

(10) a. $7 * 5$

$M = (0111)_2$

$(-M) = (1001)_2$

$Q = (0101)_2$

$n = 4$

n	AC	Q_0	Q_{-1}	Operation
4	0000	0101	0	AC→AC−M
	1001	0101	0	ASR
	1100	1010	1	
3.	1100	1010	1	AC→AC+M 1100 0111
	0011	1010	1	Discarded Carrier

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	0001	1101	0	ASR
2.	0001	1101	0	AC ← AC−M 0001 1001 1010
	1010	1101	0	ASR
	1101	0110	1	
1.	1101	0110	1	AC ← AC+M 1101 0111 01000
	0100	0110	1	ASR
	0010.	0011	0	35

0 → END

$(00100011)_2 = 32+2+1$

$= \underline{\underline{35}}$

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b) $3 * (-6)$

$M = 00011$

$-M = 11101$

$Q = 11010$

$n = 5$ register bits

n	AC	Q_0	Q_{-1}	Operation
				ASR
5	00000	11010	0	
				AC→AC-M
4	00000	01101	0	
				ASR
	11101	01101	0	
				AC←AC+M
3	11110	10110	1	11110
				+ 00011
				00001
				ASR
	00001	10110	1	
	00000	11011	0	
				AC→AC-M
2	11101	11011	0	ASR
	11110	11101	1	
1	11111	01110	1	
0 → end				

1010

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$(1111110111 0)_2$ → $\underline{\underline{-ve}}$

Since M.S.B is 1

2s complement

00000 01 0001

1

$+$

$\boxed{(000000 1 0010)_2}$

$= -(16+2)$

$= \underline{\underline{-18}}$

(c). $(-2) * 4$

$M = (11110)_2$

$-M = (00010)_2$

$Q = (00100)_2$

n	AC	Q_0	Q_{-1}	Operation
				ASR
5	00000	00100	0	ASR
4	00000	00010	0	AC→AC−M
3.	00000	00001	0	ASR
	00010	00001	0	
	00001	0000	1	AC→AC+M ~~ASR~~
2.	00001	0000	1	
	+ 11110			

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		1	ASR
	00000	0	
11111	10000		ASR
11111	11000	0	
1. 11111			

0 → end

(11111 11000)

Since M.S.B is 1

2s complem

$$\begin{array}{r} 0000000111 \\ + \quad\quad 1 \\ \hline \boxed{(0000001000)_2} \end{array}$$

$= -8$

d) $(-5) * (-3)$

$M = (-5)_{10} = (1011)_2$

$-M = (5)_{10} = (0101)_2$

$Q = (-3)_{10} = (1101)_2$

n	AC	Q_0	Q_{-1}	Operation
4	0000	1101	0	AC→AC−M 0000 0101 ASR
	0101	1101	0	
	0010	1110	1	
3	0010	1110	1	AC→AC+M 0010 1011 ASR
	1101 ~~1010~~	1110	1	
	1110	1111	0	
2.	1110	1111	0	AC→AC−M 1110 0101 ASR
	0011	1111	0	
	0001	1111	1	ASR
1.	0000	1111	1	
0	→	END		

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$$(00001111)_2$$

$$= 8 + 4 + 2 + 1$$

$$= (15)_{10}$$

$$-5 * -3 = \underline{\underline{15}}$$

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