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The UART receiver buffer register (RBR) contains the oldest byte and therefore the next byte to be read in of the RX FIFO. The RBR is read only. Before reading the RBR, the line status register (LSR) should be read first as it contains status information including the parity error (PE), framing error (FE), and break interrupt (BI) bits for the byte sitting in the RBR. Once the RBR is read, the RBR will be set to the next byte in the FIFO and the status bits in the LSR will be updated. In order to read the RBR, the divisor latch access bit (DLAB) must be set to 0 to prevent access to the UART divisor latches (used for setting the baud rate).

The UART transmitter holding register (THR) contains the newest byte of the TX FIFO. The THR is write only. Writing a byte to the THR results in the byte being put in the TX FIFO. The byte will be sent after all bytes that were put into the FIFO before it are sent. The least significant bit of the byte is sent first. Like the RBR, in order to write to the THR, the divisor latch access bit (DLAB) must be set to 0 to prevent access to the UART divisor latches (used for setting the baud rate).