EC/EE/CS & IT/IN

Digital Electronics

Combinational Circuit

MULTIPLEXER

LECTURE NO. 4

Chandan Jha Sir (CJ Sir)

बिना संघर्ष कोई महान नही होता
बिना कुछ किये जय जय कार नही होता
जब तक नहीं पड़ती हथोड़े की चोट
तब तक कोई पत्थर भी
लोगों के लिए भगवान नही होता

ABOUT ME

- Cleared Gate Multiple times with double Digit Rank (AIR 23, AIR 26)
- Qualified ISRO Exam
- Mentored More then 1 Lakhs+ Students (Offline & Online)
- More then 250+ Motivational Seminar in various Engineering College including NITs & Some of IITs

Chandan Jha

DON'T CARE CONDITION

Sunday → Evening
6:00 PM.

Combination of inputs on which the output may or may not depends are called don't care condition.

Ex. 9. Find the minimized Boolean expression for the function given as

$$f(A, B, C) = \sum m(0, 2, 3, 4) + \sum d(1, 6, 7)$$

A \ BC	00	01	11	10
0	1	X	1	1
1	1		X	X

Ex. 10. Find the minimized Boolean expression for the function given as

$$f(A, B, C, D) = \sum m\,(0, 2, 4, 6, 7, 8, 10, 11, 12, 14, 15) + \sum d(1,3)$$

AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	1	X	X	1
$\bar{A}B$ 01	1		1	1
AB 11	1		1	1
$A\bar{B}$ 10	1		1	1

C

$\bar{D}$

$C + \bar{D}$

Ans

Ex. 11 Find the minimized Boolean expression for the function given as $f(A, B, C, D) = \sum m\,(0,3,6,7,9,14) + \sum d(1,4,5,11,13,15)$

$\bar{A}\bar{C}$

D

AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	1	X	1	
$\bar{A}B$ 01	X	X	1	1
AB 11		X	X	1
$A\bar{B}$ 10		1	X	

BC

$\bar{A}\bar{C} + BC + D$

Ans

POS FORM Question

Product of Sum

Ex. 12. Find the minimized Boolean expression for the function given as

$$f(A, B, C) = \underbrace{\pi M}_{\text{POS}}(0, 2, 3, 4, 6, 7)$$

Method ①

A \ BC	00 ($B+C$, $\bar{B}\bar{C}$)	01 ($B+\bar{C}$, $\bar{B}C$)	11 ($\bar{B}+\bar{C}$, BC)	10 ($\bar{B}+C$, $B\bar{C}$)
A | $\bar{A}$ | 0	0		0	0
$\bar{A}$ | A | 1	0		0	0

C $\quad$ $\bar{B}$

$\bar{B}\cdot C$

Method ②

A \ BC	00 ($\bar{B}\bar{C}$)	01 ($\bar{B}C$)	11 (BC)	10 ($B\bar{C}$)
$\bar{A}$ 0	0		0	0
A 1	0		0	0

$\bar{C}$ $\quad$ B

$$\bar{F} = \bar{C} + B$$

$$F = \overline{\bar{C}+B} = \bar{\bar{C}}\cdot\bar{B} = \bar{B}\cdot C \text{ Ans}$$

$$f(A,B,C) = \prod M(0,2,3,4,6,7) \longrightarrow \text{POS}$$

$$= \sum m(1,5)$$

A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	0	1	0	0
A 1	0	1	0	0

$\bar{B}C$

Ans

Ex. 13. Find the minimized Boolean expression for the function given as

$$f(A, B, C, D) = \pi M(0, 2, 3, 4, 7, 8, 10, 11, \underline{13}, \underline{14}, \underline{15})$$

$A+C+D$ $\quad$ $\bar{C}+\bar{D}$

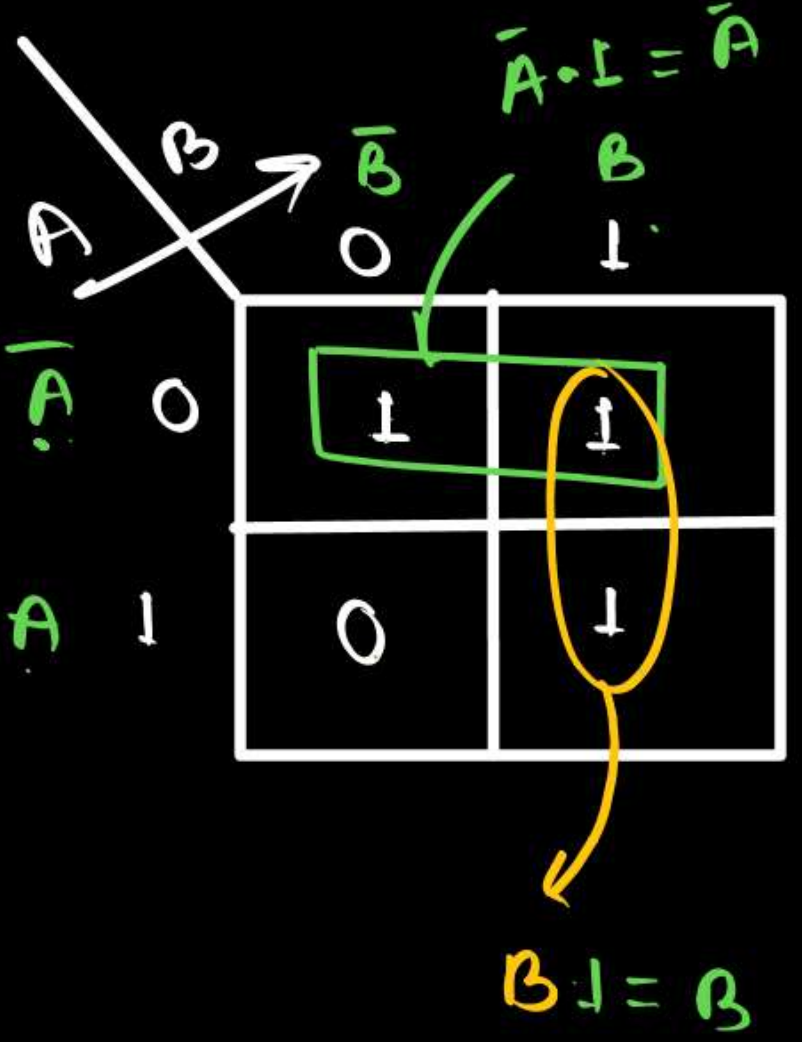
$AB \backslash CD$	$C+D$, $\bar{C}\bar{D}$, 00	$C+\bar{D}$, $\bar{C}D$, 01	$\bar{C}+\bar{D}$, CD, 11	$\bar{C}+D$, $C\bar{D}$, 10
$\bar{A}\bar{B}$ 00, $A+B$	0	1	0	0
$\bar{A}B$ 01, $A+\bar{B}$	0	1	0	1
AB 11, $\bar{A}+\bar{B}$	1	0	0	0
$A\bar{B}$ 10, $\bar{A}+B$	0	1	0	0

$B+D$ $\quad$ $\bar{A}+\bar{C}$ $\quad$ $\bar{A}+\bar{B}+\bar{D}$

POS

$$(\bar{A}+\bar{B}+\bar{D})\cdot(\bar{A}+\bar{C})\cdot(A+C+D)$$
$$(B+D)\cdot(\bar{C}+\bar{D})$$

SOP

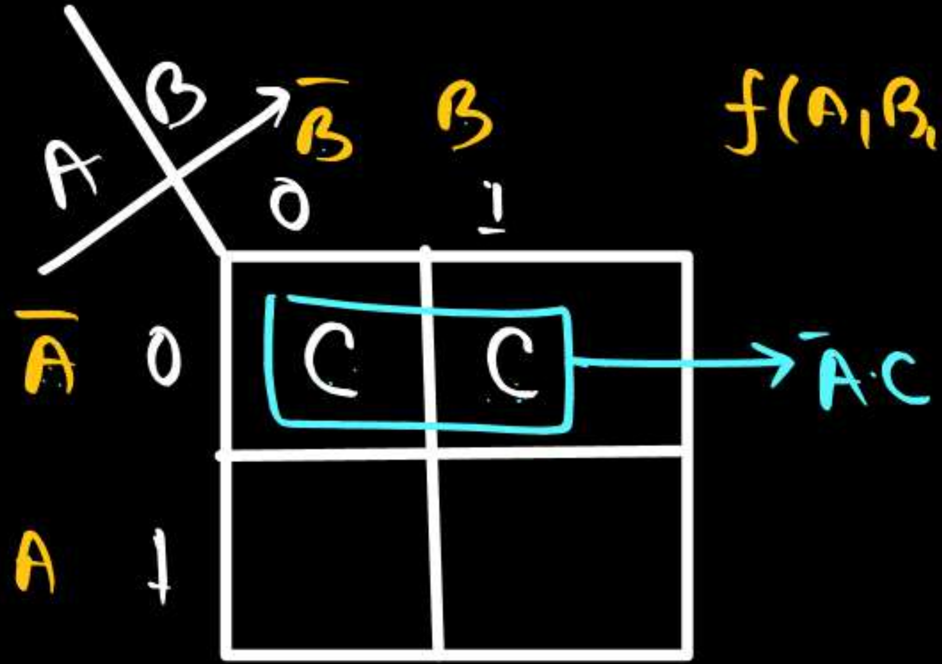


$$f(A,B) = \bar{A}\bar{B}\cdot 1 + \bar{A}B\cdot 1 + \cancel{A\bar{B}\cdot 0} + AB\cdot 1$$

$$= \Sigma m(0,1,3)$$

$\bar{A}+B$

Ex



$$f(A,B,C) = \bar{A}\bar{B}\cdot C + \bar{A}B\cdot C$$

$$= \bar{A}C(\bar{B}+B)$$

$$= \bar{A}C$$

$\bar{A}C$

Ans

$A \backslash BC$	$\bar B\bar C$ 00	$\bar B C$ 01	BC 11	$B\bar C$ 10
$\bar A$ 0	1	1		
A 1			$\bar D$	$\bar D$

↱ standard canonical

Q $f(A,B,C,D) = \bar A\bar B\bar C\cdot 1 + \bar A\bar B C\cdot 1 + ABCD + AB\bar C\bar D$

$$f(A,B,C,D) = \bar A\bar B\bar C(\bar D+D) + \bar A\bar B C(\bar D+D) + ABCD + AB\bar C D$$

$$= \overset{0000}{\bar A\bar B\bar C\bar D} + \overset{0001}{\bar A\bar B\bar C D} + \overset{0010}{\bar A\bar B C\bar D} + \overset{0011}{\bar A\bar B C D} + ABCD + \overset{1101}{AB\bar C D}$$

$$= \Sigma m(0,1,2,3,13,15)$$

$f(A,B,C,D) = \sum m(0,1,2,3,13,15)$

$AB \backslash CD$	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10	
$\bar{A}\bar{B}$ 00	1	1	1	1	$\rightarrow \bar{A}\bar{B}$
$\bar{A}B$ 01					
AB 11		1	1		$\rightarrow ABD$
$A\bar{B}$ 10					

$$= \bar{A}\bar{B} + ABD$$

Ans

Q $f(A,B,C,D) = \bar{A}\bar{B}\bar{C}\cdot 1 + \bar{A}\bar{B}C\cdot 1 + ABCD + ABC\bar{D}$

3 Variable

A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	1	1		
A 1			D	D

$\bar{A}\bar{B}\cdot 1$

$\rightarrow ABD$

$\bar{A}\bar{B} + ABD$

Ans

Implicants , Prime Implicants, Essential Prime Implicants

$= \Sigma m(0, 1, 3, 6, 7)$

Ex $f(A,B,C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + AB\bar{C} + ABC$

A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	1	1	1	
A 1			1	1

$= \bar{A}\bar{B} + AB + \bar{A}C$ ✓

A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	1	1	1	
A 1			1	1

$= \bar{A}\bar{B} + AB + BC$ ✓

Implicants = 5

Prime Implicants = 4

Essential prime Implicants = 2

Ex

$A \backslash BC$	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	1	1		1
A 1		1	1	1

$= \bar{A}\bar{B} + B\bar{C} + AC$ ✓

$A \backslash BC$	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	1	1		1
A 1		1	1	1

$= \bar{A}\bar{C} + \bar{B}C + AB$ ✓

Implicants = 6

Prime Implicants = 6

EPI = 0

Ex

$= \bar{A}\bar{C}D + \bar{A}BC + AB\bar{C} + ACD$

RPI

AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00		1		
$\bar{A}B$ 01		1	1	1
AB 11	1	1	1	
$A\bar{B}$ 10			1	

I = 8

PI = 5

EPI = 4

RPI = 1

AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	1	1		
$\bar{A}B$ 01		1	1	
AB 11			1	1
$A\bar{B}$ 10				1

$I = 7$

$PI = 6$

$EPI = 2$


Mountain Dew
Darr
ke aage
jeet
hai

Designing of Combinational Circuit

Step 1. Find the number of inputs & output

Step 2. Write the truth table.

Step 3. Write the logical Expression.

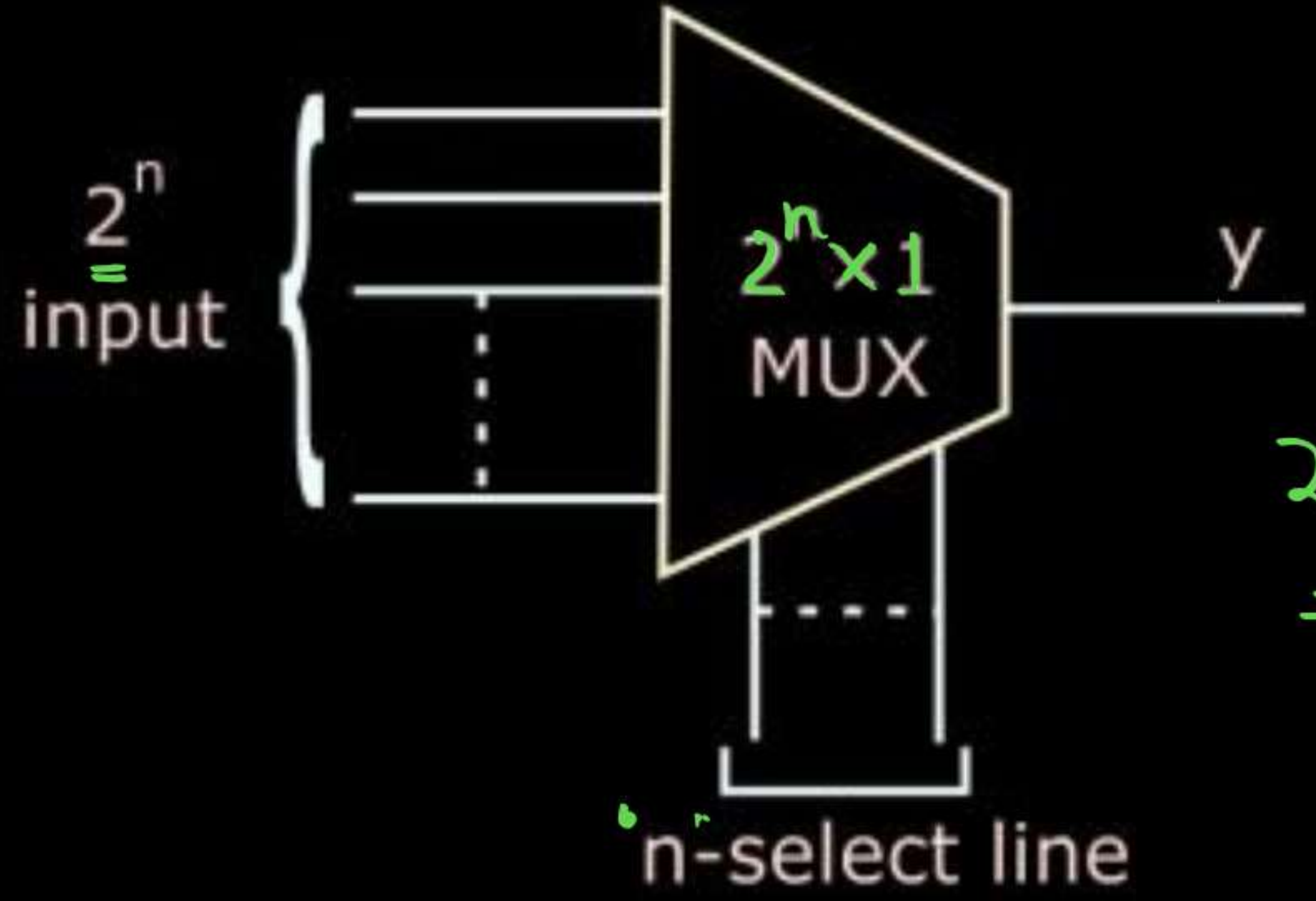
Step 4. Minimize the logical Expression.

Step 5. Hardware Implementation.

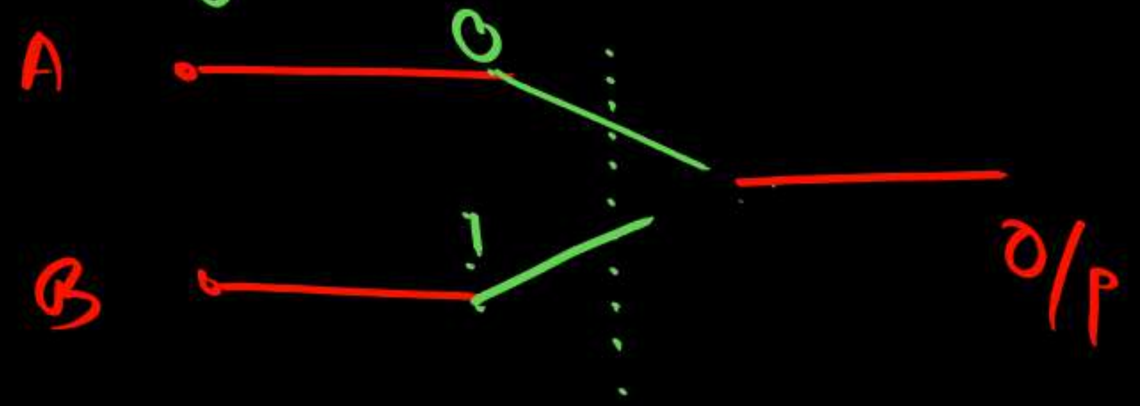
MULTIPLEXER

→ MUX → universal logic ✓

→ MUX → AND-OR Logic ✓



$2^n \longrightarrow 1$



Select line

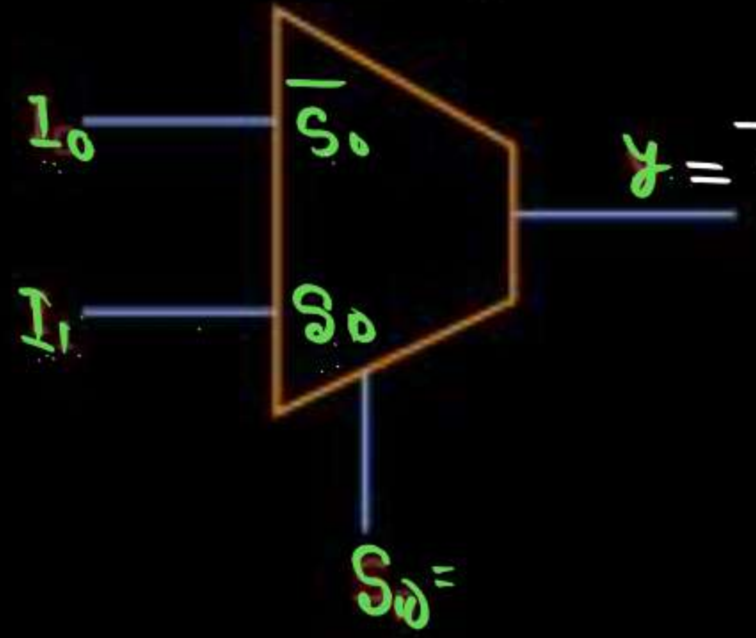
$x = 0, 1$

2

Ex. 1. Design a 2 x 1 MUX?

$$y = \overline{S_0} I_0 + S_0 I_1$$

Step-1. Number of input 2 outputs



$$y = \overline{S_0} I_0 + S_0 I_1$$

Step 2. Truth table.

S_0	Y
0	I_0
1	I_1

Step 3. Logical expression

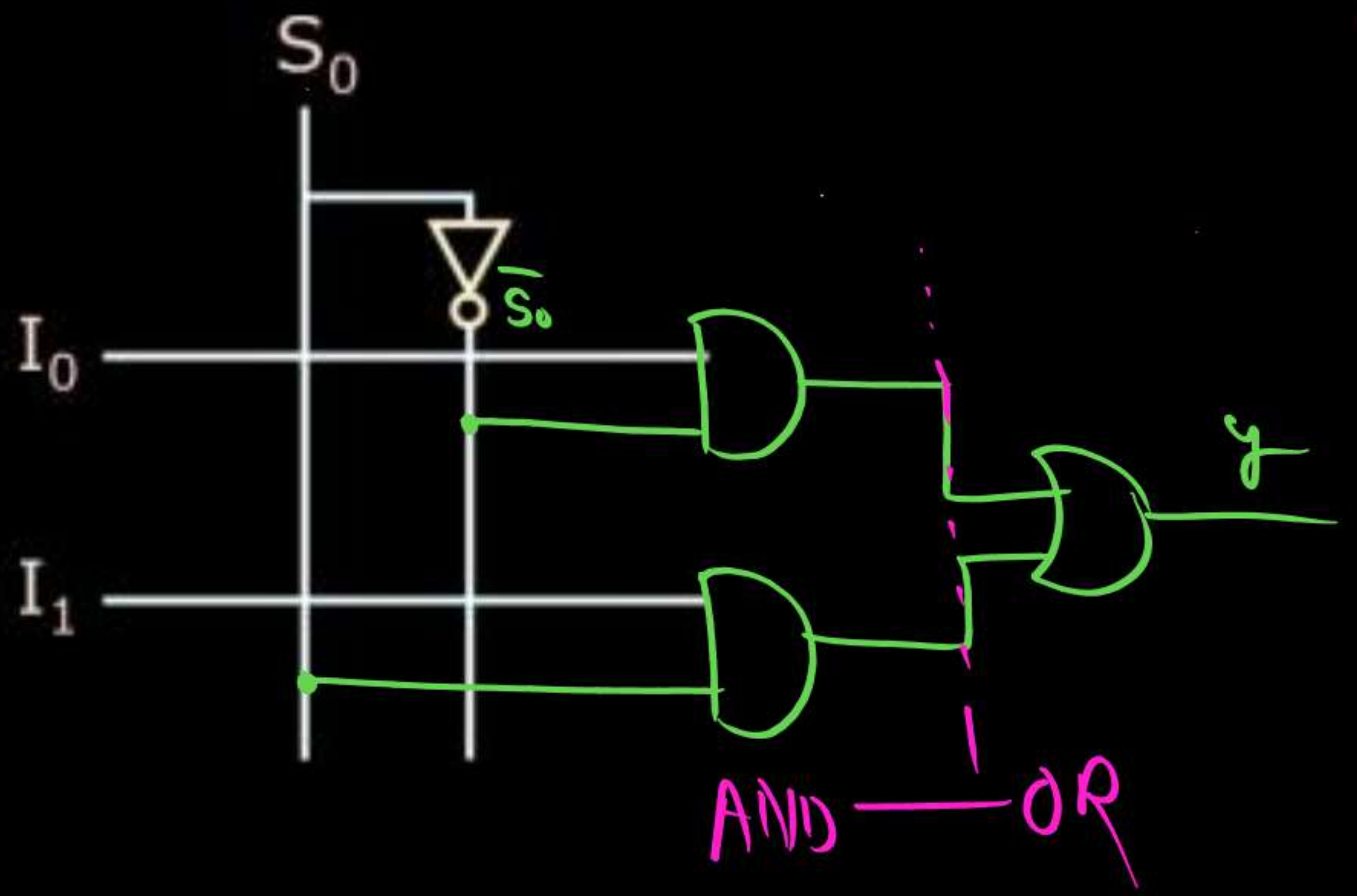
$$y = \bar{S_0} I_0 + S_0 I_1$$

Step 4. Minimization $\longrightarrow$ SOP

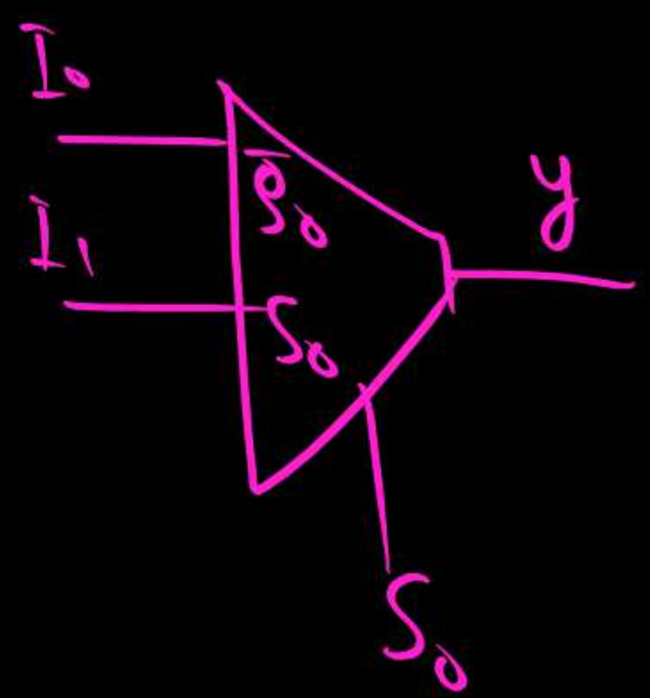
Step 5. Hardware implementation

MUX $\longrightarrow$ AND-OR Logic

De-MUX $\longrightarrow$ AND Logic



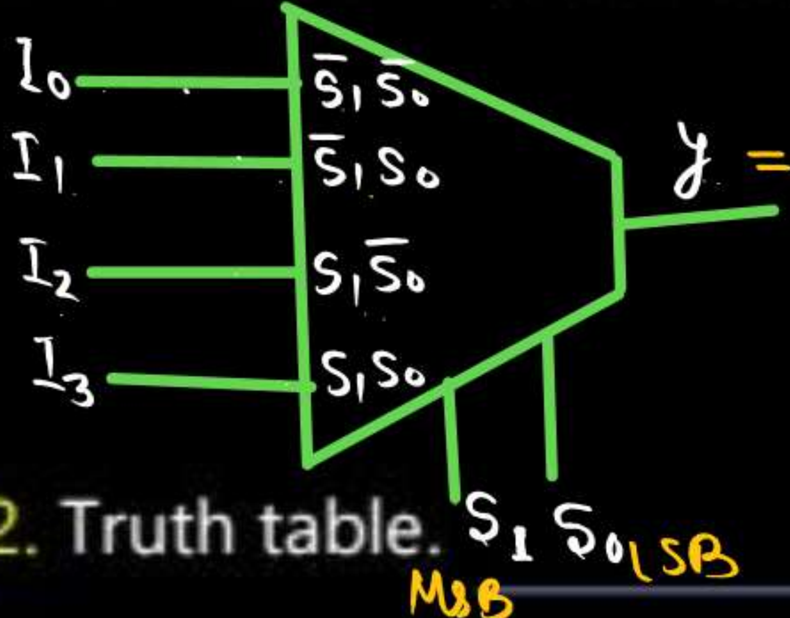
?



Ex. 2. Design a 4x1 MUX?

8

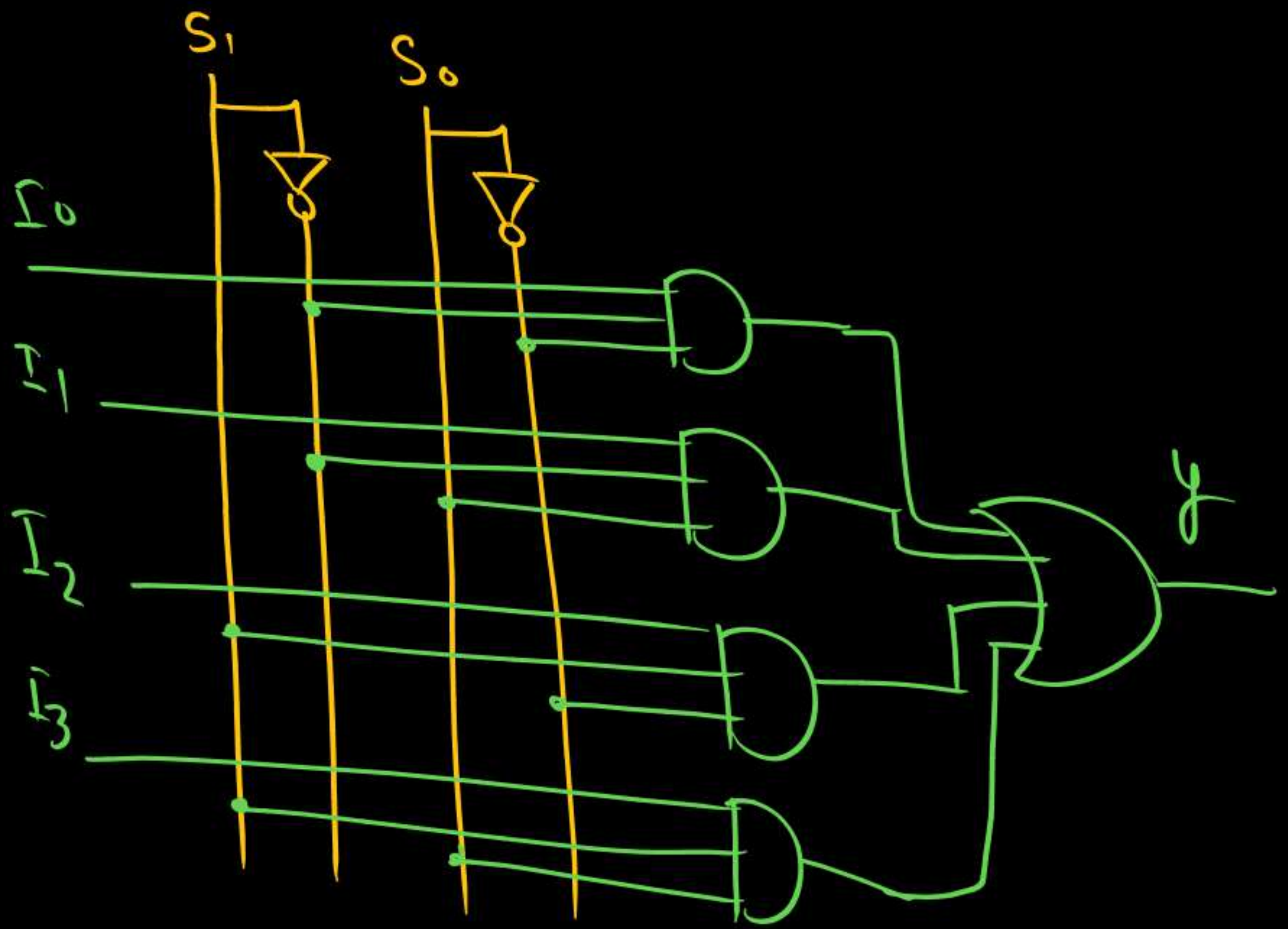
Step-1. Number of input & outputs



$$y = \bar{S}_1\bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1\bar{S}_0 I_2 + S_1 S_0 I_3$$

Step 2. Truth table.

S1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



Step 3. Logical expression

Step 4. Minimization

Step 5. Hardware implementation

Design a $\boxed{8 \times 1 \text{ MUX}}$

TYPE -1 Designing of higher order MUX by using lower order MUX

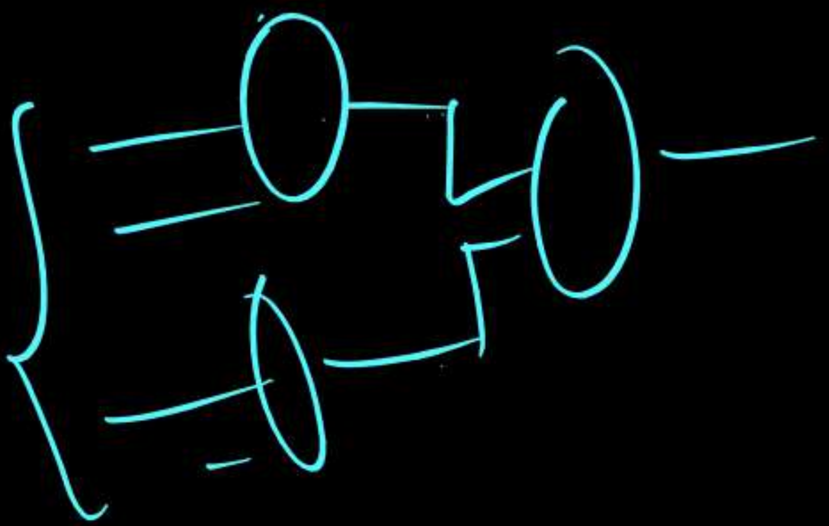
$\frac{4}{2} + \frac{2}{2}$

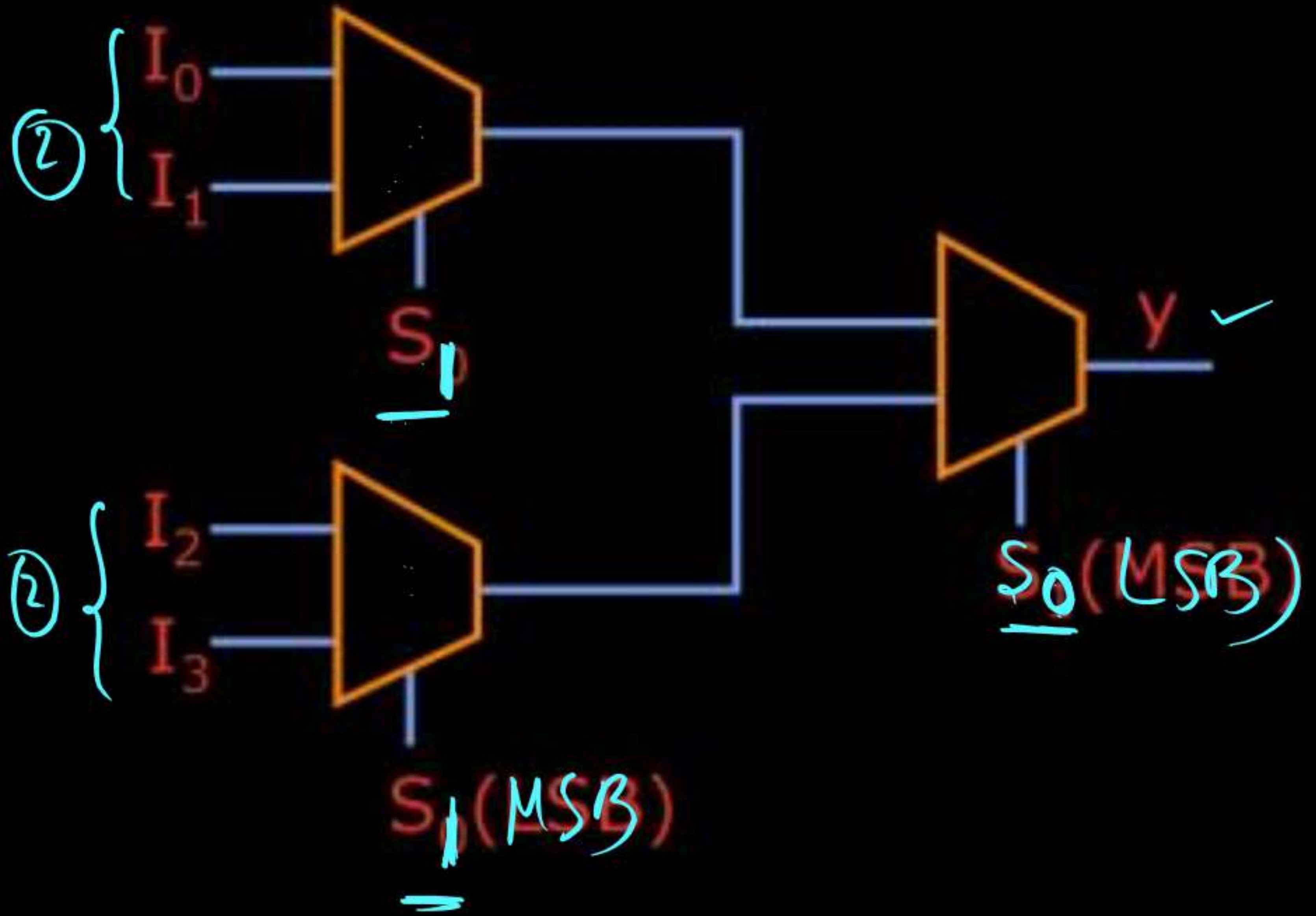
Ex. 1. 2x1 MUX ----------------------------→ 4x1 MUX

$2 + 1 = 3$

2 inputs

4 inputs





$$\frac{4}{2} + \frac{2}{2}$$

$$2\times1 \longrightarrow 4\times1$$

$2+1$

1 line

2 select line

Ex. 2. 2x1 MUX $\xrightarrow[4+2+1=7]{\frac{8}{2}+\frac{4}{2}+\frac{2}{2}}$ 8x1 MUX

Ex. 3. 2x1 MUX $\xrightarrow[8+4+2+1=15]{\frac{16}{2}+\frac{8}{2}+\frac{4}{2}+\frac{2}{2}}$ 16x1 MUX

2x1 MUX $\xrightarrow{2^n-1}$ 2^nx1 MUX

Ex. 3. 4 x 1 MUX --→ 16 x 1 MUX

$$\frac{16}{4} + \frac{4}{4}$$

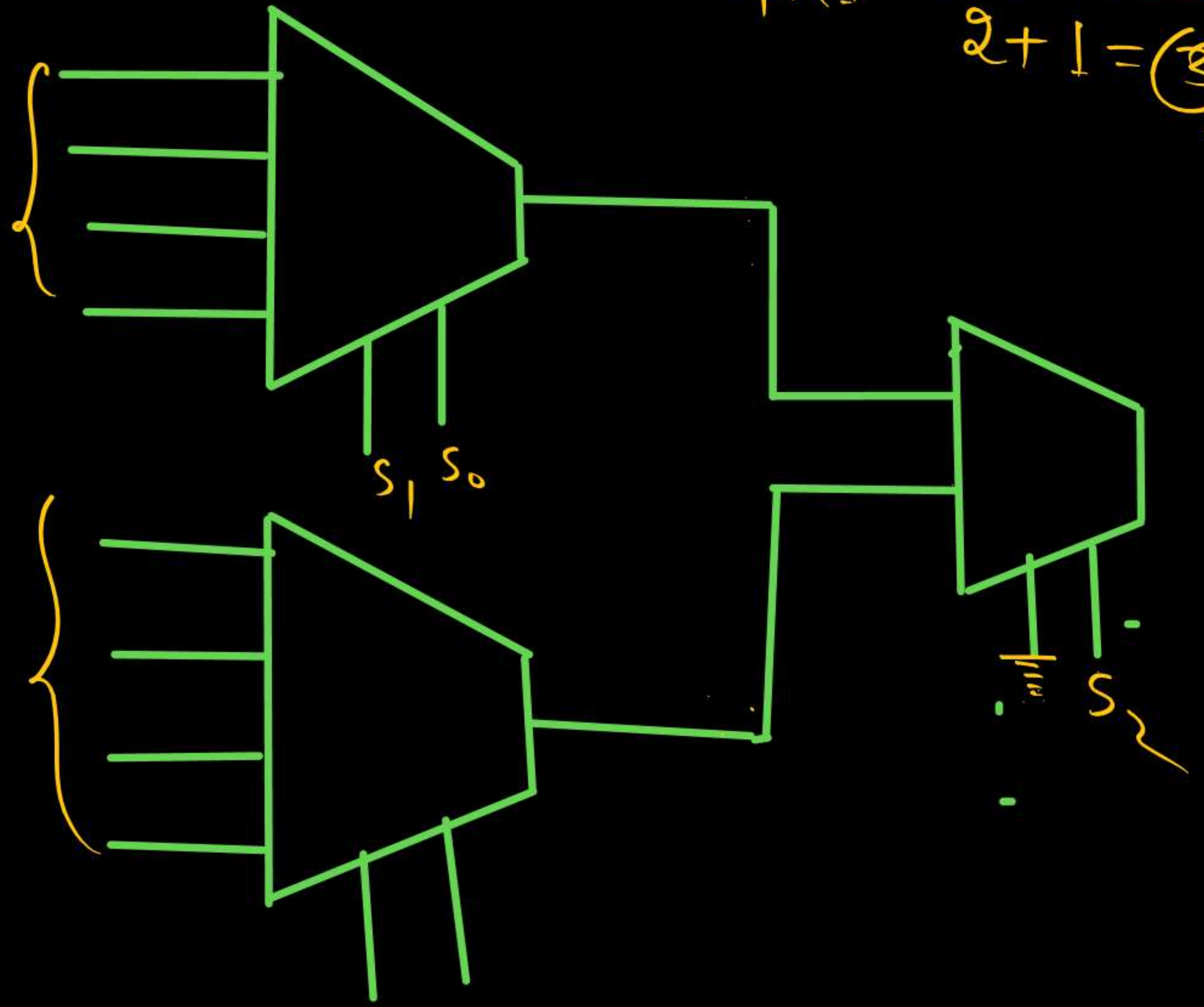
$$4 + 1 = 5$$

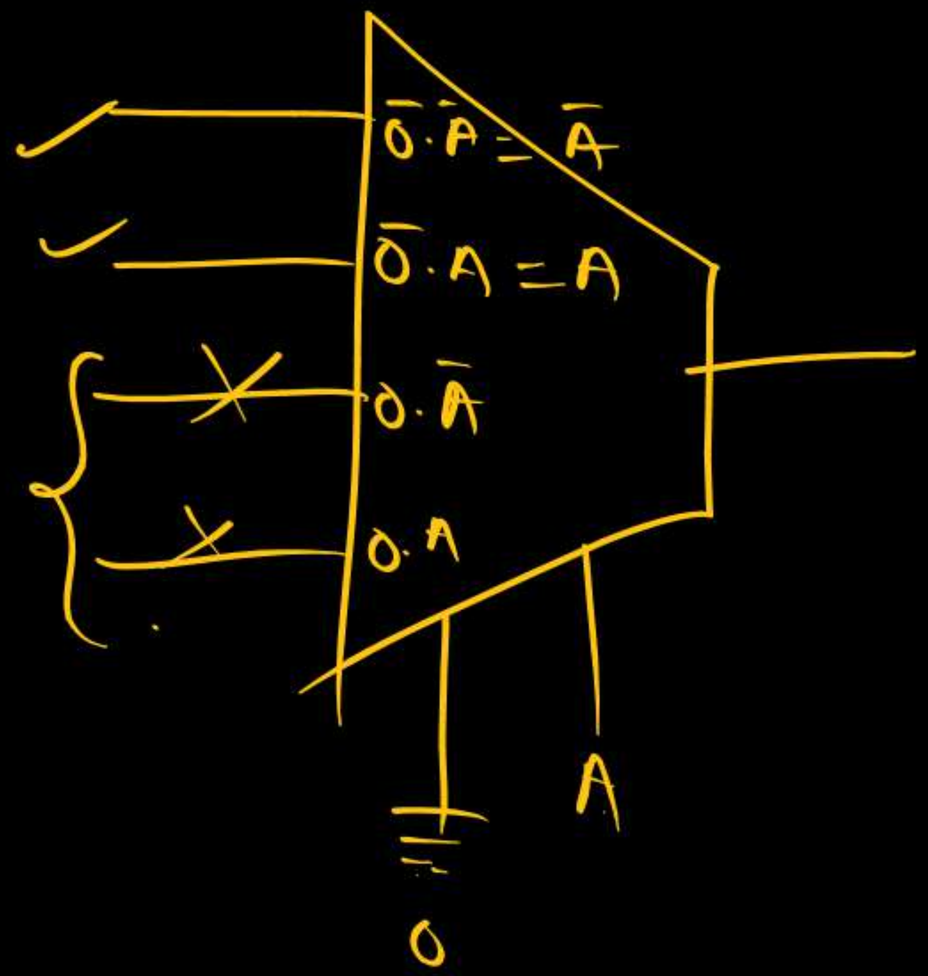
Ex. 4. 4 x 1 MUX --→ 8 x 1 MUX

$$\frac{8}{4} + \frac{2}{4}$$

$$2 + 1 = 3$$

$$4\times 1 \xrightarrow[2+1=3]{\frac{8}{4}+\frac{2}{4}} 8\times 1 \text{ MUX}$$





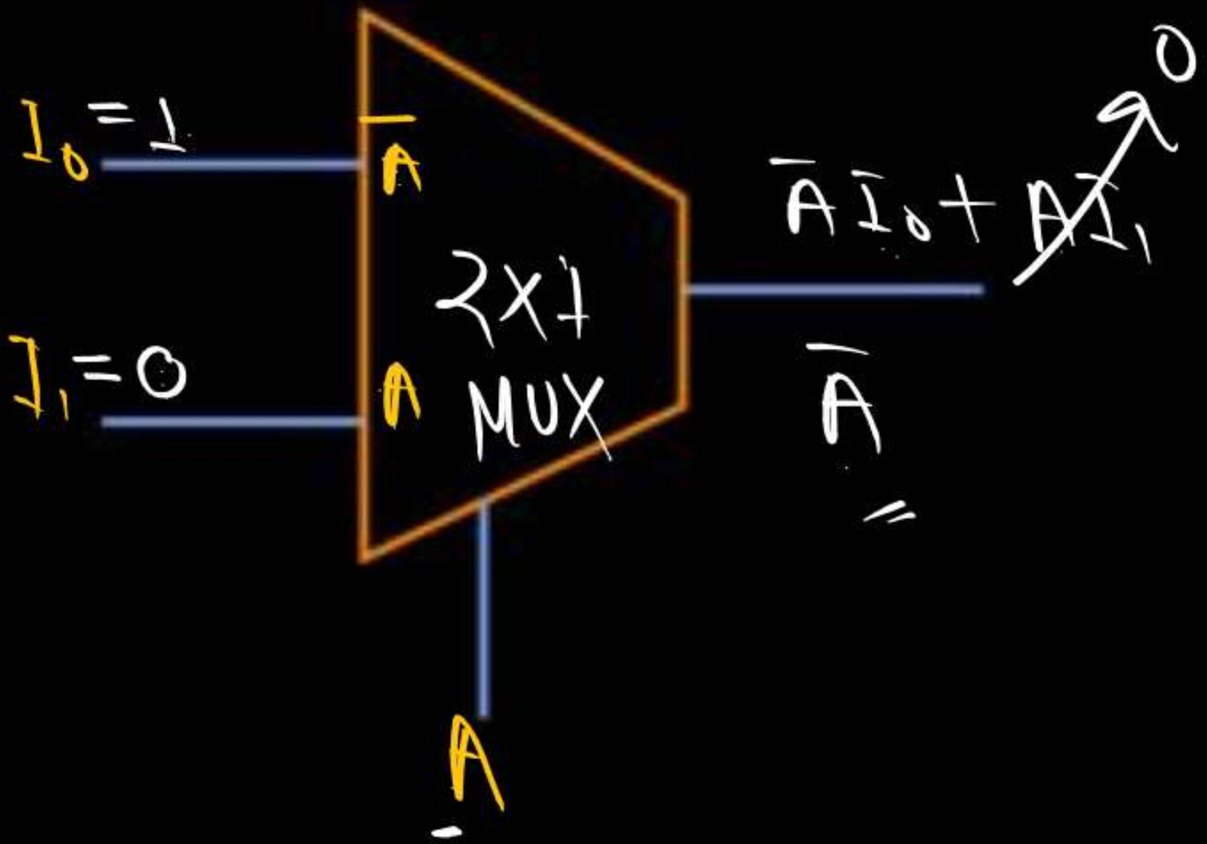
$\bar{0}\cdot\bar{A} = \bar{A}$
$\bar{0}\cdot A = A$
$0\cdot\bar{A}$
$0\cdot A$
A
0

Ex. 5. 4 x 1 MUX $\xrightarrow{\frac{64}{4} + \frac{16}{4} + \frac{4}{4}}$ 64 x 1 MUX

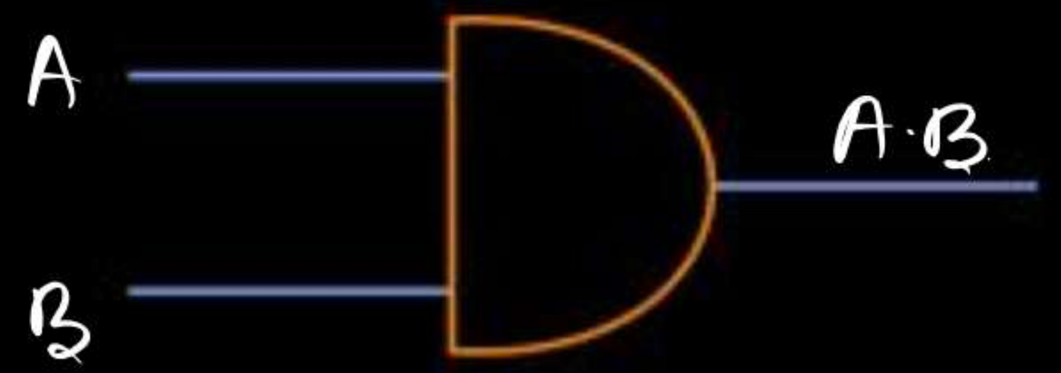
$16 + 4 + 1 = \underline{\underline{21}}$

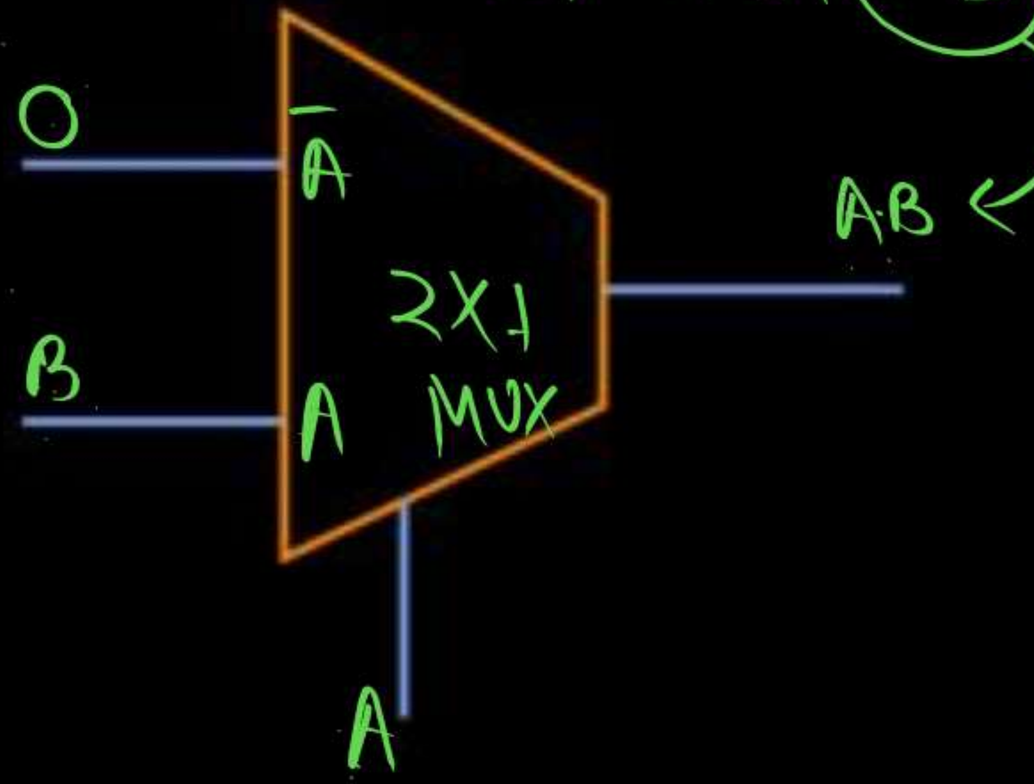
TYPE -2 MUX AS A UNIVERSAL LOGIC

1. Not Gate



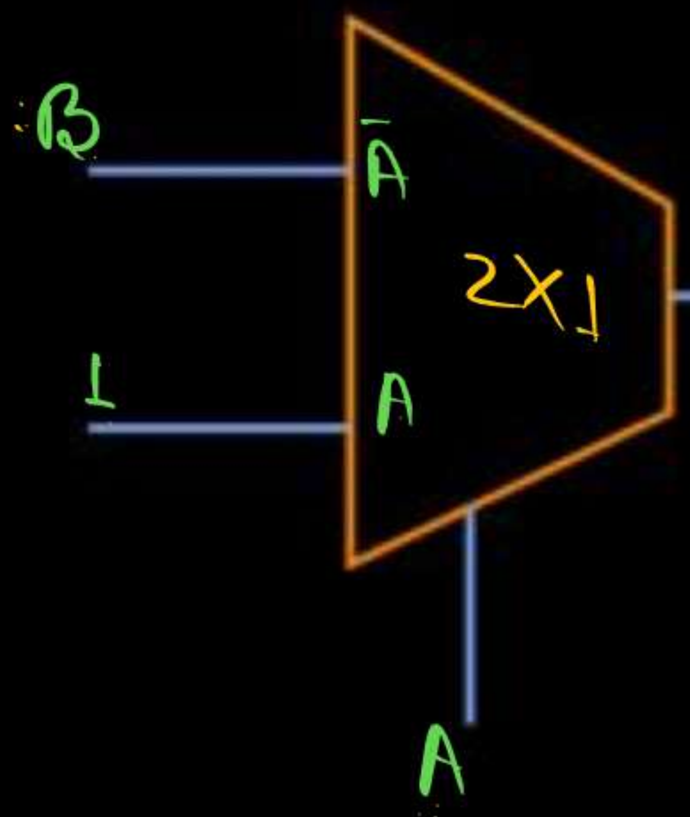
2. AND GATE





$\Rightarrow \bar{A}\cdot 0 + A\cdot B$

3. OR GATE



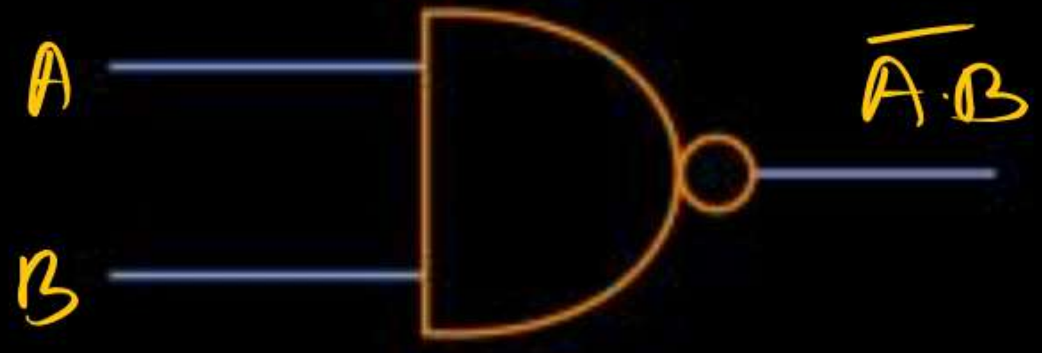
$\bar{A}B + A$

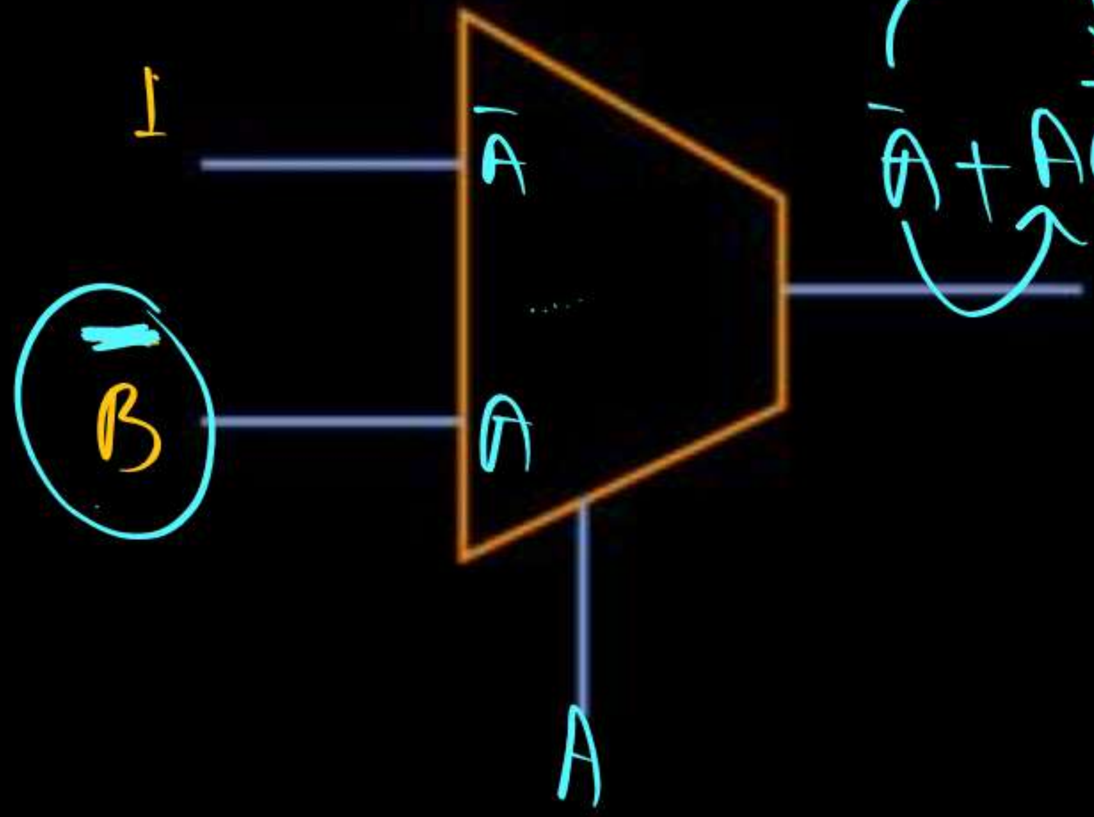
$(\bar{A}+A)\cdot(A+B)$

$\underline{\underline{A+B}}$

4. NAND GATE

2





$$\bar{A}+A\bar{B} = (\bar{A}+A)(\bar{A}+\bar{B})$$

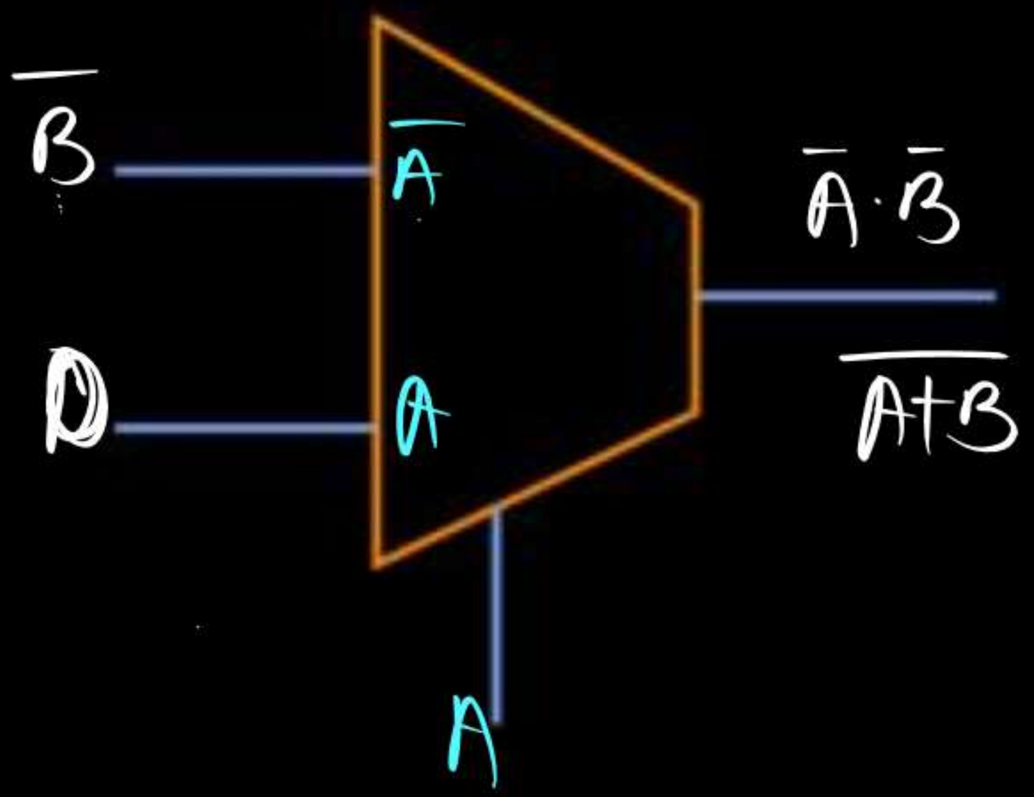
$$= \bar{A}+\bar{B}$$

$$= \overline{A\cdot B}$$

5. NOR GATE

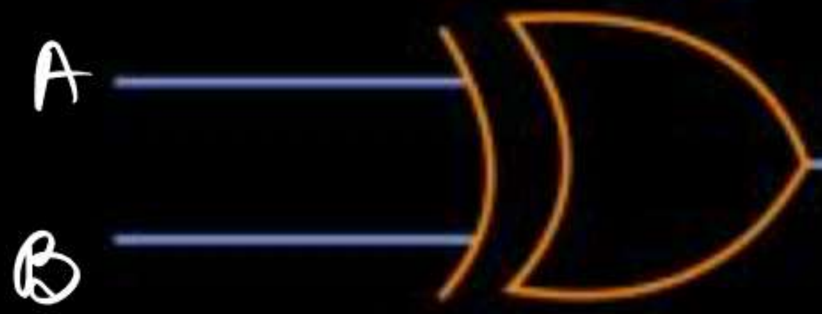
A
B
$\overline{A+B}$

2



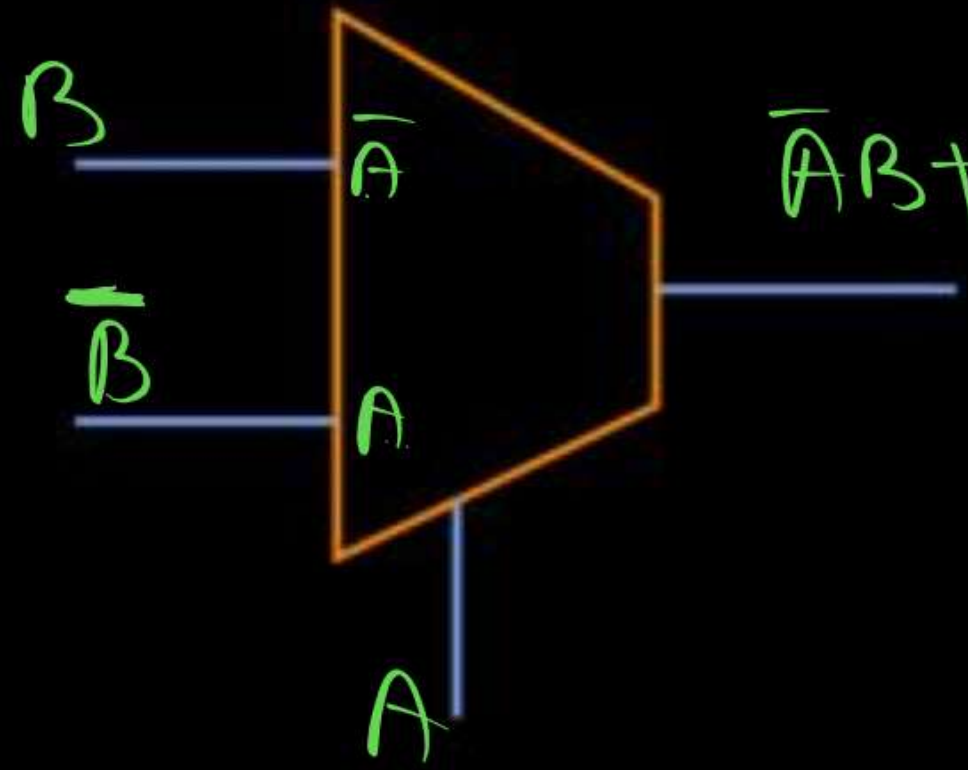
$\overline{B}$
$\overline{A}$
D
A
$\overline{A}\cdot\overline{B}$
$\overline{A+B}$
A

6. XOR GATE



$A \oplus B = \bar{A}B + A\bar{B}$

2

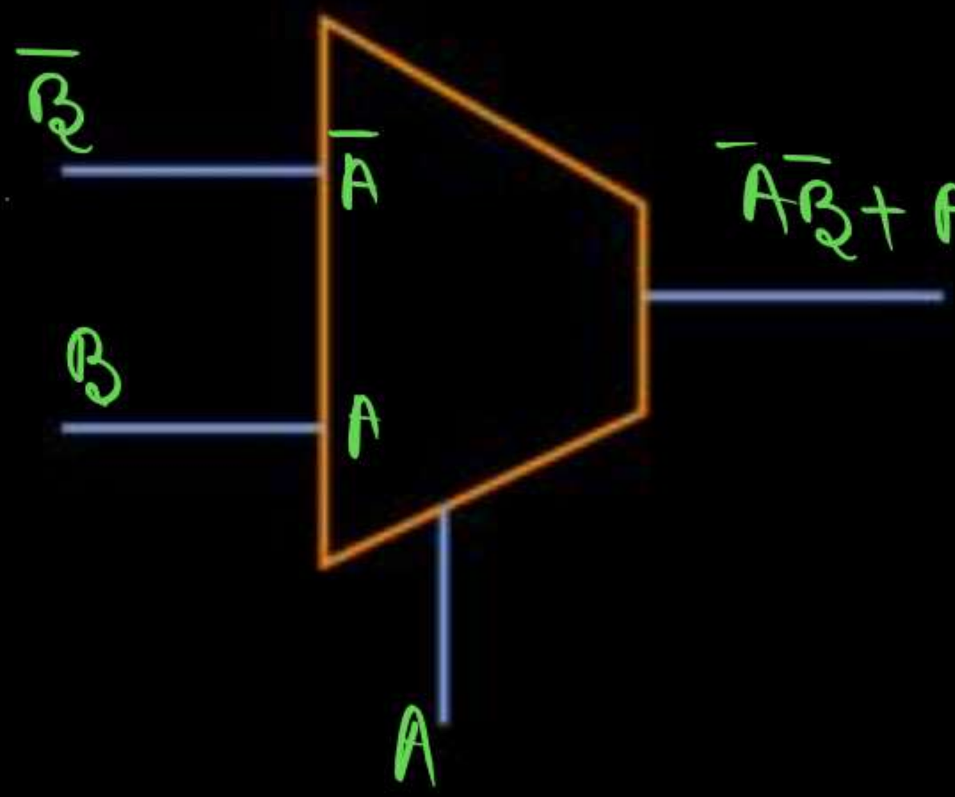


$\bar{A}B + A\bar{B} = A \oplus B$

7. XNOR GATE

$A \odot B = \bar{A}\bar{B} + AB$

Q

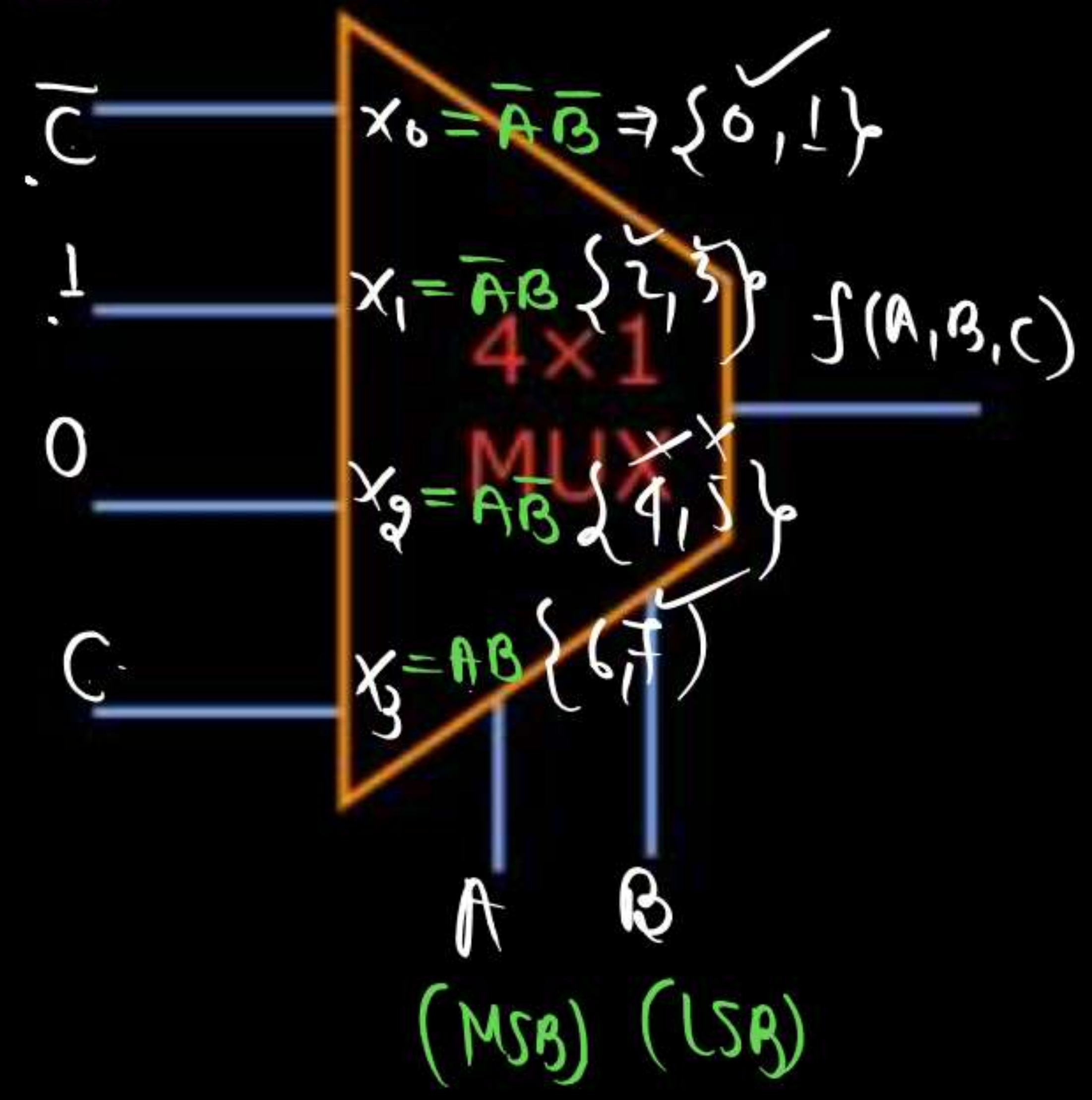


$\bar{A}\bar{B} + AB = A \odot B$

Q.

Type-3 Minimization

Ex. 1.



$$f(A,B,C) = \bar{A}\bar{B}\bar{C} + \bar{A}B\cdot 1 + A\bar{B}\cdot 0 + A\cdot B\cdot C$$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}B(\bar{C}+C) + ABC$$

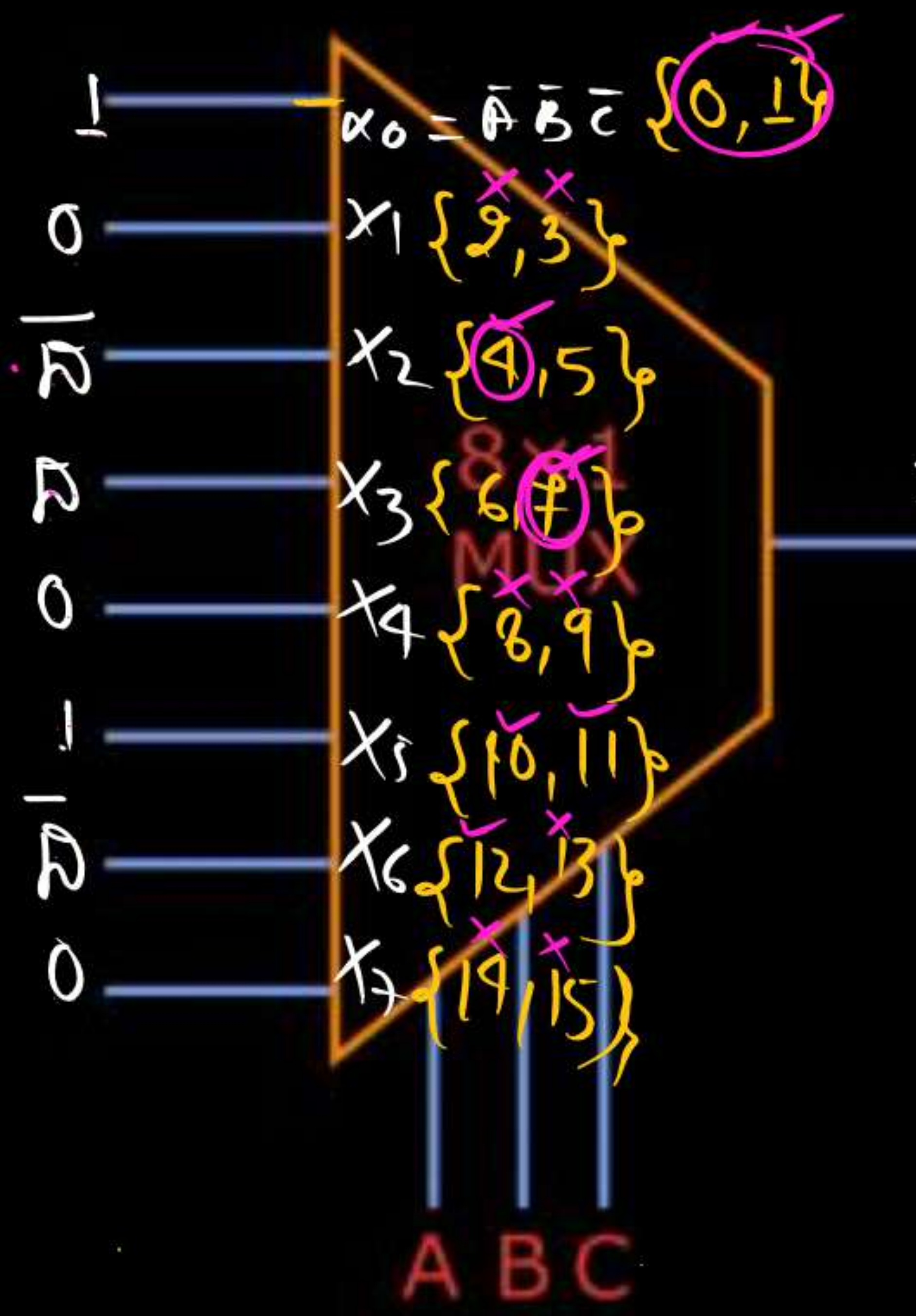
$$= \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + ABC$$

$$= \sum m(0,2,3,7)$$

A \ BC	00	01	11	10
0	1		1	1
1			1	

$\bar{A}\bar{C} + BC$ Ans

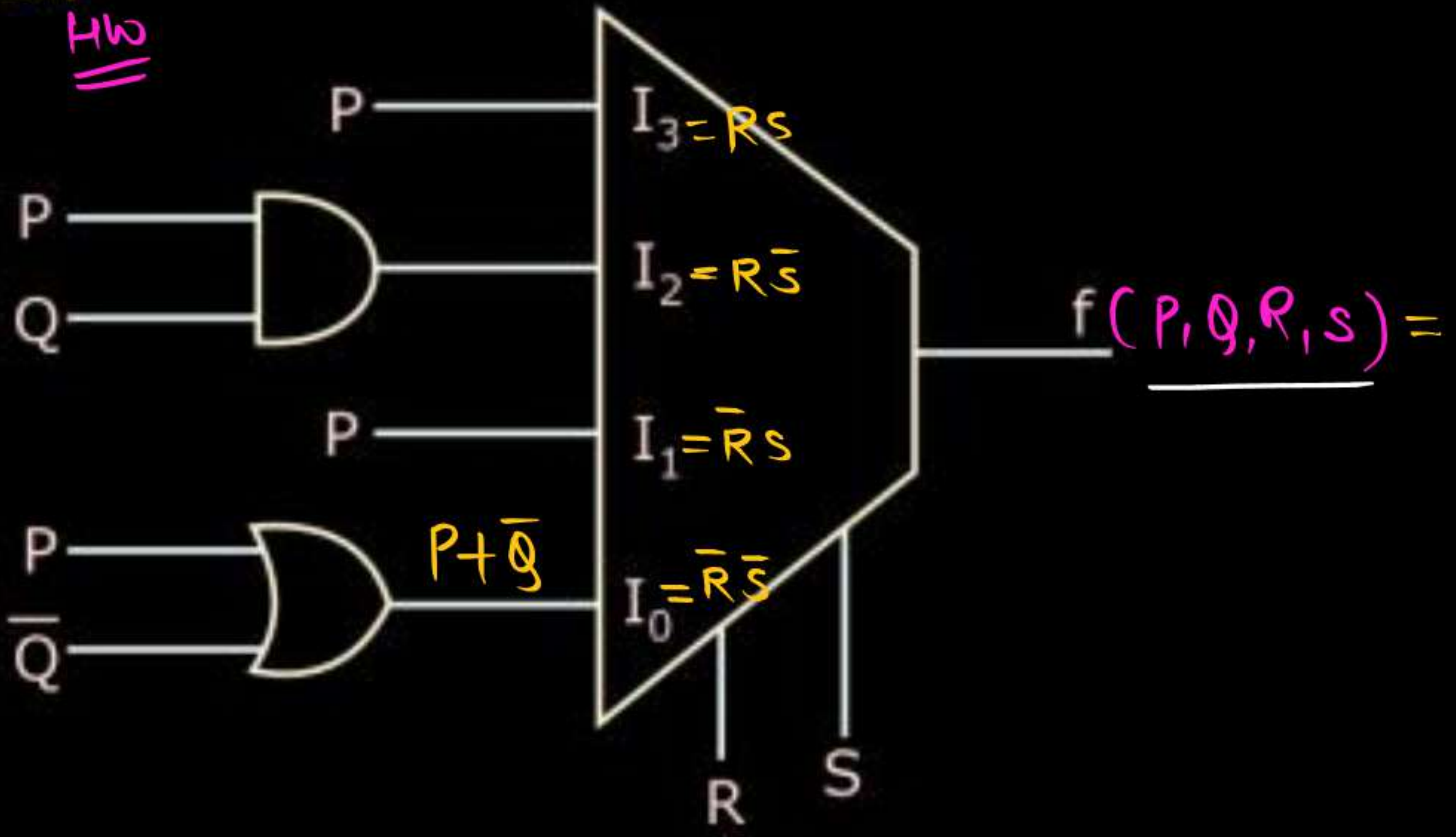
Ex.



$$f(A,B,C,D) = \sum m(0,1,4,7,10,11,12)$$

Ex. GATE

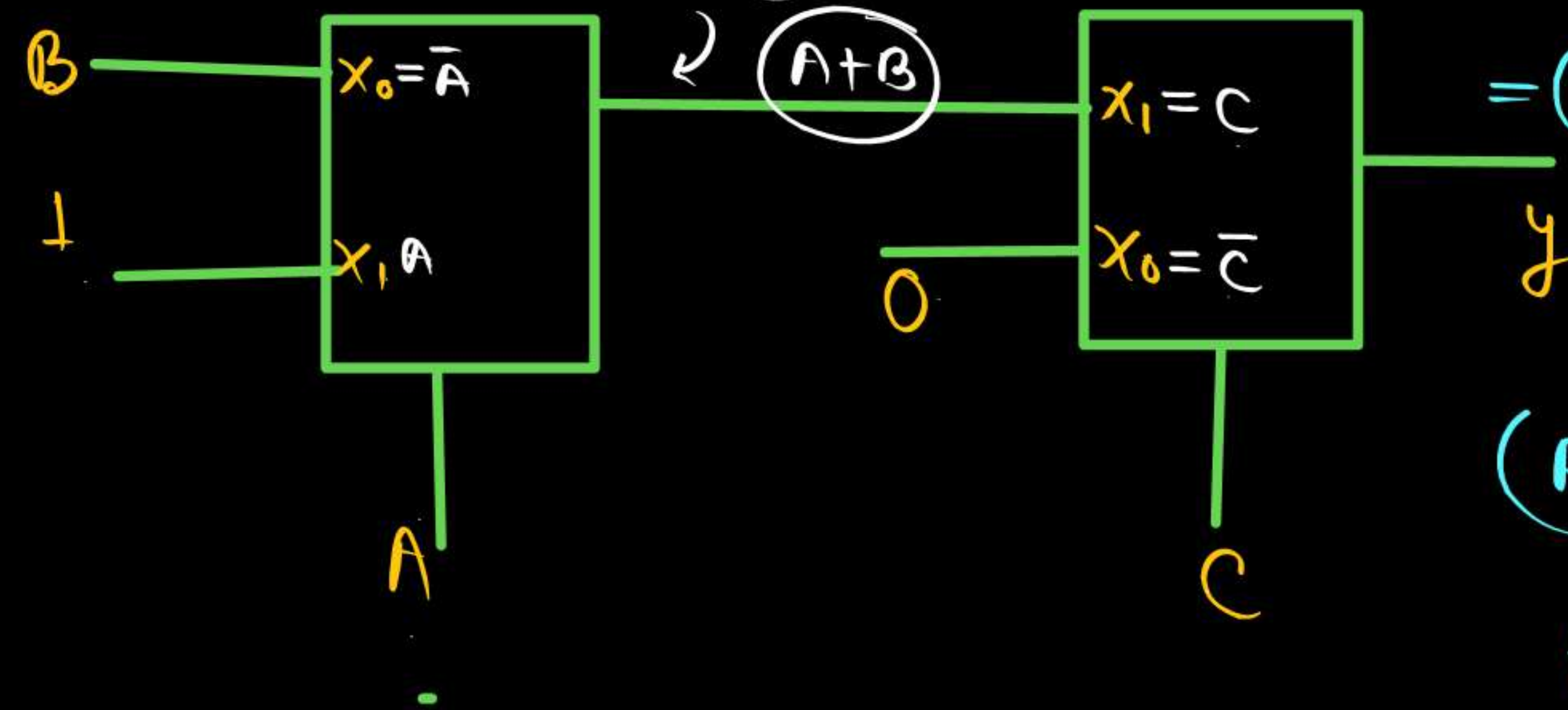
HW



P
P
Q
P
P
$\overline{Q}$
$P+\overline{Q}$
$I_3 = RS$
$I_2 = R\overline{S}$
$I_1 = \overline{R}S$
$I_0 = \overline{R}\,\overline{S}$
R
S
f(P,Q,R,S) =

Ex.

$\bar{A}B + A = (\bar{A}+A)(A+B)$



$= (A+B)C + 0$

$y = (A, B, C) = ?$

$(A+B)C$

$AC + BC$

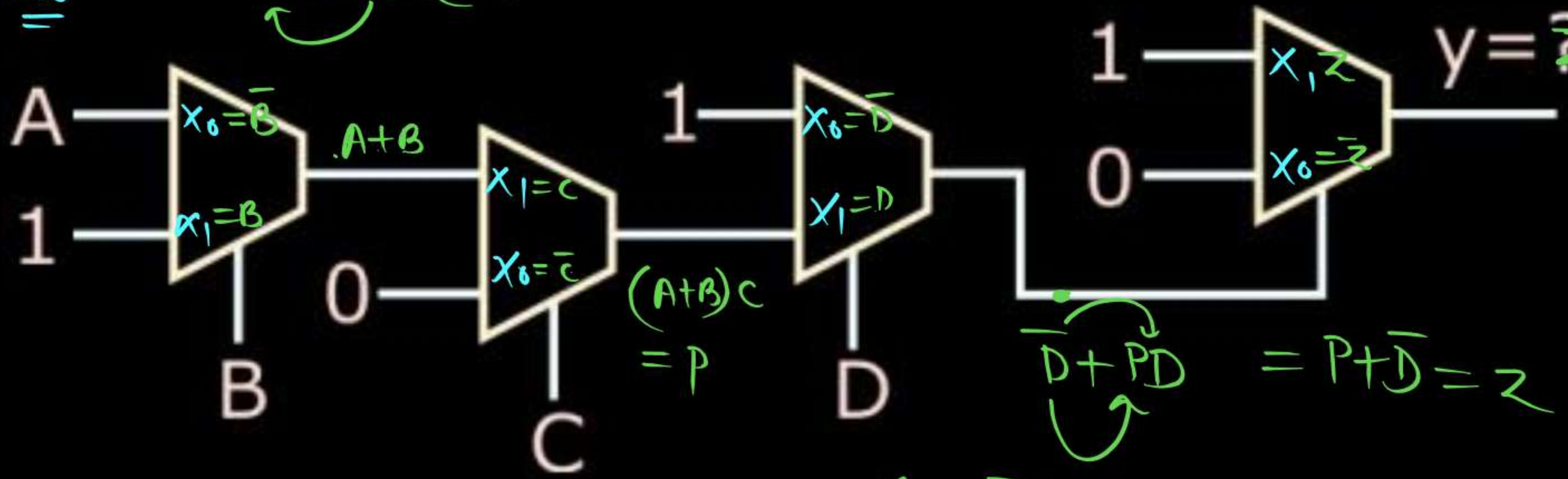
Ans

Type-4 Cascading of MUX

$(A+B)C = P$

Ex

$A\bar{B}+B = (A+B)\cdot(\bar{B}+B)$



$Z = P+\bar{D}$

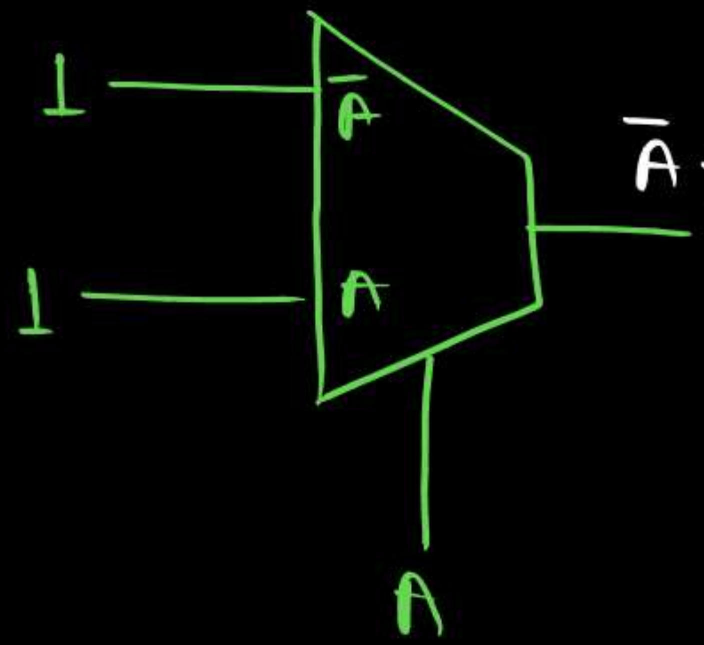
$(A+B)C+\bar{D}$

$\bar{D}+PD = P+\bar{D} = Z$

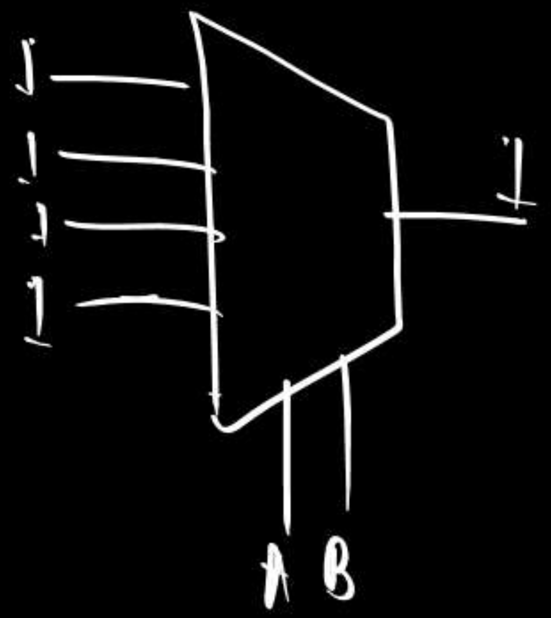
$(P+\bar{D})(\bar{D}+D)$

$P+\bar{D}$

Ans

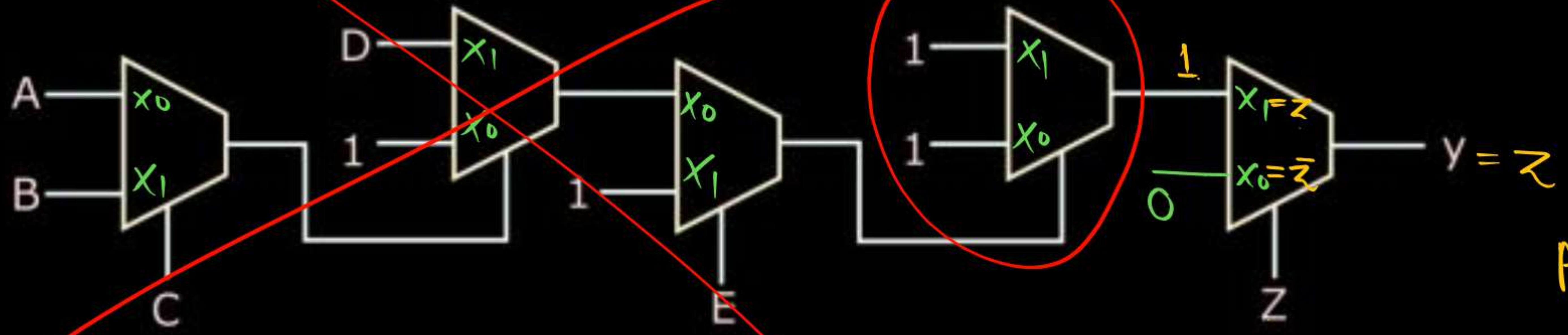


$\bar{A} + A = 1$



3 Sec

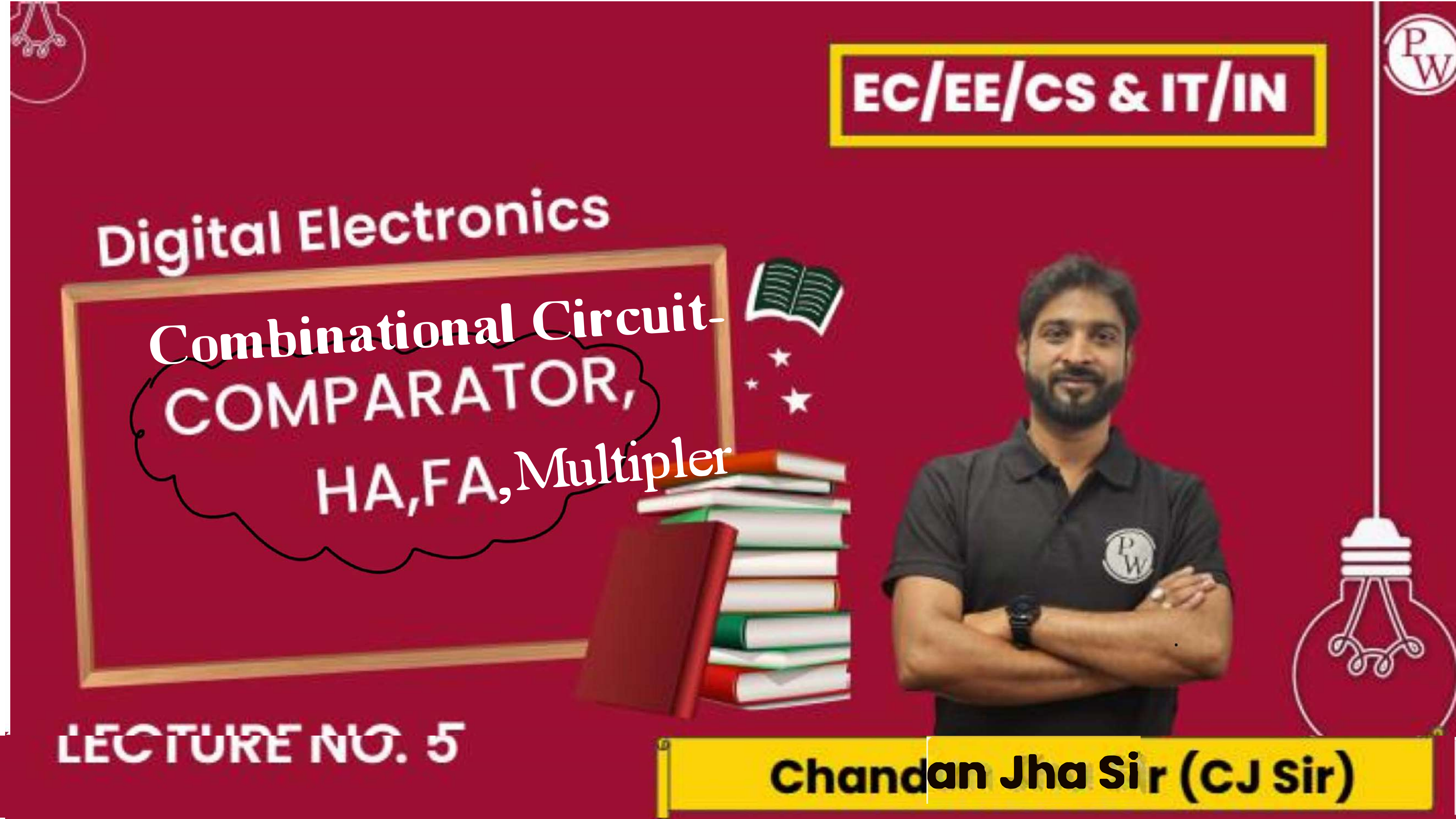
Ex.



$y = \bar{z}$

Ans

THANK YOU!


EC/EE/CS & IT/IN
Digital Electronics
Combinational Circuit-
COMPARATOR,
HA,FA,Multipler
LECTURE NO. 5
Chandan Jha Sir (CJ Sir)

मंज़िल यूँ ही नहीं
मिलती राही को,
जूनून सा दिल में
जगाना पड़ता है,
पूछा चिड़िया से
कि घोसला कैसे बनता है
वो बोली कि तिनका-तिनका
उठाना पड़ता है.

ABOUT ME

- Cleared Gate Multiple times with double Digit Rank (AIR 23, AIR 26)
- Qualified ISRO Exam
- Mentored More then 1 Lakhs+ Students (Offline & Online)
- More then 250+ Motivational Seminar in various Engineering College including NITs & Some of IITs

Chandan Jha

Logic GATE

↳ INVERTER

$$f = \frac{1}{2N \times \tau_{pd}}$$

AND

OR

$Y = A \cdot B$

$Y = A + B$

TTL → 1

ECL → 0

Sunday

↳ Monday

NAND

$Y = \overline{A \cdot B}$

NOR ?

$Y = \overline{A + B}$

POS

SOP

$\hookrightarrow$ AND-OR

NAND-NAND

AOI

$\hookrightarrow$ OR-AND

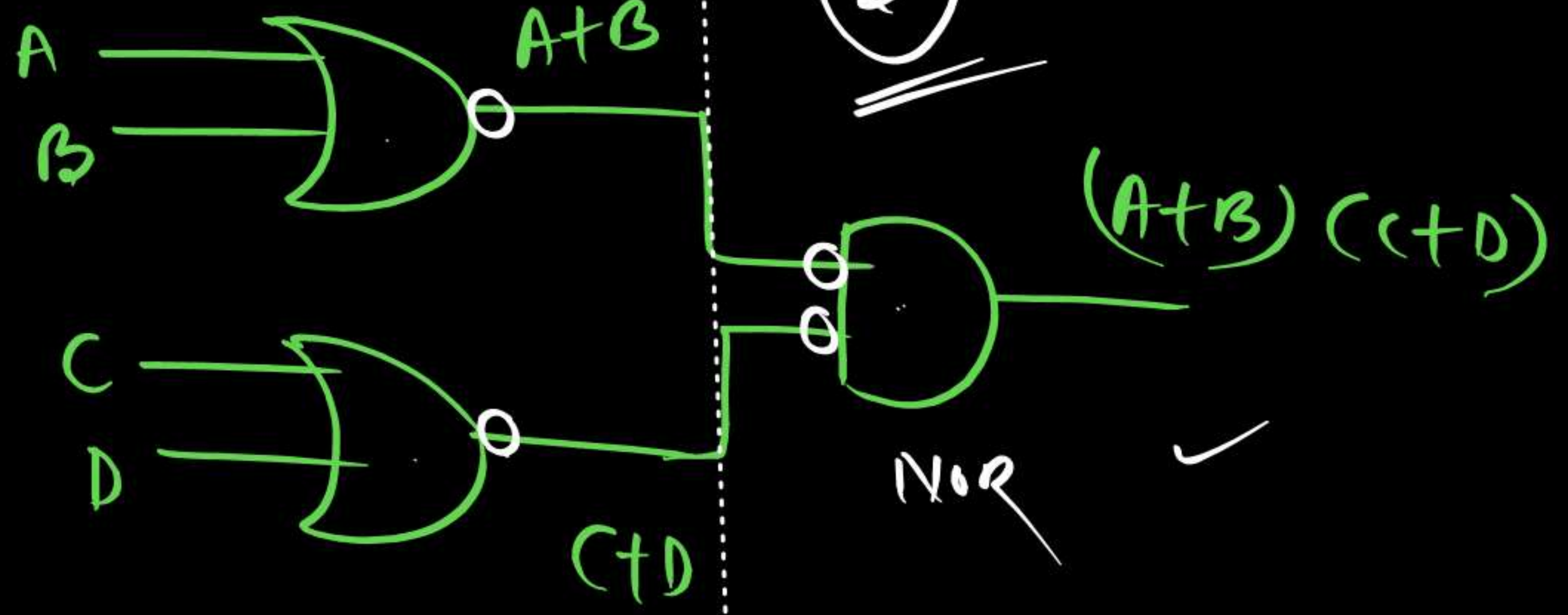
NOR-NOR

$AB + CD \rightarrow 3$

$f = (A+B)(C+D) \longrightarrow$ POS

NOR = ?

3



OR — AND

NOR — NOR

XOR

$A \oplus A = 0$

$A \oplus 0 = A$

$A \oplus \bar{A} = 1$

$A \oplus 1 = \bar{A}$

$A \oplus B \oplus C = \sum m(1,2,4,7)$

1947

BJT

X-NOR

$A \odot A = 1$

$A \odot 1 = A$

$A \odot \bar{A} = 0$

$A \odot 0 = \bar{A}$

$$(A \odot B) \odot C = A \oplus B \oplus C$$

Boolean algebra:

$\Rightarrow A + BC = (A+B)\cdot(A+C)$

$\Rightarrow AB + \bar{A}C + BC = AB + \bar{A}C$

$\Rightarrow (A+B)(\bar{A}+C) = AC + \bar{A}B$

$\Rightarrow \overline{ABC} = \bar{A} + \bar{B} + \bar{C}$

$\overline{A+B+C} = \bar{A}\cdot\bar{B}\cdot\bar{C}$

SOP

POS

K-MAP

→ Gray code

→ cyclic

Reflecting code

Unity hamming distance code

CJ BABA RULE

SOP, dont

POS

I, PI, EPI

$\{\bar{A}\bar{B}, AB, \bar{A}C, BC\}$

A \ BC	00	01	11	10
0	1	1	1	
1			1	1

EPI

$= \bar{A}\bar{B} + AB + \bar{A}C \rightarrow$ SPI

$I = 5$

$PI = 4$

$EPI = 2$

SPI

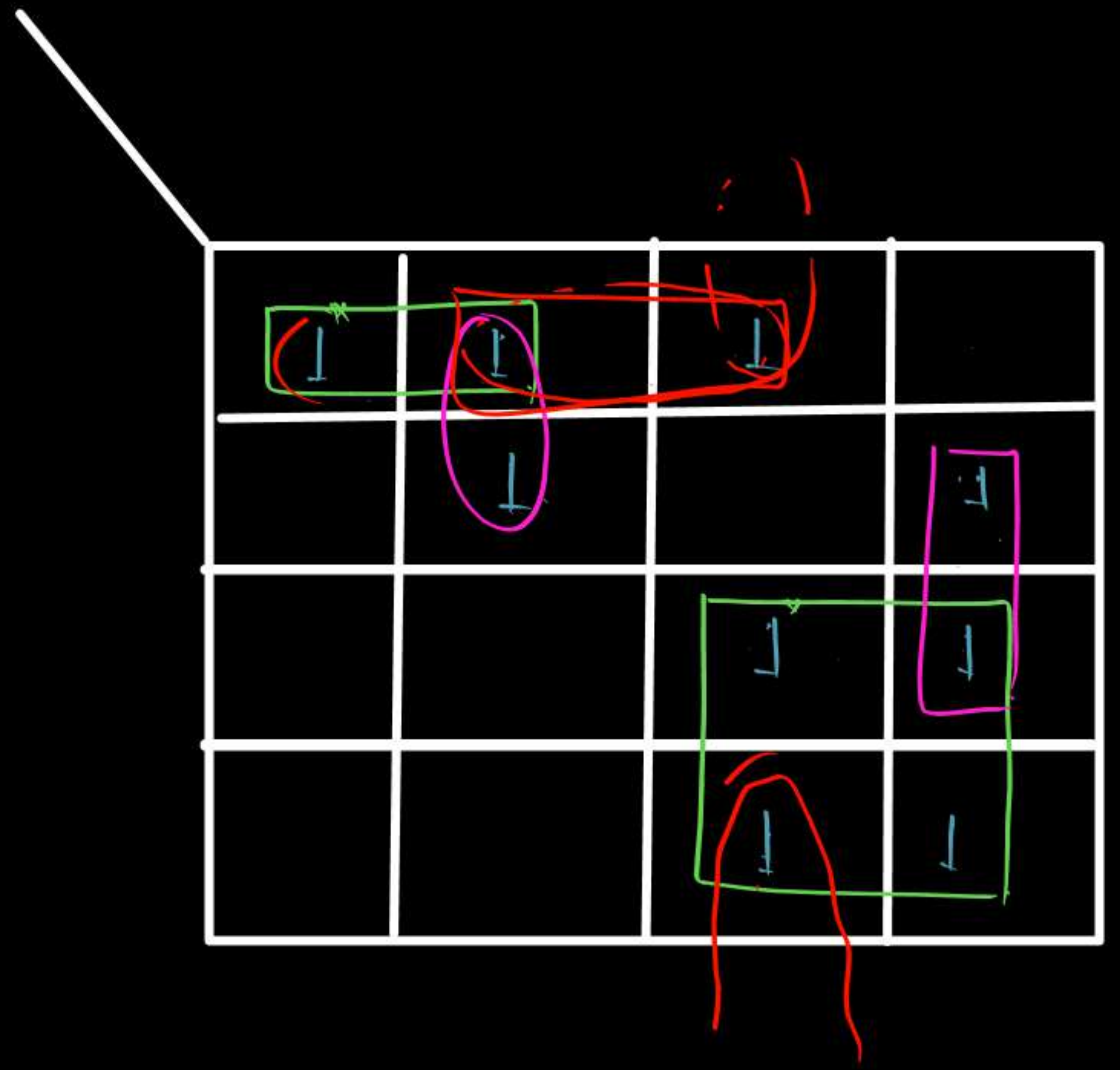
RPI

A \ BC	00	01	11	10
0	1	1	1	
1			1	1

$= \bar{A}\bar{B} + AB + BC \rightarrow$ RPI

SPI → Selective prime Implicant

RPI → Reduced prime Implicant



PI = 6

I = 9

EPI = 4

SPI = 1

RPI = 1

Combinational circuit

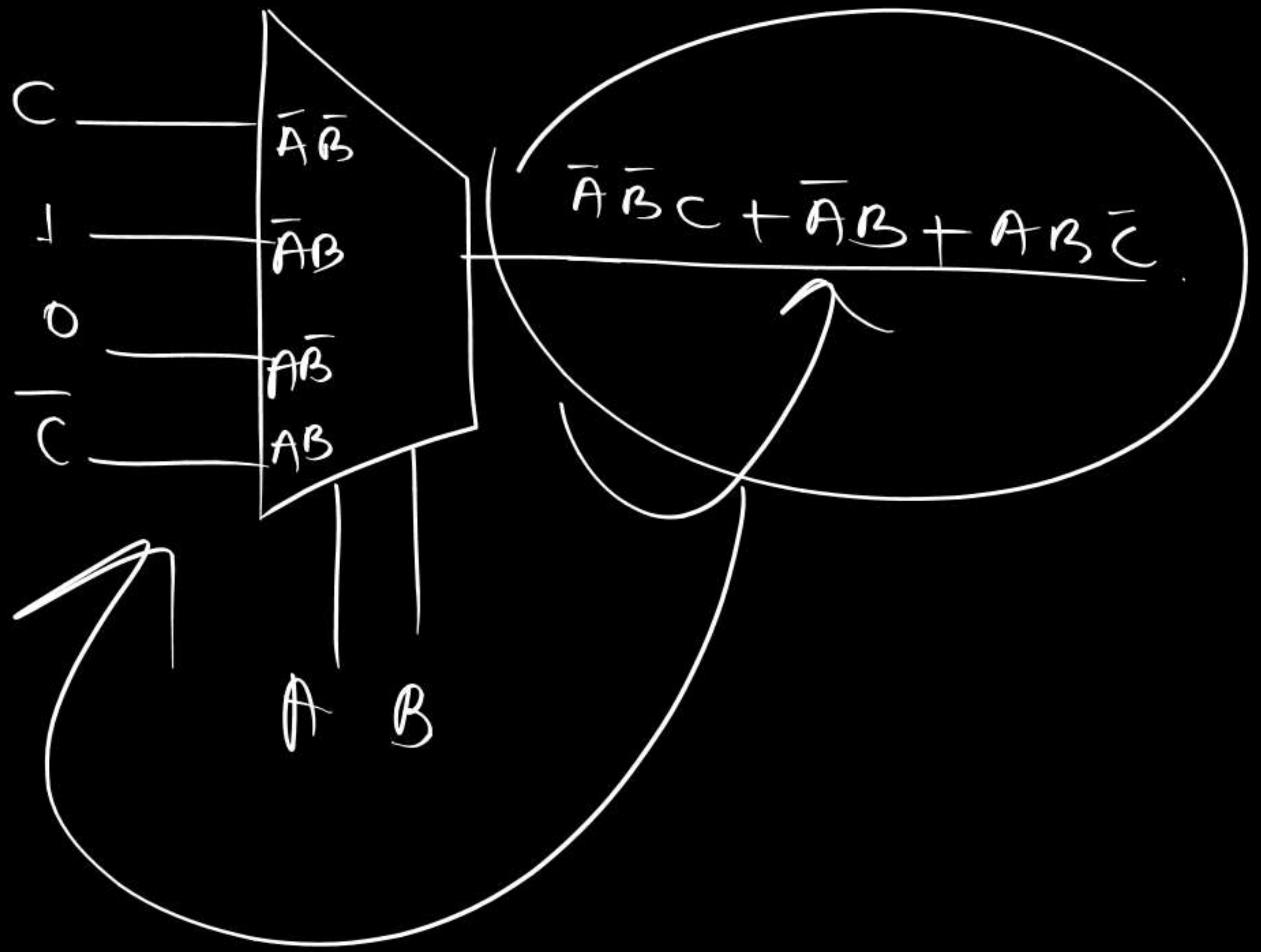
MUX → universal logic

2X1

4X1

8X1

AND-OR



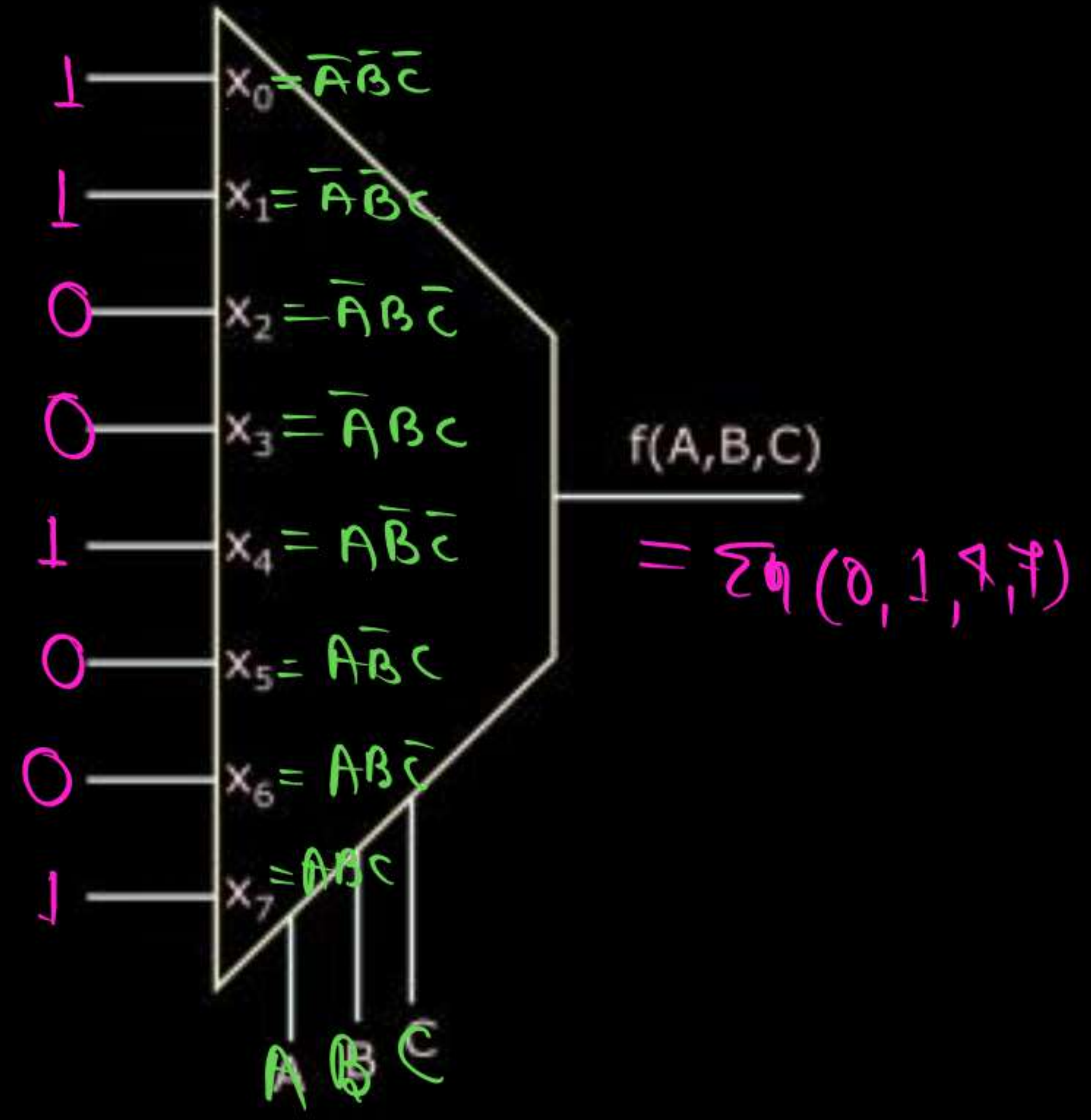
C
1
0
$\bar{C}$
$\bar{A}\bar{B}$
$\bar{A}B$
$A\bar{B}$
AB
A
B
$\bar{A}\bar{B}C + \bar{A}B + AB\bar{C}$

Type -5. Implementation of function

Ex. Implement the function given below by using 8x1 Mux

$$f(A,B,C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$$

$$= \Sigma m(0,1,4,7)$$



Type -5. Implementation of function

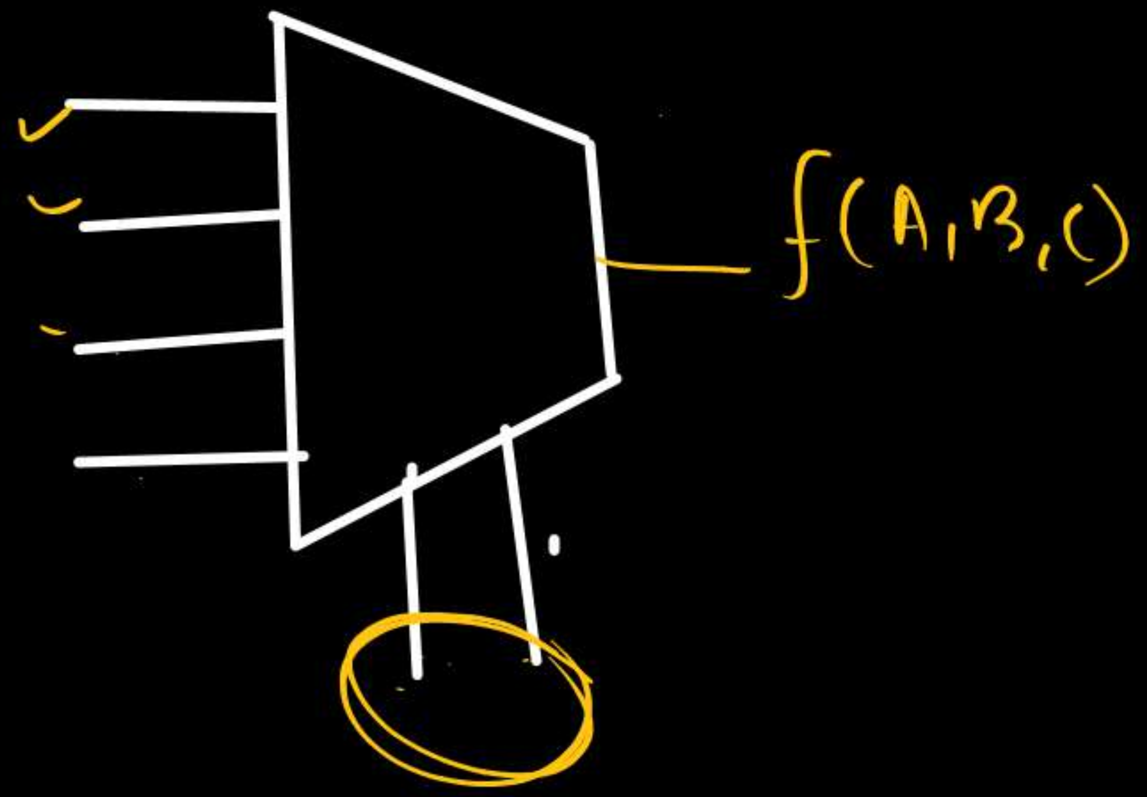
Ex. Implement the function given below by using $\boxed{4\text{x}1 \text{ Mux}}$

$$f(A, B, C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$$

no. of select line = 2.

$= \Sigma m(0, 1, 4, 7)$

1. AB as a select line
2. BC as a select line
3. AC as a select line



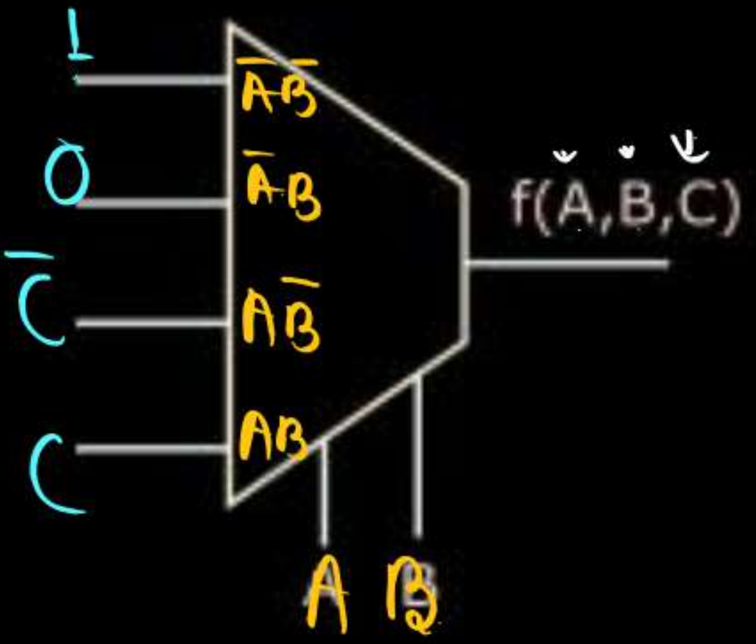
Type -5. Implementation of function

Ex. Implement the function given below by using 4x1 Mux

$$f(A,B,C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$$

$$= \Sigma m(0,1,4,7)$$

1. AB as a select line



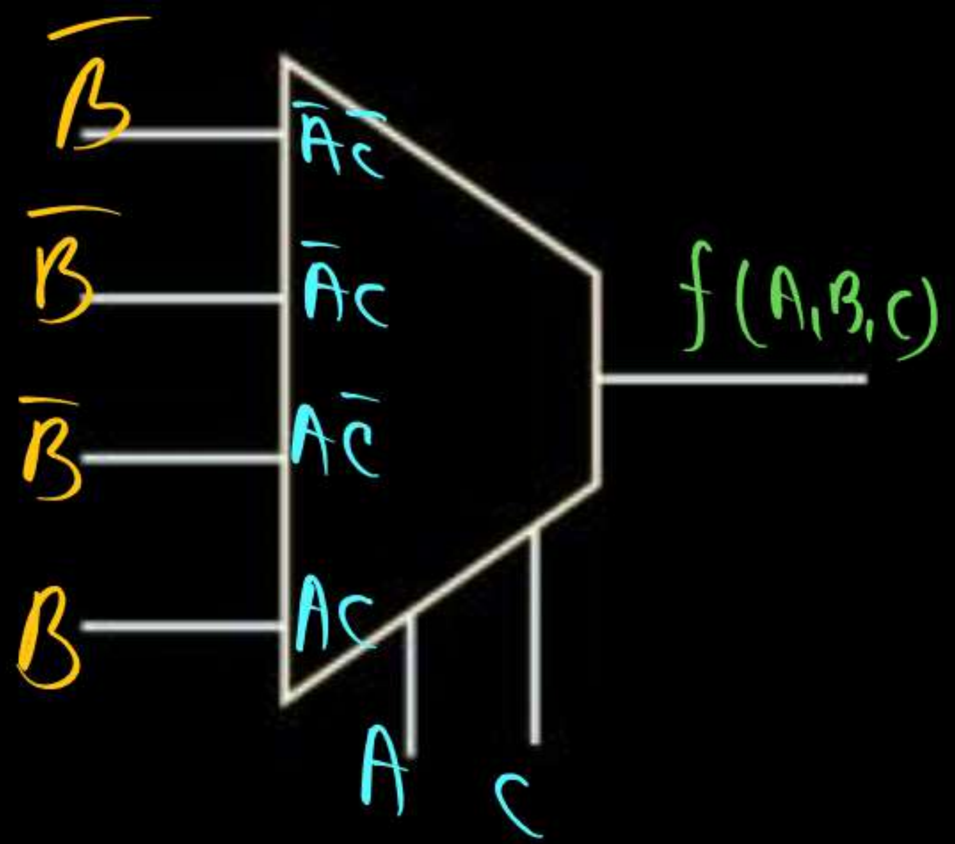
	$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	AB
$\bar{C}$	$\bar{A}\bar{B}\bar{C}$ 0	$\bar{A}B\bar{C}$ 2	$A\bar{B}\bar{C}$ 4	$AB\bar{C}$ 6
C	$\bar{A}\bar{B}C$ 1	$\bar{A}BC$ 3	$A\bar{B}C$ 5	ABC 7
	1	0	$\bar{C}$	C

Type -5. Implementation of function

Ex. Implement the function given below by using 4x1 Mux

$$f(A,B,C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$$
$$= \Sigma m(0,1,4,7)$$

3. AC as a select line



	$\bar{A}\bar{C}$	$\bar{A}C$	$A\bar{C}$	AC
$\bar{B}$	$\bar{A}\bar{B}\bar{C}$ 0	$\bar{A}\bar{B}C$ 1	$A\bar{B}\bar{C}$ 4	$A\bar{B}C$ 5
B	$\bar{A}B\bar{C}$ 2	$\bar{A}BC$ 3	$AB\bar{C}$ 6	ABC 7
	$\bar{B}$	$\bar{B}$	$\bar{B}$	B

HW

$f(A,B,C) = \Sigma m(0, 1, 4, 7$

Q BC as a select line.

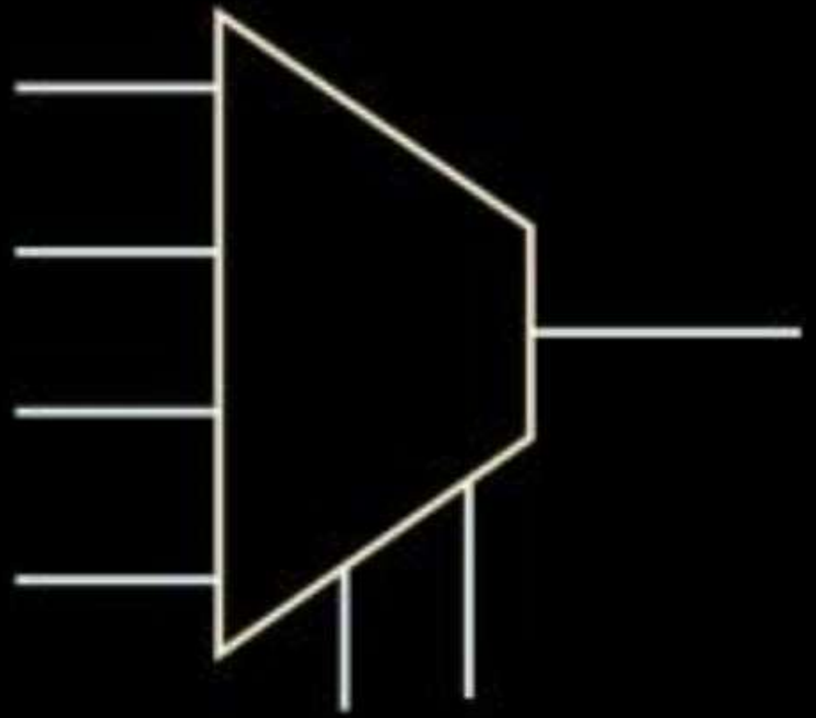
$\boxed{\text{Comment Box}}$

Type -5. Implementation of function

Ex. Implement the function given below by using 4x1 Mux

$$f(A,B,C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$$

2. BC as a select line



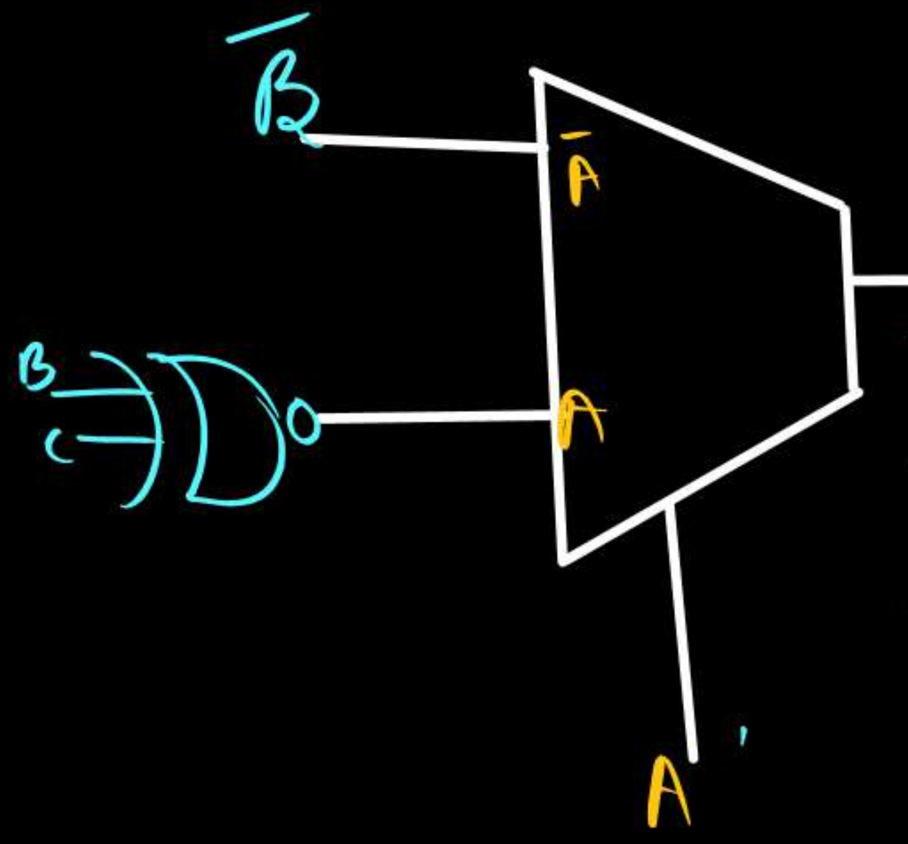
Type -5. Implementation of function

Ex. Implement the function given below by using 2x1 Mux

$$f(A,B,C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$$

Q $f(A, B, C) = \sum m(0, 1, 4, 7) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$

Implement by using 2X1 MUX ?



$f(A,B,C)$

$= \bar{A}\bar{B} + A(\bar{B}\bar{C} + BC)$

$= \bar{A}\bar{B}(\bar{C}+C) + A\bar{B}\bar{C} + ABC$

$= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$

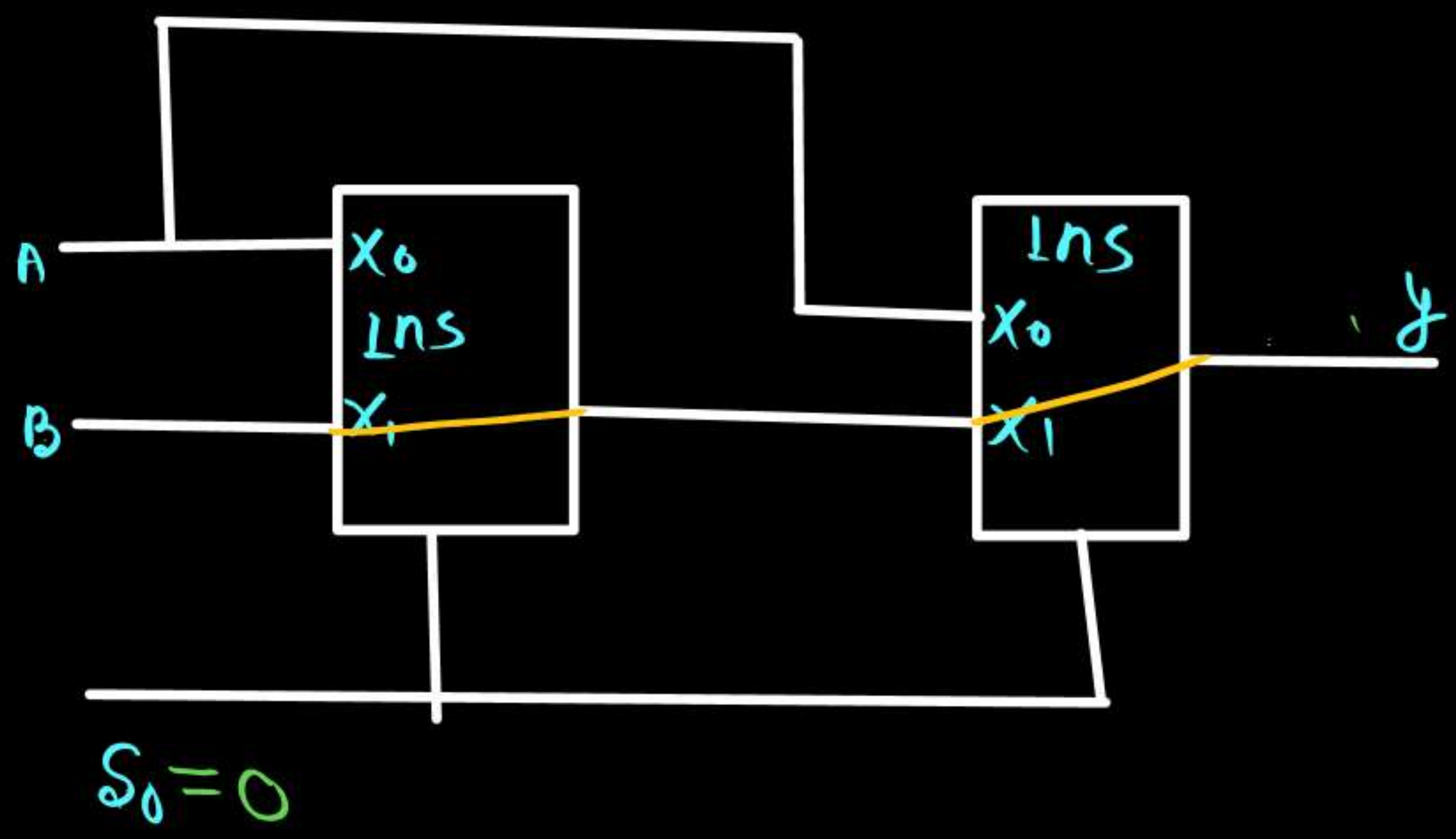
$= \sum m(0, 1, 4, 7)$

	$\bar{A}$ ✓	A ✓
$\bar{B}\bar{C}$	$\bar{A}\bar{B}\bar{C}$ 0	$A\bar{B}\bar{C}$ 4
$\bar{B}C$	$\bar{A}\bar{B}C$ 1	$A\bar{B}C$ 5
$B\bar{C}$	$\bar{A}B\bar{C}$ 2	$AB\bar{C}$ 6
BC	$\bar{A}BC$ 3	ABC 7
	$\bar{B}\bar{C} + \bar{B}C$	$\bar{B}\bar{C} + BC$
	$\bar{B}(\bar{C}+C)$	$B \odot B$ ✓
	$\bar{B}$ ✓	

Ex. HW $f(A,C,B,D) = \Sigma m\ (0, 1, 3, 5, 7, 9, 12, 15)$

1. ABD as select line

2. ACD as a select line.



Minimum Delay = 1ns.

Maximum Delay (Delay) = 2ns

Case (1) $S_0 = 0$

Delay = 1ns.

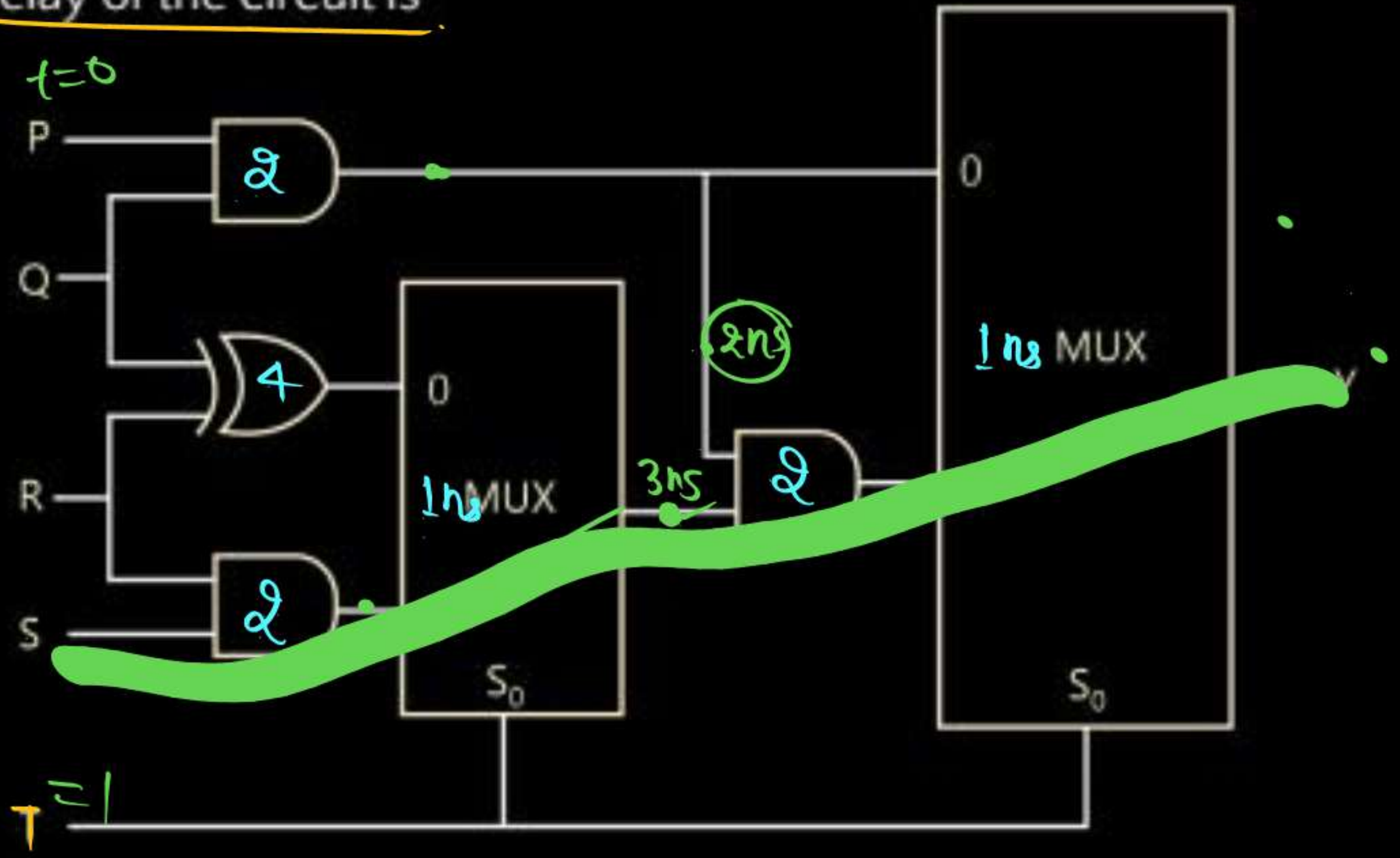
Case (2) $S_0 = 1$

Delay = 2ns

Type -6. Delay in MUX

Q. The propagation delays of the XOR gate, AND gate and multiplexer (MUX) in the circuit shown in the figure are 4 ns, 2 ns and 1 ns, respectively.

If all the inputs P, Q, R, S and T are applied simultaneously and held constant, the maximum propagation delay of the circuit is



6ns

case(1) T=0

AND + MUX(2)

2+1=3ns

case(2). T=1

AND + MUX(1) + AND + MUX(2)

2+1+2+1=6ns

DESIGNING OF COMBINATIONAL CIRCUIT

Step 1. Find the number of inputs and outputs.

Step 2. Write the truth table.

Step 3. Write the logical expression.

Step 4. Minimize the logical expression.

Step 5. Hardware implementation.

single digit 75 - 80 EC 20

Magnitude Comparator

GATE ISRO

World Q-1 K-MAP

Network

ONE BIT MAGNITUDE COMPARATOR

Step-1.

Step 3.

$X(A>B) = A\bar{B}$

$Y(A<B) = \bar{A}B$

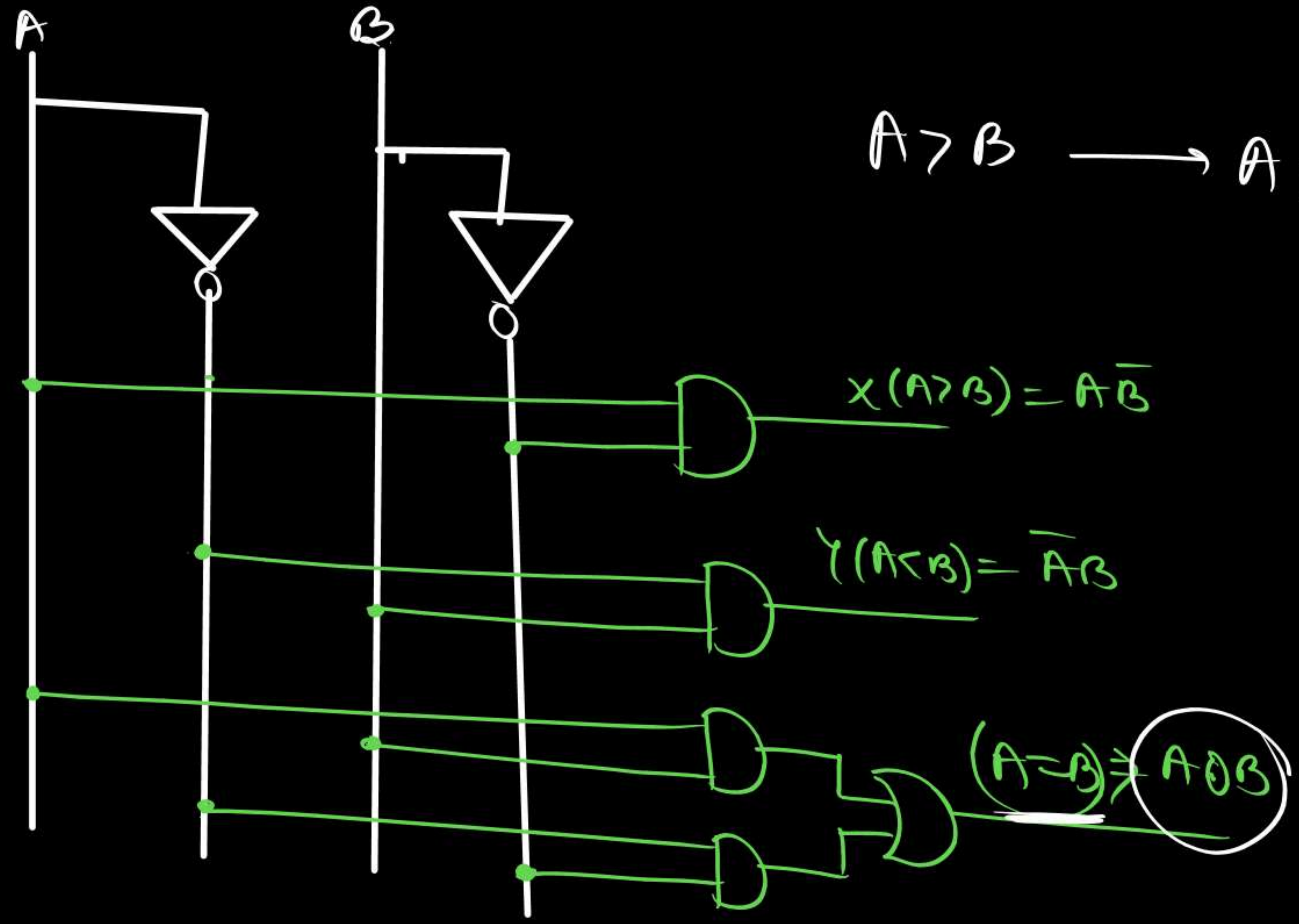
$Z(A=B) = \bar{A}\bar{B} + AB = A \odot B$

Step 4:

Step 2. Truth table

A	B	X (A>B)	Y (A<B)	Z (A=B)
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	~~0~~ 1	0	0	1

$A > B \longrightarrow A\bar{B}$



One bit comparator

Total combination = 4

Equal combination = 2

Unequal combination = 2

Greater = Less = 1

TWO BIT MAGNITUDE COMPARATOR

Step-1

Step 2.

	A		B		A>B	(A<B)	(A=B)
	A_1	A_0	B_1	B_0	x	y	Z
0	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
2 →	0	0	1	0	0	1	0
3 →	0	0	1	1	0	1	0
4 →	0	1	0	0	1	0	0
5 →	0	1	0	1	0	0	1
6 →	0	1	1	0	0	1	0
7 →	0	1	1	1	0	1	0
8 →	1	0	0	0	1	0	0
9 →	1	0	0	1	1	0	0
10 →	1	0	1	0	0	0	1
11 →	1	0	1	1	0	1	0
12 →	1	1	0	0	1	0	0
13 →	1	1	0	1	1	0	0
14 →	1	1	1	0	1	0	0
15 →	1	1	1	1	0	0	1

$X(A>B) = \Sigma m(4, 8, 9, 12, 13, 14)$

$A_1A_0 \backslash B_1B_0$	00	01	11	10
00				
01	1			
11	1	1		1
10	1	1		

$y(A<B) = \Sigma m(1, 2, 3, 6, 7, 11)$

$A_1A_0 \backslash B_1B_0$	00	01	11	10
00		1	1	1
01			1	1
11				
10			1	

$X(A>B) = A_1\bar{B}_1 + A_0\bar{B}_1\bar{B}_0 + A_1A_0\bar{B}_0$ ← minimized expression

$= A_1\bar{B}_1 + \bar{A}_1A_0\bar{B}_1\bar{B}_0 + A_1A_0B_1\bar{B}_0$

$= A_1\bar{B}_1 + (\bar{A}_1\bar{B}_1 + A_1B_1)\cdot A_0\bar{B}_0$

$\boxed{= A_1\bar{B}_1 + (A_1 \odot B_1)\cdot A_0\bar{B}_0}$ → Semimized

$Y(A<B) = \bar{A}_1B_1 + \bar{A}_1\bar{A}_0B_0 + \bar{A}_0B_1B_0$ → Minimized

$$\boxed{Y(A<B) = \bar{A}_1B_1 + (A_1 \odot B_1)\bar{A}_0B_0}$$

$$\boxed{Z(A=B) = (A_1 \odot B_1)\cdot(A_0 \odot B_0)}$$

Two bit comparator

Total combination = 16

Equal combination = 4

Unequal combination = 12

Greater = Less = 6

Three bit comparator

Total combination = 64

Equal combination = 8

unequal combination = 56

Greater = Less = 28

"n" bit comparator

Total combination = 2^{2n}

Equal combination = 2^n

unequal combination = $2^{2n} - 2^n$

Greater = Less = $\frac{2^{2n} - 2^n}{2}$

Semiminimized

$A > B \longrightarrow A\bar{B}$

$A < B \Rightarrow \bar{A}B$

$A = B \Rightarrow A \odot B$

$A = B$

$A_1 \quad A_0 \qquad B_1 \quad B_0$

2 3 2 3

$$A > B \Rightarrow A_1\bar{B}_1 + (A_1 \odot B_1)\cdot A_0\bar{B}_0$$

$$A < B \Rightarrow \bar{A}_1 B_1 + (A_1 \odot B_1)\bar{A}_0 B_0$$

$$A = B \Rightarrow (A_1 \odot B_1)\cdot(A_0 \odot B_0)$$

$$\begin{tikzcd}[column sep=small] & A \arrow[dl] \arrow[d] \arrow[dr] & \\ A_2 & A_1 & A_0 \end{tikzcd} \qquad \begin{tikzcd}[column sep=small] & B \arrow[dl] \arrow[d] \arrow[dr] & \\ B_2 & B_1 & B_0 \end{tikzcd}$$

$A > B$ $$A_2\overline{B_2} + (A_2 \odot B_2)\, A_1\overline{B_1} + (A_2 \odot B_2)\cdot(A_1 \odot B_1)\, A_0\overline{B_0}$$

$A < B$ $$\overline{A_2}B_2 + (A_2 \odot B_2)\,\overline{A_1}B_1 + (A_2 \odot B_2)\cdot(A_1 \odot B_1)\cdot\overline{A_0}B_0$$

$A = B$ $$\left((A_2 \odot B_2)\cdot(A_1 \odot B_1)\cdot(A_0 \odot B_0)\right)$$

$\longrightarrow 2^{2^n}$

$\longrightarrow 2^n$

$\longrightarrow 2^{2^n} - 2^n$

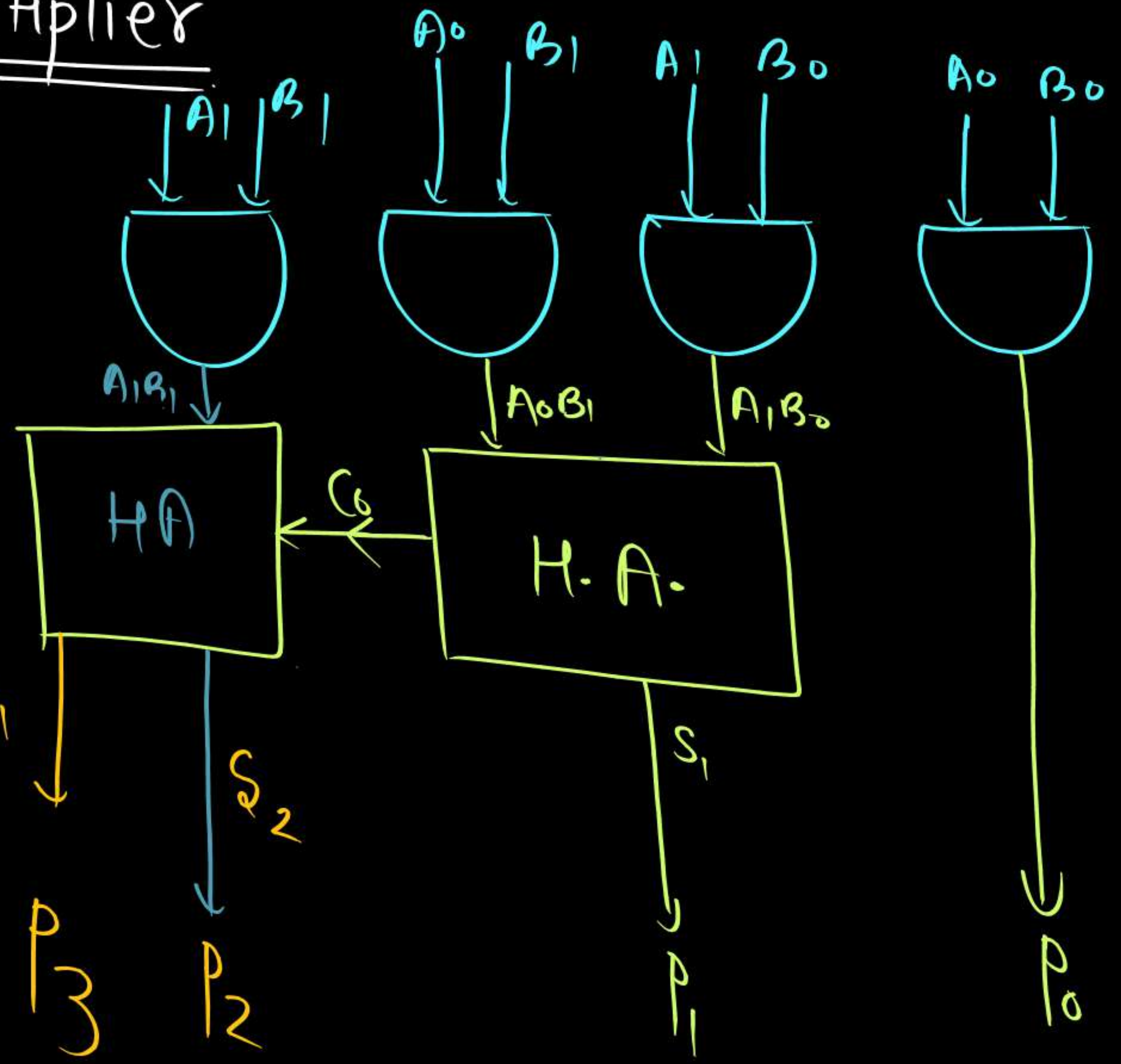
$\longrightarrow \dfrac{2^{2^n} - 2^n}{2}$


जुनून होना चाहिए
लक्ष्य को पाने के लिए,
सपना तो हर कोई देखता है
दूसरों को बताने के लिए.

Multiplier

2 bit multiplier

$A \longrightarrow$		A_1	A_0
$B \longrightarrow$		B_1	B_0
	C_0	A_1B_0	A_0B_0
	A_1B_1	A_0B_1	$\times$
C_1	S_2	S_1	S_0
P_3	P_2	P_1	P_0



"सोचने से मिलते नहीं
तमन्नाओं के शहर मंज़िल को
पाने के लिए चलना भी
जरूरी है"

$f = A + BC$

NAND = ?

NOR = ?

8:00AM

4P


THANK
YOU!

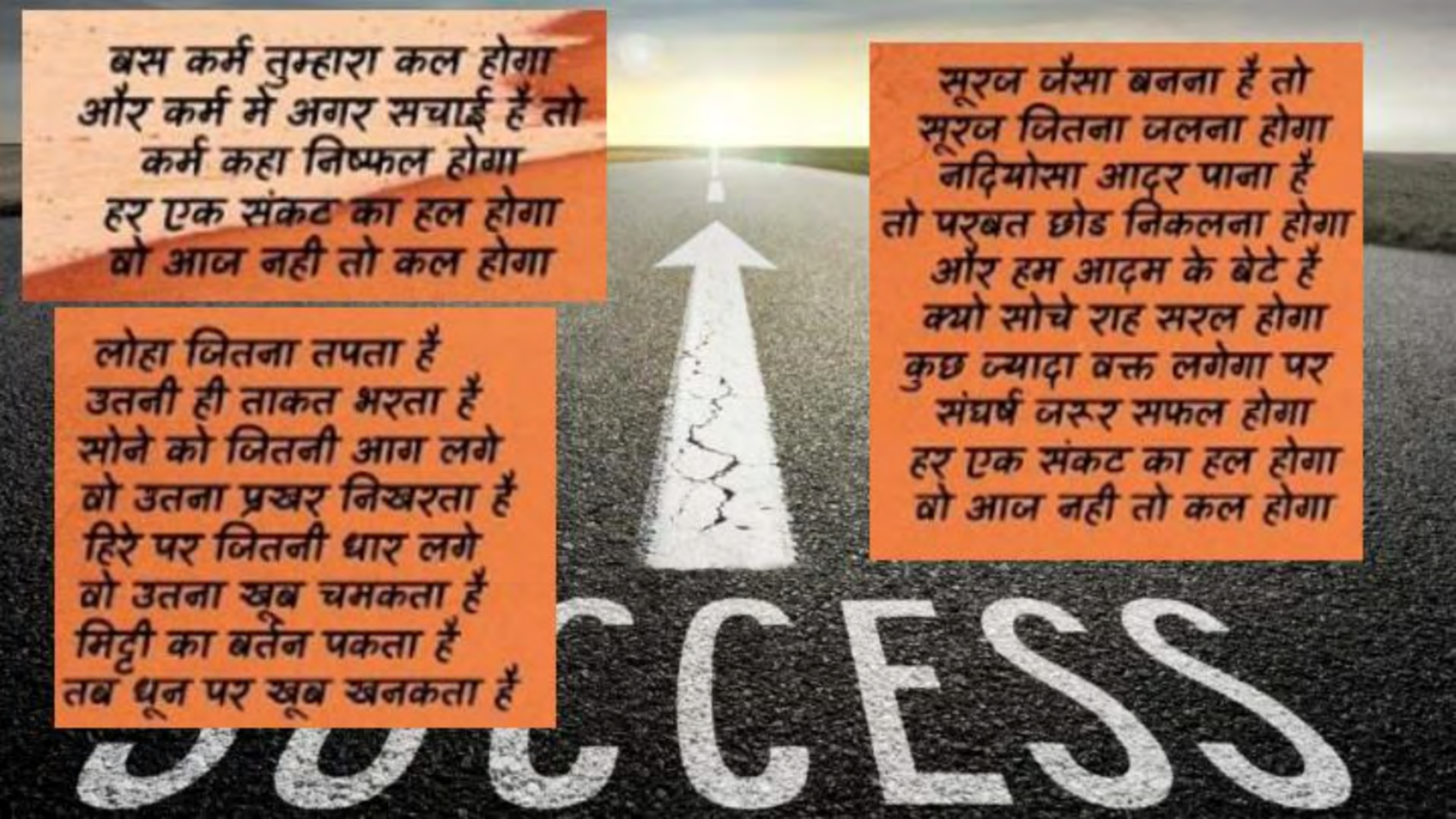
EC/EE/CS & IT/IN

Digital Electronics

Combinational circuit - Parallel Adder

LECTURE NO. 6

Chandan Jha Sir (CJ Sir)


बस कर्म तुम्हारा कल होगा
और कर्म मे अगर सचाई है तो
कर्म कहा निष्फल होगा
हर एक संकट का हल होगा
वो आज नही तो कल होगा
लोहा जितना तपता है
उतनी ही ताकत भरता है
सोने को जितनी आग लगे
वो उतना प्रखर निखरता है
हिरे पर जितनी धार लगे
वो उतना खूब चमकता है
मिट्टी का बर्तन पकता है
तब धून पर खूब खनकता है
सूरज जैसा बनना है तो
सूरज जितना जलना होगा
नदियोसा आदर पाना है
तो परबत छोड निकलना होगा
और हम आदम के बेटे है
क्यो सोचे राह सरल होगा
कुछ ज्यादा वक्त लगेगा पर
संघर्ष जरूर सफल होगा
हर एक संकट का हल होगा
वो आज नही तो कल होगा
CCESS

QUESTION

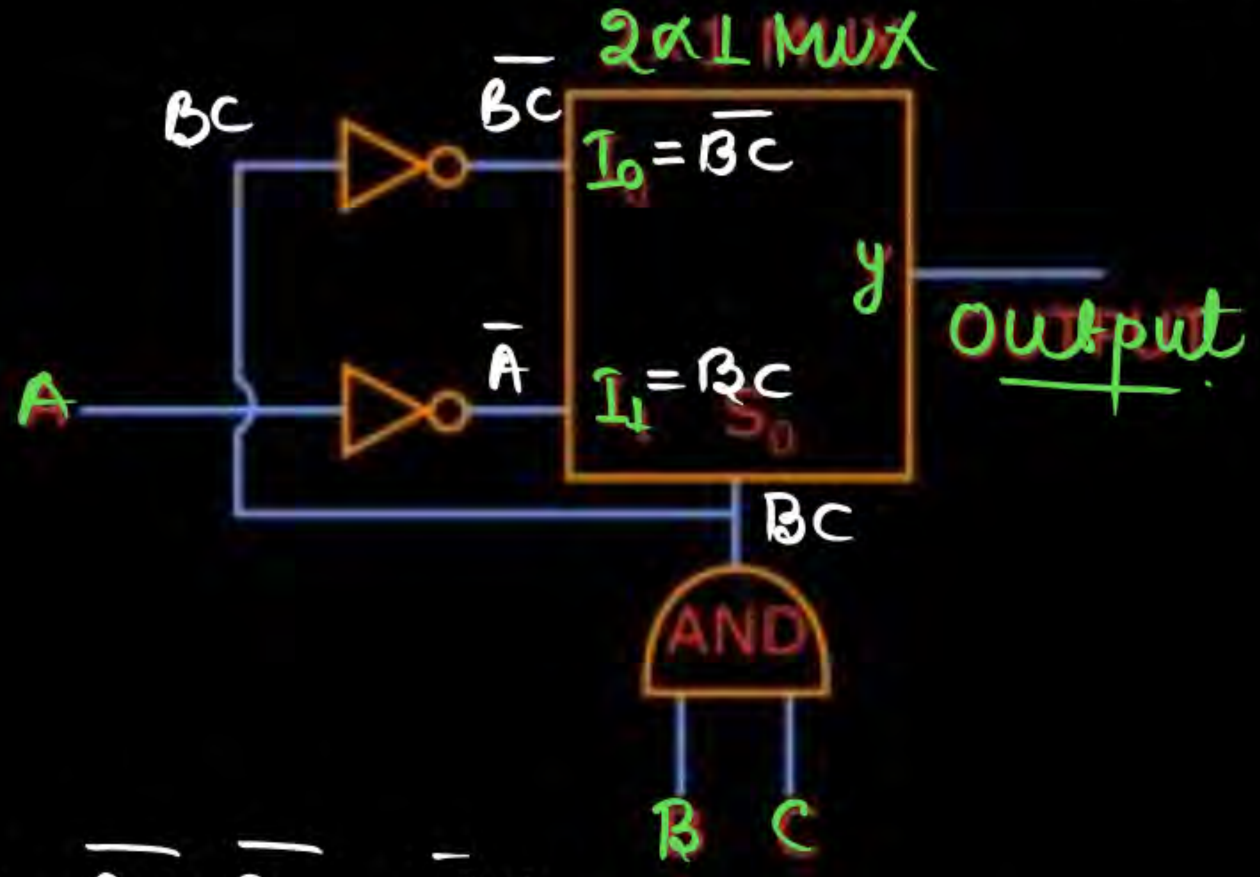
The combinational circuit given below implements which of the following

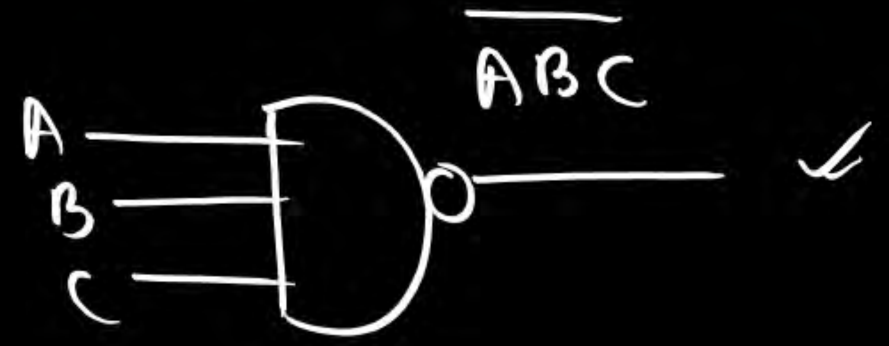
A. NAND

B. NOR

C. X OR

D. NONE





$$y = \overline{BC} \cdot \overline{BC} + \bar{A}BC$$

$$= \overline{BC} + \bar{A}BC \qquad BC = X$$

$$= \bar{X} + \bar{A}X = (\bar{A} + \bar{X})(\bar{X} + X)$$

$$= \bar{A} + \bar{X}$$

$$= \overline{A \cdot X} = \overline{A \cdot BC}$$

QUESTION

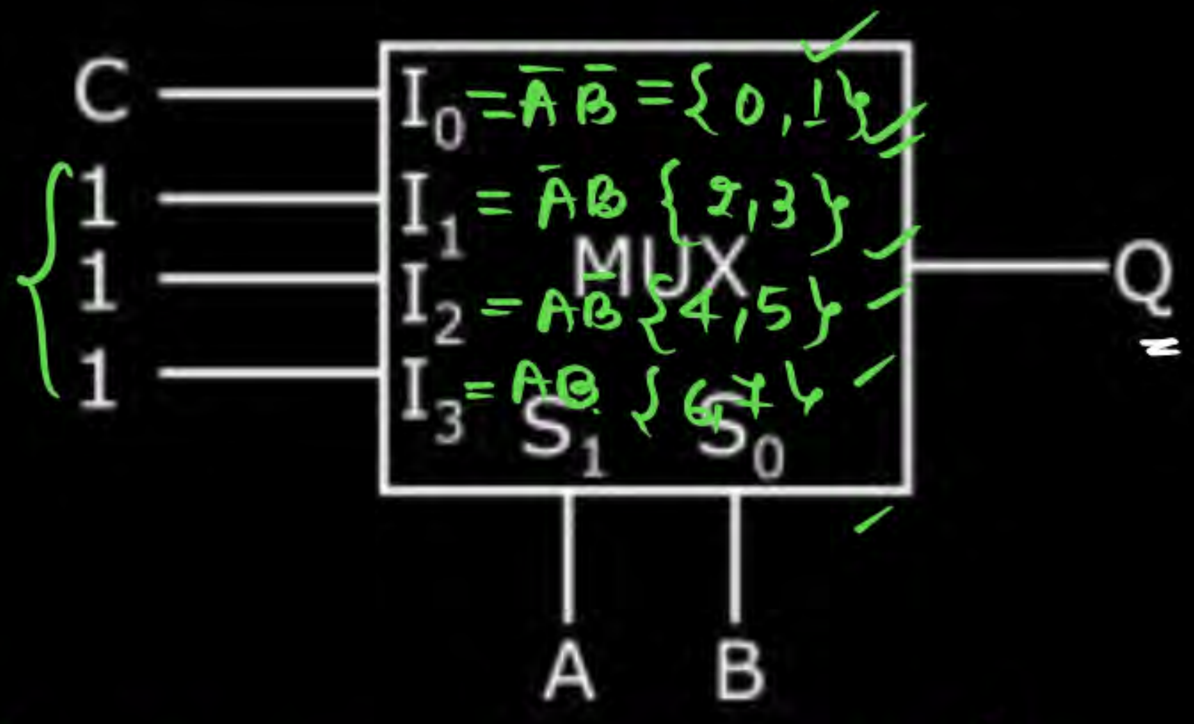
The combinational circuit given below, output Q will be

A. $A \oplus B \oplus C$

B. ABC

C. AB+C

D. A+B+C



$Q = \bar{A}\bar{B}C + \bar{A}B + A\bar{B} + AB$

$Q = \Sigma m(1,2,3,4,5,6,7)$

A \ BC	00	01	11	10
0	0	1	1	1
1	1	1	1	1

$B+C$

$A+B+C$

$A+B+C$

QUESTION

In 8 bit comparator total number of combination will be

A. 128K

B. 64K

C. 32K

D. none

'n' bit comparator

2^{2n}

$2^{2\times 8} = 2^{16} \Rightarrow 2^{6} \cdot 2^{10}$

$\Rightarrow 64K$

$2^{10} = K$

$2^{20} = M$

$2^{30} = G$

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- Cleared Gate Multiple times with double Digit Rank (AIR 23, AIR 26)
- Qualified ISRO Exam
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- More then 250+ Motivational Seminar in various Engineering College including NITs & Some of IITs

Chandan Jha

RECAPE

Comparator

n bit comparator

$T.C = 2^{2n}$

Equal $\Rightarrow 2^n$

Unequal com $\Rightarrow 2^{2n} - 2^n$

Greater $=$ Less $= \dfrac{2^{2n} - 2^n}{2}$

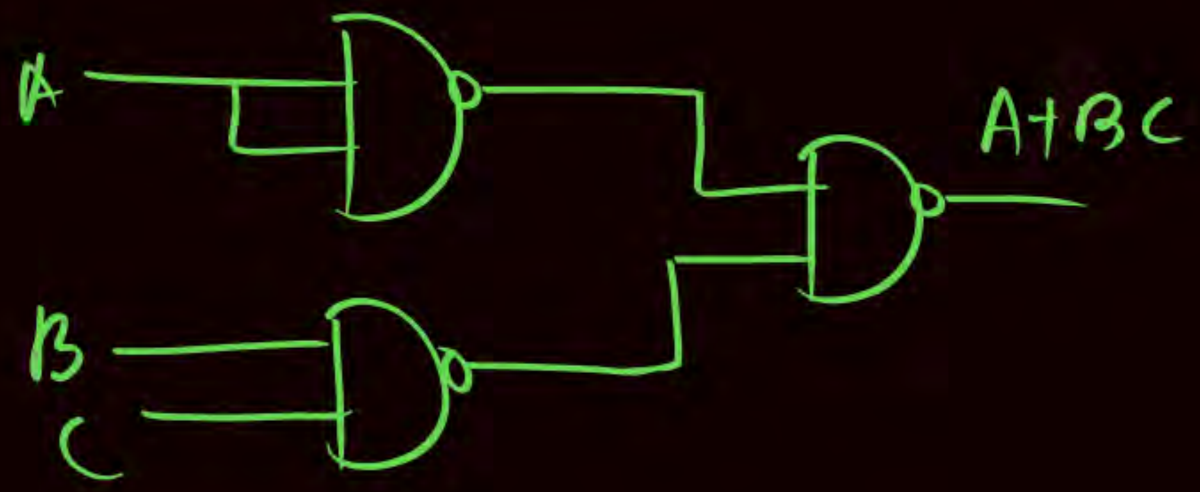
Semiminimized Expression

$A>B$: $A_1\overline{B_1} + (A_1 \odot B_1) A_0 \overline{B_0}$

$A<B$: $\overline{A_1} B_1 + (A_1 \odot B_1) \overline{A_0} B_0$

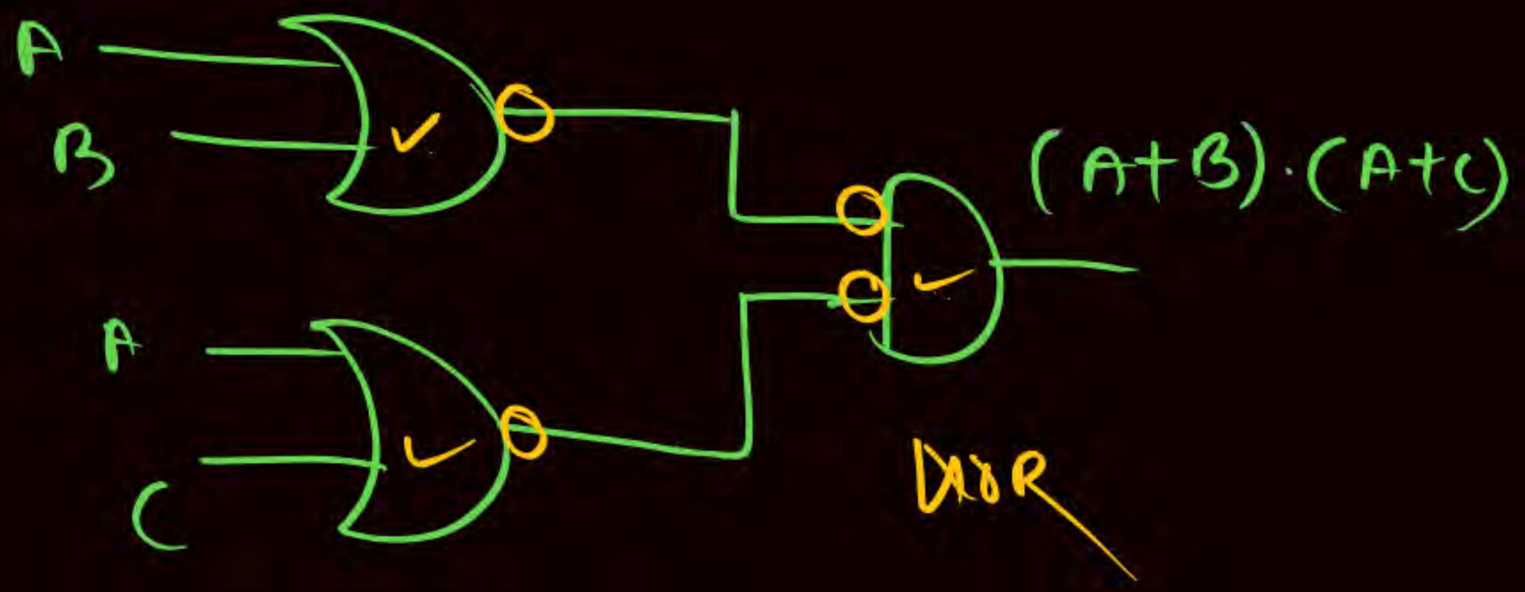
$A=B$: $(A_1 \odot B_1)(A_0 \odot B_0)$

$\underline{A+BC}$



3

$$A+BC = (A+B)(A+C)$$



3

HALF ADDER

→ 2 bit adder

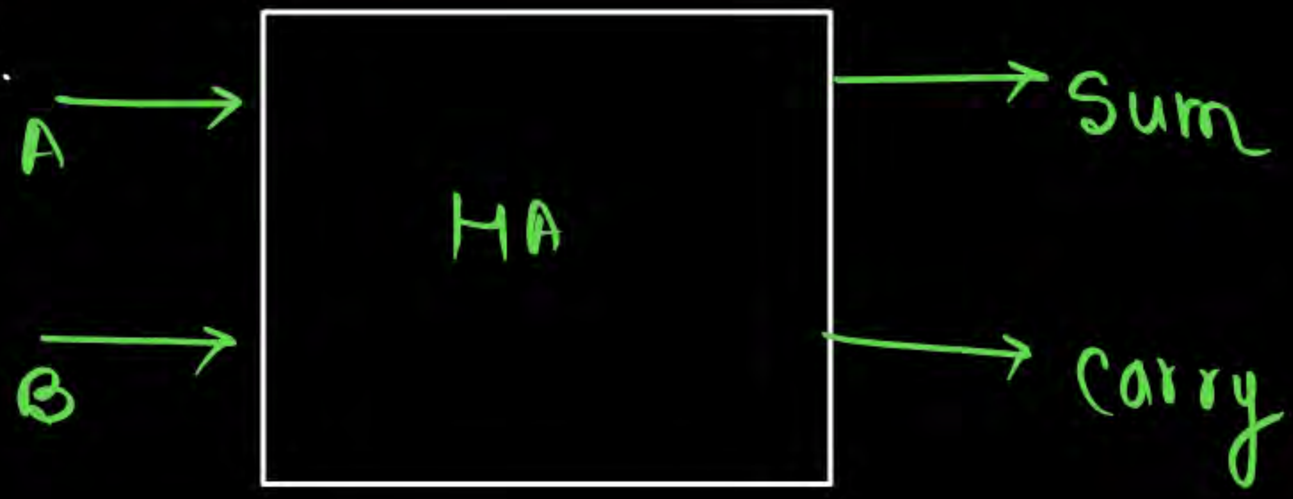
$$\begin{array}{r} 0 \\ +\ 0 \\ \hline 0\ 0 \end{array} \qquad \begin{array}{r} 0 \\ +\ 1 \\ \hline 0\ 1 \end{array} \qquad \begin{array}{r} 1 \\ +\ 0 \\ \hline 0\ 1 \end{array} \qquad \begin{array}{r} 1 \\ +\ 1 \\ \hline 1\ 0 \end{array} \qquad \begin{array}{r} 1 \\ 1 \\ \hline 1\ 0 \end{array}$$

Carry Sum

Carry Sum

HALF ADDER

Step-1.



Step-2.

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Step 3.

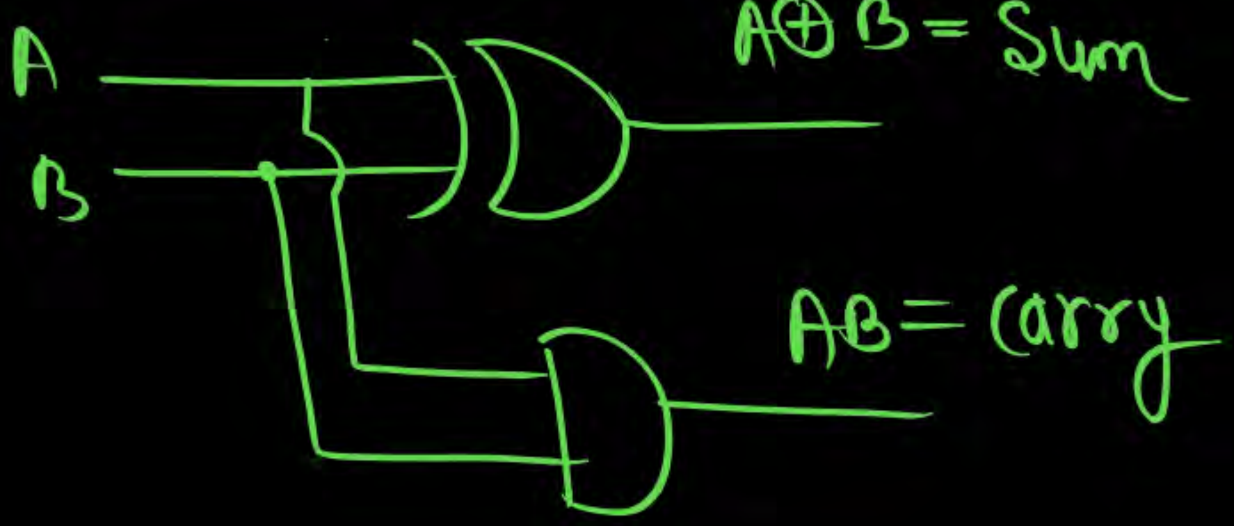
$$Sum = \bar{A}B + A\bar{B} = A \oplus B$$

$$Carry = AB$$

Step 4.

~~6~~ 5

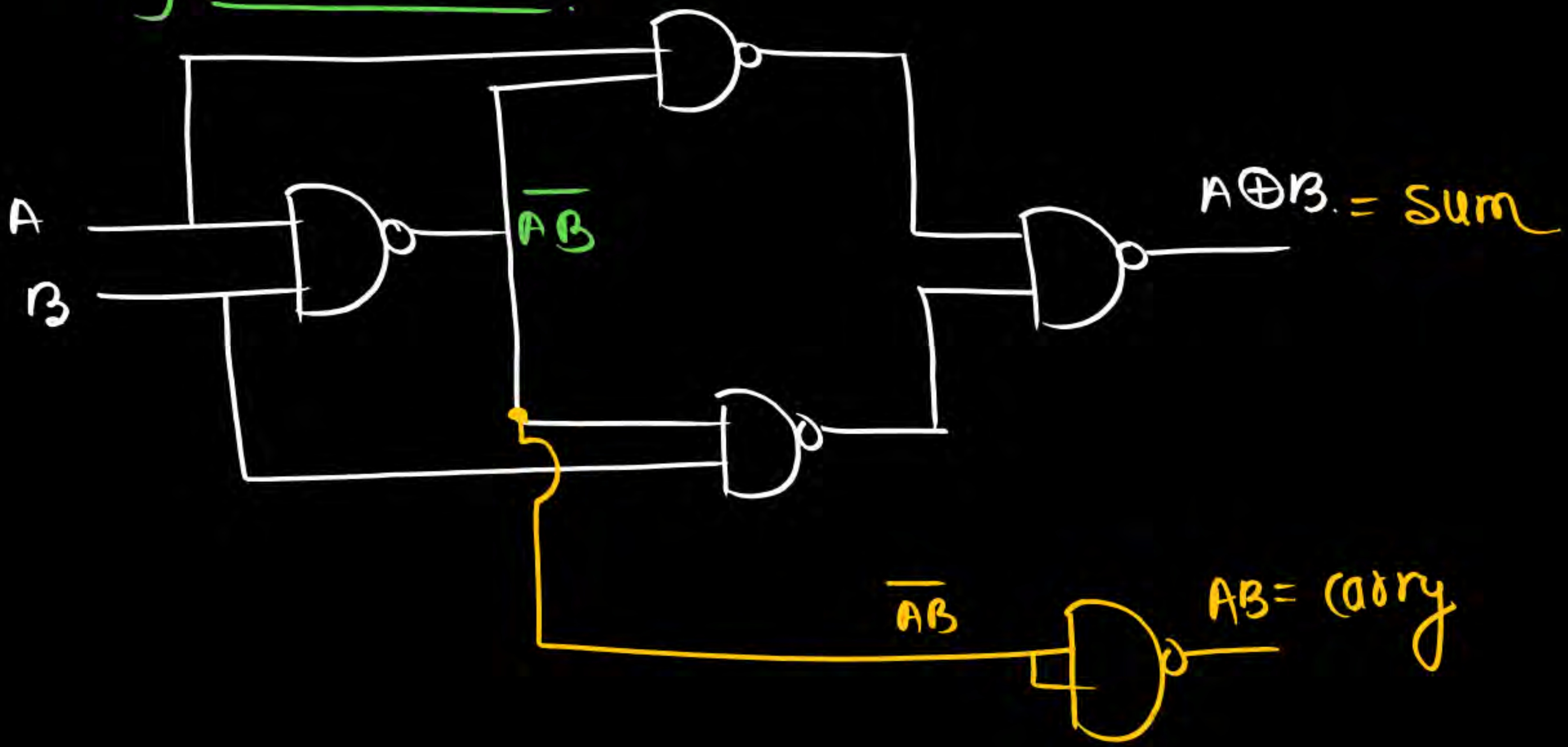
Step 5.



HALF ADDER

By NAND GATE

5



NOR

5

FULL ADDER

Step. 2.

	A	B	C	Sum	Carry
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1 ✓
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

Step 3. & Step 4

$$\text{Sum} = \Sigma m(1,2,4,7) = A \oplus B \oplus C$$

$$\text{Carry} = \Sigma m(3,5,6,7)$$

$$= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$= (\bar{A}B + A\bar{B})C + AB(\bar{C} + C)$$

$$= AB + (A \oplus B) \cdot C$$

seminimized

A \ BC	00	01	11	10
0	.	.	1	.
1	.	1	1	1

$$= AB + BC + AC$$

HALF ADDER/SUBTRACTOR

NAND/NOR

$Sum = A \oplus B$

$Carry = AB$

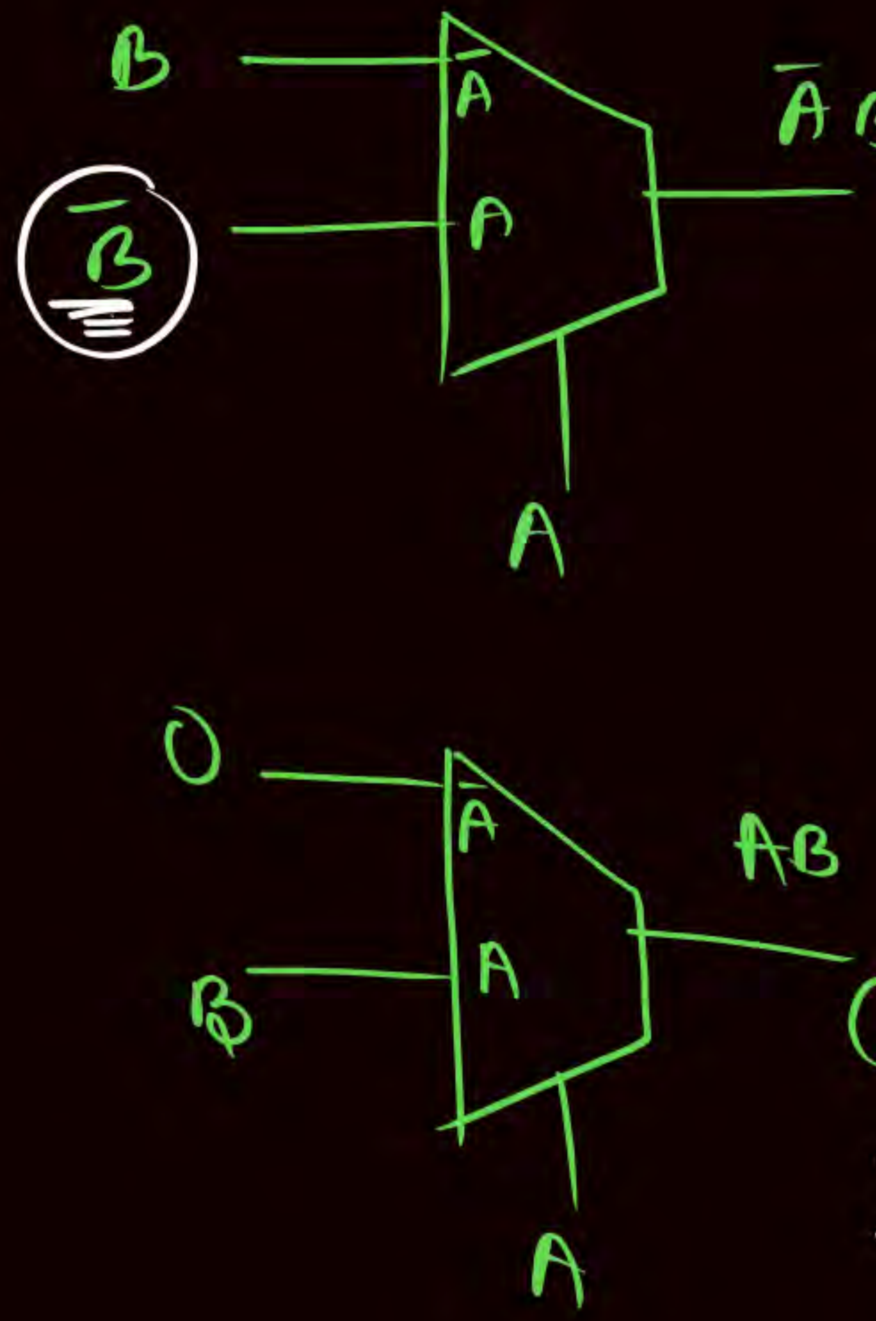
5

D+

2x1 MUX

?

HALF ADDER



$\bar{A}B + A\bar{B} = A \oplus B$

Sum

2

3

AB

Carry

1

FULL ADDER

→ 3bit adder

$$\begin{array}{r} 0 \\ 0 \\ 0 \\ \hline 0\ 0 \end{array} \qquad \begin{array}{r} 0 \\ 0 \\ +\ 1 \\ \hline 0\ 1 \end{array} \qquad \begin{array}{r} 0 \\ 1 \\ +\ 1 \\ \hline 1\ 0 \end{array} \qquad \begin{array}{r} 1 \\ 1 \\ +\ 1 \\ \hline 1\ 1 \end{array}$$

carry sum

step 1

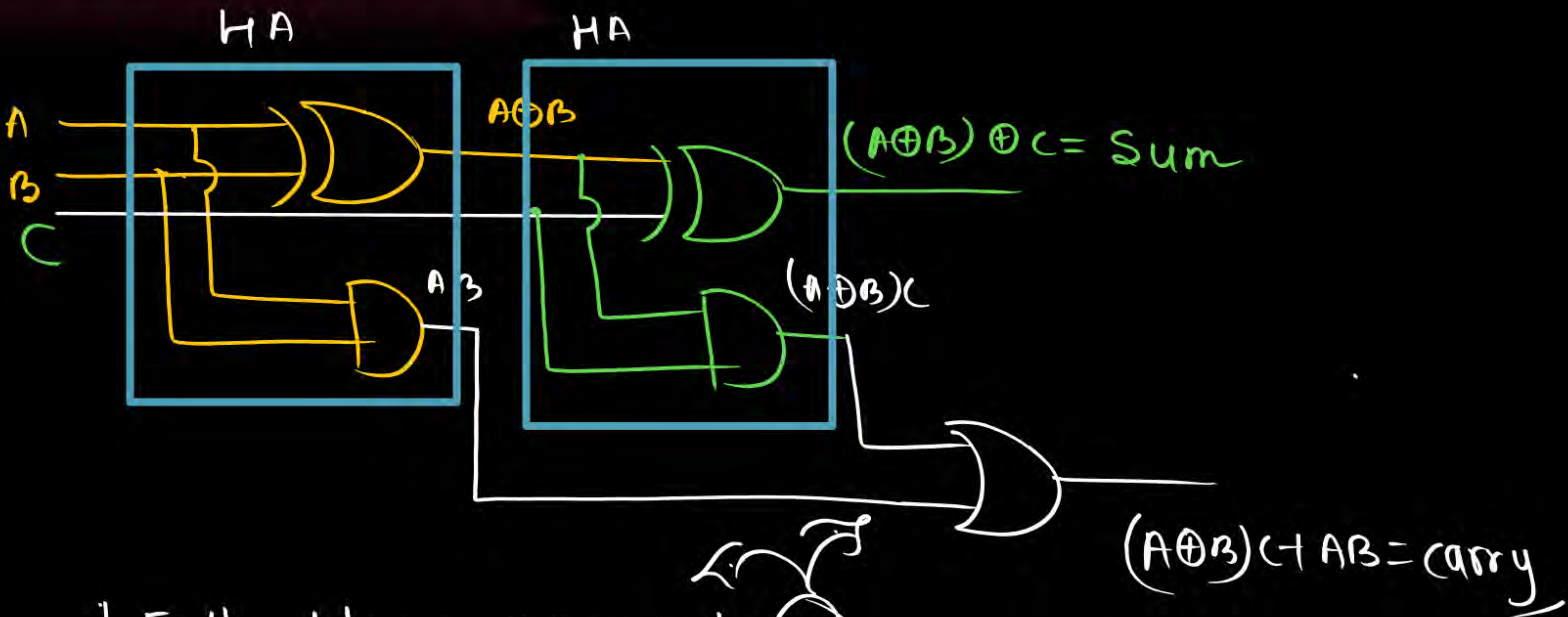
Full adder

ER.CJHA@GMAIL.COM

✓ $Sum = A \oplus B \oplus C$

$$
\begin{aligned}
Carry &= AB + BC + AC \\
&= (A \oplus B)C + AB \\
&= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC
\end{aligned}
$$

FULL ADDER



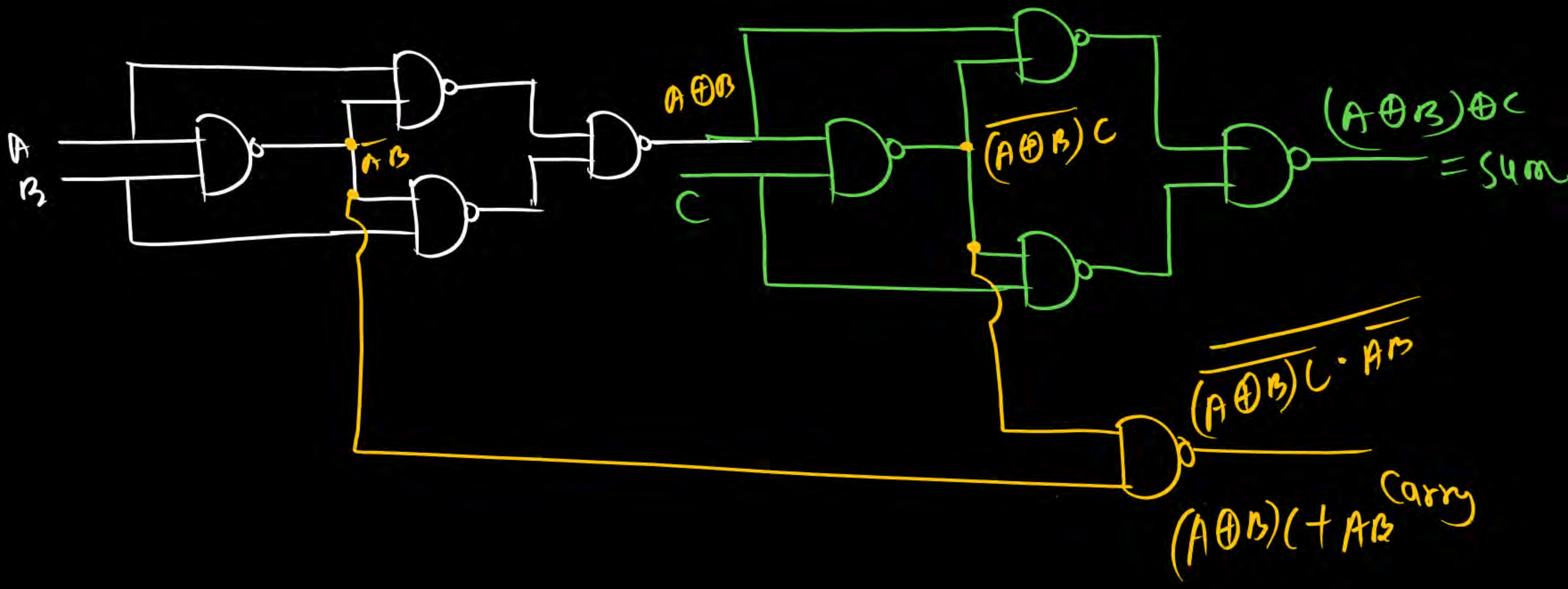
1 Full adder = 2HA + 1

GATE

BINOD

FULL ADDER

→ Number of NAND = 9



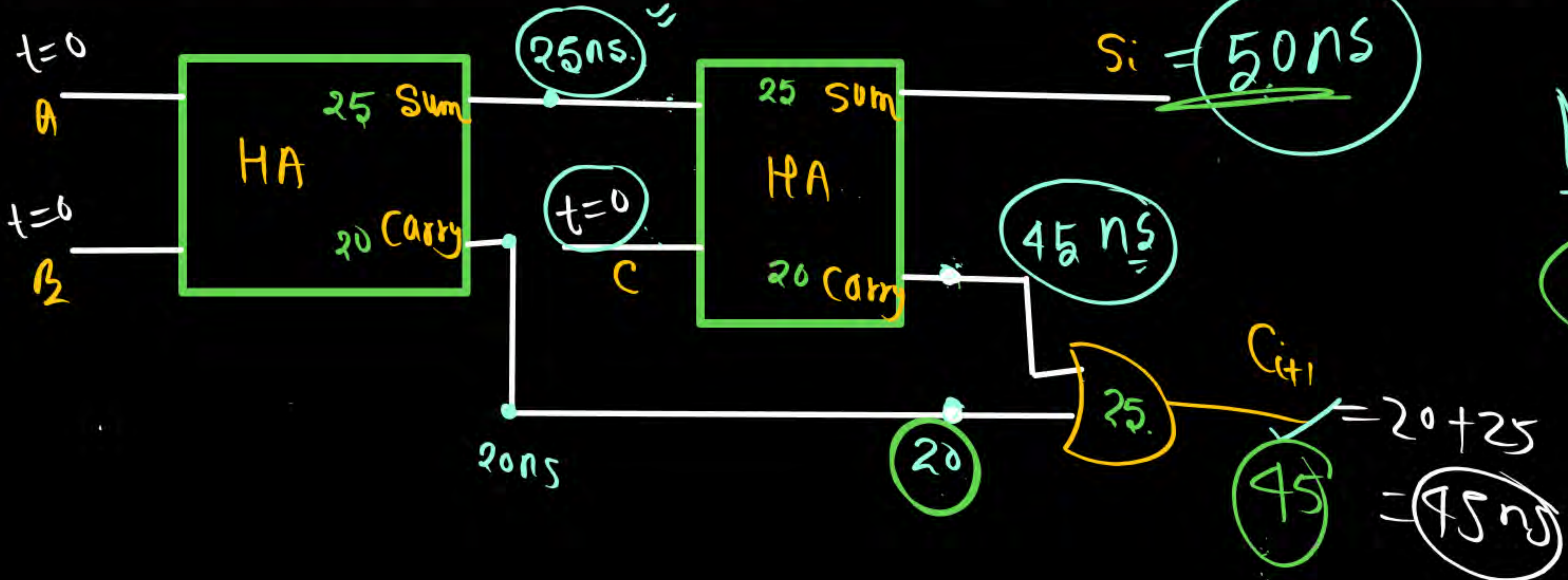
QUESTION

$T_{sum} = 50ns$ $T_{carry} = 45\ ns$

A full adder is implemented with two half adders and one OR gate. OR gate is used to derive the final carry function of full adder. In each half adder, $\boxed{T_{sum} = 25ns}$ and $\boxed{T_{carry} = 20ns}$ and $\boxed{T_{OR} = 25ns.}$ The minimum time required to derive both the sum and carry function of a full adder after applying the inputs is ______ ns

Maximum Time

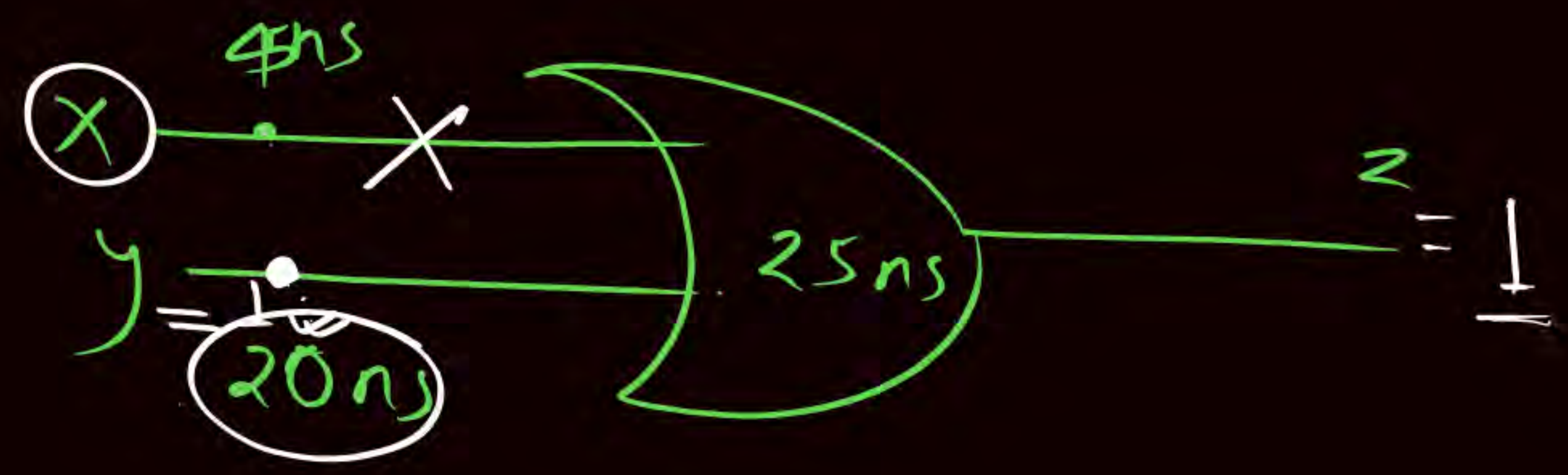
70ns



Minimum Time

20+25=45ns

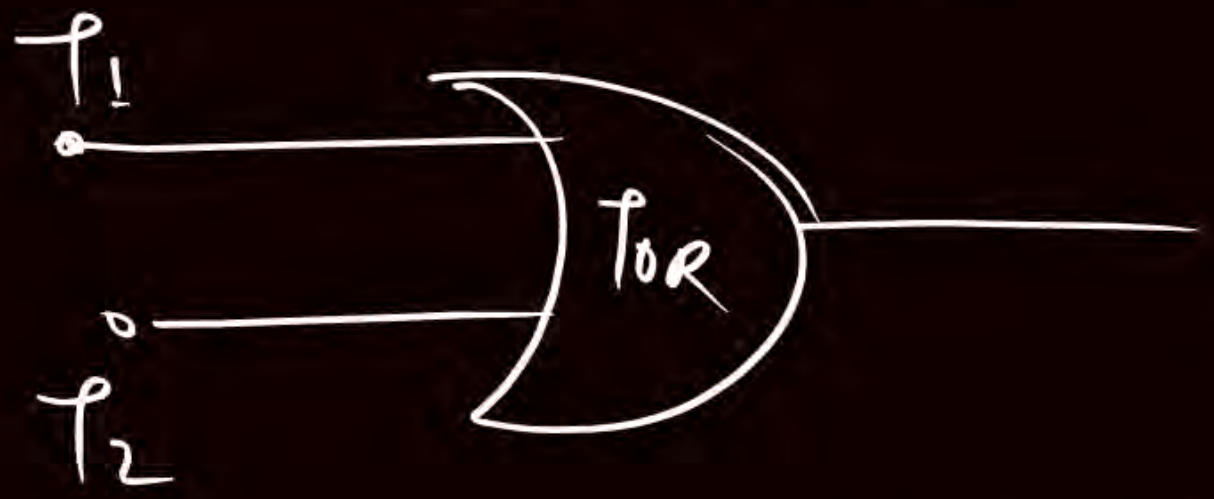
50ns



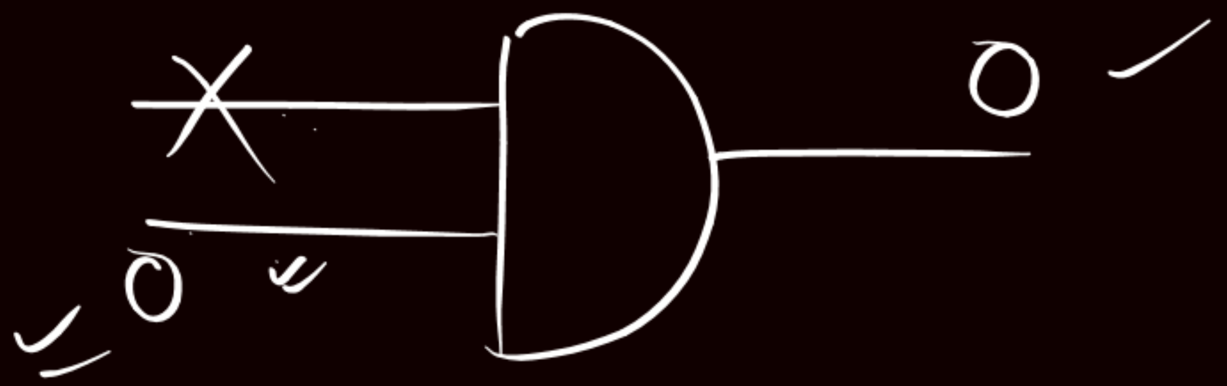
minimum Delay

#DECJ

min delay



Minimum Delay $= \text{Min}\{T_1, T_2) + T_{OR}$


0
0

Jorden

"PARALLEL ADDER"

4 bit parallel adder

FA

HA

$$
\begin{array}{ccccc}
 & C_3 & C_2 & C_1 & \\
 & A_3 & A_2 & A_1 & A_0 \\
+ & B_3 & B_2 & B_1 & B_0 \\
\hline
C_4 & S_3 & S_2 & S_1 & S_0
\end{array}
$$

4 bit parallel adder

→ 3FA + 1 HA

★ → 7 HA + 3 OR GATE

→ 4 FA

n bit parallel adder

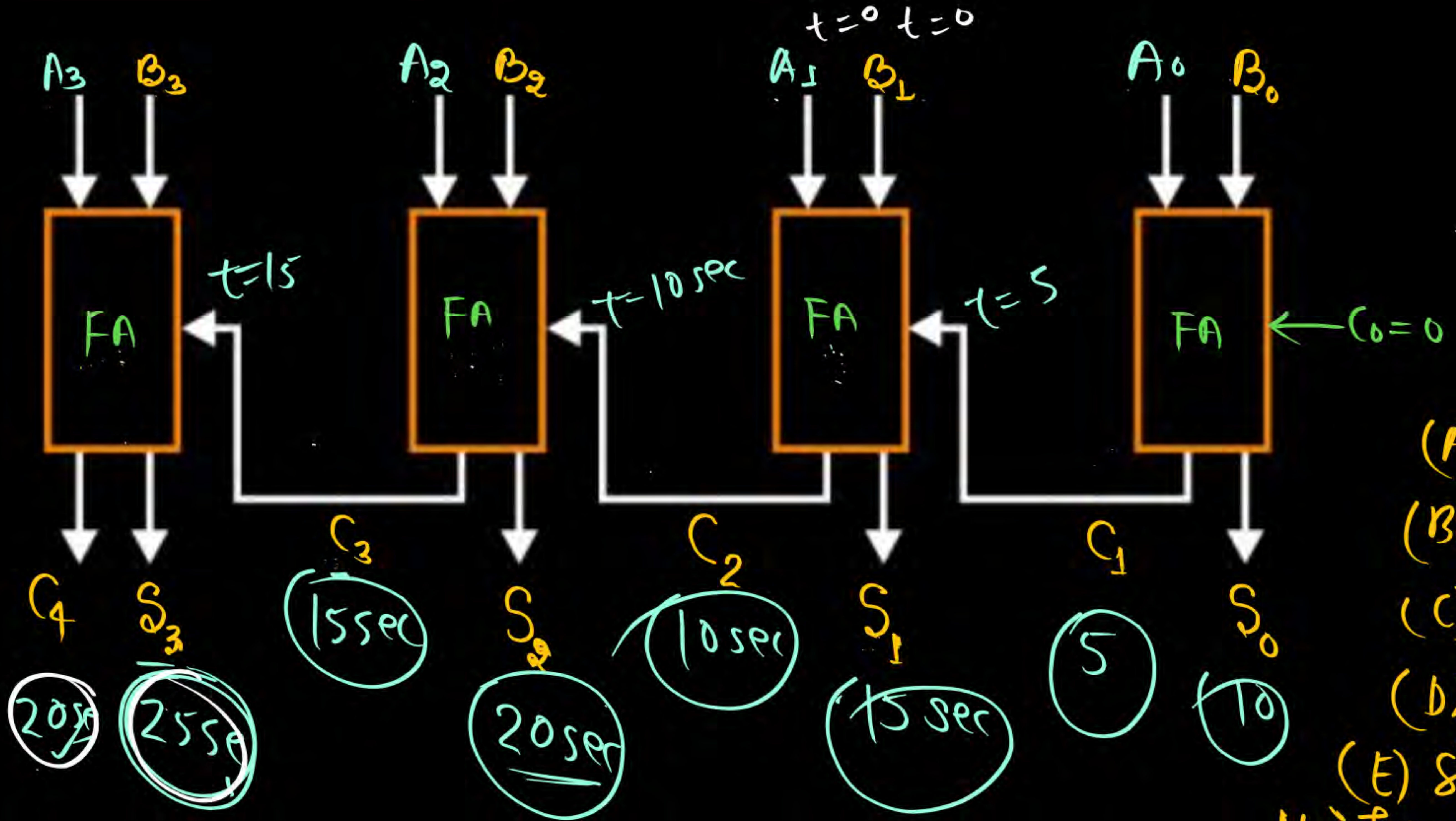
→ $(n-1)$ FA + 1 HA

→ $(2n-1)$ HA + $(n-1)$ OR

→ "n" FA

PARALLEL ADDER

RIPPLE CARRY ADDER



$T_{sum} = 10$ sec

$T_{carry} = 5$ sec

(A) 20

(B) 25

(C) 35

(D) 40

(E) Sir, Mujhe nahi aata. Mai Tare jameen par hu.

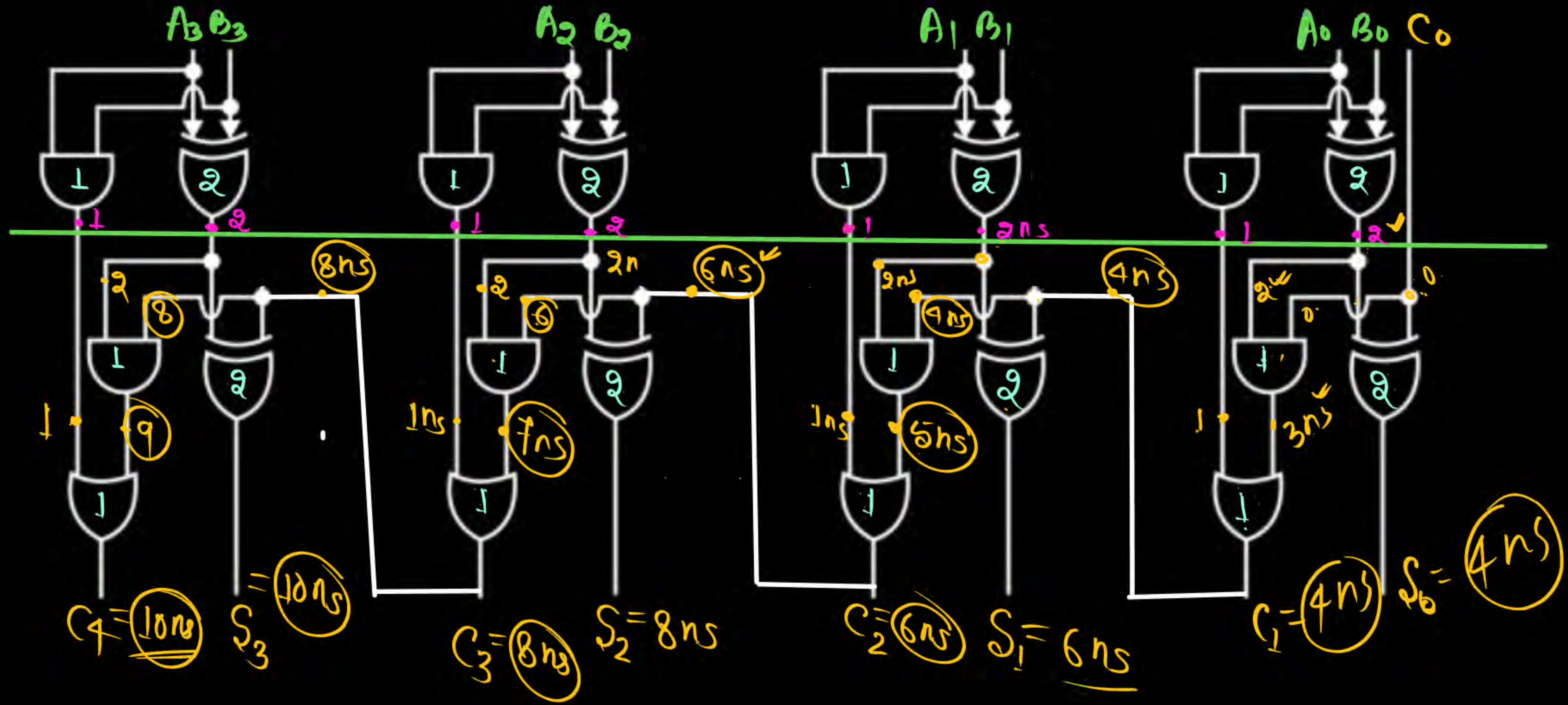
n bit Ripple carry adder

Maximum Delay

$$\boxed{T = (n-1)T_{carry} + \text{Max}\{T_{sum}, T_{carry}\}}$$

PARALLEL ADDER

X-OR → 2ns.
AND/OR → 1ns



Maximum Delay

$T_{AND}/T_{OR} = 1\,ns$
$T_{X\text{-}OR} = 2\,ns$

$T_{sum} = 4\,ns$
$T_{carry} = 4\,ns$

$$\boxed{T = (n-1)\{T_{AND} + T_{OR}\} + Max\{T_{sum}, T_{carry}\}}$$

$n \rightarrow$ no. of bits.

$$T = (4-1)\{1+1\} + Max\{4, 4\}$$
$$= 3 \times 2 + 4\ ns$$
$$= 10\,ns$$

QUESTION

A 16-bit ripple carry adder is realized using 16 identical full adders. The carry propagation delay of each full adder is 12 ns and the sum propagation delay of each full adder is 15 ns. The worst case delay of this 16 bit adder will be _____ ?

carry

sum

A. 195

B. 220

C. 250

D. NONE

$$T = (n-1)T_{carry} + \mathrm{Max}\{T_{sum}, T_{carry}\}$$

$$= (16-1) \cdot 12\,ns + \mathrm{Max}\{15\,ns, 12\,ns\}$$

$$= 15 \times 12 + 15$$

$$= \underline{195\,ns}$$

QUESTION

4-bit parallel binary adder is built using four full adders. If each full adder takes 44ns to produce the sum bit and 14ns to produce carry bit, then the time required for addition of two 4-bit numbers is.

A. 100

B. 86

C. 126

D. NONE

$T_{sum} = 44\,ns$

$T_{carry} = 14\,ns$

$n = 4$

$T = (n-1)T_{carry} + T_{sum}$

$= 3 \times 14 + 44$

$= 86\,ns$

QUESTION

PYQ

$T_{AND} / T_{OR} = 1.2\ \mu s$

$T_{XOR} = 2.4\ \mu s$

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple-carry binary adder is implemented by using full adders. The total propagation time of this 4-bit binary adder in microseconds is,

A. 19.2

B. 12

C. 25

D. NONE

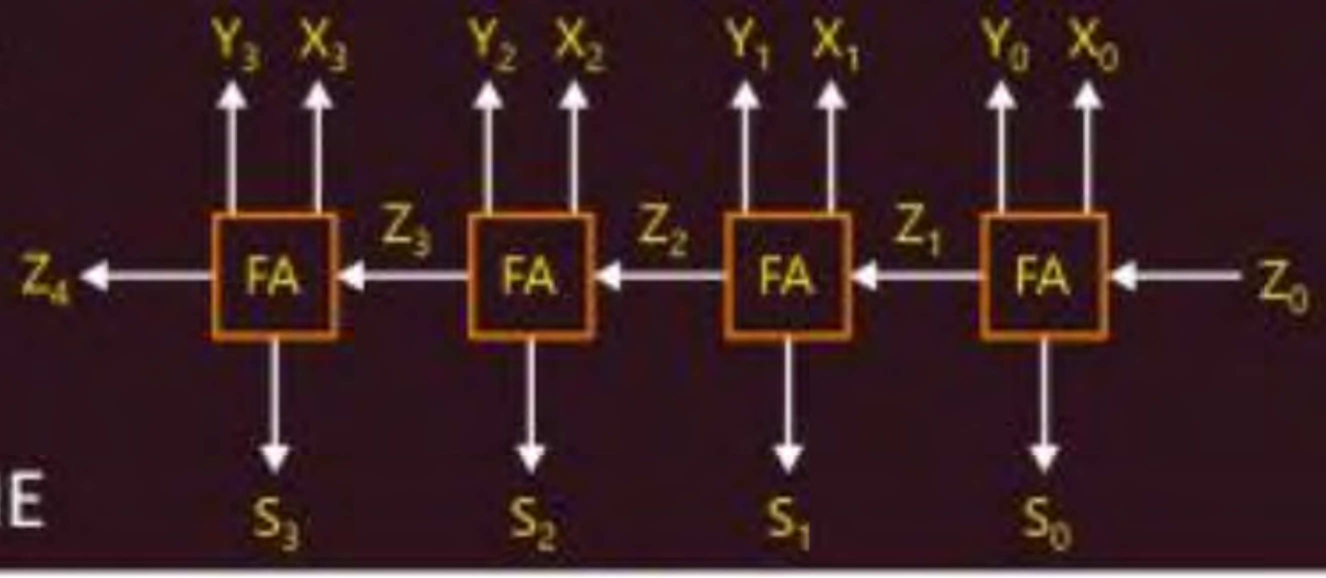


Figure-I

Figure-II

HW ?

$n = 4$ bit

$$\left\{ \begin{array}{l} t_{AND} = 3\,ns. \\ t_{OR} = 2\,ns \\ t_{X\cdot OR} = 5\,ns. \end{array} \right\}$$

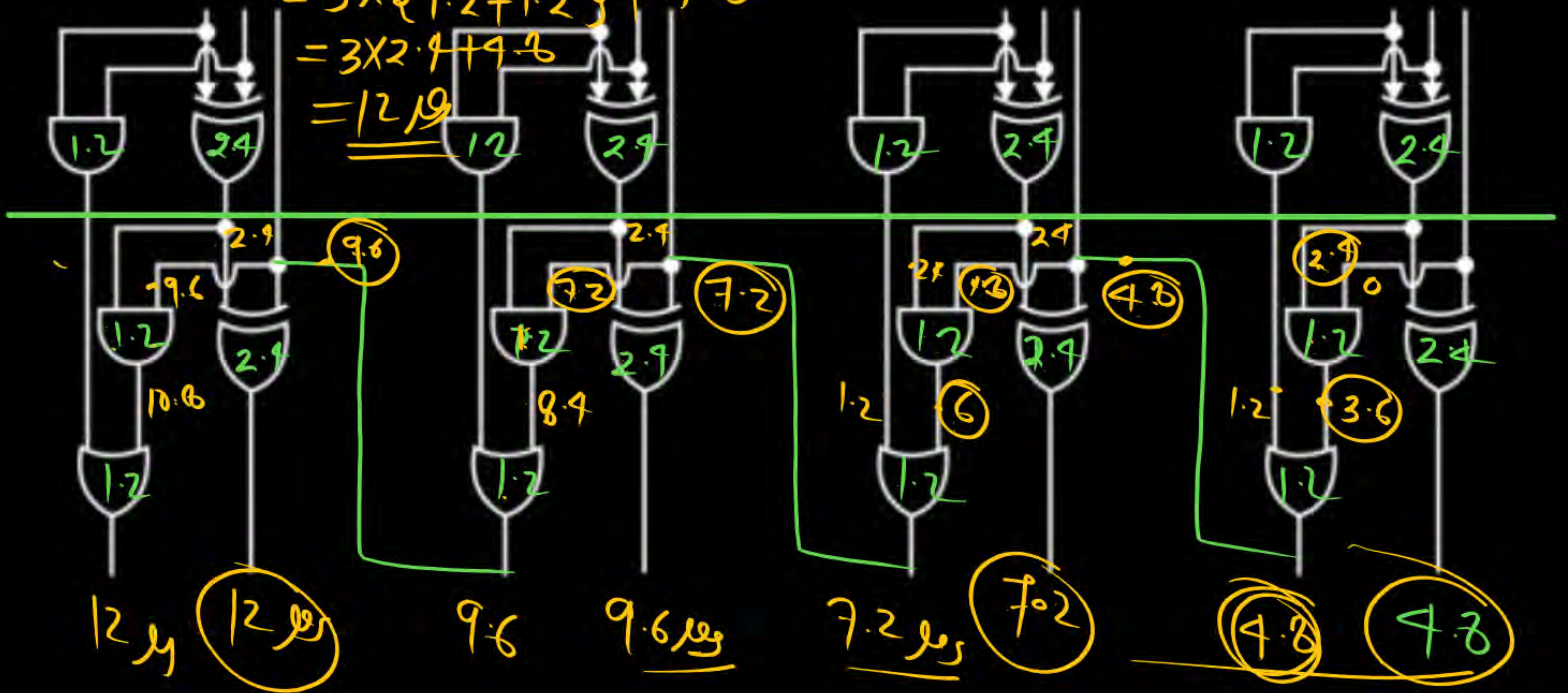
$$T = (n-1)\{T_{AND} + T_{OR}\} + \text{Max}\{\underbrace{T_{sum}, T_{carry}}_{}\}$$

4.8

$= 3 \times \{1.2 + 1.2\} + 4.8$

$= 3 \times 2.4 + 4.8$

$= 12\,ns$



QUESTION

HW.

Figure I show a 4-bits ripple carry adder realized using full adders and Figure II shows the circuit of a full-adder (FA). The propagation delay of the XOR, AND and OR gates in Figure II are 20 ns, 15 ns and 10 ns respectively. Assume all the inputs to the 4-bit adder are initially reset to 0.

At t=0, the inputs to the 4-bit adder are changed to

$X_3X_2X_1X_0 = 1100$, $Y_3Y_2Y_1Y_0 = 0100$,

And $Z_0 = 1$

The output of the ripple carry adder will be stable at t (in ns) = ______

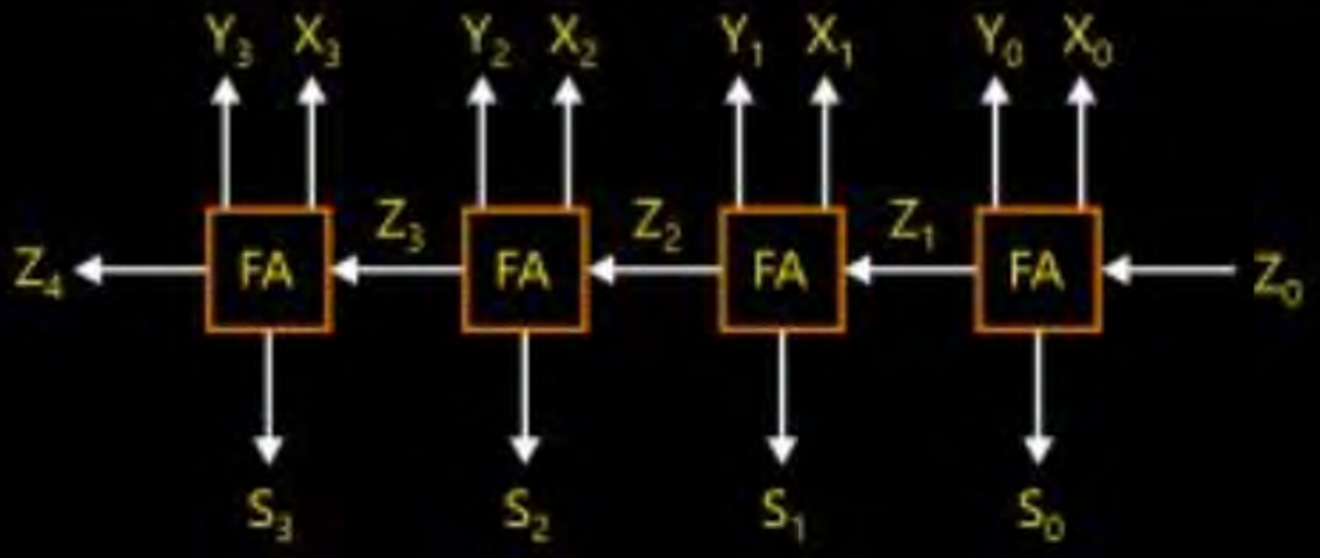


Figure-I

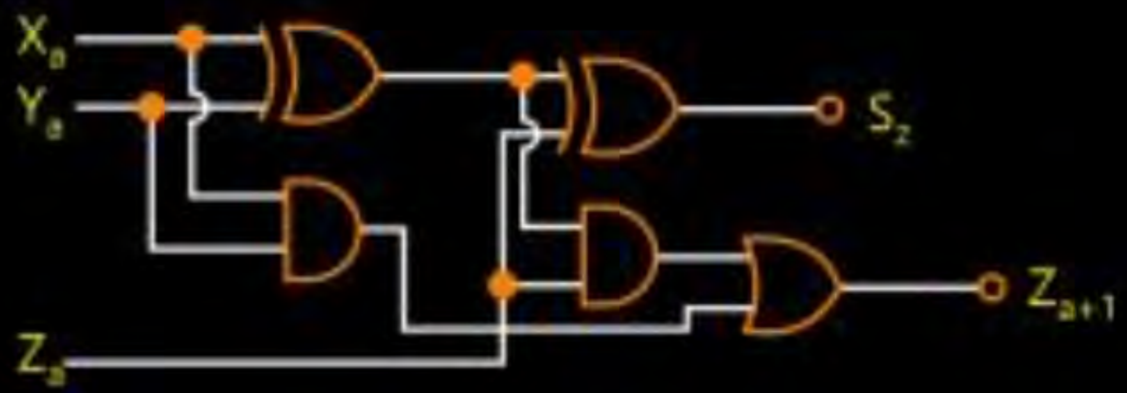
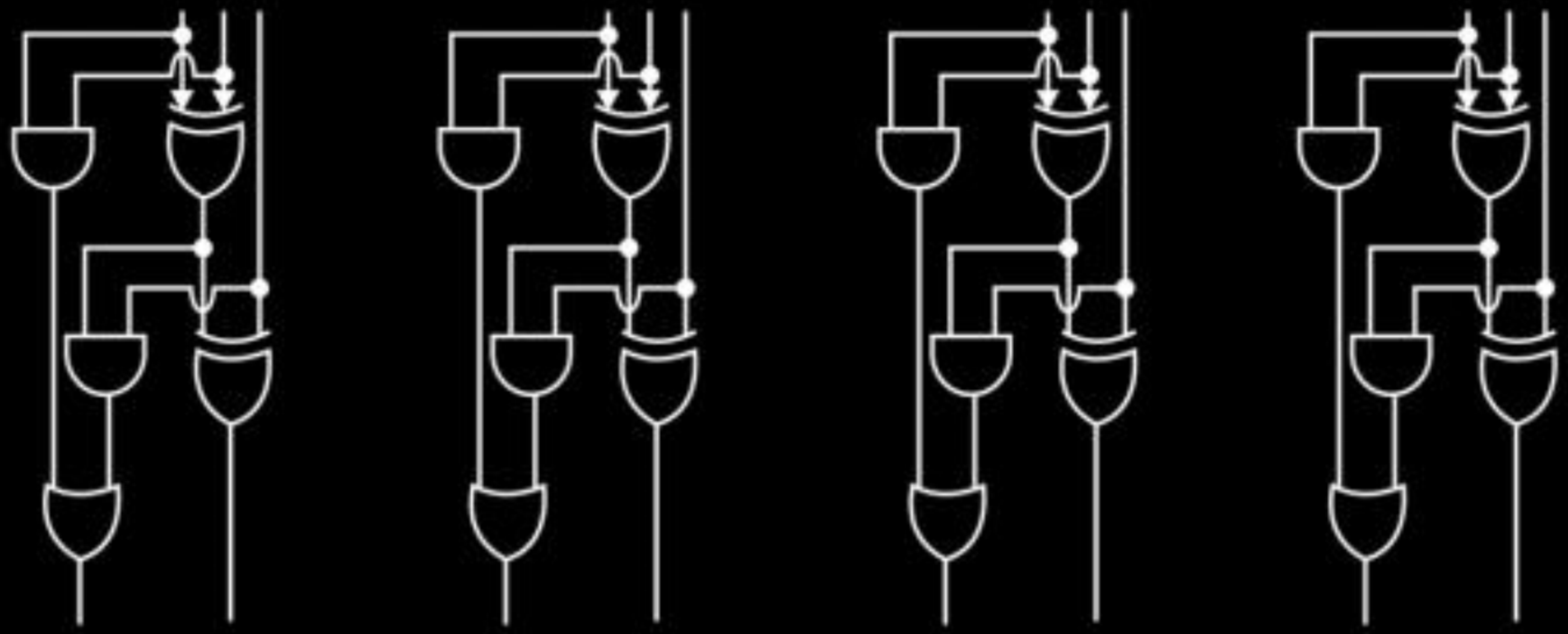


Figure-II




10 AM

ER.CJHA@GMAIL.COM

Digital Electronics

L-line

8:00 AM

EC/EE/CS & IT/IN

Digital Electronics

Latches & SR Flip Flops

LECTURE NO. 7

Chandan Jha Sir (CJ Sir)


निगाहों में मंज़िल थी, गिरे और
गिरकर सम्भालते रहे
हवाओं ने बहुत कोशिश की,
मगर चिराग़ अंशियाँ में भी
जलते रहे
SUCCESS

LATCHES & SR FF

SEQUENTIAL CIRCUIT

Latches | Registers
Flip-Flop | Counter

1. A circuit with feedback and memory are called sequential circuit.
2. Output of the sequential circuit depends on previous output as well as present state of input.

{ Dynamic circuit }

LATCHES & SR FF

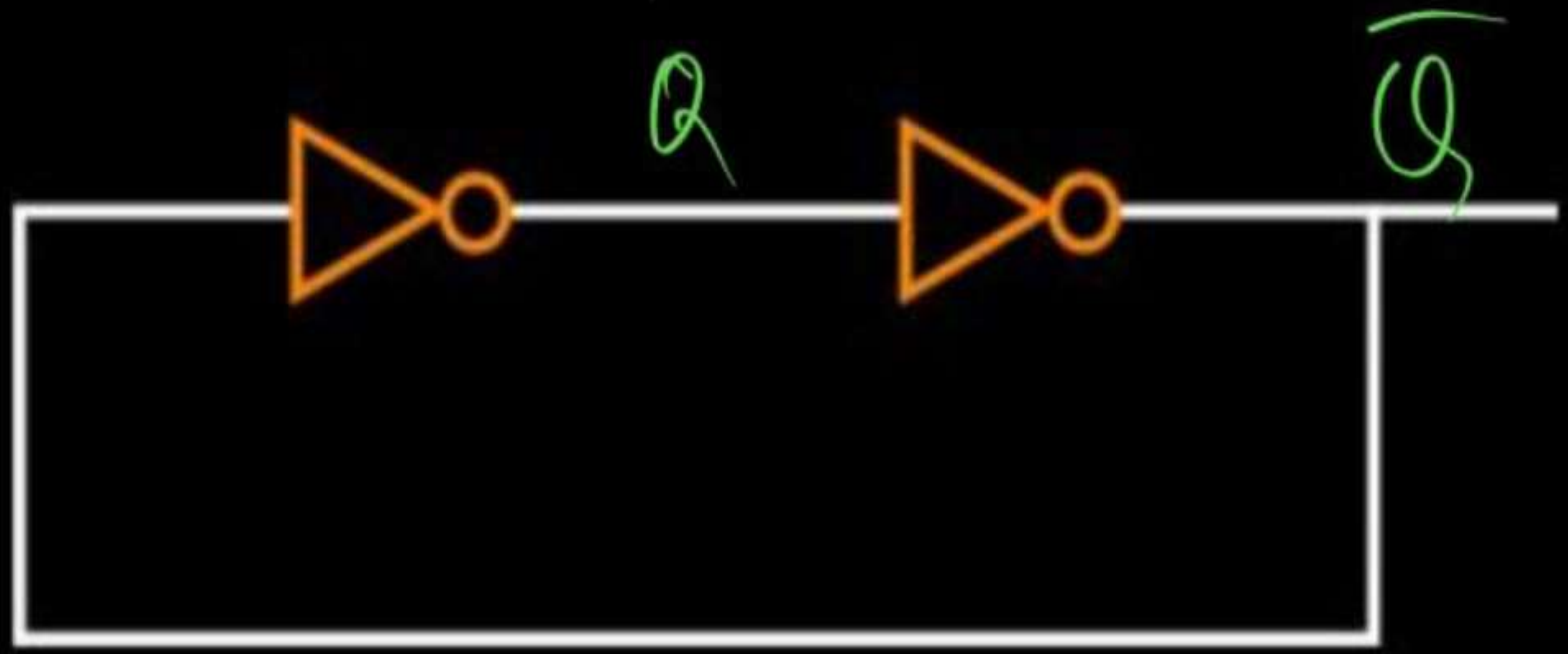
LATCHES

Even

- Basic memory element
- Latches are level triggered
- Latches has two output which is complement of each other

LATCHES & SR FF

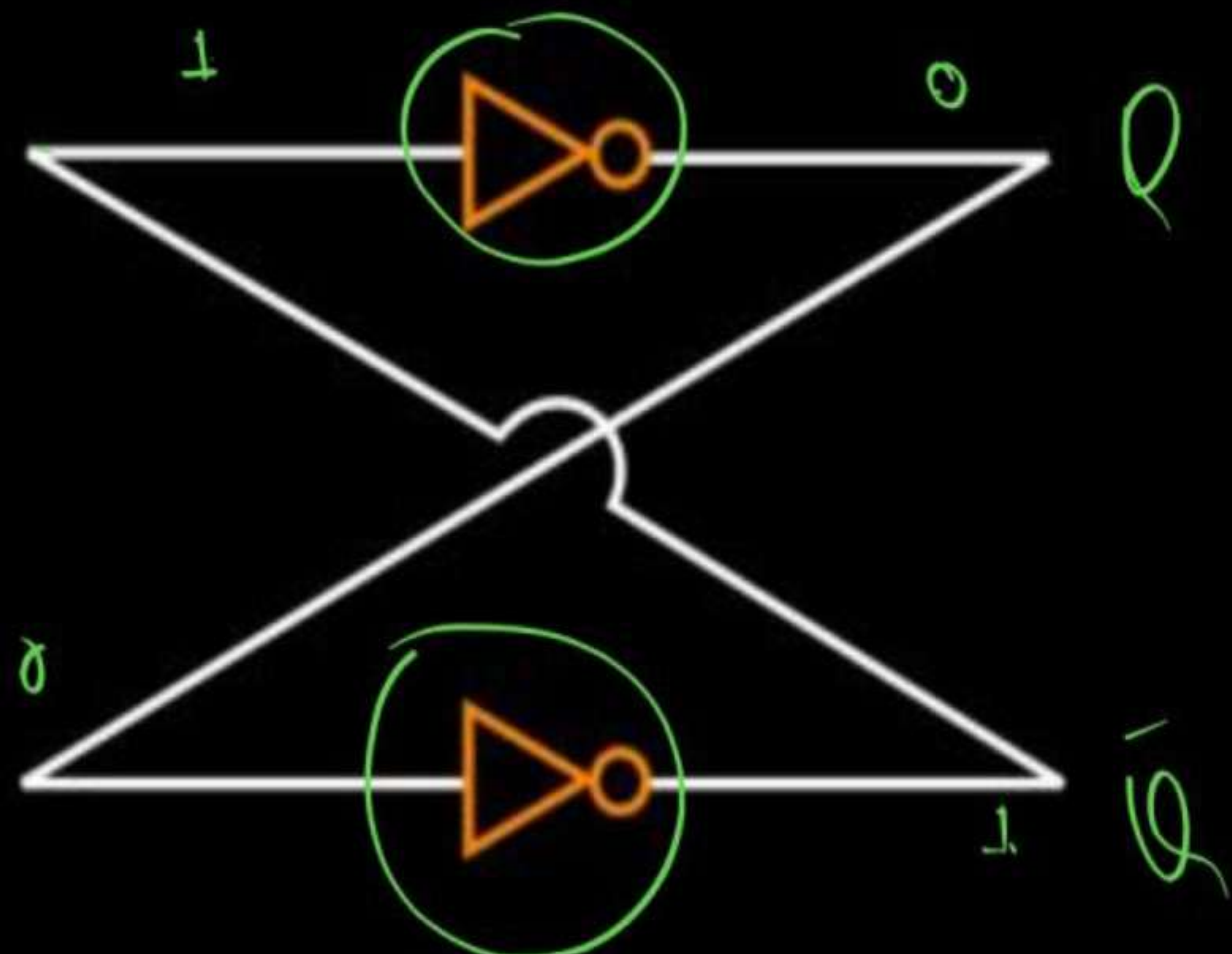
LATCHES



"Basic memory element"

LATCHES & SR FF

LATCHES

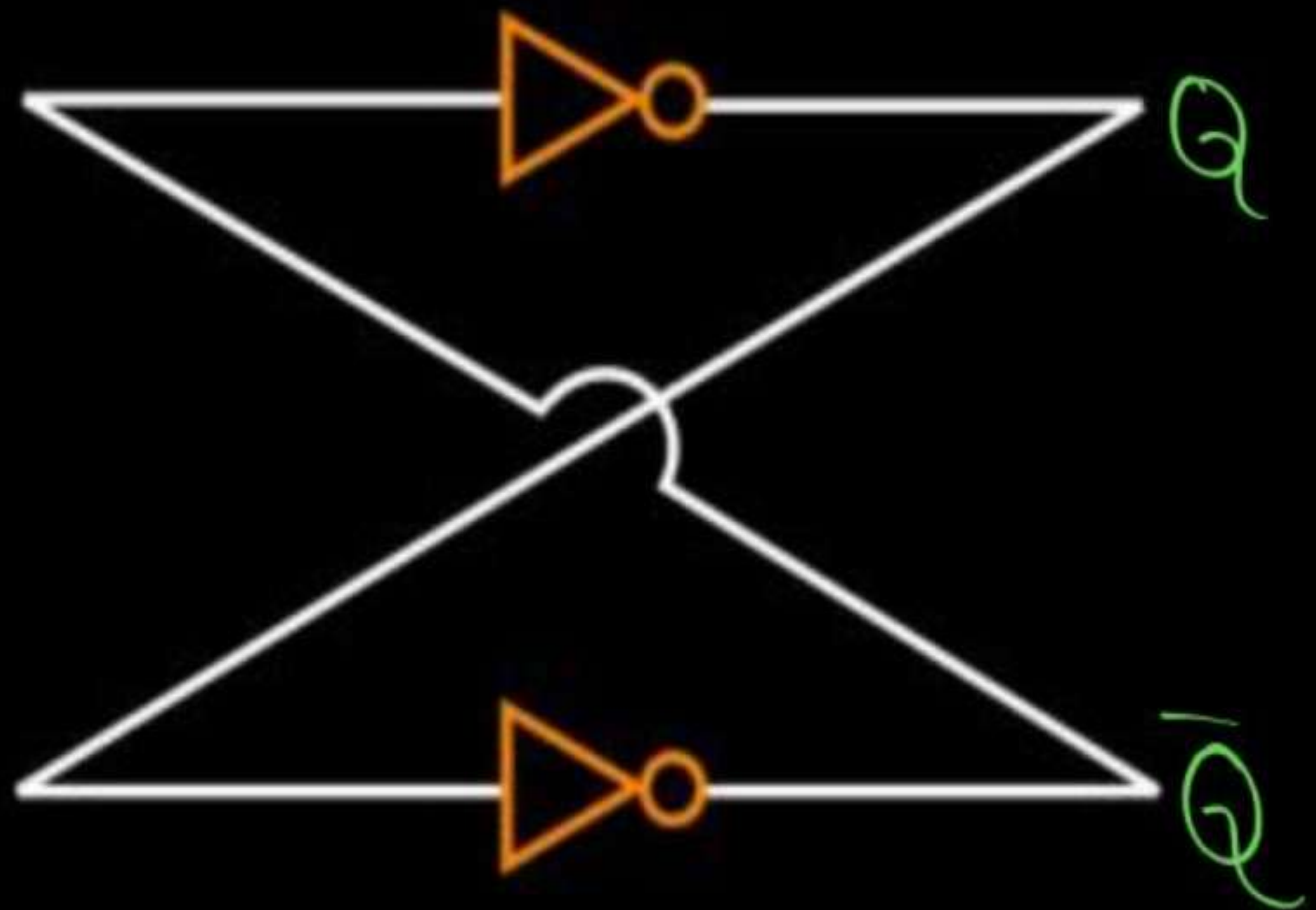


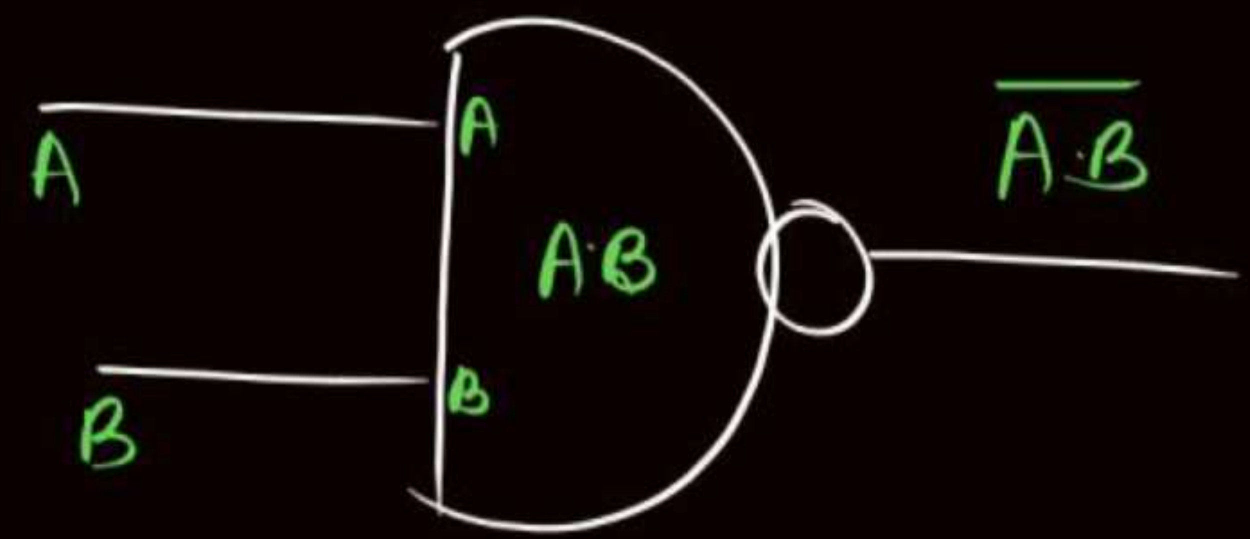
NAND

NOR

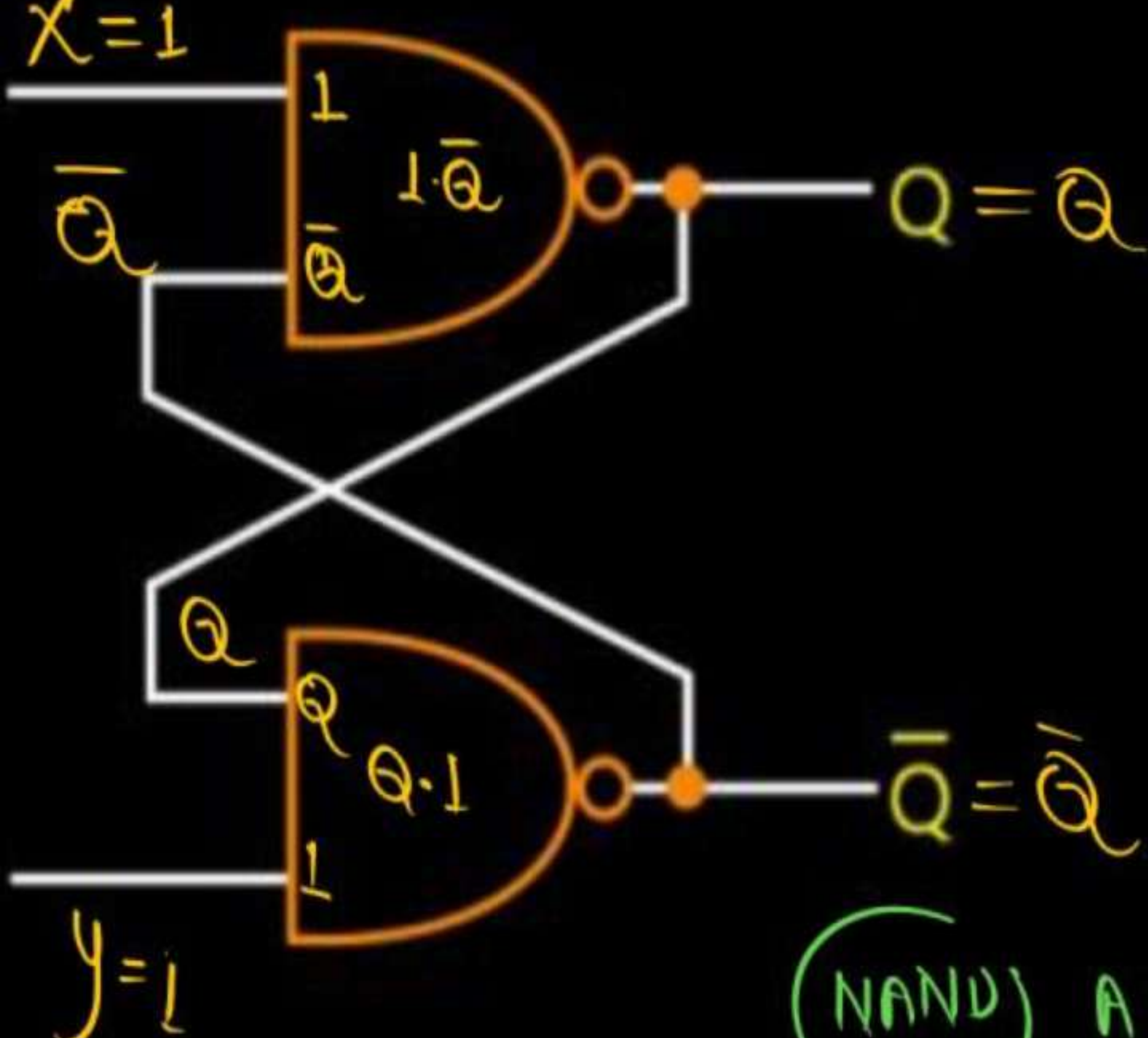
LATCHES & SR FF

LATCHES




A
B
A
B
A·B
$\overline{A \cdot B}$

$1 \cdot \bar{Q} = \bar{Q}$



गलत है मैं नही खेल
forbidden रहा
don't care

X	Y	Q	$\bar{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	Q	$\bar{Q}$

Invalid

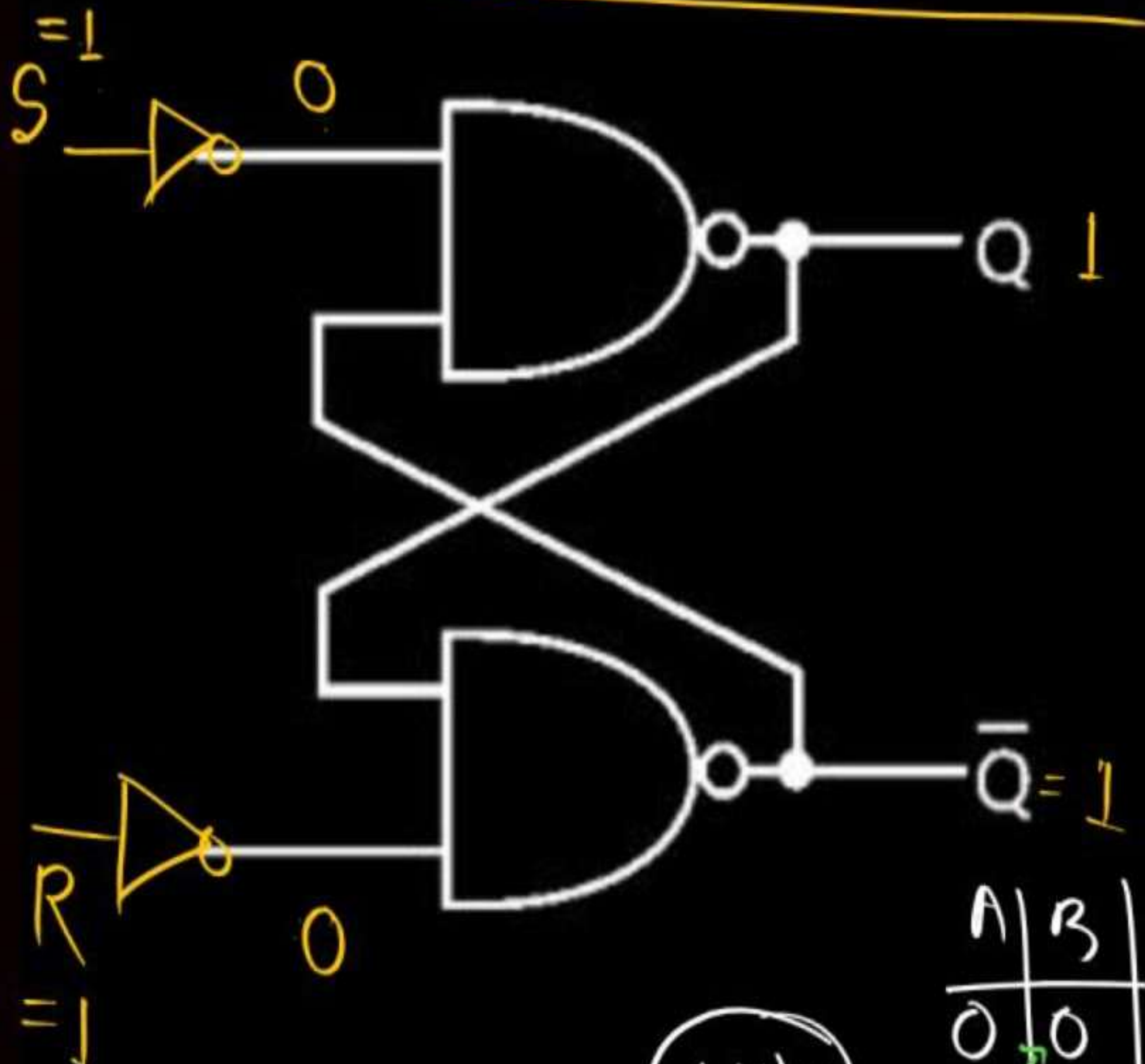
HOLD/ MEMORY

NAND

A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

LATCHES & FLIP FLOP

SET- RESET LATCH.



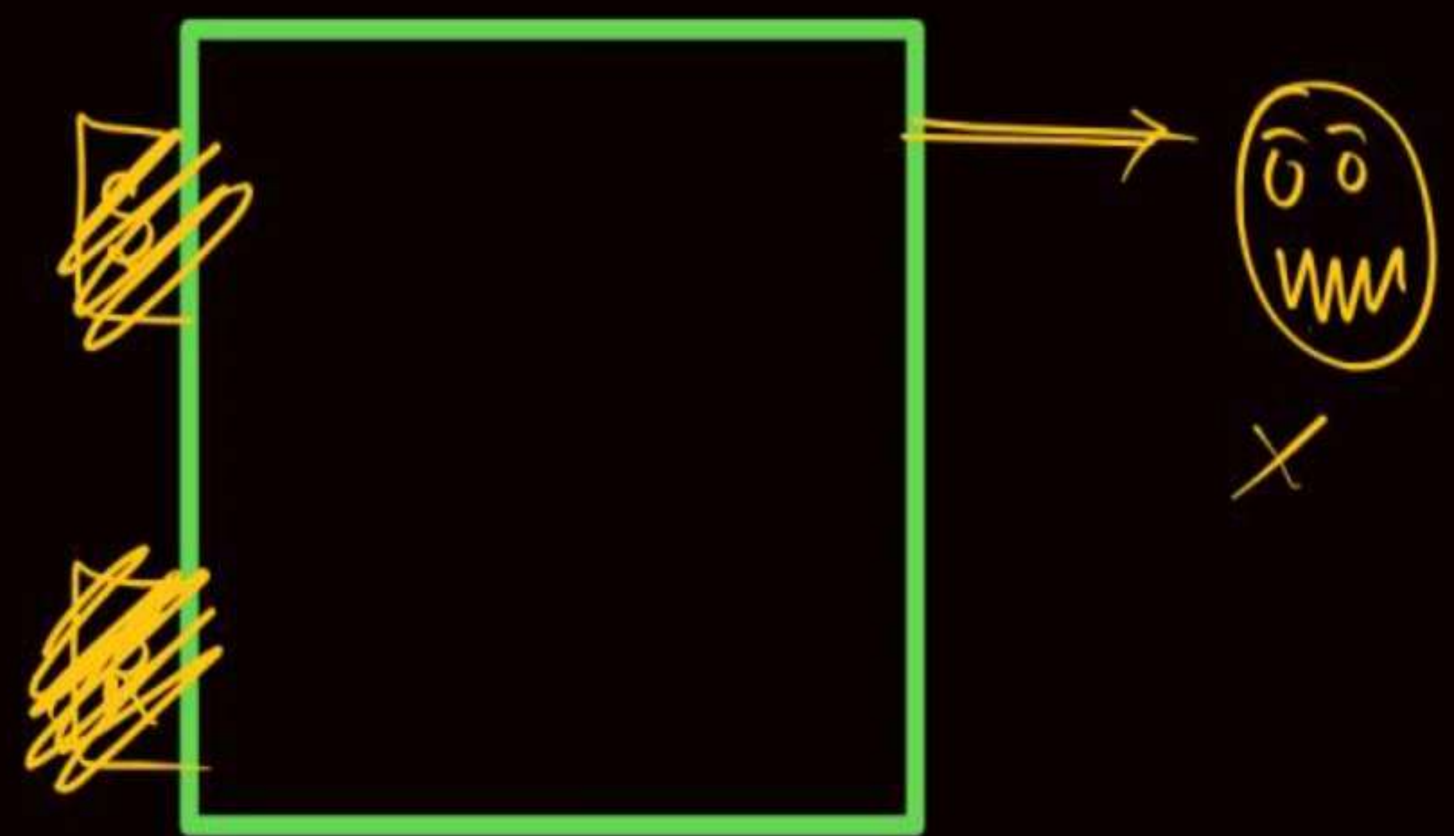
Set Reset O/P

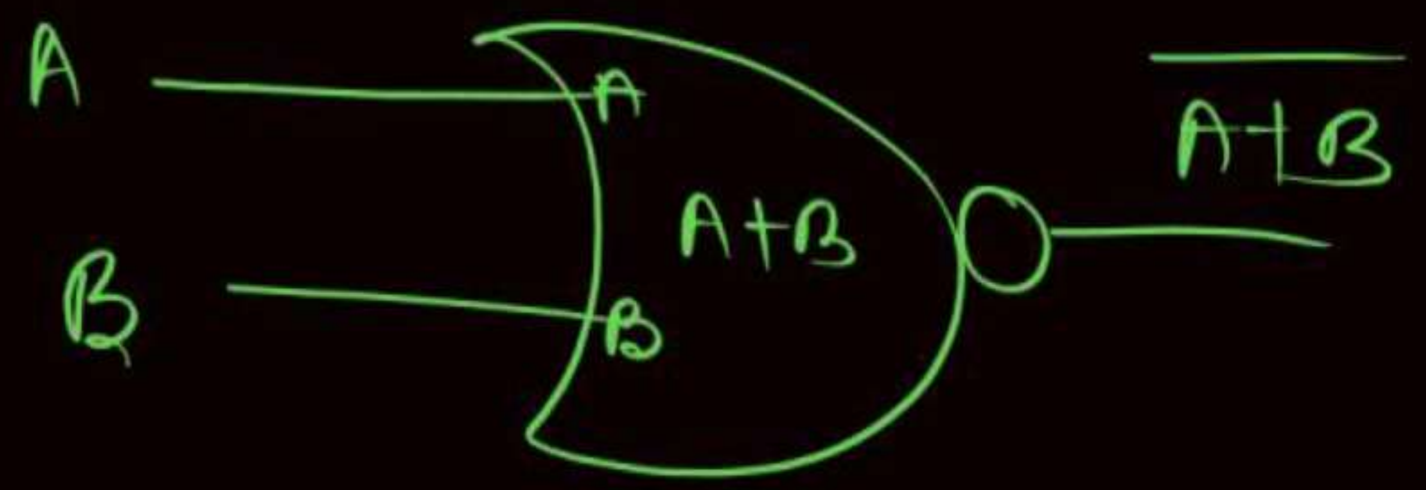
	S	R	Q	$\bar{Q}$
HOLD	0	0	Q	$\bar{Q}$
Reset	0	1	0	1
Set	1	0	1	0
Invalid	1	1	1	1

NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

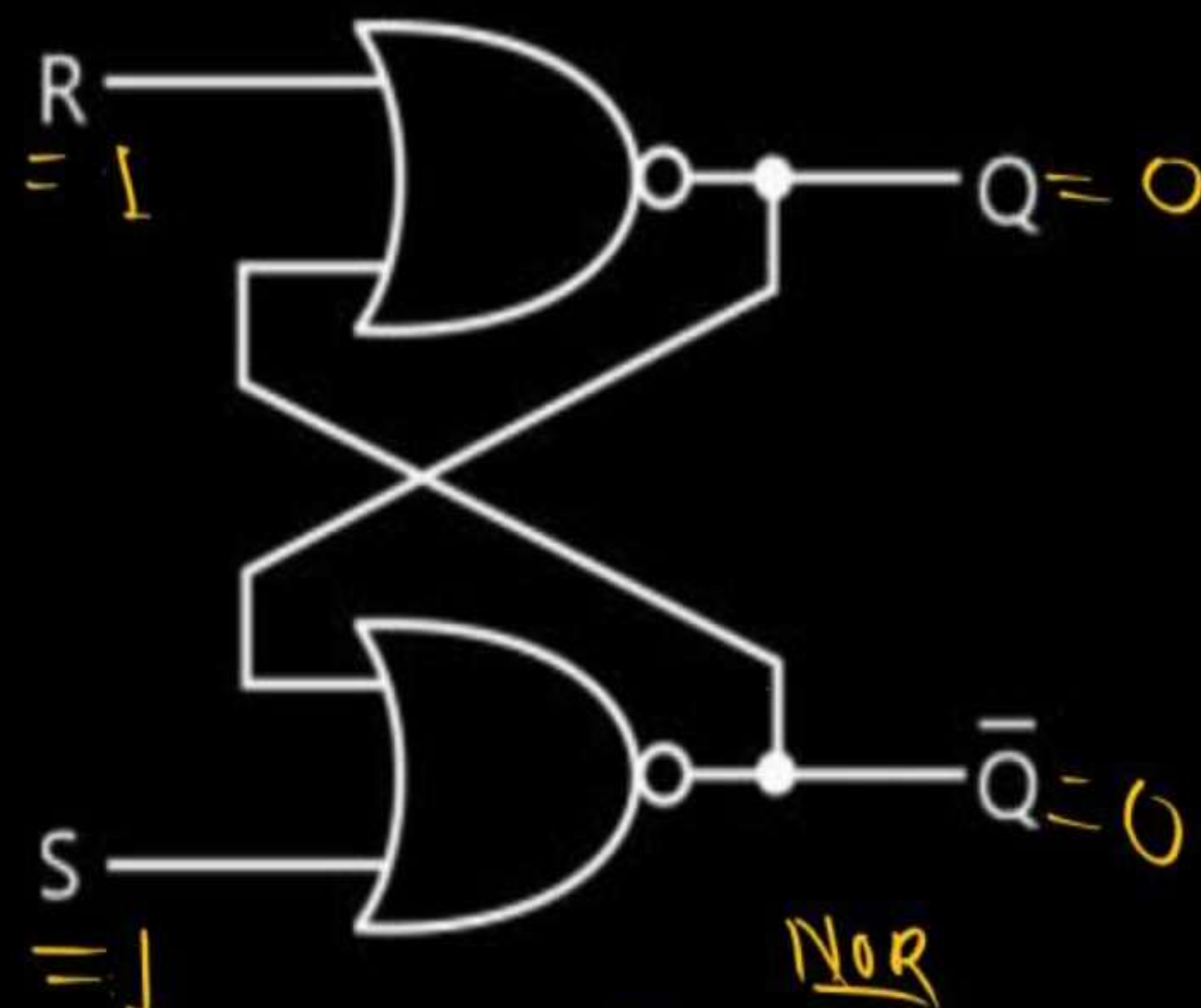
SR Latch




A
B
A
B
A+B
$\overline{A+B}$

LATCHES & FLIP FLOP

R-S Latch



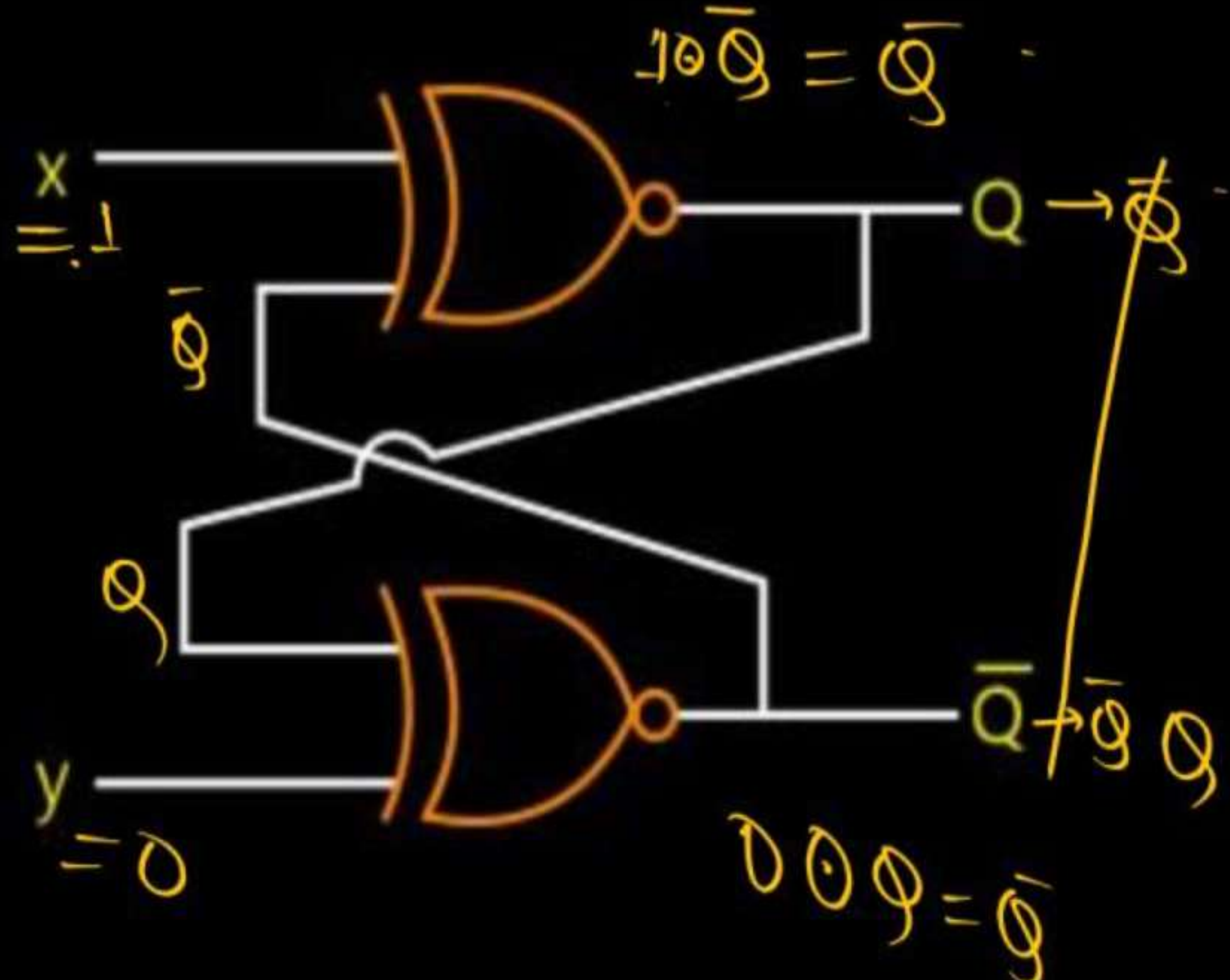
NOR

A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

	S	R	Q	$\bar{Q}$
HOLD	0	0	Q	$\bar{Q}$
Reset	0	1	0	1
Set	1	0	1	0
	1	1	X	X

LATCHES & FLIP FLOP

$$Q \odot Q = 1 \qquad Q \odot \bar{Q} = 0$$
$$Q \odot 1 = Q \qquad Q \odot 0 = \bar{Q}$$
$$\bar{Q} \odot 1 = \bar{Q} \qquad \bar{Q} \odot 0 = Q$$



X	Y	Q	$\bar{Q}$
✓ 0	0	Q	$\bar{Q}$ ✓
✓ 0	1	Q	Q ✗
✓ 1	0	$\bar{Q}$	$\bar{Q}$ ✗
1	1	$\bar{Q}$	Q ✓

Toggle

LATCHES & FLIP FLOP

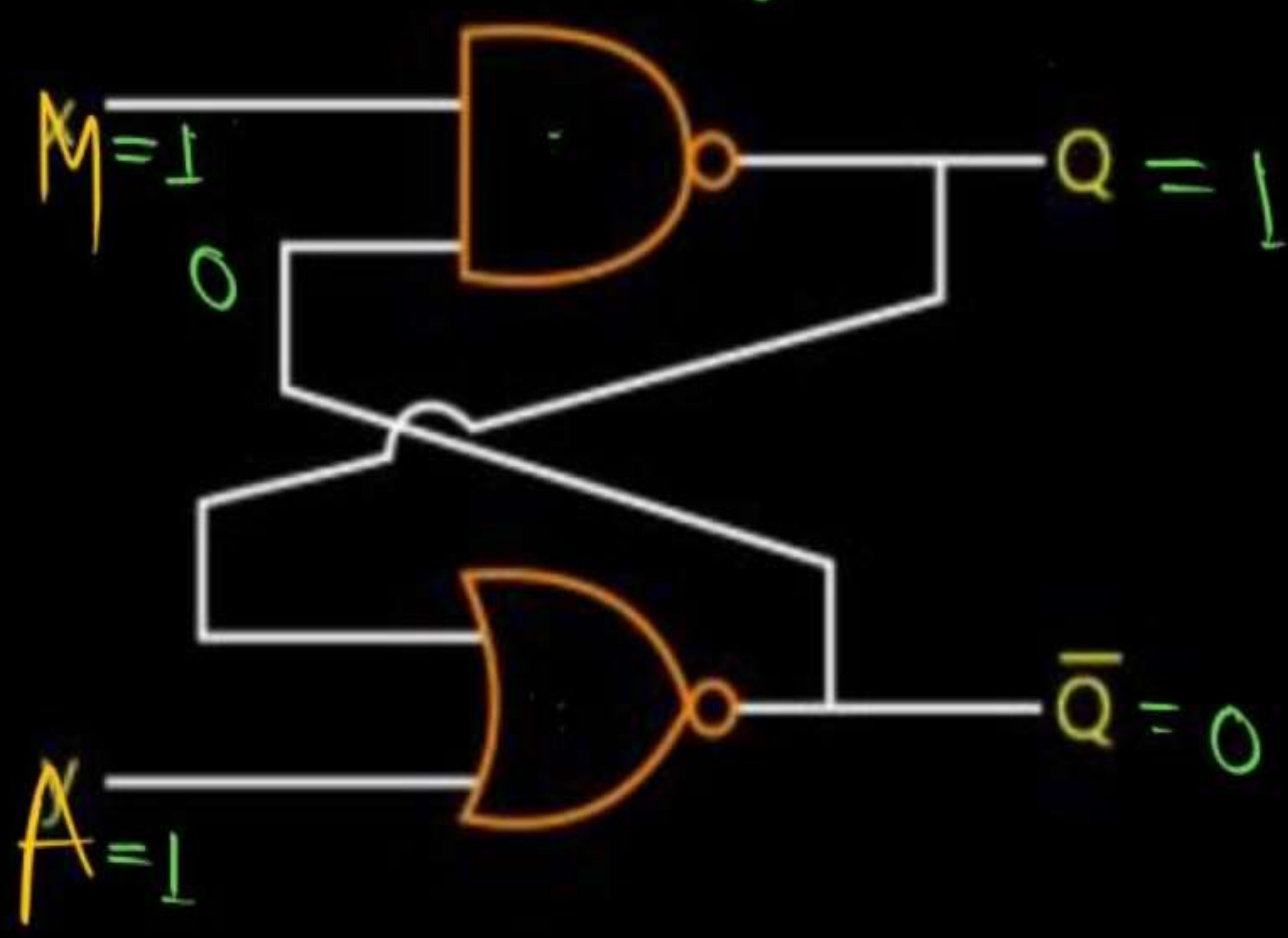
MA Latch

NAND

a	b	y
0	0	1
0	1	1
1	0	1
1	1	0

NOR

A	B	y
0	0	1
0	1	0
1	0	0
1	1	0



M	A	Q	$\bar{Q}$
0	0	1	0
0	1	1	0
1	0	Q	$\bar{Q}$
1	1	1	0

QUESTION

Consider a latch circuit shown in figure below. Which of the following set of input is invalid for circuit?

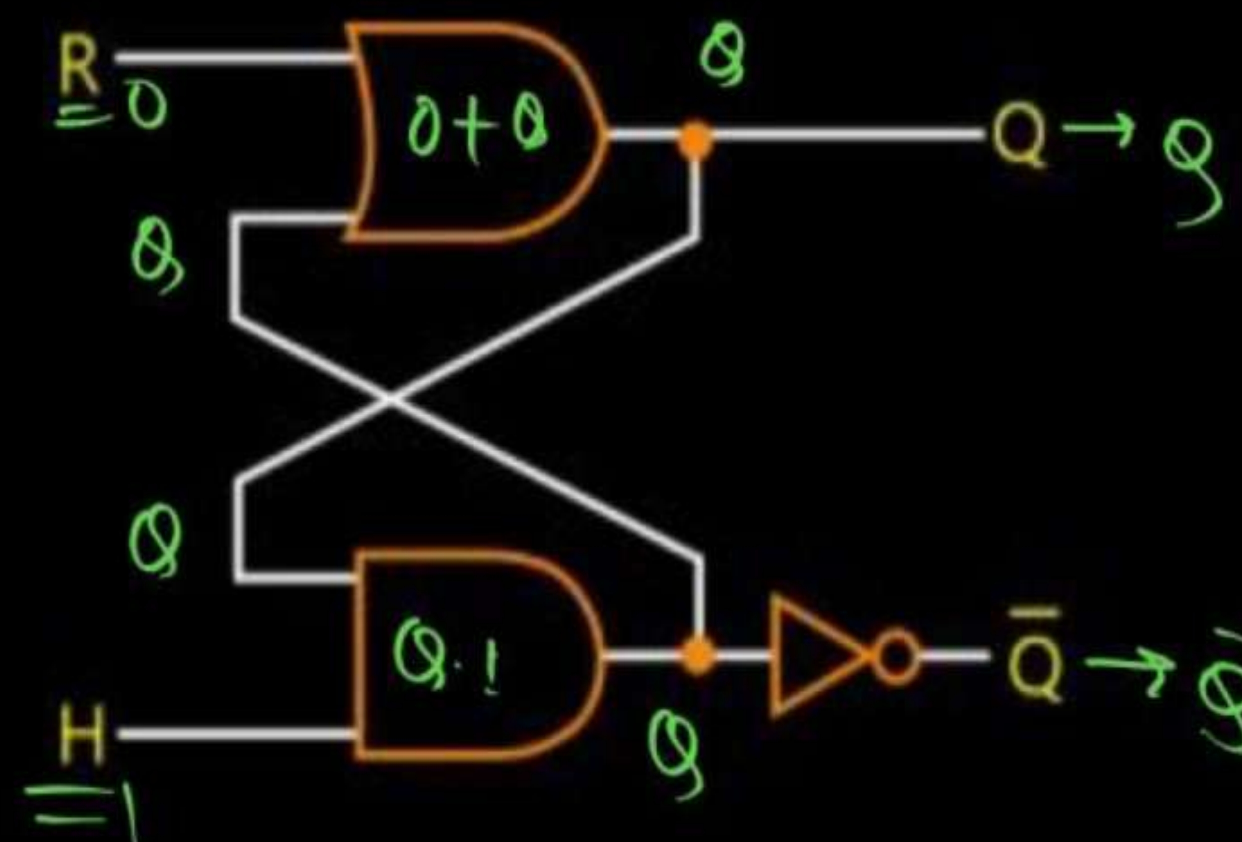
A. R=0 H=0 → $Q=0$ $\bar{Q}=1$ Valid

B. R=0 H=1 → $Q=Q$ $\bar{Q}=\bar{Q}$ Hold (Valid)

C. R=1 H=0 → $Q=1$ $\bar{Q}=1$ InValid

D. R=1 H=1 → $Q=1$ $\bar{Q}=0$ Valid

E. Sir, Mai Gajni hu.



OR

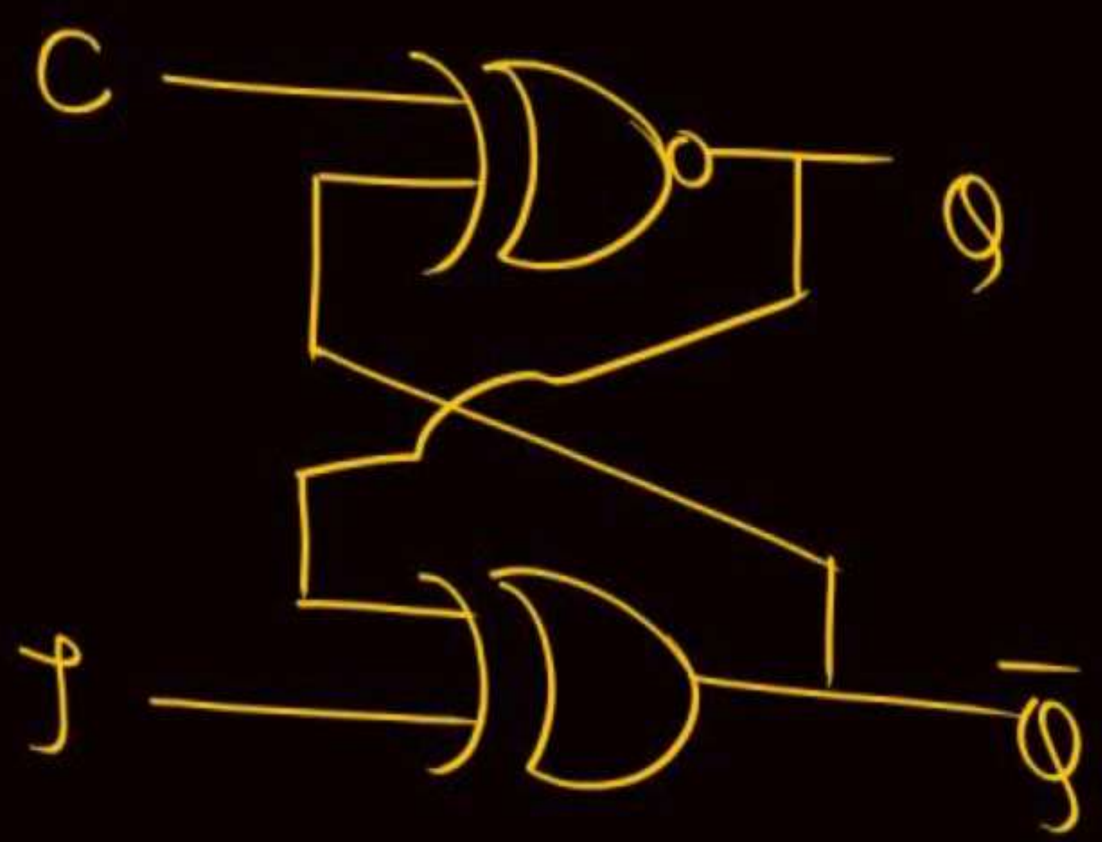
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

CJ latch

H.W



QUESTION

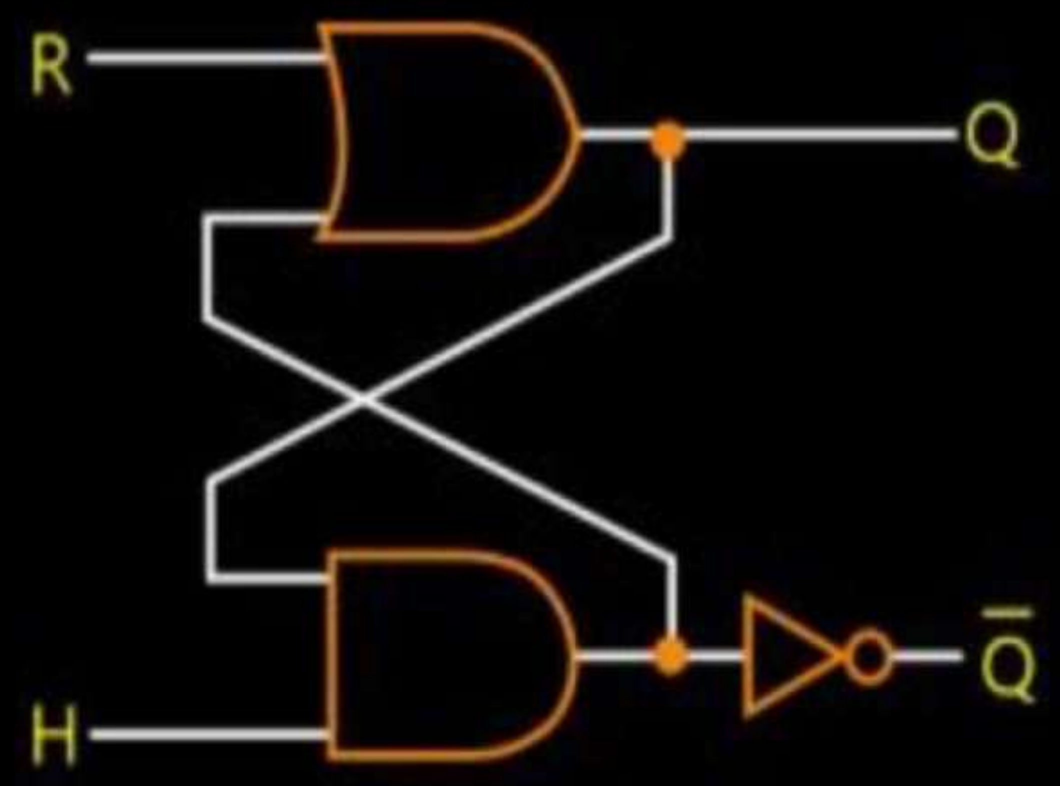
Consider a latch circuit shown in figure below. Which of the following set of input is invalid for circuit?

A. R=0 H=0

B. R=0 H=1

C. R=1 H=0

D. R=1 H=1



ABOUT ME

- Cleared Gate Multiple times with double Digit Rank (AIR 23, AIR 26)
- Qualified ISRO Exam
- Mentored More then 1 Lakhs+ Students (Offline & Online)
- More then 250+ Motivational Seminar in various Engineering College including NITs & Some of IITs

Chandan Jha

Latches

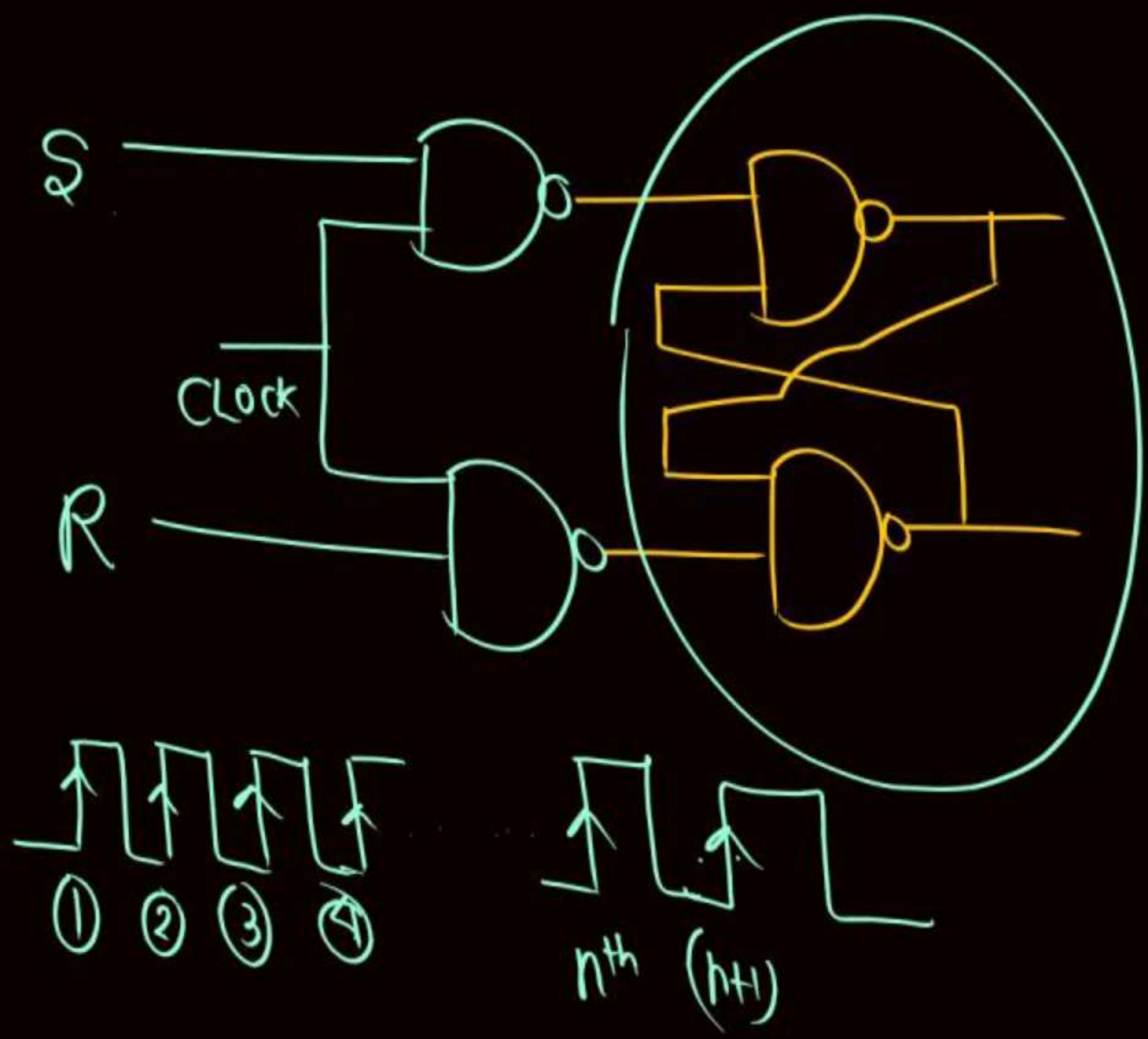
FF

Control

Clock

n^{th} $\quad$ $(n+1)$

n^{th} $\quad Q_n \quad Q_{n+1}$

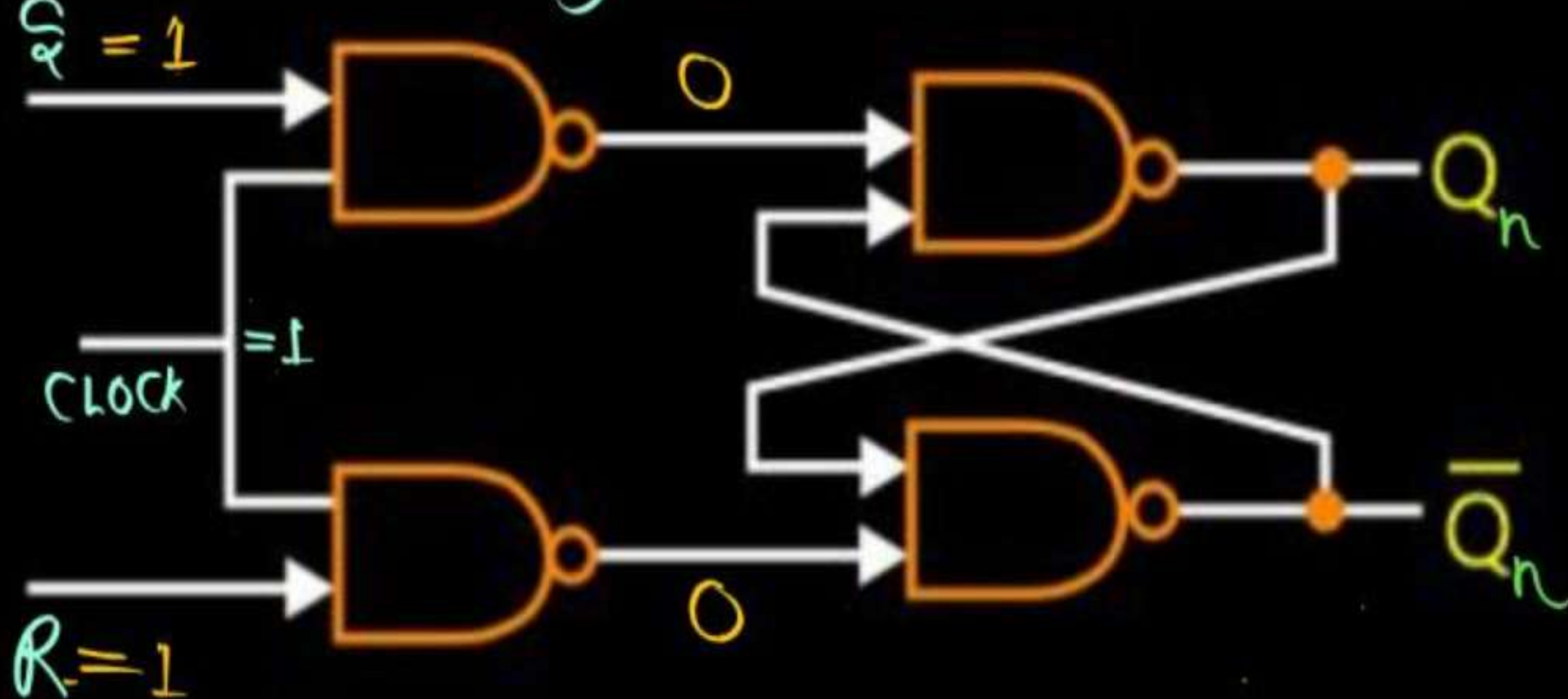


1. Circuit Diagram
2. Truth table
3. characteristic Table
4. characteristic Equation
5. Excitation Table
6. state Diagram

inputs	P.S Q_n	N.S Q_{n+1}

LATCHES & FLIP FLOP

① Circuit Diagram



Q_{n+1}

1

1

② Truth Table

S	R	Q_{n+1}	$\overline{Q}_{n+1}$	
0	0	Q_n	$\overline{Q}_n$	→ HOLD
0	1	0	1	RESET
1	0	1	0	SET
1	1	X	X	invalid / forbidden / don't care, [illegible]

(3) Characteristic Table :→

	S	R	Q_n	Q_{n+1}
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0 ✓
3	0	1	1	0 ✓
4	1	0	0	1 ✓
5	1	0	1	1 ✓
6	1	1	0	×
7	1	1	1	×

S	R	Q_{n+1}
0	0	Q_n
0	1	0 ✓
1	0	1
1	1	×

$$Q_{n+1}(S, R, Q_n) = \sum m(1,4,5) + \sum d(6,7)$$

(4) Characterstic Equation

$$Q_{n+1}(S,R,Q_n)=\sum m(1,4,5)+\sum d(6,7)$$

$S \backslash RQ_n$	$\bar{R}\bar{Q}_n$ 00	$\bar{R}Q_n$ 01	RQ_n 11	$R\bar{Q}_n$ 10
$\bar{S}$ 0		1		
S 1	1	1	X	X

$$Q_{n+1}=S+\bar{R}Q_n$$

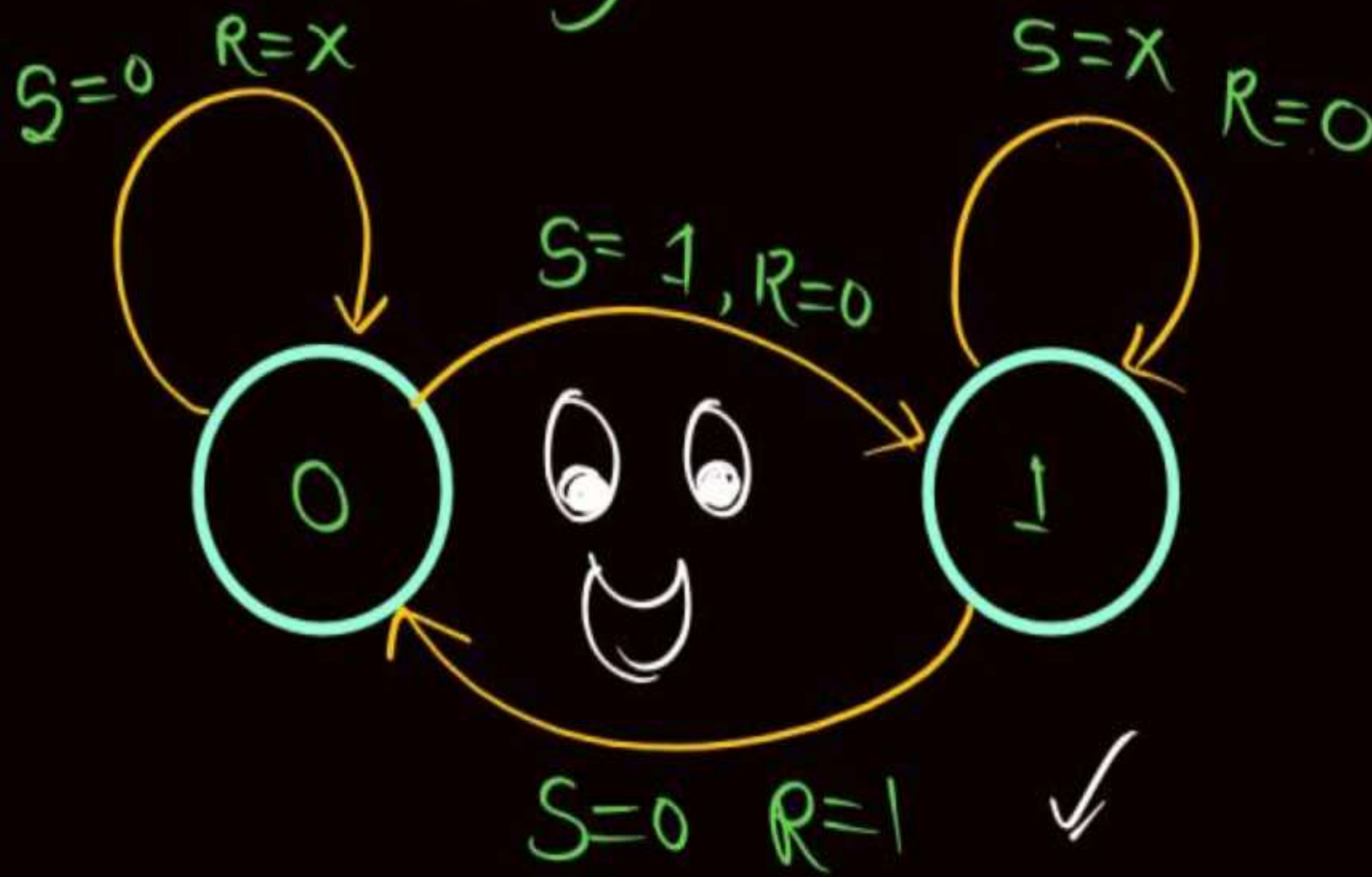
⑤ Excitation Table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

C.T.

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

6 State Diagram



E.T

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

RECAPE

Maza

DEC

Circuit Diagram
↓
Truth Table
↓
Char. Table ⟶ Excitation Table ⟶ State Diagram
↓
Char. Equation

Truth Table

C	J	Q_{n+1}
0	0	0
0	1	$\overline{Q_n}$
1	0	1
1	1	Q_n

1. Char. T
2. Char. Eq
3. Excitation Table
4. State Diagram


THANK
YOU!

EC/EE/CS & IT/IN

Digital Electronics

JK Flip Flop, D & T Flip Flop , Designing of Flip flop

LECTURE NO. 8

Chandan Jha Sir (CJ Sir)

मोटिवेशन

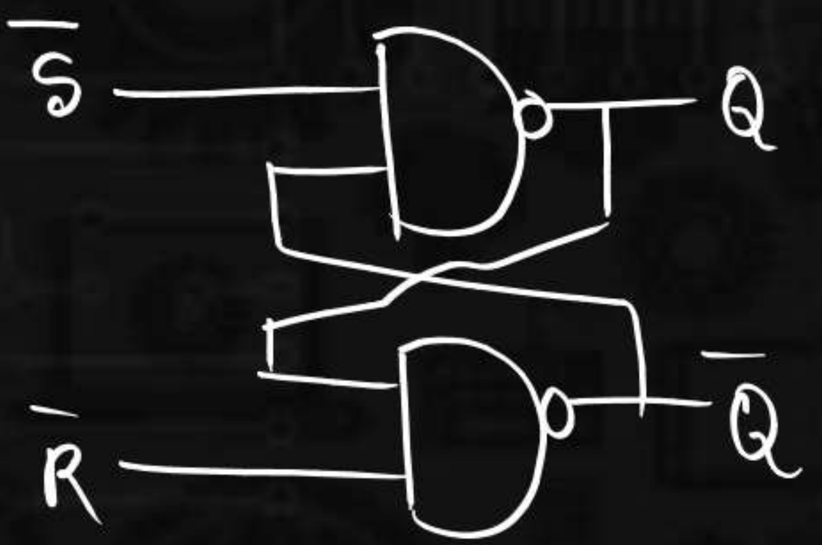
कोशिश करने वालों की हार नहीं होती

कोशिश करने वालों की हार नही होती,
लहरों से डरकर नौका पार नही होती।
नन्हीं चीटी जब दाना लेकर चलती है,
चढ़ती दीवारों पर, सौ बार फिसलती है।
मन का विश्वास रगों में साहस भरता है,
चढ़कर गिरना, गिरकर चढ़ना ना अखरता है।
आखिर उसकी मेहनत बेकार नही होती,
कोशिश करने वालों की हार नही होती।
डुबकियां सिंधु में गोताखोर लगाता है,
जा जाकर खाली हाथ लौट आता है।
मिलते नहीं सहज ही मोती गहरे पानी में,
बढ़ता दुगुना उत्साह इसी हैरानी में।
मुट्ठी उसकी खाली हर बार नही होती,
कोशिश करने वालों की हार नहीं होती।
असफलता एक चुनौती है, इसे स्वीकार करों,
क्या कमी रह गयी, देखों और सुधार करों
जब तक न सफल हो, नींद चैन से त्यागो तुम
संघर्ष का मैदान छोड़कर मत भागो तुम।
कुछ किये बिना ही जय जयकार नही होती,
कोशिश करने वालों की हार नहीं होती।

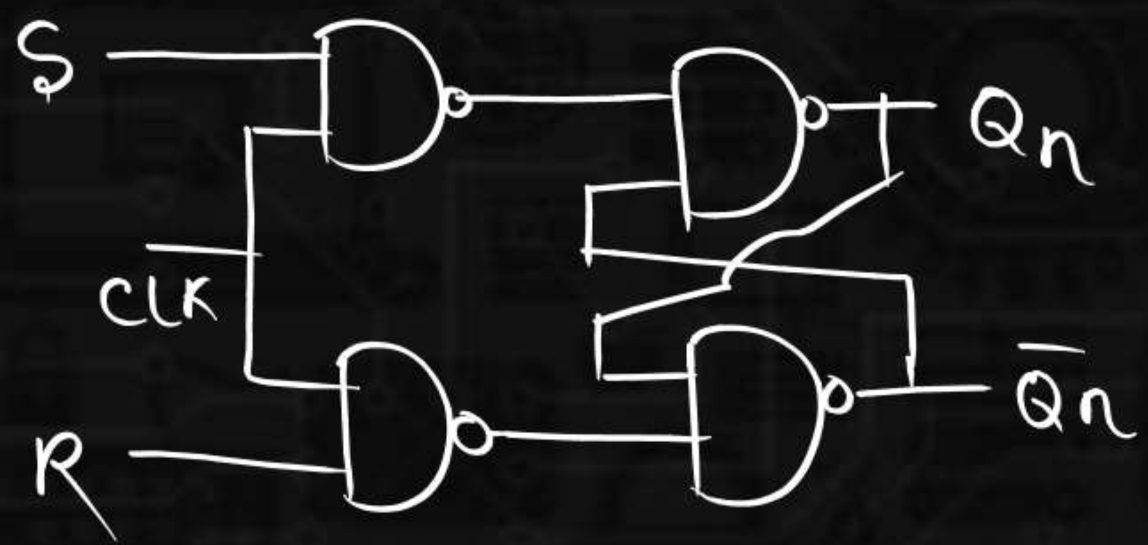
RECAPE

Latches:

SR Latch



S-R Flip-Flop.



S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

Characteristic Equation

$$Q_{n+1} = S + \bar{R} Q_n$$

Excitation Table.

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

TOPICS TO BE COVERED

01 JK Flip Flop

02 D Flip Flop

03 T Flip Flop

04 Desiging of Flip Flops

JK Flip Flop

Jack Keilby.

(1) Symbol

(2) Truth Table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

JK Flip Flop

(3) Characteristic Table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

	J	K	Q_n	Q_{n+1}
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

JK Flip Flop

(4) Characteristic Equation

$$Q_{n+1}(J, K, Q_n) = \sum m(1, 4, 5, 6)$$

$J \backslash KQ_n$	00	01	11	10
0		1		
1	1	1		1

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

JK Flip Flop

(5) Excitation Table

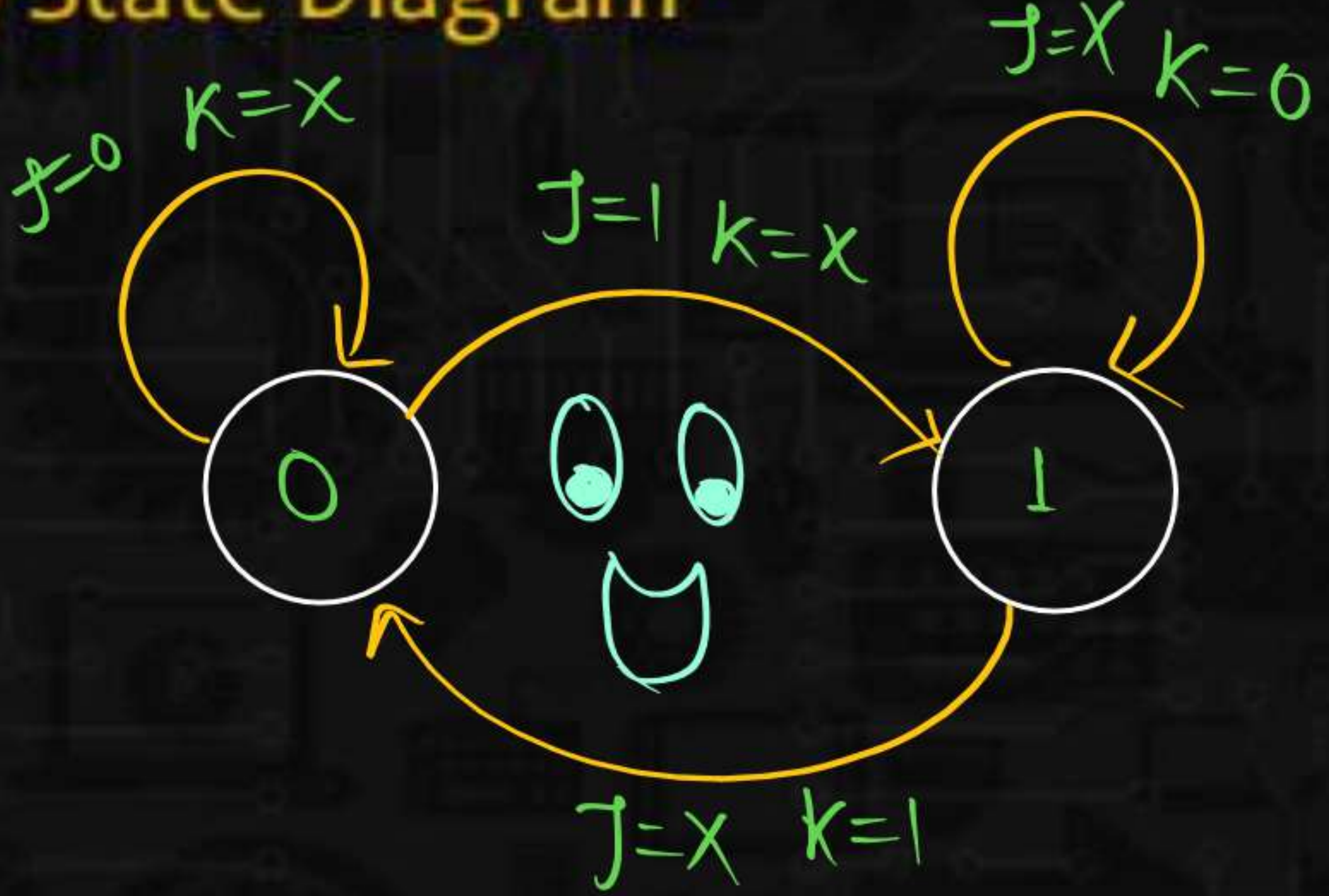
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

characteristic Table.

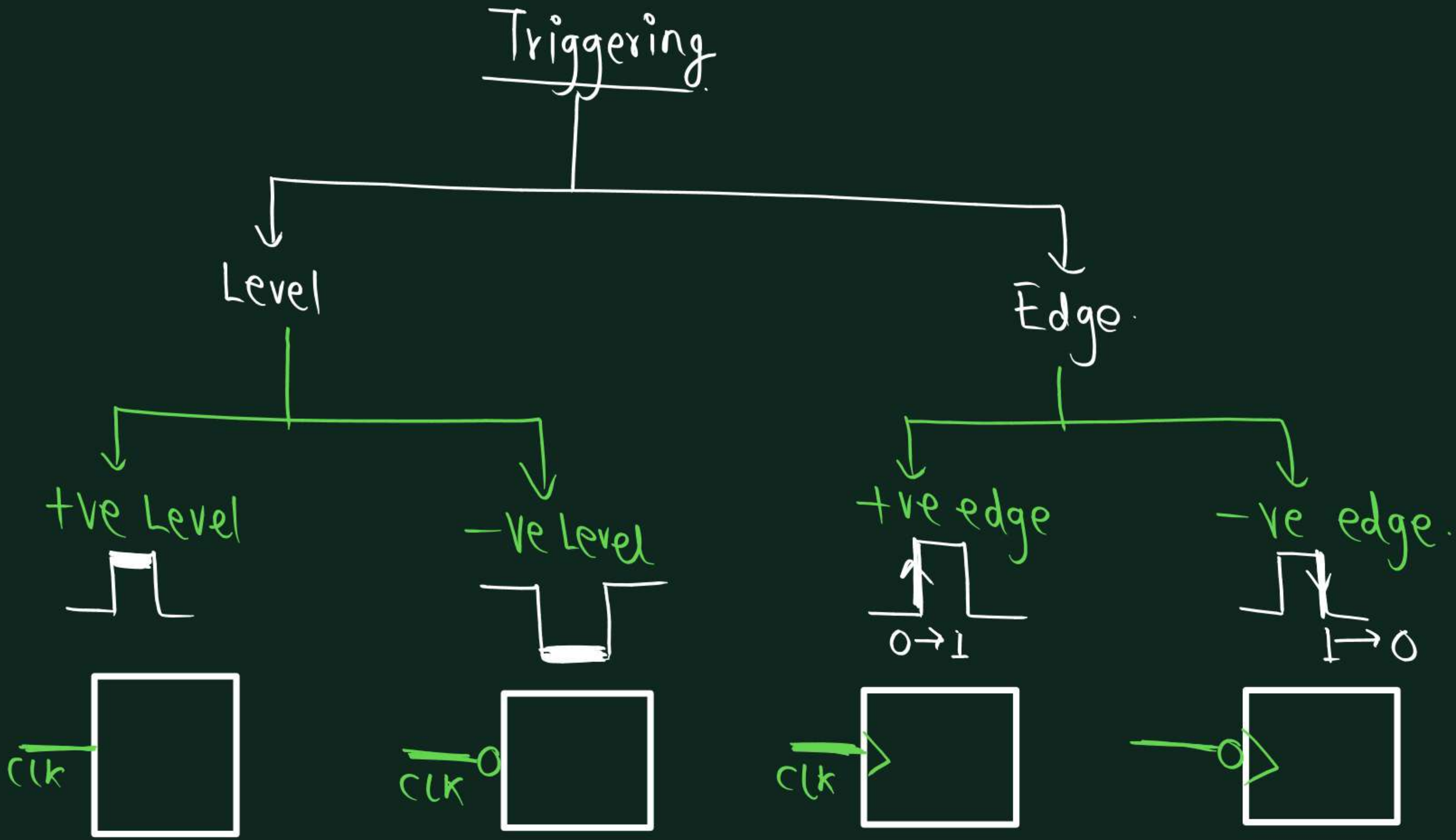
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

JK Flip Flop

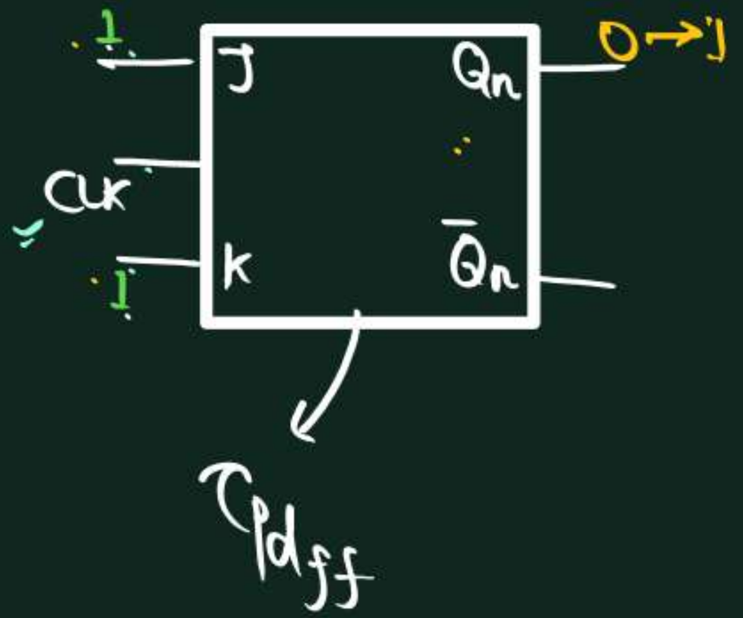
(6) State Diagram

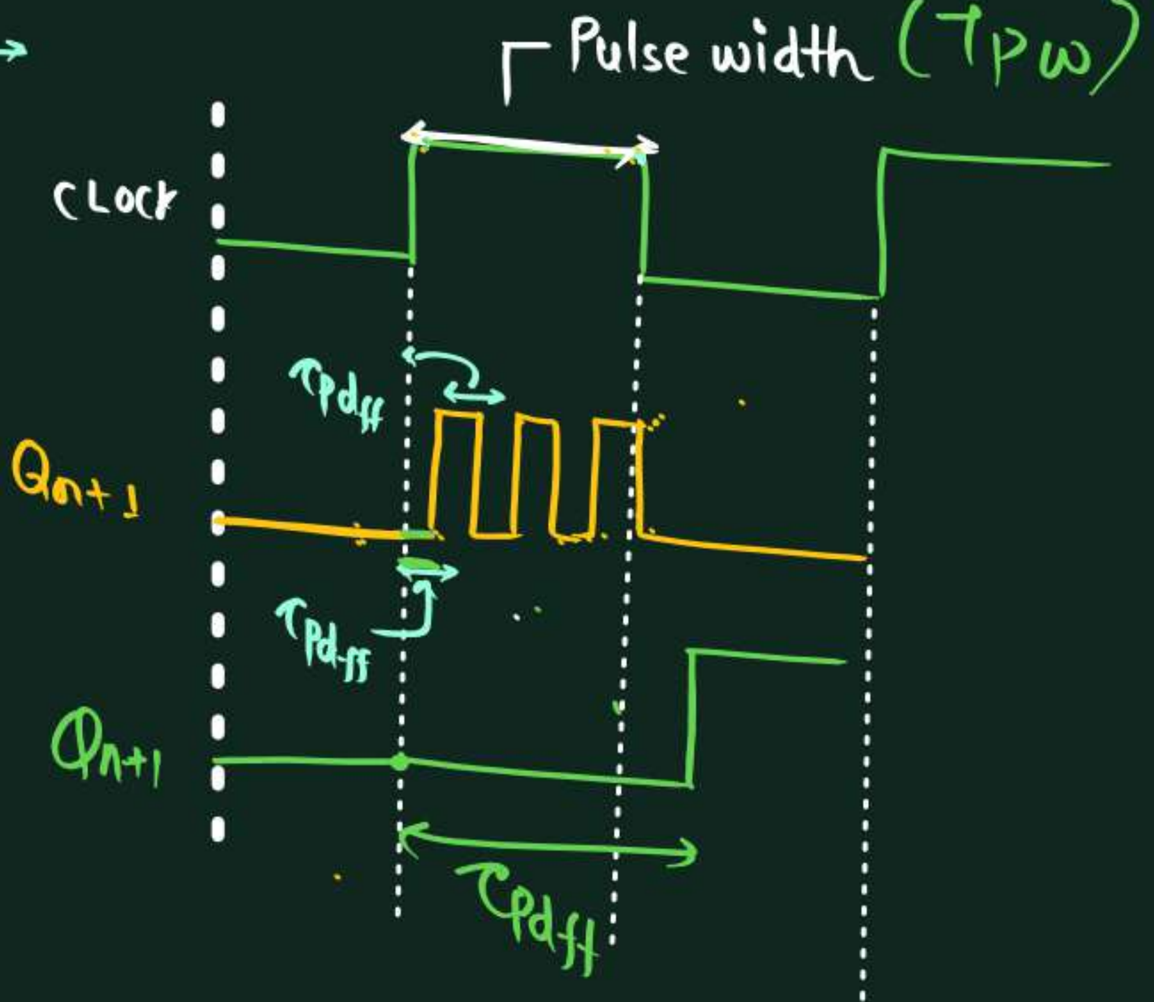


Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0


Triggering
Level
Edge
+ve Level
-ve Level
+ve edge
-ve edge
0→1
1→0
clk
clk
clk

Race around Problem :→

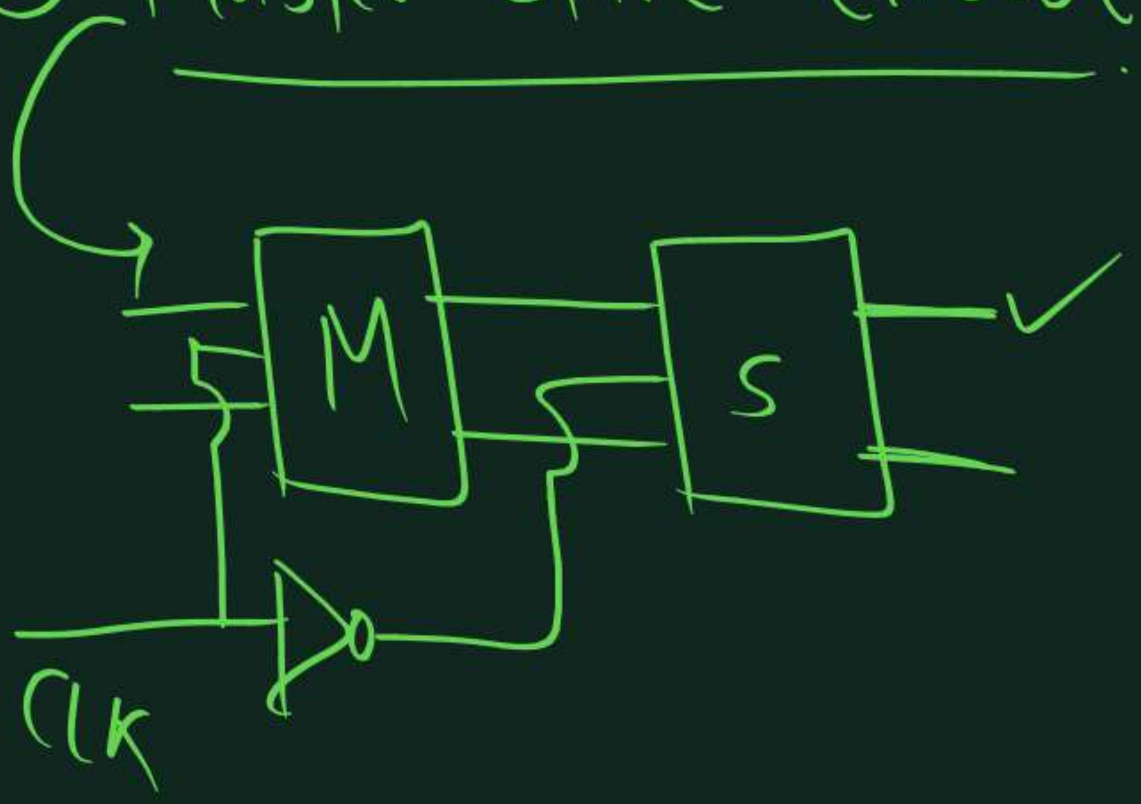




To avoide Race Around problem

① $T_{pw} < \tau_{pdff} < T_{clk}$

② Master-Slave circuit



DJ Wale Babu → Ashmit

$t=0$

$t=10\,\text{min}$

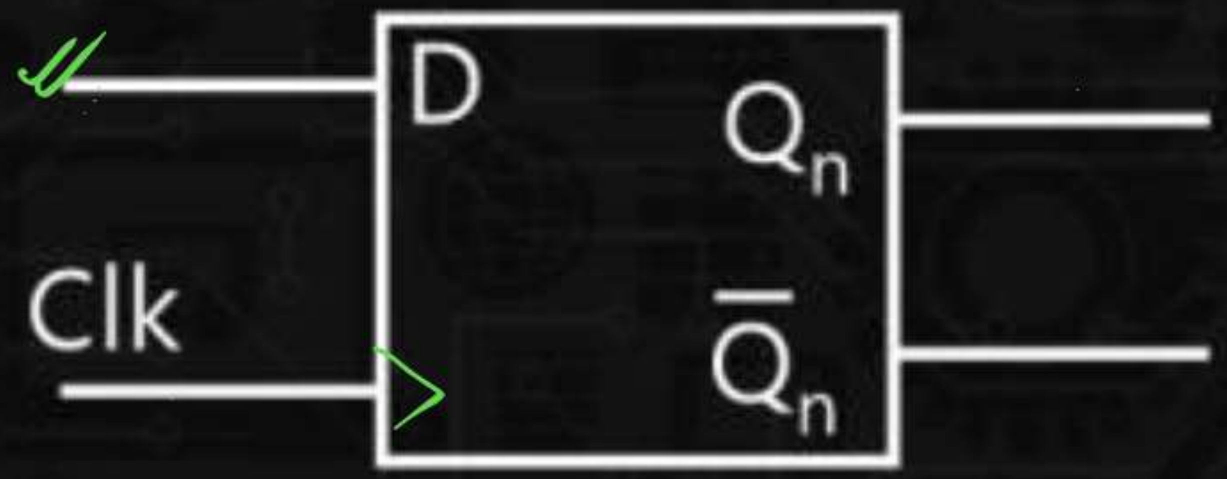
U

CJ S Sp Rj DR Nishu Rahul AR unicorn

D Flip Flop

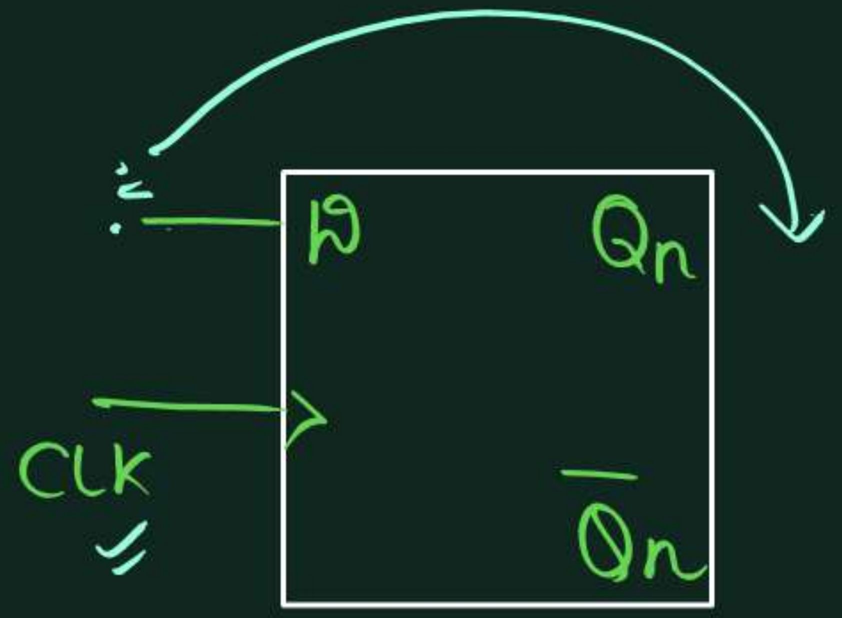
Data, Transparent

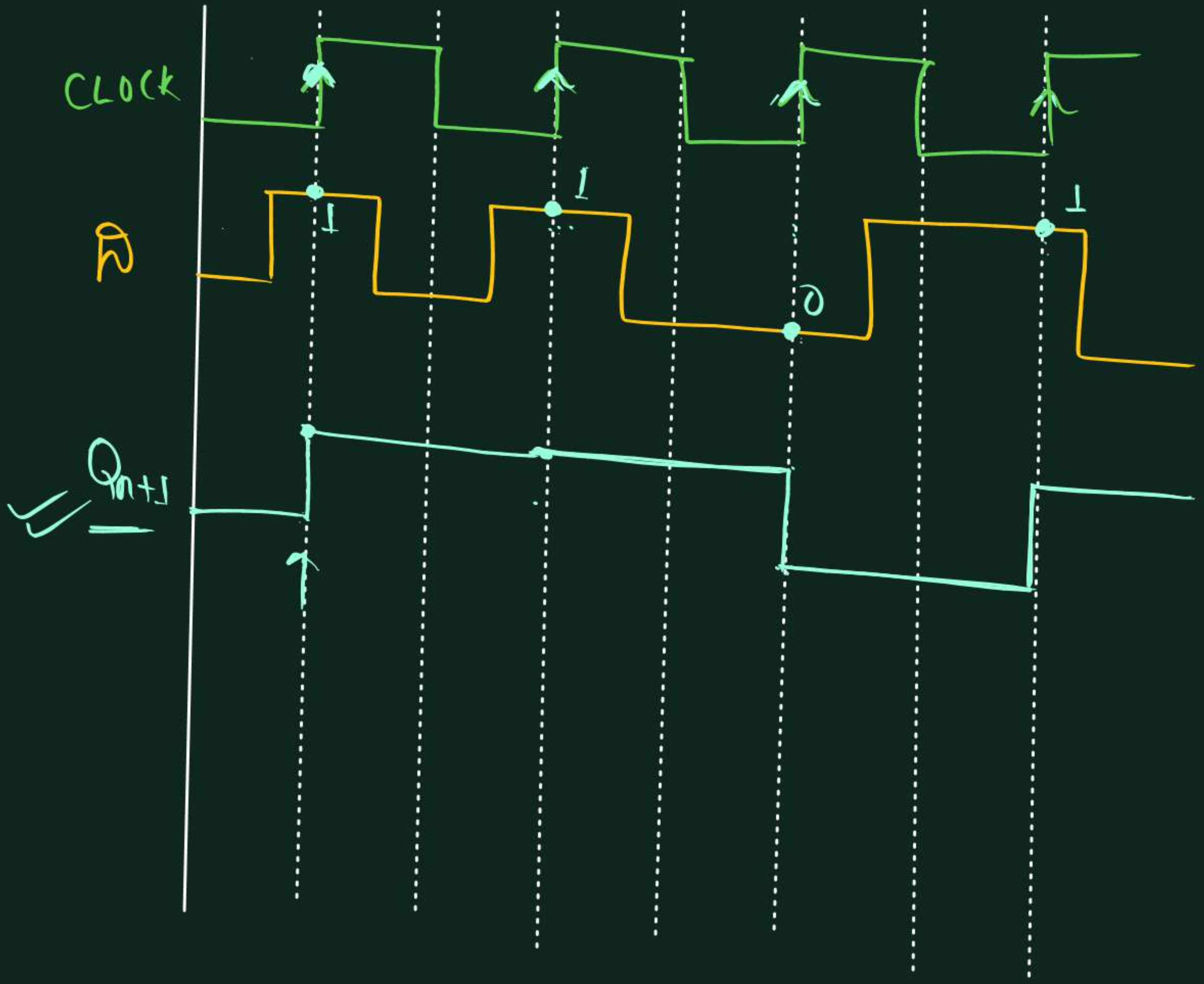
(1) Symbol



(2) Truth Table

D	Q_{n+1}
0	0
1	1


D
Qn
CLK
Q̄n


CLOCK
D
1
1
0
1
Qn+1

D Flip Flop

(3) Characteristic Table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$$Q_{n+1} = D\bar{Q}_n + DQ_n$$
$$= D(\bar{Q}_n + Q_n)$$
$$= D$$

D Flip Flop

(4) Characteristic Equation

$$\boxed{Q_{n+1} = D}$$

SR

$Q_{n+1} = S + \bar{R}Q_n$

JK

$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$

DFF

$Q_{n+1} = D$

D Flip Flop

(5) Excitation Table

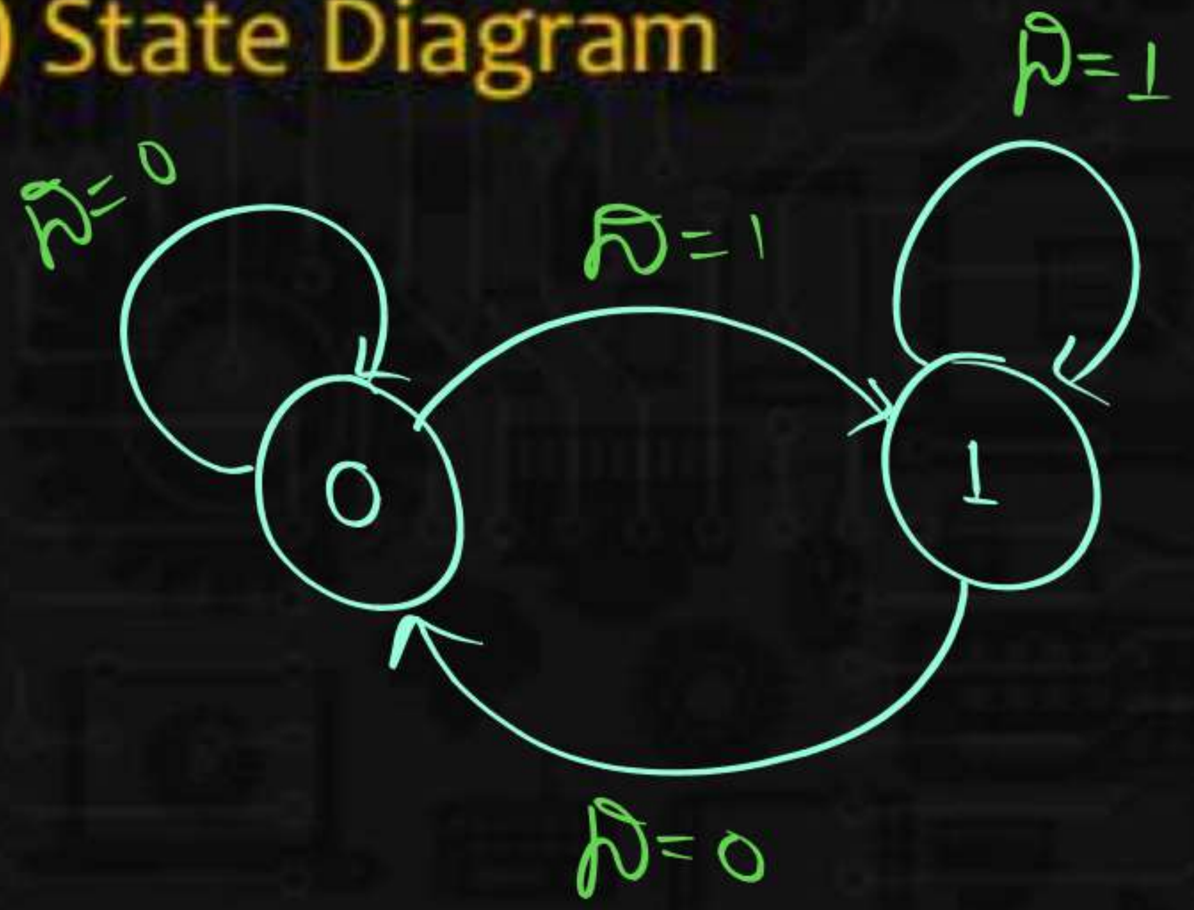
Q_n	Q_{n+1}	D
0	0	0 ✓
0	1	1 ✓
1	0	0 ✓
1	1	1 ✓

D	Q_n	Q_{n+1}
0 ✓	0	0
0	1	0
1	0	1
1	1	1

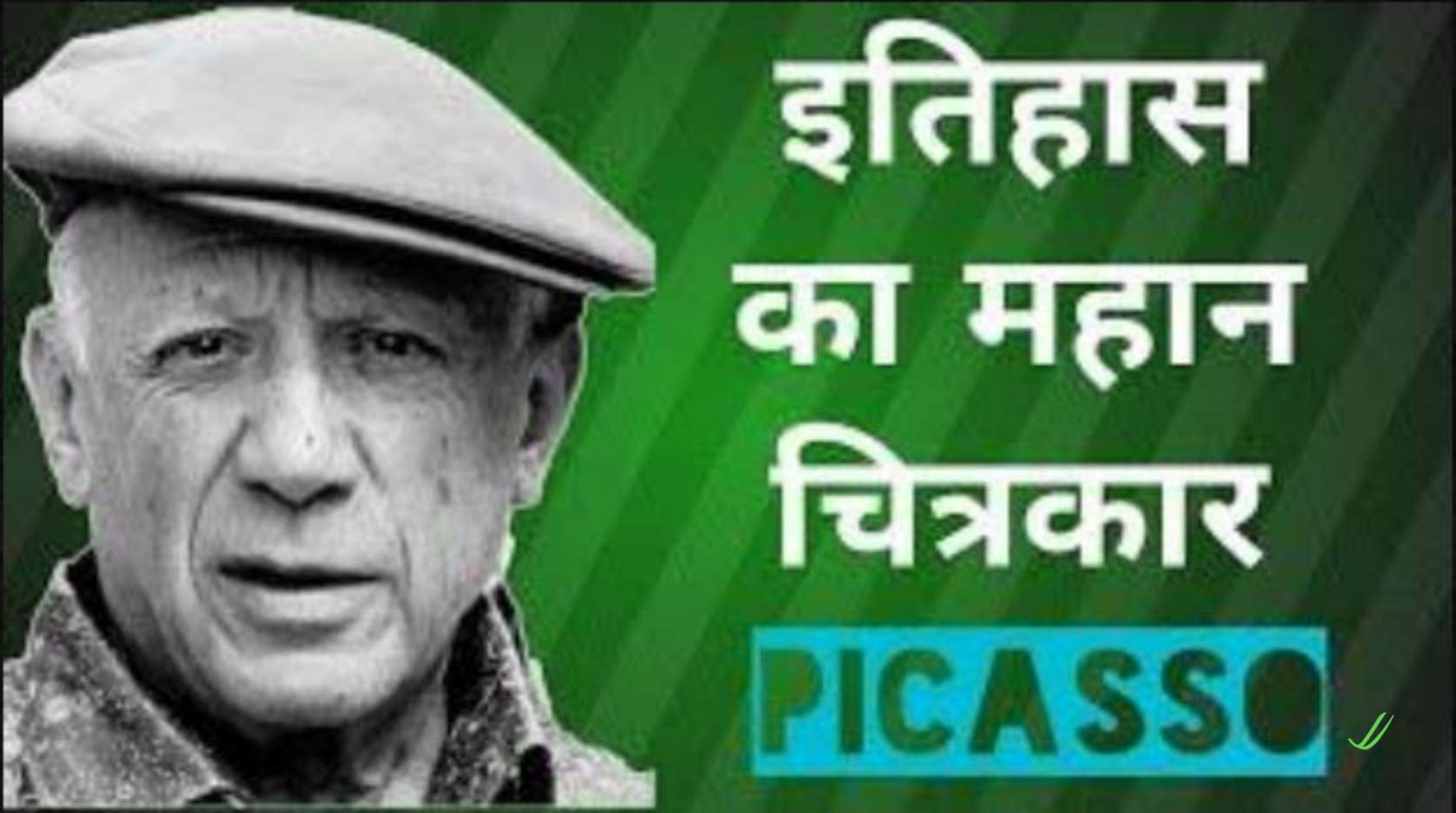
$$\boxed{Q_{n+1} = D}$$

D Flip Flop

(6) State Diagram



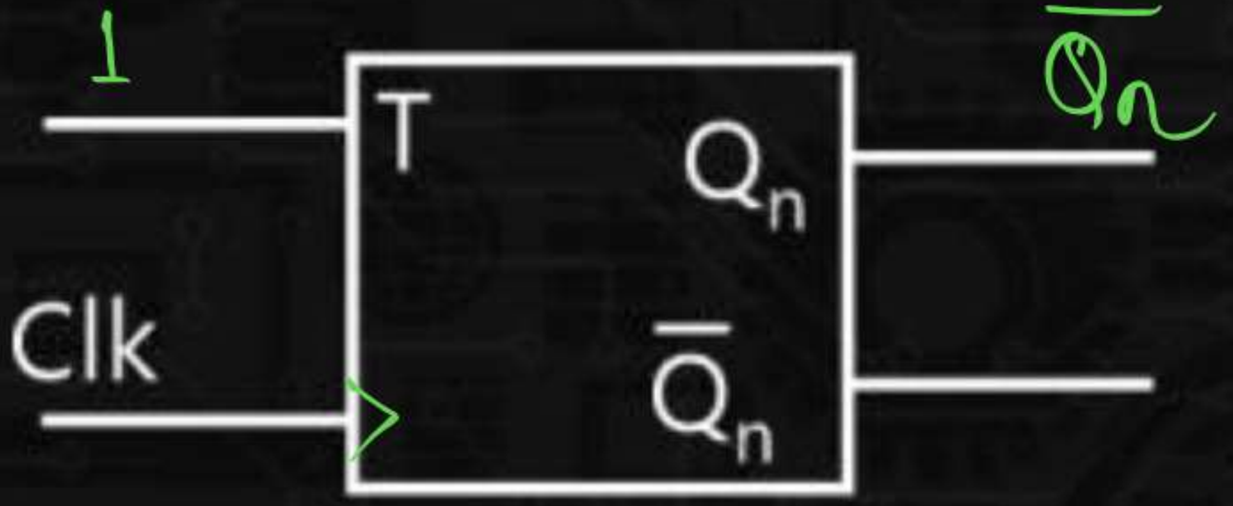
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1


इतिहास
का महान
चित्रकार
PICASSO

T Flip Flop

Toggle FF

(1) Symbol



(2) Truth Table

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

T Flip Flop

(3) Characteristic Table

$T=0 \quad Q_{n+1}=Q_n$

$T=1 \quad Q_{n+1}=\overline{Q}_n$

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$Q_{n+1}=\overline{T}Q_n+T\overline{Q}_n$

$Q_{n+1}=T\oplus Q_n$

T Flip Flop

(4) Characteristic Equation

$$\boxed{Q_{n+1} = T \oplus Q_n}$$

T Flip Flop

(5) Excitation Table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

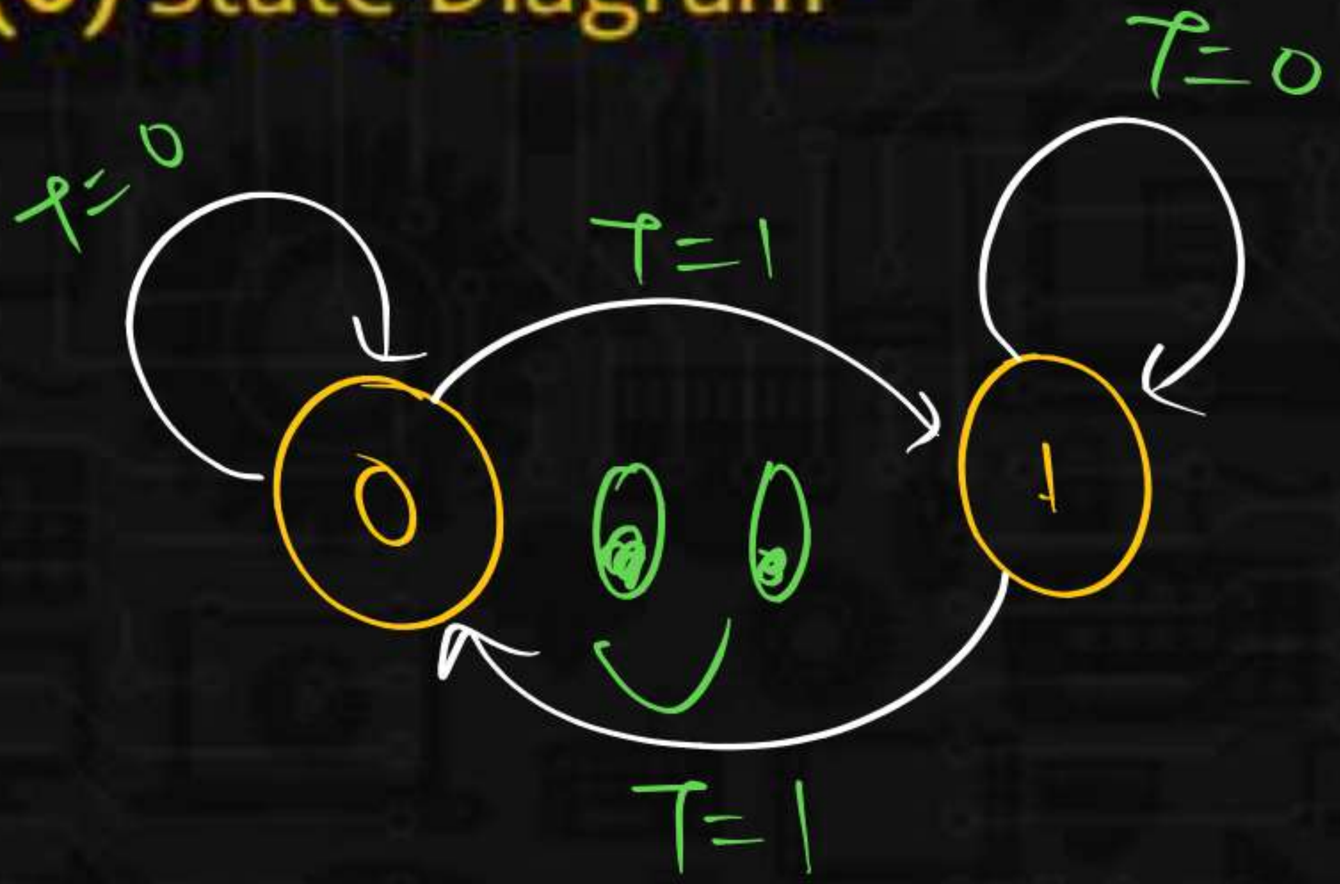
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$$Q_{n+1} = T \oplus Q_n$$

$$\boxed{T = Q_n \oplus Q_{n+1}}$$

~~D~~ T Flip Flop

(6) State Diagram



Q_n	Q_{n+1}	~~D~~ T
0	0	0
0	1	1
1	0	~~0~~ 1
1	1	~~1~~ 0

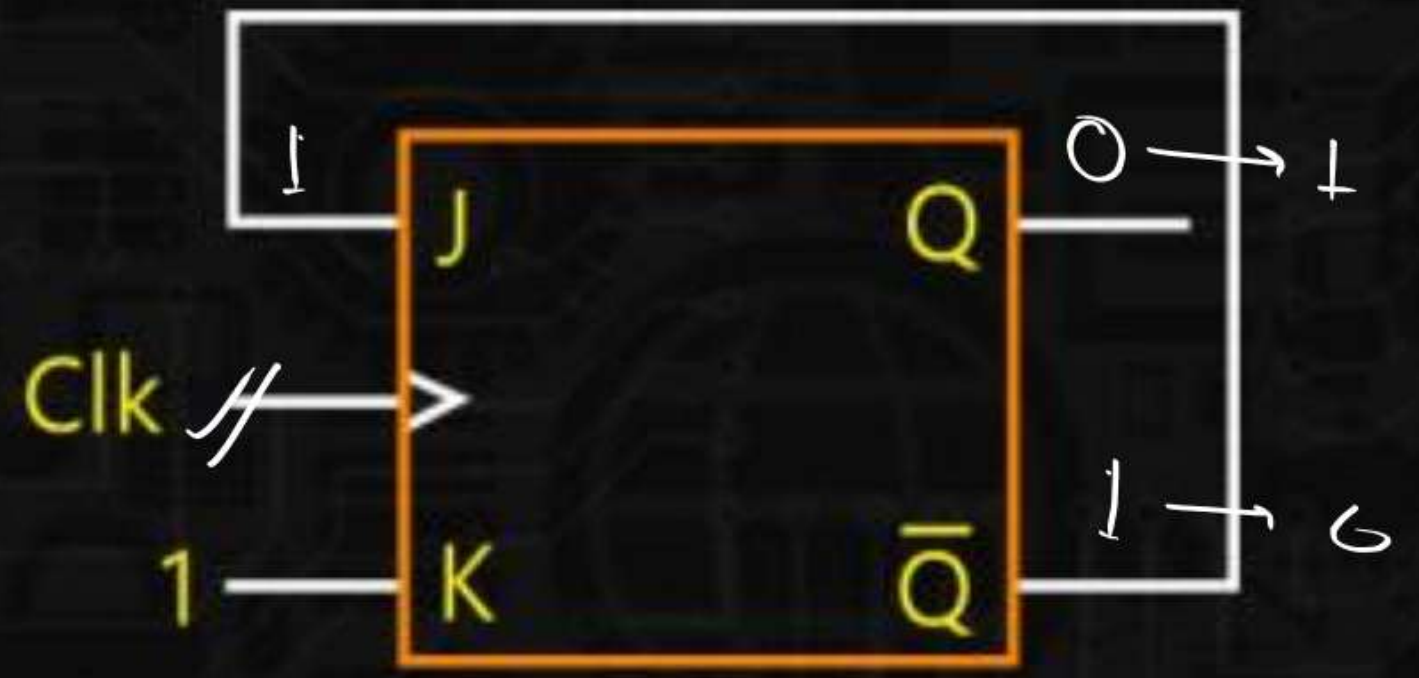
Q.1 The J-K FF shown below is initially cleared and then clocked for 5 pulses, the sequence at the Q output will be

A. 010000

B. 011001

C. 010010

D. 010101



$0 \to 1 \to 0 \to 1 \to 0 \to 1$

Q.1 For the circuit given below x & y condition will be-

A. x stable y toggle

B. x toggle y stable

C. x & y both toggle

D. x & y both stable

Designing of Flip Flops

avaliabl FF → Desired FF

E

C

Step (1) : Write the characteristic table of desired Flip Flop.

Step (2) : Write the excitation table of available Flip Flop.

Step (3) : Write the logical expression.

Step (4) : Minimize the logical expression.

Step (5) : Hardware implementation.

CD

chara. Table

Desired

Q.2 Design a D FF by using T FF?

Desired

Excitation Table

Step 1

& Step 2

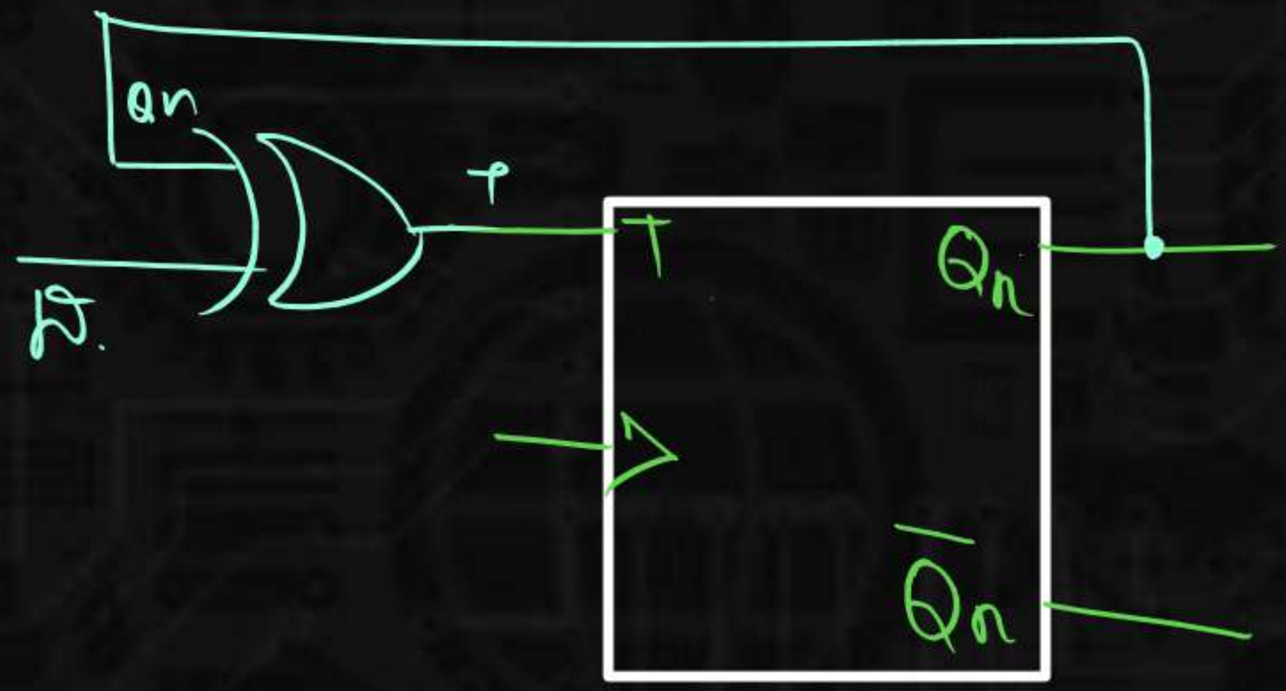
D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Step 3. $T = \bar{D} Q_n + D \bar{Q}_n$

$T = D \oplus Q_n$

Step 4:

Step 5.



Q.3 Design a D FF by using SR Flip Flop?

desired — D FF; avaliable — SR Flip Flop.

Step-1 & Step-2.

D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

Step 3. $S(D, Q_n) = \Sigma m(2) + \Sigma d(3)$

& Step 4

$S \Rightarrow$

D \ Q_n	0	1
0		
1	1	X

$S = D$

$R(D, Q_n) = \Sigma m(1) + \Sigma d(0)$

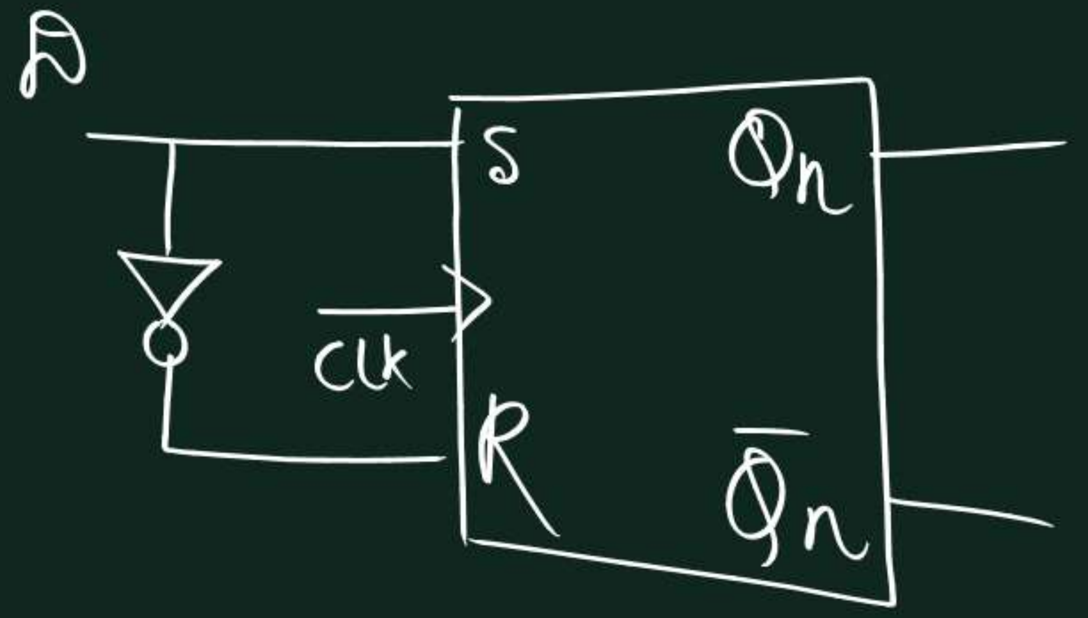
D \ Q_n	0	1
0	X	1
1		

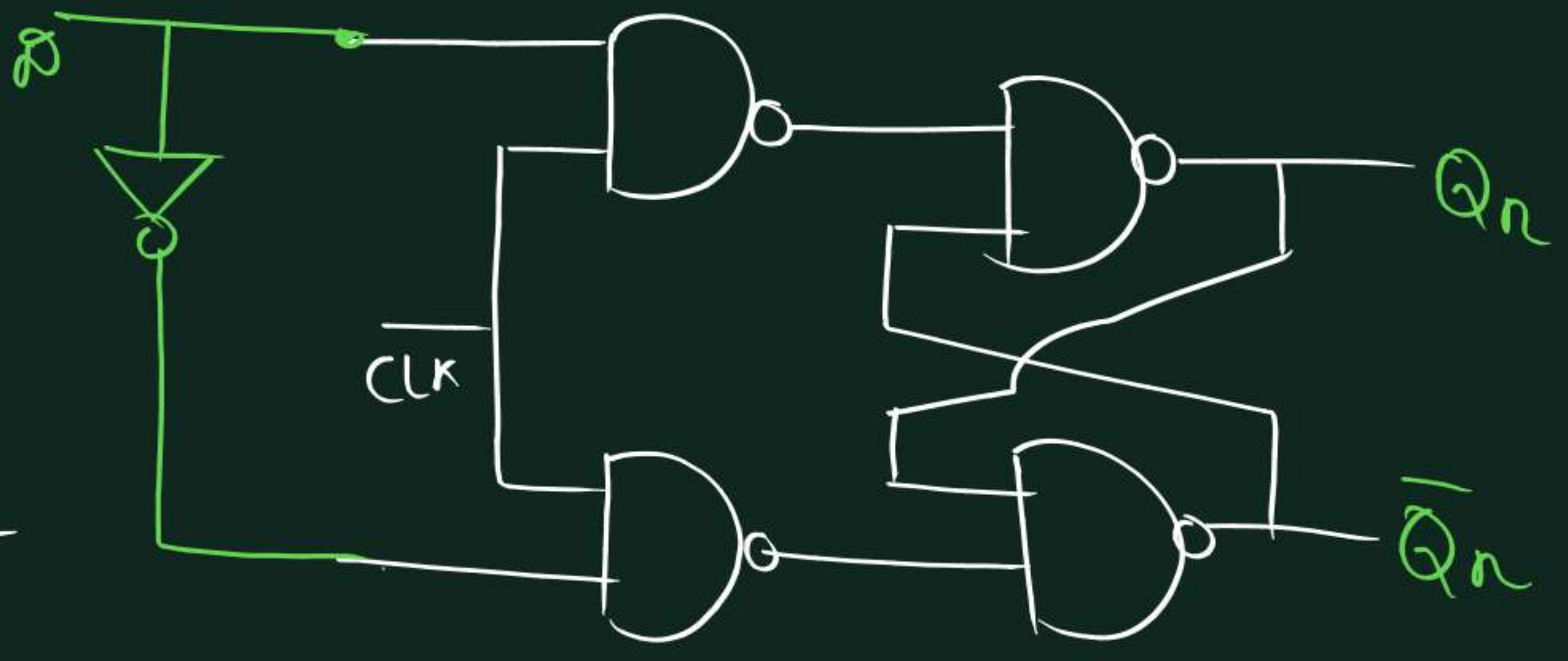
$\boxed{R = \overline{D}}$

ER.CJHA@gmail.com

$S = D$

$R = \overline{D}$





Q.4 Design a D FF by using JK FF?

HW

$J(D, Q_n)$

$K(D, Q_n)$

D	Q_n	Q_{n+1}	J	K
0	0	0		
0	1	0		
1	0	1		
1	1	1		

Q.5 Design a JK FF by using SR FF?

Q.6 Design a JK FF by using SR FF?

Q.7 Design a CJ by using SR FF?

C	J	Q_{n+1}
0	0	1
0	1	0
1	0	$\overline{Q}_n$
1	1	Q_n

CJ → chandan Jha

Comment

S = ?

R = ?

S = (C, J, Qn)

R = (C, J, Qn)

Step (1)

C	J	Q_n	Q_{n+1}	S	R
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

C	J	Q_{n+1}
0	0	1
0	1	0
1	0	Q_n
1	1	Q_n

Flip Flops

Discussion


comment
B.Tech
THANK YOU GW
SOLDIERS !

EC/EE/CS & IT/IN

Digital Electronics

Asynchronous Counter

LECTURE NO. 9

Chandan Jha Sir (CJ Sir)

ज़िंदगी कि असली उड़ान बाकी है
जिंदगी के कई इम्तेहान अभी बाकी है
अभी तो नापी है मुट्ठी भर ज़मीन हमने
अभी तो सारा आसमान बाकी है

Design a CJ by using SR FF?

C	J	Q_{n+1}
0	0	1
0	1	0
1	0	$\overline{Q_n}$
1	1	Q_n

Step-1 & step 2.

C	J	Q_n	Q_{n+1}	S	R
0	0	0	1	1	0
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	1	0	0	0	X
1	1	1	1	X	0

C	J	Q_{n+1}
0	0	1
0	1	0
1	0	$\overline{Q_n}$
1	1	Q_n

Q_n	Q_{n+1}	S	R
0	0	0	X
→ 0	1	1	0
1	0	0	1
1	1	X	0

Step 3 & Step 4

$$S(C, J, Q_n) = \Sigma m(0, 4) + \Sigma d(1, 7)$$

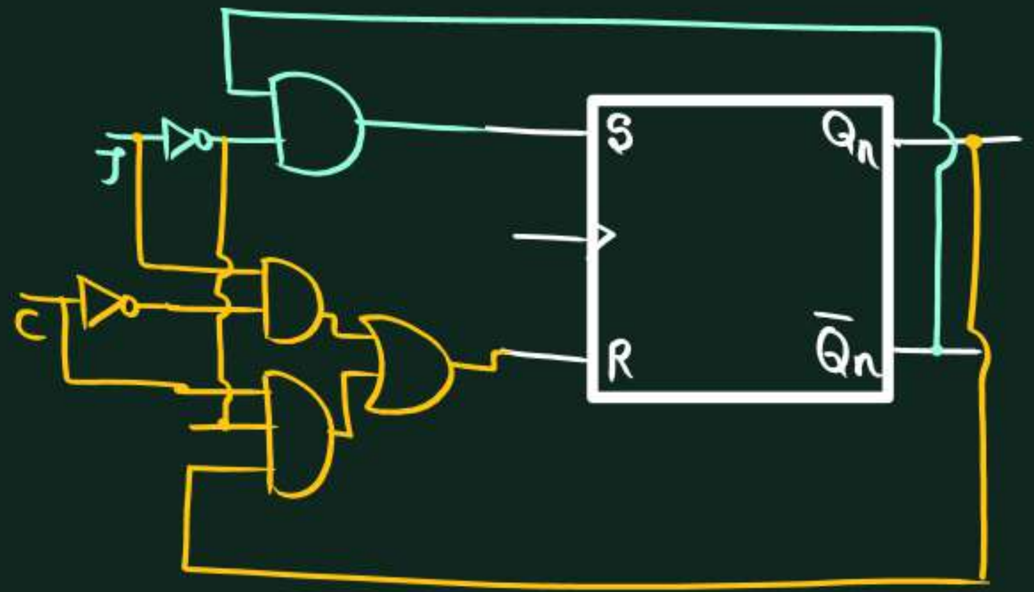
$C \backslash JQ_n$	00	01	11	10
0	1	X		
1	1		X	

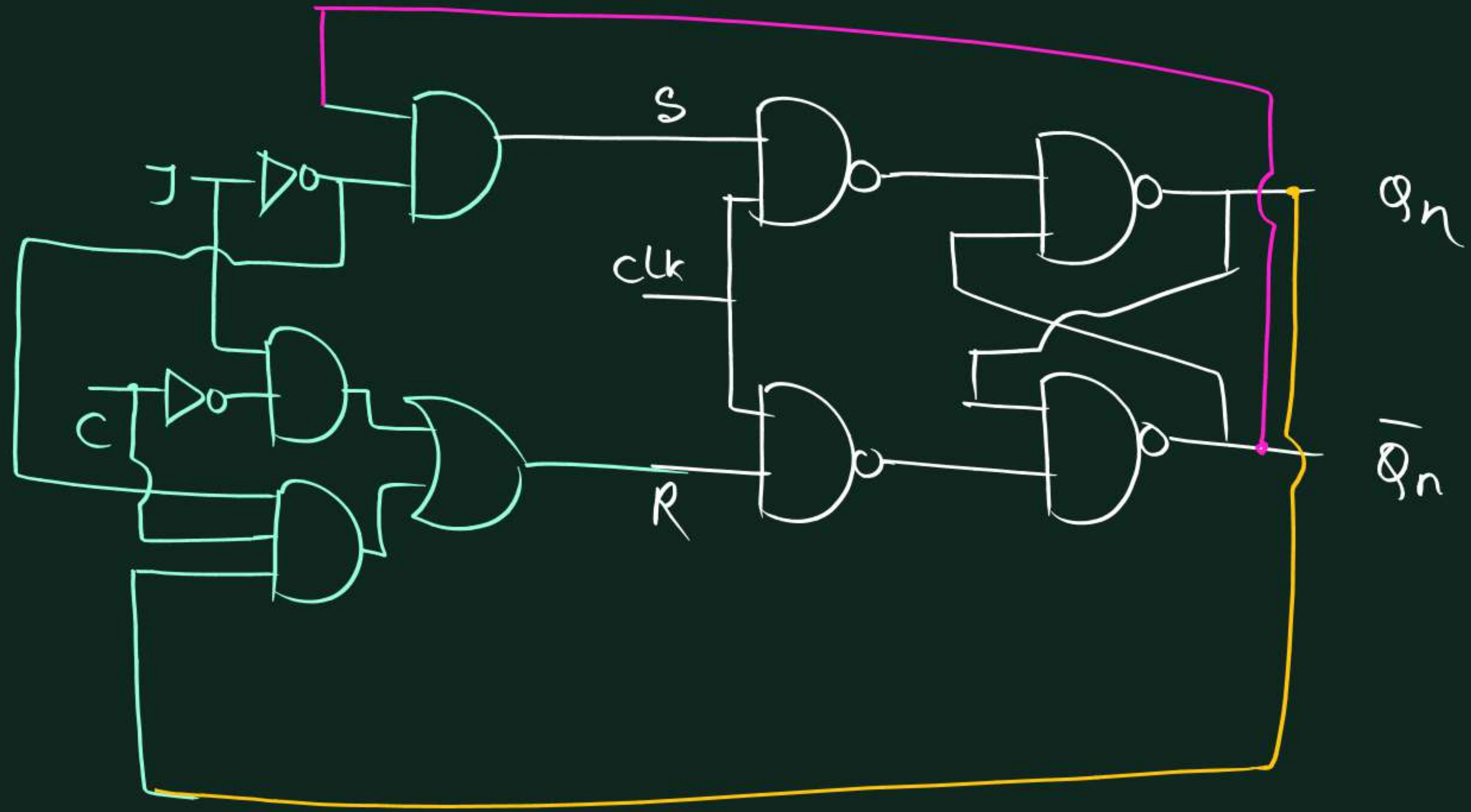
$$S = \bar{J}\bar{Q}_n$$

$$R(C, J, Q_n) = \Sigma m(3, 5) + \Sigma d(2, 6)$$

$C \backslash JQ_n$	00	01	11	10
0			1	X
1		1		X

$$R = C\bar{J}Q_n + \bar{C}J$$

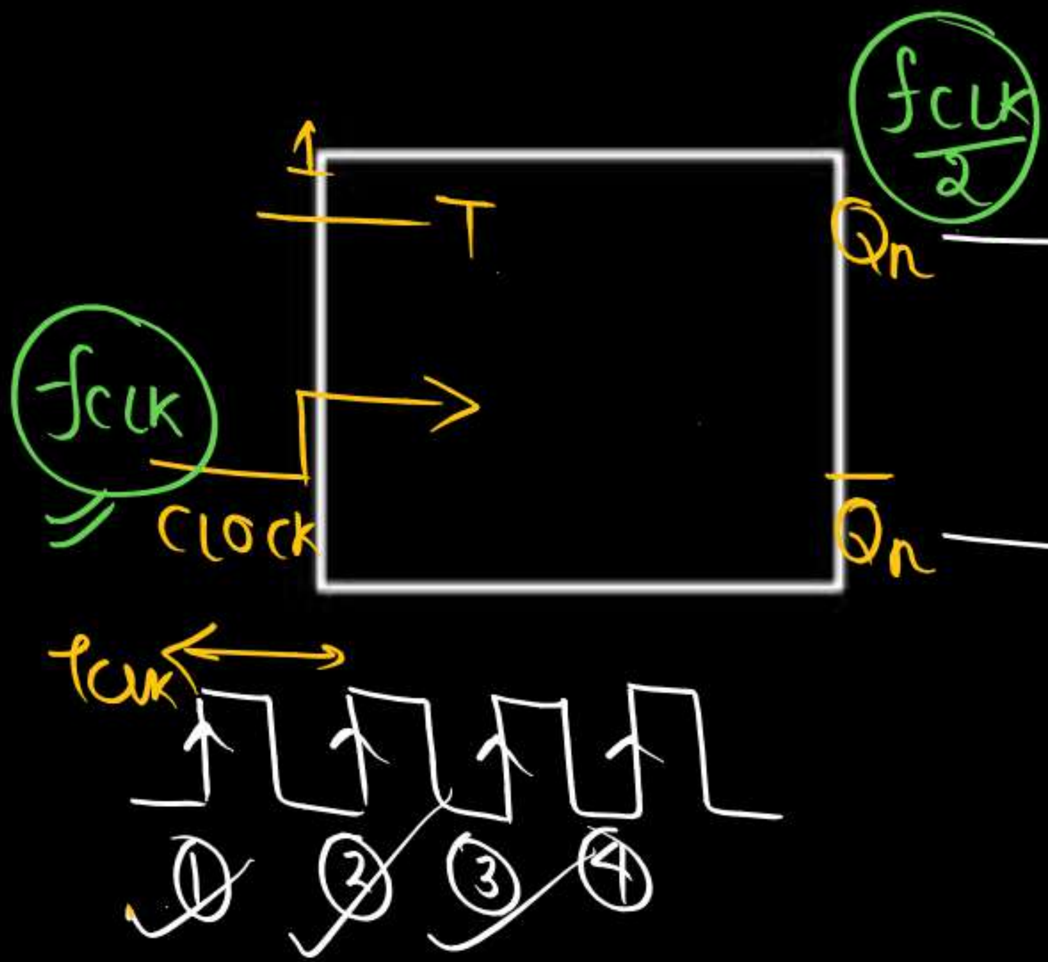

J
C
S
R
Qn
$\bar{Q}n$


J
C
S
clk
R
Qn
$\bar{Q}n$

Design a JK FF by using SR FF FF?

J	K	Q_n	Q_{n+1}	S	R
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

TOGGLE MODE OF THE FLIP FLOP



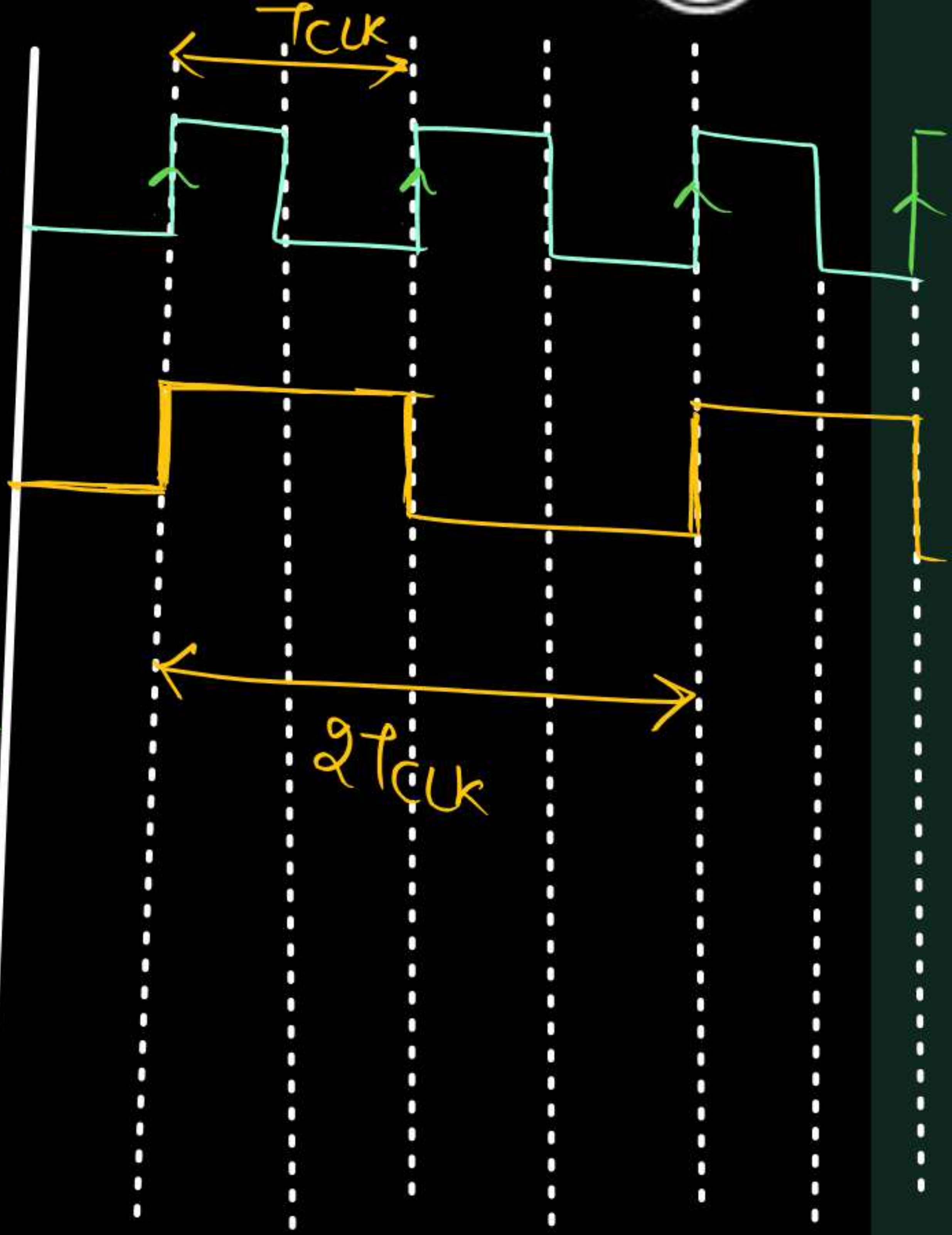
Q_n: $0 \to 1 \to 0 \to 1 \to \ldots$

$\overline{Q_n}$: $1 \to 0 \to 1 \to 0 \to \ldots$

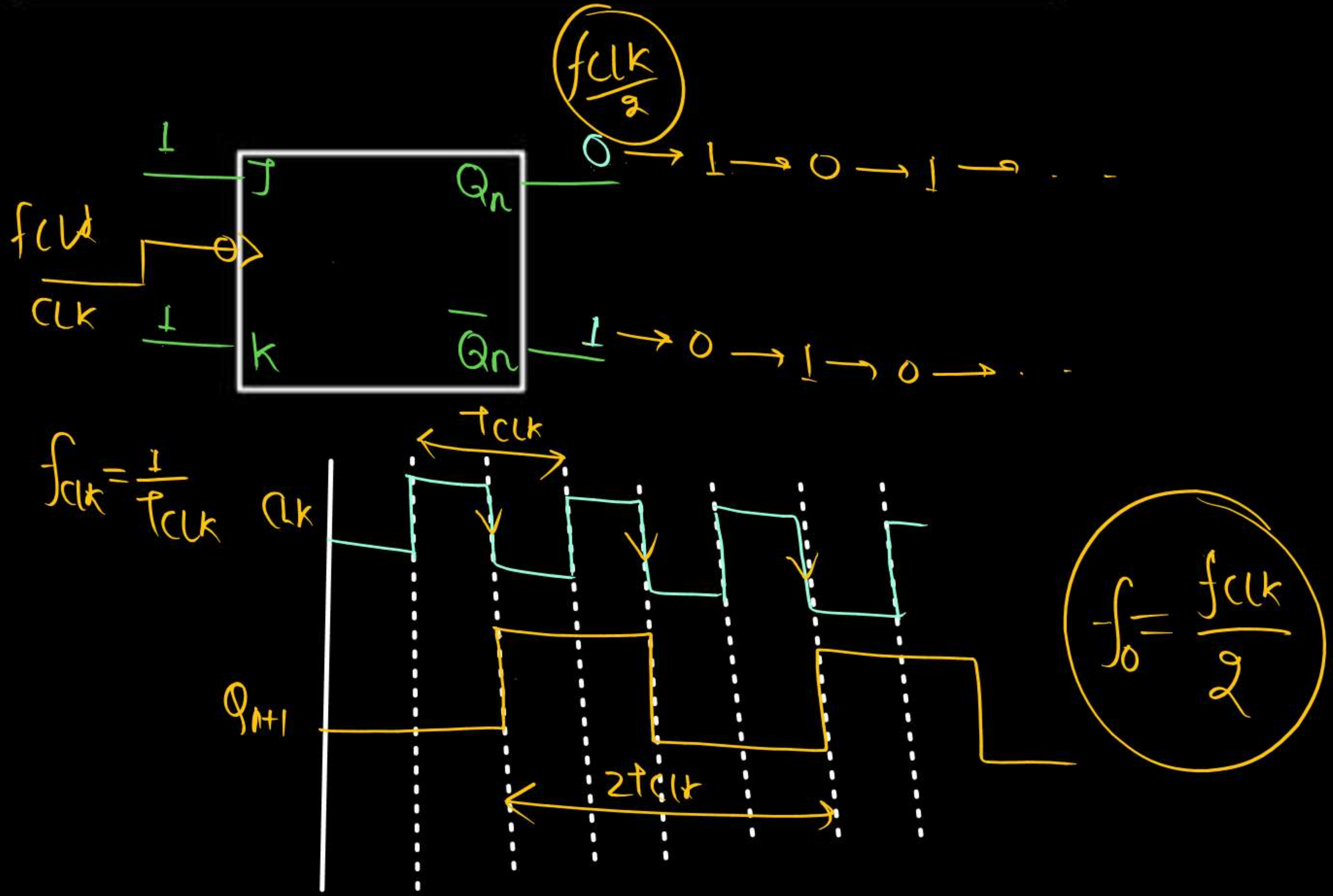
Q_{n+1}

$f_{clk} = \frac{1}{T_{clk}}$ CLOCK

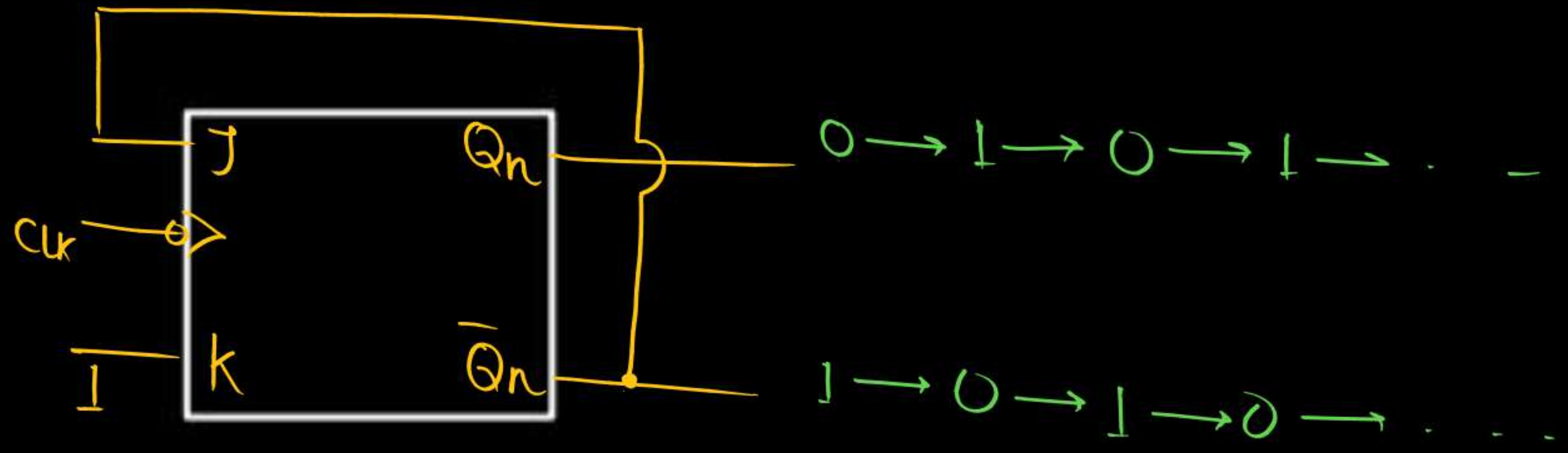
$f_0 = \frac{1}{2T_{clk}} = \frac{f_{clk}}{2}$

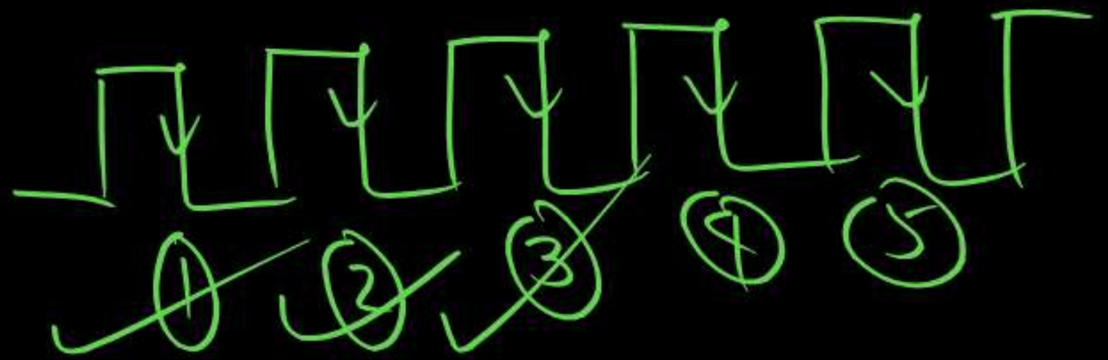


TOGGLE MODE OF THE FLIP FLOP

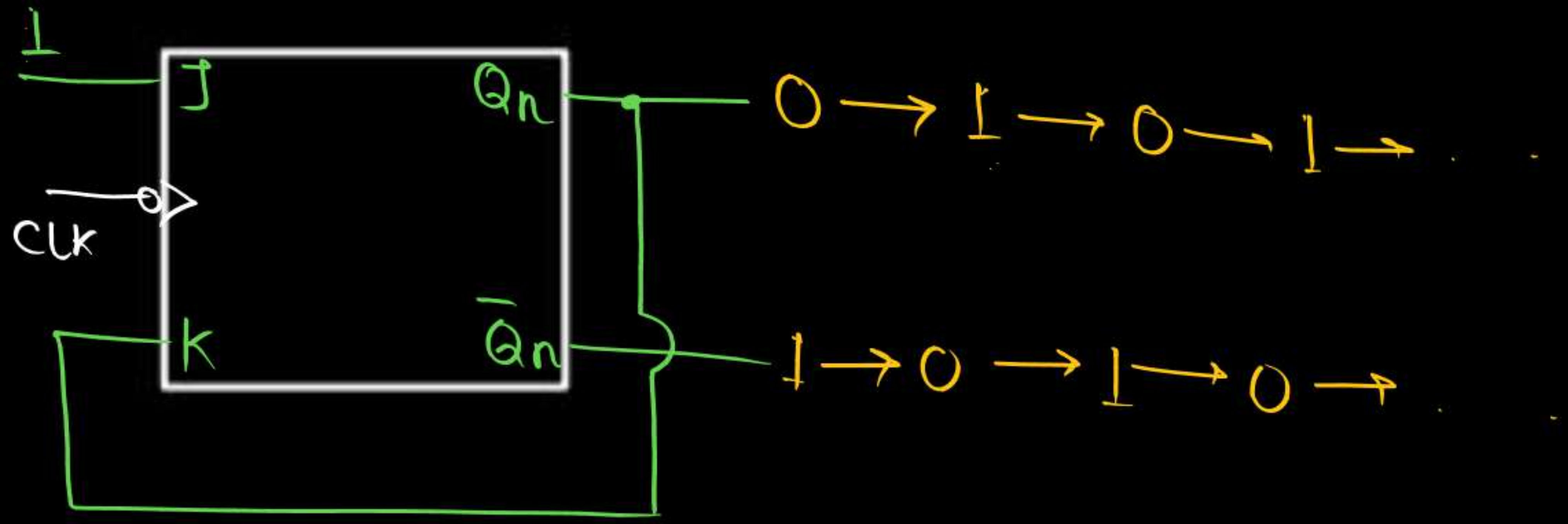


TOGGLE MODE OF THE FLIP FLOP

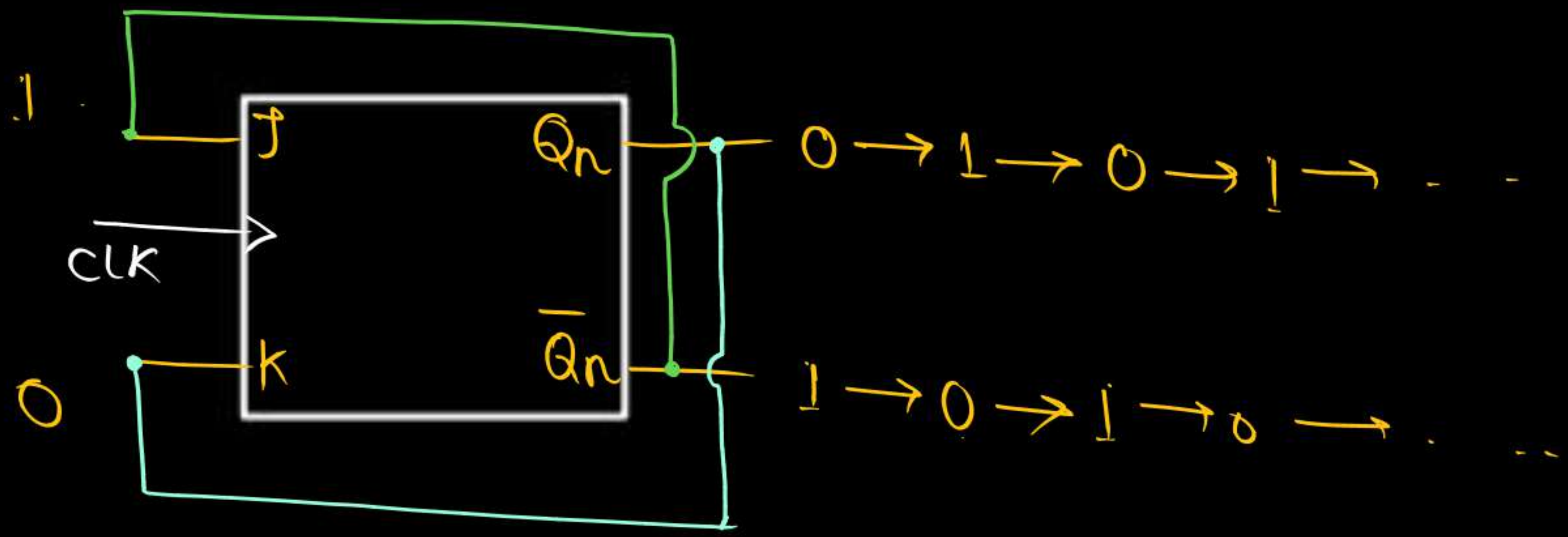




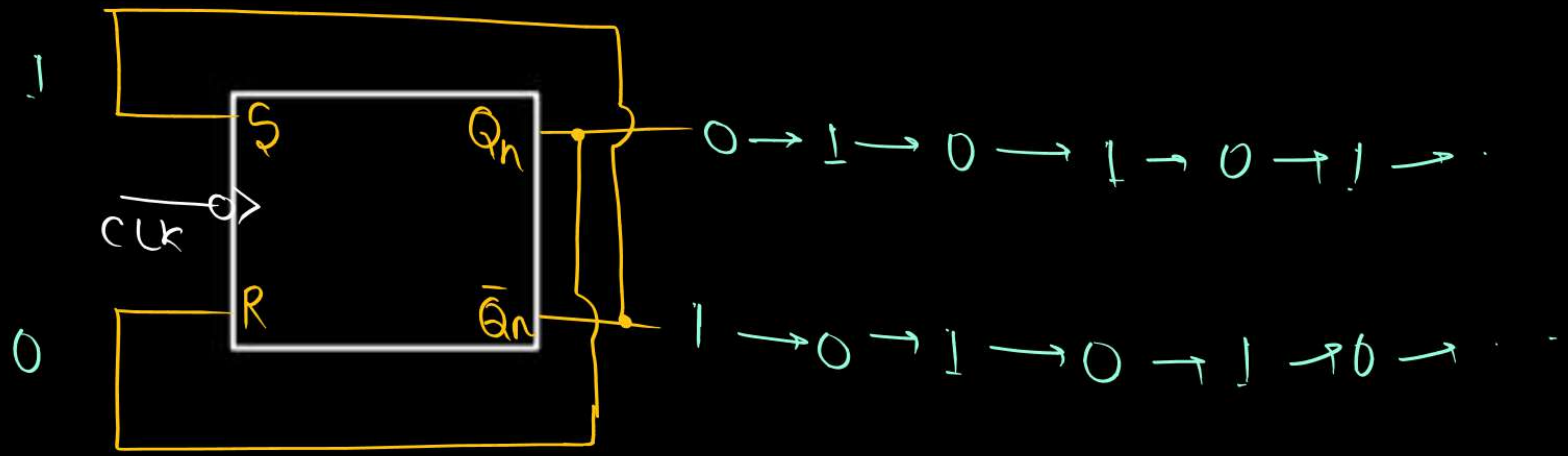
TOGGLE MODE OF THE FLIP FLOP



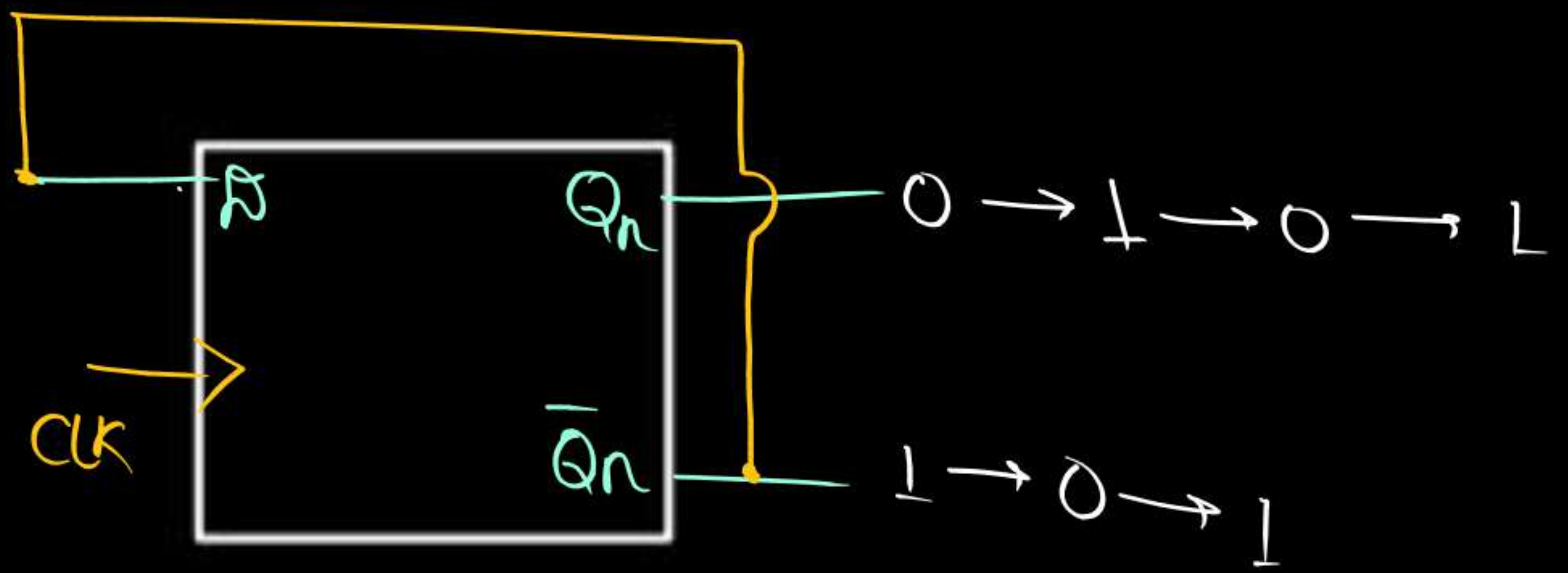
TOGGLE MODE OF THE FLIP FLOP



TOGGLE MODE OF THE FLIP FLOP



TOGGLE MODE OF THE FLIP FLOP



Counters

1. Counter are used to count number of clock.
2. Counters are also known as frequency divider circuit.

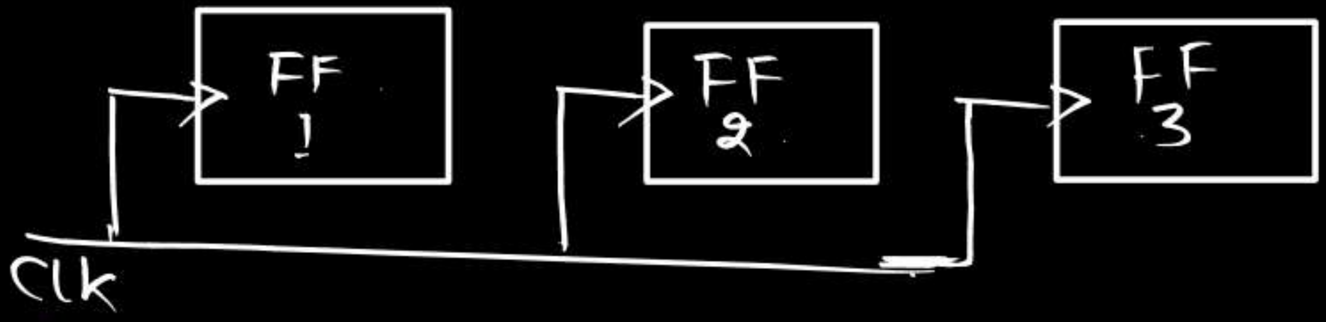
① Synchronous counter

② Asynchronous counter

UP	DOWN	RANDOM
1	5	1
2	4	3
3	3	2
4	2	5
5	1	4

Synchronous Counters

1. All the flip flops are connected with same clock.



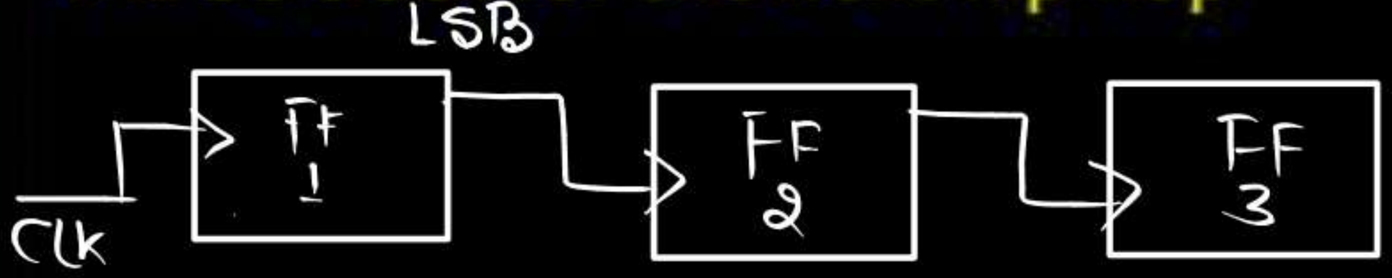
(2) fast

(3) All type of counting are possibble.

(4) Ex. Ring, Johnson counter

Asynchronous Counters

1. Only one Flip Flop having External clock and the outputs of that flip flop will be clock for the next flip flop



(2) Slow

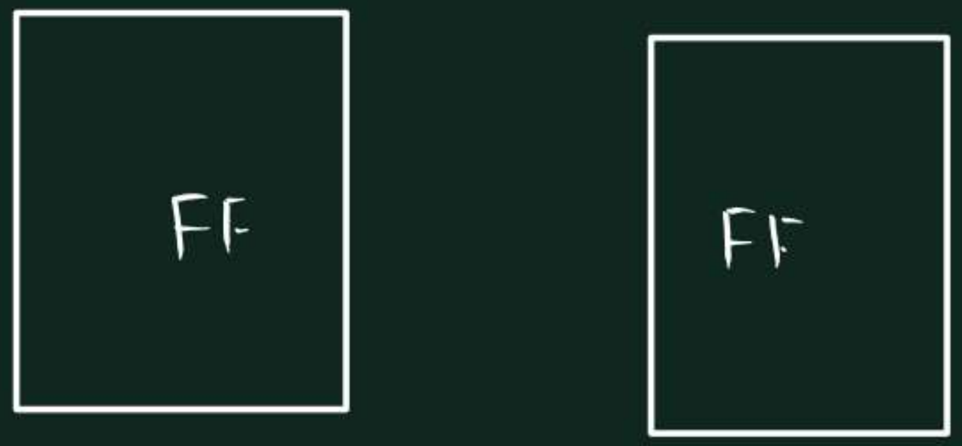
(3) Generally UP & DOWN counting are possible.

(4) Ex. Ripple counter

0, 1

$\downarrow$

2



$$\left\{\begin{matrix}0 & 0\\0 & 1\\1 & 0\\1 & 1\end{matrix}\right\}$$

$$\boxed{\text{Maximum number of states} = 2^n}$$

$n \rightarrow$ Number of FF

MOD

Number of states used by the counter.

$0 \to 1 \to 2 \to 3 \to 4$

MOD = 5

$7 \to 8 \to 9 \to 10 \to 11$

MOD = 5

$60 \to 61 \to 63 \to 65 \to 101$

MOD = 5

$$\boxed{MOD(M) \leq 2^n}$$

$$M \leq 2^n$$

$$\boxed{n \geq \log_2 M}$$

Q MOD-10 counter.

no. of FF ?

$$M \leq 2^n$$

$$n \geq \log_2 M$$

$$n \geq \log_2 10$$

$n \geq 3.$ something

$$\boxed{n \approx 4}$$

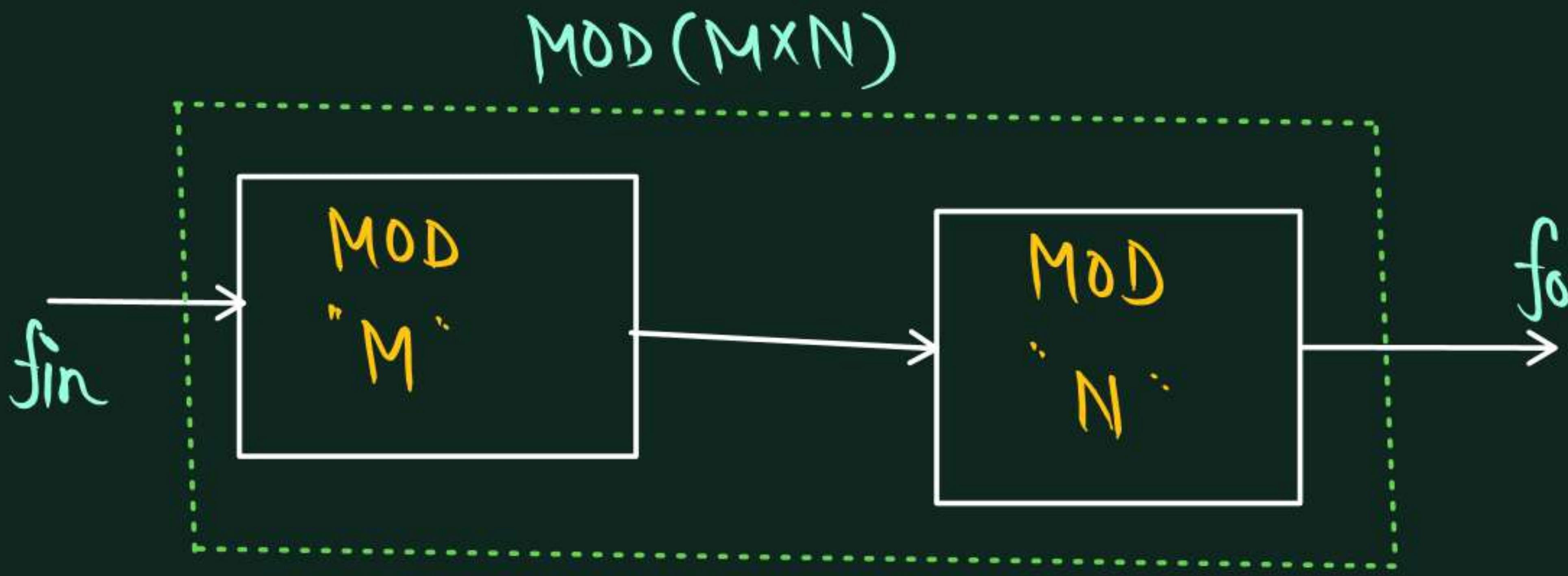
₹.10

NOTE

1.

$$f_{out} = \frac{f_{in}}{M}$$

2.



$$f_{out} = \frac{f_{in}}{M \times N}$$

BCD

→ Binary coded decimal

→ Every decimal number are represented by 4 bit.

0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

BCD

BCD

100
101
102
103
104
105
105
107
106
109

MOD-10

Q When MOD '5' counter is cascaded by MOD '2' counter Then it will become.

~~(A) MOD-10 counter~~

(B) BCD counter

~~(C) Both (A) & B~~

(D) MOD "7" counter

(E) Sir, Mujhe ata to hai par mai batunga nahi.

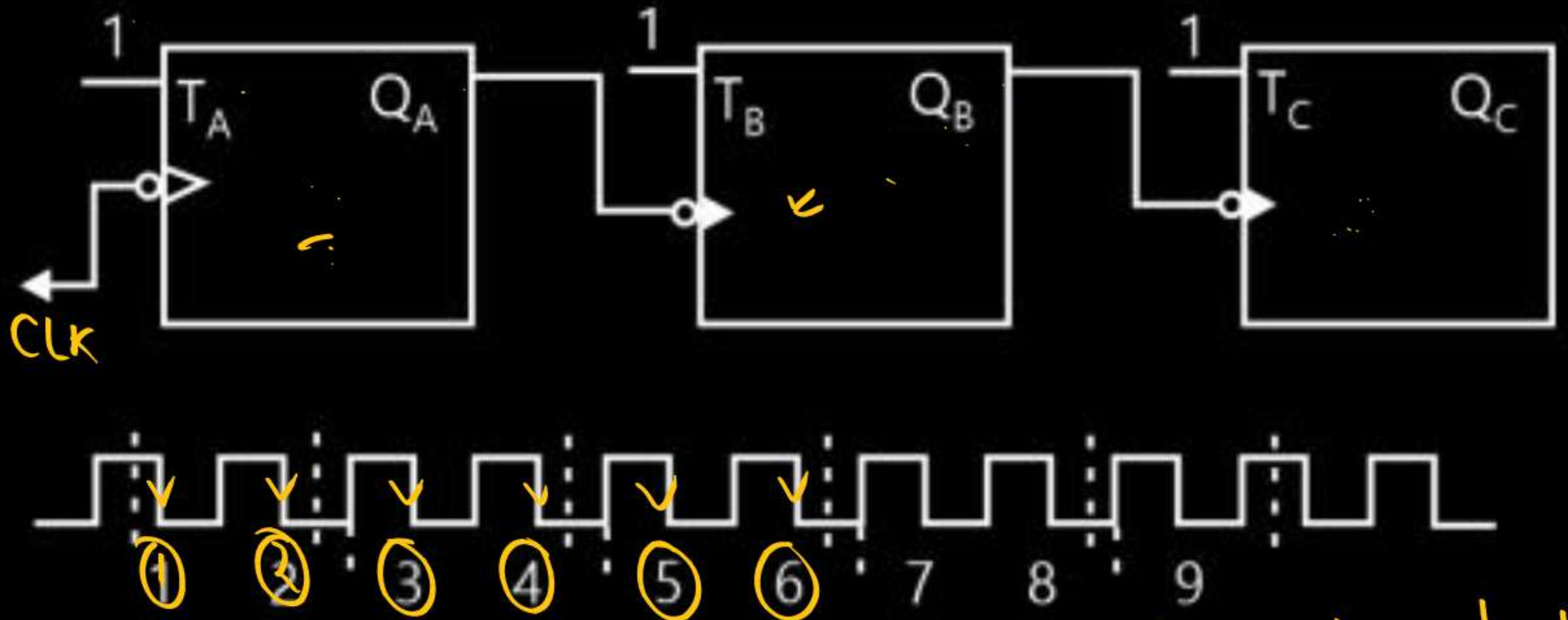
$5 \times 2 = 10$

MOD

काम करो ऐसा कि एक पहचान बन जाए,
हर कदम ऐसा चलो कि निशान बन जाए,
यहां जिंदगी तो हर कोई काट लेता है,
जिंदगी जियो इस कदर कि मिसाल बन जाए।

ASYNCHRONOUS COUNTER → All the FF's are used in toggle MOD.

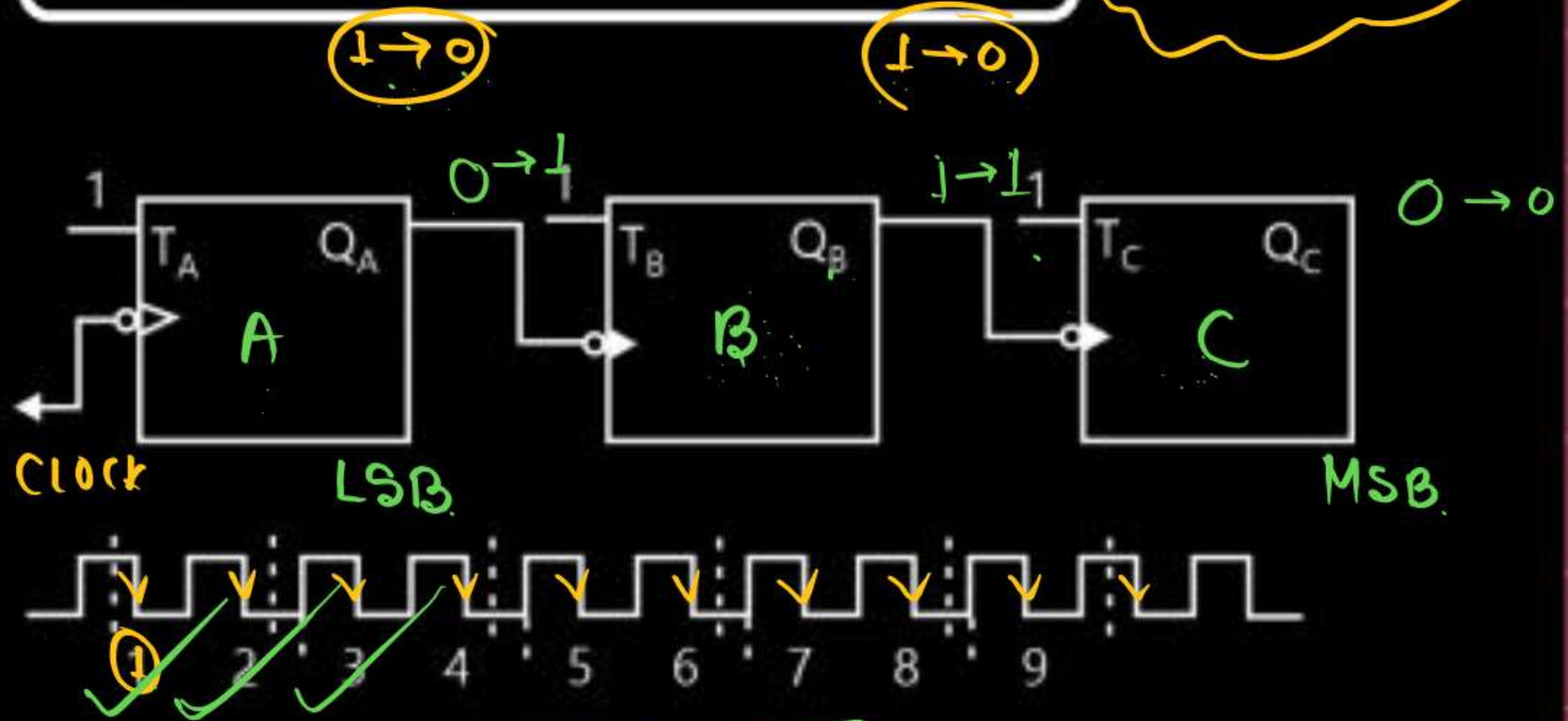
Ripple counter → 3 bit



- Q_A will toggle for every -ve edge of the external clock.
- Q_B will toggle when Q_A goes from $1 \to 0$.
- Q_C will toggle when Q_B goes from $1 \to 0$.

Asynchronous Counter

3bit Ripple counter



$Q_C \; Q_B \; Q_A$

MSB ← Q_C Q_A → LSB

clock	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

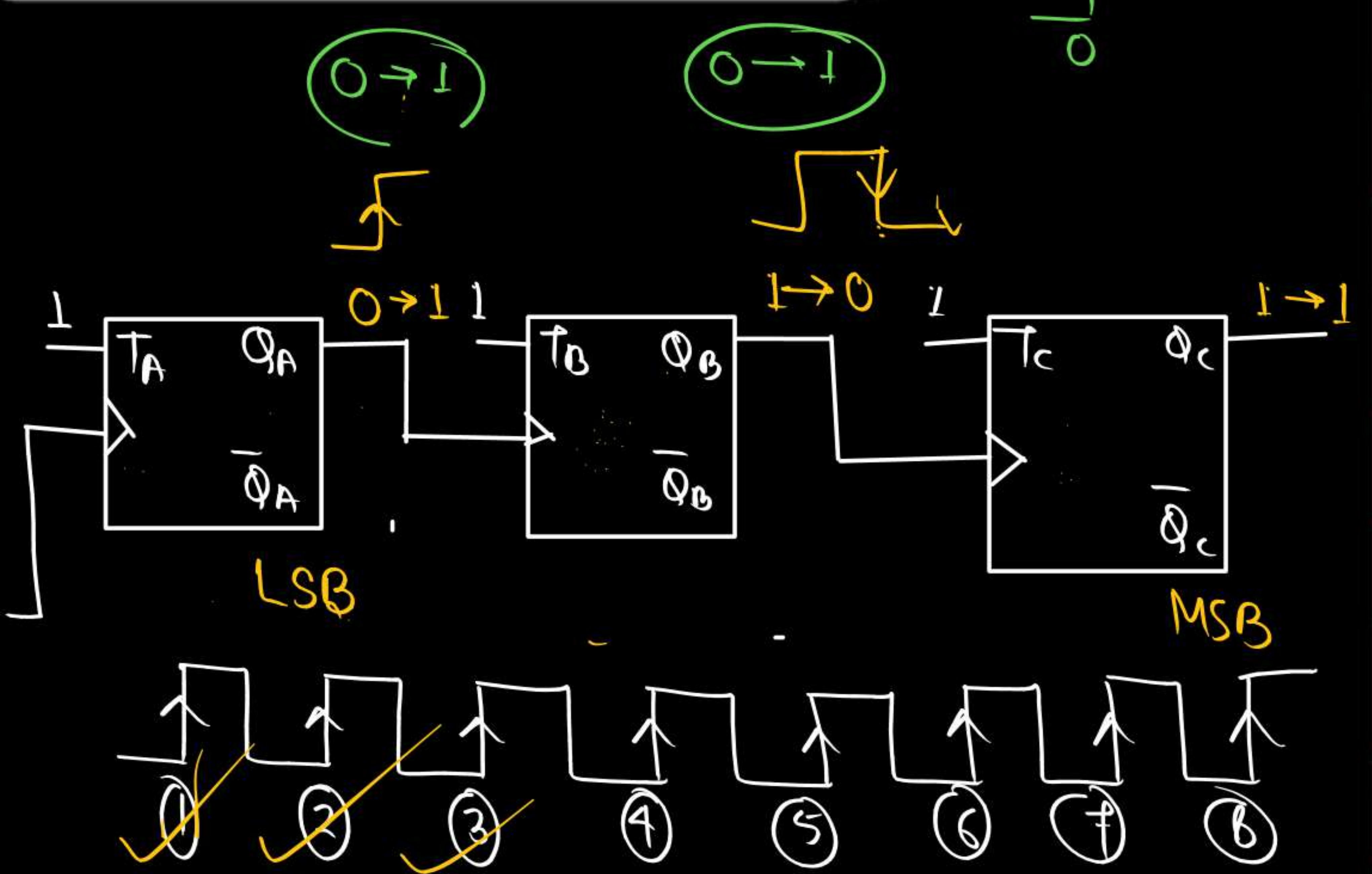
Ext. clk

$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7$

$000 \rightarrow 001 \rightarrow 010 \rightarrow 011 \rightarrow 100 \rightarrow 101 \rightarrow 110 \rightarrow 111$

MOD "8" UP RIPPLE COUNTER

Asynchronous Counter



clock	Q_C	Q_B	Q_A
0	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0

000 → 111 → 110 → 101 → 100 → 011 → 010 → 001 → 000

MOD-8 DOWN RIPPLE COUNTER

Asynchronous Counter

clock	Q_c	Q_B	Q_c
0			
1			
2			
3			
4			
5			
6			
7			
8			

Asynchronous Counter

clock	Q_c	Q_B	Q_c
0			
1			
2			
3			
4			
5			
6			
7			
8			

Asynchronous Counter

Bubble

0 ⟶ −ve.

$\overline{Q}$ ⟶ −ve

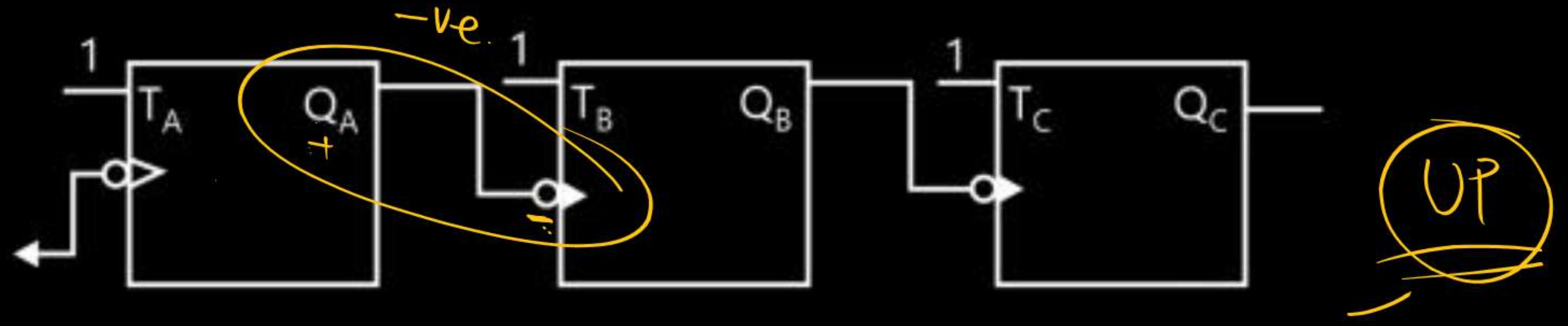
−ve → UP
+ve → DOWN

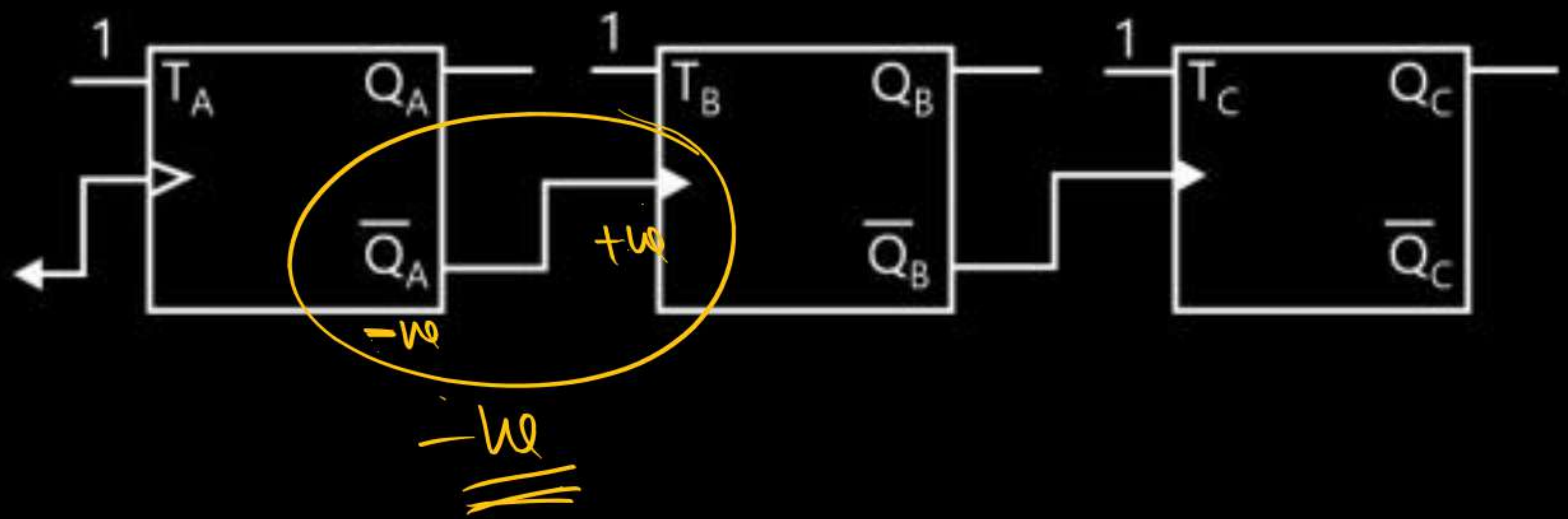
clock	Q_c	Q_B	Q_c
0			
1			
2			
3			
4			
5			
6			
7			
8			

Asynchronous Counter

−ve → UP

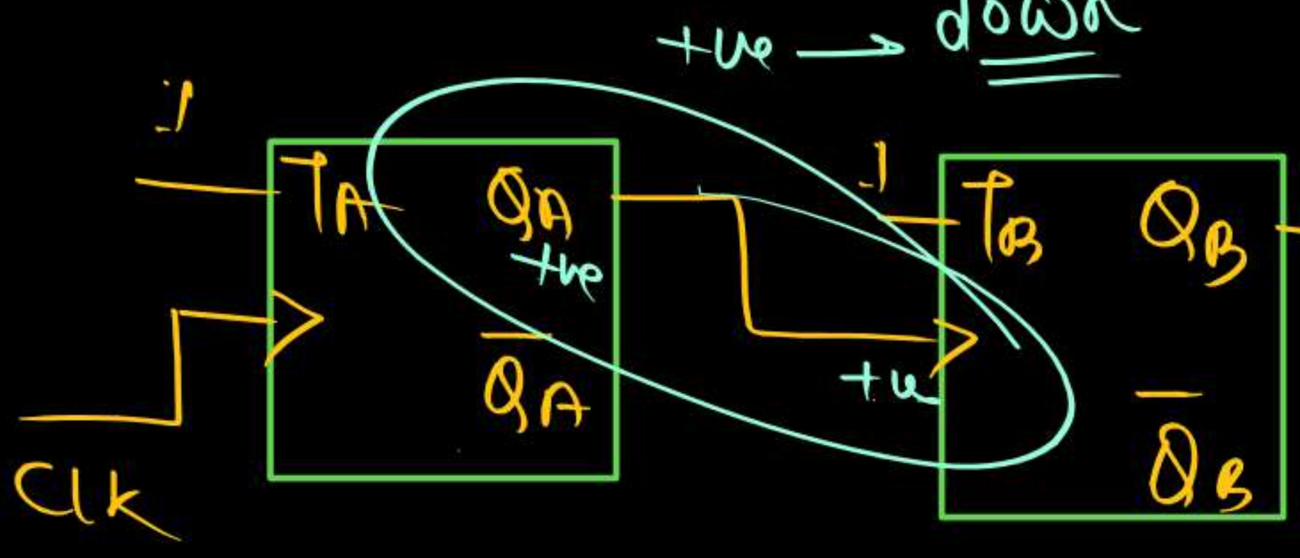
+ve → DOWN

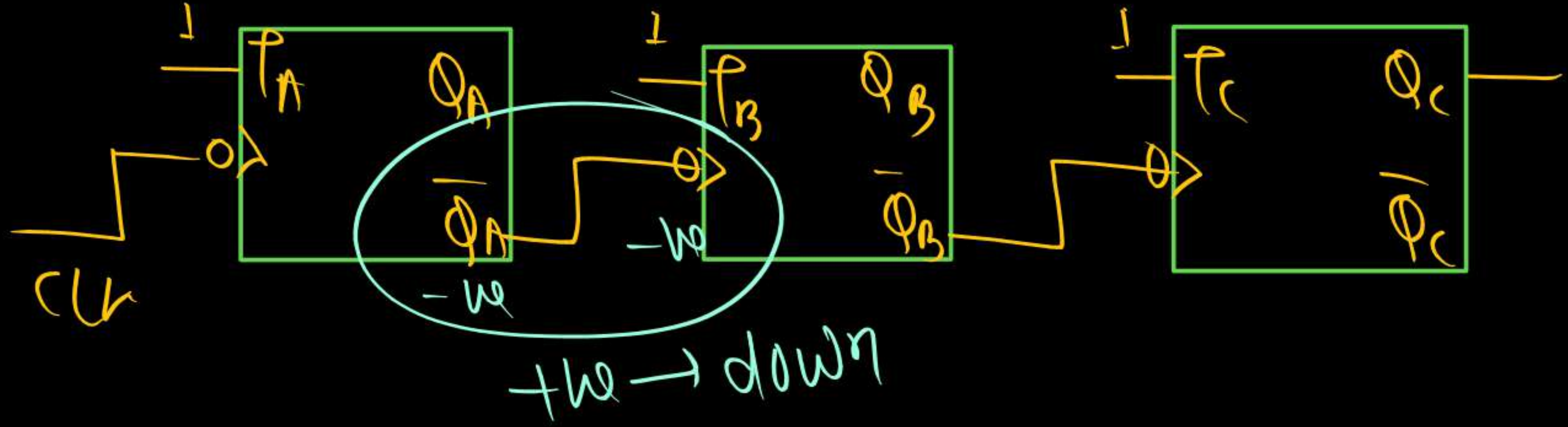




Asynchronous Counter

$n \rightarrow 2^n$

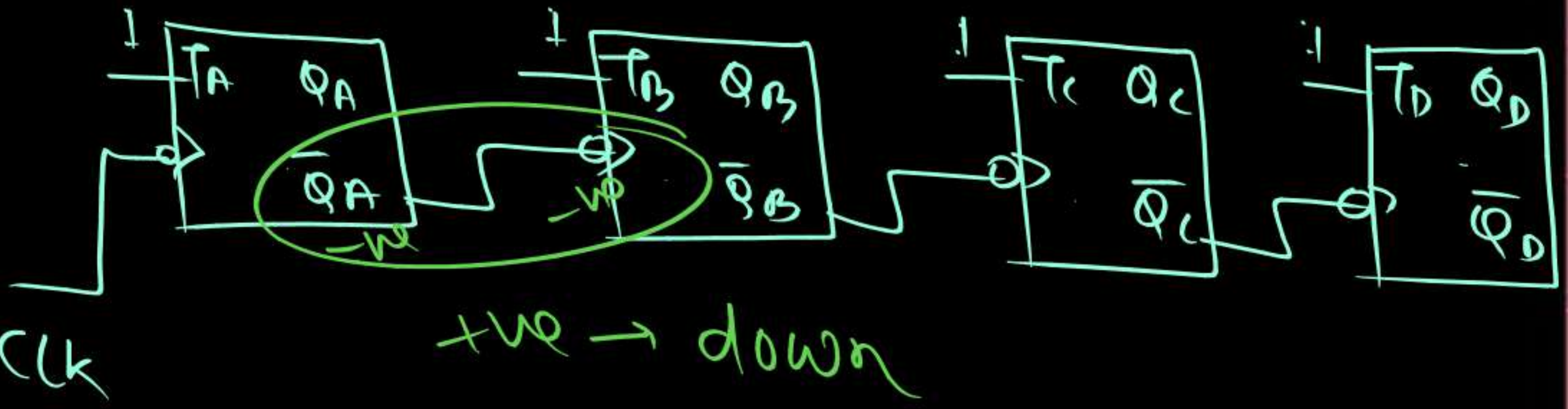




Down counter

Asynchronous Counter

$MOD = 2^4 = 16$



MOD 16 down Ripple counter

clock	Q_c	Q_B	Q_c	Clr
0				
1				
2				
3				
4				
5				
6				
7				
8				

Asynchronous Counter

LDC

#11PM

1000 → 500

200

100

50

20

10

5

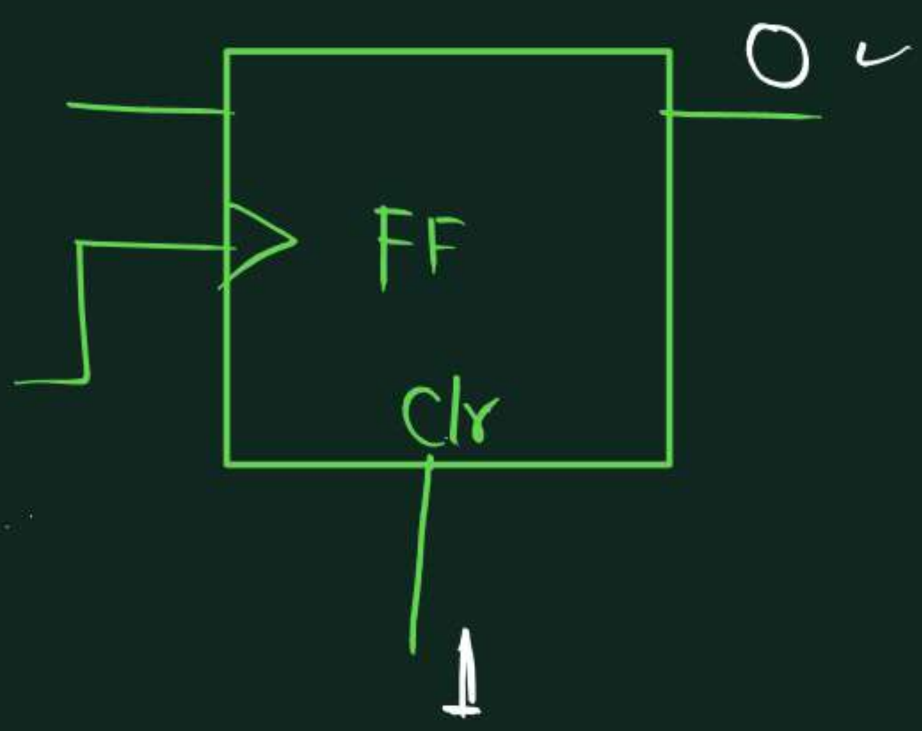
2

1

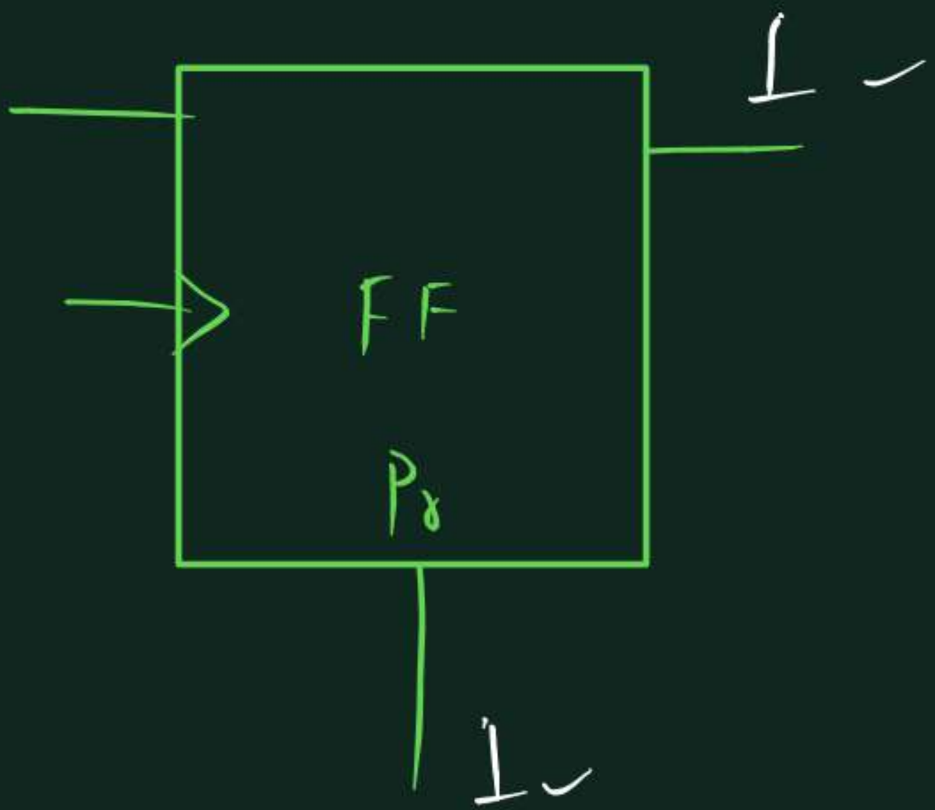
0

clock	Q_c	Q_B	Q_c	Clr
0				
1				
2				
3				
4				
5				
6				
7				
8				

Reset (Clr)



Preset

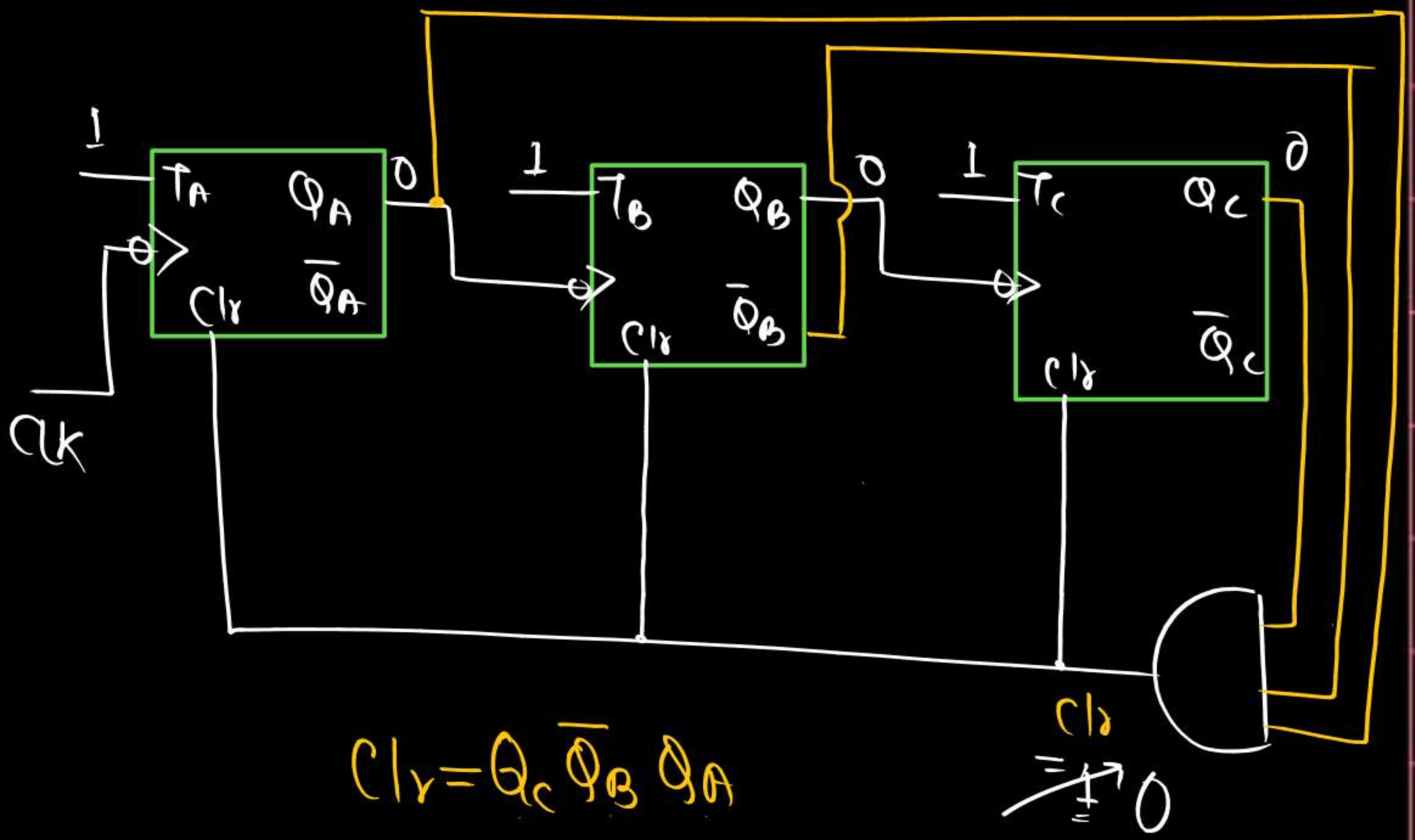


Asynchronous Counter

UP ✓ $Clr = Q_C \cdot \bar{Q}_B \cdot Q_A$

101 → 5 MOD

MOD 5 UP COUNTER



$Clr = Q_C \bar{Q}_B Q_A$

1 0 1

clock	Q_C	Q_B	Q_A	$Clr = Q_C \bar{Q}_B Q_A$
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	$\cancel{1}$ 0	$\cancel{0}$ 0	$\cancel{1}$ 0	$\cancel{1}$ 0
6	0	0	1	0
7	0	1	0	0
8	0	1	1	0

$000 \rightarrow 001 \rightarrow 010 \rightarrow 011 \rightarrow 100$

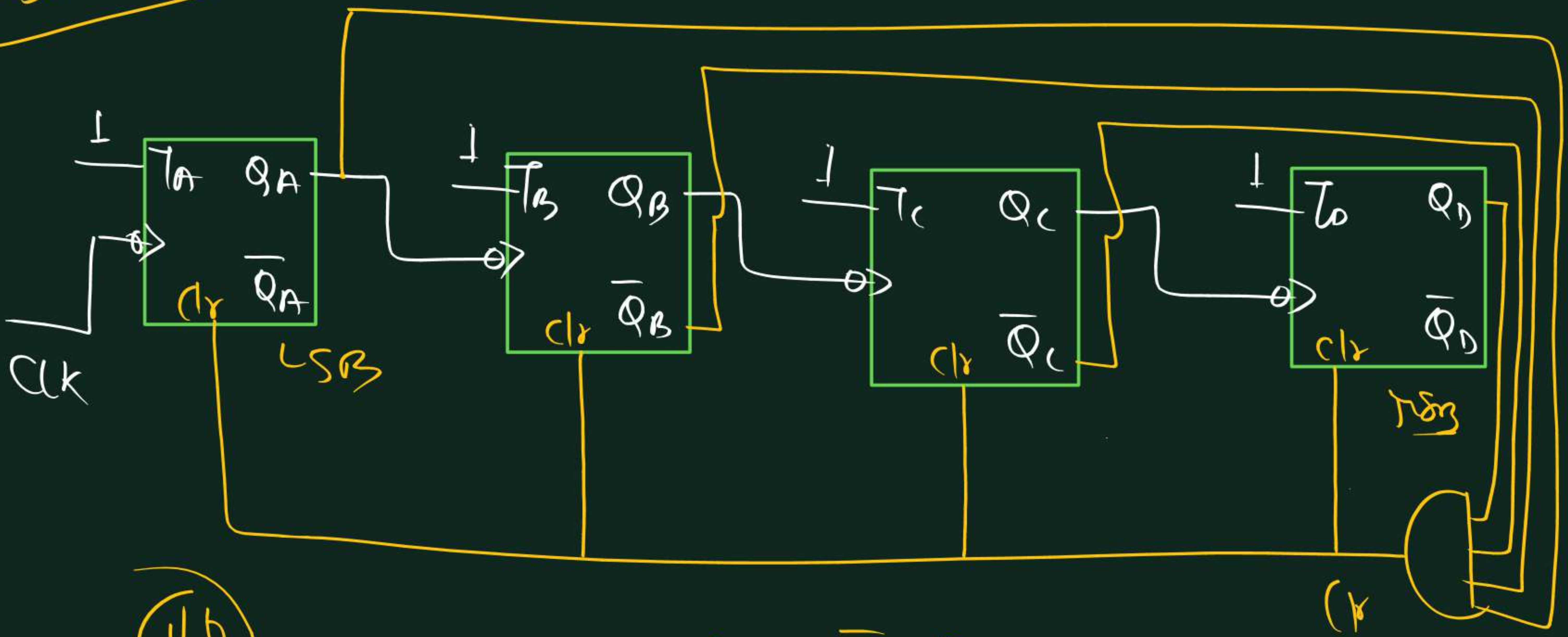
MOD = 5

जीत की ख़ातिर बस जूनून चाहिए,
जिसमें उबाल हो ऐसा खून चाहिए,
ये आसमान भी आ जाएगा ज़मीन पर,
बस इरादों में जीत की गूँज चाहिए।

Asynchronous Counter

clock	Q_c	Q_B	Q_c	Clr
0				
1				
2				
3				
4				
5				
6				
7				
8				

SHANDAR



UP

$$Clr = Q_D \bar{Q}_C \bar{Q}_B Q_A$$

1 0 0 1 → 9

MOD-9 UP Ripple counter

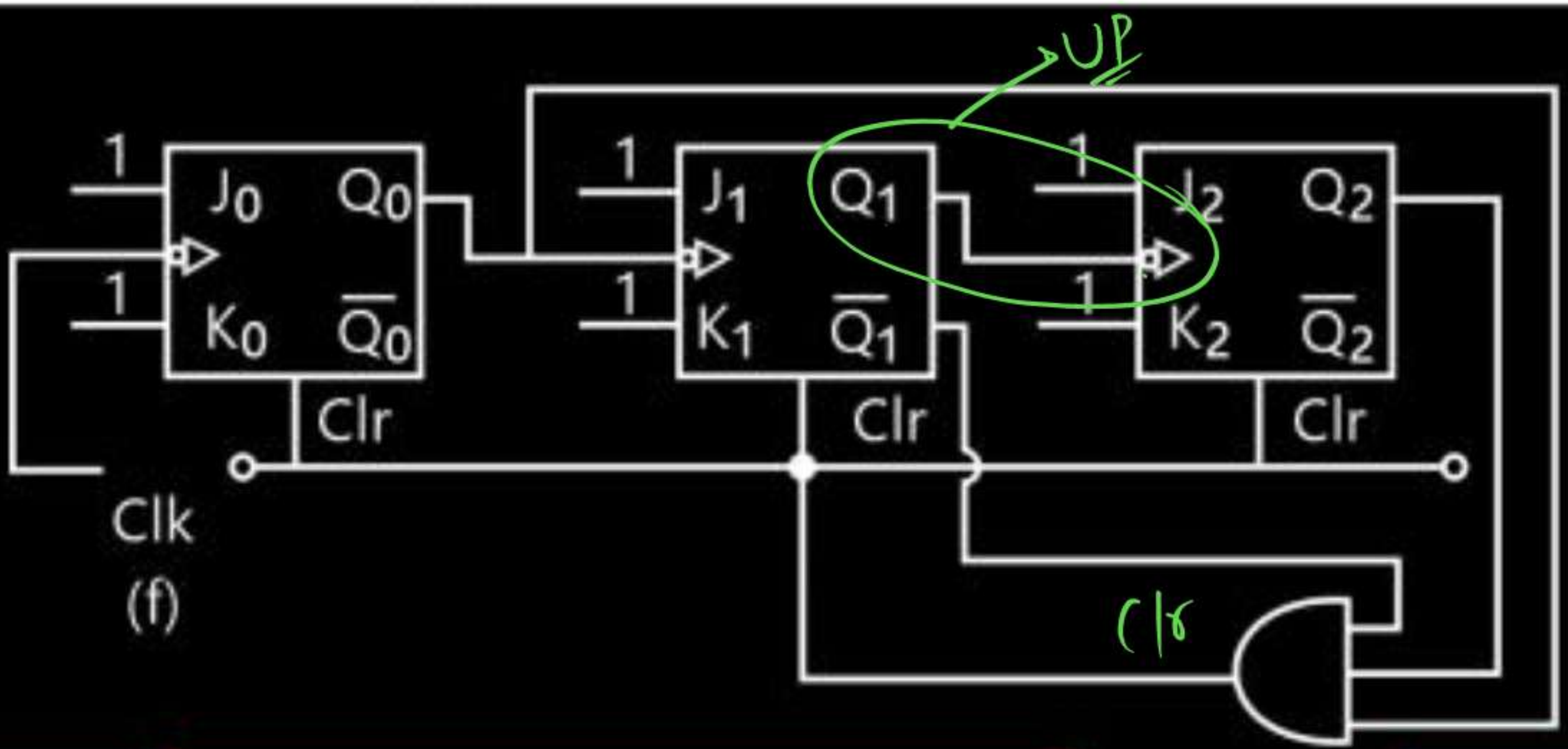
Asynchronous Counter

$Q_D \, Q_C \, Q_B \, Q_A$

Q. Design a BCD counter

$\text{Clr} =$

Q. Which type of counter is shown below?



$Clr = Q_2 \bar{Q}_1 Q_0$

$1\ 0\ 1 = 5$

A. mod 5 down counter

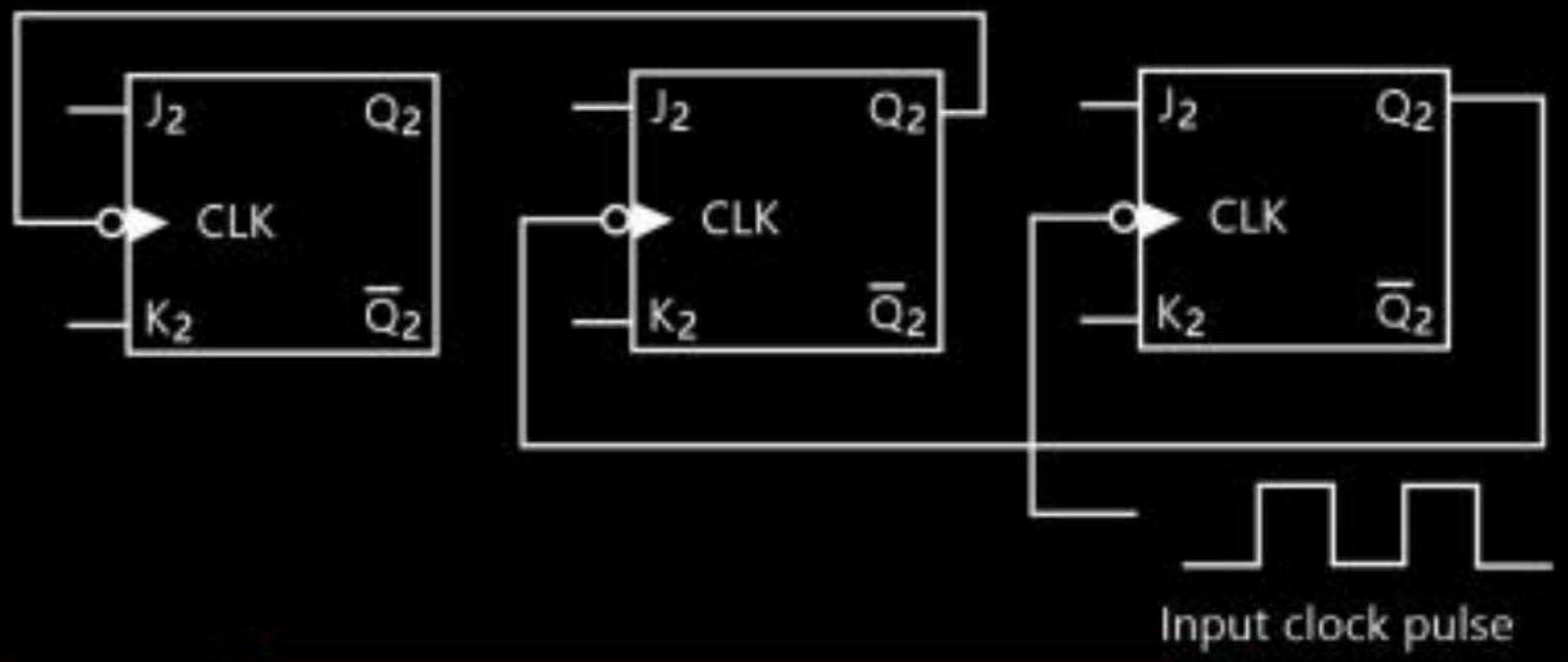
B. mod 5 up counter

C. mod 6 up counter

D. mod 6 down counter

Q. Consider the following counter

If counter starts at 000, what will be the count after 13 clock pulses?



HW

Comment

A 100

B 101

C 110

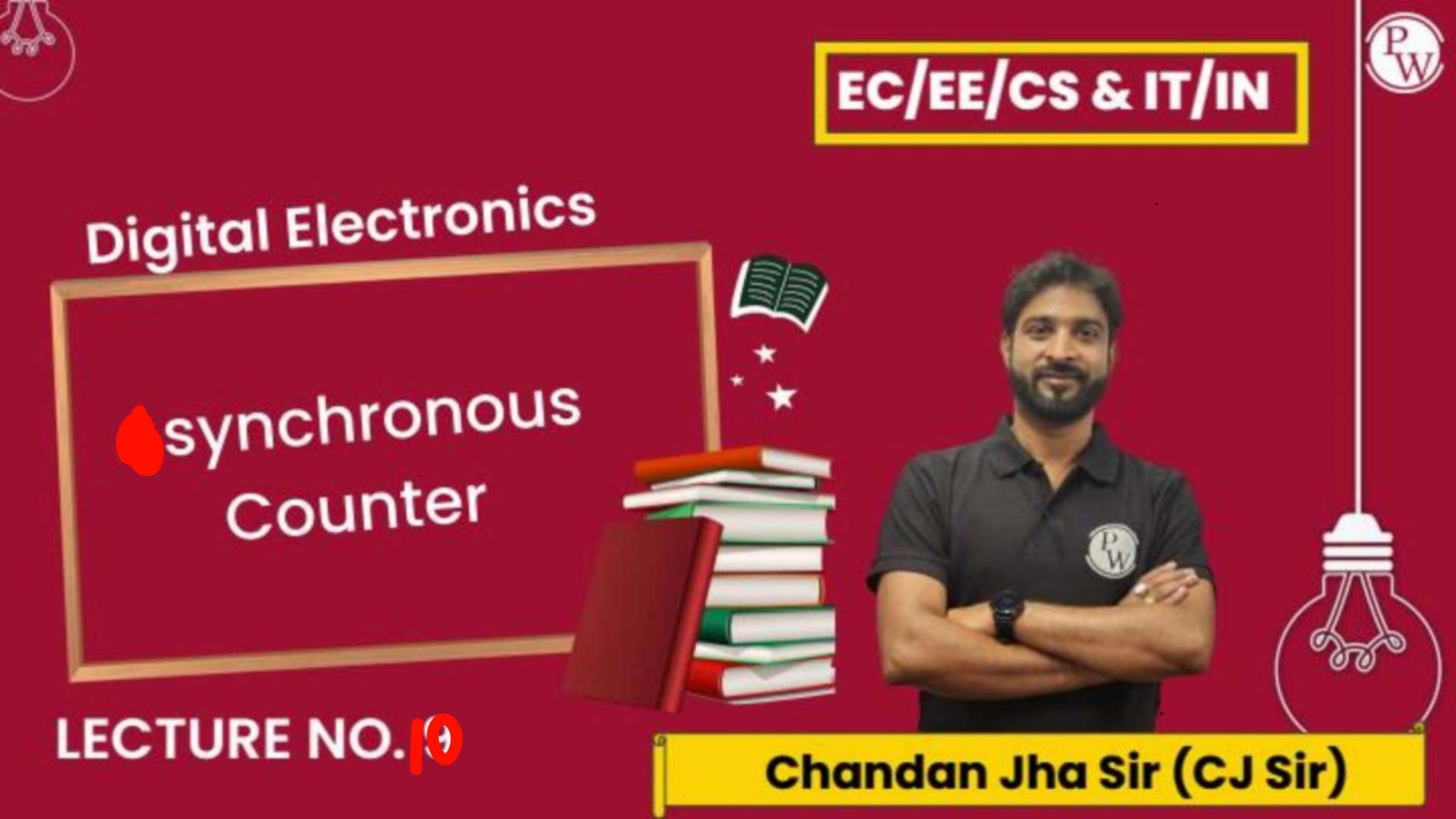
D 111

BCD

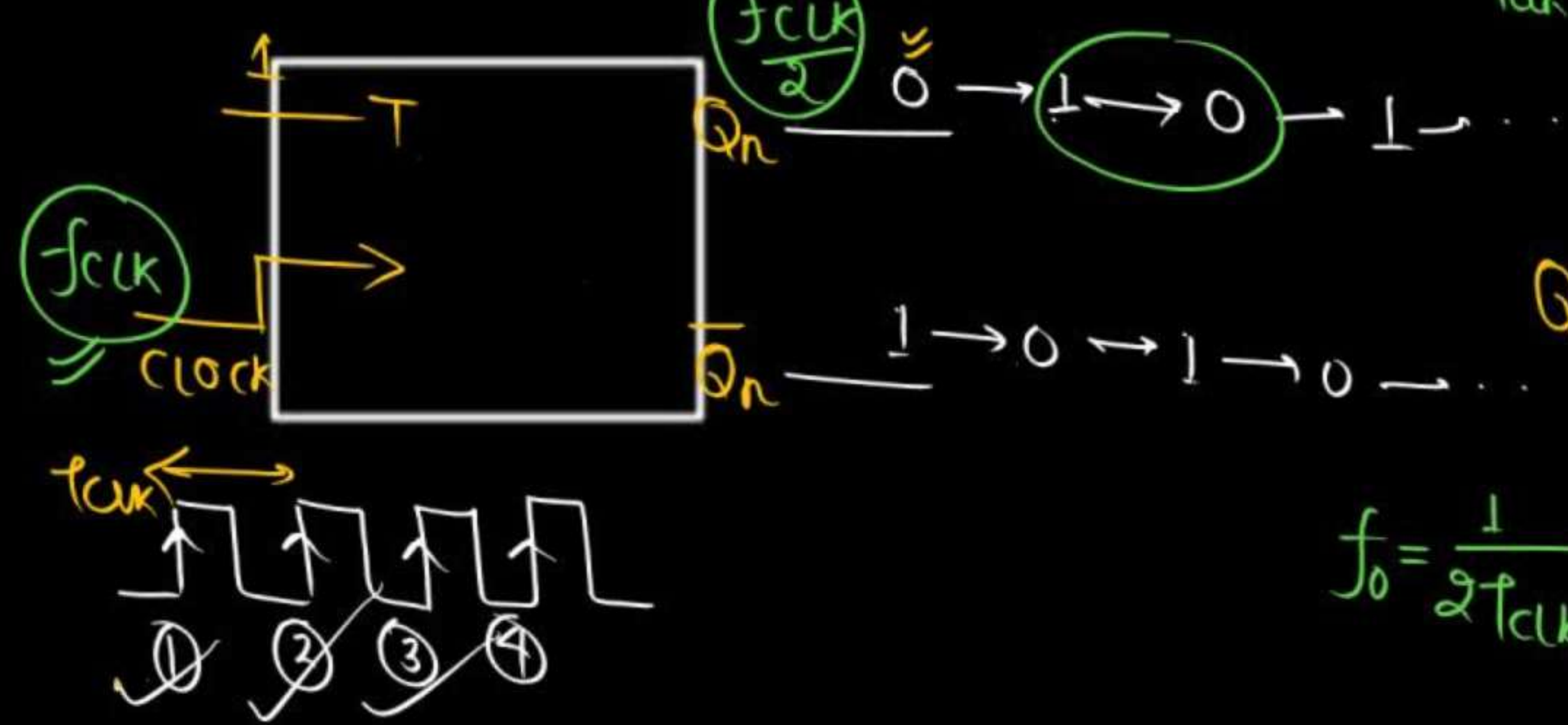
Clr = ?

सपने उनके सच होते हैं,
जिनके सपनों में जान होती है,
पँखो से कुछ नहीं होता,
हौंसलो से उड़ान होती है।


Thank You!


EC/EE/CS & IT/IN
Digital Electronics
synchronous
Counter
LECTURE NO. 10
Chandan Jha Sir (CJ Sir)

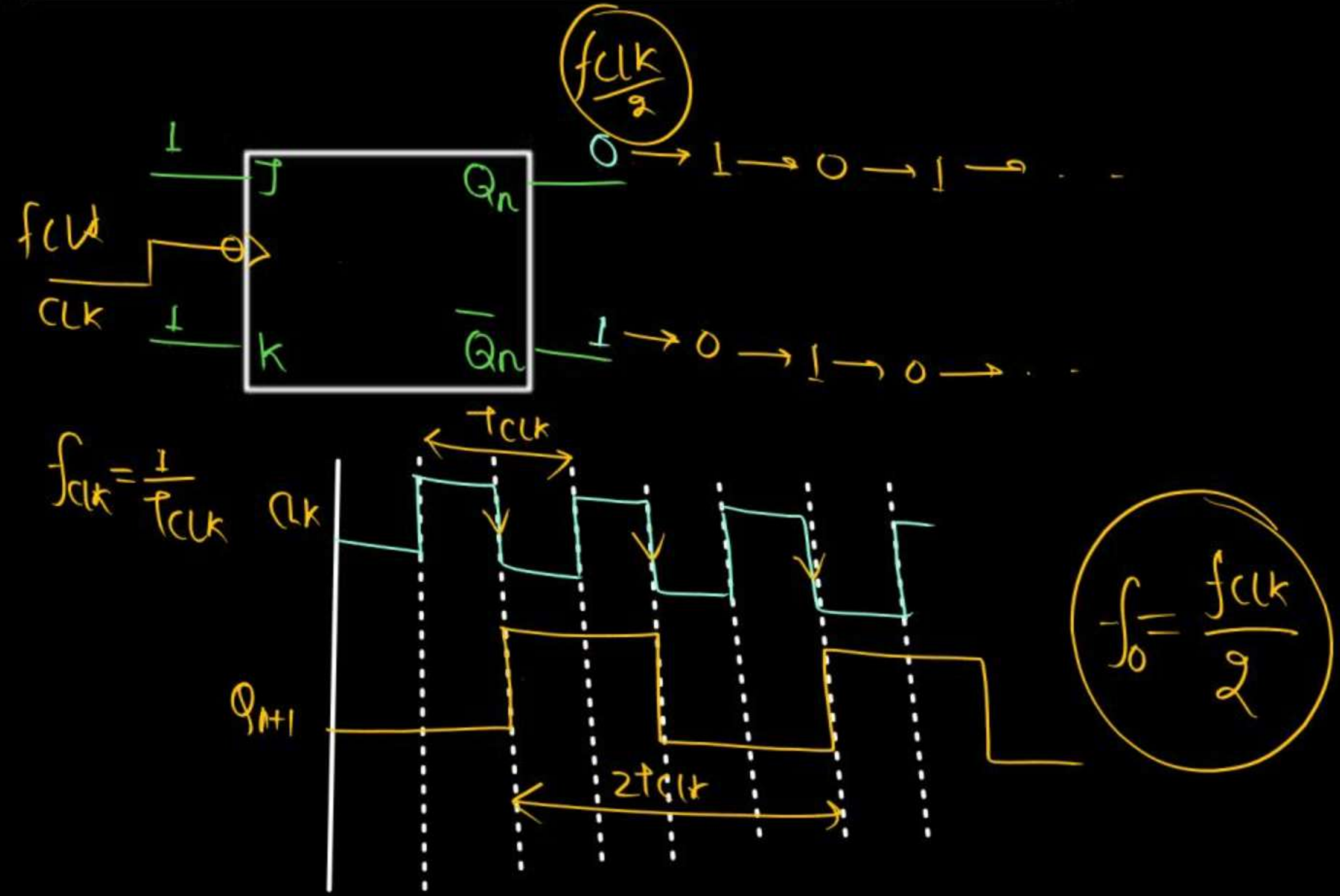
TOGGLE MODE OF THE FLIP FLOP



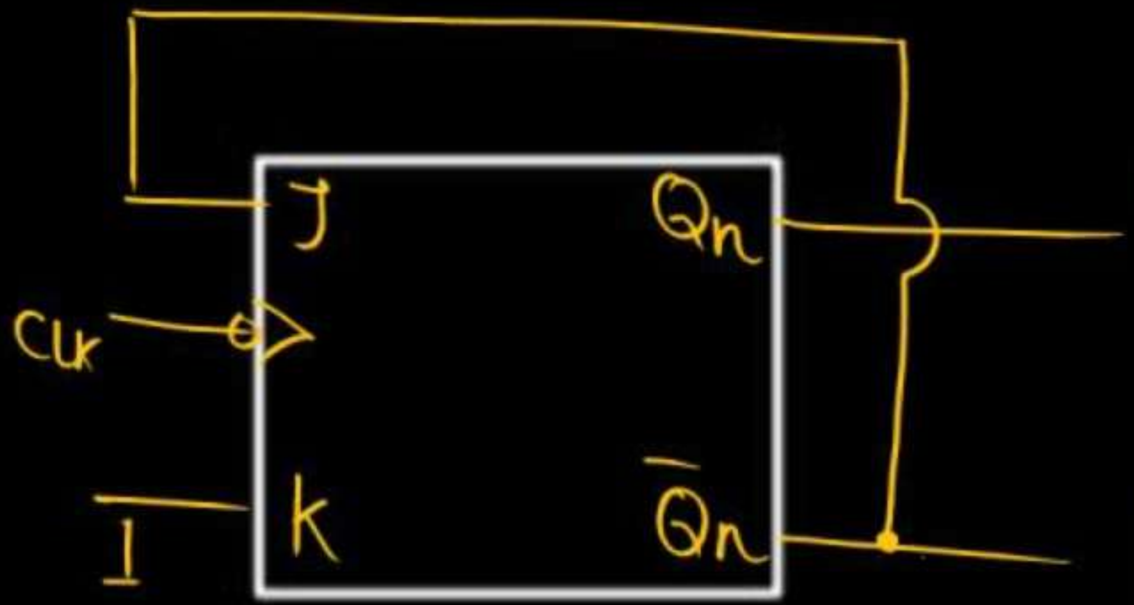
$f_{CLK} = \frac{1}{T_{CLK}}$ CLOCK

$f_0 = \frac{1}{2T_{CLK}} = \frac{f_{CLK}}{2}$

TOGGLE MODE OF THE FLIP FLOP

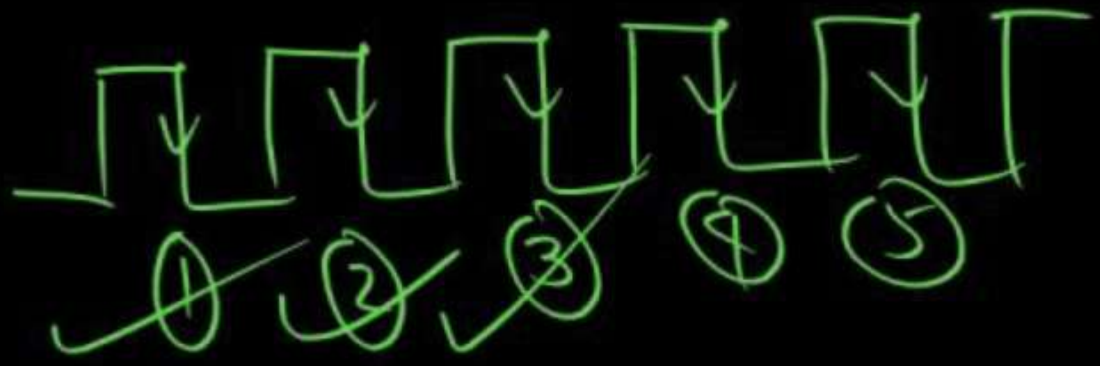


TOGGLE MODE OF THE FLIP FLOP

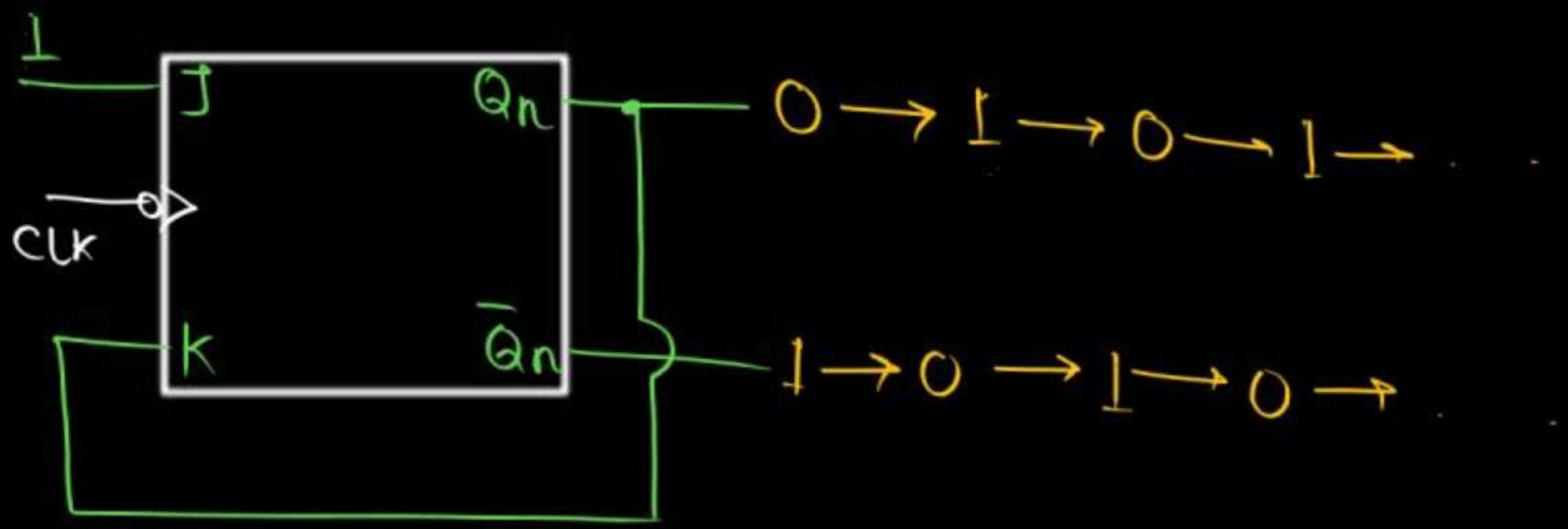


$0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow \ldots$

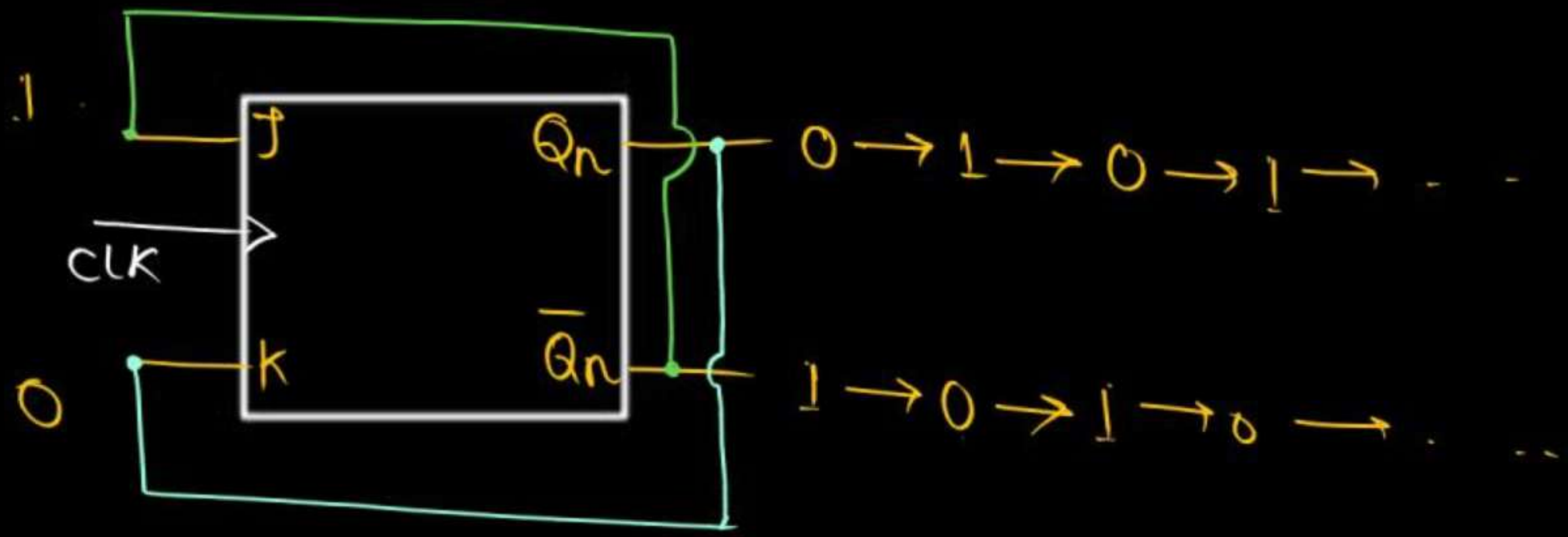
$1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow \ldots$



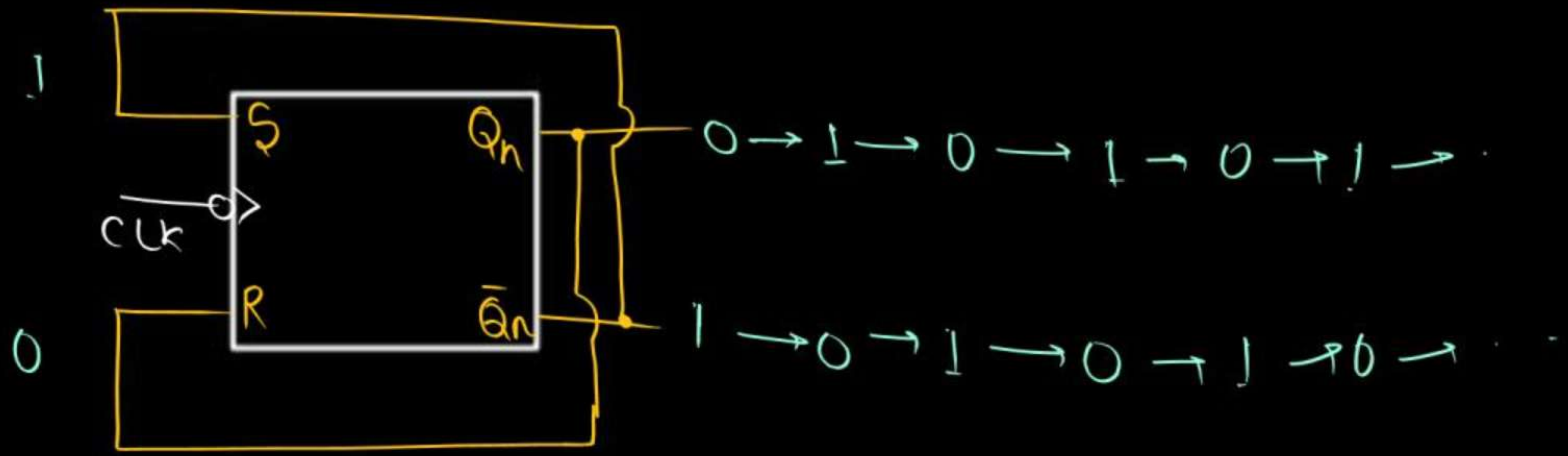
TOGGLE MODE OF THE FLIP FLOP



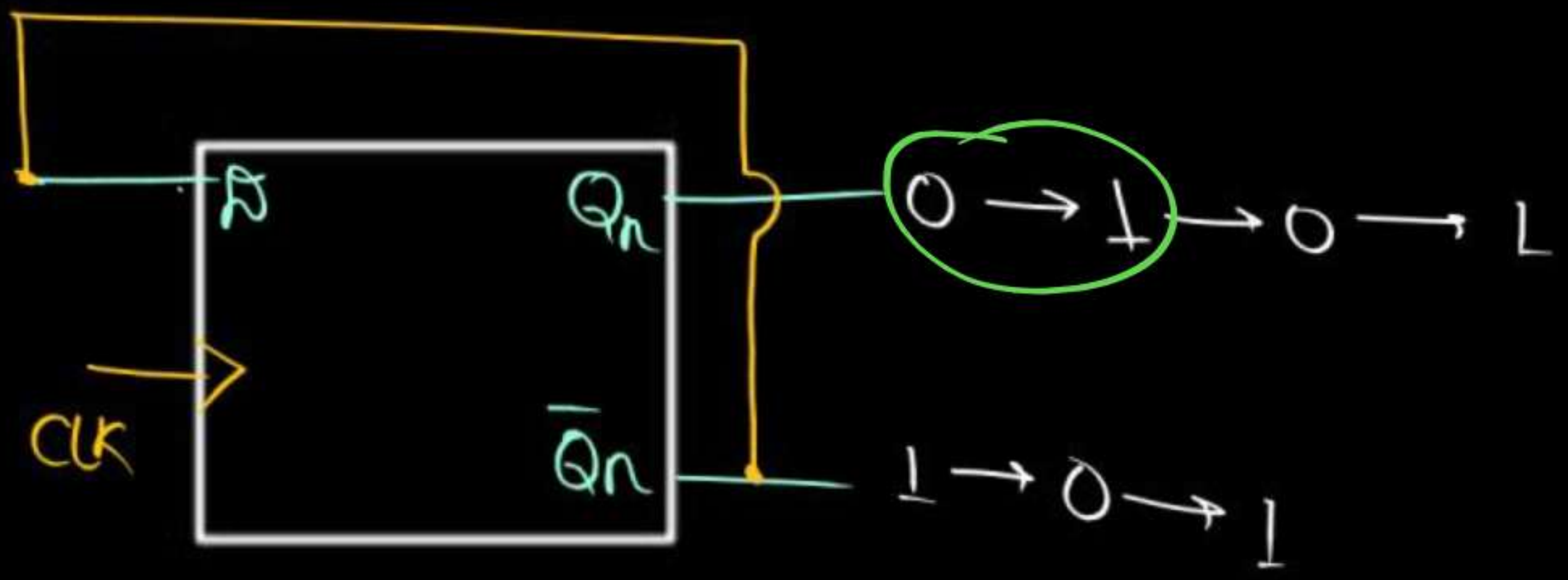
TOGGLE MODE OF THE FLIP FLOP



TOGGLE MODE OF THE FLIP FLOP



TOGGLE MODE OF THE FLIP FLOP



Counters

1. Counter are used to count number of clock.
2. Counters are also known as frequency divider circuit.

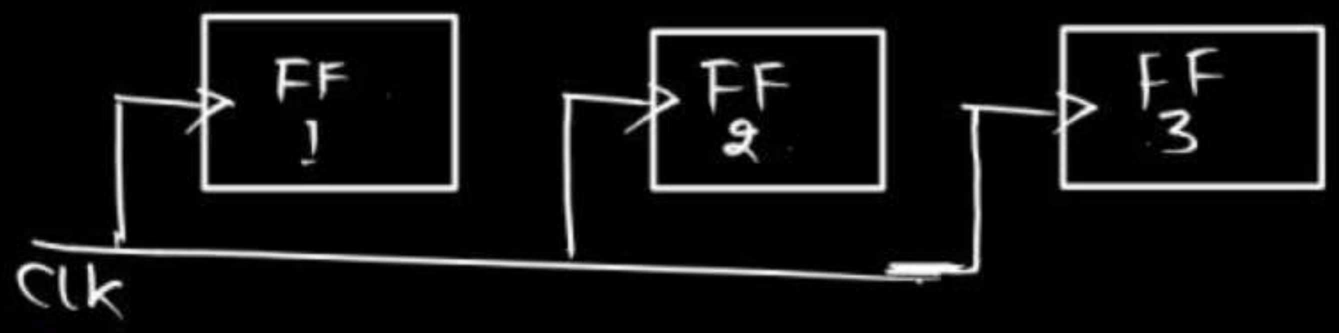
(1) Synchronous counter

(2) Asynchronous counter

UP	DOWN	RANDOM
1	5	1
2	4	3
3	3	2
4	2	5
5	1	4

Synchronous Counters

1. All the flip flops are connected with same clock.



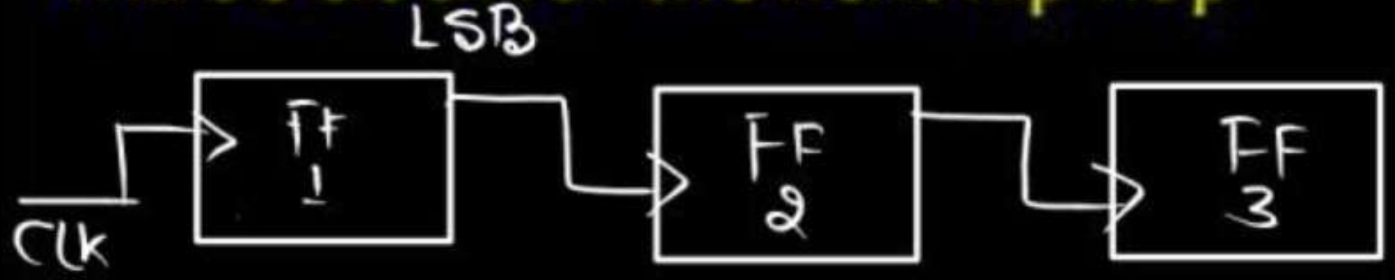
(2) fast

(3) All type of counting are possibble.

(4) Ex. Ring, Johnson counter

Asynchronous Counters

1. Only one Flip Flop having External clock and the outputs of that flip flop will be clock for the next flip flop



(2) slow

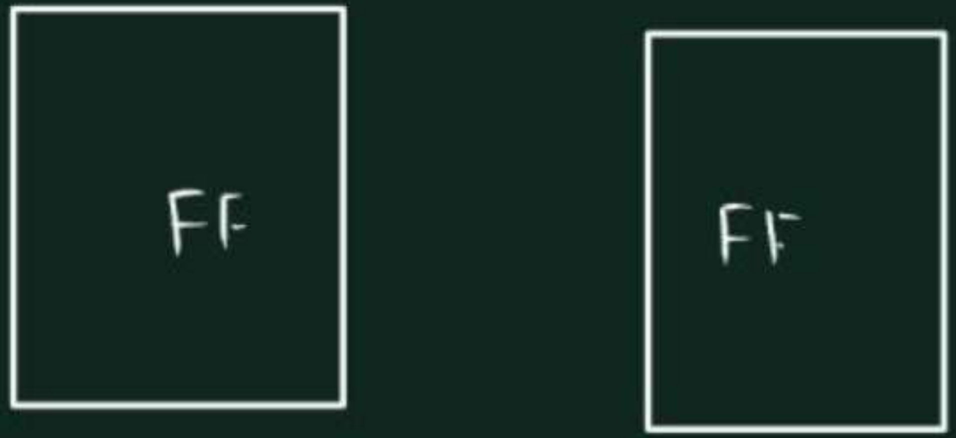
(3) Generally UP & DOWN counting are possible.

(4) Ex. Ripple counter

0, 1

$\downarrow$

2



$$\left\{\begin{matrix} 0 & 0 \\ 0 & 1 \\ 1 & 0 \\ 1 & 1 \end{matrix}\right\}$$

$$\boxed{\text{Maximum number of states} = 2^n}$$

$n \rightarrow$ Number of FF

MOD

Number of states used by the counter.

$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4$

MOD = 5

$7 \rightarrow 8 \rightarrow 9 \rightarrow 10 \rightarrow 11$

MOD = 5

$60 \rightarrow 61 \rightarrow 63 \rightarrow 65 \rightarrow 101$

MOD = 5

$$\boxed{MOD(M) \leq 2^n}$$

$$M \leq 2^n$$

$$\boxed{n \geq \log_2 M}$$

Q MOD-10 counter.

no. of FF ?

$$M \leq 2^n$$

$$n \geq \log_2 M$$

$$n \geq \log_2 10$$

$$n \geq 3.\text{something}$$

$$\boxed{n \approx 4}$$

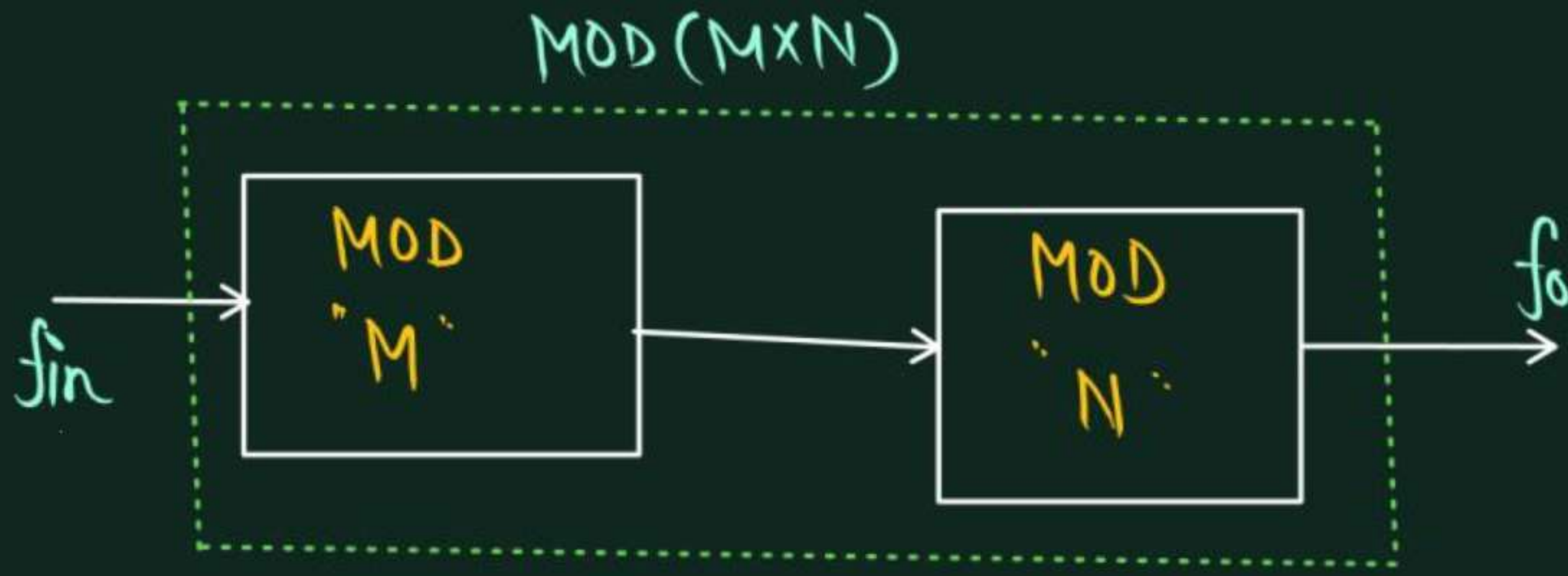
₹. 10

NOTE

1.

$$f_{out} = \frac{f_{in}}{M}$$

2.



$$f_{out} = \frac{f_{in}}{M \times N}$$

BCD

└→ Binary coded decimal

└→ Every decimal number are represented by 4 bit

0 →	0000
1 →	0001
2 →	0010
3 →	0011
4 →	0100
5 →	0101
6 →	0110
7 →	0111
8 →	1000
9 →	1001

BCD

BCD

100
101
102
103
104
105
105
107
106
109

MOD-10

Q When MOD'5' counter is cascaded by MOD'2' counter Then it will become.

(A) MOD-10 counter

(B) BCD counter

~~(C)~~ Both (A) & B

(D) MOD'7' counter

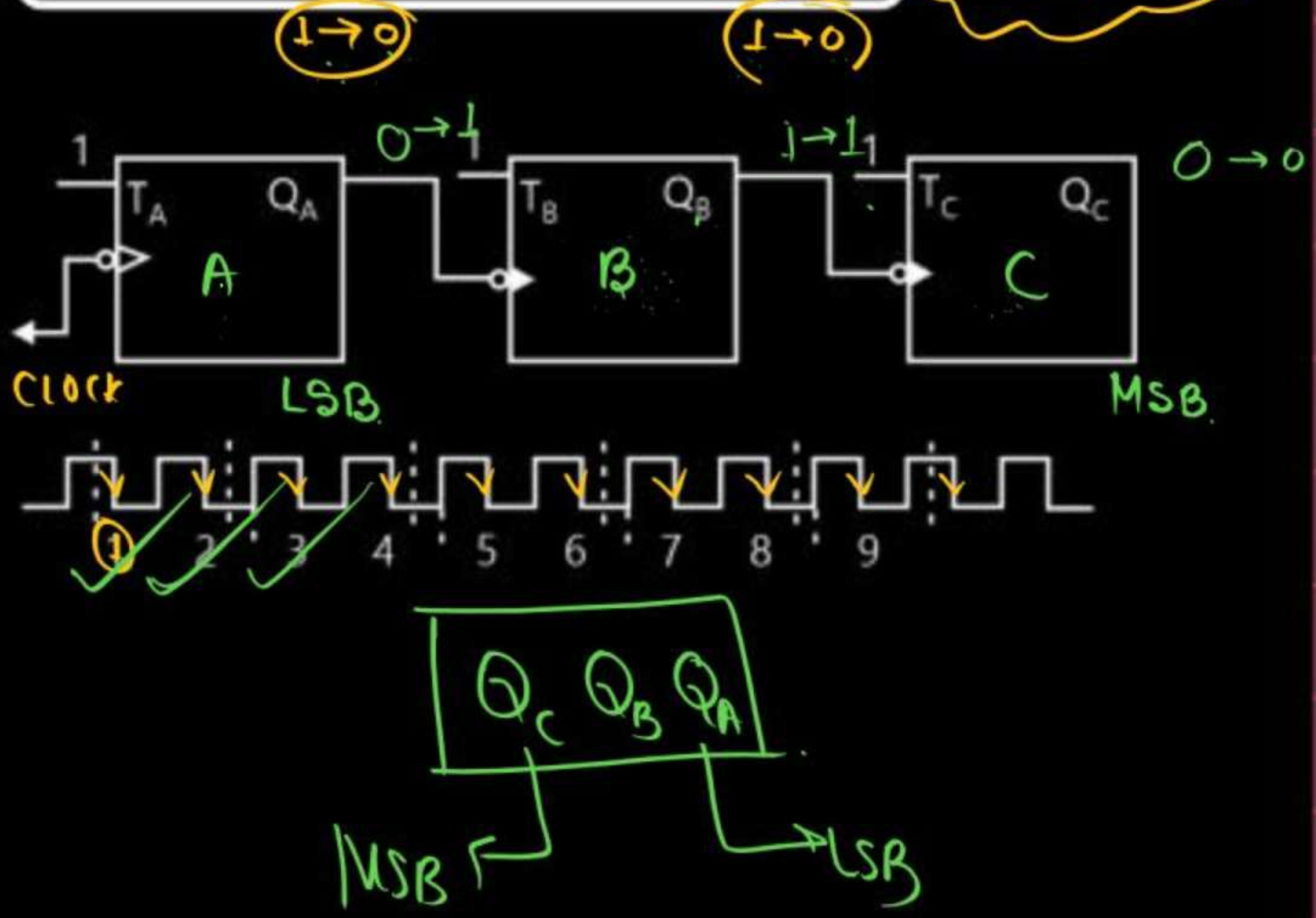
(E) Sir, Mujhe ata to hai par mai batunga nahi.

$5 \times 2 = 10$

MOD

Asynchronous Counter

3 bit Ripple counter



Ext clk

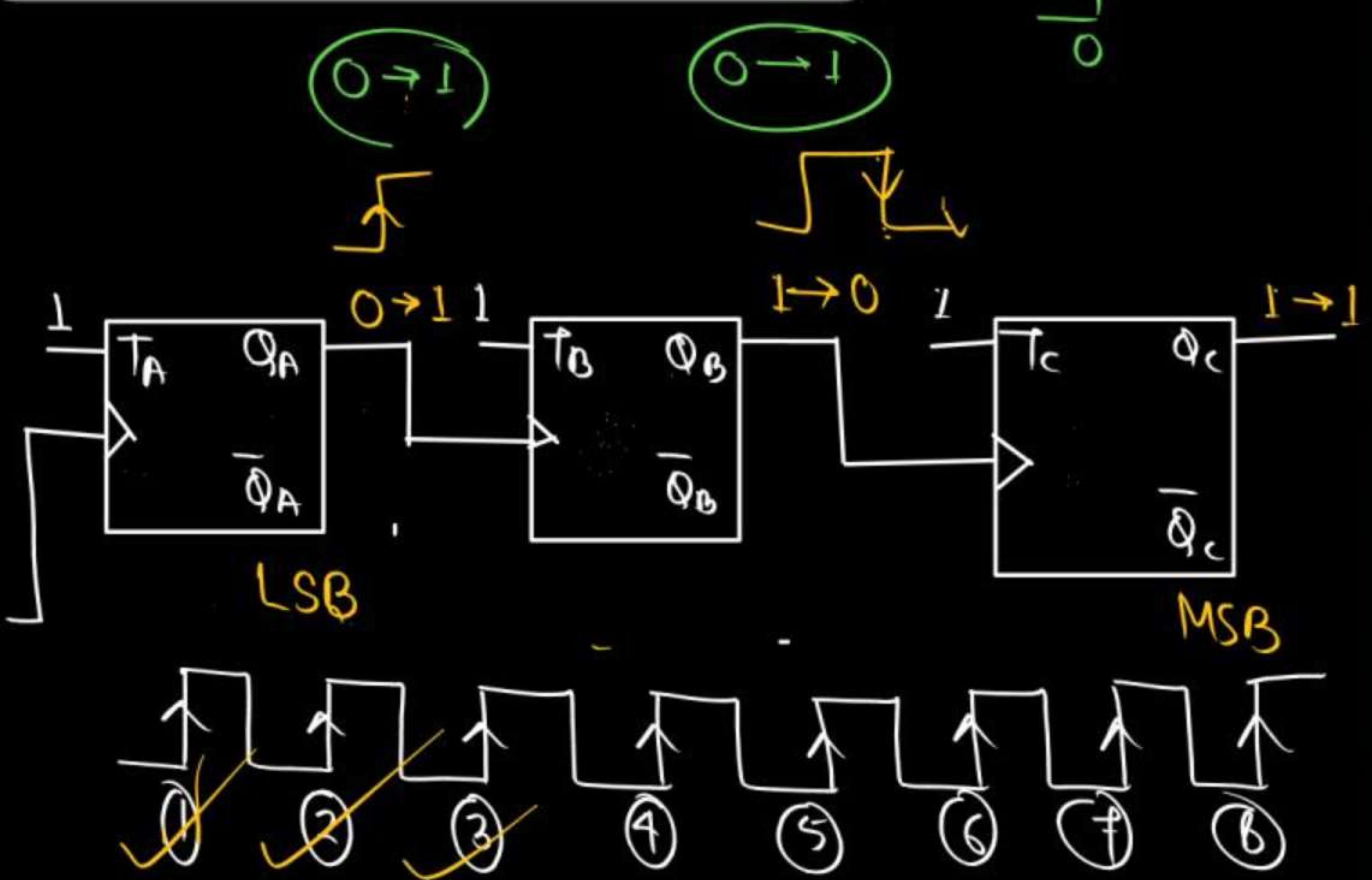
clock	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7$

$000 \rightarrow 001 \rightarrow 010 \rightarrow 011 \rightarrow 100 \rightarrow 101 \rightarrow 110 \rightarrow 111$

MOD "8" UP RIPPLE COUNTER

Asynchronous Counter



clock	Q_C	Q_B	Q_A
0	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0

$000 \rightarrow 111 \rightarrow 110 \rightarrow 101 \rightarrow 100 \rightarrow 011 \rightarrow 010 \rightarrow 001 \rightarrow 000$

MOD-8 DOWN RIPPLE COUNTER

Asynchronous Counter

Bubble

$\left\{\begin{array}{l} Q \longrightarrow -ve \\ \overline{Q} \longrightarrow -ve \end{array}\right.$

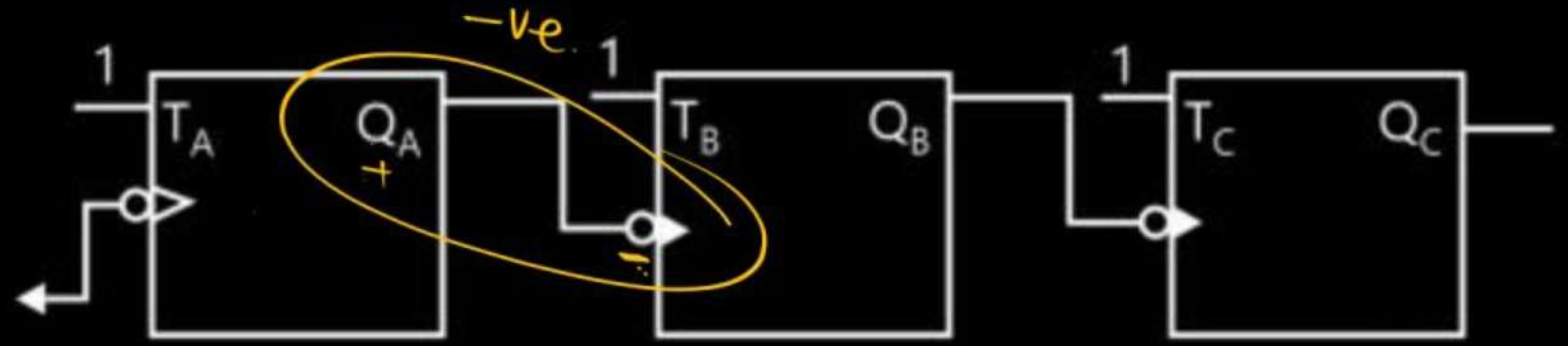
$-ve \rightarrow$ UP
$+ve \rightarrow$ DOWN

clock	Q_c	Q_B	Q_c
0			
1			
2			
3			
4			
5			
6			
7			
8			

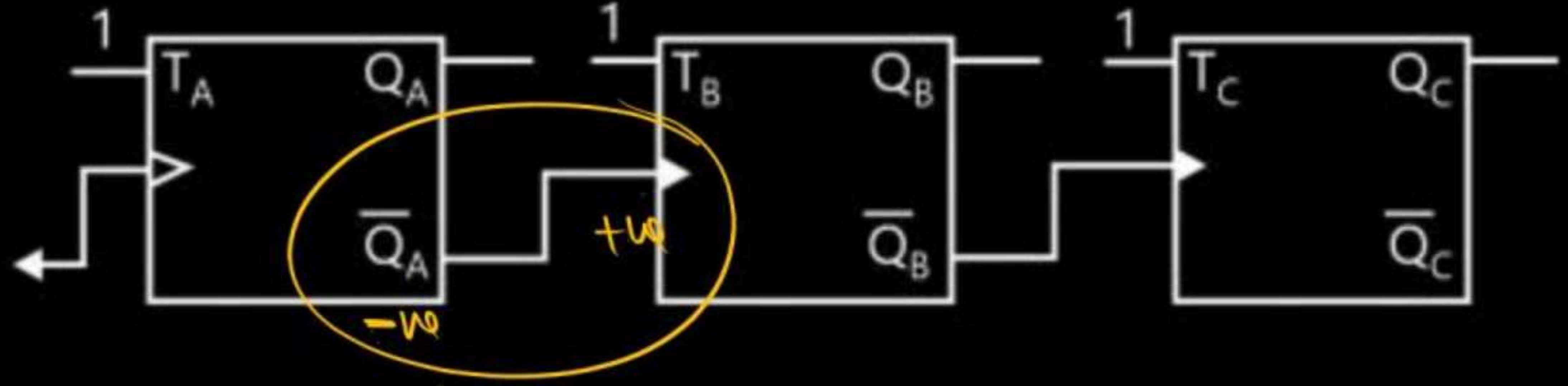
Asynchronous Counter

−ve → UP

+ve → DOWN



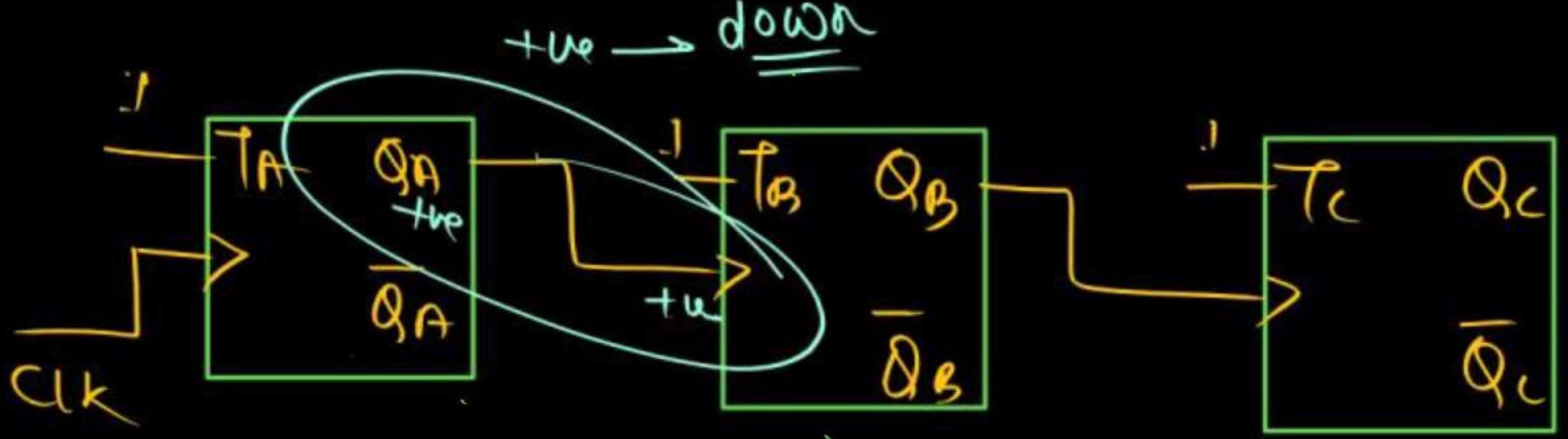
UP



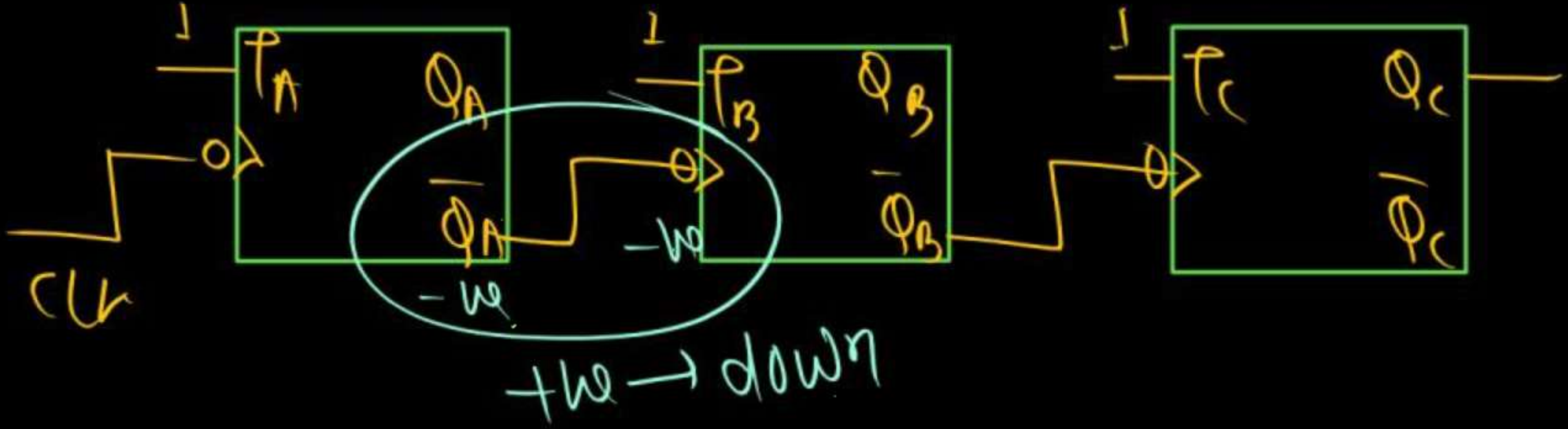
−ve

Asynchronous Counter

$n \rightarrow 2^n$



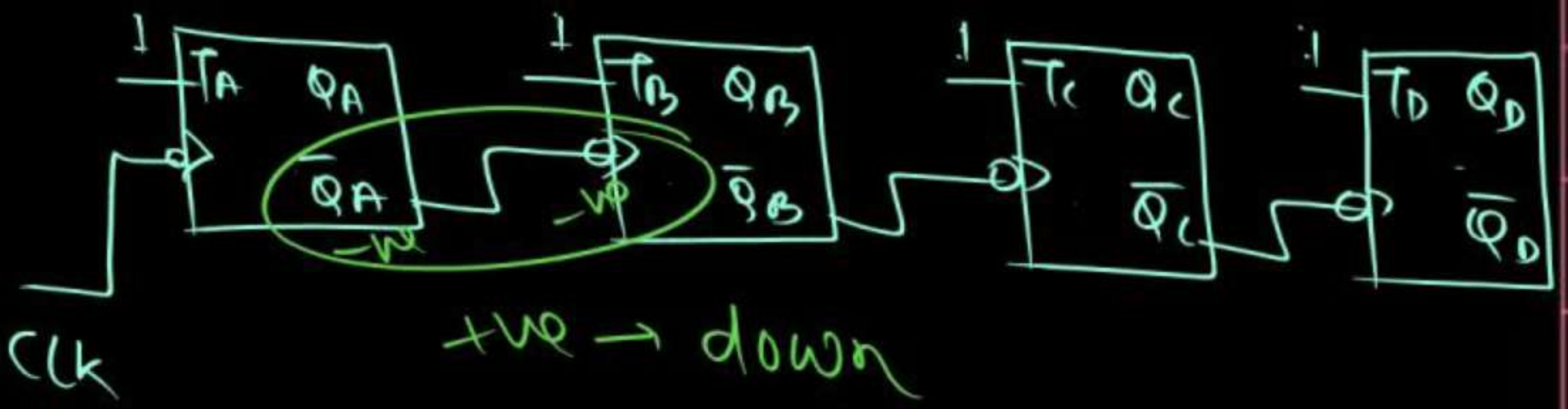
DOWN



Down counter

Asynchronous Counter

$MOD = 2^4 = 16$



MOD 16 down Ripple counter

clock	Q_C	Q_B	Q_C	Clr
0				
1				
2				
3				
4				
5				
6				
7				
8				

Asynchronous Counter

LDC

#11PM

1000 → 500

200

100

50

20

10

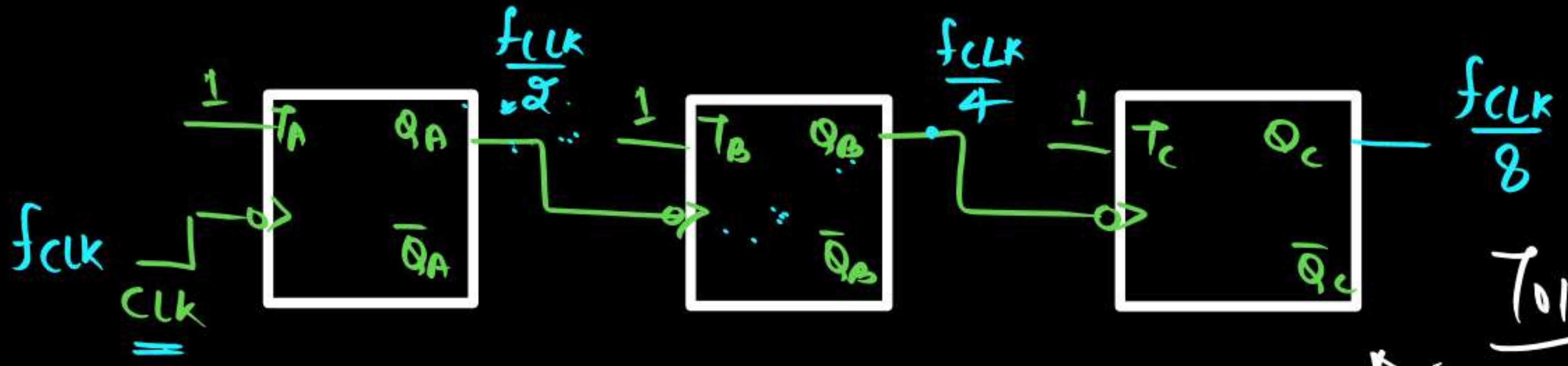
5

2

1

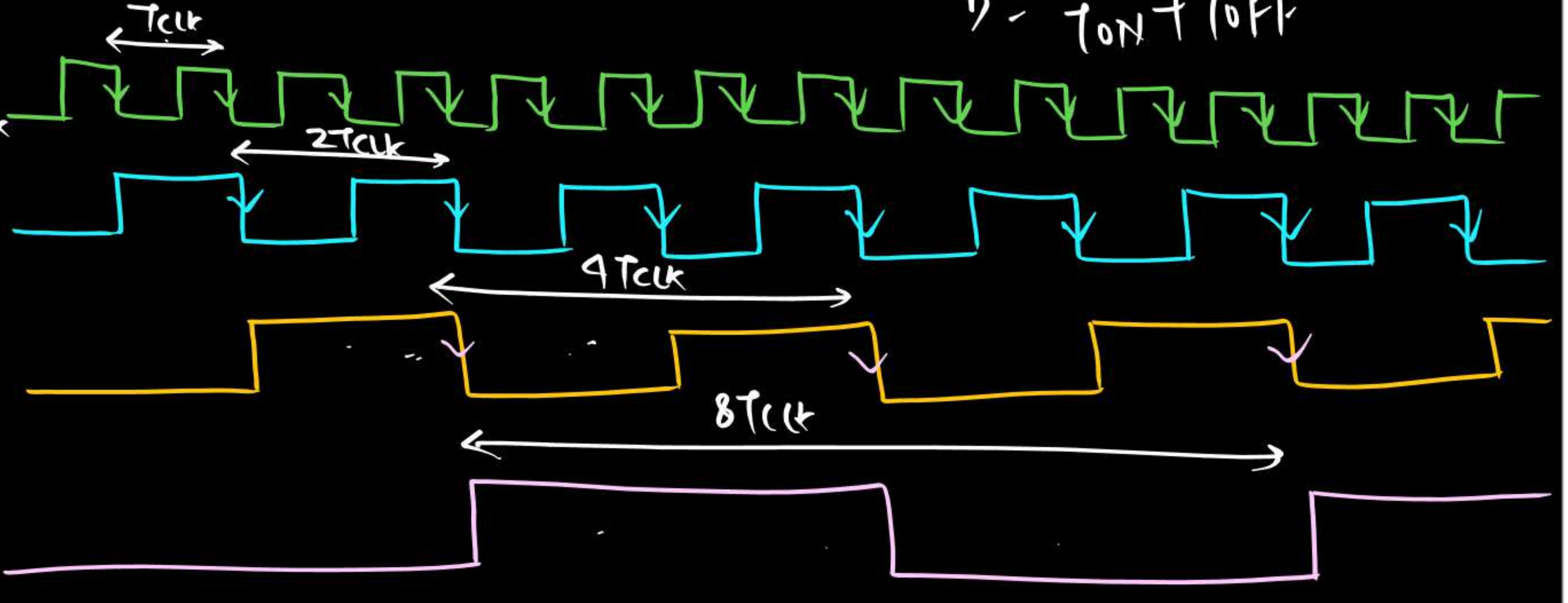
0

clock	Q_C	Q_B	Q_C	Clr
0				
1				
2				
3				
4				
5				
6				
7				
8				



$$D = \frac{T_{ON}}{T_{ON}+T_{OFF}}$$

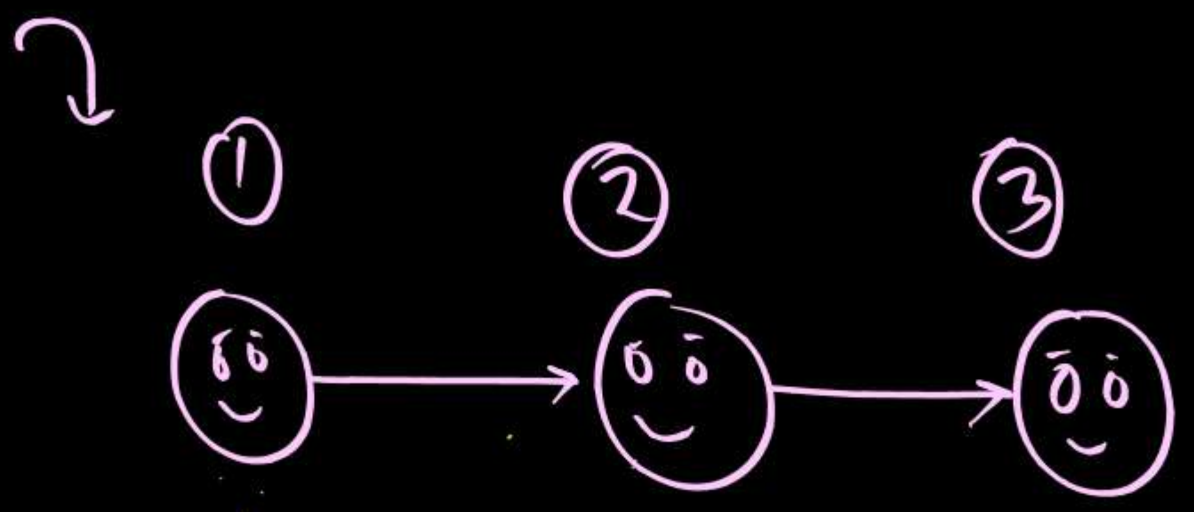
$f_{clk} = \frac{1}{T_{clk}}$



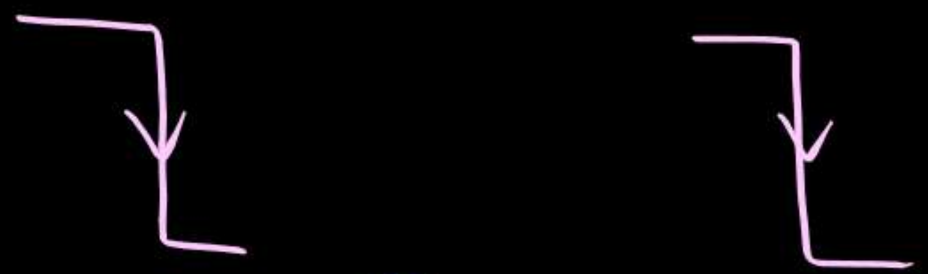
$$f_{Q_A} = \frac{1}{2T_{clk}} = \frac{f_{clk}}{2} \quad Q_A$$

$$f_{Q_B} = \frac{1}{4T_{clk}} = \frac{f_{clk}}{4} \quad Q_B$$

$$f_{Q_C} = \frac{1}{8T_{clk}} = \frac{f_{clk}}{8} \quad Q_C$$



10min 10min 10 min

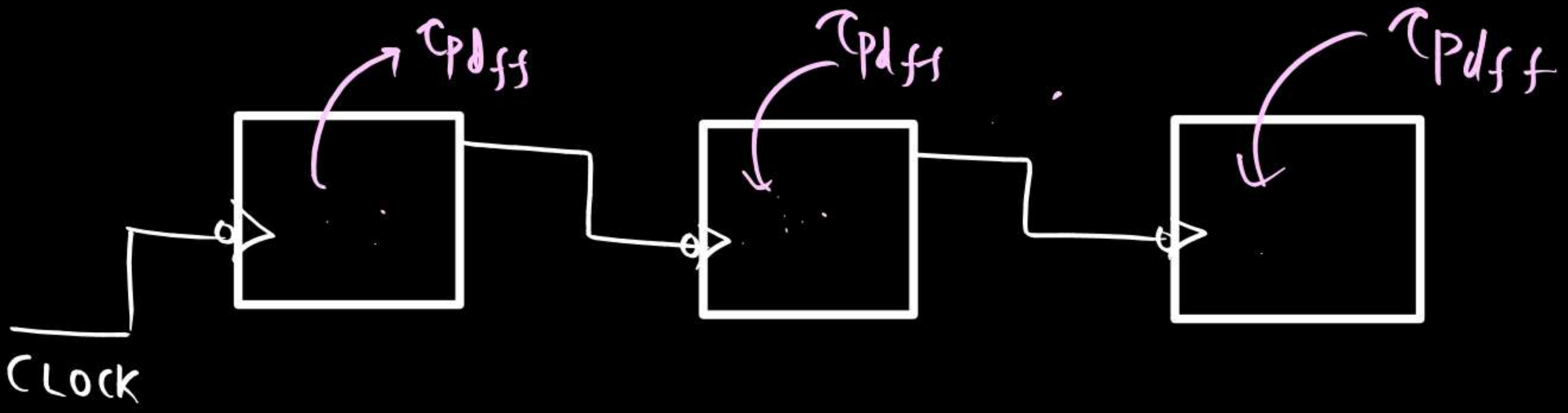


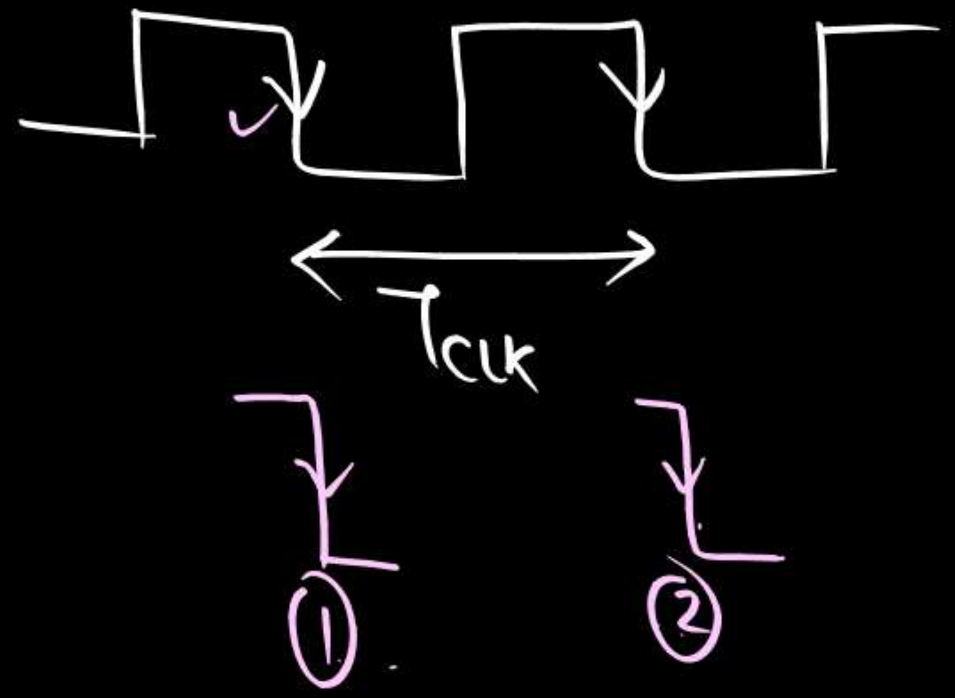
T_{clk}

30 min

3×10 min

$n \times T_{pd}$





$$\boxed{T_{clk} \geq 3\tau_{pdff}}$$

"n" FF

$$\boxed{T_{clk} \geq n \cdot \tau_{pd_{ff}}}$$

$$\frac{1}{T_{clk}} \leq \frac{1}{n \cdot \tau_{pd_{ff}}}$$

$$\boxed{f_{clk} \leq \frac{1}{n \cdot \tau_{pd_{ff}}}}$$

$$\boxed{(f_{clk})_{max} = \frac{1}{n \cdot \tau_{pd_{ff}}}}$$

$T_{clk} \geq$ Sum of Delay of all the FF

(Asynchronous)

Q In BCD counter. Delay of FF is 10ns.

all FF are identical.

Find the clock frequency for stable operation?

$$f_{CLK} \leq \frac{1}{n \cdot \tau_{pd_{FF}}}$$

$$\leq \frac{1}{4 \times 10 \times 10^{-9}} \text{ Hz}$$

$$\leq \frac{10^9}{4 \times 10} \text{ Hz}$$

$$\leq \frac{\cancel{1000}^{25} \times 10^6}{\cancel{4}} \text{ Hz}$$

$(f_{CLK})_{max} = 25 \text{ MHz}$

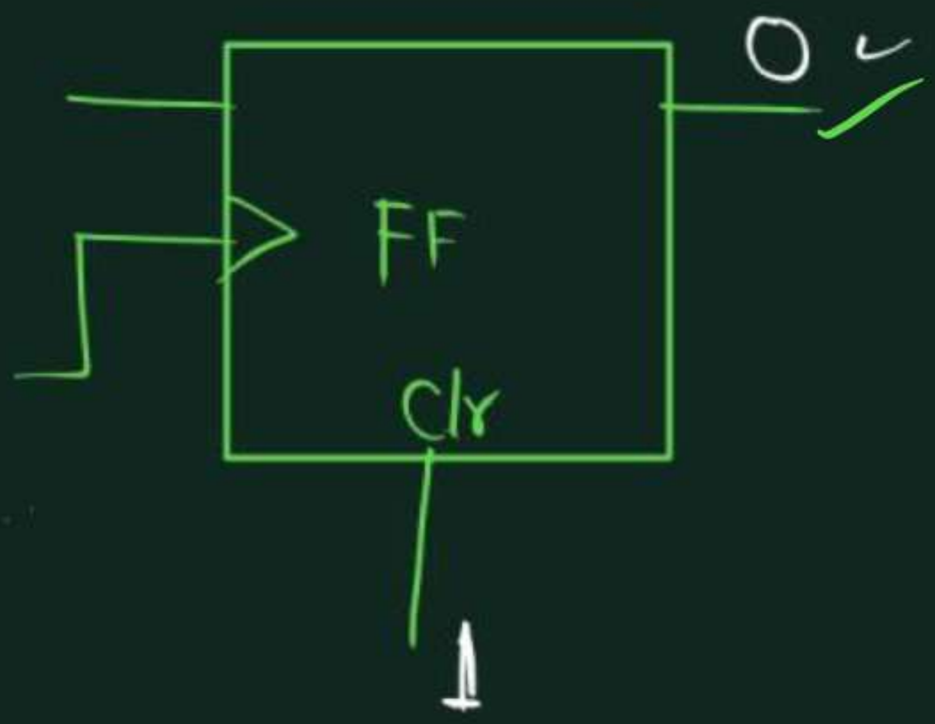
MOD = 10

$M \leq 2^n$

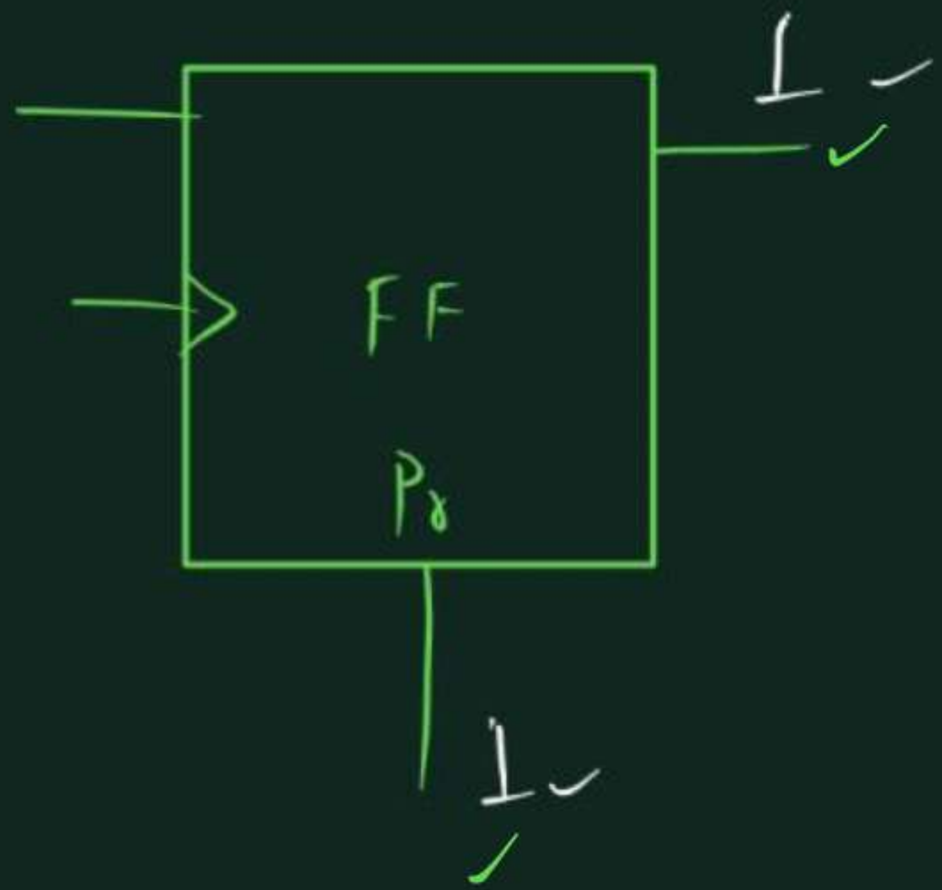
$n \geq \log_2 M$

$n \geq 4$

Reset (clr)



Preset

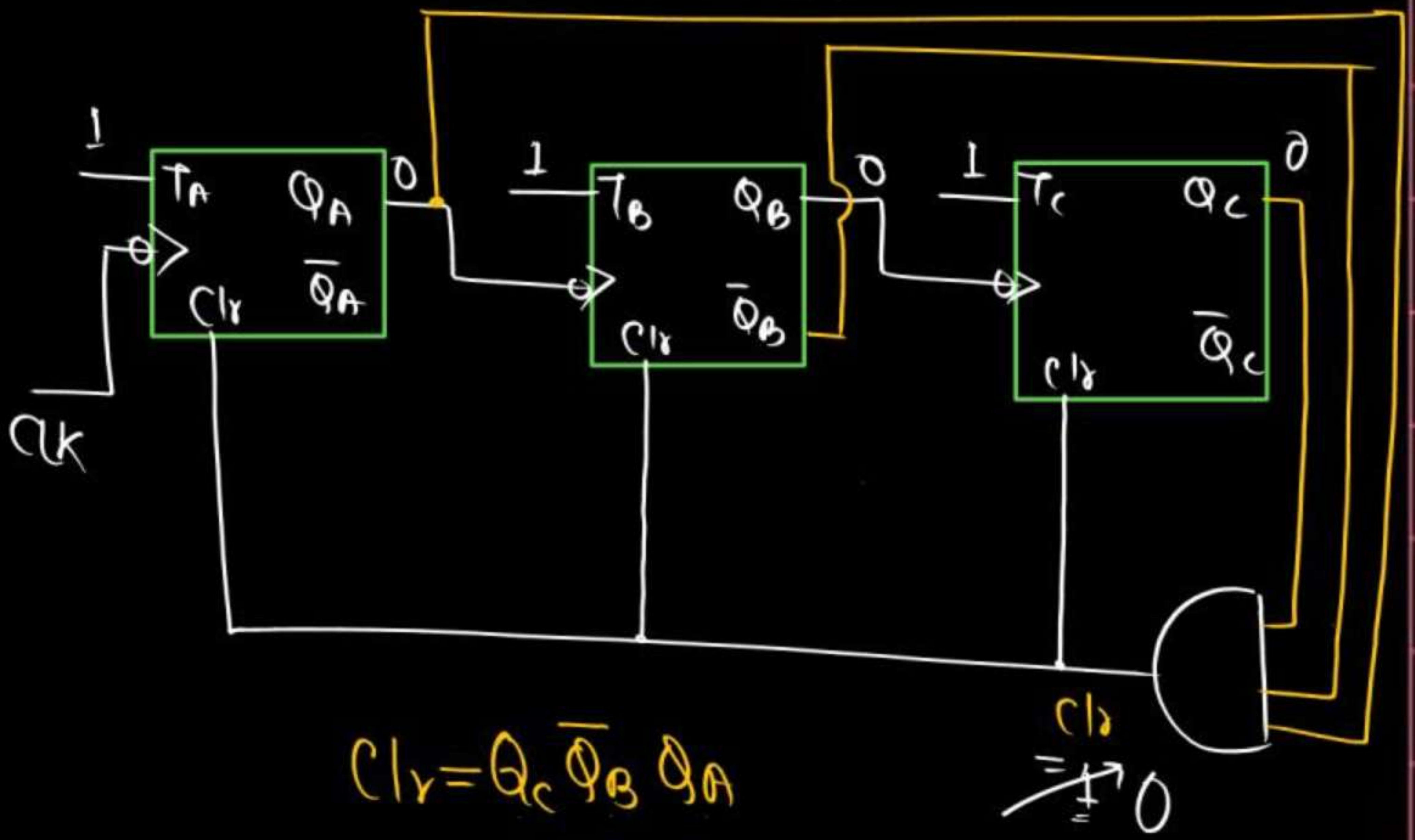


Asynchronous Counter

UP $Clr = Q_C \bar{Q}_B Q_A$

1 0 1 → 5 MOD

MOD-5 UP COUNTER



$$Clr = Q_C \bar{Q}_B Q_A$$

1 0 1

clock	Q_C	Q_B	Q_A	$Clr = Q_C \bar{Q}_B Q_A$
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	$\cancel{1} \to 0$	$\cancel{0} \to 0$	$\cancel{1} \to 0$	$\cancel{1} \to 0$
6	0	0	1	0
7	0	1	0	0
8	0	1	1	0

$000 \to 001 \to 010 \to 011 \to 100$

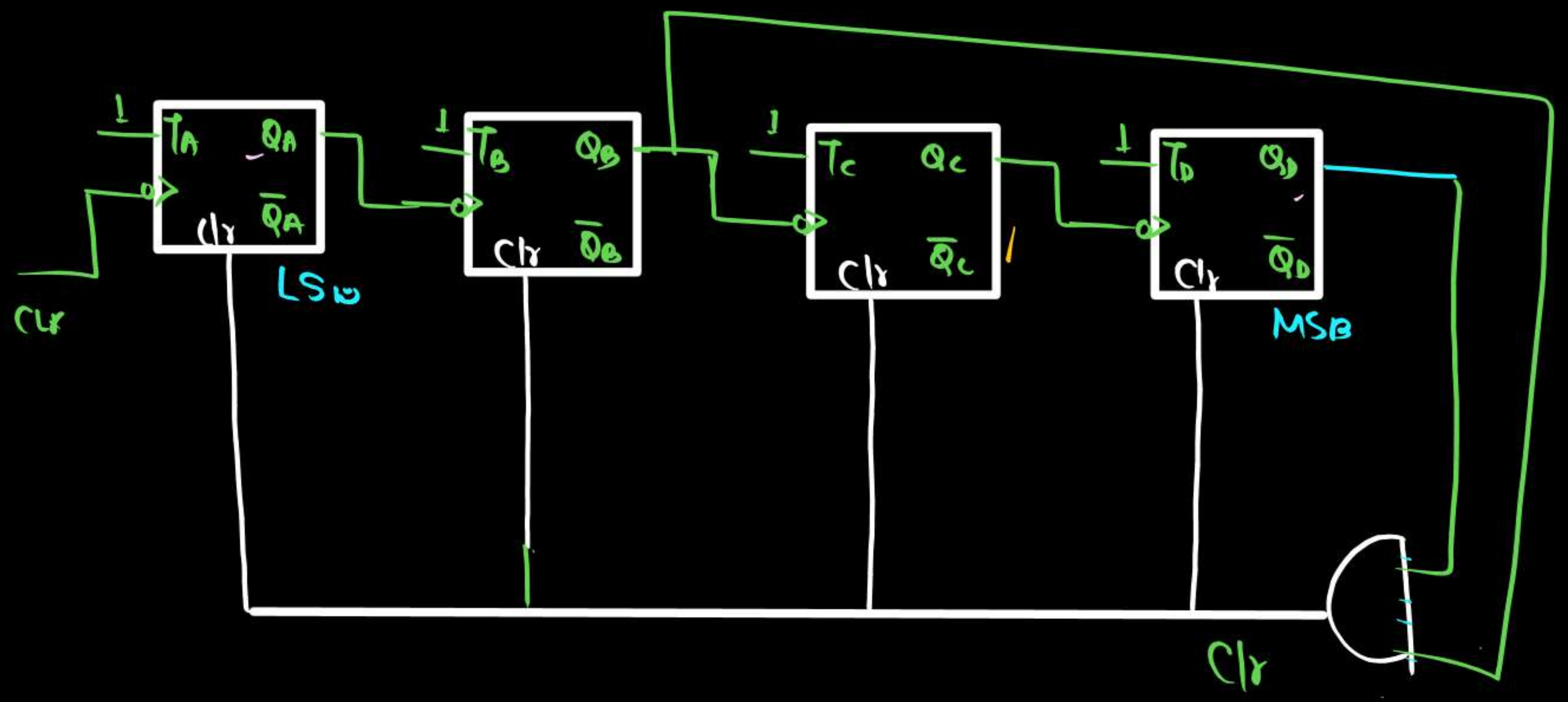
MOD = 5

जीत की ख़ातिर बस जूनून चाहिए,
जिसमें उबाल हो ऐसा खून चाहिए,
ये आसमान भी आ जाएगा ज़मीन पर,
बस इरादों में जीत की गूँज चाहिए।

Asynchronous Counter

clock	Q_C	Q_B	Q_C	Clr
0				
1				
2				
3				
4				
5				
6				
7				
8				

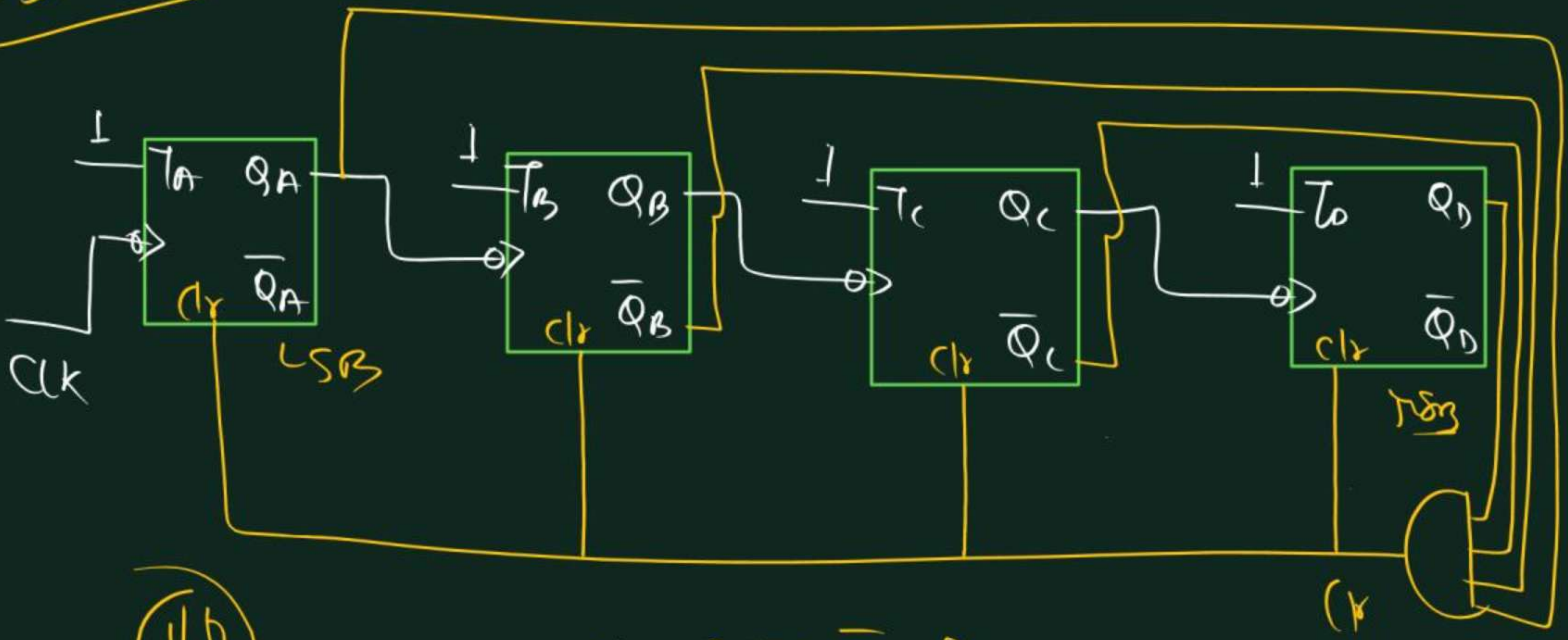
BCD Ripple counter:



$$Clr = Q_D \bar{Q}_C Q_B \bar{Q}_A$$

$1010 \rightarrow 10 \rightarrow$ MOD

SHANDAR



UP

$Clr = Q_D \overline{Q}_C \overline{Q}_B Q_A$

1 0 0 1 → 9

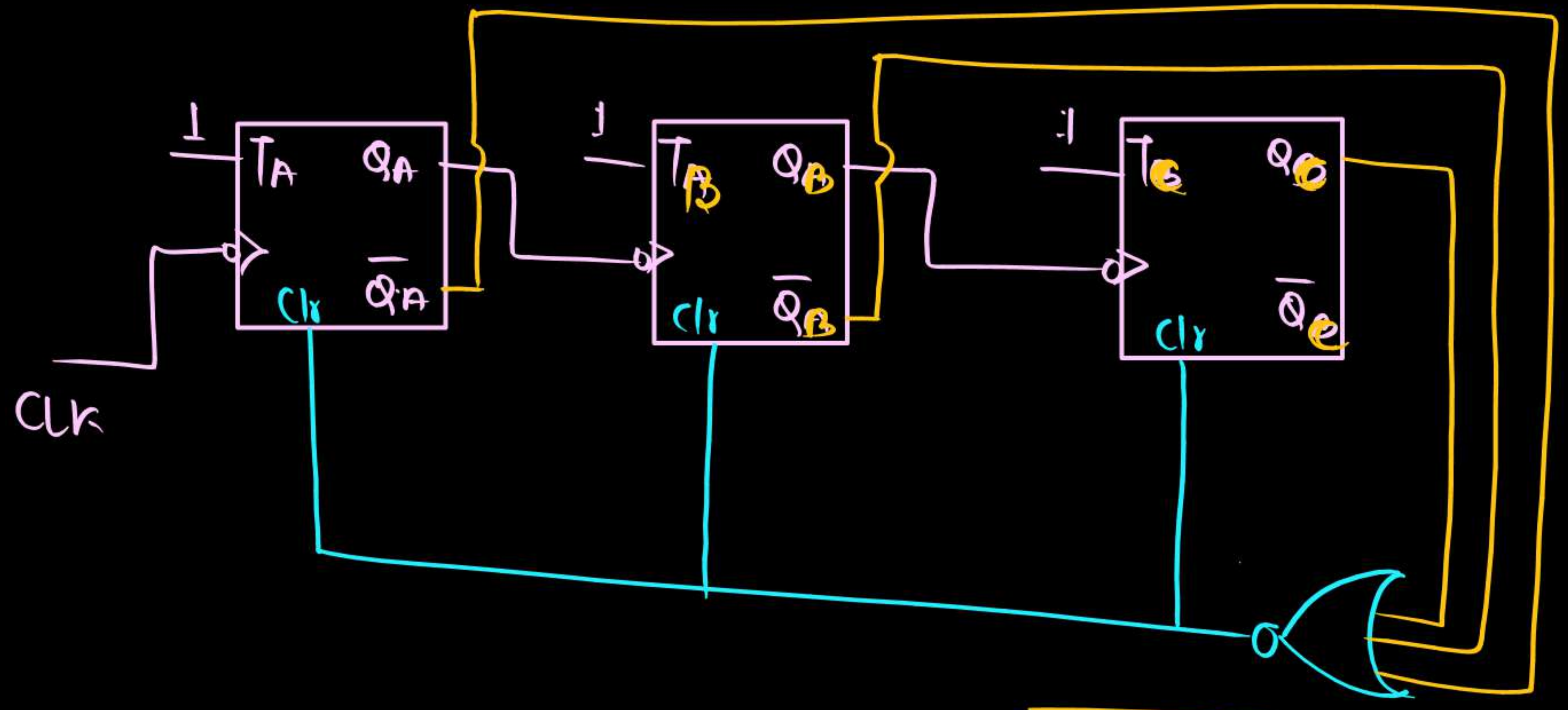
MOD-9 UP Ripple counter

Asynchronous Counter

$Q_D\, Q_C\, Q_B\, Q_A$

Q. Design a BCD counter

Clr =



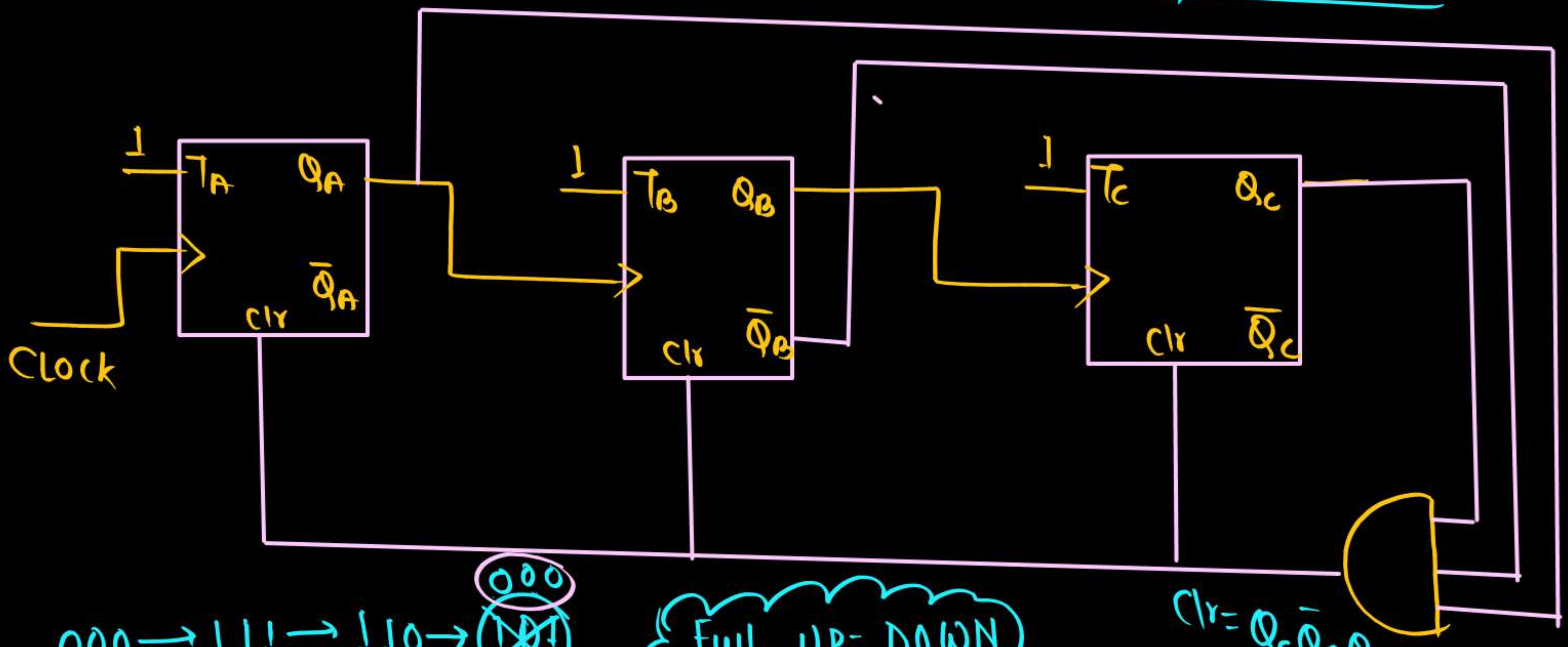
$$Clr = \overline{Q_C + \overline{Q_B} + \overline{Q_A}}$$

$$Clr = \overline{Q_C} \cdot Q_B \cdot Q_A$$

$0 \quad 1 \quad 1 \rightarrow$ MOD-3

Asynchronous Counter

Mod. 3 Down Ripple counter.



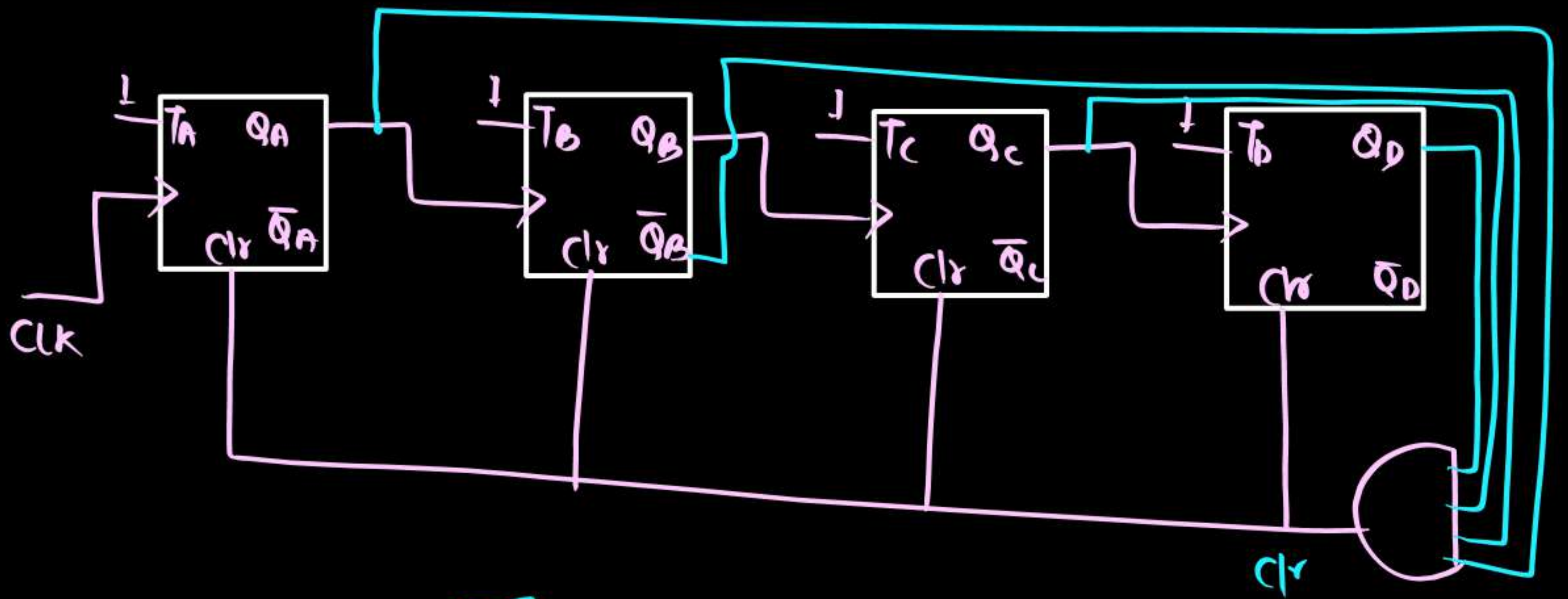
000 → 111 → 110 → ~~101~~ 000

Full-UP = DOWN

8 − 5 = 3

$Clr = Q_C \bar{Q}_B Q_A$

101 → 5



$Clr = Q_D Q_C \bar{Q}_B Q_A$

1 1 0 1

$= 13$

Full $\rightarrow$ 16

UP $\rightarrow$ 13

DOWN = Full − UP

= 16 − 13

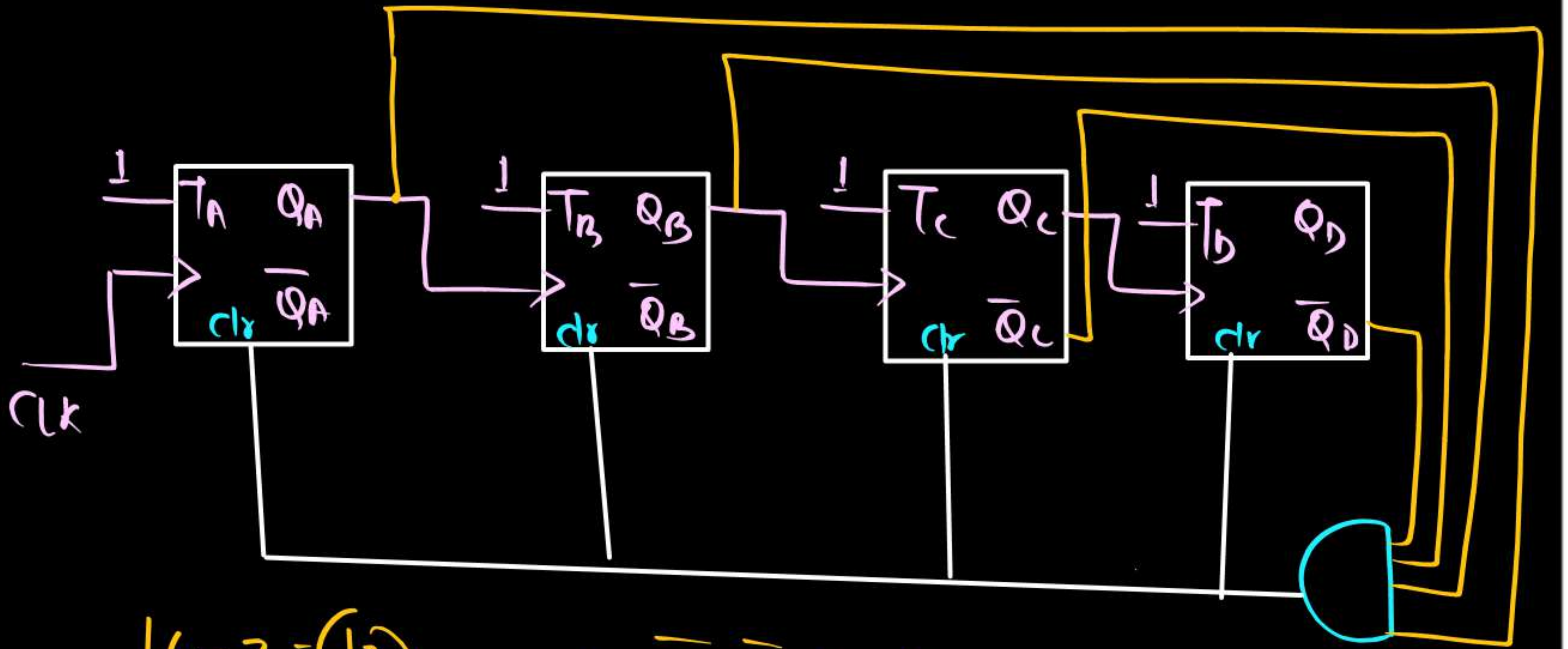
= 3

Q Design MOD-13 Down Ripple counter by using 4 FF ?

FULL − UP = DOWN

UP = FULL − DOWN

$= 16 - 13 = 3$



$3 = 0011$

$Clr = \bar{Q}_D \bar{Q}_C Q_B Q_A$

$16 - 3 = 13$

down

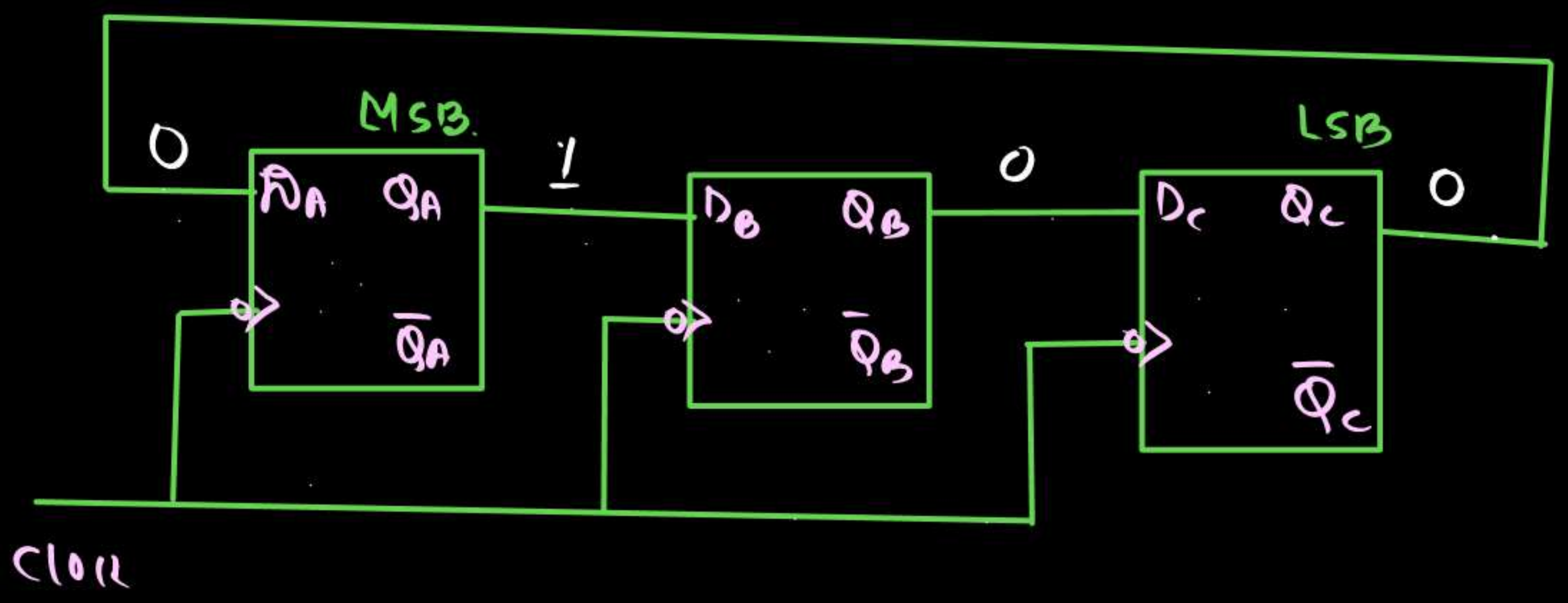
$Clr = \bar{Q}_D \bar{Q}_C Q_B Q_A$

$0011 \rightarrow UP = 3$

Synchronous counter

1. Ring counter
2. Johnson counter

RING COUNTER :→



Clock	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	0	1	0
3	0	0	1
4	1	0	0

100
010
001

MOD = 3

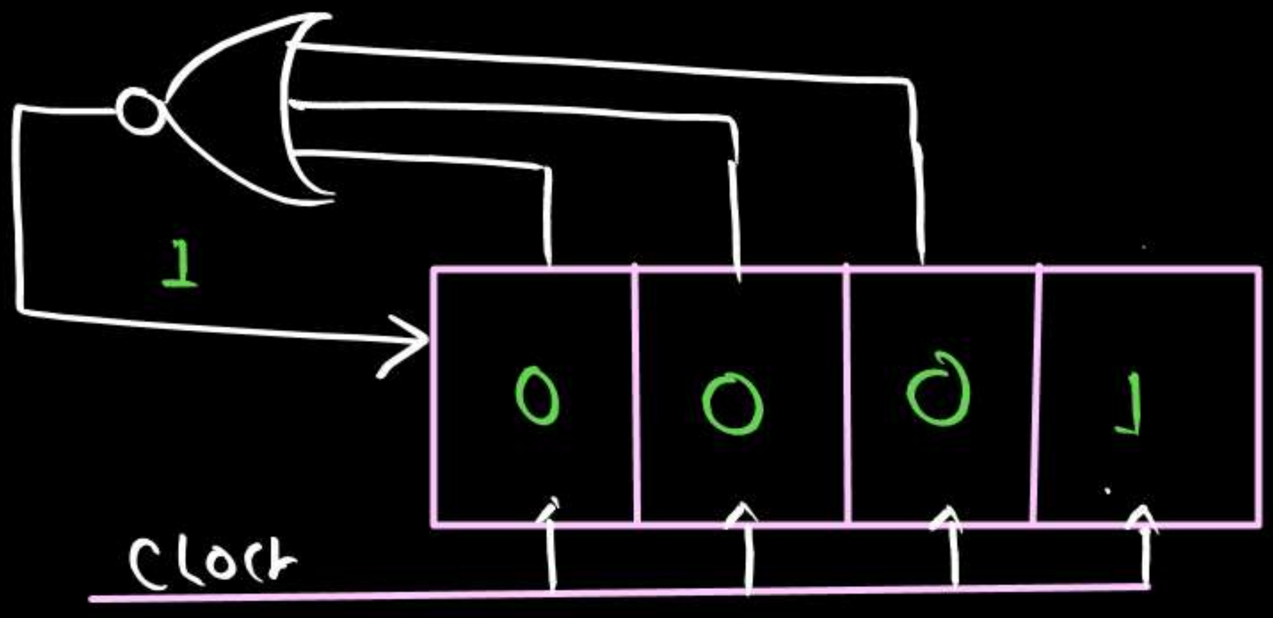
$$\left\{\begin{matrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{matrix}\right\} \text{MOD } 4$$

N bit Ring counter

$\boxed{MOD = N.}$

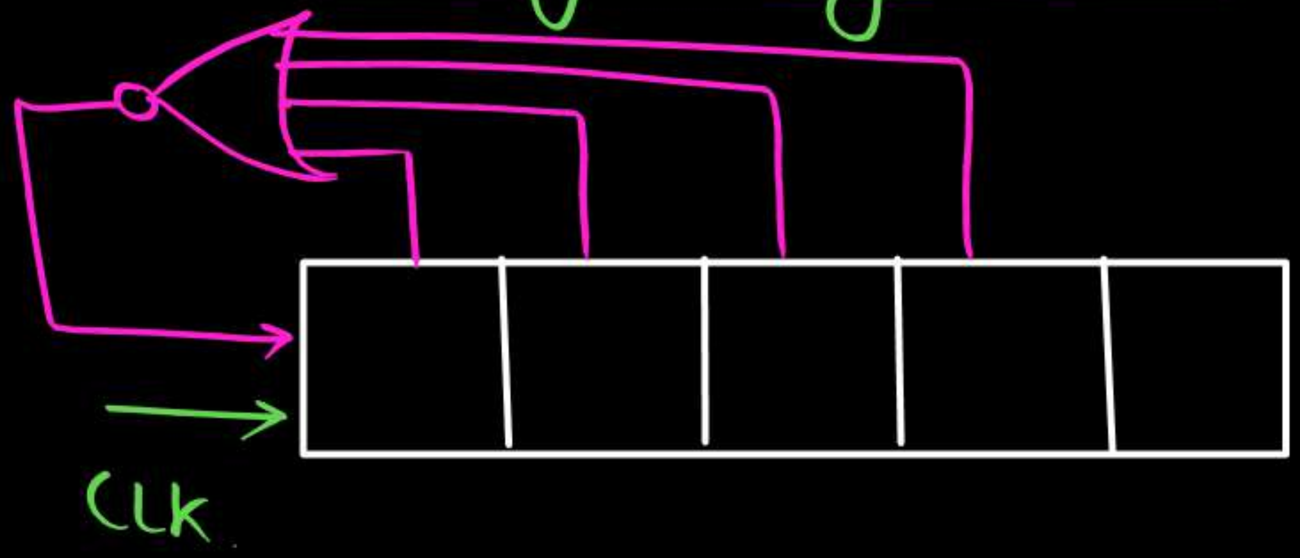
$0000 \to 1000 \to 0100 \to 0010 \to 0001$

Symbolic Representation:



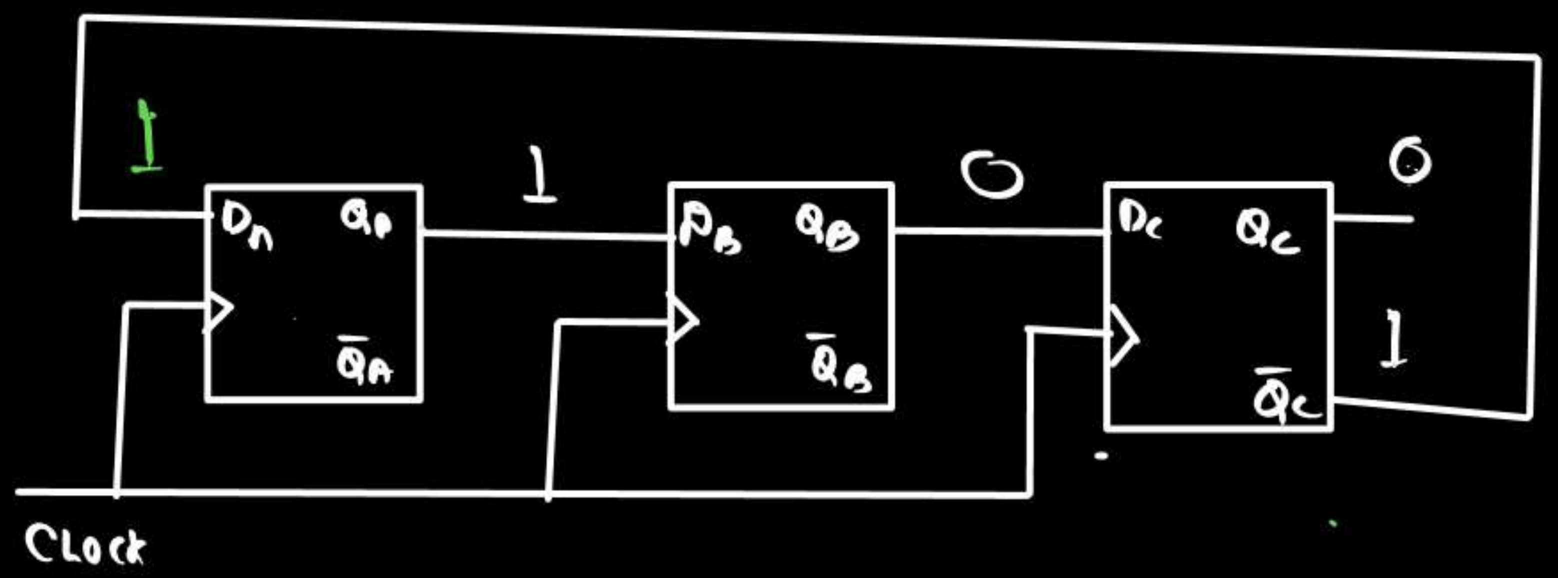
CLOCK	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0

Self starting Ring counter.



Johnson counter

- → Twisted Ring counter
- → Creeping counter
- → Mobies counter
- → Walking counter



Clock	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1
6	0	0	0
7	1	0	0

$$\left\{\begin{matrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 1 & 1 & 0 \\ 1 & 1 & 1 \\ 0 & 1 & 1 \\ 0 & 0 & 1 \end{matrix}\right\} \text{MOD 6}$$

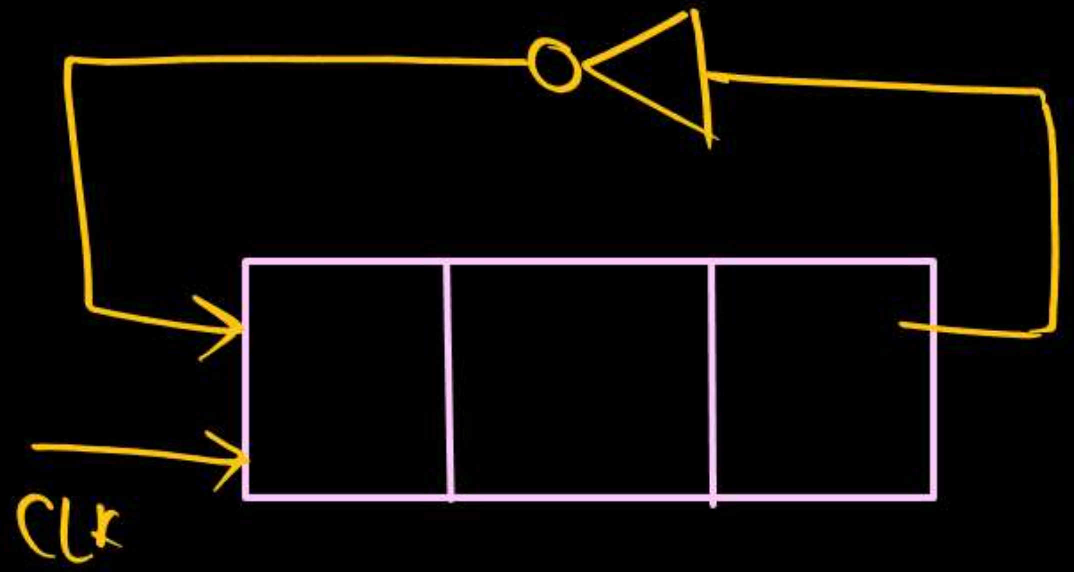
4 bit Johnson counter

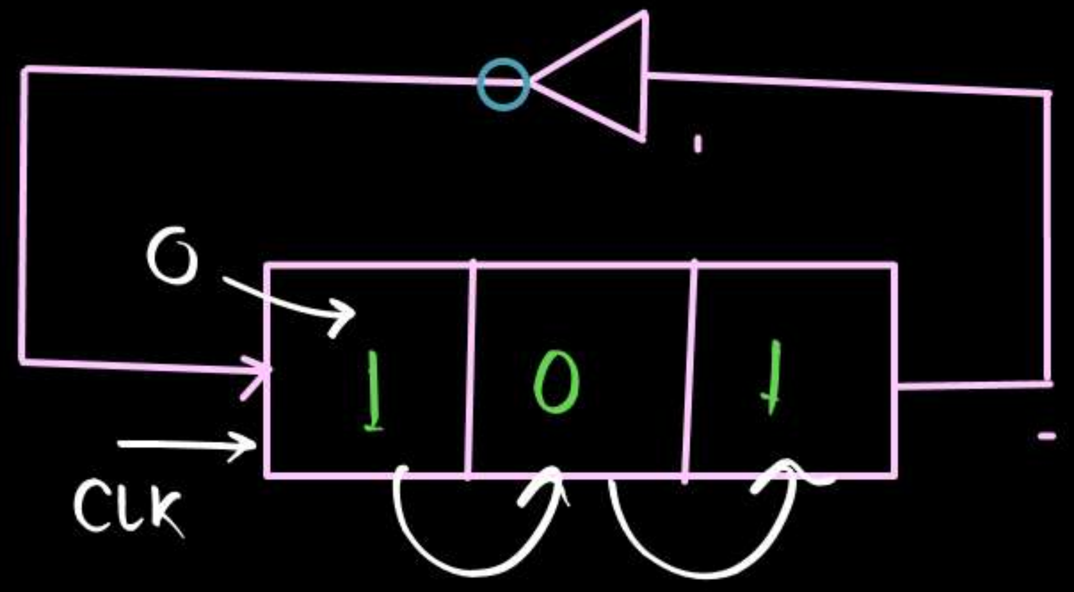
$$8\,MOD \left\{ \begin{array}{cccc} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \end{array} \right.$$

'N' bit Johnson counter

Used state = MOD = 2N

Symbolic Representation



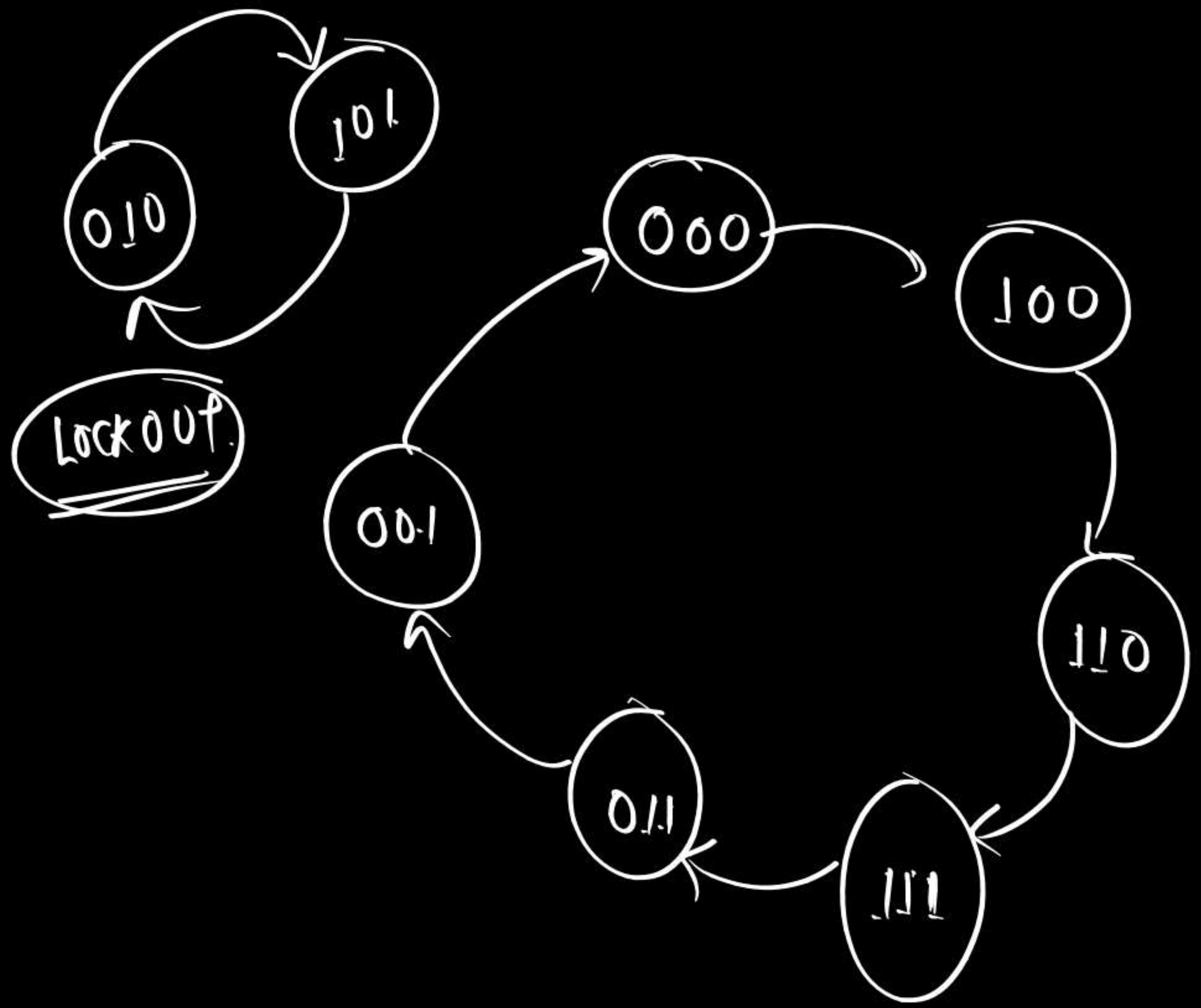


LOCKOUT PROBLEM

Clock	Q_1	Q_2	Q_3
0	0	1	0
1.	1	0	1
2.	0	1	0
3.	1	0	1
4	0	1	0

Lock into unused state

000
001
Unused → 010
011
100
Unused → 101
110
111



010
101
LOCKOUT
000
100
110
111
011
001

Synchronous Counter Design

Step-1: Write the present and Next state.

Step 2. Write the excitation table of Flip-Flop.

Step 3. Write the Logical expression

Step 4. Minimization

Step 5 → Hardware Implementation.

Q Design a synchronous counter by using T-FF which count

$\{ \overset{Q_1 Q_0}{00} \to 01 \to 10 \to 11 \}$

Step 1.

Step 2.

Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

Step 3.
Step 4

$T_1 = \bar{Q}_1 Q_0 + Q_1 Q_0$

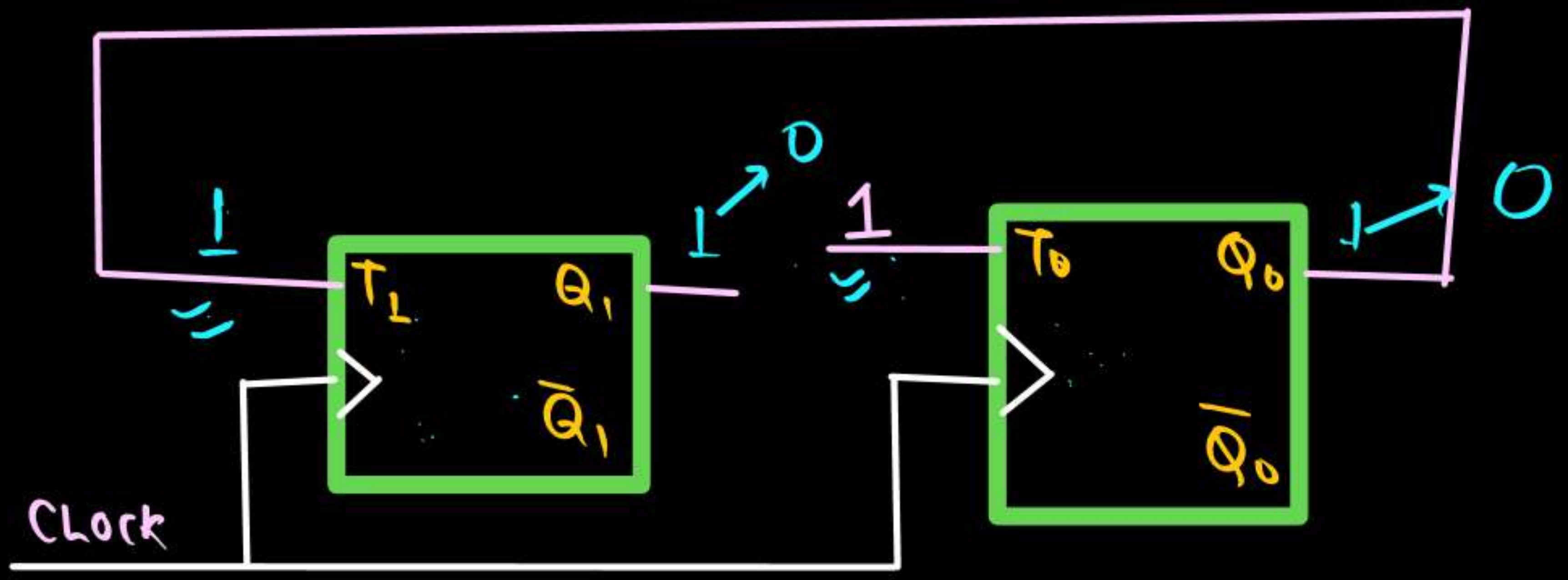
$T_1 = Q_0(\bar{Q}_1 + Q_1)$

$\boxed{T_1 = Q_0}$

$\boxed{T_0 = 1}$

Step 5:

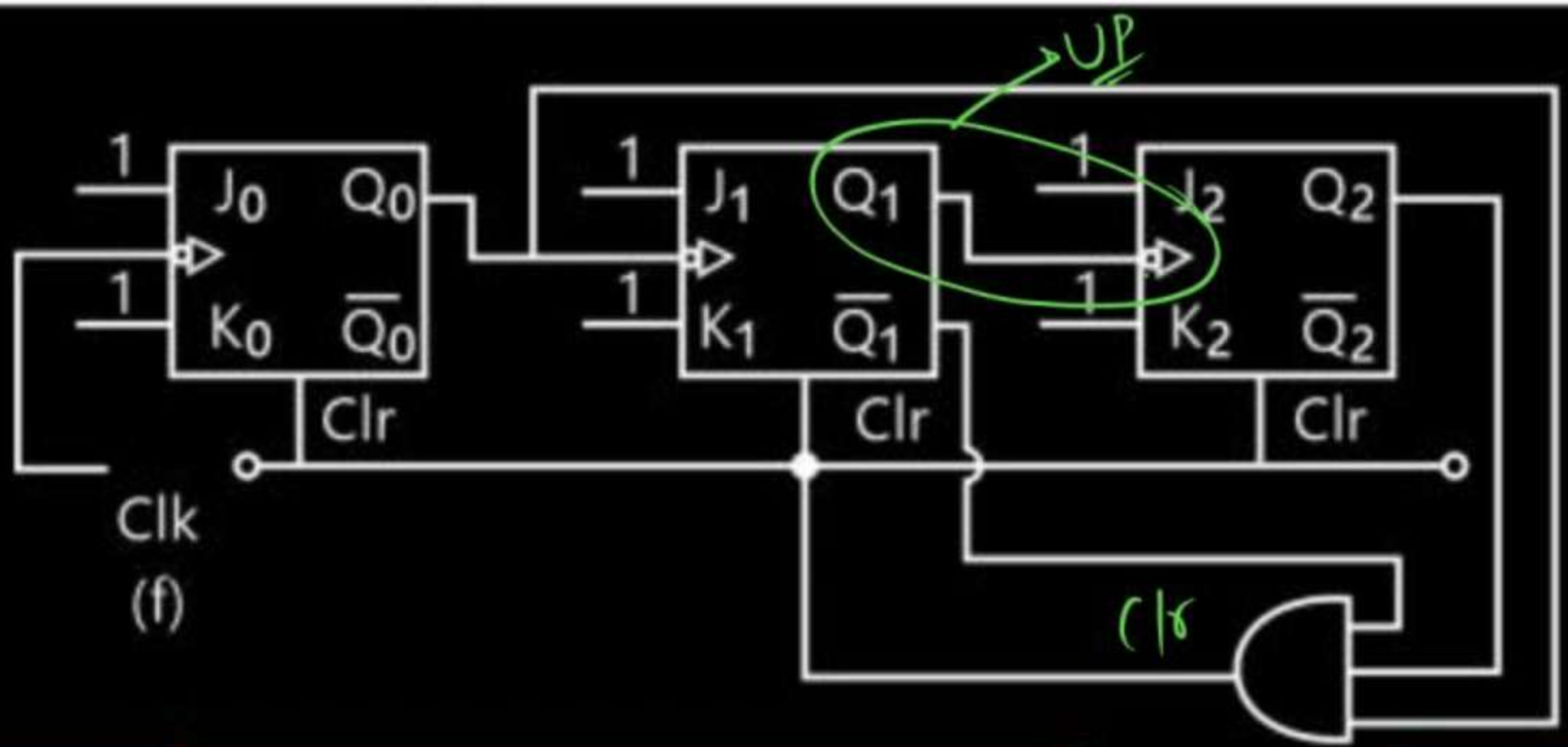
$T_1 = Q_0$ $T_0 = 1$



Clock	Q_1	Q_0
0	0	0
1	0	1
2	1	0
3	1	1
4	0	0

#CHAMKA

Q. Which type of counter is shown below?



$Clr = Q_2\bar{Q}_1 Q_0$

$1\ 0\ 1 = 5$

A. mod 5 down counter

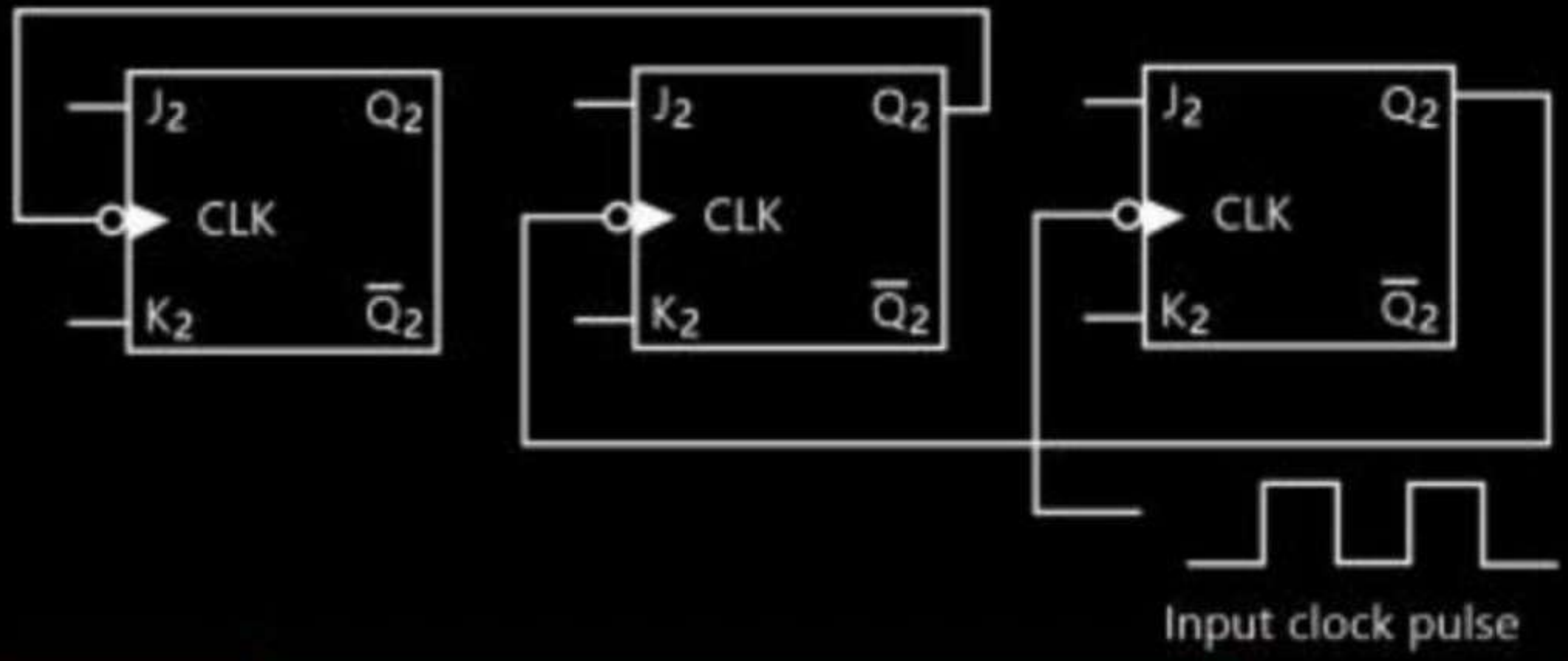
B. mod 5 up counter

C. mod 6 up counter

D. mod 6 down counter

Q. Consider the following counter

If counter starts at 000, what will be the count after 13 clock pulses?



HW

Comment

A 100

B 101

C 110

D 111

BCD

Clr = ?

सपने उनके सच होते हैं,
जिनके सपनों में जान होती है,
पँखो से कुछ नहीं होता,
हौंसलो से उड़ान होती है।


THANK YOU!

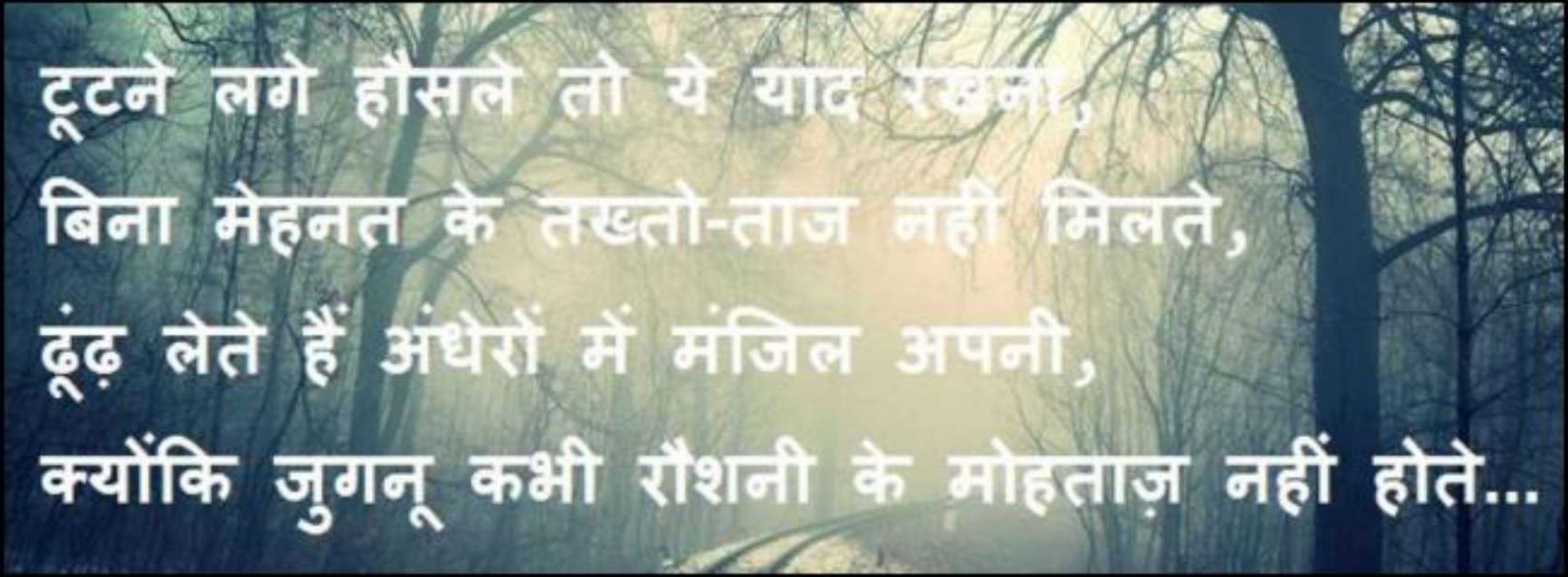
EC/EE/CS & IT/IN

Digital Electronics

NUMBER SYSTEM

LECTURE NO. 11

Chandan Jha Sir (CJ Sir)


टूटने लगे हौसले तो ये याद रखना,
बिना मेहनत के तख्तो-ताज नहीं मिलते,
ढूंढ़ लेते हैं अंधेरों में मंजिल अपनी,
क्योंकि जुगनू कभी रौशनी के मोहताज़ नहीं होते...

ABOUT ME

- Cleared Gate Multiple times with double Digit Rank (AIR 23, AIR 26)
- Qualified ISRO Exam
- Mentored More then 1 Lakhs+ Students (Offline & Online)
- More then 250+ Motivational Seminar in various Engineering College including NITs & Some of IITs

Chandan Jha

SYNCHRONOUS COUNTER

STEP 1. Write the Present and next state.

STEP 2. Write the Excitation Table of FF.

STEP 3. Write the Logical Expression.

STEP 4. Minimize the Logical expression.

STEP 5. Hardware Implementation.

Q Design a Synchronous Counter by using "T" Flip Flop which count the sequence

$0 \rightarrow 2 \rightarrow 3 \rightarrow 0$ $\{00 \rightarrow 10 \rightarrow 11 \rightarrow 00 \rightarrow \dots\}$

Method 1

Step 1

Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	1	0	1	0
1	0	1	1	0	1
1	1	0	0	1	1

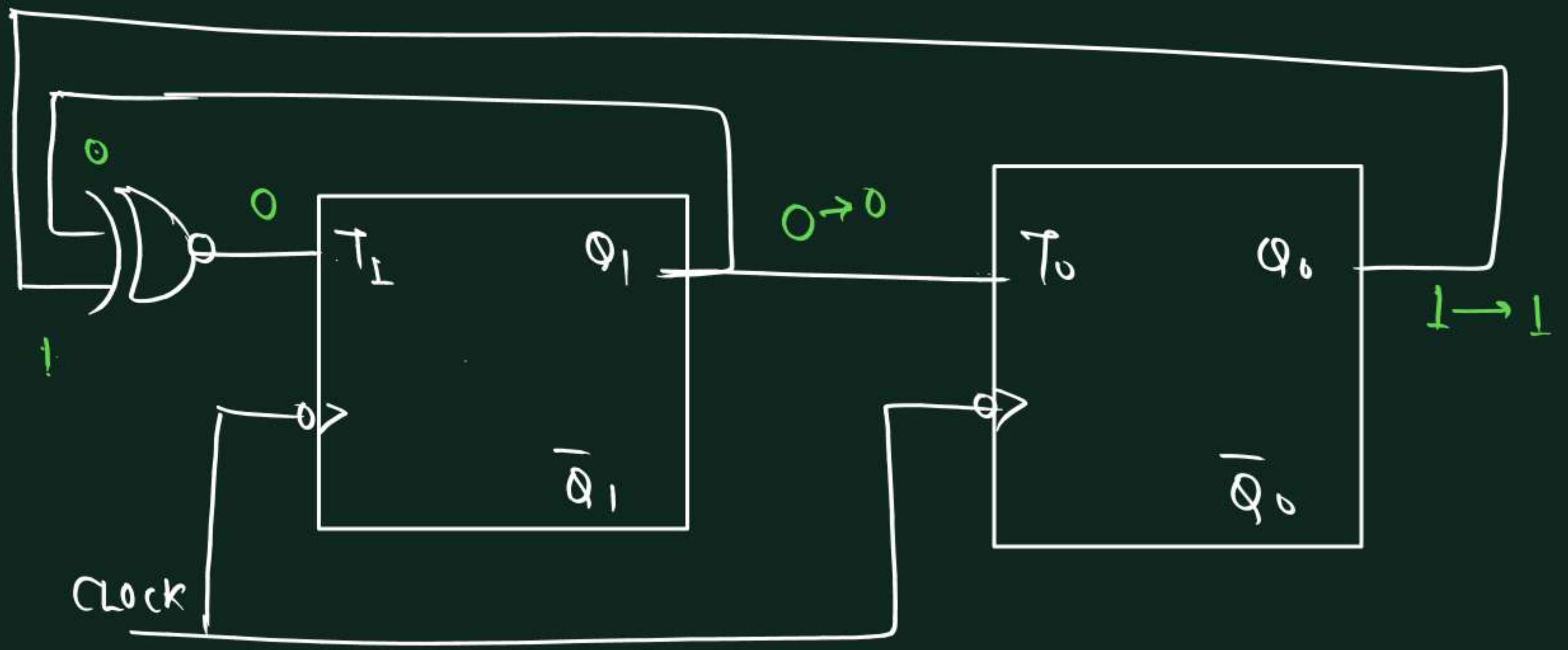
Step 3.

Step 4. $T_1 = \bar{Q}_1\bar{Q}_0 + Q_1Q_0$

$$\boxed{T_1 = Q_1 \odot Q_0}$$

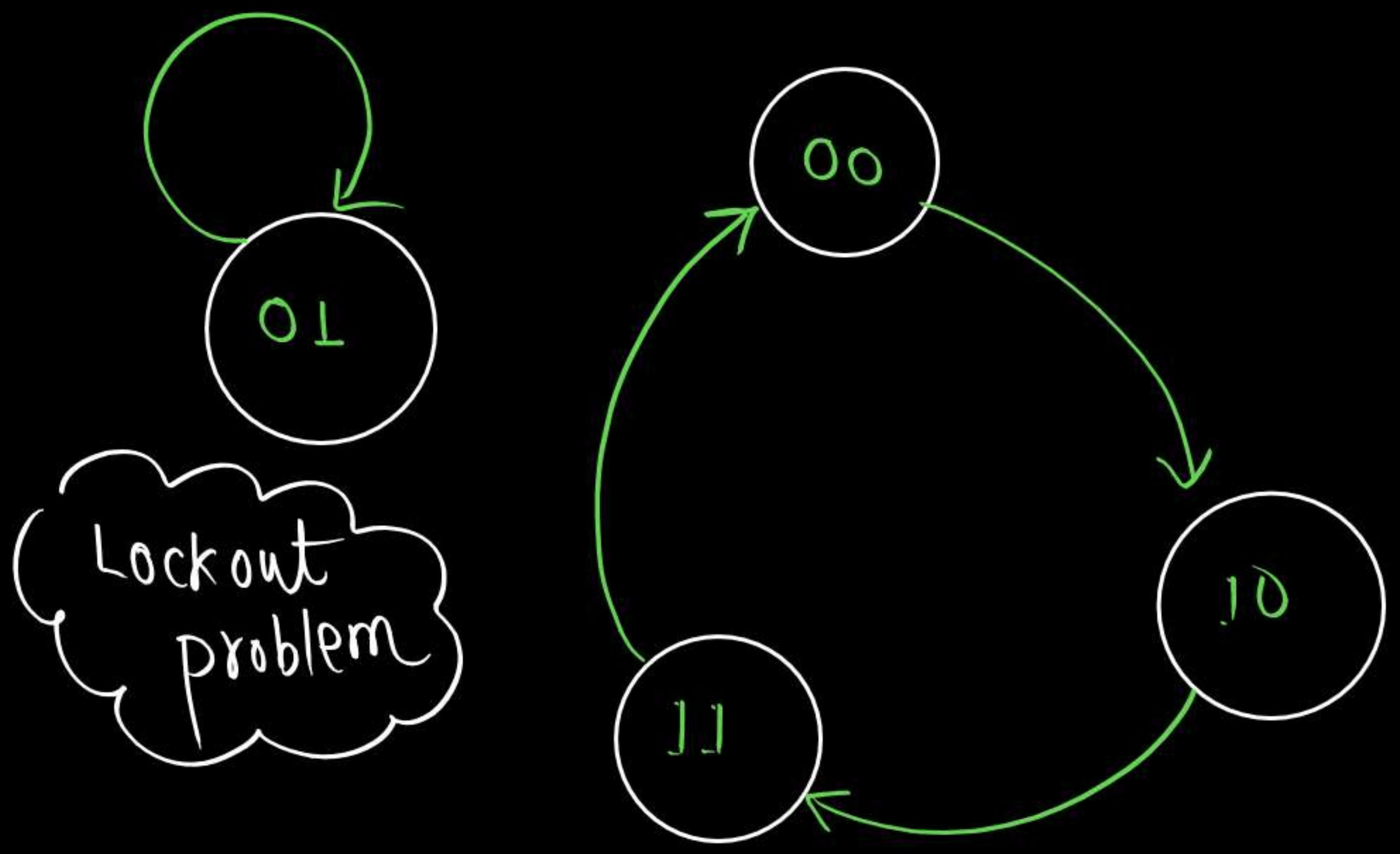
$T_0 = Q_1\bar{Q}_0 + Q_1Q_0$

$$\boxed{T_0 = Q_1}$$



Clock	Q_1	Q_0
0	0	0
1	1	0
2	1	1
3	0	0
4	1	0
	1	1

01 → Not used


01
Lockout problem
00
10
11

Method ② Without lockout design. $\{00 \rightarrow 10 \rightarrow 11 \rightarrow 00\}$

Step 1

Step 2

Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	1	0	1	0
0	1	X	X	X	X
1	0	1	1	0	1
1	1	0	0	1	1

Step 3

Step 4

$T_1 \rightarrow$

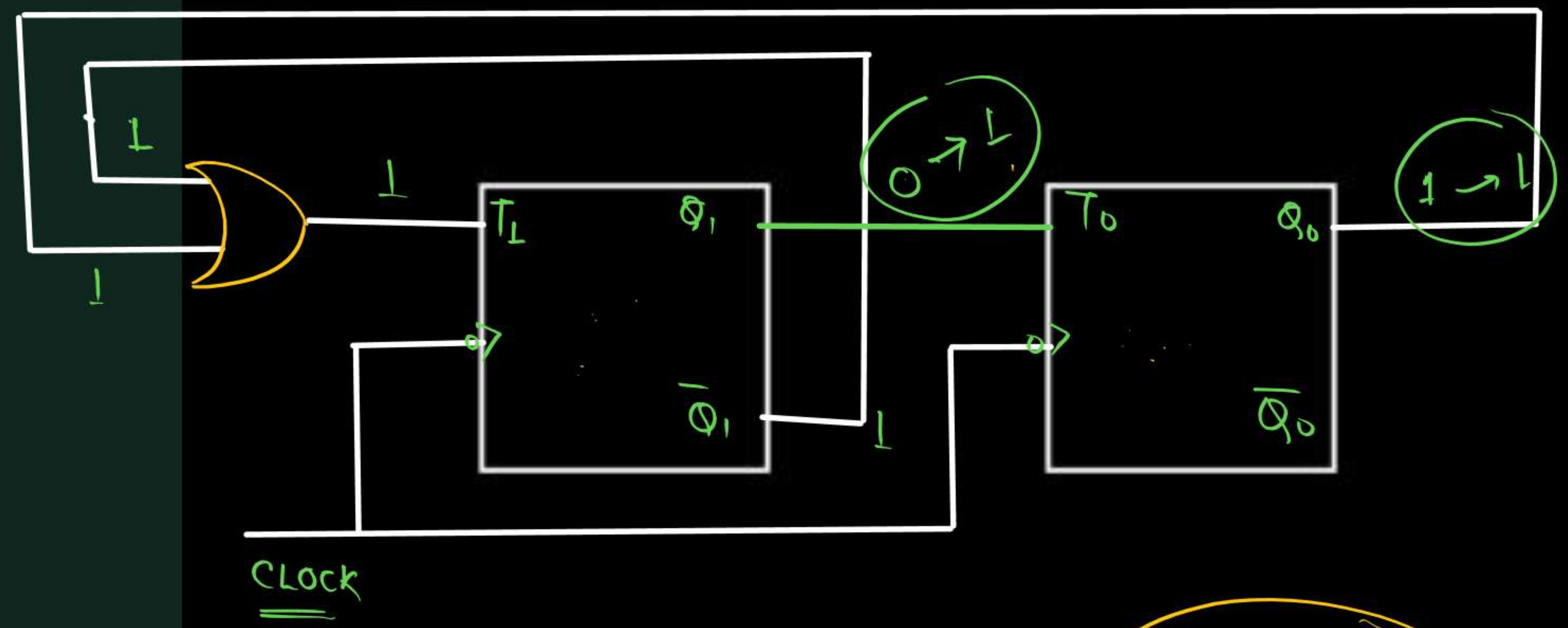
$Q_1 \backslash Q_0$	0	1
0	1	X
1		1

$$T_1 = \bar{Q}_1 + Q_0$$

$\rightarrow T_0$

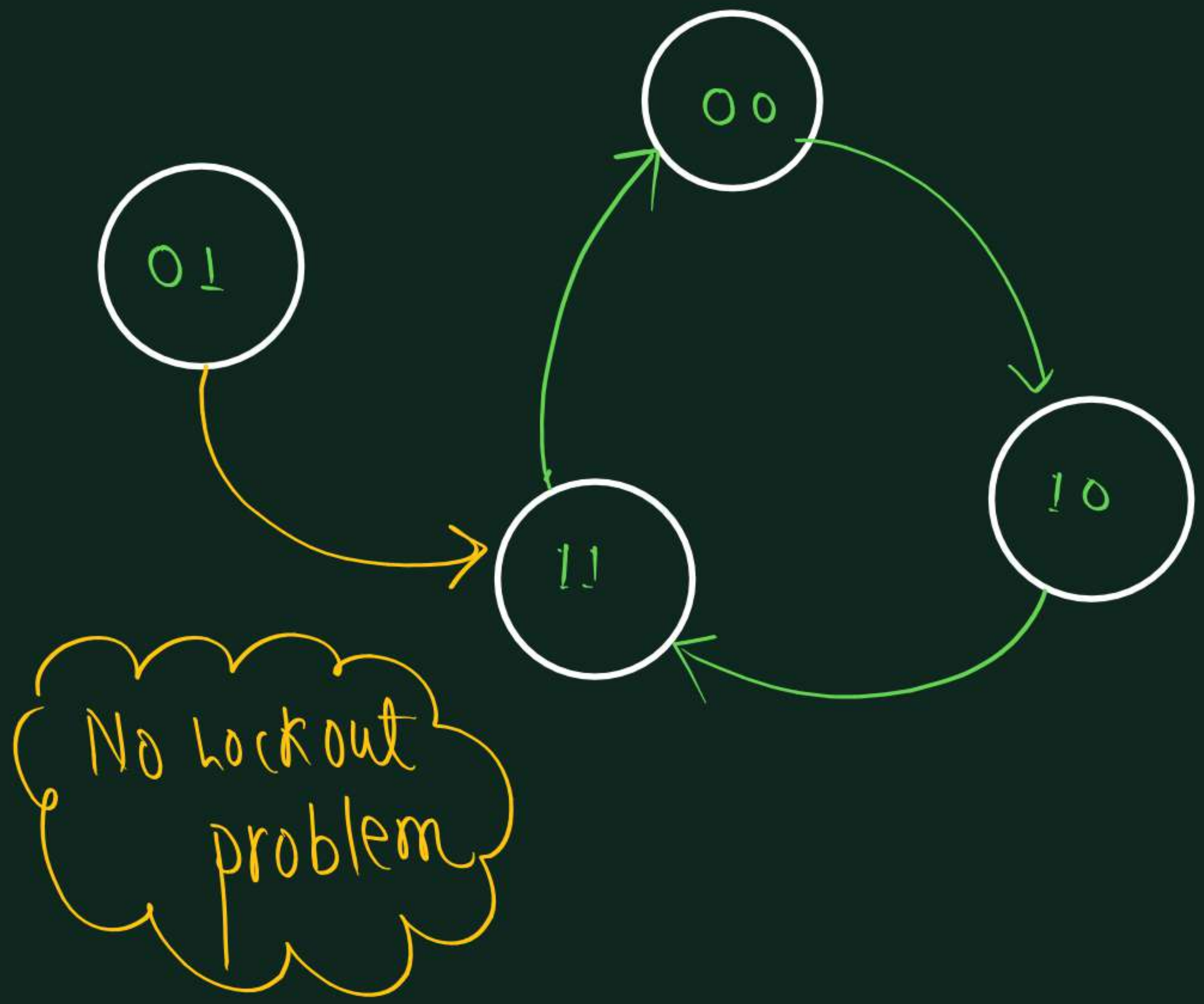
$Q_1 \backslash Q_0$	0	1
0		X
1	1	1

$$T_0 = Q_1$$

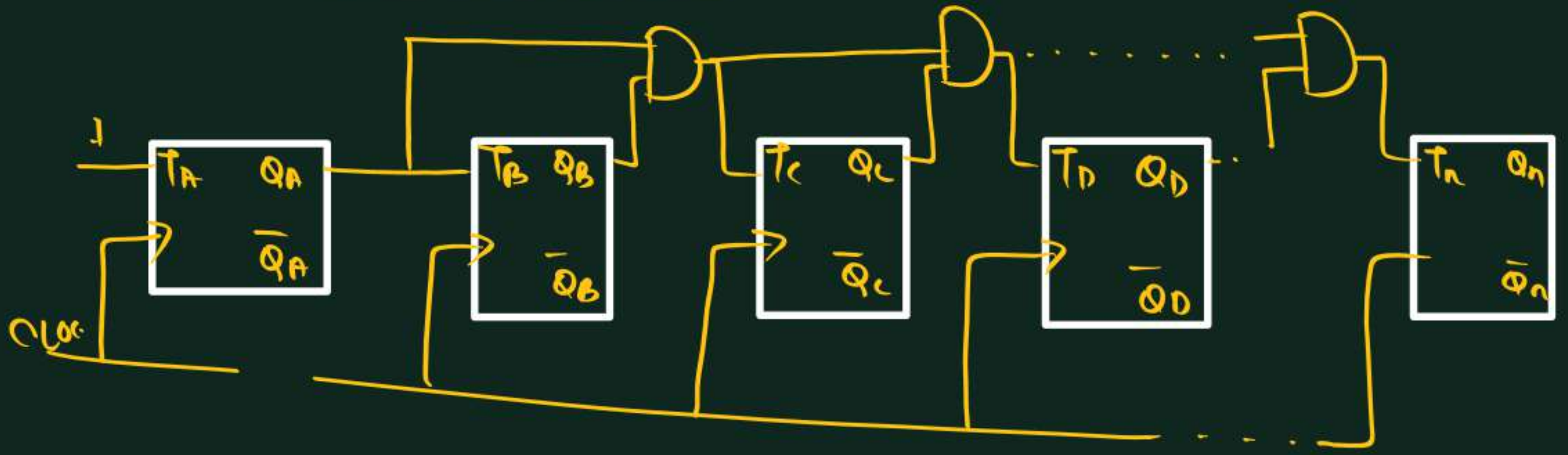


Clock	Q_1	Q_0
0	0	0
1	1	0
2	1	1
3	0	0
4	1	0

01 → unused


00
01
10
11
No lockout problem

Series carry synchronous counter.



$$\boxed{T_{clk} \geq \tau_{pd_{ff}} + (n-2)\,\tau_{pd_{AND}}}$$

$$\boxed{f_{clk} \leq \frac{1}{\tau_{pd_{ff}} + (n-2)\,\tau_{pd_{AND}}}}$$

parallel carry synchronous counter

$$\boxed{T_{clk} \geq \tau_{pd_{ff}} + \tau_{pd_{AND}}}$$

$$\boxed{f_{clk} \leq \frac{1}{\tau_{pd_{ff}} + \tau_{pd_{AND}}}}$$


कामयाबी मुझे ना मिले ये अलग बात हैं।
पर मै मेहनत ही न करुँ ये गलत बात हैं।

Nikhil 8

Final

48

100 200

43

Drop 63

57

Rohit

Avg

91

93

19

78

<10

Q

Design a Synchronous Counter by using T Flip Flop which count the sequence

HW

$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 0$

NUMBER SYSTEM

- ✓ BASE CONVERSION
- ✓ MAGNITUDE REPRESENTATION

जो मुस्कुरा रहा है उसे दर्द ने पाला होगा
जो चल रहा है उसके पाँव में छाला होगा
बिना संघर्ष के इंसान चमक नहीं सकता
जो जलेगा उस दिये में तो उजाला होगा

Can't say

$(12C)_{13, 14, 15, 16}$

BASE(RADIX)

$(101)_x$ $(12C)_{x=13,14,15,16}$

BASE(RADIX)	DIGIT
2	0, 1
3	0, 1, 2
4	0, 1, 2, 3
5	0, 1, 2, 3, 4
6	0, 1, 2, 3, 4, 5
7	0, 1, 2, 3, 4, 5, 6,
Octal 8	0, 1, 2, 3, 4, 5, 6, 7
9	0, 1, 2, 3, 4, 5, 6, 7, 8

BASE(RADIX)	DIGIT
Decimal 10	0 – 9
11	0 – 9, A
12	0 – 9, A, B
13	0 – 9, A, B, C
14	0 – 9, A, B, C, D
15	0 – 9, A, B, C, D, E
16	0 – 9, A – F

$10^2 \; 10^1 \; 10^0$

$(523)_{10}$

Cofficient

$5 \times 10^2 + 2 \times 10^1 + 3 \times 10^0$

$(a_3 \; a_2 \; a_1 \; a_0)_r$

$r^3 \quad r^2 \quad r^1 \quad r^0$

$a_3 \quad a_2 \quad a_1 \quad a_0$

Binary

$$(1011)_2$$

$$2^3 \quad 2^2 \quad 2^1 \quad 2^0$$

$$1 \quad 0 \quad 1 \quad 1$$

Any Base to Decimal Conversion:

$$\begin{array}{cccccc} r^3 & r^2 & r^1 & r^0 & r^{-1} & r^{-2} \\ \end{array}$$
$$(a_3\ a_2\ a_1\ a_0 \cdot a_{-1}\ a_{-2})_r = (\ ?\ )_{10}$$

$$\left[(a_3 \times r^3) + (a_2 \times r^2) + (a_1 \times r^1) + (a_0 \times r^0) + (a_{-1} \times r^{-1}) + (a_{-2} \times r^{-2})\right]_{10}$$

Ex ① Binary to Decimal

$$\begin{array}{cccccc} 2^3 & 2^2 & 2^1 & 2^0 & 2^{-1} & 2^{-2} \\ \end{array}$$
$$(1011 \cdot 11)_2 = (\ ?\ )_{10}$$

$$(1 \times 2^3 + 0 \times 2^0 + 1 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 1 \times 2^{-2})_{10}$$

$$8 + 0 + 2 + 1 + 0.5 + 0.25 \Rightarrow (11.75)_{10}$$

Ex. Octal to Decimal

$$\overset{8^2\,8^1\,8^0}{(623)_8} = (\,?\,)_{10}$$

$$6\times8^2 + 2\times8^1 + 3\times8^0$$

$$= 6\times64 + 16 + 3$$

$$= (403)_{10}$$

Ans

Ex. Hexadecimal to Decimal

Q $\overset{16^2\,16^1\,16^0}{(A2F)_{16}} = (\,?\,)_{10}$

$$A\times16^2 + 2\times16^1 + F\times16^0$$

$$10\times16^2 + 2\times16 + 15$$

$$(2607)_{10}$$

Ans

$$\left\{\begin{array}{l} A=10 \\ B=11 \\ C=12 \\ D=13 \\ E=14 \\ F=15 \end{array}\right.$$

Any Base to Decimal Conversion:

Ex. Determine the base of the numbers in each case for the following operations to be correct:

a) 14/2 = 5

b) 54/4 = 13

c) 24 + 17 = 40

(a) $\left(\frac{14}{2}\right)_x = (5)_x$

$\frac{(14)_x}{(2)_x} = (5)_x$

$\frac{1 \times x^1 + 4 \times x^0}{2 \times x^0} = 5 \times x^0$

$\frac{x+4}{2} = 5$

$x + 4 = 10$

$\boxed{x = 6}$

(b) $\left(\frac{54}{4}\right)_x = (13)_x$

$\frac{(54)_x}{(4)_x} = (13)_x$

$\frac{5 \times x^1 + 4 \times x^0}{4 \times x^0} = 1 \times x^1 + 3 \times x^0$

$5x + 4 = 4[x + 3]$

$5x + 4 = 4x + 12$

$x = 8$

$24 + 17 = 40$

$(24)_x + (17)_x = (40)_x$

$[2 \times x^1 + 4 x^0] + [1 \times x^1 + 7 \times x^0] = [4 \times x^1 + 0 \times x^0]$

$2x + 4 + x + 7 = 4x$

$x = 11$

Ans

Q $(432)_5 = (\ ?\ )_{10}$

$4 \times 5^2 + 3 \times 5^1 + 2 \times 5^0$

$100 + 15 + 2$

$(117)_{10}$ Ans

Q $(243)_4 = (\ ?\ )_{10}$

$2\times4^2 + 4\times4^1 + 3\times4^0$

$32 + 16 + 3$

$(51)_{10}$

Written in wrong format

Decimal to Any Base Conversion

$$(\underbrace{a_3\, a_2\, a_1\, a_0}\cdot\underbrace{a_{-1}\, a_{-2}\, a_{-3}})_{10} = (\quad ? \quad)_r$$

r	$a_3\, a_2\, a_1\, a_0$	R
		x_0
		x_1
		x_2
		x_3

$$0\cdot a_{-1}\, a_{-2}\, a_{-3} \times r = b_0 \cdot a_{-4}\, a_{-5}\, a_{-6} \qquad b_0$$

$$0\cdot a_{-4}\, a_{-5}\, a_{-6} \times r = b_1 \cdot a_{-7}\, a_{-8}\, a_{-9} \qquad b_1$$

$$0\cdot a_{-7}\, a_{-8}\, a_{-9} \times r = b_2 \cdot a_{-10}\, a_{-11} \qquad b_2$$

$$(x_3\, x_2\, x_1\, x_0 \cdot b_0\, b_1\, b_2)_r$$

Ans

Decimal to Any Base Conversion

Ex. Decimal to Binary

$(\underbrace{13}.\underbrace{75})_{10} = (\ ?\ )_2$ $\boxed{r=2}$

2	13	R
2	6	1
2	3	0
	1	1
		1

$0.75 \times 2 = 1.5$ 1

$0.5 \times 2 = 1.0$ 1

$(13.75)_{10} = (1101.11)_2$

Ans

Decimal to Any Base Conversion

Ex. Convert the number given below in decimal to Binary, 4th order, octal, Hexadecimal

(1) 319.6875

$(319.687)_{10} = (\quad)_8$

$(319.687)_{10} = (\quad)_2$

$8 \,|\, 319$ R

$0.687 \times 8 =$

$2 \,|\, 319$ R

0.687×2

Decimal to Any Base Conversion

(1) $\underbrace{319}.\underbrace{6875} = (\ ?\ )_2$

Ans.

		R
2	319	
2	159	1
2	79	1
2	39	1
2	19	1
2	9	1
2	4	1
2	2	0
	1	0
		1

$0.6875 \times 2 = 1.375 \Rightarrow 1$

$0.375 \times 2 = 0.75 = 0$

$0.75 \times 2 = 1.5 = 1$

$0.5 \times 2 = 1.0 = 1$

$(100111111.1011)_2$ Ans

Decimal to Any Base Conversion

$(319.6875)_{10} = (\ ?\ )_4$

4	319	R
4	79	3
4	19	3
4	4	3
4	1	0
	0	1

$0.6875 \times 4 = 2.75 = 2$

$0.75 \times 4 = 3.0 \quad 3$

$\Rightarrow (10333.23)_4$

Ans

Decimal to Any Base Conversion

$(319.6875)_{10} = (\ ?\ )_8$

8	319	R
8	39	7
8	4	7
	0	4

$0.6875 \times 8 = 5.5 = 5$

$0.5 \times 8 = 4.0 = 4$

$\Rightarrow (477.54)_8$

Ans

Decimal to Any Base Conversion

$(319.6875)_{10} = (\ ?\ )_{16}$

Hexadecimal

16	319	R
16	19	15 → F
16	1	3
	0	1

$(13F.B)_{16}$ Ans

DECJ

$0.6875 \times 16 = 11.0$ 11(B)

$\Rightarrow$ (13 F.B)

₹100 NOTE

Ex $(1011)_2 = (\ ?\ )_4$

Method (1) $(1011)_2 \longrightarrow (\quad)_{10}$

$\longrightarrow (\quad)_4$

$(1011)_2 = (11)_{10} = (23)_4$

$(1011)_2 = (\quad)_{10}$

$1\times2^3+0\times2^2+1\times2^1+1\times2^0$

$(11)_{10} \longrightarrow (\quad)_4$

4	11	R
	2	3
		2

Method 2

$(1011)_2 = (\quad)_4$

$4 = 2^{2}$

2 bits

$\overbrace{1\ 0}\ \overbrace{1\ 1}$

2 3

$(1011)_2 = (23)_4$

Ans

Ex

$(2331)_4 = (\ ?\ )_2$

$\hookrightarrow 4 = 2^{2} =$

Mentos Jindgi

$[1011111101]_2$

Ans

Ex. $(3201)_4 = (\quad)_8$

Method ① Aam zindgi

$(3201)_4 \Rightarrow (\quad)_{10} \Longrightarrow (\quad)_8$

Method ② Mendos zindgi

$(3201)_4 \longrightarrow (\quad)_2 \longrightarrow (\quad)_8$

$4 = 2^{2}$ → 2 bits

$8 = 2^{3}$ → 3 bits

$(\underbrace{011}_{3}\,\underbrace{100}_{4}\,\underbrace{001}_{1})_2$

$(341)_8$ Ans

Q $(745)_8 = (\ ?\ )_{16}$

$8 = 2^3$

$7 \rightarrow 111$ (4 2 1)

Method 1. Aam Zindgi [Normal Army]

$(745)_8 \longrightarrow (\quad)_{10} \longrightarrow (\quad)_{16}$

Method 2. Mendos zindgi [CJ Army]

$(745)_8$ $\;8 \to 2^3 \to$ 3 bits

$(\ -\ )_{16}$

$16 = 2^4 \to$ 4 bits group.

$\overbrace{0001}^{1}\ \overbrace{1110}^{14\ E}\ \underbrace{0101}_{5}$

$(1E5)_{16}$ Ans

Decimal to Any Base Conversion

Ex. 1. A number is 120 in octal (that is, base 8) notation. The same number is decimal (base 10) notation would be

A. 56

B. 80

C. 86

D. NONE

Decimal to Any Base Conversion

Ex. 2. Representation of $(23.14)_6$ in base 5 number system will be ____ (upto two decimal)

$$(23.14)_6 = (\ ?\ )_5$$

$$(23.14)_6 = (\ .\ )_{10}$$

$$\left(2\times6^{1}+3\times6^{0}+1\times6^{-1}+4\times6^{-2}\right)_{10}$$

$$(15.277)_{10} = (\quad)_5$$

Solution. $(23.14)_6 = [(2 \times 6^1) + (3 \times 6^0) + (1 \times 6^{-1}) + (4 \times 6^{-2})] = (15.277)_{10}$

5	15	0
	3	3

$\Rightarrow (15)_{10} = (30)_5$

0.277 × 5 = 1 .385 1

0.385 × 5 = 1 .925 1

$\Rightarrow (0.277)_{10} = (0.11)5$

Hence

$(15.277)_{10} = (30.11)_5$

$(30 \cdot 11)_5$

Ans

	8	4	2	1
0 →	0	0	0	0
1 →	0	0	0	1
2 →	0	0	1	0
3 →	0	0	1	1
4 →	0	1	0	0
5 →	0	1	0	1
6 →	0	1	1	0
7 →	0	1	1	1

Magnitude Representation.

	unsigned	Signed	complement 1's	complement 2's
+5	101	0101	0101	0101
−5	X	1101	1010	1011

1's complement → Decimal

Q① 0 1101 → +13

Q② 00000 11001 → +25

Q③ 101001 → −22 Ans
010110

Q④ 111111101001 ⇒ −22 Ans
000000010110
22

Q⑤ 0000 → +0

Q⑥ 1111 → −0
0000

2's complement → Decimal

Q1 01101 → +13

Q2 000011001 → +25

Q3 101001 → −23

23 ← 010111

Q4 11111101001 → −23

00000010111

Q5 0000 → +0

Q6 1111 → −1

0001

EX. –13 in 2's complement will be-

A. 1 1 1 0 1

B. 0 1 1 0 1

C. 1 0 0 1 0

D. NONE

$+13 \longrightarrow \quad 0\,1\,1\,0\,1$

$-13 \quad\quad\quad\; \underline{1\,0\,0\,1\,1}$

EX. If $(12x)_3 = (123)_x$ then the value of x is

A. 3

B. 3 or 4

C. 2

D. None of these

$(123)_x$

$\begin{matrix} 3^2 & 3^1 & 3^0 \\ 1 & 2 & x \end{matrix}$ $\quad$ $\begin{matrix} x^2 & x^1 & x^0 \\ 1 & 2 & 3 \end{matrix}$

$(12x)_3 = (123)_x \qquad x = ?$

$(1\times 3^2 + 2\times 3^1 + x\times 3^0)_{10} = (1\times x^2 + 2x + 3\times x^0)_{10}$

$9 + 6 + x = x^2 + 2x + 3$

$15 + x = x^2 + 2x + 3$

$x^2 + x - 12 = 0$

$x^2 + x - 12 = 0$

$(x+4)(x-3) = 0$

$x = -4 \qquad x = 3$

Ex. 11001, 1001 and 111001 correspond to the 2's complement representation of which one of the following sets of number?

A. 25,9 and 57 respectively

B. -6, -6 and -6 respectively

C. -7, -7 and -7 respectively

D. -25, -9 and -57 respectively

00111 → +7

11001 → -7

1001 → -7

0111

111001 -7

$1000

20 years

1 → Majdoor

999

1000

$$(1.01)^{365} \simeq 37$$

3700%

1%

$$(1)^{365} = 1$$

1%

$$(0.99)^{365} = 0.03\ldots$$


THANK
YOU!