

# DB Code

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March 2014

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1 library ieee;
2 use ieee.std_logic_1164.all;
3 use ieee.numeric_std.all;
4 use work.project_pack.all;
5 use work.draw_any_octant;
6
7 entity db is
8     generic(vsize : integer := 6);
9     port(
10         clk          : in std_logic;
11         reset        : in std_logic;
12
13         -- host processor connections
14         hdb          : in std_logic_vector(2*vsize+3 downto 0);
15         dav          : in std_logic;
16         hdb_busy     : out std_logic;
17
18         -- rcb connections
19         dbb_bus      : out db_2_rcb;
20         dbb_delaycmd : in std_logic;
21         dbb_rcbclear : in std_logic;
22
23         -- vdp connection
24         db_finish    : out std_logic
25     );
26 end db;
27
28 architecture rtl of db is
29     signal dao_draw, dao_xbias, dao_done, dao_swap, dao_negx, dao_negy,
30         dao_disable, dao_reset : std_logic;
31     signal dao_xin, dao_yin, dao_xout, dao_yout: std_logic_vector(vsize
32         downto 0);
33     signal pen_x, pen_y: std_logic_vector(vsize-1 downto 0);
34     signal previous_command : std_logic_vector(2*vsize+3 downto 0);
35
36     type state_t is (idle, draw_reset, draw_start, send_command);
37     signal state, nstate : state_t;
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36
37 type opcode_t is array (1 downto 0) of std_logic;
38 constant movepen_op : opcode_t := "00";
39 constant drawline_op : opcode_t := "01";
40 constant clearscreen_op : opcode_t := "10";
41
42 type pentype_t is array (1 downto 0) of std_logic;
43 constant white : pentype_t := "01";
44 constant black : pentype_t := "10";
45 constant invert : pentype_t := "11";
46
47 type command_t is record
48     op : opcode_t;
49     x, y : std_logic_vector(vsize-1 downto 0);
50     pen : pentype_t;
51 end record;
52 signal command_in, command, prev_command : command_t;
53 begin
54     -- decoding command
55     command_in.op <= opcode_t(hdb(2*vsize+3 downto 2*vsize+2));
56     command_in.x <= hdb(2*vsize+1 downto vsize+2);
57     command_in.y <= hdb(vsize+1 downto 2);
58     command_in.pen <= pentype_t(hdb(1 downto 0));
59
60     -- disable dao when rcb not ready
61     dao_disable <= dbb_delaycmd;
62
63     dao: entity draw_any_octant generic map(vsize) port map(
64         clk => clk,
65         resetx => dao_reset,
66         draw => dao_draw,
67         xbias => dao_xbias,
68         xin => dao_xin,
69         yin => dao_yin,
70         done => dao_done,
71         x => dao_xout,
72         y => dao_yout,
73         swapxy => dao_swap,
74         negx => dao_negx,
75         negy => dao_negy,
76         disable => dao_disable
77     );
78
79     read_new_command: process
80     begin
81         wait until clk'event and clk='1';
82         if state = idle and dav = '1' then
83             command.op <= opcode_t(hdb(2*vsize+3 downto 2*vsize+2));
84             command.x <= hdb(2*vsize+1 downto vsize+2);
85             command.y <= hdb(vsize+1 downto 2);

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86     command.pen <= pentype_t(hdb(1 downto 0));
87     prev_command <= command;
88     end if;
89 end process read_new_command;
90
91 set_dao_inputs: process(command, prev_command) -- drives negx, negy,
92     swapxy,                                     -- xin, yin, xbias
93     variable dx: signed(vsize downto 0);
94     variable dy: signed(vsize downto 0);
95     --variable zero : std_logic_vector(vsize-1 downto 0) := (others
96         =>'0');
97 begin
98     dx := signed(resize(unsigned(command.x), vsize+1)) -
99         signed(resize(unsigned(prev_command.x), vsize+1));
100     dy := signed(resize(unsigned(command.y), vsize+1)) -
101         signed(resize(unsigned(prev_command.y), vsize+1));
102     -- set negx if dx is negative
103     if dx >= 0 then
104         dao_negx <= '0';
105     else
106         dao_negx <= '1';
107     end if;
108     -- set negy if dy is negative
109     if dy >= 0 then
110         dao_negy <= '0';
111     else
112         dao_negy <= '1';
113     end if;
114     -- set swapxy if dx is closer to 0 than dy
115     if abs(dx) < abs(dy) then
116         dao_swap <= '1';
117     else
118         dao_swap <= '0';
119     end if;
120     --
121     if state = draw_reset then
122         dao_xin <= prev_command.x;
123         dao_yin <= prev_command.y;
124     else
125         dao_xin <= command.x;
126         dao_yin <= command.y;
127     end if;
128     dao_xbias <= 'X'; --God knows
129 end process set_dao_inputs;
130
131 db_fsm_clocked: process
132 begin
133     wait until clk'event and clk='1';
134     -- go to next state

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132     state <= nstate;
133 end process db_fsm_clocked;
134
135 db_fsm_comb: process(state, command, dav, dao_done, dbb_delaycmd) --
136     drives nstate, hdb_busy, dao_draw, dao_reset
137 begin
138     nstate <= state; --default, stay in current state
139     case state is
140     when idle =>
141         -- outputs for idle state
142         hdb_busy <= '0';
143         dao_draw <= '0';
144         dao_reset <= '0';
145         --compute next state
146         if dav = '1' then
147             --read command and decide which state to go to.
148             case command_in.op is
149             when movepen_op => nstate <= send_command;
150             when drawline_op => nstate <= draw_reset;
151             when clearscreen_op => nstate <= send_command;
152             when others => null;
153             end case;
154         end if;
155     when draw_reset =>
156         --outputs for draw_reset state
157         hdb_busy <= '1';
158         dao_draw <= '0';
159         dao_reset <= '1';
160         --compute next state
161         nstate <= draw_start;
162     when draw_start =>
163         --outputs for draw_start state
164         hdb_busy <= '1';
165         dao_draw <= '1';
166         dao_reset <= '0';
167         --compute next state
168         nstate <= send_command;
169     when send_command =>
170         --outputs for send_command state
171         hdb_busy <= '1';
172         dao_draw <= '0';
173         dao_reset <= '0';
174         --compute next state
175         if (command.op = drawline_op and dao_done = '0') or dbb_delaycmd
176             = '1' then nstate <= send_command;
177         else nstate <= idle;
178         end if;
179     when others => nstate <= idle; -- reset undefined states to idle
180     state
181 end case;

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179 end process db_fsm_comb;
180
181 send_rcb_inputs: process(state, prev_command, command, dao_xout,
182   dao_yout) --drives dbb_bus
183   variable undefined : std_logic_vector(vsize-1 downto 0) := (others
184     =>'X');
185 begin
186   if state = send_command then
187     if command.op = drawline_op then
188       dbb_bus.x <= dao_xout;
189       dbb_bus.y <= dao_yout;
190       dbb_bus.startcmd <= '1';
191     else
192       dbb_bus.X <= command.x;
193       dbb_bus.Y <= command.y;
194       dbb_bus.startcmd <= '1';
195     end if;
196   else
197     dbb_bus.X <= undefined;
198     dbb_bus.Y <= undefined;
199     dbb_bus.startcmd <= '0';
200   end if;
201
202   -- encode operation
203   case command.pen is
204     when white => dbb_bus.rcb_cmd(1 downto 0) <= "01";
205     when black => dbb_bus.rcb_cmd(1 downto 0) <= "10";
206     when invert => dbb_bus.rcb_cmd(1 downto 0) <= "11";
207     when others => dbb_bus.rcb_cmd <= "100"; -- invalid command
208   end case;
209   case command.op is
210     when movepen_op => dbb_bus.rcb_cmd <= "000";
211     when drawline_op => dbb_bus.rcb_cmd(2) <= '0';
212     when clearscreen_op => dbb_bus.rcb_cmd(2) <= '1';
213     when others => dbb_bus.rcb_cmd <= "100"; -- invalid command
214   end case;
215 end process send_rcb_inputs;
216
217 finished: process(state, dav) -- drives db_finish
218 begin
219   if state = idle and dav = '0' then db_finish <= '1';
220   else db_finish <= '0';
221   end if;
222 end process finished;
223 end rtl;

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