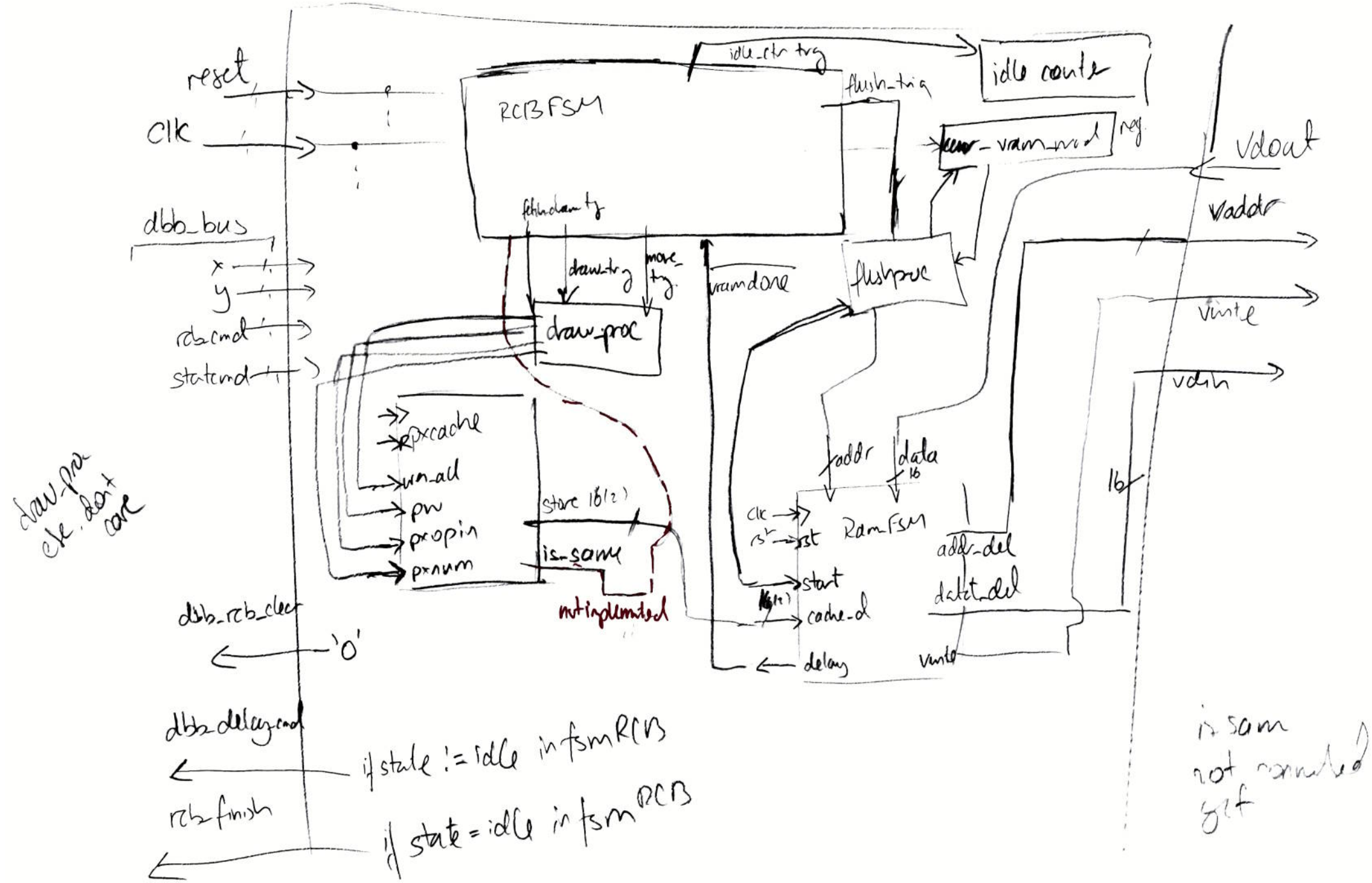
reset
clk
dbb_bus
x
y
rcbcmd
statemd
RCBFSM
idle_ctr trg
idle counter
flush_trig
vram_mod
reg
Vdout
Vaddr
Vinte
Vdin
fetchdraw trg
draw_trg
move_trg
vramdone
flushproc
draw_proc
pxcache
vram_ad
pw
pxpin
pxnum
store 16(2)
is_same
not implemented
addr
data
16
clk
rst
Ram_FSM
start
cache_d
delay
addr_del
datat_del
16
dbb_rcb_clear
'0'
dbb_delay_cmd
if state != idle in fsm RCB
rcb_finish
if state = idle in fsm RCB
draw_pxc
clk. don't care
is sam
not connected yet