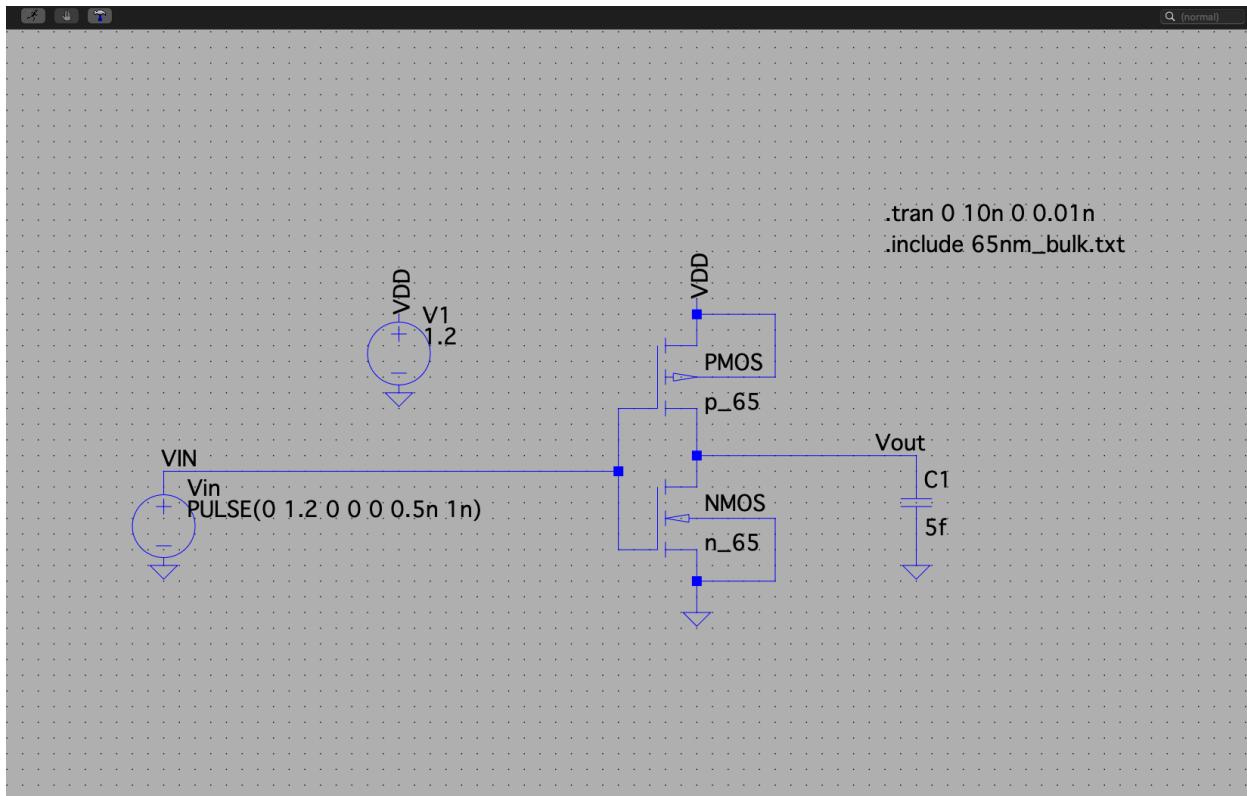


VLSI Summer School Project Documentation 2025

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Kushagra Poonia(23EE10036)

Assignment 1: CMOS Inverter

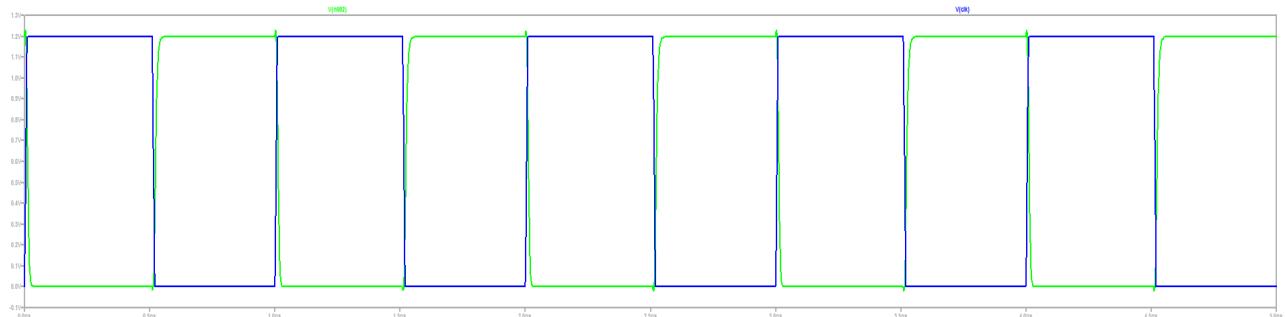
- Circuit Diagram



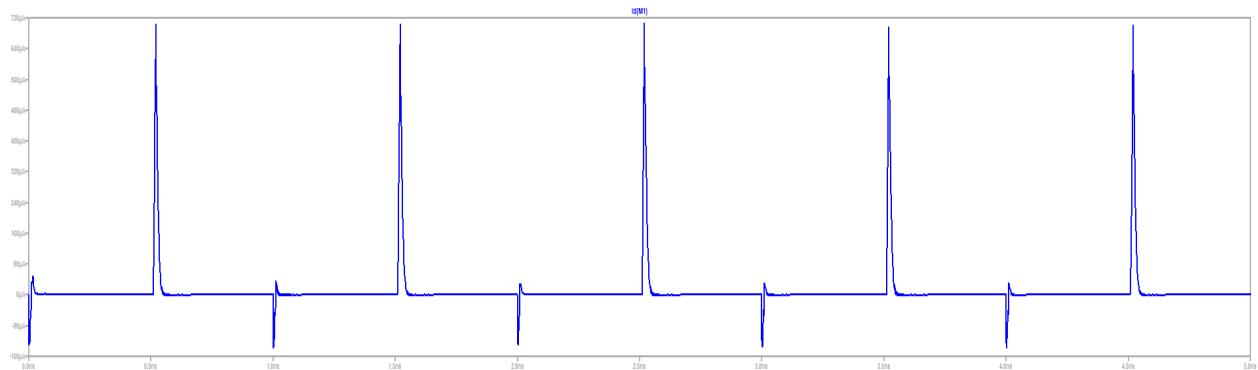
1. Simulate a CMOS inverter with following dimensions: PMOS = 1um/65nm NMOS = 0.5um/65nm, load capacitor = 5fF, Vdd = 1.2V

Assignment 1: CMOS Inverter

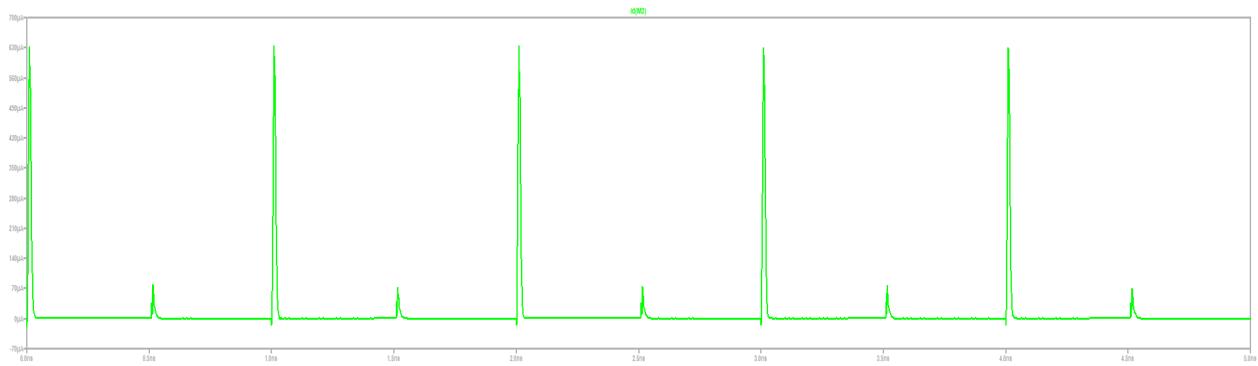
a) Perform transient simulation with 1 GHz clock signal, plot the input and output voltages, PMOS and NMOS currents.



Input Voltage (Blue) AND Output Voltage (Green)



$I_d(\text{PMOS})$



$I_d(\text{NMOS})$

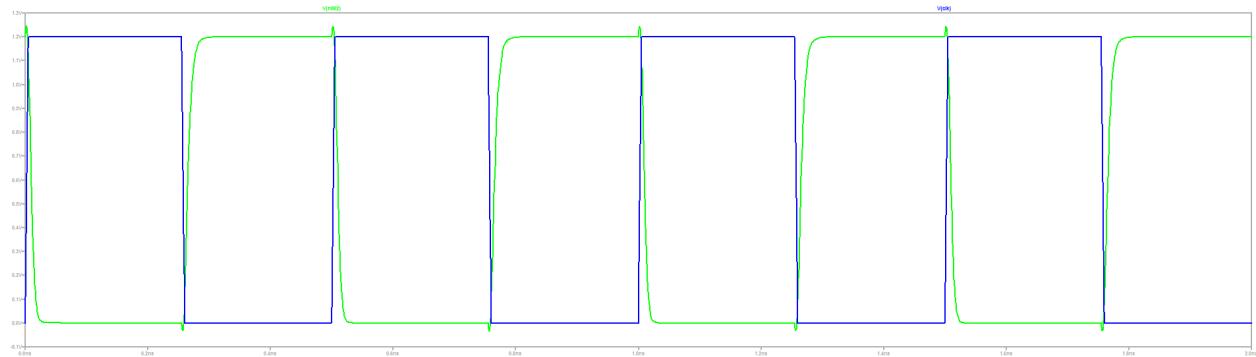
- Spice directive commands :

.tran 0 10n 0 0.01n

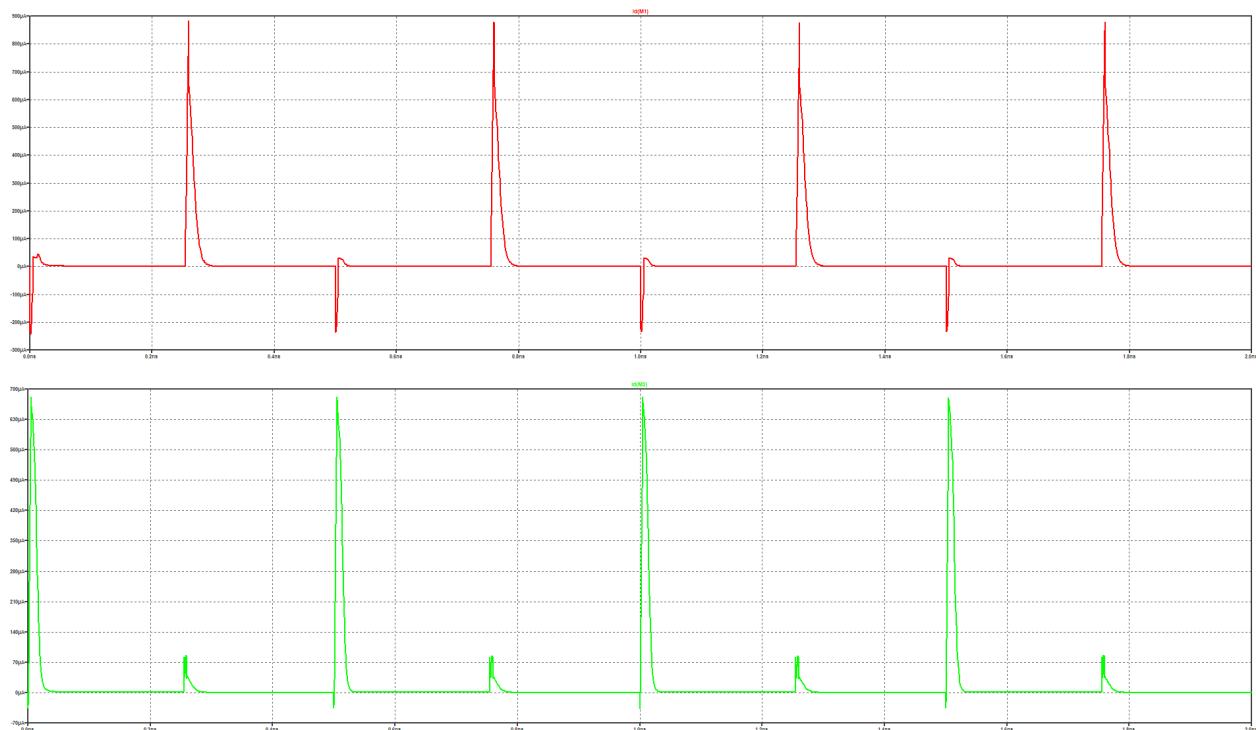
$V_{in} = \text{PULSE}(0 \ 1.2 \ 0 \ 0 \ 0 \ 0.5n \ 1n)$

Assignment 1: CMOS Inverter

- At 2G Hz



Input Voltage (blue) and Output Voltage (green)



I_d (PMOS, red) and I_d (NMOS, green)

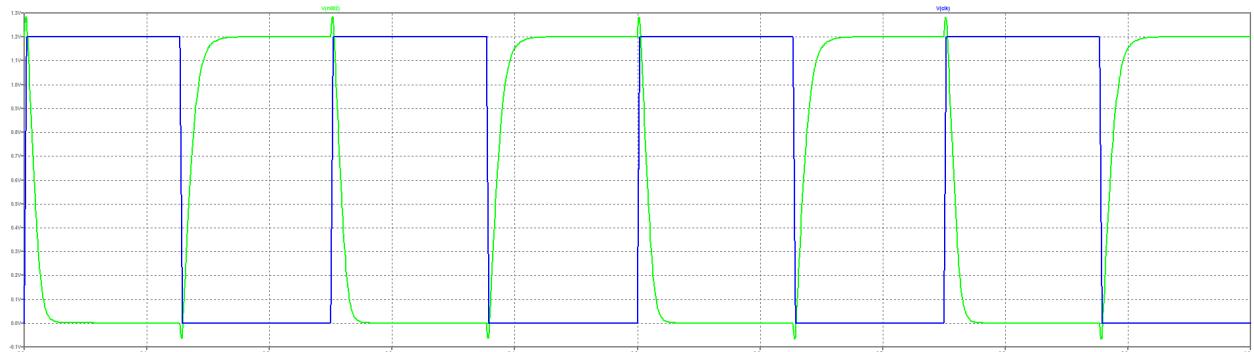
- Spice directive commands :

.tran 0 10n 0 0.01n

$V_{in} = \text{PULSE}(0 \ 1.2 \ 0 \ 0 \ 0 \ 0.25n \ 0.5n)$

Assignment 1: CMOS Inverter

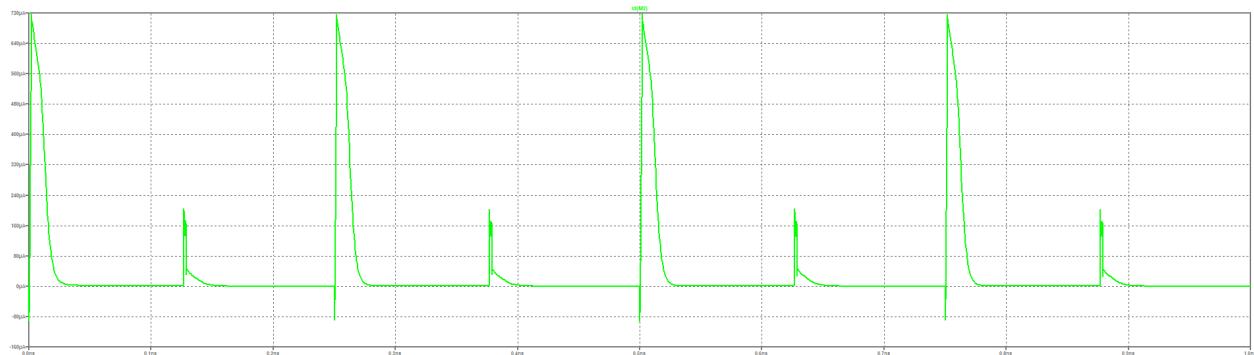
- At 4G Hz



Input Voltage (blue) and Output Voltage (green)



$I_d(PMOS)$



$I_d(NMOS)$

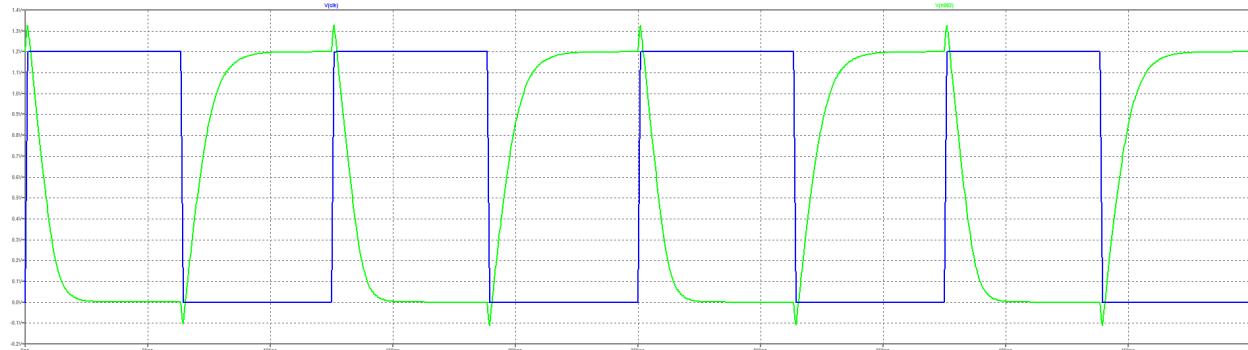
- Spice directive commands :

.tran 0 10n 0 0.01n

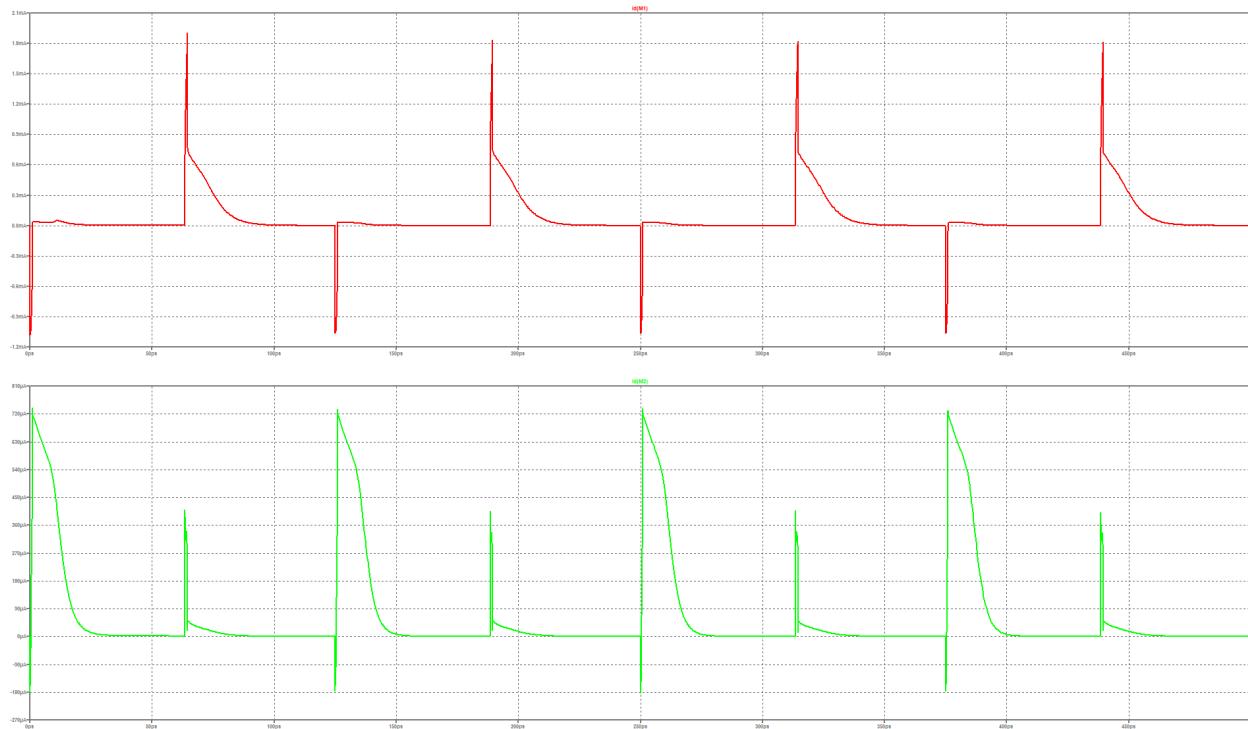
$Vin = PULSE(0 1.2 0 0 0 0.125n 0.25n)$

Assignment 1: CMOS Inverter

At 8G Hz



Input Voltage (blue) and Output Voltage (green)



$I_d(\text{PMOS},\text{red})$ and $I_d(\text{NMOS},\text{green})$

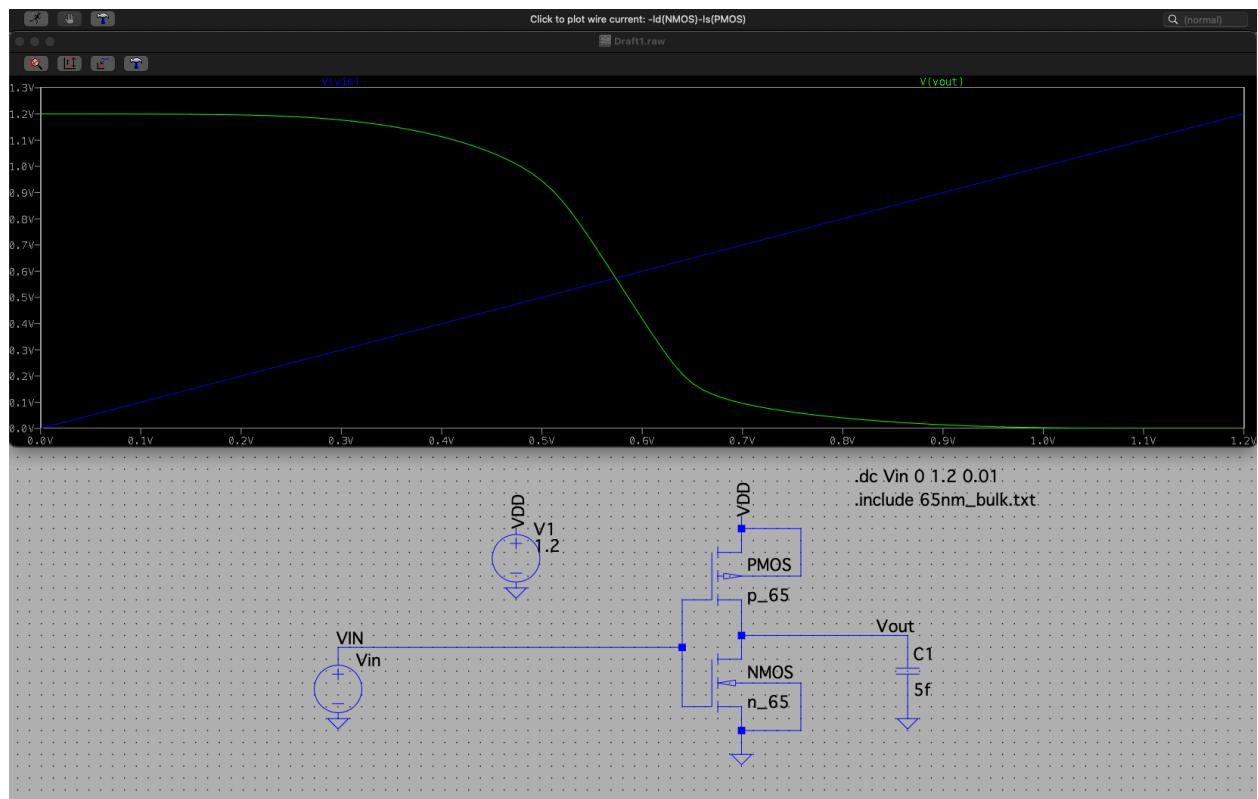
- Spice directive commands :

.tran 0 10n 0 0.01n

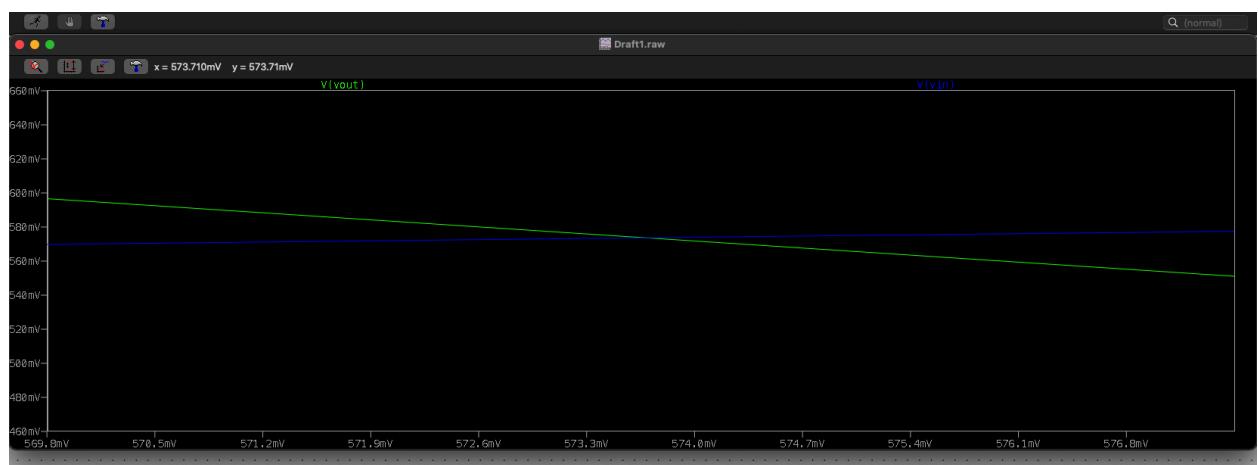
$V_{in} = \text{PULSE}(0 \ 1.2 \ 0 \ 0 \ 0 \ 0.0625n \ 0.125n)$

Assignment 1: CMOS Inverter

c) Obtain DC transfer characteristics of the inverter, obtain the trip point of the inverter.



DC transfer characteristics

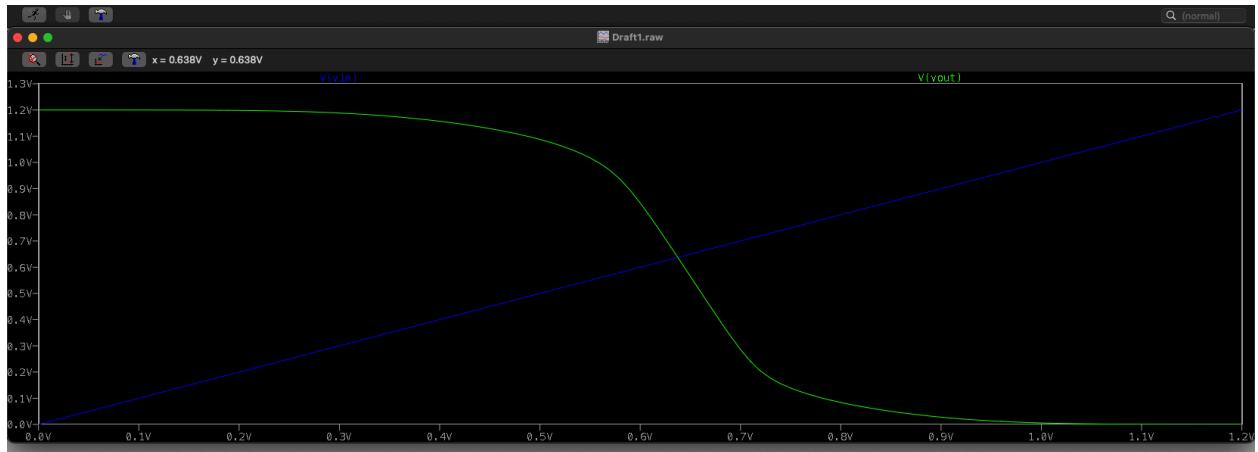


Trip point :573.71mV

Assignment 1: CMOS Inverter

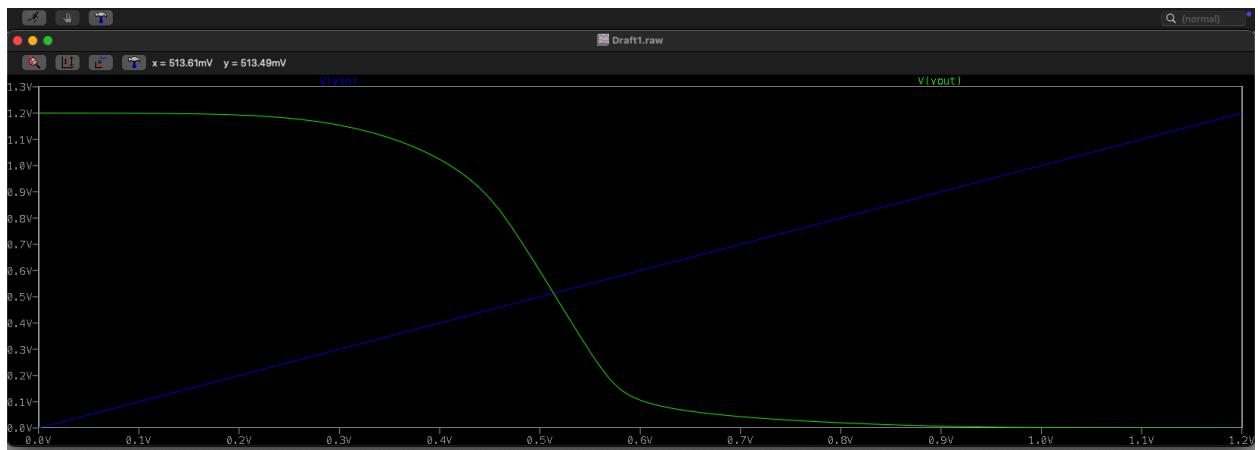
d) Observe the effect of doubling PMOS and NMOS (one by one), on the trip point in the transfer characteristics.

- Doubling PMOS width(2um) :



Trip point shifts to $\sim 638\text{mV}$

- Doubling NMOS width(1um) :



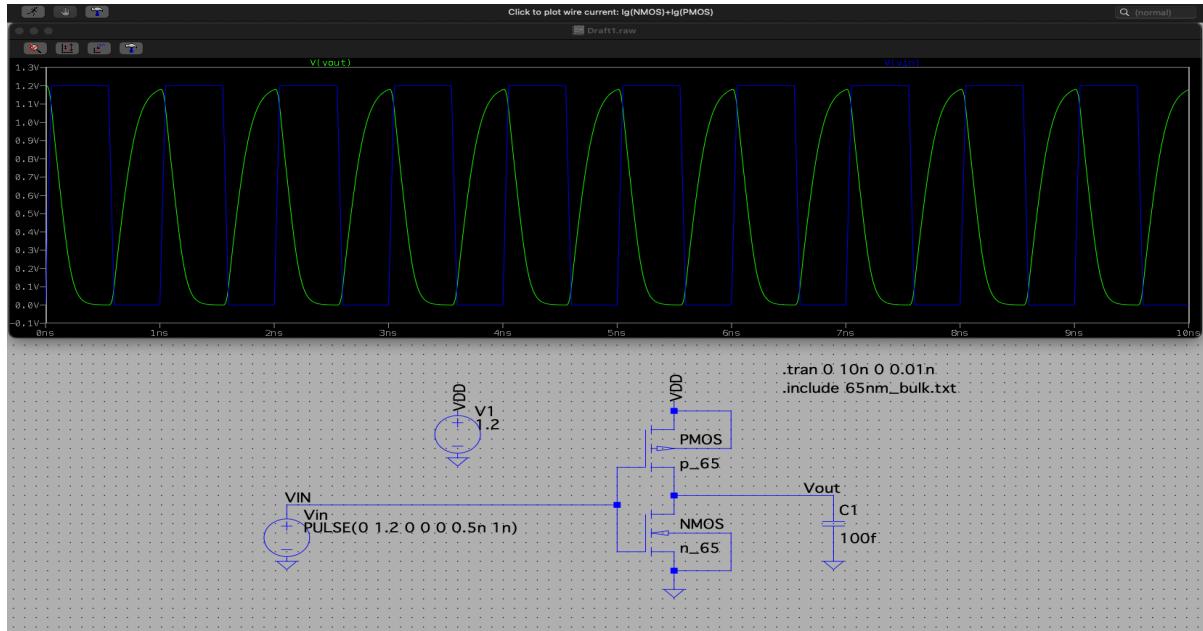
Trip point shifts to $\sim 513.49\text{mV}$

- Spice directive commands :

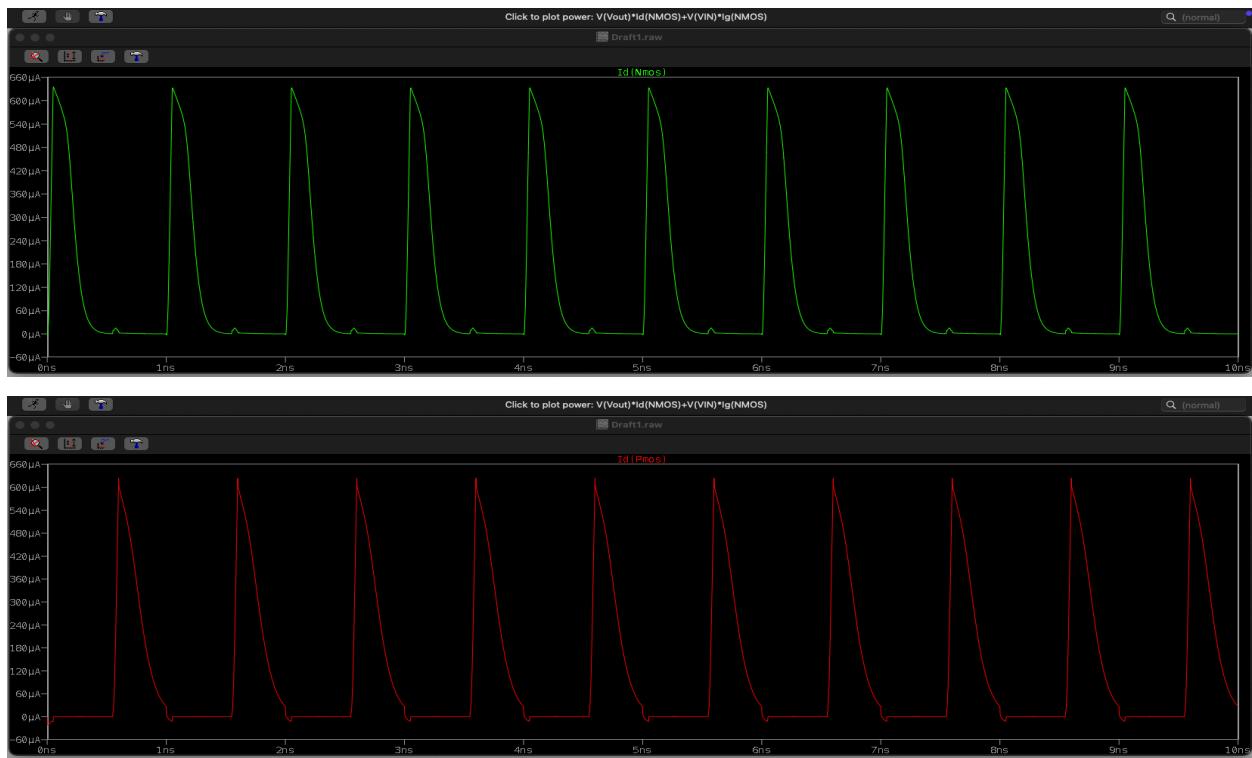
.dc Vin 0 1.2 0.01

Assignment 1: CMOS Inverter

e) For the original inverter in 1.a , increase the load capacitor to 100fF. Check the output waveform for 1G Hz clock input signal.



Input Voltage (blue) and Output Voltage (green)

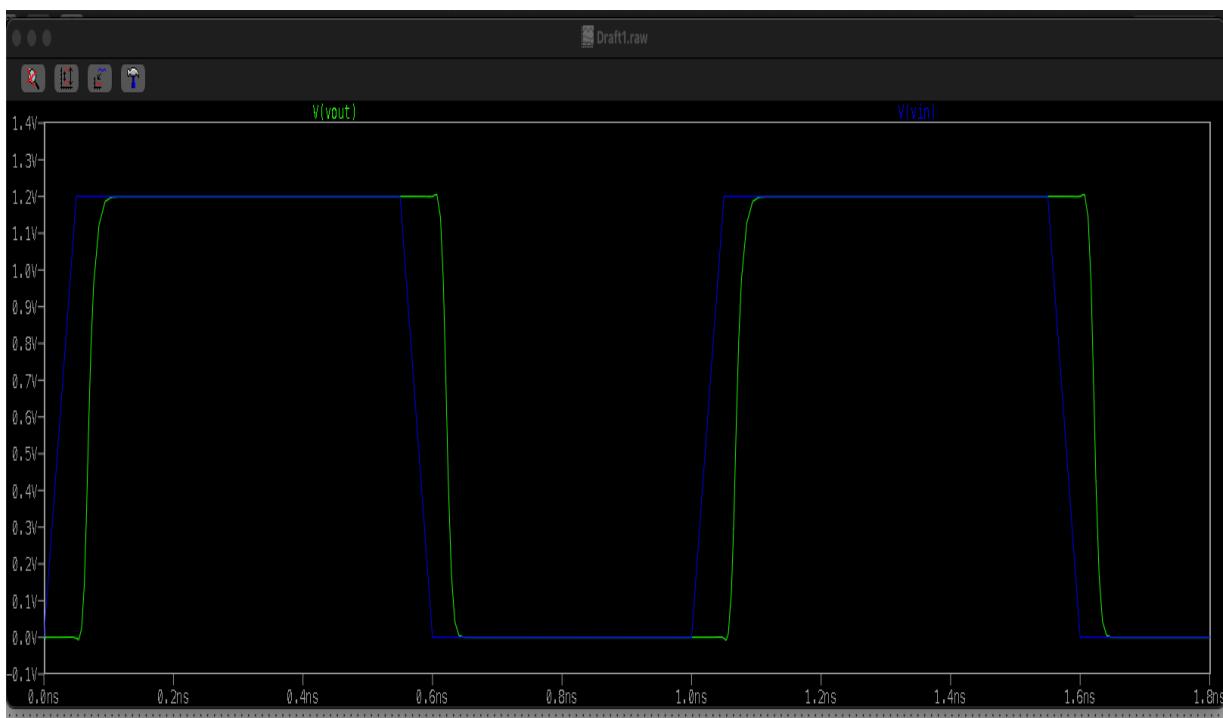
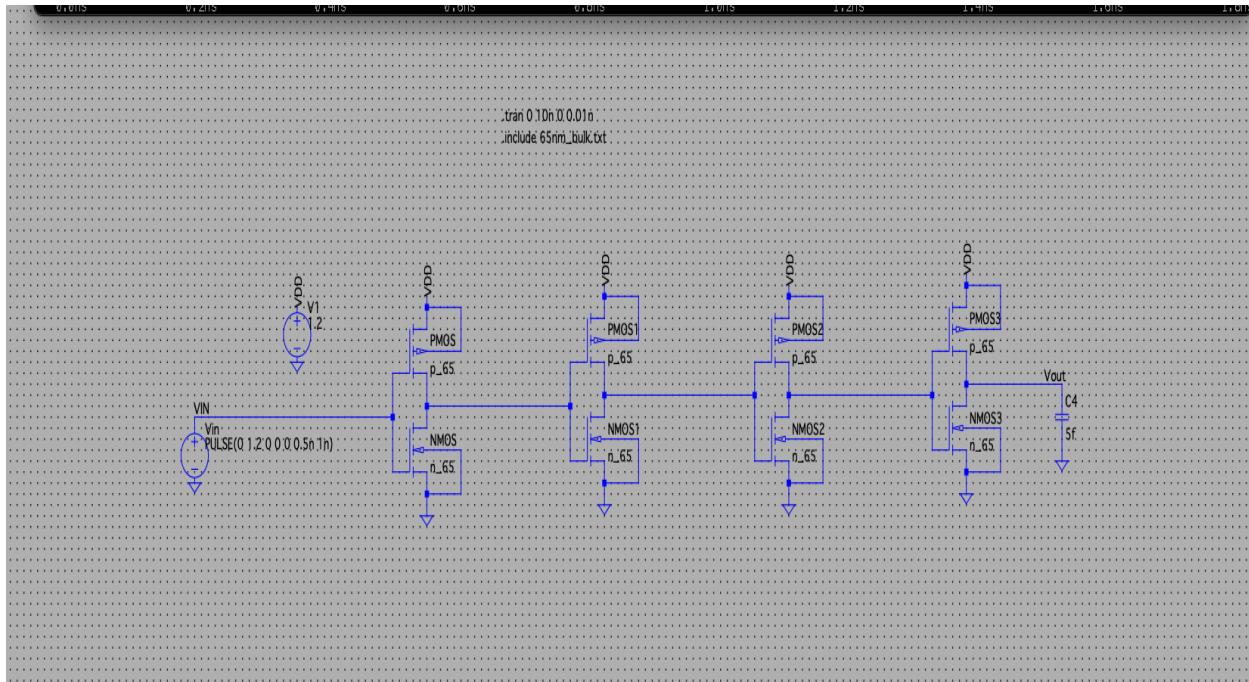


$I_d(PMOS,red)$ and $I_d(NMOS,green)$

Assignment 1: CMOS Inverter

f) Insert two inverters of 3x and 9x widths, between the 1st inverter and the 2nd inverter, check the output waveform.

Circuit Diagram:



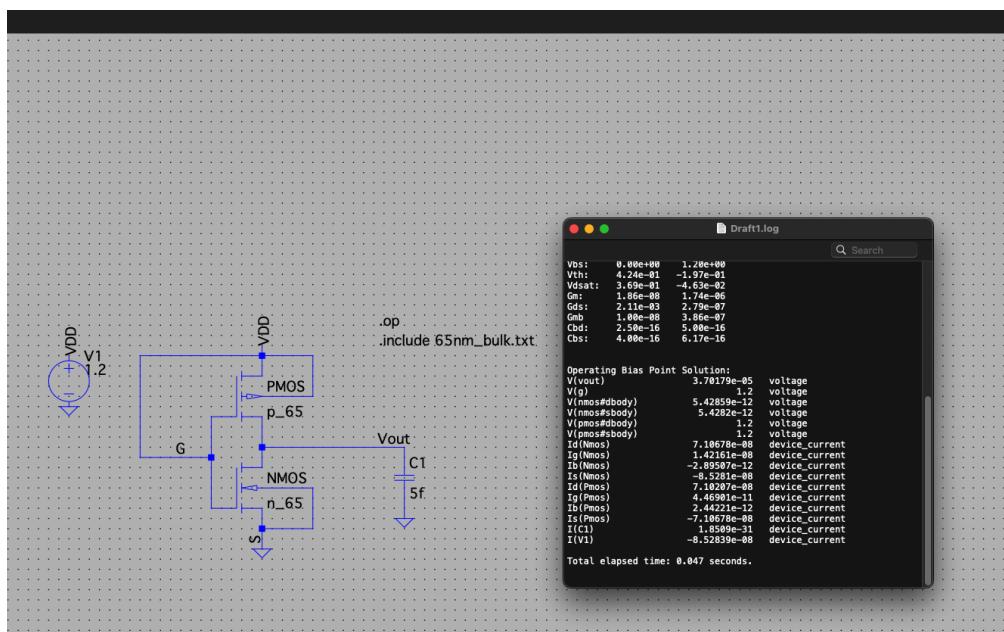
Input Voltage (blue) and Output Voltage (green)

Assignment 1: CMOS Inverter

g)For the inverter in 1.a, check the gate leakage current and source to drain leakage current for Vin = Vdd and Vin = 0V

- Vin=Vdd:

In this case, the PMOS is off and we only have leakage currents flowing through it.



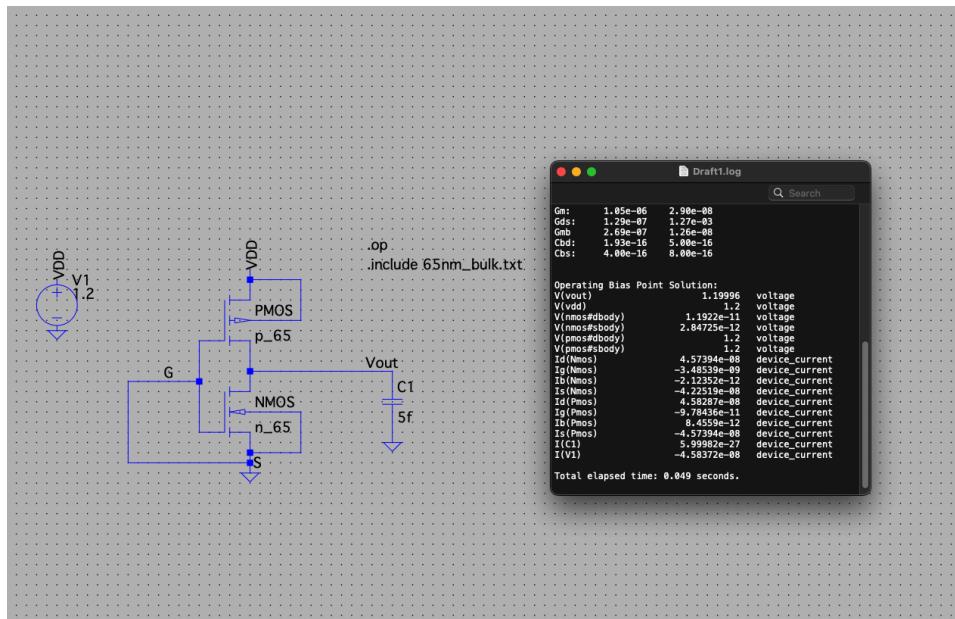
| | | |
|--------------|--------------|---|
| $Id(Pmos)$ = | 7.10207e-08 | PMOS is OFF \rightarrow leakage current |
| $Ig(Pmos)$ = | 4.46901e-11 | Very low gate leakage |
| $Ib(Pmos)$ = | 2.44221e-12 | device_current |
| $Is(Pmos)$ = | -7.10678e-08 | Balances drain current |

- Spice directive commands : .op

Assignment 1: CMOS Inverter

- V_{in}=0

In this case, the NMOS is off and we only have leakage currents flowing through it.



$I_d(\text{Nmos}) = 4.57394\text{e-}08$ (Drain leakage in OFF NMOS → subthreshold leakage)

$I_g(\text{Nmos}) = -3.48539\text{e-}09$ (Gate leakage)

$I_s(\text{Nmos}) = -2.12352\text{e-}12$ (Balances I_d (as expected))

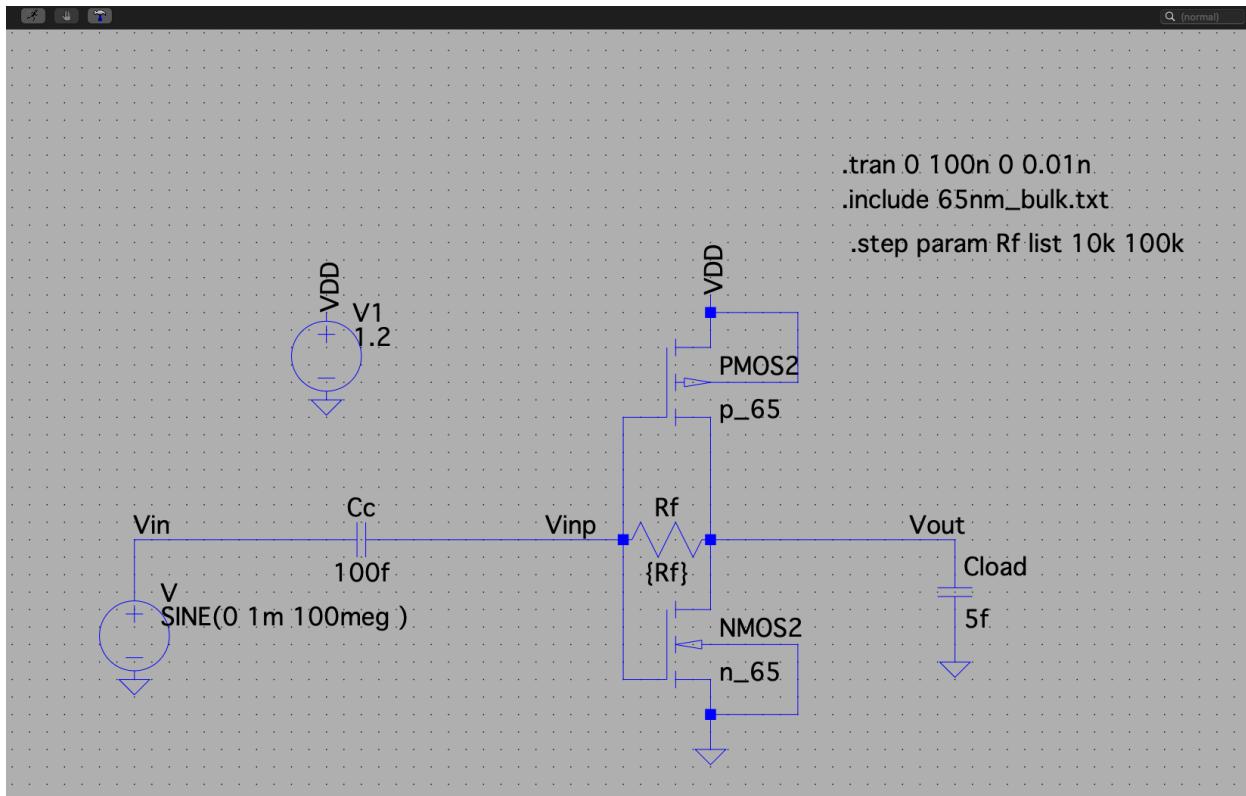
$I_b(\text{Nmos}) = -4.22519\text{e-}08$ device_current

- Spice directive commands : .op

Assignment 1: CMOS Inverter

2. Simulate CMOS inverter as amplifier. Use $W_p = 5\mu$, $W_n = 2.5\mu$, $L = 0.3\mu$, $C_{load} = 5fF$.

Circuit Diagram



Task: Use transient simulation with 1mV input, to obtain output signal with two different values of $R_f = 10k$, $R_f = 100k$.

Also obtain the AC transfer function.

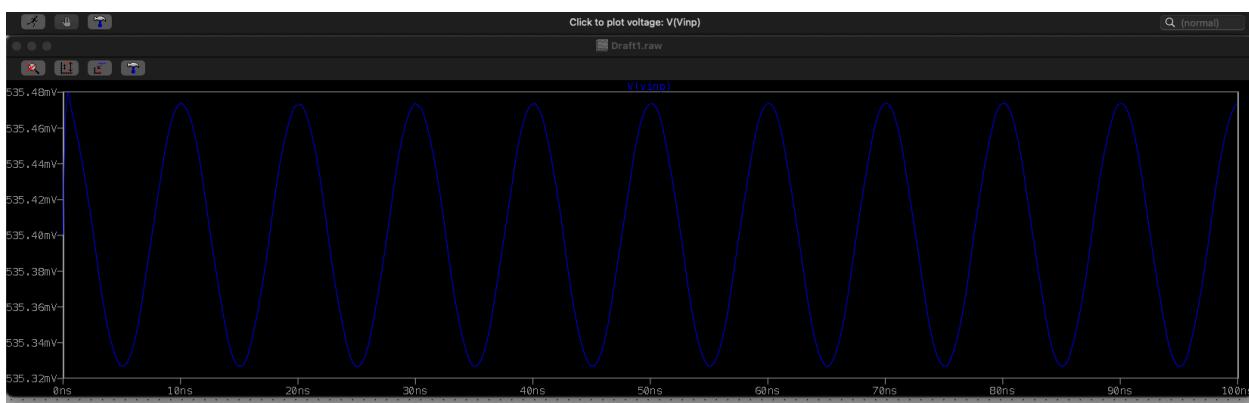
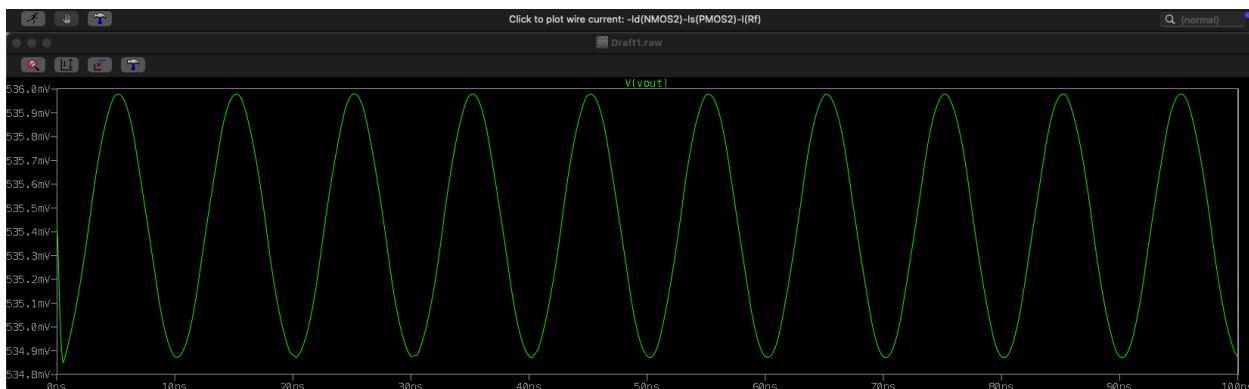
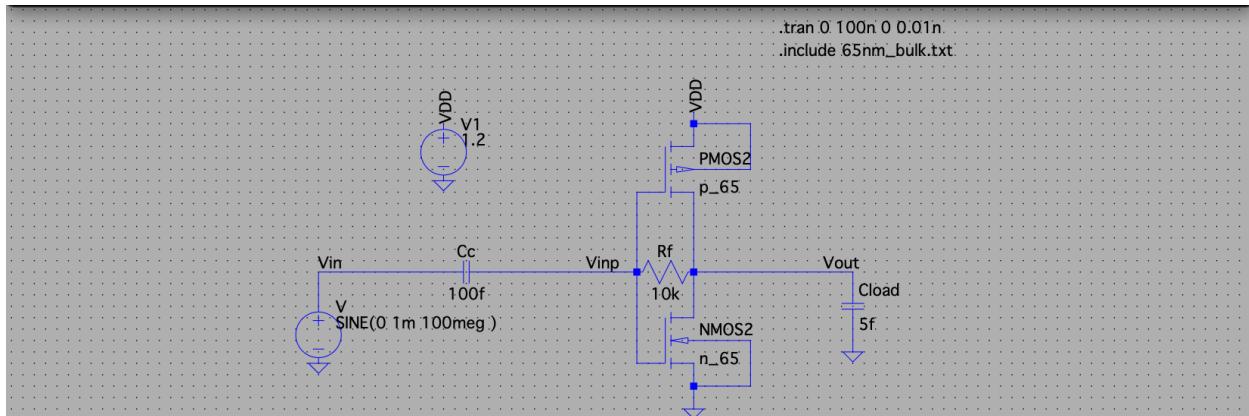
Repeat the experiment with $L = 1\mu$.

Assume coupling cap to the input source as $100fF$.

Assignment 1: CMOS Inverter

a)(i) With L=0.3um and Rf=10K ohm

- Circuit diagram

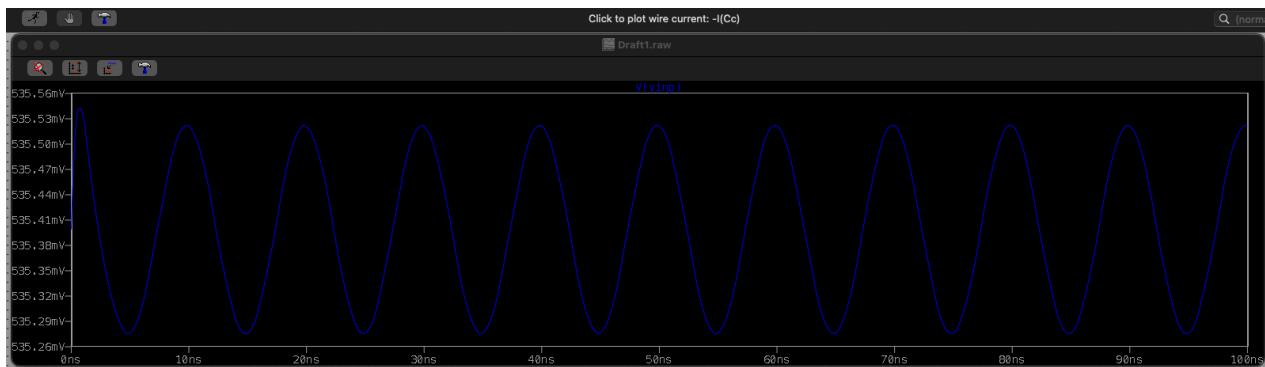
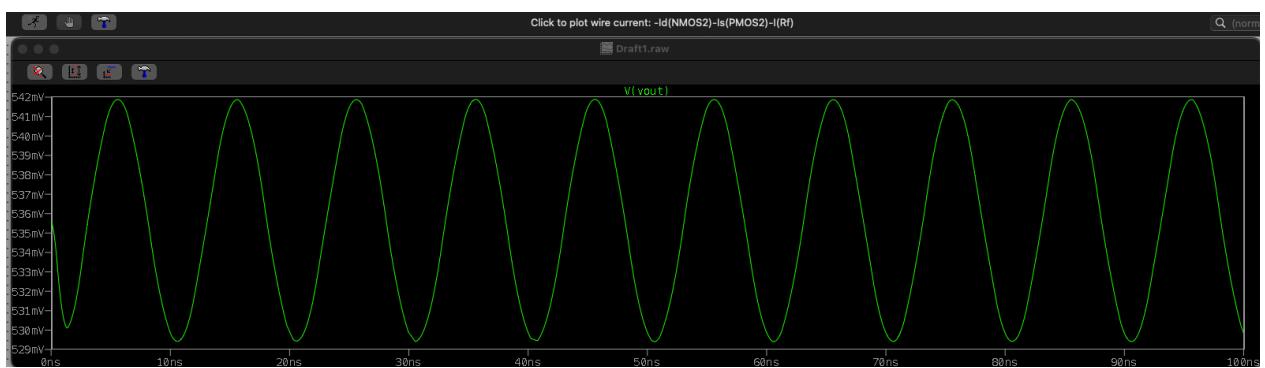
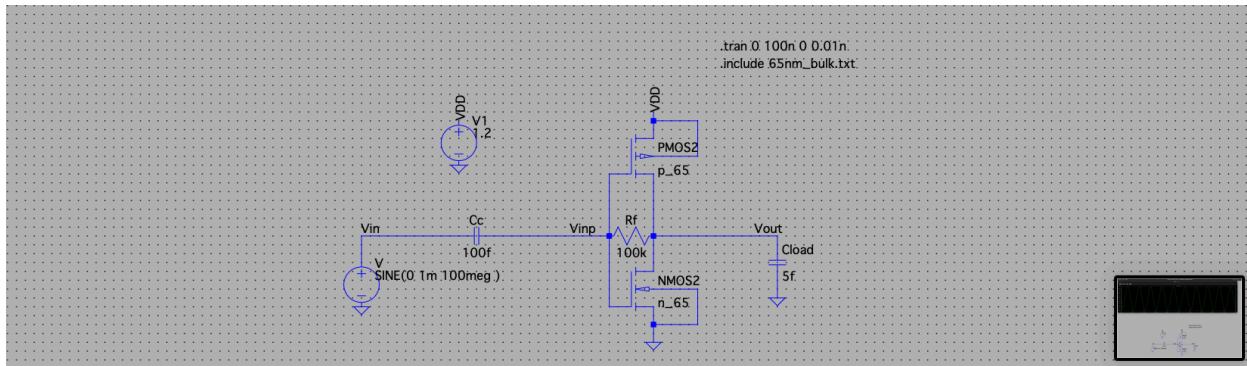


Input voltage(Vin,blue) and output voltage(Vout,green)

Assignment 1: CMOS Inverter

a)(ii) With L=0.3um and Rf=100K ohm

- Circuit diagram

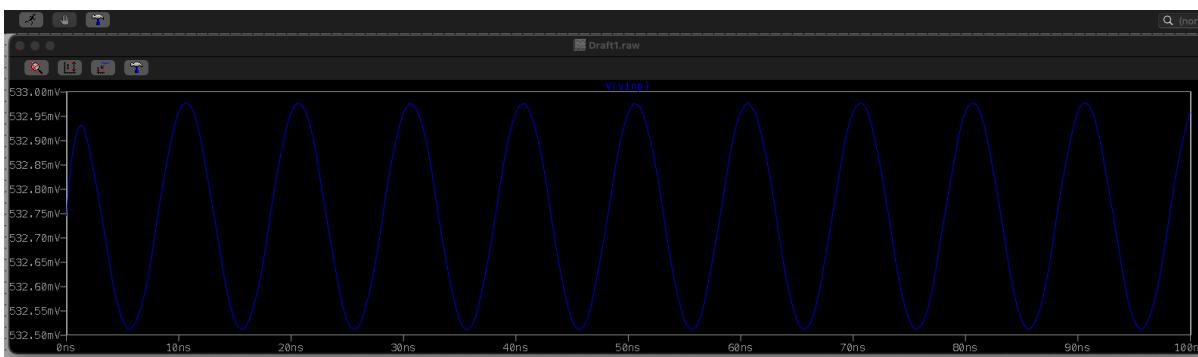
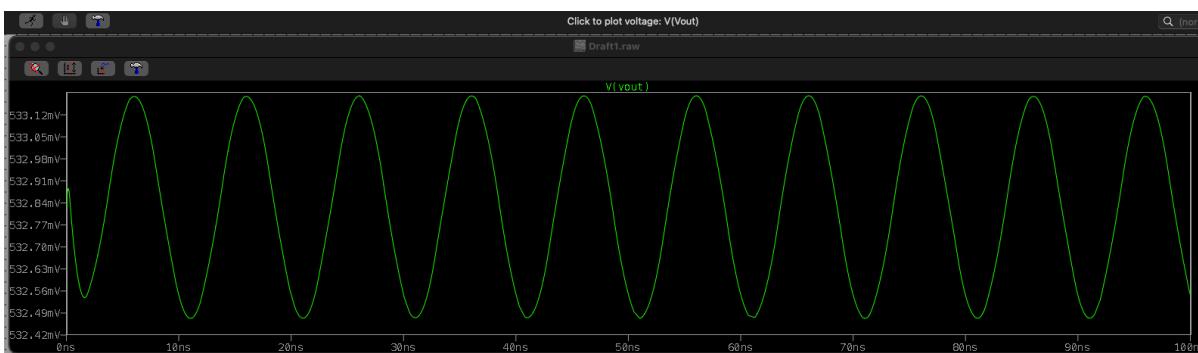
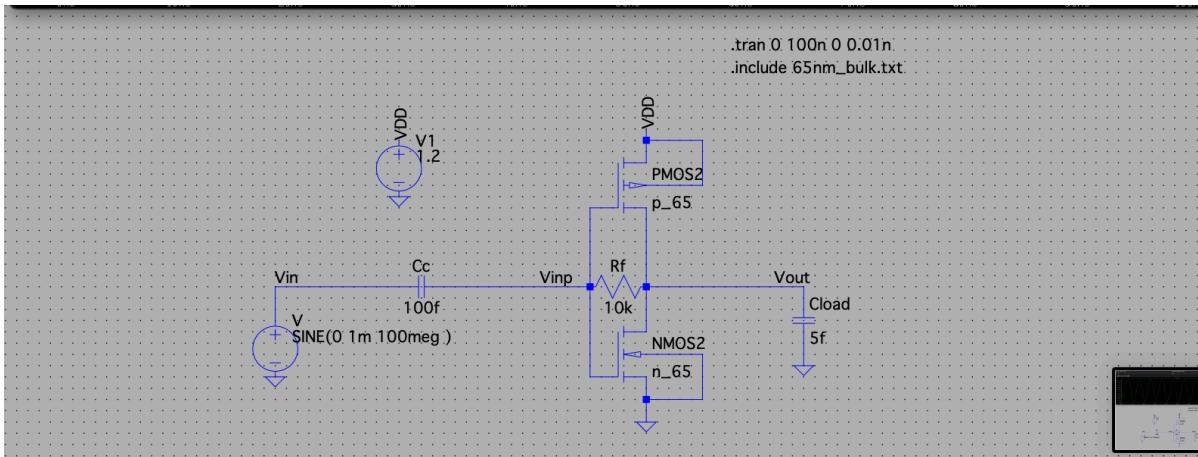


Input voltage(Vin,blue) and output voltage(Vout,green)

Assignment 1: CMOS Inverter

b)(i) With L=1um and Rf=10K ohm

- Circuit diagram

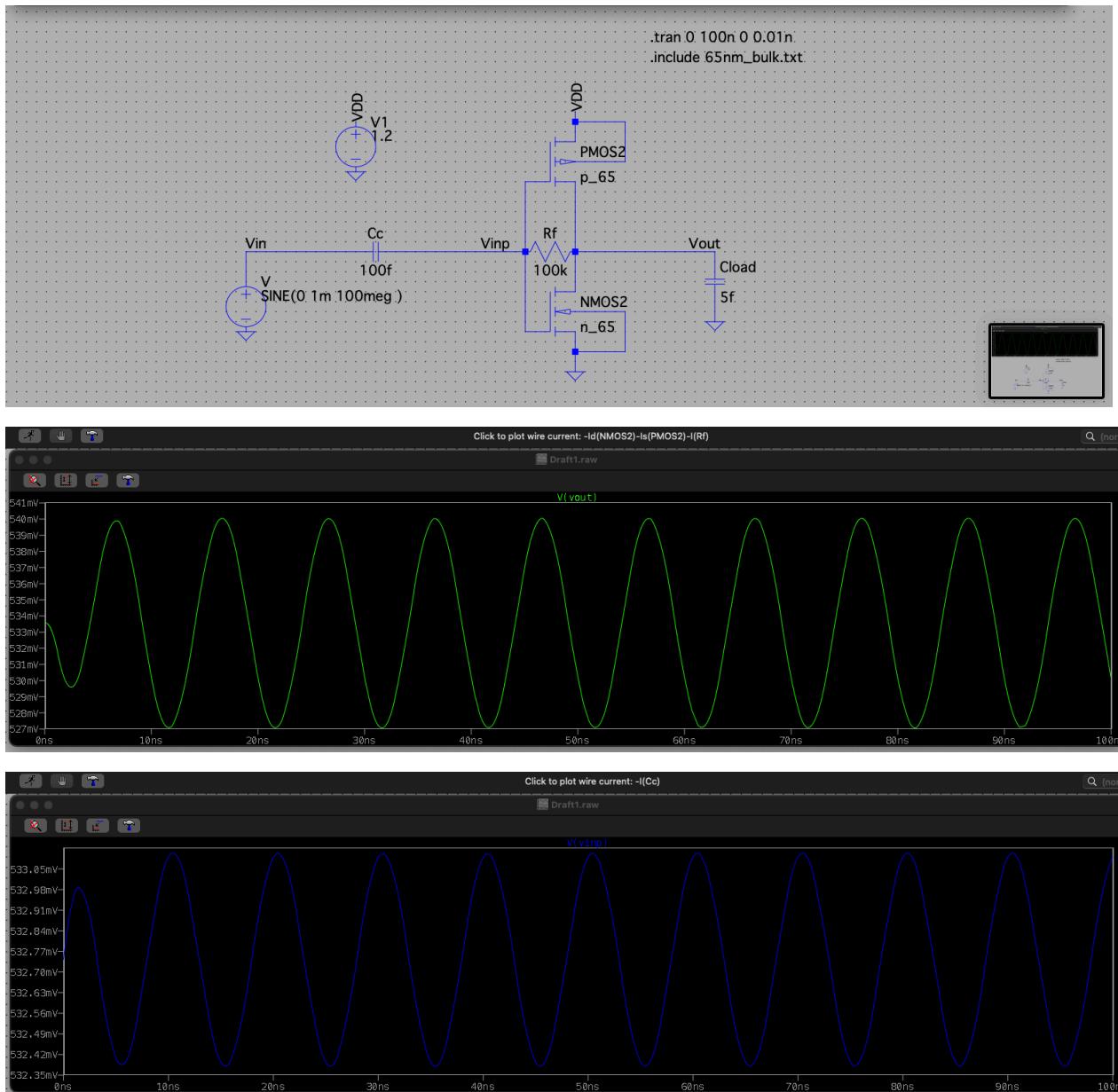


Input voltage(Vin,blue) and output voltage(Vout,green)

Assignment 1: CMOS Inverter

b)(ii) With L=1um and Rf=100K ohm

- Circuit diagram



Input voltage(V_{in} ,blue) and output voltage(V_{out} ,green)

Assignment 1: CMOS Inverter

- Discussion:

- 1.(a) Inverter switches properly at 1GHz; PMOS/NMOS alternate conduction.
- (b) Output degrades at higher frequencies due to insufficient charging time.
- (c) Trip point ($V_{in} = V_{out}$) marks inverter switching threshold.
- (d) Increasing PMOS strength shifts the trip point right; increasing NMOS shifts it left.
- (e) Increasing load capacitance slows down transitions due to higher delay.
- (f) Inverter chain with 3x and 9x sizes improves driving strength and restores signal integrity.

3x Inverter : PMOS W=3u L=65n, NMOS W=1.5u L=65n

9x Inverter : PMOS W=9u L=65n, NMOS W=4.5u L=65n

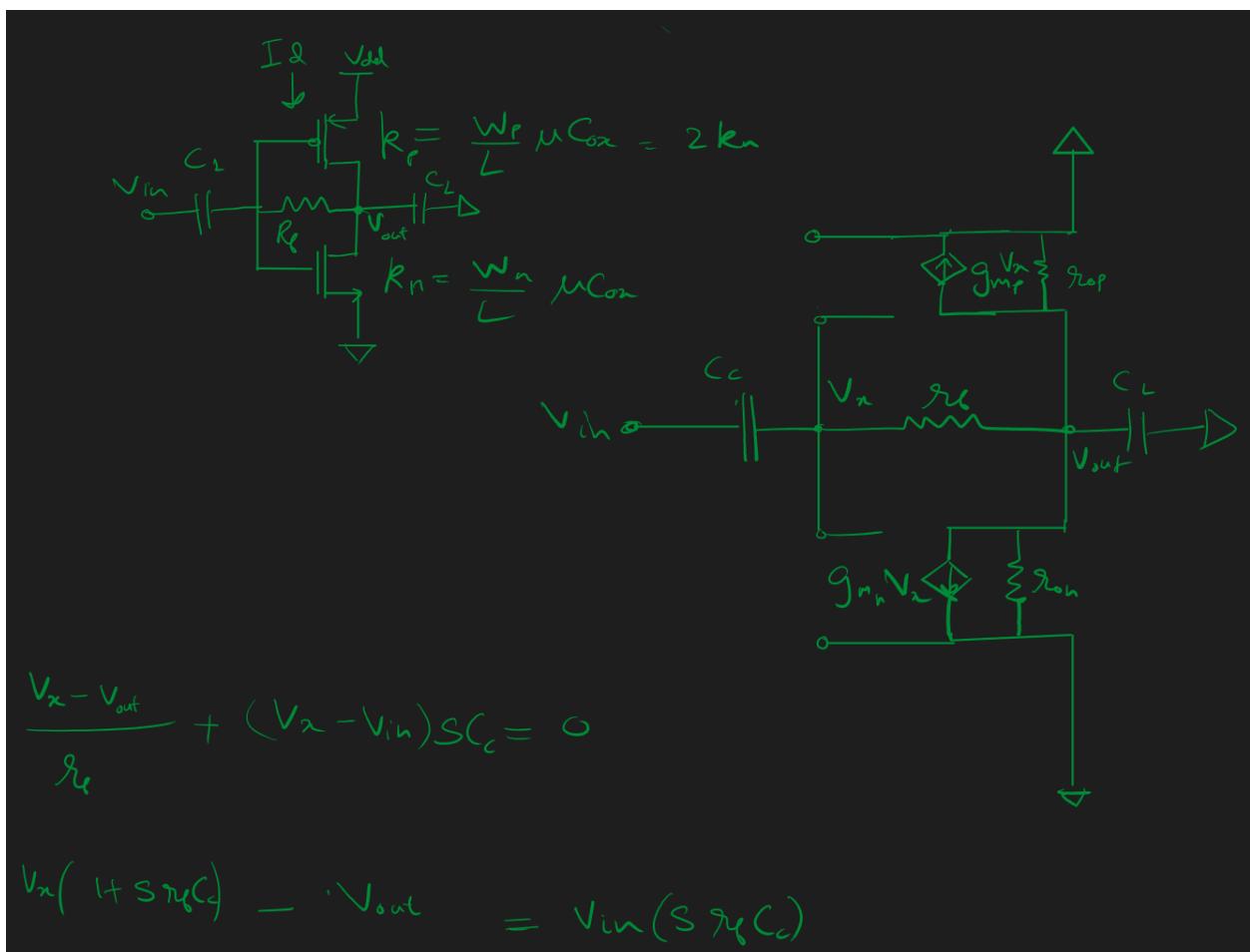
- (g) Leakage currents are small but noticeable; increase with scaling.

- When $V_{in} = V_{dd}$, PMOS is off and we have leakage currents flowing through it.
- When $V_{in} = 0$, NMOS is off and we have leakage currents flowing through it.

Assignment 1: CMOS Inverter

- Discussion:

2. The CMOS inverter, when biased at its switching threshold using a feedback resistor R_f , functions as a high-gain analog amplifier for small input signals. The gain and bandwidth are influenced by R_f , the input coupling capacitor C_c , and transistor sizing. Increasing channel length reduces gm but improves output resistance, affecting overall gain and frequency response.



Assignment 1: CMOS Inverter

$$V_{out} SC_L + \frac{V_{out} - V_n}{r_L} + \frac{V_{out}}{r_{in} || r_{out}} + V_n (g_{mp} + g_{mn}) = 0$$

$\underbrace{g_{mp} + g_{mn}}_{G_m}$

$$V_{out} SC_L + \frac{V_{out}}{r_{in} || r_{out} || r_{op}} = V_n \left(\frac{G_m r_L + 1}{r_L} \right)$$

$$V_{out} \left(\frac{SC_L R_{\Sigma} + 1}{R_{\Sigma}} \right) = V_n \left(\frac{G_m r_L + 1}{r_L} \right) \Rightarrow V_{out} \left(\frac{SC_L R_{\Sigma} + 1}{G_m r_L + 1} \right) \cdot \frac{r_L}{R_{\Sigma}} = V_n$$

$$V_{out} \left(\frac{SC_L R_{\Sigma} + 1}{G_m r_L + 1} \right) \left(1 + S r_L C_c \right) \frac{r_L}{R_{\Sigma}} - V_{out} = V_{in} (S r_L C_c)$$

$$V_{out} \left(\frac{(SC_L R_{\Sigma} + 1)(1 + S r_L C_c) r_L}{(G_m r_L + 1) R_{\Sigma}} - 1 \right) = V_{in} (S r_L C_c)$$

$$V_{out} = V_{in} \frac{S r_L C_c (G_m r_L + 1) (R_{\Sigma})}{(SC_L R_{\Sigma} + 1)(1 + S r_L C_c) r_L - G_m r_L R_{\Sigma} - R_{\Sigma}}$$