Custom Binary Memory Array (Verilog + Falstad)

Individual Project - IIT Kharagpur

Overview:

This project involves the design and simulation of a binary memory array using gate-level logic and JK flip-flop-based binary cells. The system mimics a simple SRAM-like memory but is built entirely from custom logic for educational and demonstration purposes.

Key Contributions:

- Developed modular RTL in Verilog for a compact multi-bit memory array using binary memory cells based on JK flip-flop behavior.
- Implemented hierarchical components including a 2:4 decoder, memory rows, and read/write control logic with clocked operation.
- Simulated the complete gate-level memory design in Falstad using logic gates and flip-flops to visualize internal signal behavior.

Implementation Structure:

- binary_cell: Core memory bit cell designed using JK flip-flop logic.
- memory_row: A 3-bit memory row constructed from three binary_cell modules.
- decoder_2to4: Selects the active memory row based on 2-bit input.
- memory_4x3: Top-level module integrating decoder, memory rows, and data I/O routing logic.
- testbench: Validates functionality by simulating write and read operations across the memory.

Tools Used:

- Verilog HDL for RTL modeling and simulation.
- Falstad logic simulator for visual gate-level design.
- GTKWave/ModelSim for waveform and signal analysis.

Project Repository:

GitHub: https://github.com/krrish1310/Custom-Binary-Memory-Array