VLSI Summer School Project Documentation 2025

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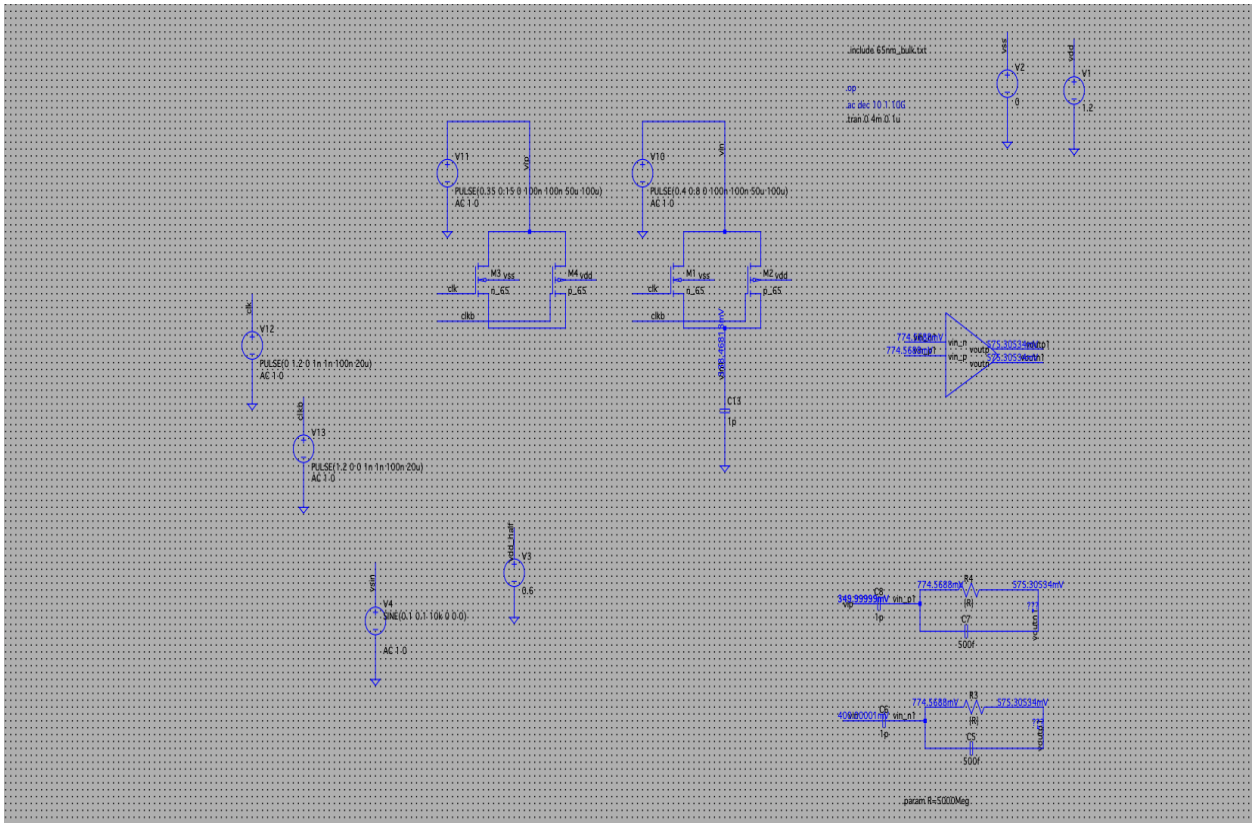
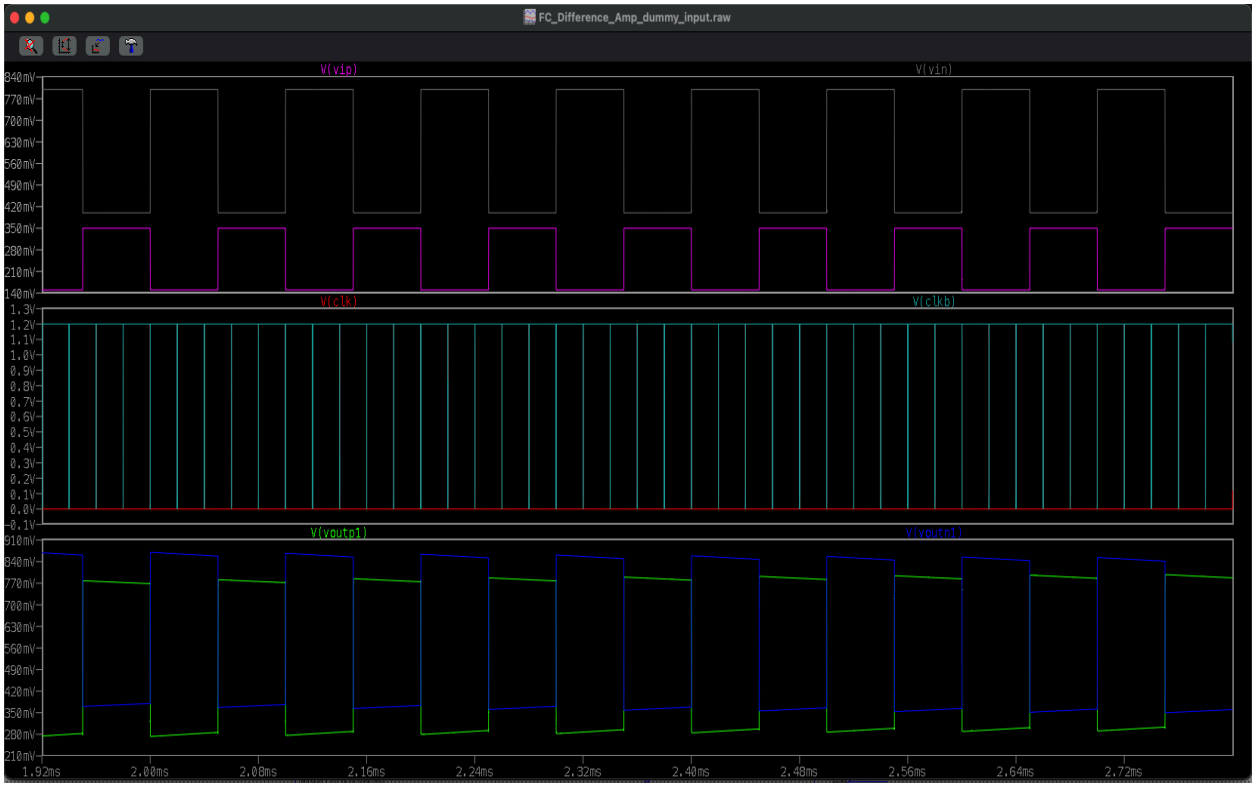
Assignment 7: FC_DIFF_DUMMY

- ## Circuit Diagram:



Assignment 7: FC_DIFF_DUMMY

- Transient analysis:



Input signals :

Vip : PULSE(0.35 0.15 0 100n 100n 50u 100u)

Vin : PULSE(0.4 0.8 0 100n 100n 50u 100u)

Clk signal : PULSE(0 1.2 0 1n 1n 100n 20u)

Output signals :

Vout_p1 : ranging from 300mV TO 800 mV

Vout_n1 : ranging from 350mV TO 840 mV