Applications of μC - I
Topic-2. MCS - 51 Architecture

Mrs. Deepti Khimani

Department of Instrumentation Engg.
V.E.S. Institute of Technology, Mumbai

ODD SEMESTER, 2015

Table of Content

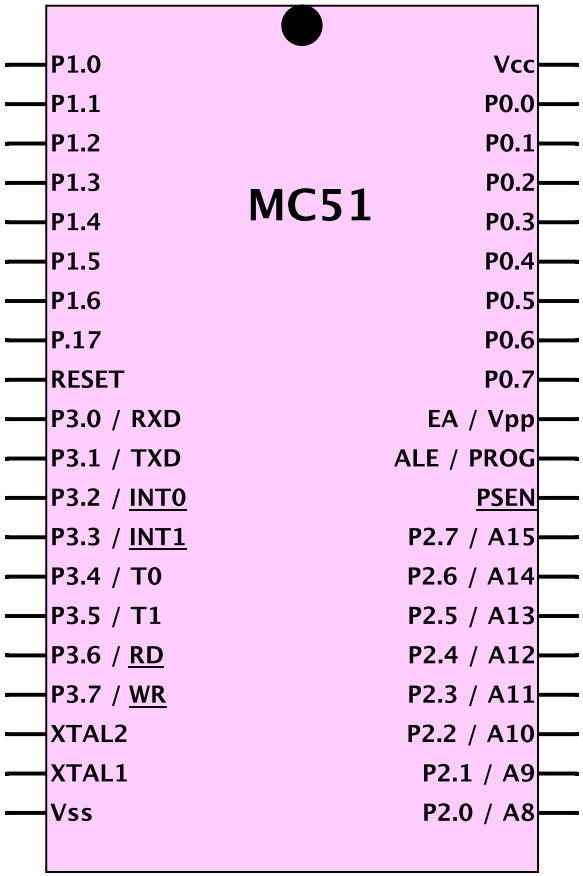
MCS-51 family of microcontrollers

- The MCS-51 family includes microcontroller variants ranging from 8031 to 8751.
- They are available in N-channel Metal Oxide Silicon (NMOS) or Complementary Metal Oxide Silicon (CMOS) construction and in various types of packages.
- A generic 8051 microcontroller has following features–
  - Up to 12 MHz operating frequency.
  - Thirty-two digital input / output pins (arranged as four 8-bit ports).
  - Internal data (RAM) memory – 128 bytes.
  - 4K bytes internal mask-programmed ROM (8051)
  - Two 16-bit timer / counters (Timer 0 and Timer 1).
  - Five interrupt sources (two external) with two priority levels.
  - One programmable, full-duplex, serial port.

- 8031 has no program memory, all programs are stored in external memory.
- 8051 has 4K $\times$ 8 bits internal mask-programmed ROM.
- 8751 has 4K $\times$ 8 bits UV-erasable EPROM.
- The 8052 had the following features–
  - Internal data (RAM) memory was increased to 256 bytes.
  - Two 8052 versions were available with different program memory options:
    - 8032-No program memory, all programs needed to be stored in external memory.
    - 8052-8K $\times$ 8 bits internal mask-programmed ROM.
  - Three 16-bit timer / counters (Timer 0, Timer 1 and Timer 2).
  - Six interrupt sources were provided (two external) with two priority levels.

- The popular Atmel 89S53 is a representative example of a modern Standard 8051. Listed here is a summary of the main features of the AT89S53:
  - Fully static operation: 0–24 MHz operating frequency.
  - Thirty-two input / output lines (arranged as four 8-bit ports).
  - Internal data (RAM) memory – 256 bytes.
  - 12 Kbytes of 'in circuit programmable' ROM.
  - Three 16-bit timers / counters (Timer 2 with up/down counter feature).
  - Nine interrupts (two external) with two priority levels.
  - Programmable watchdog timer.
  - SPI interface.
  - Low-power idle and power-down modes.
  - 4V to 6V operating range.

MCS-51 PIN diagram



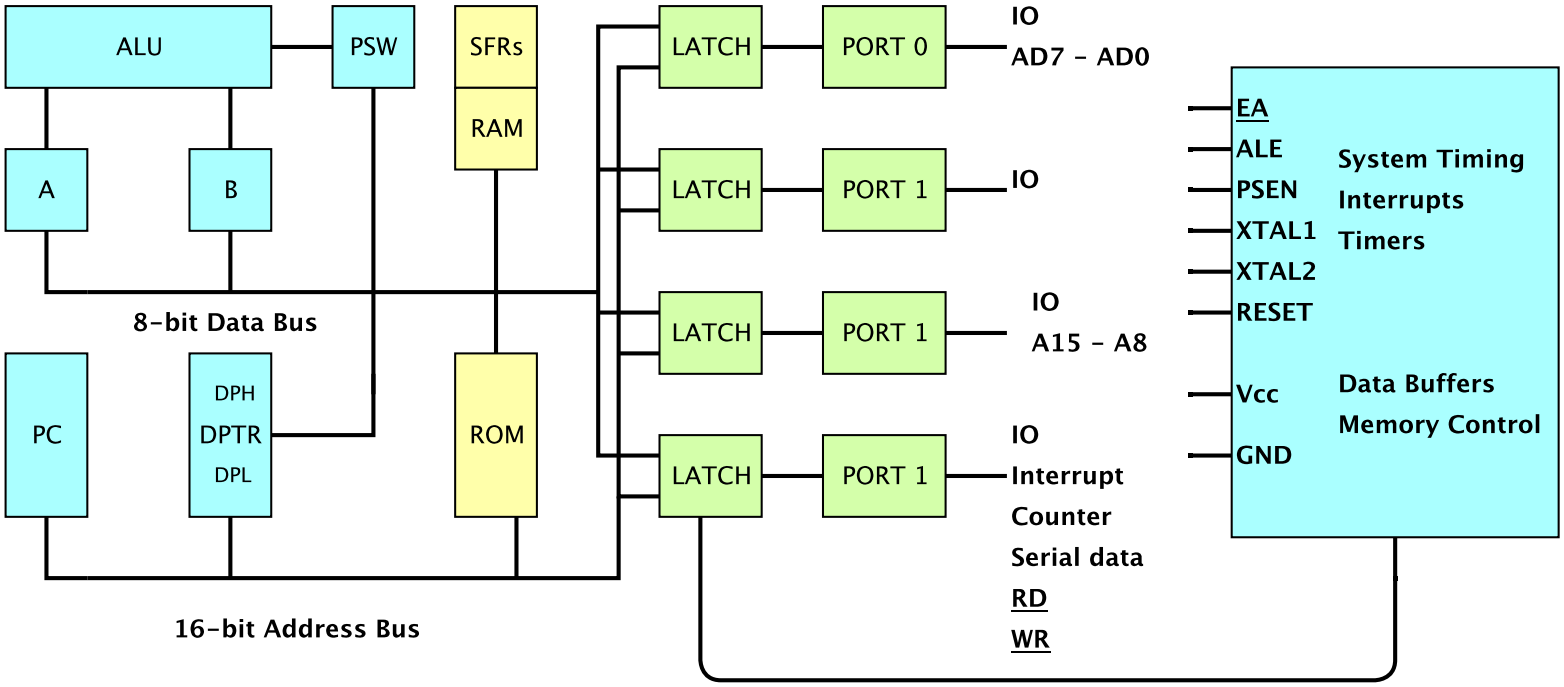
PIN diagram of 8051 microcontroller

Note that– In 8052, pins P1.0 and P1.1 have additional functionality of Timer 2 external input and Timer 2 external reload/capture.

MCS-51 architecture

The 8051 architecture consists of following features–

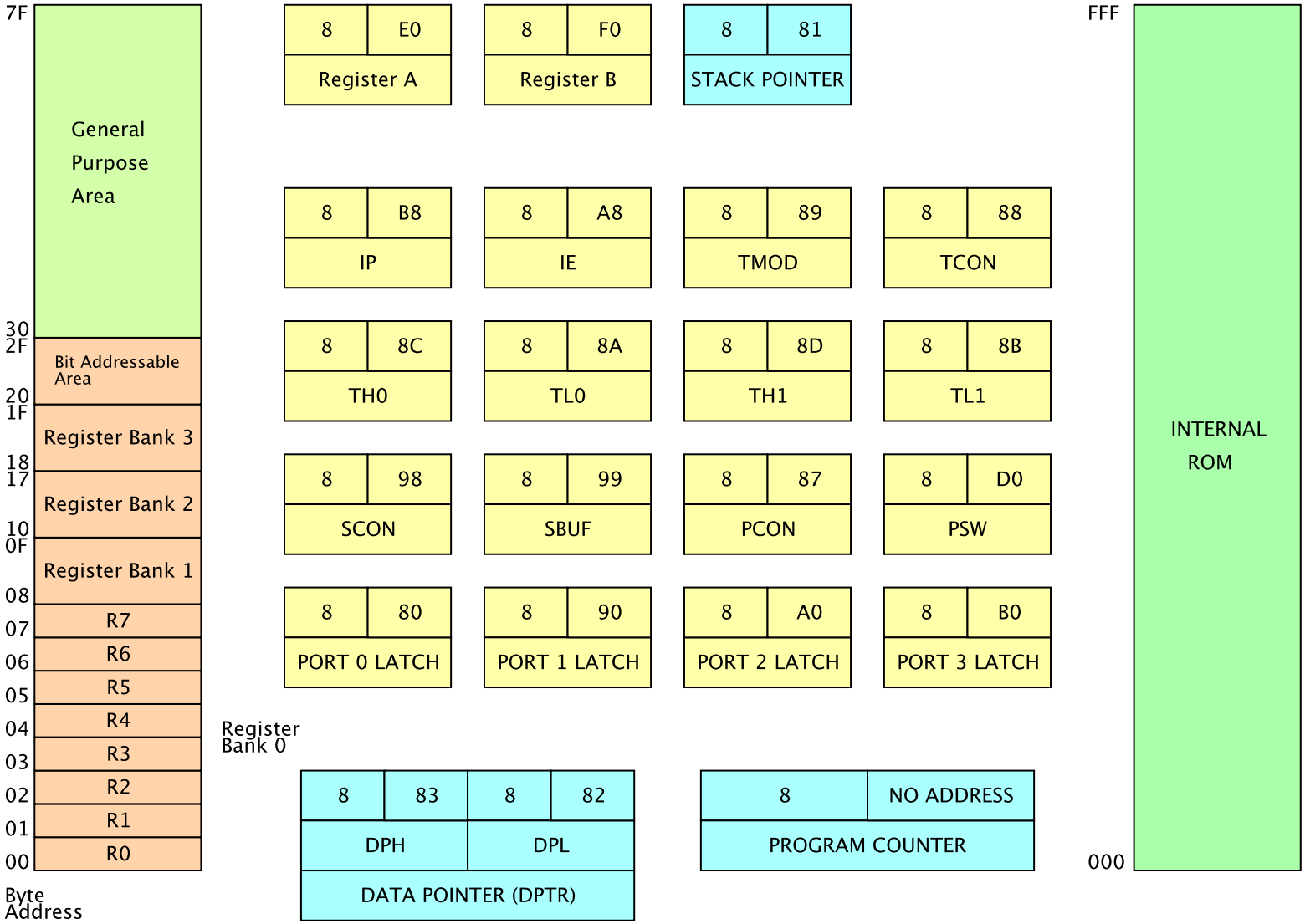
- 8-bit CPU with registers A (Accumulator) and B.
- 8-bit program status word (PSW).
- 16-bit program counter (PC) and data Pointer (DPTR). DPTR registers can be accessed separately for lower byte (DPL) and higher byte (DPH).
- 8-bit stack pointer (SP).
- Internal ROM 4K bytes.
- 128 bytes of RAM.



Block diagram of 8051 microcontroller

- 32 I/O pins are arranged as four 8-bit ports: P0-P3.
- Two 16-bit time/counters: T0 and T1.
- Full duplex serial data receiver/transmitter: SBUF
- Control regiters: TCON, TMOD, SCON, PCON, IP and IE.
- Two external and three internal interrupt sources.
- Oscillator and Clock circuits.

Programming Model of 8051

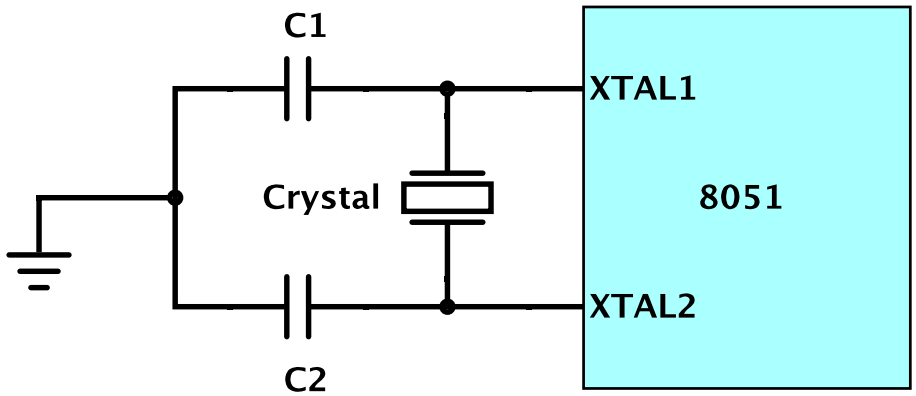


Programming model of 8051 microcontroller

- Programming model of 8051 represents a collection of 8 and 16-bit registers and 8-bit memory locations that can be made to operate using software instructions.
- Most of the registers have specific functions and they are identified by unique symbols such as A (Accumulator), SCON (serial control), TH0 (timer - 0 higher byte), PC (program counter) etc.
- Each register, except the program counter, has an internal 8-bit address assigned to it.
- Some of the registers such as A, B, IP, IE, TCON, SCON, PSW and all port latches are bit addressable.

MCS-51 clock and oscillator circuit

- This circuit is the 'heartbeat' of the system and is crucial for the correct operation.
- If the oscillator fails, the system will not function at all; if the oscillator runs irregularly, any timing calculations performed by the system will be inaccurate.



Oscillator circuit for 8051 microcontroller

- A resonant circuit is connected to XTAL1 and XTAL2 pins to form an oscillator.
- A typical resonant circuit employs the quartz crystal and capacitors.
- Typically, the start up time for the oscillators is 0.1 to 10 ms.
- If the start of the oscillator is delayed, then the reset cycle may be completed before the oscillation begins. If this happens, the chip will not be reset.

- The manufacturer specifies the minimum and maximum clock frequency range for the operation of microcontroller.
- If the clock frequency is less than specified minimum frequency, the data in dynamic memory may lost.
- The most important parameter that determines the speed of microcontroller is clock frequency. However, if the frequency of the oscillator selected is higher then–
  - More supply current is needed because in modern microcontrollers (CMOS based)

$$I_{cc} \propto f_{crystal}$$

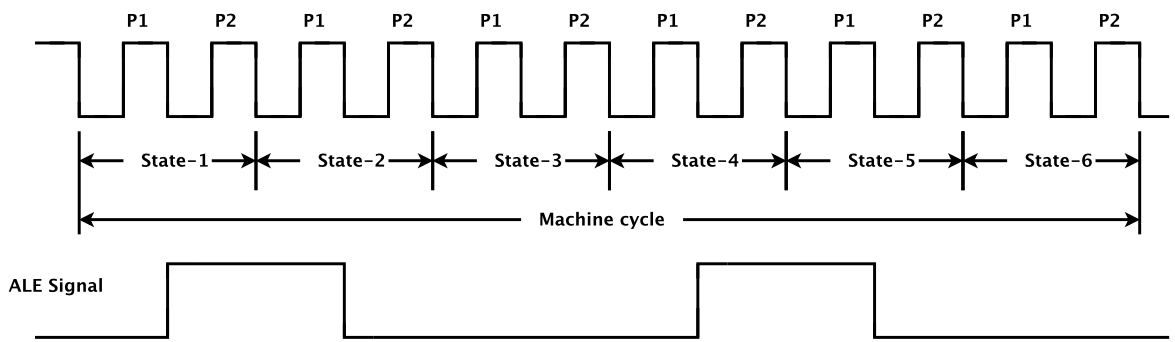
  - The electromagnetic interference (EMI) generated by a circuit increases with clock frequency.

Timings in the 8051

- Any instruction may require to 1, 2 or 4 machine cycles for the execution.
- Each machine cycle consists of 6 states and each state consists of 2 pulses (periods) of oscillator.
- So time taken by processor to execute any instruction can be given by

$$T_{instruction} = \frac{N * 12}{f_{crystal}}$$

Where, N is number of machine cycles required for the instruction to be executed as specified by manufacturer.



Oscillator circuit for 8051 microcontroller

Memory Pointers: Program Counter and Data Pointer

- Program Counter (PC)
  - Used to point the address of the instruction byte stored in internal ROM (0000h-0FFFh) or external ROM (1000h-FFFFh). In case of 8031/32 all external.
  - It holds the address of the instruction byte to be fetched, and is incremented after the instruction is fetched.
  - Upon reset PC holds 0000h.
  - It is the only register that does not have internal address. Contents of PC can be altered by certain instructions only.
- Data Pointer (DPTR)
  - It is used to furnish the internal and external code access and external data access.
  - DPTR is under the control of program instructions and can be specified by its 16-bit name DPTR or each individual byte name DPH and DPL.
  - DPTR does not have single internal address, however DPH and DPL are each assigned an internal address.

CPU registers: A & B

- The 8051 has 34 general purpose registers– A, B and 32 registers in four banks.
- A & B are part of the mathematical core of CPU, called ALU.
- Register A, called as accumulator participates in all arithmetic operations such as addition, subtraction, multiplication, division and in boolean bit manipulations (logical operations).
- Register B works with register A in multiplication and division operations only. Otherwise it is used just to store a data byte like any other general purpose register.

Flags and program status word (PSW)

- Flags are individual flip-flops provided to store the results of certain program instructions.
- They are also used by some instructions to test the condition and make the decision.
- There are 4 math flags and 3 general purpose flags, grouped together in program status word (PSW) and power control (PCON) registers.
- Math flags include carry (CY), auxiliary carry (AC), overflow (OV) and parity (P) are all in PSW.
- Three general purpose flags are, F0 in PSW and GF1 and GF0 in PCON register.
- Besides flags, PSW contains RS1 and RS0 bits and they are used to select the any one of the register bank.

CY	AC	F0	RS1	RS0	OV	–	P
7	6	5	4	3	2	1	0

The 8051 program status word (PSW)

Table: Function of bits in PSW

Bit	Symbol	Function
7	CY	Used in arithmetic, JUMP, ROTATE and BOOLEAN instructions.
6	AC	Auxiliary carry, used for BCD arithmetic.
5	F0	User flag 0 .
4, 3	RS1,RS0	*RS*1 *RS*0 0 0 Select register bank-0 0 1 Select register bank-1 1 0 Select register bank-2 1 1 Select register bank-3
2	OV	Overflow flag, used in arithmetic instructions.
1	-	Reserved for future use.
0	P	Parity flag, shows parity of register A. OV=1 is odd parity.

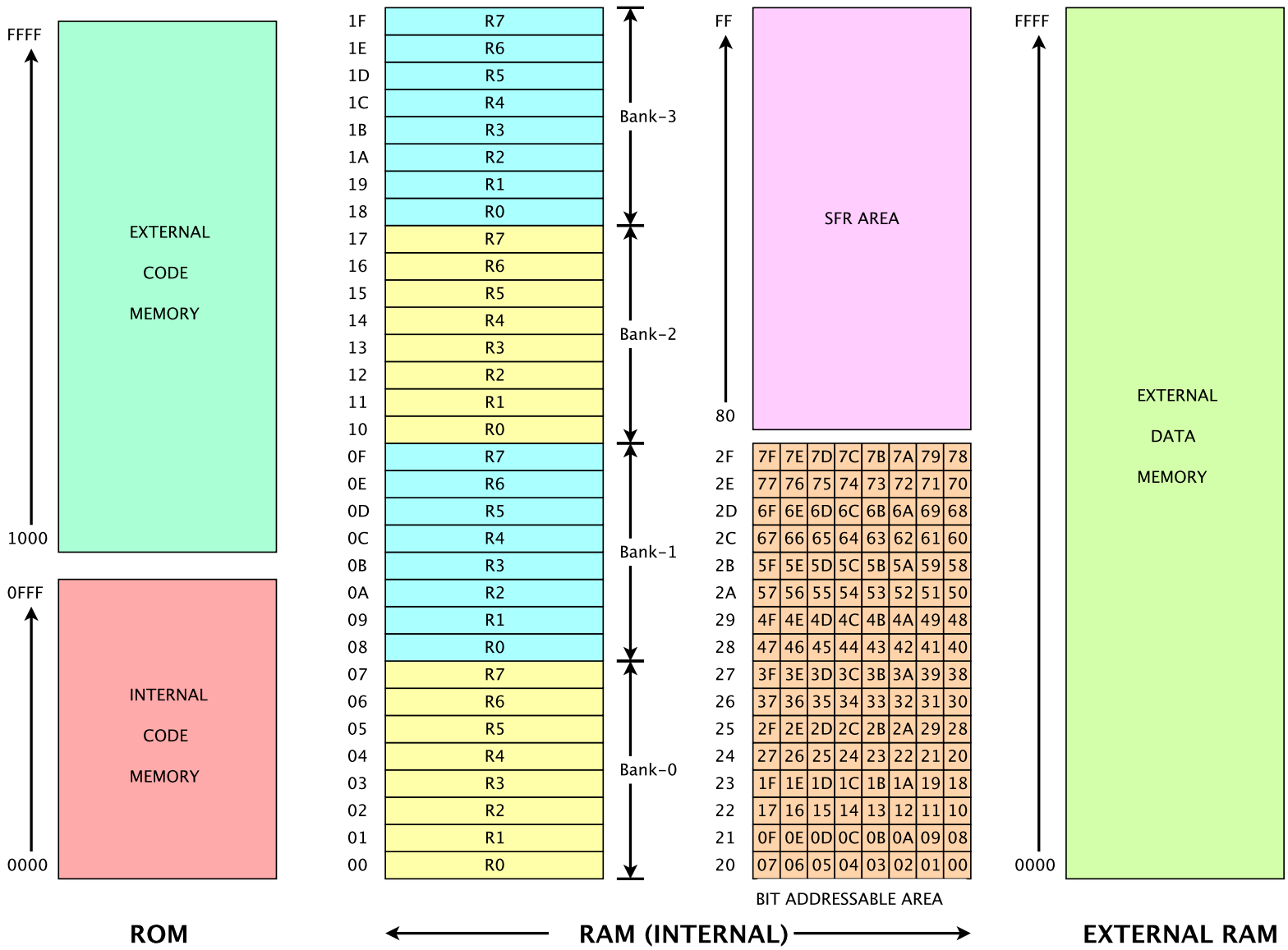
Memory Organization

The 8051 has Harvard architecture, which uses same memory address for both code and data memory.

- 4K of code memory (ROM) in which program instructions reside.
- 128 bytes of RAM is divided as–
  - 32 bytes of RAM ranging from 00h to 1Fh are divided across 4 register banks.
    - Each bank containing 8 registers named as R0-R7.
    - Each register is addressed by an internal address or by name (when the bank is selected).
    - Register bank is selected through PSW bits RS1 and RS0. Remaining bank registers can be treated as general purpose RAM.
- 16 bytes ranging from byte address 20h to 2Fh forms bit addressable area.
  - These bytes may be addressed at bit level with the address 00h to 7Fh .

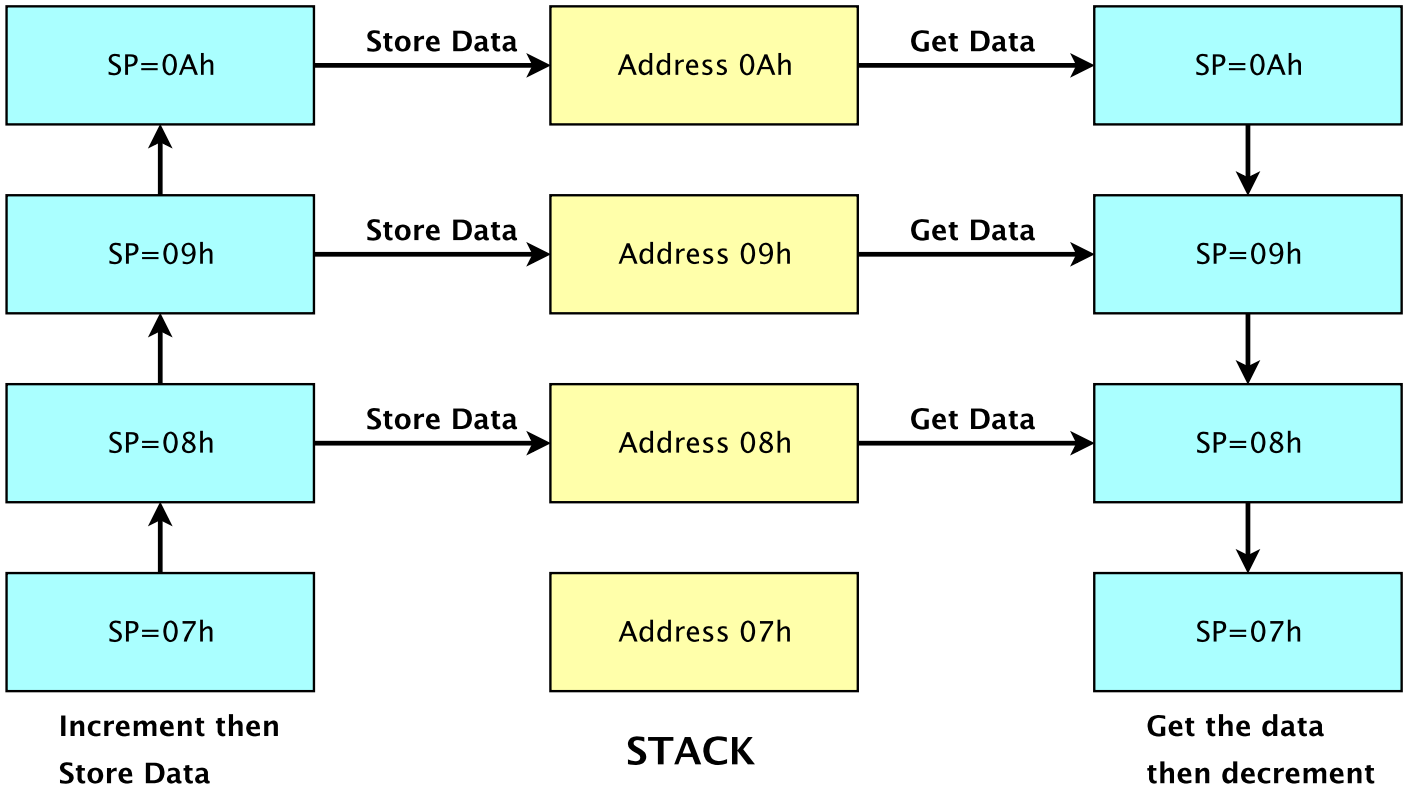
- RAM Contd..
  - 80 bytes of general purpose data memory (30-7F).
  - Some of the remaining bytes are utilized for internal operations, called as special function registers (SFRs).

The 8051 Memory Organization



Stack Pointer

- Stack is the area in RAM defined through certain instructions used to store the data.
- Stack pointer (SP) is the register which holds the RAM address in which the data is to be stored or from which the data is to be retrieved.
- When the data is to be placed on the stack, SP is incremented before the storing of the data. So the stack grows up as the data is stored.
- When the data is retrieved, the SP is decremented after reading (retrieve) the data.
- Note that stack operation in 8051 is exactly opposite to the 8085 microprocessor where stack is decremented before storing and incremented after retrieval.



The 8051 stack operation

Special Function Registers (SFR)

- Some of the registers in RAM other than 00h to 7Fh, are assigned for certain internal functions.
- They are called as special function registers (SFRs).
- Some of the SFRs are bit addressable as well.

Table: Special Function Registers of the 8051.

SFR	Address	Function	Comment
A	E0h	Accumulator	Bit addressable
B	F0h	Arithmetic	Bit addressable
DPH	83h	Addressing external memory	H. O. Byte
DPL	82h	Addressing external memory	L. O. Byte
IE	A8h	Interrupt Enable Control	Bit addressable
IP	B8h	Interrupt Priority	Bit addressable
PCON	87h	Power Control	Bit addressable
PSW	D0h	Program Status Word	Bit addressable

Table: Special Function Registers of the 8051.

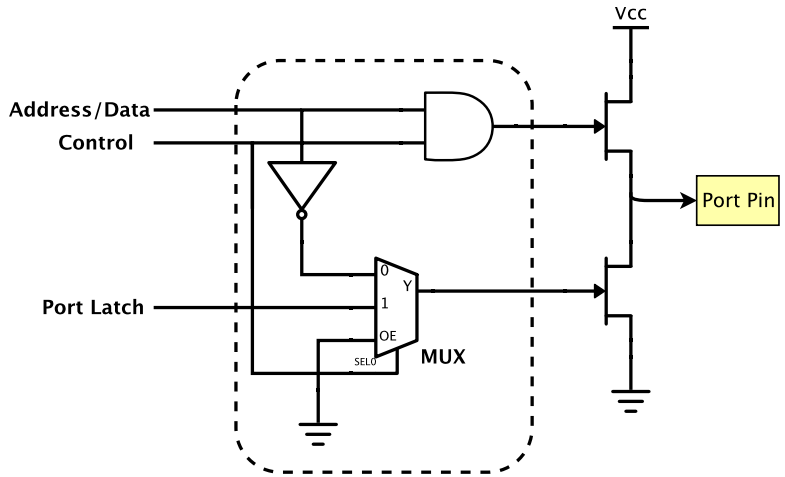
SFR	Address	Function	Comment
P0	80h	Input/Output Port-0 Latch	Bit addressable
P1	90h	Input/Output Port-1 Latch	Bit addressable
P2	A0h	Input/Output Port-2 Latch	Bit addressable
P3	B0h	Input/Output Port-3 Latch	Bit addressable
SCON	98h	Serial Port Control	Bit addressable
SBUF	99h	Serial Port Data Buffer	-
SP	81h	Stack Pointer	-
TMOD	89h	Timer/Counter Mode Control	-
TCON	88h	Timer/Counter Control	Bit addressable
TL0	8Ah	Timer 0 Low Byte	-
TH0	8Ch	Timer 0 High Byte	-
TL1	8Bh	Timer 1 Low Byte	-
TH1	8Dh	Timer 1 High Byte	-

Input/Output Ports of 8051

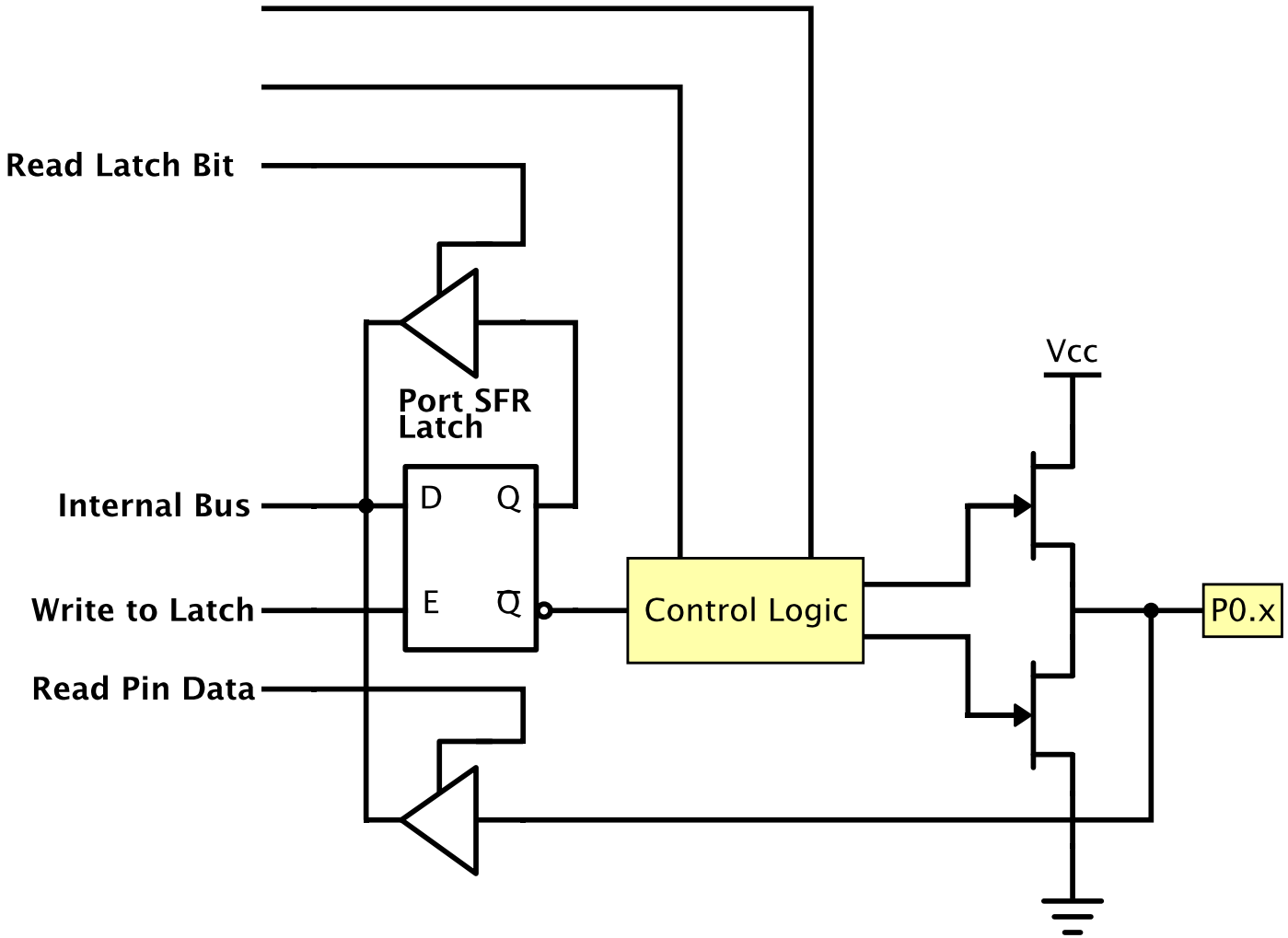
- The 8051 has 4 bi-directional 8-bit I/O ports.
- Each port is connected to an 8-bit register in the SFR, P0 = 80h, P1 = 90h, P2 = A0h, P3 = B0h.
- Each port is also connected to an output driver and an input buffer.
- The individual bits of each port can be operated as either input or output.
- It is made an input by writing 1 in its corresponding bit in the SFR register.
- All ports are configured as output ports at reset.
- Some of the 4 ports have dual role i.e pins have additional functionality–
  - Ports P0 and P2 are also used as Address and Data buses.
  - Port P3 pins have additional functionality for timers and counters, serial communication, interrupts and external control lines.

Port 0

- P0 can be used for input or output.
- The pins of P0 are connected internally to an "open drain" circuit (similar to open collector
- but using MOS transistors).
- Therefore, it must be connected to an external pull-up resistor (10 KW) to operate properly as an output port.
- To operate P0 as an input port, it must be programmed by writing 1's to all of its bits.



Dual Functionality Port Control Logic

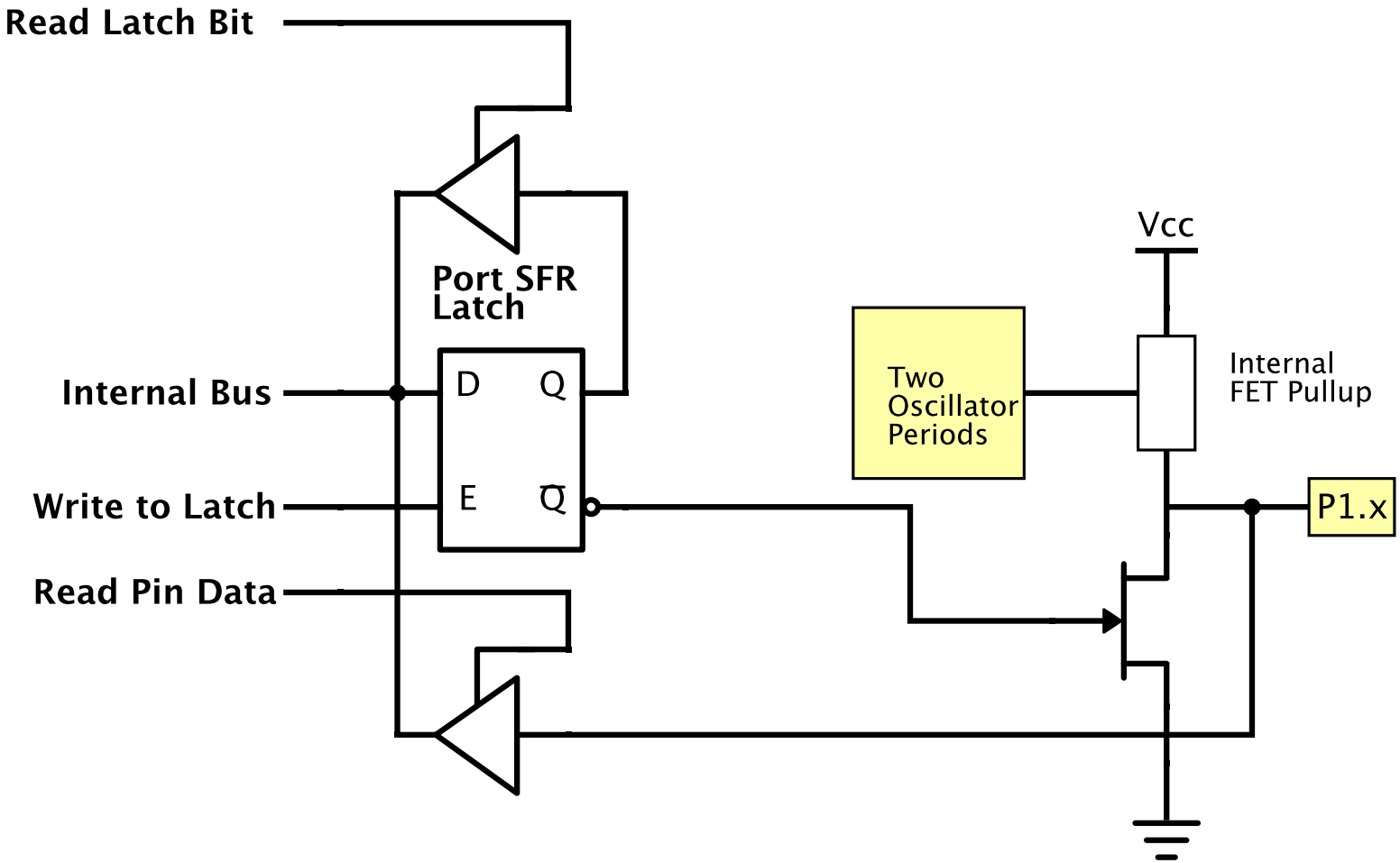


The 8051 Port 0 Pin

- P0 is also designated as AD0 – AD7 which means that it can also be used as the multiplexed lower 8 bits of the address bus and the 8 bits of the data bus.
- When accessing external memory (program or data), the address/data demultiplexing is done as follows–
  - ALE is used to differentiate when the pins are carrying an address vs. data.
  - ALE = 1 when the port 0 pins carry an address (if not I/O).
  - ALE=0 can be used to enable an external address latch that will hold the address value after it has been removed from the pins.
  - Now port P0 pins carry data in remaining machine cycle.

Port 1

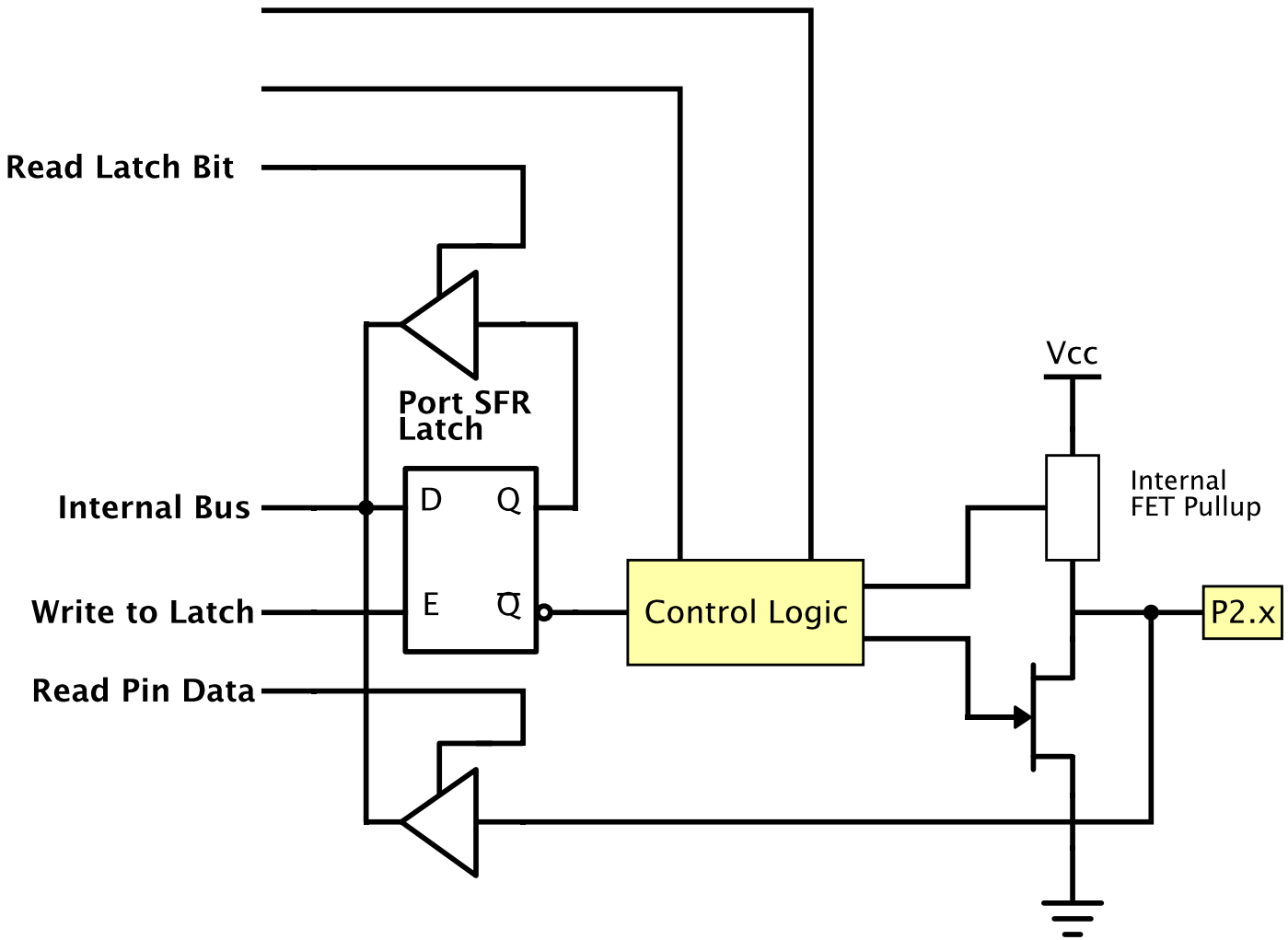
- Port 1 can be used both for input and output.
- Unlike Port 0, it's pins are connected to internal pull-up resistors so no external pull-up is needed.
- Therefore, if the external pin is left unconnected, the matching bit will be read as a logic high.
- Configured for input by default.



The 8051 Port 1 Pin

Port 2

- Port P2 is very similar to P1 in its basic operation and in the fact that it does not need external pull-up.
- As it was shown for port P0, port P2 also serves as the upper 8 bits of he address bus (A8 – A15) when accessing external memory.
- The upper 8 bits of the address will be kept on the P2 pins for the duration of the memory cycle.
- No need for external latching as pins have no address/data multiplexing.



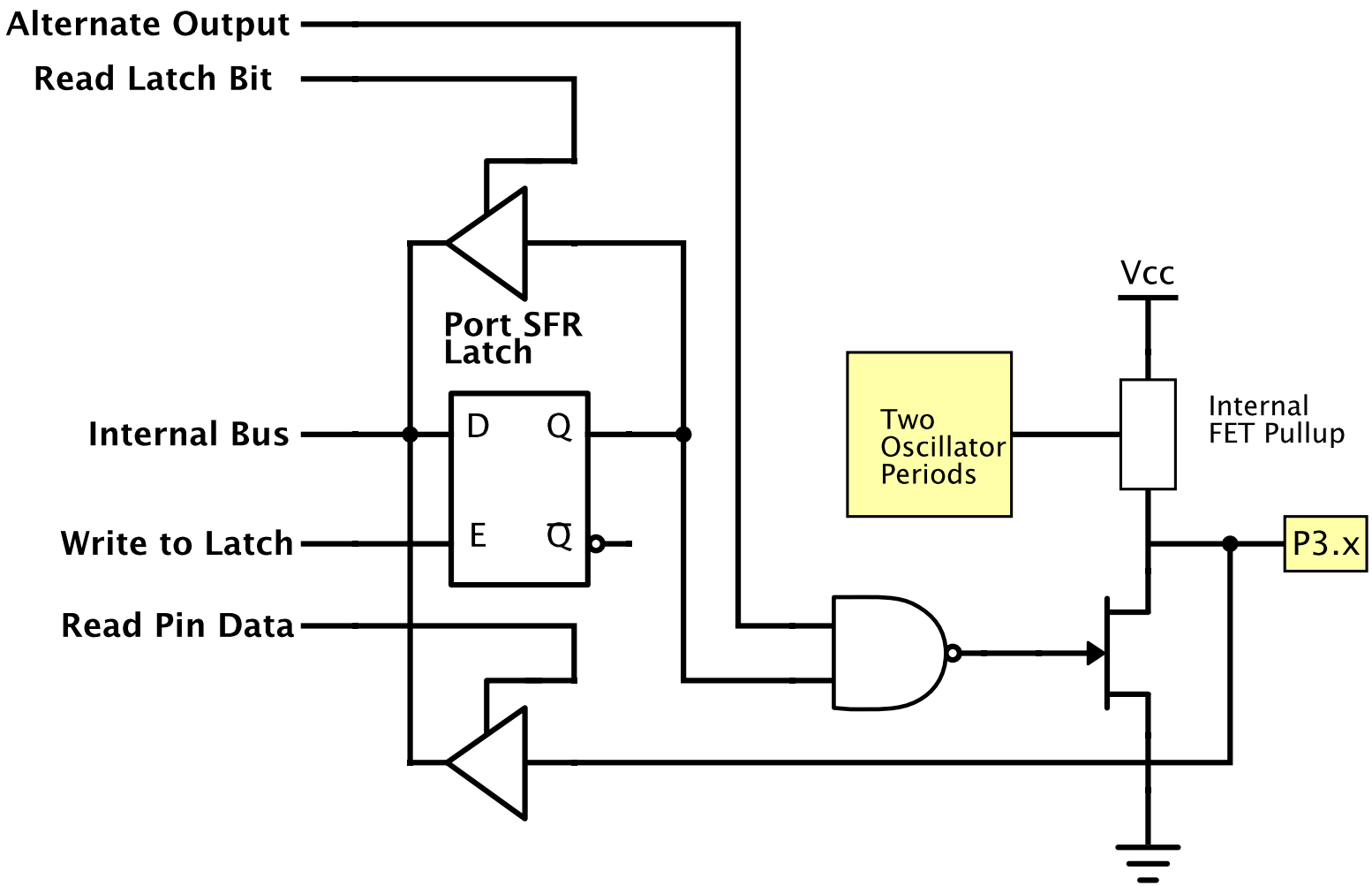
The 8051 Port 2 Pin

Port 3

- P3 is similar to P1 and P2 in its basic operation and in the fact that it does not need external pull-up.
- All port P3 pins are multifunctional, they are not only I/O port pins but they also serve special functions.

Note that–

- All pins on all ports are controlled by two signals (Read-Latch and Read-Pin).
- Depending on which signal is active, we either read the last value stored in the latch or the present value on the pin.
- Which signal will be activated?
  - Depends on the instruction.
  - All instructions that perform a Read-Modify-Write cycle read from the latch. e.g.– ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ, MOV PX.Y, C, CLR PX.Y, SETB PX.Y
  - All others read from the pin.



The 8051 Port 3 Pin

Timers/Counters

- The 8051 has two registers that can be used either as timers or counters, namely Timer0 and Timer1.
- These timers exist in the SFR area as pairs of 8-bit registers.
  - TL0 (8AH) and TH0 (8CH) for Timer0.
  - TL1 (8BH) and TH1 (8DH) for Timer1.
- LSB bit of the time counter is bit 0 of TL0 (or TL1) and MSB bit depends on the timer mode.

The timers can be used for:

- Interval timing: The timer is programmed to overflow at a regular interval and set the timer overflow flag. Overflow means reaching maximum count of FFFFH.
- Event counting: Determine the number of occurrences of an event. An event is any external stimulus that provides a 1-to-0 transition on a pin of the 8051.
- Baud rate generation for the built-in serial port.

TCON Register

Table: Function of bits in TCON

Bit	Symbol	Function
7, 5	TF1, TF0	Timer 1, Timer 0 overflow flags. Set when timer rolls from all 1s to 0. Cleared when processor vectors to execute ISR at address 001Bh, 000Bh.
6, 4	TR1, TR0	Run control bits for Timer 1, Timer 0. Set to 1 by program to enable timer/counter. Set to 0 by program to halt timer/counter. It does not reset timer.

07	06	05	04	03	02	01	00
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

The 8051 TCON Register

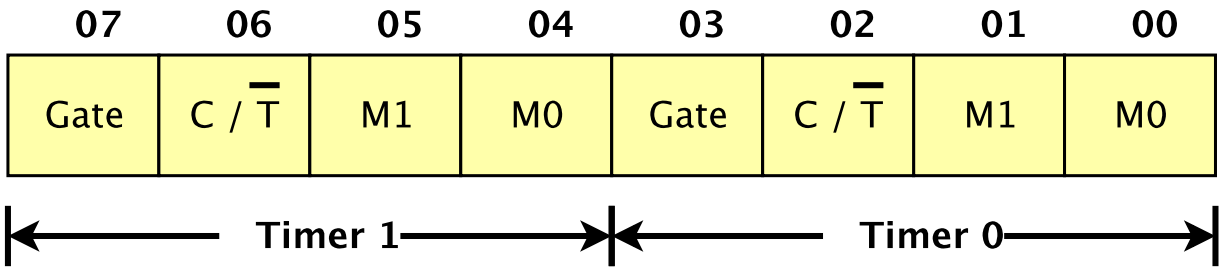
Table: Function of bits in TCON

Bit	Symbol	Function
3, 1	IE1, IE0	External interrupts 1, 0 edge flags. Set to 1 in the event of high to low transition (1 to 0) on port pin 3.3 ($\overline{INT1}$), port pin 3.2 ($\overline{INT0}$). Cleared when processor vectors to execute ISR at 0013h, 0003h.
2, 0	IT1, IT0	External intrrupt 1, 0 signal type control bit. Set to 1 by program to enable external interrupt1 to be triggered by falling edge. Set to 0 by program to enable external interrupt1 to be triggered by low level signal on.

TMOD Register

Table: Function of bits in TMOD

Bit	Symbol	Function
7, 3	Gate	OR gate enable bit for RUN/STOP of the timer. ■ RUN Timer1, 0 in *interrupt Mode* if we set, Gate =1 **AND** TR1 (TR0) = 1 **AND** $\overline{INTA0}$ ($\overline{INTA1}$) =0 . ■ RUN Timer1, 0 in *polling Mode* if we set, Gate =1 **AND** TR1 (TR0) = 1.



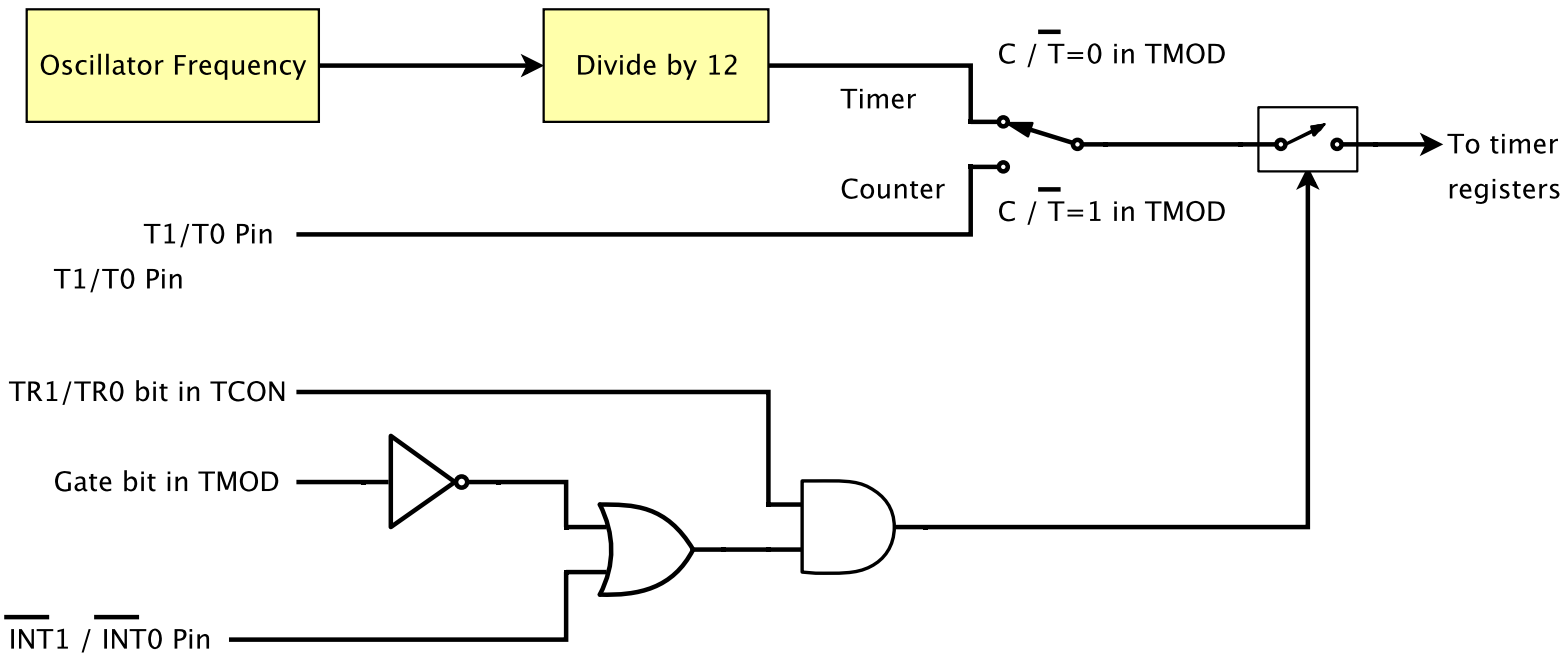
The 8051 TMOD Register

Table: Function of bits in TMOD

Bit	Symbol	Function
6, 2	$C/\bar{T}$	Set or reset by program. ■ $C/\bar{T} = 1$, sets timer as 'counter' that counts the pulses (events) on the pin 3.5 (T1) or pin 3.4 (T0). ■ $C/\bar{T} = 0$, sets timer as 'timer' that counts the internal frequency.
[5,4], [1,0]	[M1, M0]	Timer/Counter mode control bits. $M1$ $M0$ 0 0 Mode 0 0 1 Mode 1 1 0 Mode 2 1 1 Mode 3

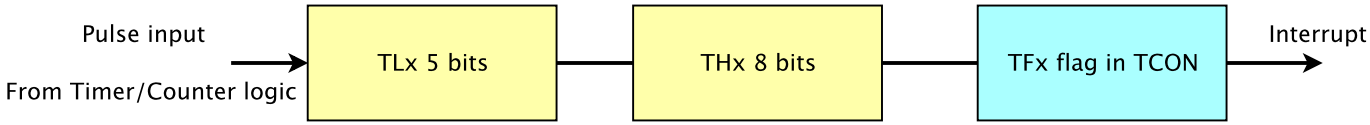
Timer/Counter Control Logic

- Timer/Counter functions when TRx bit in TCON=1 'AND' Gate in TMOD=1 OR *barINTx*=1.
- For timer operation i.e. $C/\bar{T} = 0$, it counts after every 12 clock pulses. ie. counts at ' frquency divided by 12' rate. e.g. If internal clock frequency is 6 Mhz, the timer clock will have 500 Khz frequency.
- When used as counters i.e. $C/\bar{T} = 0$, the registers will be incremented once on every 1-0 (negative edge) on the appropriate input pin (T0 – P3.4 or T1 – P3.5).
- The pin must be held high for one complete machine cycle and then low for one complete machine cycle.

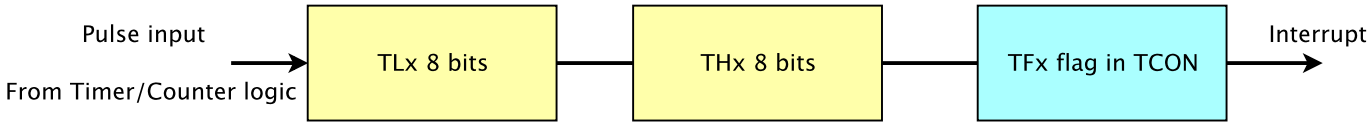


Timer/Counter Control Logic

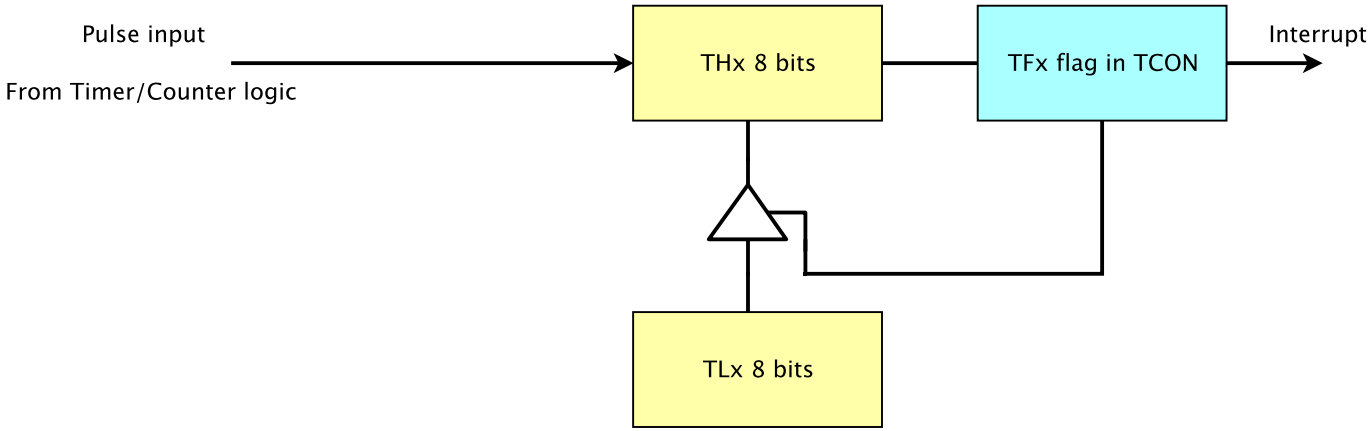
Timer Modes



Timer Mode 0, 13 bit Timer/Counter



Timer Mode 1, 16 bit Timer/Counter



Timer Mode 2, Auto reload of TLx from THx

Timer/Counter Mode 0, Mode 1 and Mode 2

- Timer/Counter Mode 0 (M1=0, M0=0 in TMOD)
  - This mode uses TLx as 5 bit counter and THx as 8 bit counter. i.e Resultant counter is 13-bit counter.
  - So the input pulses (from timer/counter control circuit) are divided by ($2^5 = 32$) in TLx.
    e.g. If the crystal frequency is 6 MHz, the input frequency to TLx is 6MHz/12=500KHz. The output frequency is 500KHz/32=15.625KHz.
  - The timer flag TFx is set when THx goes from FFh to 00h.
- Timer/Counter Mode 1 (M1=0, M0=1 in TMOD)
  - This mode uses TLx as 8 bit counter and THx as 8 bit counter. i.e Resultant counter is 16-bit counter.
  - So the input pulses (from timer/counter control circuit) are divided by ($2^8 = 256$) in TLx.
    e.g. If the crystal frequency is 6 MHz, the input frequency to TLx is 6MHz/12=500KHz. The output frequency is 500KHz/256=1.9531KHz.
  - The timer flag TFx is set when THx goes from FFh to 00h.

- Timer/Counter Mode 2 (M1=1, M0=0 in TMOD)
  - This mode uses TLx as 8 bit counter and THx is used to hold the value which is reloaded into TLx whenever TLX goes from FFh to 00h.
  - The timer flag TFx is set when TLx goes from FFh to 00h.
  - e.g. To generate the delay of 0.2 ms at 6 MHz crystal frequency,

$$delay = (Count_{max} - Count)_{10} * \frac{12}{f}$$

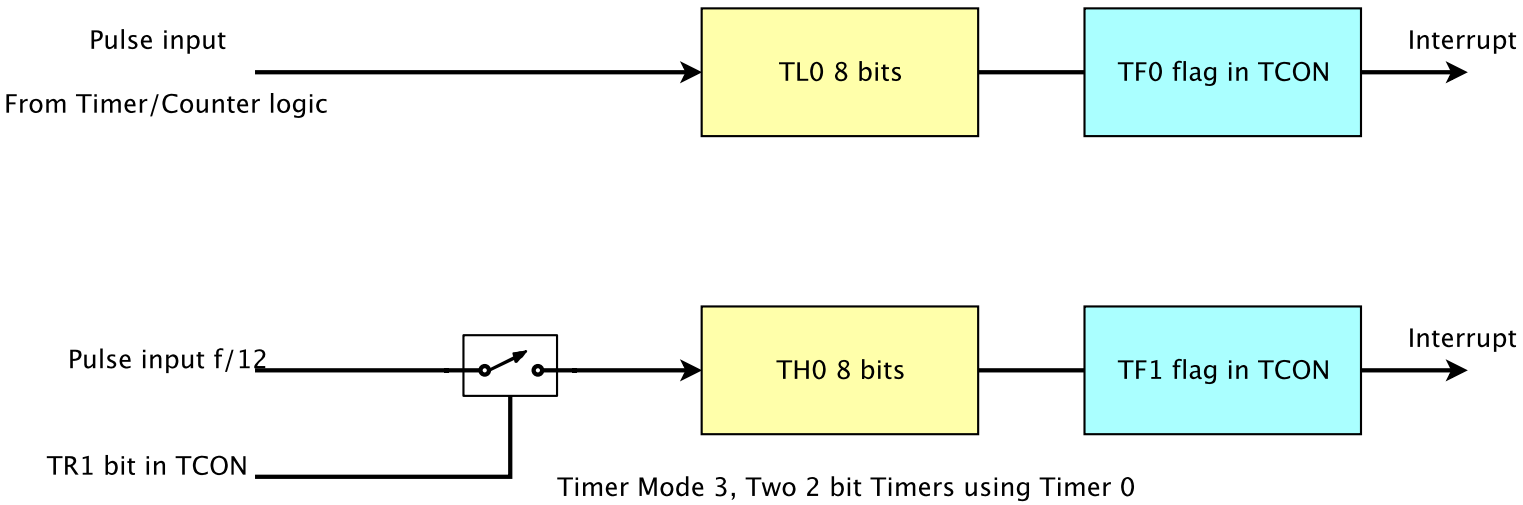
$$0.2 \times 10^{-3} = (256 - Count)_{10} * \frac{12}{6 \times 10^{6}}$$

$$\Rightarrow Count_{10} = 156$$

$$\Rightarrow Count_{16} = 9C$$

i.e. Load the THx with 9Ch to generate 0.2ms delay pulses continuously.

- Timer/Counter Mode 3 (M1=1, M0=1 in TMOD)
  - Timer 0 and Timer 1 can be used independently in either Mode 0, 1 or 2. However, If Timer 0 is working in Mode 3, the Timer 1 can not be used independently. As Timer 0 in Mode 3 uses both the overflow flags.



Timer/Counter Mode 0, Mode 1 and Mode 2

- If Timer 1 is configured in Mode 3, it stops counting. The start bit TR1 and overflowflag TF1 are used by timer 0.
- Timer 0 in Mode 3, becomes to seperate 8 bit counters.
- TL0 receives input pulses from Control logic circuit, while TH0 counts f/12 input pulses.
- The operation of the TH0 is controlled by TR1 and TF1 flag sets when transition from FFh to 00h occurs.
- Note that–Timer 1 can be set in either Mode 0, 1 or 2 when Timer 0 in Mode 3. But only it can not generate interrupt.
- Therefore Timer 1 in this case can be used in operations where timer interrupt is not needed such as baud rate generation for serial port that does not depend on interrupt or any other use of overflow flag.

Event Counting

- The only difference between the time and counter is the source of clock pulses.
- When $C/\bar{T}$=1, the counting operation in TLx and THx is done from the Tx pin of the microcontroller.
- Tx pulse is sampled at P2 of state 5 in every machine cycle.
- Therfore, the pin should held constant for atleast one machine cycle.
- Change of pulse from high to low only increases the counter value.

Serial Data Communication

- The 8051 has serial data communication circuit that uses register SBUF to hold the data.
- SBUF is physically two registers (having the same address)–
  - One is 'write only' and is used to hold the data to be transmitted through TXD pin.
  - Another is 'read only' and holds the received data through the RXD pin.
- Serial control operation in various modes is primarily controlled via SCON register.
- Serial data communication is relatively slow process.
- To utilize the processor time, serial data flags TI and RI are used. TI and RI are Ored together to produce an interrupt to the program.
- These flags are not cleared automatically after interrupt generation, programmer has to reset it before the next use.
- Note that–Transmission is under complete control of program but reception of data is unpredictable.

SCON Register

Table: Function of bits in SCON

Bit	Symbol	Function
7,6	SM0, SM1	Serial port mode bits.

*SM*0	*SM*1	*Mode*	
0	0	0	Shift register, baud=f/12
0	1	1	8-bit UART, baud=variable
1	0	2	9-bit UART, baud=f/32 or 64
1	1	3	9-bit UART, baud=variable

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

The 8051 SCON Register

Table: Function of bits in SCON

Bit	Symbol	Function
5	SM2	Multiprocessor communication bit for Mode 2 & 3. Set/Cleared by program. When SM2=1 AND bit 9 of received data is 1, an interrupt is generated. If bit 9 of received data is 0, no interrupt is generated. In Mode 1, an interrupt is generated only if valid stop bit is received. Clear to 0 in Mode 0.
4	REN	Receive enable bit. Set to 1 to enable reception. Clear to 0 to disable reception.
3	TB8	Transmitted bit 8. Set/cleared by program in Mode 2 & 3.
2	RB8	Received bit 8. Bit 8 of received data in Mode 2 & 3 Stop bit in Mode 1. Not used in Mode 0.

Table: Function of bits in SCON

Bit	Symbol	Function
1	TI	Transmit interrupt flag. Set to 1 at the end of bit 7 time in Mode 0, and at the beginning of the stop bit in other modes. Must be cleared by program.
0	RI	Receive interrupt flag. Set to 0 at the end of bit 7 time in Mode 0, and halfway through the stop bit in other modes. Must be cleared by program.

PCON Register in Serial Data Communication

- Bit 7 of PCON register, called as SMOD, is used to modify the baud rate. Set/Cleared by program.
- Set to 1 to double the baud rate using timer 1 in serial Modes 1, 2 and 3.
- Clear to 0 to use timer 1 baud rate.
- Other bits of the PCON are–
  - GF1 (bit 3) and GF0 (bit 2) bits are general purpose user flags which are set/clear by program.
  - PD (bit 1) is power down bit. Set to 1 by program to enter power down configuration (for CHMOS family)
  - IDL (bit 0) is idle mode bit. Set to 1 by program to enter power down configuration (for CHMOS family)

7	6	5	4	3	2	1	0
SMOD	–	–	–	GF1	GF0	PD	IDL

The 8051 PCON Register

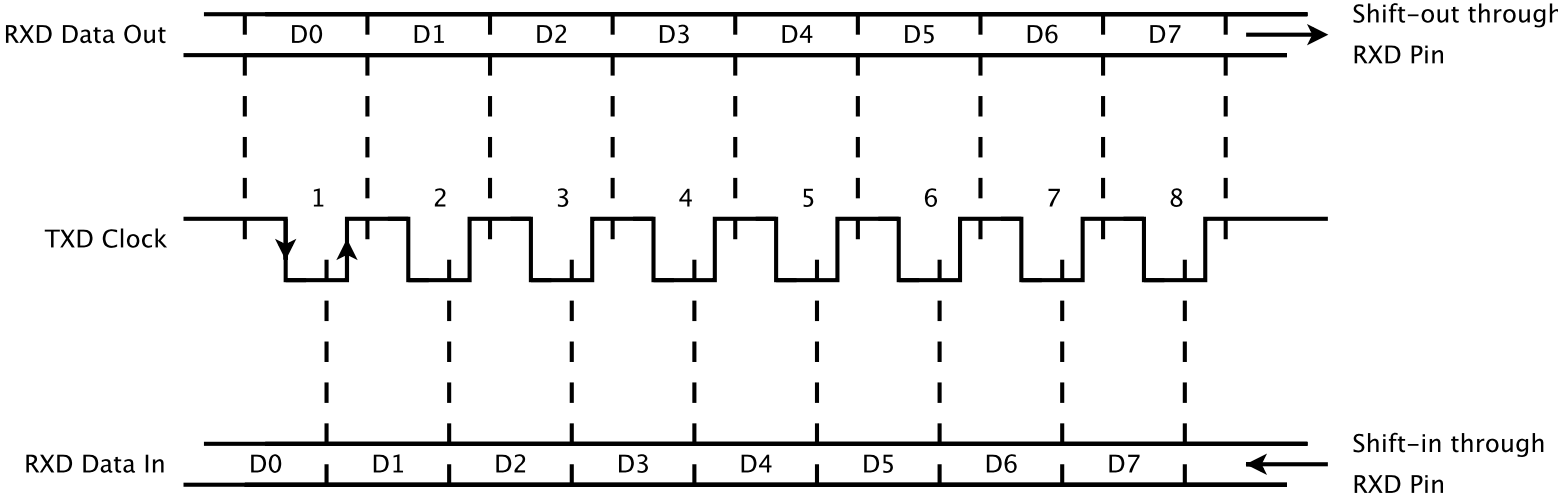
Serial data transmission and reception

- Transmission:
  - Serial transmission begins any time the data is written to SBUF.
  - TI is set to 1 when the data byte has been transmitted (i.e. SBUF is empty for transmission purpose) and that the other data byte can be sent. If program fails to wait for the TI flag and byte is overwritten SBUF, this results into 'garbage out'.
- Reception:
  - Reception of serial data will begin when REN in SCON register is 1. Also, in Mode 0 RI must be reset to 0 to begin the reception.
  - In other modes, reception can be began with RI=1, but it must be cleared by program before last bit is received otherwise the data will be lost.
  - incoming data is not transferred to the SBUF until last bit is received so that data byte can be read from SBUF while new data is being received.

Serial data communication modes

Mode 0 – Shift register mode:

- SBUF is configured to receive and transmit the data using RXD pin only.
- TXD pin is connected internally to the shift frequency pulse source so as to supply shift pulses to the external circuit.
- Shift frequency or baud rate is fixed at $f_{baud} = \frac{f}{12}$.
- The shift clock pulses are low for machine cycle states S3-S4-S5 and high for states S6-S1-S2.
- When transmitting, data is shifted out of RXD one pulse after the rising edge of TXD shift clock (S6-P2).
- The data received through RXD is sampled at falling edge of the TXD shift clock (S5-P1).

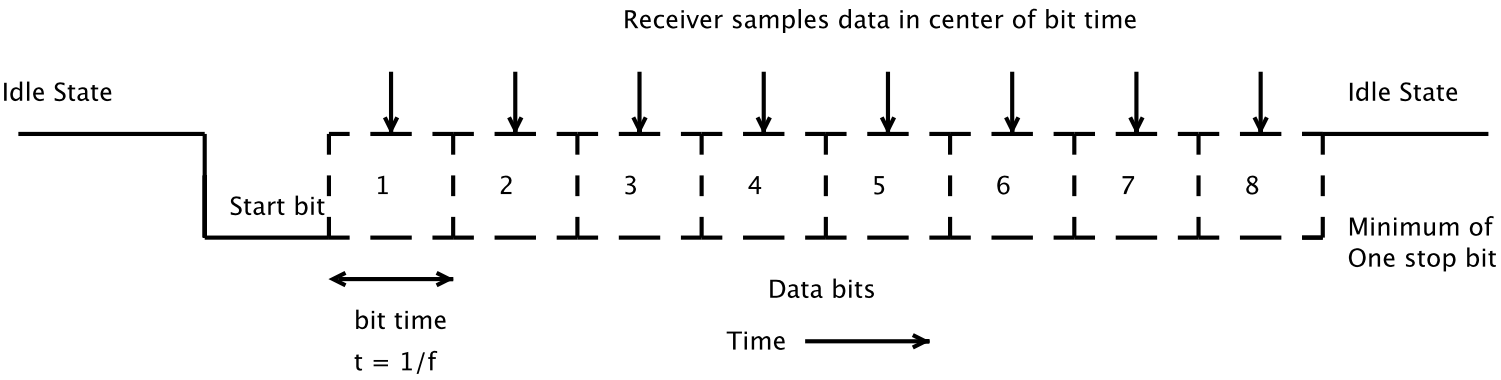


The 8051 serial Mode 0 timing diagram.

Mode 1 – Standard UART:

- In Mode 1, SBUF becomes 10 bits full duplex receiver/transmitter that may receive and transmit the data at the same time.
- Pin RXD receives all the data and pin TXD transmits all the data.
- The data is transmitted through TXD as start bit, 8 data bits (LSB first) and stop bit and received through RXD in the same order.
- Interrupt flag TI is set once all the ten bits have been sent.
- Reception is triggered by the falling edge of start bit and continues till valid stop bit (logic 1) is received.

- SBUF is loaded by a byte if RI=0 AND (STOP BIT=1 OR SM2=0)
- ie. if SM2=1, no meaning of stop bit. Thus in Mode 1 usally set SM2=0.
- Of the received 10 bits, start bit is discarded, 8 bit data is stored in SBUF and stop bit in RB8.
- RI becomes 1, it indicates that the data byte is received.
- Bit interval is inverse of baud rate frequency $t = \frac{1}{f_{baud}}$.



The 8051 serial Mode 1 timing diagram.

Setting the baud rates in Mode 1

- If timer 1 in auto-relaod mode (timer Mode 2) is used to generate baud rate.
- The baud rate in this case is given by,

$$f_{baud} = \frac{2^{SMOD}}{32} \times \frac{f}{12 \times (256 - TH1)}$$

- Thus SMOD=1 in PCON makes the baud rate doubled.
- If timer1 is in anyother mode but Mode 2, then baud rate is given by

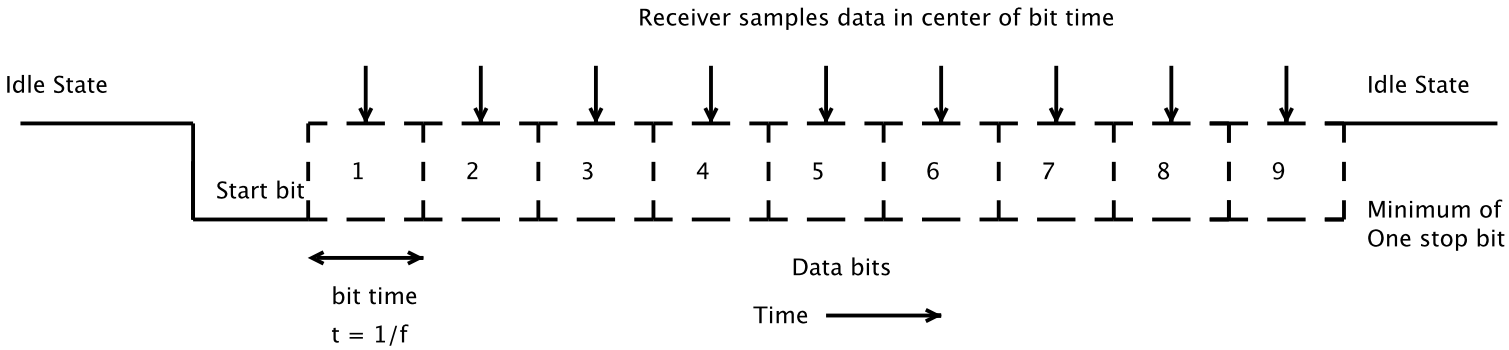
$$f_{baud} = \frac{2^{SMOD}}{32} \times (Timer\ 1\ overflow\ frequency)$$

Mode 2 – Multiprocessor Mode:

- In Mode 2, SBUF becomes 11 bits full duplex receiver/transmitter that may receive and transmit the data at the same time.
- 11 bits are transmitted: a start bit, nine data bits and a stop bit.
- The ninth bit is copied from TB8 in SCON during transmission and stored in RB8 during reception.
- The baud rate is programmed as:

$$f_{baud} = \frac{2^{SMOD}}{32} \times (Oscillator\ frequency)$$

- For setting RI for mode 2 needs RI=0 and SM2=0 or ninth bit=1.
- Setting RI based on SM2 in the receiving 8051 and state of ninth bit in transmitted message makes multiprocessing possible.



The 8051 serial Mode 2 timing diagram.

Mode 3 – Serial Data Mode:

- Mode 3 is identical to mode 2 except that the baud rate is determined exactly as in mode 1, using timer 1 to generate communication frequencies.

Interrupts

- Hardware signals that force the program to call a subroutine are Interrupts.
- Interrupts may be generated by internal chip operations or provided by external sources.
- Five Interrupts are provided in 8051.
- Timer flag 0, Timer flag 1 and the serial port interrupt (RI or TI) which are generated automatically by internal operations.
- Two interrupts are triggered by external signals provided by circuitry connected to INT0 and INT1 pins.
- All interrupts are under the control of program.
- After the interrupt has been handled by ISR placed at interrupt location in memory, main program must resume operation.

External Interrupts

- Inputs on INT0 and INT1 set interrupt flags IE0 and IE1 in TCON register.
- IEX flags may be set when a high-to-low transition takes place on the INTX pin.
- IT0 and IT1 bits of TCON are used to set level triggered and edge triggered interrupts.
- Edge triggered interrupt will be reset on execution of ISR but level triggered interrupt needs reset by the program.

Interrupt Control

Interrupt Enable

- Bits in IE register are set to 1 if corresponding interrupt source is to be enabled and set to 0 to disable the interrupt source.
- Bit EA is a master bit that can enable or disable all of the interrupts.

7	6	5	4	3	2	1	0
EA	–	–	ES	ET1	EX1	ET0	EX0

The 8051 IE Register

Table: Function of bits in IE

Bit	Symbol	Function
2, 0	EX1, EX0	External interrupts 1, 0. Set to 1 by program to enable ($\overline{INT1}$) and ($\overline{INT0}$). Cleared to 0 to disable.
3, 1	ET1, ET0	Timer overflow interrupt 1, 0. Set to 1 by program to enable timer overflow.Cleared to 0 to disable.
4	ES	Serial Port interrupt. Set to 1 by program to serial port interrupt.Cleared to 0 to disable.
7	EA	Enable All interrupts.Set to 1 by program to permit individual interrupts to be enabled by their enable bits.Cleared to 0 to disable all the interrupts.

Interrupt Priority

- Priority to various interrupts can be assigned using IP register of 8051.
- IP bits determine if any interrupt is to have a high or low priority.
- Bits set to 1 give corresponding interrupt high priority , a 0 assigns a low priority.
- A high priority interrupt can interrupt another one with low priority.
- If two interrupts with same priority occur at the same time, they have following ranking : IE0, TF0, IE1, TF1 and Serial interrupts.

IP Register

7	6	5	4	3	2	1	0
–	–	–	PS	PT1	PX1	PT0	PX0

Table: Function of bits in IP Register

Bit	Symbol	Function
2, 0	PX1, PX0	Priority of External interrupts 1, 0. Set/cleared by program.
3, 1	PT1, PT0	Priority of Timer overflow interrupts 1, 0. Set/cleared by program.
4	PS	Priority of serial port interrupt. Set/cleared by program.

Interrupt Destinations

- Interrupt causes a hardware call to dedicated addresses in program memory.
- A routing should be placed at that memory addresses.
- The interrupt saves PC of the program, on to stack and a call is made.
- RETI at the end of routine restores the PC to its place and resets interrupt logic so that another interrupt can be serviced.
- IE0 0003, TF0 000B, IE1 0013, TF1 001B and Serial 0023 are the interrupts and their locations in program memory for ISRs.

Power Saving Modes

- 8051 has two power saving modes.
- They are - Idle Mode and Power Down Mode
- Idle mode is set by setting IDL bit to 1 in PCON register.
- Clock signal to CPU is gated off but is given to interrupt, timer and serial port functions.
- CPU status is preserved along with SP, PC, PSW, Accumulator and other registers.
- Activation of any enabled interrupt clears IDL bit also hardware reset cause exit from this mode.
- Power down mode is set by setting PD bit to 1 in PCON register.
- The internal clock to the entire microcontroller is stopped but program is not dead.
- Hardware reset cause exit from this mode

That's the end of TOPIC-2 !