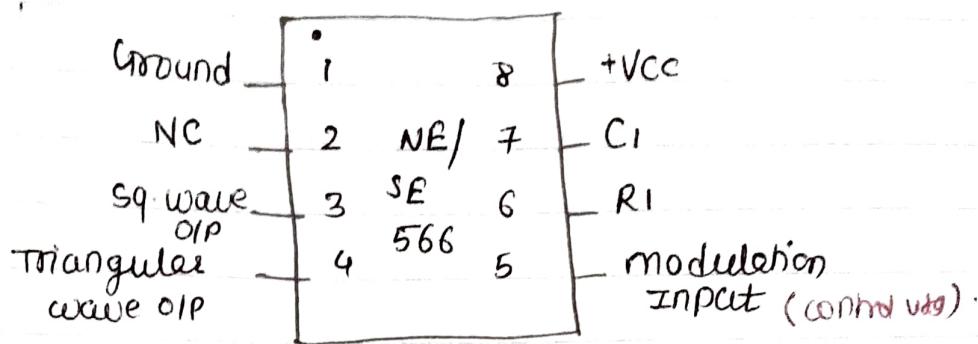


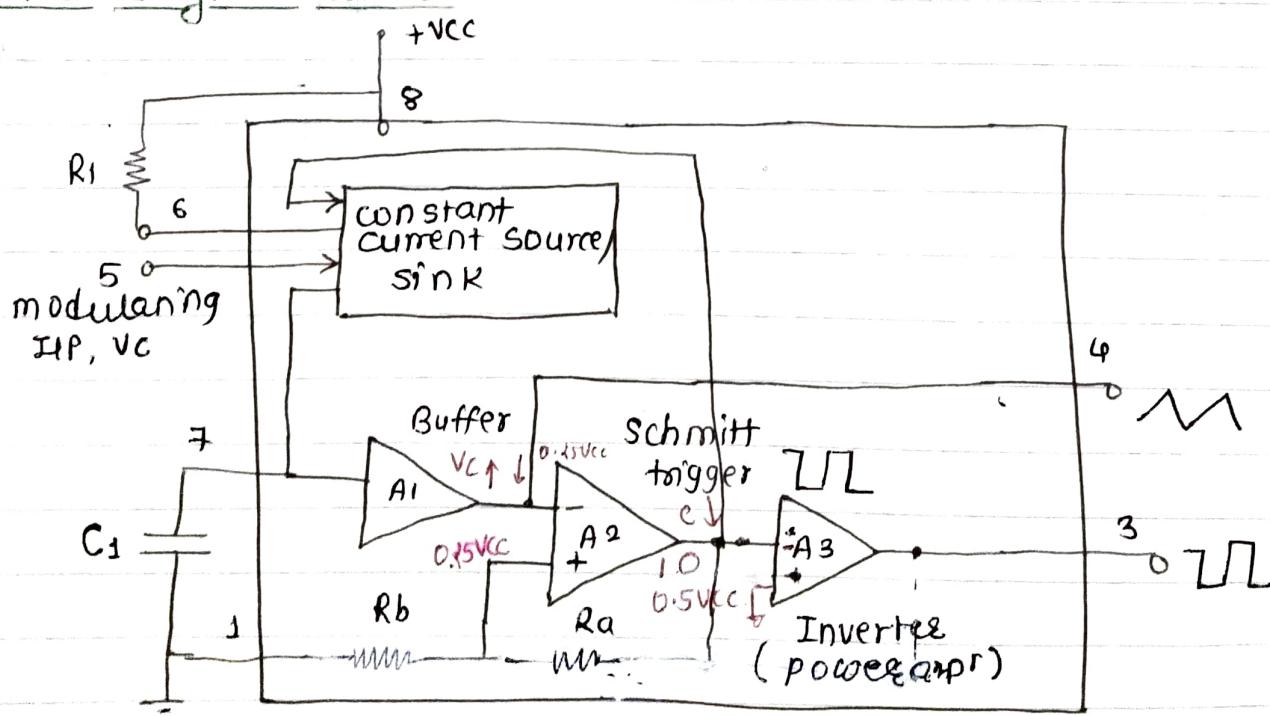
## Voltage Controlled oscillator NE/SE 566 :-

### Pin Diagram :-



- Freq' of oscillations is determined by an externally connected  $R_1$  &  $C_1$ .
- The control vdg. or modulating input  $v_c$  is applied at pin 5.
- Triangular wave is generated by charging & discharging of  $C$ . The amount of charge & discharge vdg is determined by Schmitt trigger. Schmitt trigger also provides sq. wave o/p at pin 3 thr' the power amp<sup>r</sup>  $A_3$  & the triangular o/p is available at pin 4 thr' buffer amp<sup>r</sup>  $A_1$ .

### Block diagram of VCO :-

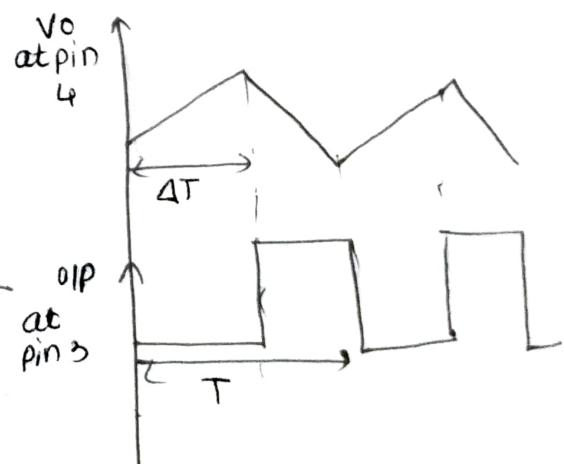
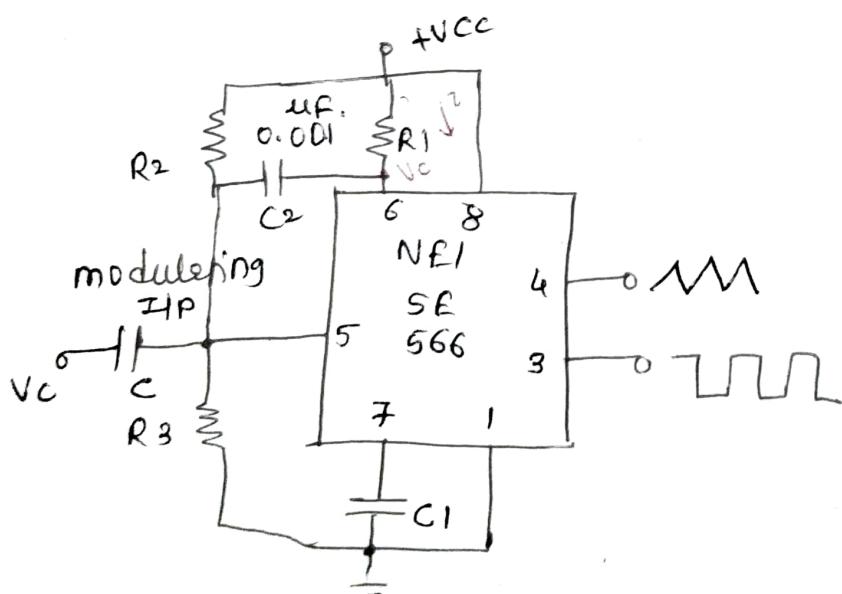


## Operation of VCO:-

- The o/p utg. swing of schmitt trigger is set to the levels  $V_{CC}$  &  $0.5V_{CC}$ . If  $R_a = R_b$  in the +ve f/b path, the utg at non-inverting terminal of op-amp A2 swings from  $0.5V_{CC}$  to  $0.25V_{CC}$ . During charging of  $C_1$ , when the utg alc  $C_1$  just exceeds  $0.5V_{CC}$ , schmitt trigger switches to low ( $0.5V_{CC}$ ) & the 'C' starts discharging. When utg. alc  $C_1 \downarrow$  to  $0.25V_{CC}$ , the schmitt trigger switches to HIGH ( $V_{CC}$ ).

By maintaining the source current & sink current of the two current sources equal, a uniform  $\Delta$  utg with equal +ve & -ve slopes is obtained at pin 4. The sq. wave o/p of schmitt trigger inverted & buffered is available at pin 8.

## Typical connection dia:-



$$f_o = \frac{2[V_{CC} - (718)V_{CC}]}{C_1 R_1 V_{CC}} = \frac{1}{4R_1 C_1}$$

Derivation of  $f_0$  of VCO:

c discharge  
Vc ↓ Vc < C charge

Vtg change w.r.t  $C_1$  is  $\Delta V = 0.25V_{CC}$  [0.5V<sub>CC</sub> - 0.25V<sub>CC</sub>].

∴ constant current source used, the rate of change of Vtg w.r.t  $C_1$  is

$$\frac{\Delta V}{\Delta t} = \frac{i}{C_1} \quad (\because I = C \cdot \frac{dV}{dt})$$

$$\therefore \frac{0.25V_{CC}}{\Delta t} = \frac{i}{C_1}$$

$$\text{or } \Delta t = \frac{0.25V_{CC} \cdot C_1}{i} \quad \dots \dots \textcircled{1}$$

The time period T of A wave is  $2\Delta t$

∴  $f_0$  is

$$f_0 = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{i}{0.5V_{CC} \cdot C_1} \quad \text{--- \textcircled{2}}$$

$$\& i = \frac{V_{CC} - V_c}{R_1}, \quad f_0 = \frac{V_{CC} - V_c}{R_1 \cdot 0.5V_{CC} \cdot C_1} = \frac{2(V_{CC} - V_c)}{R_1 C_1 V_{CC}}$$

$$f_0 = \frac{2(V_{CC} - V_c)}{C_1 R_1 V_{CC}}$$

∴ VCO can be varied by, freq<sup>n</sup>:

- i)  $R_1$
- ii)  $C_1$
- iii)  $V_c$

If  $V_c$  is set to  $7/8 V_{CC}$  then

$$f_0 = \frac{2(V_{CC} - (7/8)V_{CC})}{C_1 \cdot R_1 \cdot V_{CC}} = \frac{1}{4R_1 C_1} \leftarrow \text{independent of } V_c$$

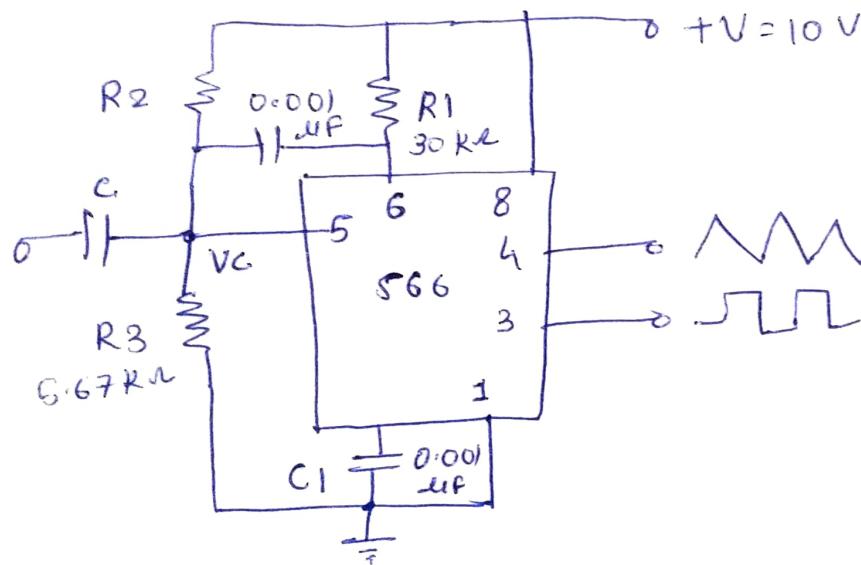
$V_{CO} \rightarrow$  Design IC 566 for freq<sup>n</sup> range of 10 KHz. Find the change in control voltage if freq<sup>n</sup> is varied from 9 KHz to 10 KHz.

Sol<sup>n</sup>:  $f_0 = 2[V^+ - V_C]/R_1 C_1 (V)$   $\therefore V_C = \frac{3}{4} V^+$   
 let  $V_C = 0.85 (+V)$  &  $V^+ = 10V$ . i.e  $V_C = 8.5V$   
 $V_C = \frac{R_3}{R_2 + R_3} (+V)$  i.e  $\frac{R_3}{R_2 + R_3} = 0.85$  i.e  $R_3 = 5.667 R_2$

Let  $R_2 = 1\text{ k}\Omega$   $\therefore R_3 = 5.667\text{ k}\Omega$ .

$$\therefore f_0 = \frac{2[10 - 8.5]}{R_1 C_1 \times 10} = 10 \times 10^3 \text{ i.e } R_1 C_1 = 3 \times 10^{-5}$$

choose  $C_1 = 0.001\text{ }\mu\text{F}$ ,  $\therefore R_1 = 30\text{ k}\Omega$ ,

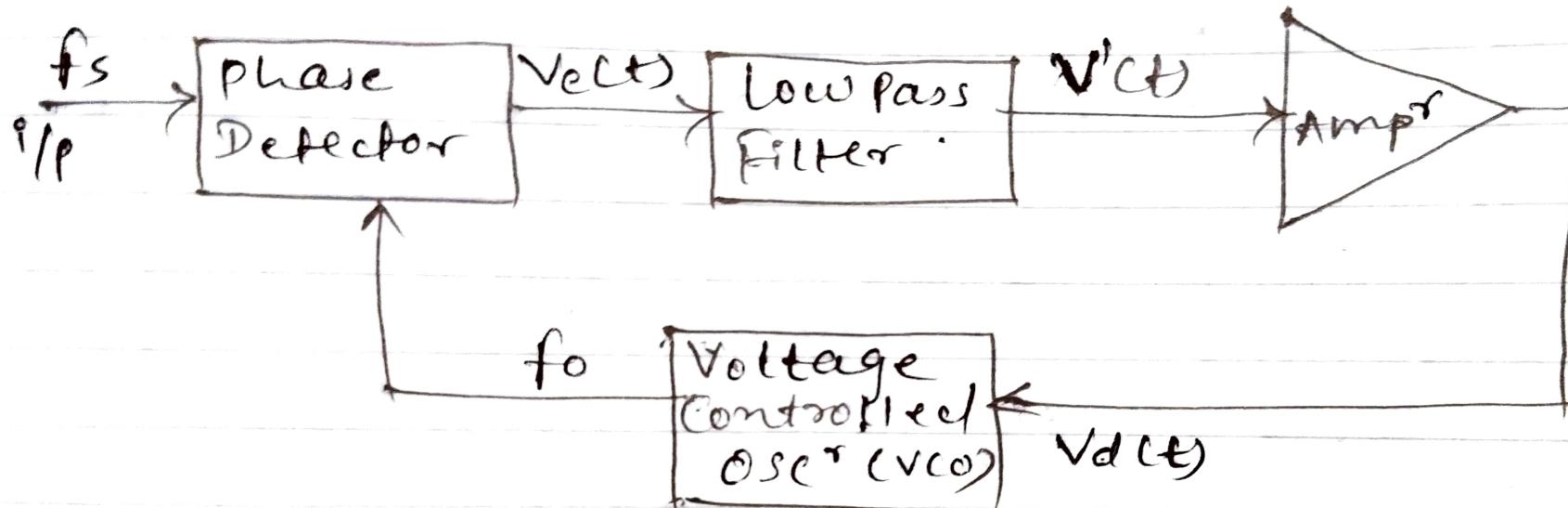


$$\Delta f_0 = 10 - 9 = 1\text{ KHz.}$$

$$\therefore \Delta V_C = \frac{R_1 C_1 \Delta f_0 (+V)}{2} = \frac{30 \times 10^3 \times 0.001 \times 10^{-6} \times 1 \times 10^3}{2} = 0.15$$

Thus  $V_C$  must be changed by 0.15V to change the freq<sup>n</sup> by 1 KHz.

# Phase Locked Loop (PLL)



A PLL is defined as a control mechanism by which the frequency & phase of incoming signal is synchronized with freq. & phase of VCO.

It consists of three blocks.

- i) Phase detector
- ii) Low pass filter
- iii) Voltage Controlled oscillator.

PLL passes through three modes of operation to go into lock condition.

→ Before application of i/p, the VCO operates at freq. depending upon the external resistance & capacitor. This is called free running frequency or the centre frequency ' $f_0$ ' of the VCO. This mode of operation of the PLL is called the free running mode.

→ On the application of an external i/p  $V_s \sin \omega_s t$ , the output of phase detector, which is mixer stage, has sum & difference freq. components. [ $f_s + f_0$  &  $f_s - f_0$ ].

→ The phase detector compares the i/p freq.  $f_s$  with the feedback freq.  $f_0$ . The o/p of phase detector is proportional to the phase difference  $\theta$  between  $f_s$  &  $f_0$ . The o/p of phase detector has a dc component, called error voltage  $V_e(t)$ .

→ The low pass filter passes the low freq. component ( $f_s - f_0$ ) & attenuates the high freq. component. Thus ( $f_s + f_0$ ) component is removed by the low pass filter & new error v/g  $V_e'(t)$  is obtained.

→ This signal is amplified & is given as the control input to the VCO so that the freq.

freq. of VCO approaches the freq. of incoming signal. This mode of operation when the VCO freq. changes & approaches the incoming signal freq. is called capture mode.

→ When two ilps to the phase detector are equal, the o/p of phase detector has an error voltage which is just sufficient to keep the VCO operate at the frequency of the incoming signal  $f_s$ . This mode of operation is lock mode.

→ The design of VCO should be such that  $f_{st} - f_0$  &  $f_s - f_0$  component are significantly apart. The action of loop is to make 'O' take just that value which is required to generate the DC control vlg necessary to change the frequency of VCO from its free running value to the frequency of the incoming signal.

This allows the PLL to track any frequency changes of the ilp signal, once the lock have been acquired.

Lock Range: The range of frequencies of the ilp signal over which a PLL can maintain lock is called lock range.

Capture Range: The range of frequencies of ilp signal over which a PLL can acquire lock is called the capture range.

The greatest capture range possible is equal to lock range but capture range is less than lock range.

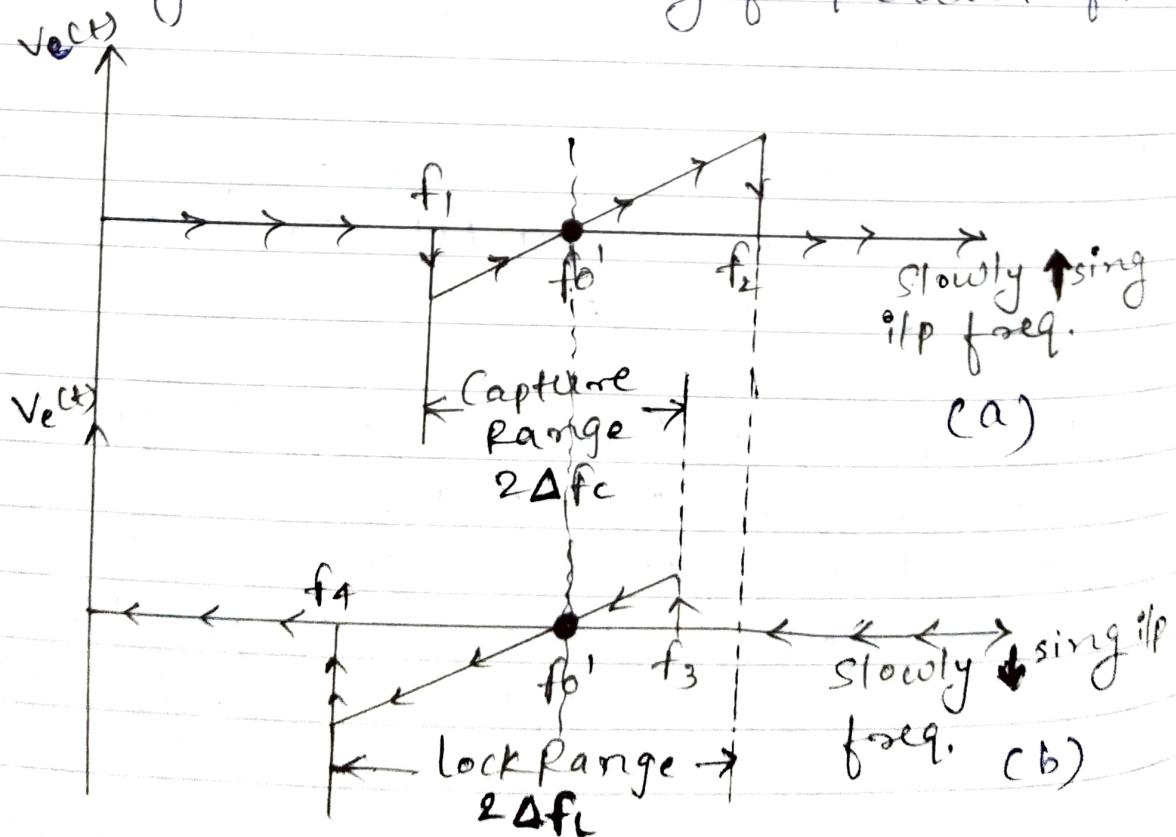
→ The capture of an i/p signal does not take place as soon as the signal is applied but takes finite time, called pull-in-time. It depends on the initial frequency & phase difference between the i/p & vco signal as well as on the overall loop gain.

→ Phase detector compares the i/p freq. & vco freq. & generates a d.c. voltage that is proportional to the phase difference between two frequencies.

It is classified as Analog & Digital.

## \* Transfer characteristics

When PLL is in lock, a frequency shift at the i/p is transferred to voltage level shift at the vco control terminal. The following chart shows vlg freq. chara. of PLL.



→ The i/p is assumed to be sine wave, whose freq. is slowly swept over a broad frequency range & the vertical axis corresponds to the error voltage  $V_e(t)$ .

In fig (a) the incoming i/p freq. is slowly rising. The loop does not respond till the i/p freq. reaches  $f_1$ .

This frequency  $f_1$  corresponds to the lower edge of the capture range. After this, the loop immediately locks on to the i/p signal causing a-ve jump of error voltage. As the i/p signal freq. is further increased beyond  $f_1$ ,  $V_e(t)$  varies with freq. with slope equal to the reciprocal of the VCO gain,  $\frac{1}{k}$  & goes +ve when i/p frequency is greater than VCO freq. The loop tracks the i/p until the i/p freq. reaches  $f_2$  which corresponds to upper edge of the lock range. Then the PLL loses track of i/p freq. It is no more in the lock state.

If the i/p frequency is slowly swept back, the cycle repeats itself. The PLL recaptures signal of freq.  $f_3$  & traces it down to freq.  $f_4$ .  $f_3$  is called upper edge of capture range &  $f_4$  is the lower edge of lock range.

The frequency range between  $f_1$  &  $f_3$  corresponds to the total capture range,

$$\text{ie. } f_3 - f_1 = 2\Delta f_c \text{ &}$$

freq. range between  $f_2$  &  $f_4$  corresponds to total lock range  $f_2 - f_4 = 8\Delta f_L$

Example of the input freq. The multiplying factor being governed by scaling factor of the  $\frac{1}{N}$  counter.

## \* Phase locked loop (IC 565)

### → features

- 200 ppm/°C freq. stability of the VCO.
- Power supply range of  $\pm 5$  to  $\pm 12$  V
- TTL & DTL compatible phase detector i/p & square wave o/p.

Adjustable hold in range ~~from~~ of  $\pm 1\%$  to  $> \pm 60\%$ .

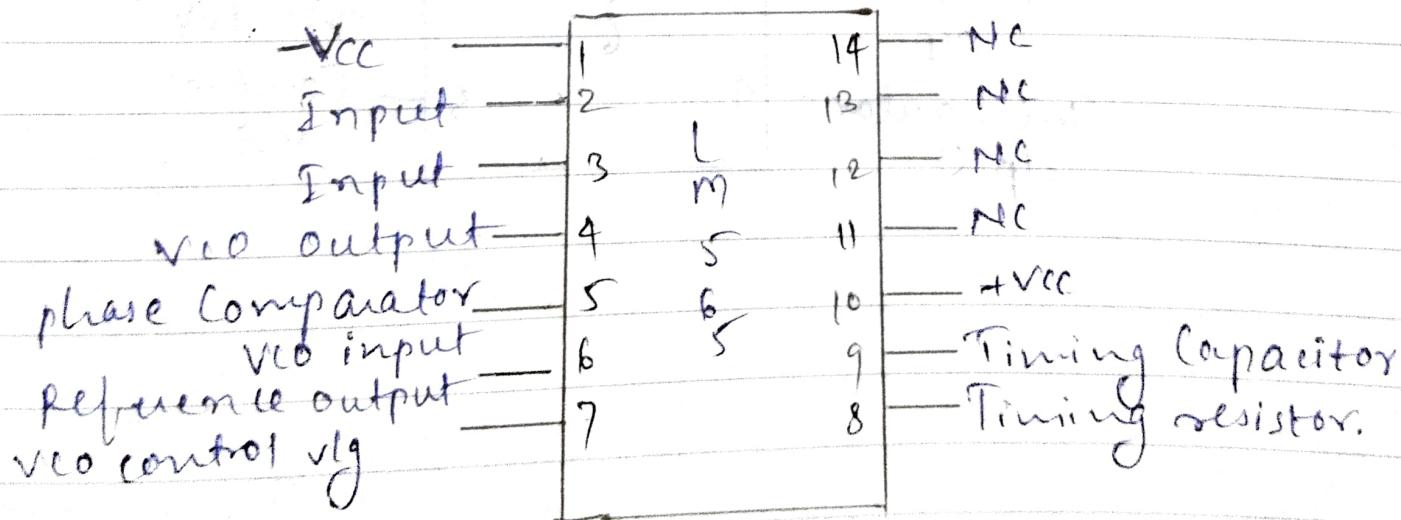
### → Application

- Data ~~synchronization~~ synchronization
- Modems
- FSK demodulation
- FM demodulation
- Freq. synthesizer
- Tone decoding.
- PIN diagram.

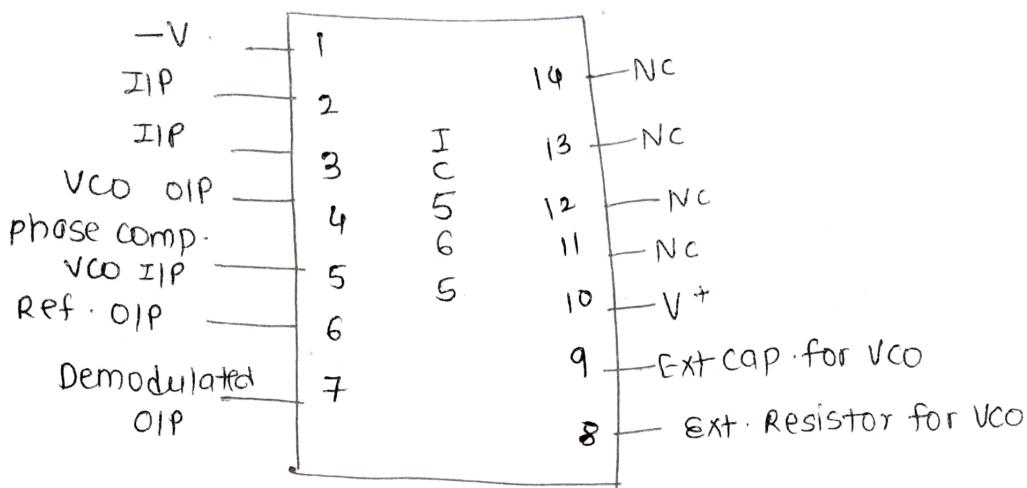
$$\text{Free running freq. } (f_0) = \frac{0.25}{R T C T}$$

$$\text{Lock range} = \pm \frac{8 f_0}{V}$$

$$\text{Capture range} = \pm \sqrt{\frac{f_i}{2 \pi \times 3.6 \times 10^3 \times C}}$$



# pin dia of IC 565 :-



## Specifications :-

- 1) operating freq<sup>n</sup> range : 0.001 Hz to 500 kHz
- 2) operating utg. range :  $\pm 6$  to  $\pm 12$  V
- 3) IIP impedance :  $10\text{ k}\Omega$ .
- 4) OIP sink current =  $1\text{ mA}$
- 5) OIP source current =  $10\text{ mA}$ .
- 6) Triangular wave amplitude =  $2.4\text{ Vpp}$  at  $\pm 6\text{ V}$
- 7) Sq. wave amplitude =  $5.4\text{ Vpp}$  at  $\pm 6\text{ V}$ .
- 8) BW adj range  $\rightarrow \leq \pm 1$  to  $> \pm 60\%$ .

$$f_{out} \cong \frac{1.2}{4R_1C_1} \text{ Hz.}$$

$$-f_L \rightarrow \text{lock range} \rightarrow \pm \frac{8f_{out}}{V} \text{ Hz.}$$

where  $f_{out} \rightarrow$  free running freq<sup>n</sup> of VCO

$$V = (+V) - (-V)$$

& capture range ,

$$f_C = \pm \left[ \frac{f_L}{2\pi \times 3.6 \times 10^3 \times C^2} \right]^{1/2}$$

1)  $f_L \uparrow, \uparrow V_{in}$  &  $f_L \downarrow, \uparrow V$

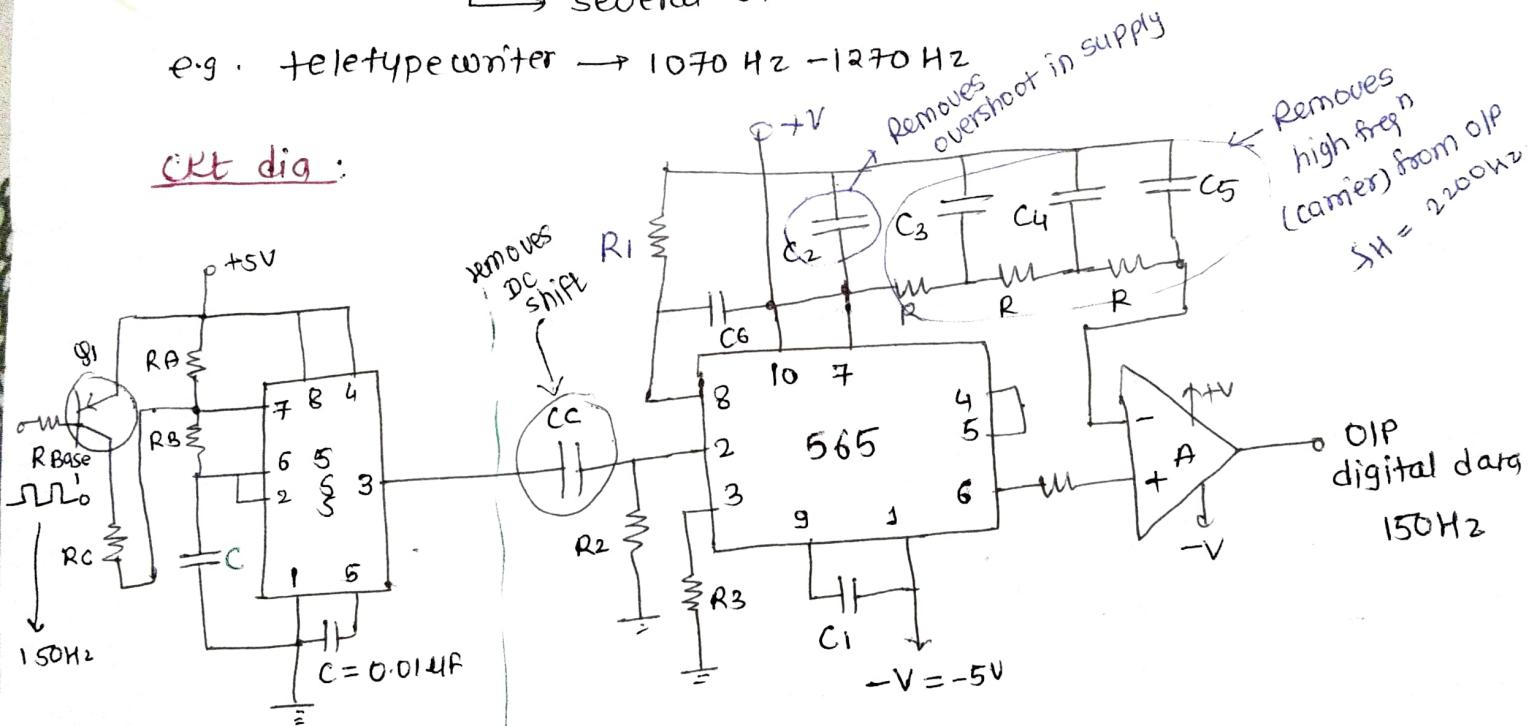
## IC 565 as FSK demodulator :-

- In wireless comm<sup>n</sup> → binary data or code is transmitted by means of a carrier freq<sup>n</sup> that is shifted bet<sup>n</sup> two preset freq<sup>n</sup>s.  
 ∵ Carrier freq<sup>n</sup> is shifted bet<sup>n</sup> two preset freq<sup>n</sup>s, the data transmission is said to use a freq<sup>n</sup> shift keying (FSK) tech.
- In 565 → freq<sup>n</sup> shift is accomplished by driving a VCO with the binary data signal so that two resulting freq<sup>n</sup>s correspond to the logic 0 or logic 1 states of binary signal.
- 1 → mark, 0 → space ← commonly called.  
 ↪ several std. used to decide these freq<sup>n</sup>s.

e.g. teletypewriter → 1070 Hz - 1270 Hz

removes overshoot in supply  
 removes high freq<sup>n</sup> (carrier) from o/p  
 $SH = 2200\text{Hz}$

### Ckt dig:



← FSK generator →

(555-astable mode)  
 $f \rightarrow Q_1$

when I/P  $\rightarrow 1$   $Q_1 \rightarrow$  off  
 555 → astable - C charges.

$V_C \rightarrow \frac{2}{3} V_{cc}$  & discharge to  $\frac{1}{3} V_{cc}$

when I/P = 1

$$f_0 = \frac{1.44}{(RA + 2RB) \cdot C} \leftarrow \text{mark freqn.}$$

when I/P = 0

$Q_1 \rightarrow$  ON,  $RC$  q/c  $RA(RA||Rc)$ .



↓ charging time of 'C'

$\therefore f_0 \uparrow$  given by

$$f_0 = \frac{1.44}{[(RA||Rc) + 2RB] \cdot C} \leftarrow \text{space freqn.}$$

if<sup>n</sup> bet<sup>n</sup> mark & space  $\rightarrow$  freq<sup>n</sup> shift.  
OIP of 555  $\rightarrow$  565 (FSR demodulator)  $\rightarrow$  cap. coupling used at IIP to remove dc shift.  
As IIP applied  $\rightarrow$  565  $\rightarrow$  loop locks to fin & tracks it bet<sup>n</sup> too freq. with corresponding dc shift at the oip.

$\rightarrow R_1, C_1 \rightarrow$  free running freq<sup>n</sup> of VCO

$C_2 \rightarrow$  loop filter cap establishes dynamic char. of demod.

$\rightarrow$  must be < usual  $\Leftarrow$  to remove overshoot on the oip pulse.

$\rightarrow$  3 stage RC (LPF)  $\rightarrow$  remove carrier from oip.

$$f_H = 1/2\pi R_C \approx 2200 \text{ Hz}$$

$\rightarrow$  OIP 150 Hz  $\rightarrow$  made compatible by using vtg. comparator bet<sup>n</sup> oip af filter & pin 6 of PLL.

$\rightarrow$  VCO freq<sup>n</sup> is adj. with  $R_1$  so that at  $f_{in} = 1070 \text{ Hz}$  a slightly positive vtg. is obtained at the oip.

pin 7  $\rightarrow$  Demodulated oip  $\rightarrow$  3 stage filter  $\xrightarrow{\text{LPF}}$  removes high freq<sup>n</sup> from oip.  
(carrier) (2200Hz).

comparator  $\rightarrow$  make 150Hz gp compatible

pin 6  $\rightarrow$  Ref oip  $\rightarrow$