

## 4.1 THE MOSFET AMPLIFIER

**Objective:** • Investigate the process by which a single-transistor circuit can amplify a small, time-varying input signal and develop the small-signal models of the transistor that are used in the analysis of linear amplifiers.

In this chapter, we will be considering **signals**, **analog circuits**, and **amplifiers**. A signal contains some type of information. For example, sound waves produced by a speaking human contain the information the person is conveying to another person. A sound wave is an analog signal. In this chapter, we are interested in electrical analog signals. The electrical signals are in the form of time-varying currents and voltages.

The magnitude of an **analog signal** can take on any value, within limits, and may vary continuously with time. Electronic circuits that process analog signals are called **analog circuits**. One example of an analog circuit is a **linear amplifier**. A **linear amplifier** magnifies an input signal and produces an output signal whose magnitude is larger and directly proportional to the input signal.

In this chapter, we analyze and design linear amplifiers that use field-effect transistors as the amplifying device. The term **small signal** means that we can linearize the ac equivalent circuit. We will define what is meant by small signal in the case of MOSFET circuits. The term **linear amplifiers** means that we can use superposition so that the dc analysis and ac analysis of the circuits can be performed separately and the total response is the sum of the two individual responses.

The mechanism with which MOSFET circuits amplify small time-varying signals was introduced in the last chapter. In this section, we will expand that discussion using the graphical technique, dc load line, and ac load line. In the process, we will develop the various small-signal parameters of linear circuits and the corresponding equivalent circuits.

### 4.1.1

#### Graphical Analysis, Load Lines, and Small-Signal Parameters

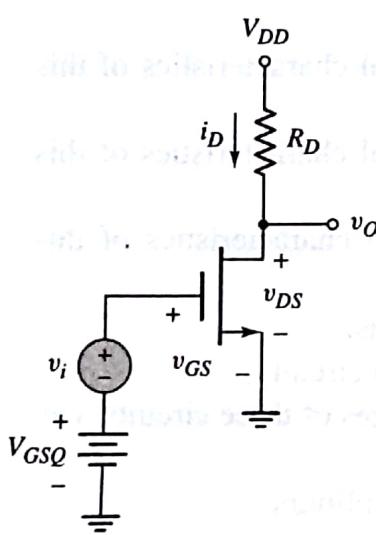
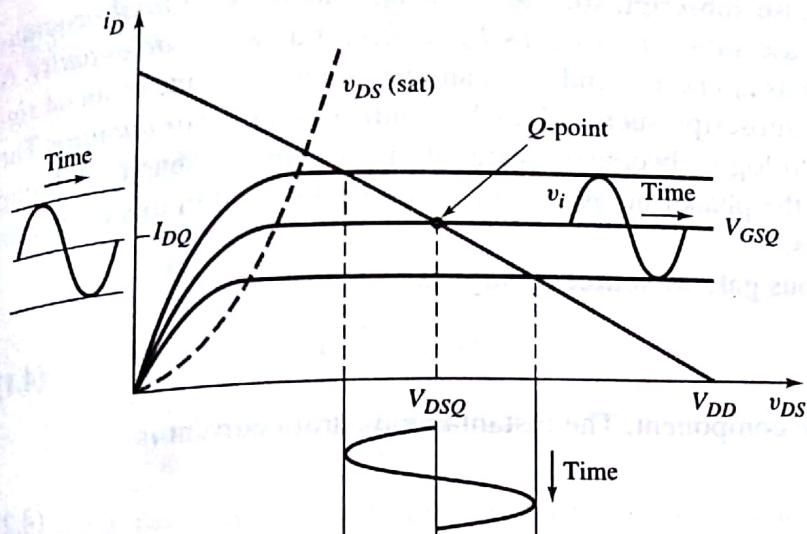


Figure 4.1 NMOS common-source circuit with time-varying signal source in series with gate dc source

Figure 4.1 shows an NMOS common-source circuit with a time-varying voltage source in series with the dc source. We assume the time-varying input signal is sinusoidal. Figure 4.2 shows the transistor characteristics, dc load line, and *Q*-point, where the dc load line and *Q*-point are functions of  $v_{GS}$ ,  $V_{DD}$ ,  $R_D$ , and the transistor parameters. For the output voltage to be a linear function of the input voltage, the transistor must be biased in the saturation region. (Note that, although we primarily use n-channel, enhancement-mode MOSFETs in our discussions, the same results apply to the other MOSFETs.)

Also shown in Figure 4.2 are the sinusoidal variations in the gate-to-source voltage, drain current, and drain-to-source voltage, as a result of the sinusoidal source  $v_i$ . The total gate-to-source voltage is the sum of  $V_{GSQ}$  and  $v_i$ . As  $v_i$  increases, the instantaneous value of  $v_{GS}$  increases, and the bias point moves up the load line. A larger value of  $v_{GS}$  means a larger drain current and a smaller value of  $v_{DS}$ . For a negative  $v_i$  (the negative portion of the sine wave), the instantaneous value of  $v_{GS}$  decreases below the quiescent value, and the bias point



**Figure 4.2** Common-source transistor characteristics, dc load line, and sinusoidal variation in gate-to-source voltage, drain current, and drain-to-source voltage

moves down the load line. A smaller  $v_{GS}$  value means a smaller drain current and increased value of  $v_{DS}$ . Once the  $Q$ -point is established, we can develop a mathematical model for the sinusoidal, or small-signal, variations in gate-to-source voltage, drain-to-source voltage, and drain current.

The time-varying signal source  $v_i$  in Figure 4.1 generates a time-varying component of the gate-to-source voltage. In this case,  $v_{gs} = v_i$ , where  $v_{gs}$  is the time-varying component of the gate-to-source voltage. For the FET to operate as a linear amplifier, the transistor must be biased in the saturation region, and the instantaneous drain current and drain-to-source voltage must also be confined to the saturation region.

When symmetrical sinusoidal signals are applied to the input of an amplifier, symmetrical sinusoidal signals are generated at the output, as long as the amplifier operation remains linear. We can use the load line to determine the maximum output symmetrical swing. If the output exceeds this limit, a portion of the output signal will be clipped and signal distortion will occur.

In the case of FET amplifiers, the output signal must avoid cutoff ( $i_D = 0$ ) and must stay in the saturation region ( $v_{DS} > v_{DS}(\text{sat})$ ). This maximum range of output signal can be determined from the load line in Figure 4.2.

### Transistor Parameters

We will be dealing with time-varying as well as dc currents and voltages in this chapter. Table 4.1 gives a summary of notation that will be used. This notation was discussed in the Prologue, but is repeated here for

**Table 4.1** Summary of notation

Variable	Meaning
$i_D, v_{GS}$	Total instantaneous values
$I_D, V_{GS}$	DC values
$i_d, v_{gs}$	Instantaneous ac values
$I_d, V_{gs}$	Phasor values

convenience. A lowercase letter with an upper case subscript, such as  $i_D$  or  $v_{GS}$ , indicates a *total instantaneous value*. An uppercase letter with an uppercase subscript, such as  $I_D$  or  $V_{GS}$ , indicates a *dc quantity*. A lowercase letter with a lowercase subscript, such as  $i_d$  and  $v_{gs}$ , indicates an instantaneous value of an *ac signal*. Finally, an uppercase letter with a lowercase subscript, such as  $I_d$  or  $V_{gs}$ , indicates a *phasor quantity*. The phasor notation, which is also reviewed in the Prologue, becomes especially important in Chapter 7 during the discussion of frequency response. However, the phasor notation will generally be used in this chapter in order to be consistent with the overall ac analysis.

From Figure 4.1, we see that the instantaneous gate-to-source voltage is

$$v_{GS} = V_{GSQ} + v_i = V_{GSQ} + v_{gs} \quad (4.1)$$

where  $V_{GSQ}$  is the dc component and  $v_{gs}$  is the ac component. The instantaneous drain current is

$$i_D = K_n(v_{GS} - V_{TN})^2 \quad (4.2)$$

Substituting Equation (4.1) into (4.2) produces

$$i_D = K_n[V_{GSQ} + v_{gs} - V_{TN}]^2 = K_n[(V_{GSQ} - V_{TN}) + v_{gs}]^2 \quad (4.3(a))$$

or

$$i_D = K_n(V_{GSQ} - V_{TN})^2 + 2K_n(V_{GSQ} - V_{TN})v_{gs} + K_n v_{gs}^2 \quad (4.3(b))$$

The first term in Equation (4.3(b)) is the dc or quiescent drain current  $I_{DQ}$ , the second term is the time-varying drain current component that is linearly related to the signal  $v_{gs}$ , and the third term is proportional to the square of the signal voltage. For a sinusoidal input signal, the squared term produces undesirable harmonics, or nonlinear distortion, in the output voltage. To minimize these harmonics, we require

$$v_{gs} \ll 2(V_{GSQ} - V_{TN}) \quad (4.4)$$

which means that the third term in Equation (4.3(b)) will be much smaller than the second term. *Equation (4.4) represents the small-signal condition that must be satisfied for linear amplifiers.*

Neglecting the  $v_{gs}^2$  term, we can write Equation (4.3(b))

$$i_D = I_{DQ} + i_d \quad (4.5)$$

Again, small-signal implies linearity so that the total current can be separated into a dc component and an ac component. The ac component of the drain current is given by

$$i_d = 2K_n(V_{GSQ} - V_{TN})v_{gs} \quad (4.6)$$

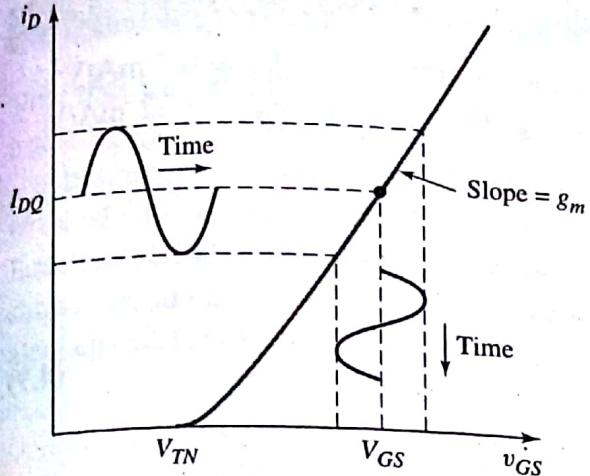
The small-signal drain current is related to the small-signal gate-to-source voltage by the transconductance  $g_m$ . The relationship is

$$g_m = \frac{i_d}{v_{gs}} = 2K_n(V_{GSQ} - V_{TN}) \quad (4.7)$$

The transconductance is a transfer coefficient relating output current to input voltage and can be thought of as representing the gain of the transistor.

The transconductance can also be obtained from the derivative

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS}=V_{GSQ}=\text{const.}} = 2K_n(V_{GSQ} - V_{TN}) \quad (4.8(a))$$



**Figure 4.3** Drain current versus gate-to-source voltage characteristics, with superimposed sinusoidal signals

which can be written

$$g_m = 2\sqrt{K_n I_{DQ}} \quad (4.8(b))$$

The drain current versus gate-to-source voltage for the transistor biased in the saturation region is given in Equation (4.2) and is shown in Figure 4.3. The transconductance  $g_m$  is the slope of the curve. If the time-varying signal  $v_{gs}$  is sufficiently small, the transconductance  $g_m$  is a constant. With the  $Q$ -point in the saturation region, the transistor operates as a current source that is linearly controlled by  $v_{gs}$ . If the  $Q$ -point moves into the nonsaturation region, the transistor no longer operates as a linearly controlled current source.

As shown in Equation (4.8(a)), the transconductance is directly proportional to the conduction parameter  $K_n$ , which in turn is a function of the width-to-length ratio. Therefore, increasing the width of the transistor increases the transconductance, or gain, of the transistor.

### EXAMPLE 4.1

**Objective:** Calculate the transconductance of an n-channel MOSFET.

Consider an n-channel MOSFET with parameters  $V_{TN} = 1$  V,  $(\frac{1}{2}) \mu_n C_{ox} = 20 \mu\text{A/V}^2$ , and  $W/L = 40$ . Assume the drain current is  $I_D = 1$  mA.

**Solution:** The conduction parameter is

$$K_n = \left( \frac{1}{2} \mu_n C_{ox} \right) \left( \frac{W}{L} \right) = (20)(40) \mu\text{A/V}^2 \Rightarrow 0.80 \text{ mA/V}^2$$

Assuming the transistor is biased in the saturation region, the transconductance is determined from Equation (4.8(b)),

$$g_m = 2\sqrt{K_n I_{DQ}} = 2\sqrt{(0.8)(1)} = 1.79 \text{ mA/V}$$

**Comment:** The transconductance of a bipolar transistor is  $g_m = (I_{CQ}/V_T)$ , which is 38.5 mA/V for a collector current of 1 mA. The transconductance values of MOSFETs tend to be small compared to those of BJTs. However, the advantages of MOSFETs include high input impedance, small size, and low power dissipation.

## 4.1.2

## Small-Signal Equivalent Circuit

Now that we have the ac equivalent circuit for the NMOS amplifier circuit, (Figure 4.4), we must develop a small-signal equivalent circuit for the transistor.

Initially, we assume that the signal frequency is sufficiently low so that any capacitance at the gate terminal can be neglected. The input to the gate thus appears as an open circuit, or an infinite resistance. Equation (4.14) relates the small-signal drain current to the small-signal input voltage, and Equation (4.7) shows that the transconductance  $g_m$  is a function of the  $Q$ -point. The resulting simplified small-signal equivalent circuit for the NMOS device is shown in Figure 4.5. (The phasor components are in parentheses.)

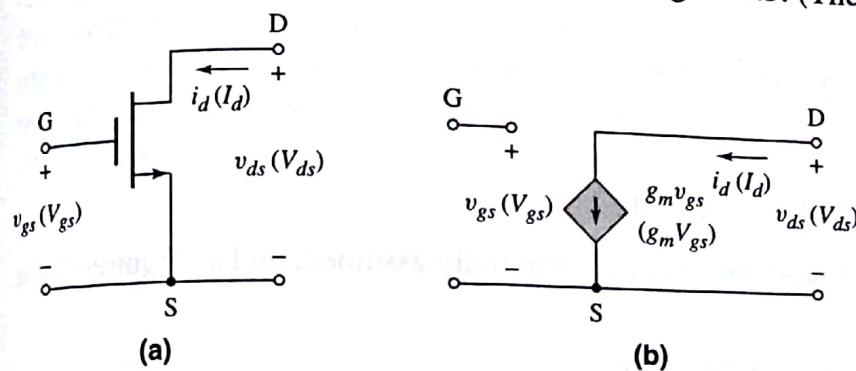


Figure 4.5 (a) Common-source NMOS transistor with small-signal parameters and (b) simplified small-signal equivalent circuit for NMOS transistor

This small-signal equivalent circuit can also be expanded to take into account the finite output resistance of a MOSFET biased in the saturation region. This effect, discussed in the last chapter, is a result of the nonzero slope in the  $i_D$  versus  $v_{DS}$  curve.

We know that

$$i_D = K_n [(v_{GS} - V_{TN})^2 (1 + \lambda v_{DS})] \quad (4.16)$$

where  $\lambda$  is the channel-length modulation parameter and is a positive quantity.

The small-signal output resistance, as previously defined, is

$$r_o = \left( \frac{\partial i_D}{\partial v_{DS}} \right)^{-1} \Big|_{v_{GS}=V_{GSQ}=\text{const.}} \quad (4.17)$$

or

$$r_o = [\lambda K_n (V_{GSQ} - V_{TN})^2]^{-1} \cong [\lambda I_{DQ}]^{-1} \quad (4.18)$$

This small-signal output resistance is also a function of the  $Q$ -point parameters.

The expanded small-signal equivalent circuit of the n-channel MOSFET is shown in Figure 4.6 in phasor notation. Note that this equivalent circuit is a transconductance amplifier in that the input signal is a voltage and the output signal is a current. This equivalent circuit can now be inserted into the amplifier ac equivalent circuit in Figure 4.4 to produce the circuit in Figure 4.7.

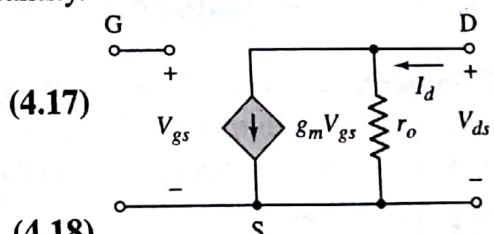


Figure 4.6 Expanded small-signal equivalent circuit, including output resistance, for NMOS transistor

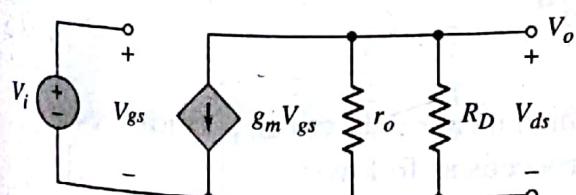


Figure 4.7 Small-signal equivalent circuit of common-source circuit with NMOS transistor model

**EXAMPLE 4.2**

**Objective:** Determine the small-signal voltage gain of a MOSFET circuit.

For the circuit in Figure 4.1, assume parameters are:  $V_{GSQ} = 2.12$  V,  $V_{DD} = 5$  V, and  $R_D = 2.5$  k $\Omega$ . Assume transistor parameters are:  $V_{TN} = 1$  V,  $K_n = 0.80$  mA/V $^2$ , and  $\lambda = 0.02$  V $^{-1}$ . Assume the transistor is biased in the saturation region.

**Solution:** The quiescent values are

$$I_{DQ} \cong K_n(V_{GSQ} - V_{TN})^2 = (0.8)(2.12 - 1)^2 = 1.0 \text{ mA}$$

and

$$V_{DSQ} = V_{DD} - I_{DQ}R_D = 5 - (1)(2.5) = 2.5 \text{ V}$$

Therefore,

$$V_{DSQ} = 2.5 \text{ V} > V_{DS(\text{sat})} = V_{GS} - V_{TN} = 1.82 - 1 = 0.82 \text{ V}$$

which means that the transistor is biased in the saturation region, as initially assumed, and as required for a linear amplifier. The transconductance is

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(0.8)(2.12 - 1) = 1.79 \text{ mA/V}$$

and the output resistance is

$$r_o = [\lambda I_{DQ}]^{-1} = [(0.02)(1)]^{-1} = 50 \text{ k}\Omega$$

From Figure 4.7, the output voltage is

$$V_o = -g_m V_{gs}(r_o \parallel R_D)$$

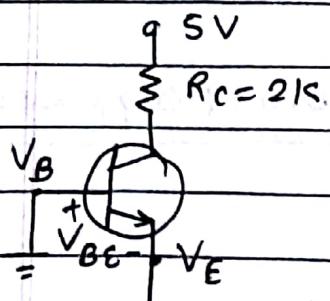
Since  $V_{gs} = V_i$ , the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \parallel R_d) = -(1.79)(50 \parallel 2.5) = -4.26$$

**Comment:** Because of the relatively low value of transconductance, MOSFET circuits tend to have a relatively low value of small-signal voltage gain. Note that the small-signal voltage gain contains a minus sign, which means that the sinusoidal output voltage is 180 degrees out of phase with respect to the input sinusoidal signal.

soln

$$\beta = 120 \text{ & } V_A = \infty$$



Step ① Determine  $V_{CEQ}$  -

$$\text{let } I_C = I_Q = 1 \text{ mA}$$

$$V_C = 5 - I_Q R_C$$

$$= 5 - (1 \times 2)$$

$$\underline{\underline{V_C = 3 \text{ V}}}$$

$$I_Q = 1 \text{ mA}$$

$$5 \text{ V}$$

$$V_E = V_B - V_{BE} = 0 - 0.7 = -0.7 \text{ V}$$

$$V_{CE} = V_C - V_E = 3 - (-0.7) = \underline{\underline{3.7 \text{ V}}}$$

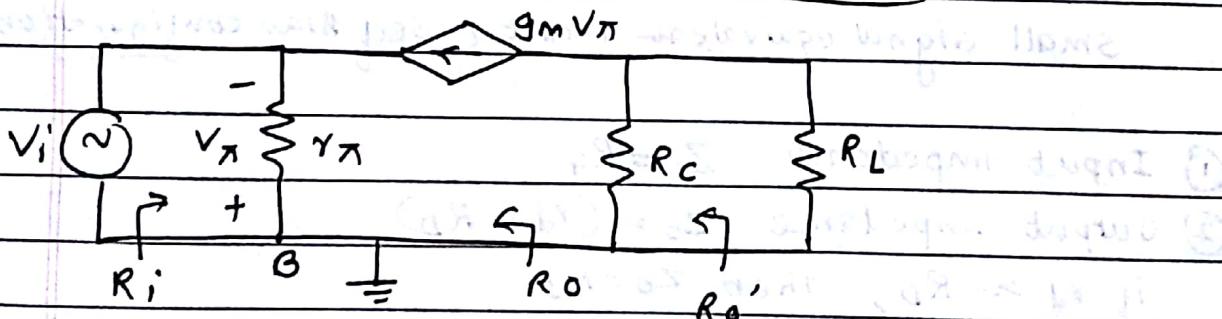
Step ② Find  $\gamma_\pi$ ,  $g_m$  &  $\gamma_o$

$$\gamma_\pi = \frac{V_T \beta}{I_{CQ}} = \frac{26 \times 120}{1} = 3.12 \text{ k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1 \text{ mA}}{26 \times 10^{-3} \text{ V}} = 38.46 \text{ mA/V}$$

$$\gamma_o = \frac{V_A}{I_{CQ}} = \infty$$

Step ③ find voltage gain  $A_V$ ,  $R_i$  &  $R_o$



$$A_V = \frac{V_o}{V_i} = \frac{-g_m V_\pi (R_C \parallel R_L)}{-V_\pi} = g_m (R_C \parallel R_L) = 38.46 (2 \parallel 10) = \boxed{A_V = 64.1}$$

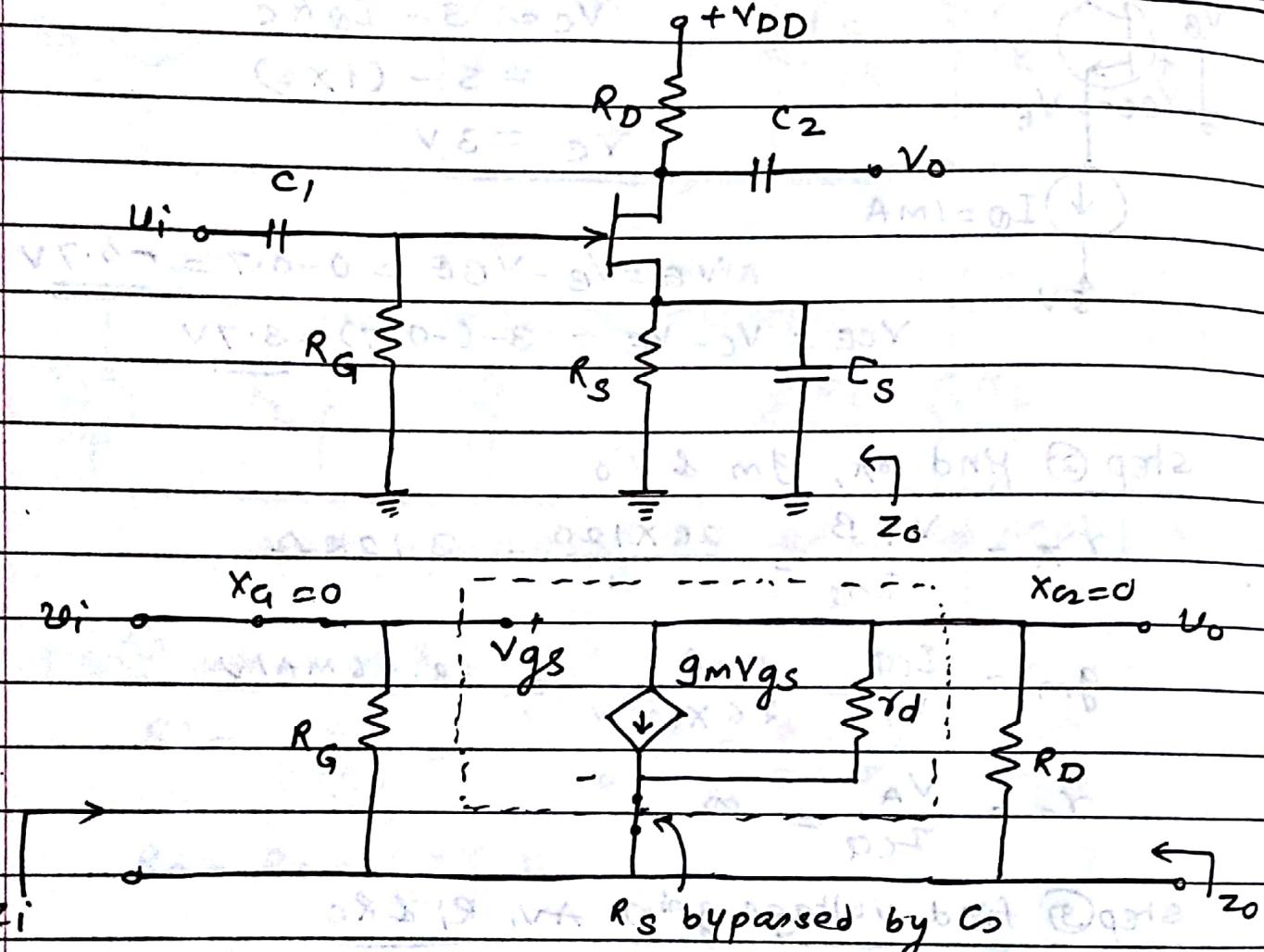
$$R_i' = \frac{V_\pi}{(1 + \beta)} = \frac{3120}{121} = \underline{\underline{2579 \Omega}}$$

$$R_o = \infty$$

$$R_o' = R_C \parallel R_L = (2 \parallel 10) = \underline{\underline{1.67 \text{ k}\Omega}}$$

# small signal Analysis of JFET Amplifiers

## \* Common Source Amplifier with self Bias (Bypassed $R_s$ ):



small signal equivalent circuit of self bias configuration

① Input impedance  $Z_i = R_G$

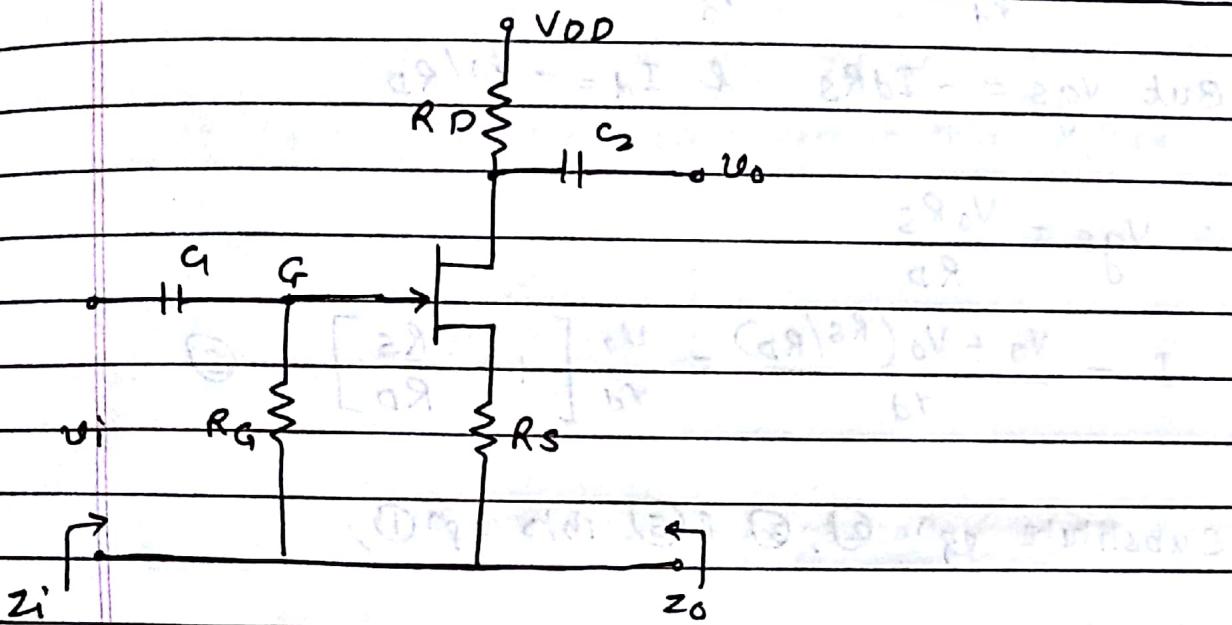
② Output impedance  $z_o = (r_d \parallel R_D)$

if  $r_d \gg R_D$ , then  $z_o = R_D$

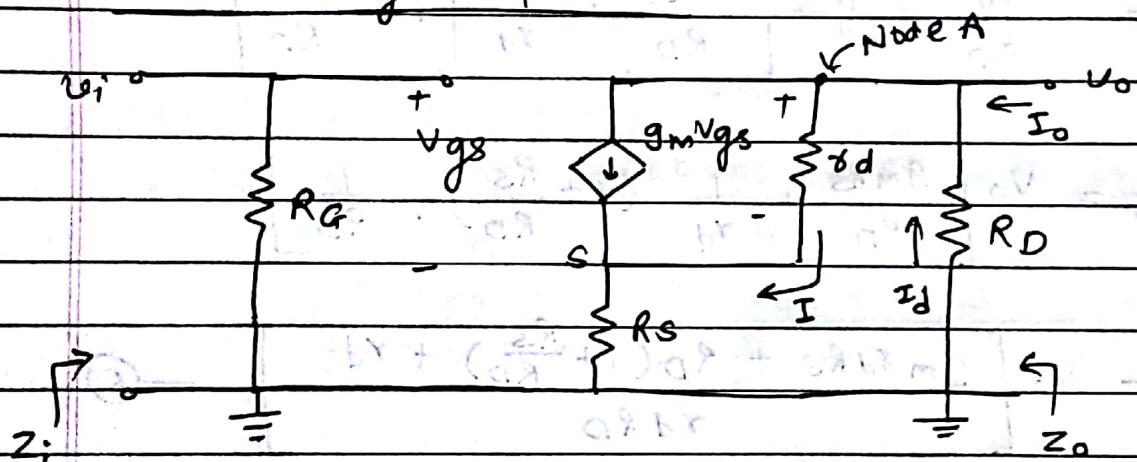
③ Voltage gain  $A_v = -g_m (r_d \parallel R_D)$

for  $r_d \gg R_D$ ,  $A_v = -g_m R_D$

\* CS JFET Amplifier with self Bias (Unbypassed  $R_s$ ) :-



DRAW small signal equivalent



step① input impedance ( $Z_i$ ) :-  $Z_i = R_G$

step② output impedance ( $Z_o$ ) :-

Put  $V_i = 0$  when JFET is short circuited.

$$Z_o = \frac{U_o}{I_o} \quad \text{Apply KCL at node A,}$$

$$I_o + I_d = g_m V_{gs} + I \quad \text{--- (1)}$$

$$\therefore I_d = -\frac{U_o}{R_D} \quad \text{--- (2)}$$

$$g_m V_{gs} = g_m (-I_d R_s) \quad \therefore V_{gs} = -I_d R_s$$

$$g_m V_{gs} = g_m \left[ \frac{U_o}{R_D} \cdot R_s \right] \quad \text{--- (3)} \quad \text{as } I_d = -\frac{U_o}{R_D}$$

$$\& I = \frac{V_{rd}}{R_D} \quad \text{But } V_{rd} = U_o - V_{sg}$$

$$I = \frac{V_o - V_{sg}}{r_d} = \frac{V_o + V_{gs}}{r_d} \quad (4)$$

But  $V_{gs} = -I_d R_s$  &  $I_d = -V_o / R_D$

$$\therefore V_{gs} = \frac{V_o R_s}{R_D}$$

$$I = \frac{V_o + V_o (R_s/R_D)}{r_d} = \frac{V_o}{r_d} \left[ 1 + \frac{R_s}{R_D} \right] \quad (5)$$

Substitute eqn ②, ③ & ⑤ into eqn ①,

$$I_o = \frac{V_o}{R_D} = g_m \left[ \frac{V_o R_s}{R_D} \right] + \frac{V_o}{r_d} \left[ 1 + \frac{R_s}{R_D} \right]$$

$$I_o = \frac{V_o}{R_D} \left[ g_m R_s + \frac{1}{r_d} \cdot \left( 1 + \frac{R_s}{R_D} \right) + \frac{1}{R_D} \right]$$

$$= \frac{V_o}{r_d R_D} \left[ g_m r_d R_s + R_D \left( 1 + \frac{R_s}{R_D} \right) + r_d \right] \quad (6)$$

$$= \frac{V_o}{r_d R_D} \left[ \mu R_s + R_D + R_s + r_d \right]$$

$$= \frac{V_o}{r_d R_D} \left[ R_D + r_d + (1 + \mu) R_s \right]$$

$$Z_o = \frac{V_o}{I_o} = \frac{R_D r_d}{R_D + r_d + (1 + \mu) R_s} \quad \text{Exact expression}$$

Consider eqn ⑥,

$$T_o = V_o \left[ \frac{g_m r_d R_s + (R_D + R_s + r_d)}{r_d R_D} \right]$$

$$Z_o = \frac{V_o}{I_o} = \frac{r_d R_D}{g_m r_d R_s + R_D + R_s + r_d} \quad \text{Divide N & D by } r_d$$

$$Z_o = \frac{R_D}{1 + g_m R_S + \left( \frac{R_D + R_S}{r_d} \right)}$$

If  $r_d \gg (R_D + R_S)$  last term in this eqn can be neglected

$$Z_o \approx \frac{R_D}{1 + g_m R_S}$$

#### Step ④ Expression for Voltage gain ( $A_v$ )

$$A_v = \frac{V_o}{V_i}$$

$$V_o = \text{Voltage across } R_D = -I_d R_D \quad \text{--- (7)}$$

first we find expression for  $I_d$ .

referring AC equivalent ckt, apply KVL to gfp ckt

$$V_i - V_{gs} - V_{RS} = 0$$

$$\therefore V_i = V_{gs} + V_{RS} = V_{gs} + I_d R_S$$

$$\therefore V_{gs} = V_i - I_d R_S \quad \& \quad V_S = I_d R_S \text{ we get,}$$

$$I_d = g_m V_{gs} + I = g_m V_{gs} + \frac{V_o - U_S}{r_d}$$

substitute  $V_{gs} = V_i - I_d R_S \quad \& \quad V_S = I_d R_S$  we get,

$$I_d = g_m [V_i - I_d R_S] + \frac{V_o - I_d R_S}{r_d}$$

$$= g_m V_i - g_m I_d R_S + \frac{V_o}{r_d} - \frac{I_d R_S}{r_d}$$

$$I_d = \frac{g_m r_d V_i - g_m r_d I_d R_S + V_o - I_d R_S}{r_d}$$

substitute  $V_o = -I_d R_D$

$$\therefore I_d r_d = g_m r_d V_i - g_m r_d I_d R_S - I_d R_D - I_d R_S$$

$$I_d [r_d + g_m r_d R_S + R_D + R_S] = g_m r_d V_i \quad \text{But } g_m r_d = u$$

$$\therefore I_d [r_d + R_D + (1+u) R_S] = u V_i$$

$$\therefore I_d = \frac{uV_i}{r_d + R_D + (1+u)R_S} \quad \text{Put in eqn ②}$$

$$U_0 = \frac{-\mu V_{RD}}{R_d + R_D + (1+\mu)R_S}$$

$\text{Voltage gain } A_v = \frac{U_o}{U_i} = \frac{-N R_D}{\tau_d + R_D + (1+N) R_S}$	Exact expression
--	---------------------

Approximate expression :- (for Av)

We know  $v_i = v_{gs} + IdR_s$

neglecting  $r_d$ , we can write,  $I_d = g_m V_{GS}$

$$\therefore V_{GS} = \frac{I_D}{g_m}$$

$$V_i = \frac{Id}{g_m} + IdR_S = Id \left[ \frac{1}{g_m} + R_S \right]$$

$$\therefore I_d = \frac{V_i}{[(Y_{gm}) + R_s]} = \frac{g_m V_i}{1 + g_m R_s} \quad (8)$$

Output Voltage  $V_o = -I_d R_D$  Put  $I_d$  from eq<sup>n</sup> ⑧,

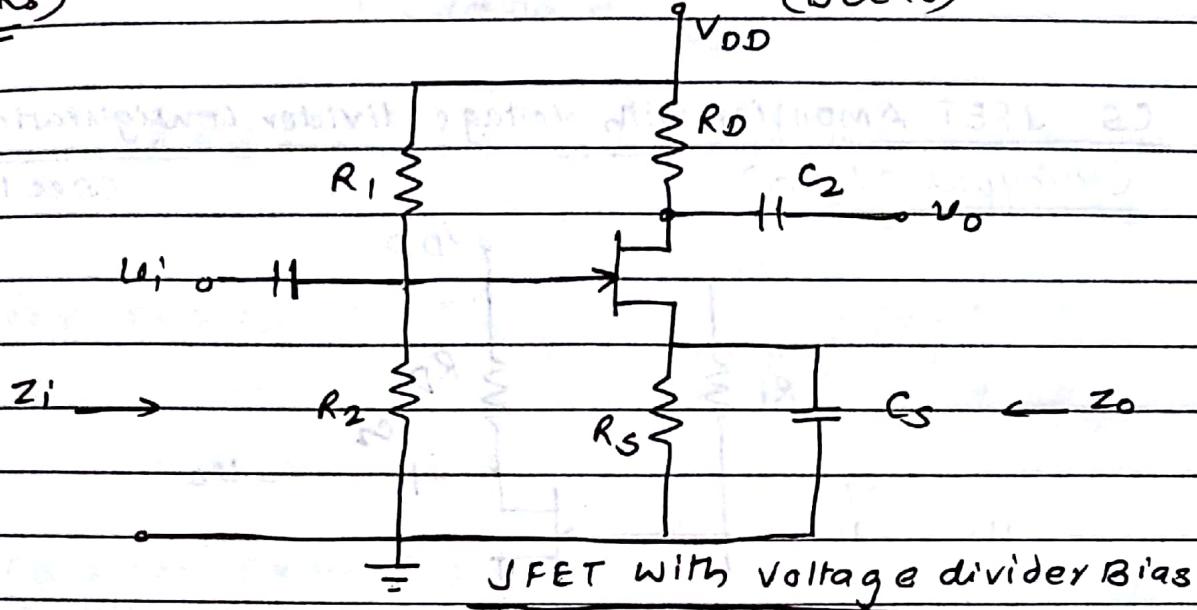
$$V_o = \frac{-g_m R_D V_i}{(1 + g_m R_S)}$$

$$\Delta V = \frac{V_0}{V_i} = \frac{-g_m R_D}{1 + g_m R_S}$$

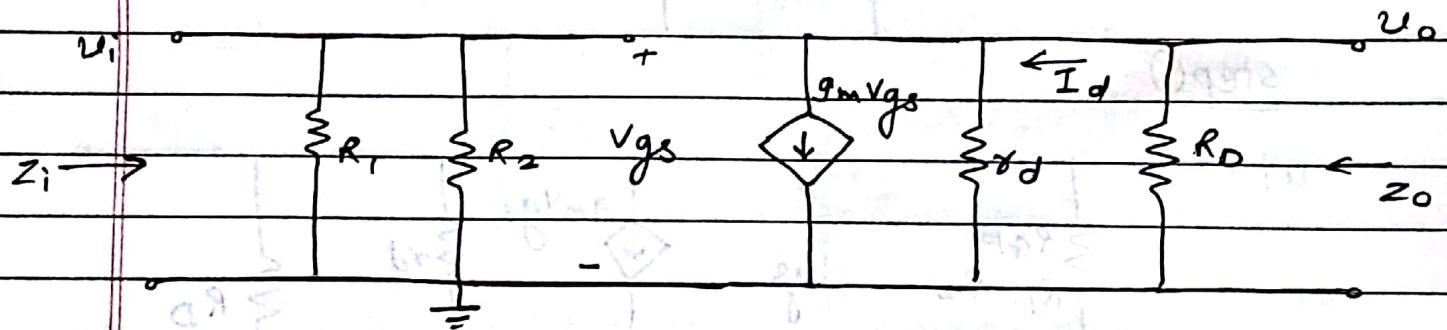
\* CS Amplifier with voltage divider configuration (Bypassed)

$R_S$ )

(Dec 10)



step① small signal equivalent circuit



step② - ① Input impedance ( $z_i$ ) =

$$z_i = (R_1 \parallel R_2)$$

② o/p impedance ( $z_o$ )

$$v_i = v_{gs} = 0 \therefore z_o = \infty \parallel R_D$$

$$\text{if } r_d \gg R_D, z_o = R_D$$

③ Voltage gain (AV) -

$$AV = \frac{V_o}{V_i} \quad \text{where } V_i = v_{gs}$$

$$\& V_o = -I_d (R_D \parallel r_d)$$

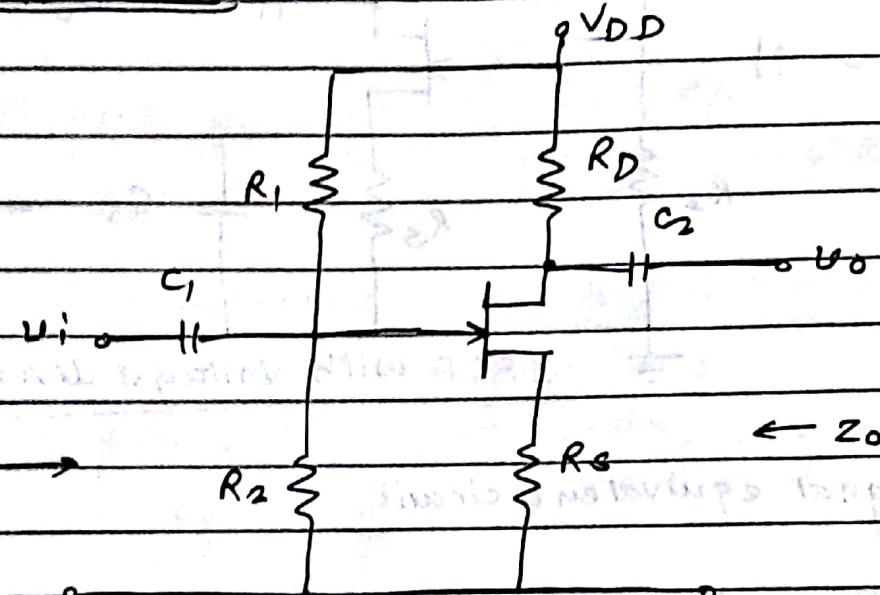
$$\text{But } I_d = g_m v_{gs}$$

$$\therefore AV = \frac{-g_m v_{gs} (R_D \parallel r_d)}{v_{gs}} = -g_m (R_D \parallel r_d)$$

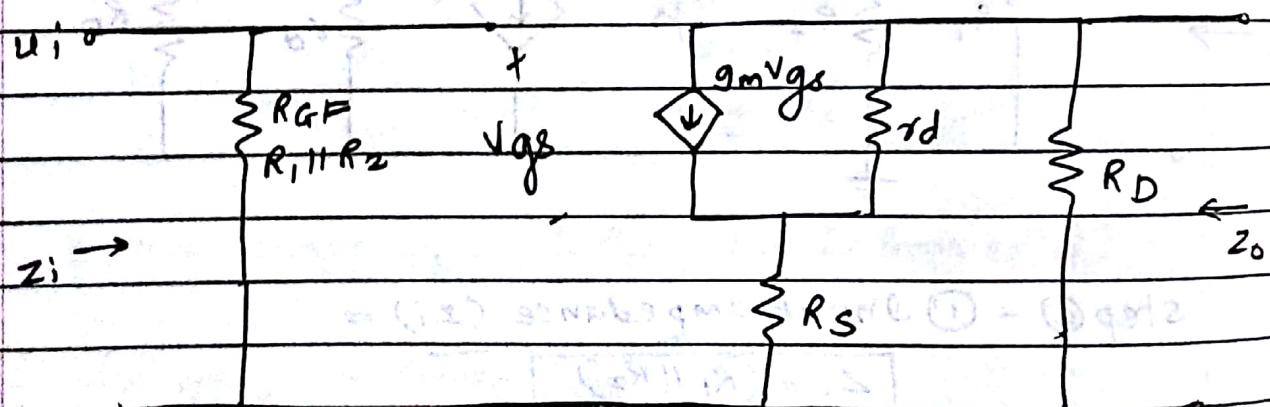
If  $\tau_d \gg R_D$ ,  $A_V = -g_m R_D$

\* CS JFET Amplifier with voltage divider configuration  
(Unbypassed  $R_E$ )

(Dec 11) (10)



step ①



small signal equivalent ckt

step ② Input Impedance  $Z_i = R_G = R_1 \parallel R_2$

③ Output Impedance  $Z_o = R_D$

$$\left[ 1 + g_m R_S + \frac{(R_D + R_S)}{r_d} \right]$$

$$\text{or } Z_o = \frac{\tau_d R_D}{[\tau_d + R_D + (1 + g_m) R_S]}$$

if  $\tau_d \gg (R_D + R_S)$ ,

$$Z_o = \frac{R_D}{[1 + g_m R_S]}$$

$$A_V = \frac{-g_m R_D}{[1 + g_m R_S + (R_D + R_S)]}$$

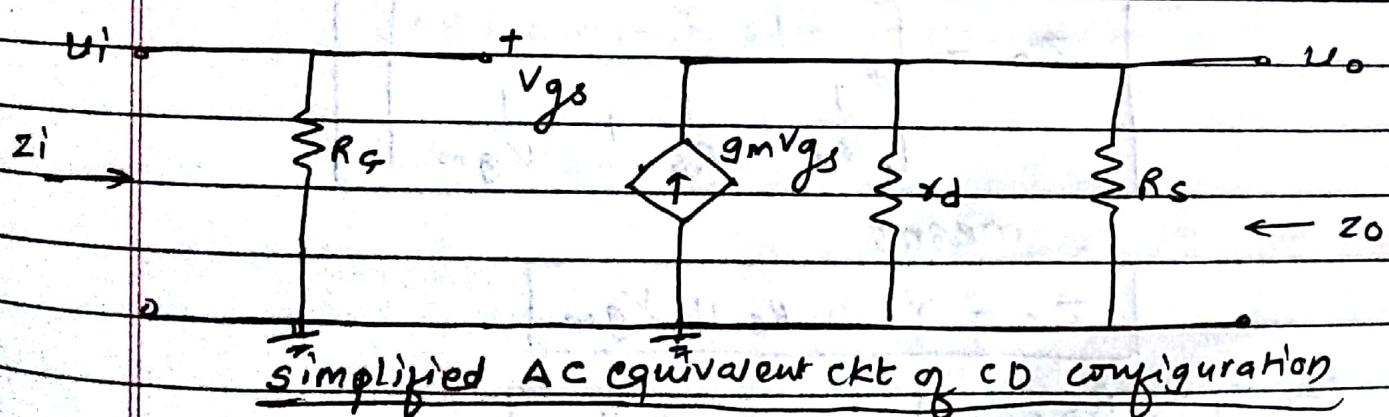
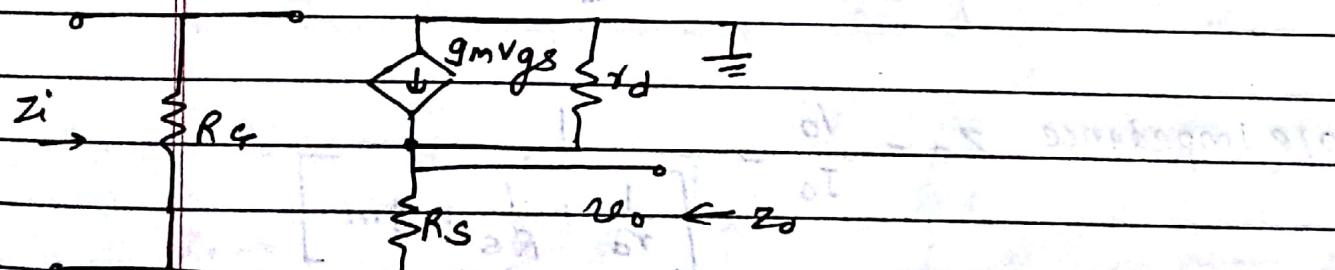
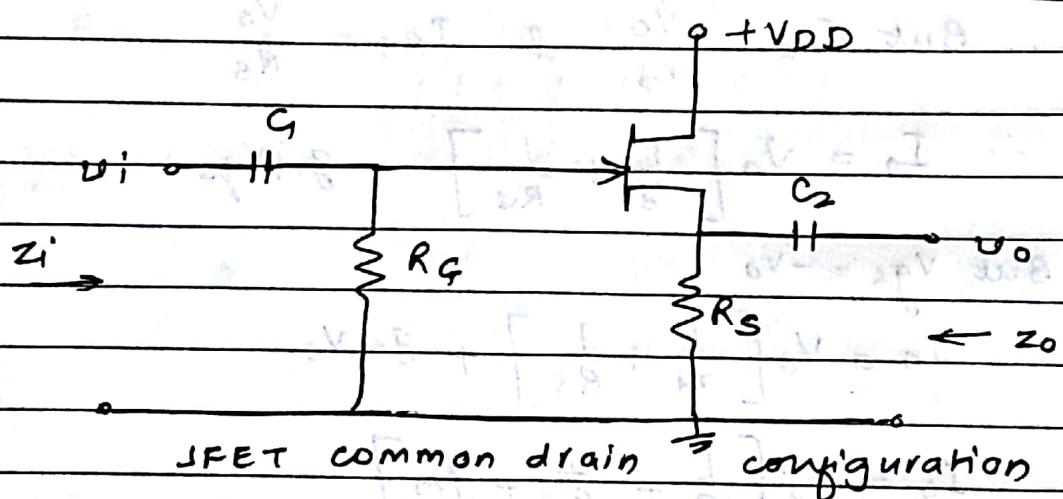
OR

$$A_V = \frac{-\mu R_D}{[r_d + R_D + (1 + \mu) R_S]}$$

for  $r_d \gg (R_D + R_S)$

$$A_V = \frac{-g_m R_D}{[1 + g_m R_S]}$$

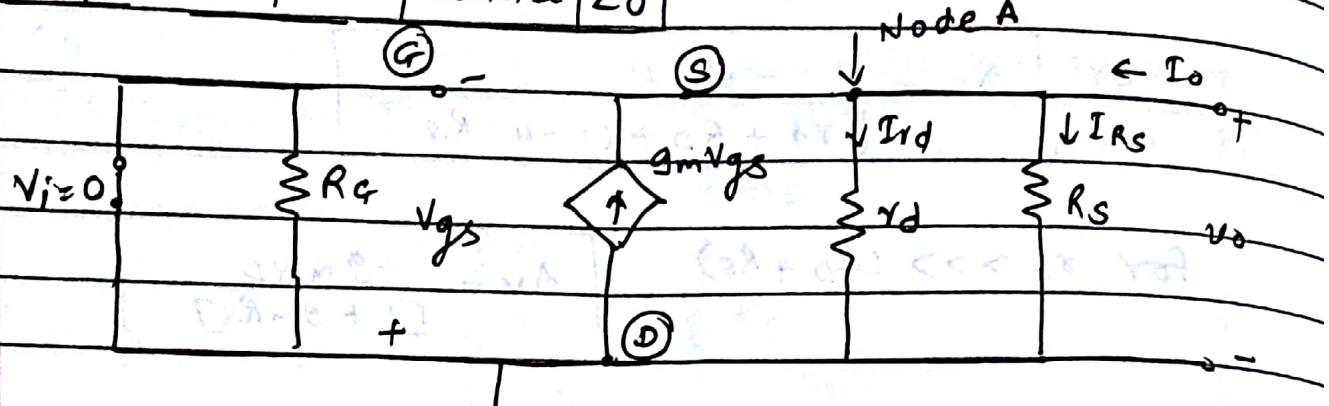
### \* Common Drain (CD) or Source Follower Configuration -



step ① calculate  $|Z_i|$

$$Z_i = R_G$$

step ② output impedance  $Z_o$



Apply KCL at Node A

$$I_o + g_m V_{GS} = I_{RD} + I_{RS}$$

$$\text{But } I_{RD} = \frac{V_o}{R_d} \quad \& \quad I_{RS} = \frac{V_o}{R_s}$$

$$\therefore I_o = V_o \left[ \frac{1}{R_d} + \frac{1}{R_s} \right] - g_m V_{GS}$$

$$\text{But } V_{GS} = -V_o$$

$$I_o = V_o \left[ \frac{1}{R_d} + \frac{1}{R_s} \right] + g_m V_o$$

$$I_o = V_o \left[ \frac{1}{R_d} + \frac{1}{R_s} + g_m \right]$$

$$\text{O/P impedance } Z_o = \frac{V_o}{I_o} = \frac{1}{\left[ \frac{1}{R_d} + \frac{1}{R_s} + g_m \right]}$$

$$Z_o = \frac{1}{\frac{1}{R_d} + \frac{1}{R_s} + g_m}$$

means

$$Z_o = R_d \parallel R_s \parallel g_m$$

for  $R_d \gg R_s$ ,

$$Z_o = R_s \parallel g_m$$

### Step ③ Voltage gain ( $A_V$ ) -

$$V_o = g_m V_{gs} (r_d \parallel R_s) \quad \text{--- (1)}$$

Apply KVL to o/p loop

$$V_i = V_{gs} + V_o$$

$$\& V_{gs} = V_i - V_o \quad \text{Put in eqn (1)}$$

$$V_o = g_m (V_i - V_o) (r_d \parallel R_s)$$

$$= g_m V_i (r_d \parallel R_s) - g_m V_o (r_d \parallel R_s)$$

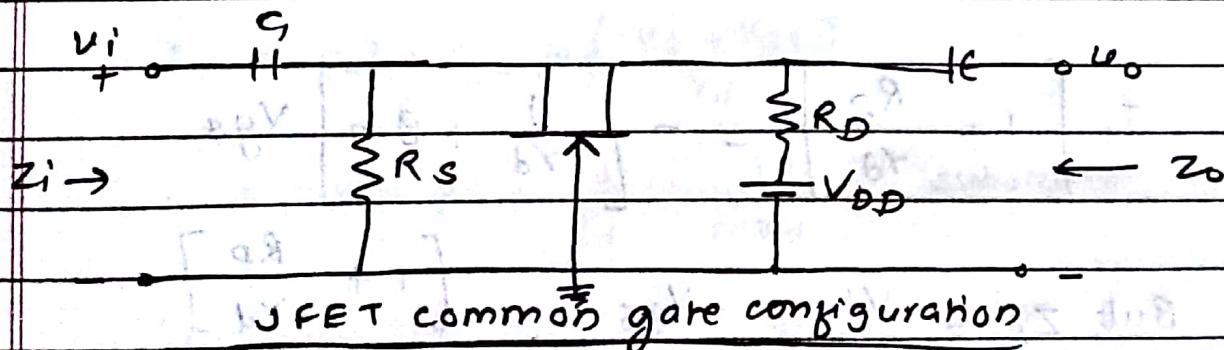
$$V_o [1 + g_m (r_d \parallel R_s)] = g_m V_i (r_d \parallel R_s)$$

$$A_V = \frac{V_o}{V_i} = \frac{g_m (r_d \parallel R_s)}{[1 + g_m (r_d \parallel R_s)]}$$

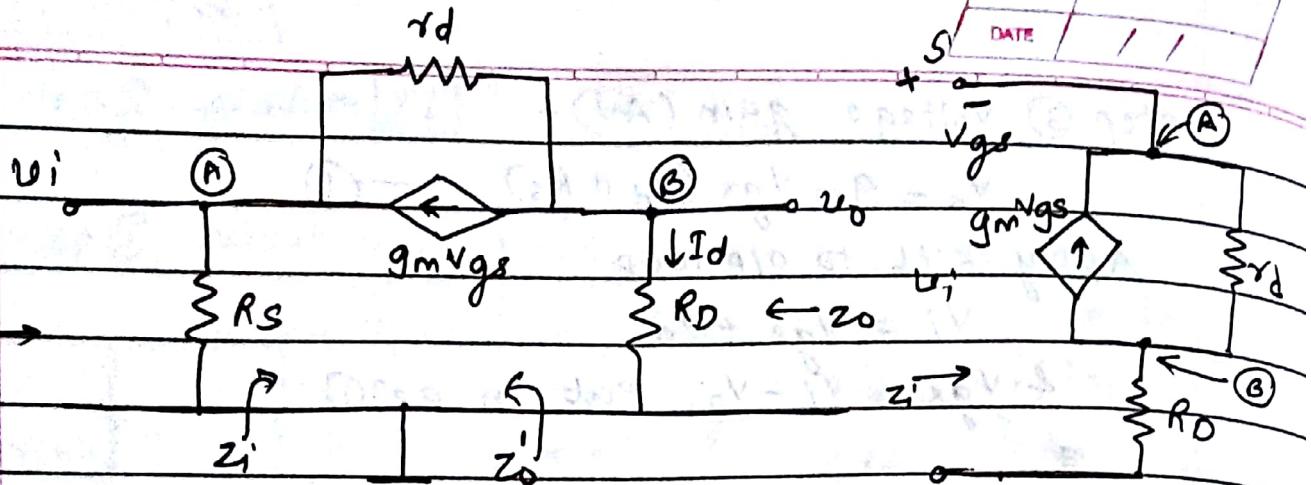
for  $r_d \gg R_s$ ,  $r_d \parallel R_s \approx R_s$

$$A_V = \frac{g_m R_s}{1 + g_m R_s}$$

### \* JFET Common Gate configuration -



$$V_o = V_{DD} - I_d R_D$$



AC equivalent ckt of JFET CG

Network to obtain \$z\_i'\$

Step ① Input impedance

$$z_i = R_s \parallel z_i' \quad (1)$$

To obtain \$z\_i'\$ -

Apply KCL to node A,

$$I_1 = I_{rd} - g_m v_{gs} \quad \text{But } I_{rd} = \frac{V_{rd}}{r_d} \quad (2)$$

& \$V\_{rd} = -V\_{gs} - I\_1 R\_D\$ put this in eqn ①,

$$I_1 = -\frac{V_{gs}}{r_d} - \frac{I_1 R_D}{r_d} - g_m v_{gs}$$

$$= -\frac{V_{gs}}{r_d} - \frac{I_1 R_D}{r_d} - g_m v_{gs}$$

$$= -\left[\frac{1}{r_d} + g_m\right] V_{gs} - \frac{I_1 R_D}{r_d}$$

$$I_1 \left[ 1 + \frac{R_D}{r_d} \right] = -\left[ \frac{1}{r_d} + g_m \right] V_{gs}$$

$$\text{But } z_i' = \frac{V_i}{I_1} = \frac{-V_{gs}}{\left[ 1 + \frac{R_D}{r_d} \right]} = \frac{\left[ 1 + \frac{R_D}{r_d} \right]}{\left[ g_m + \frac{1}{r_d} \right]}$$

$$z_i' = \frac{r_d + R_D}{1 + g_m r_d}$$

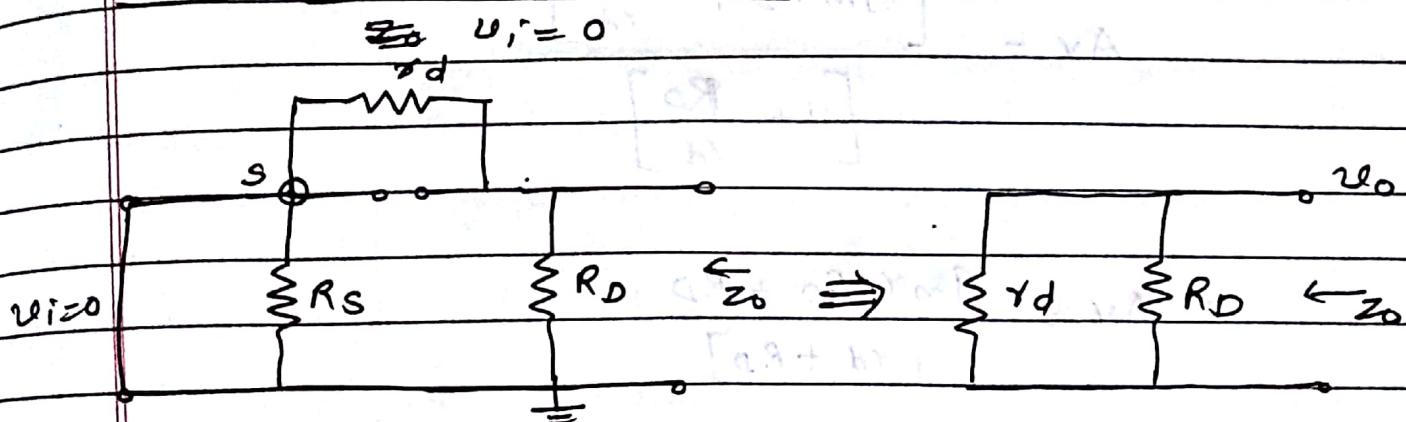
$$z_i = z_i' \parallel R_s$$

$$z_i = R_s \parallel \left[ \frac{r_d + R_D}{1 + g_m r_d} \right]$$

for \$r\_d \gg 10 R\_D

$$z_i = R_s \parallel [g_m]$$

## Step ② output impedance $Z_o$



AC equivalent ckt with  $v_i = 0$  used to calculate the o/p impedance  $Z_o$

$$Z_o = y_d \parallel R_D \quad \text{for } y_d \gg R_D \quad | Z_o = R_D$$

## ③ Voltage gain ( $A_v$ ) :-

$$A_v = \frac{V_o}{V_i}$$

$$V_i = -V_{gs}, \quad V_o = I_d R_D \quad \text{--- (2)}$$

Apply KCL to node ③

$$I_d + g_m V_{gs} + I_{rd} = 0$$

$$\therefore I_d = -g_m V_{gs} - I_{rd}$$

$$\text{But } y_d = \frac{V_o - V_i}{R_D} = \frac{V_o + V_{gs}}{y_d}$$

$$I_d = -g_m V_{gs} - \left[ \frac{V_o + V_{gs}}{y_d} \right]$$

$$I_d = -g_m V_{gs} - \frac{V_o}{R_D} - \frac{V_{gs}}{y_d} \quad \text{substitute into eqn (2),}$$

$$V_o = -g_m V_{gs} R_D - V_o \frac{R_D}{y_d} - \frac{V_{gs} R_D}{y_d}$$

$$\left[ 1 + \frac{R_D}{y_d} \right] V_o = - \left[ g_m R_D + \frac{R_D}{y_d} \right] V_{gs}$$

$$\text{Now } A_v = \frac{V_o}{V_i} = \frac{V_o}{-V_{gs}} \quad \text{as } V_i = -V_{gs}$$

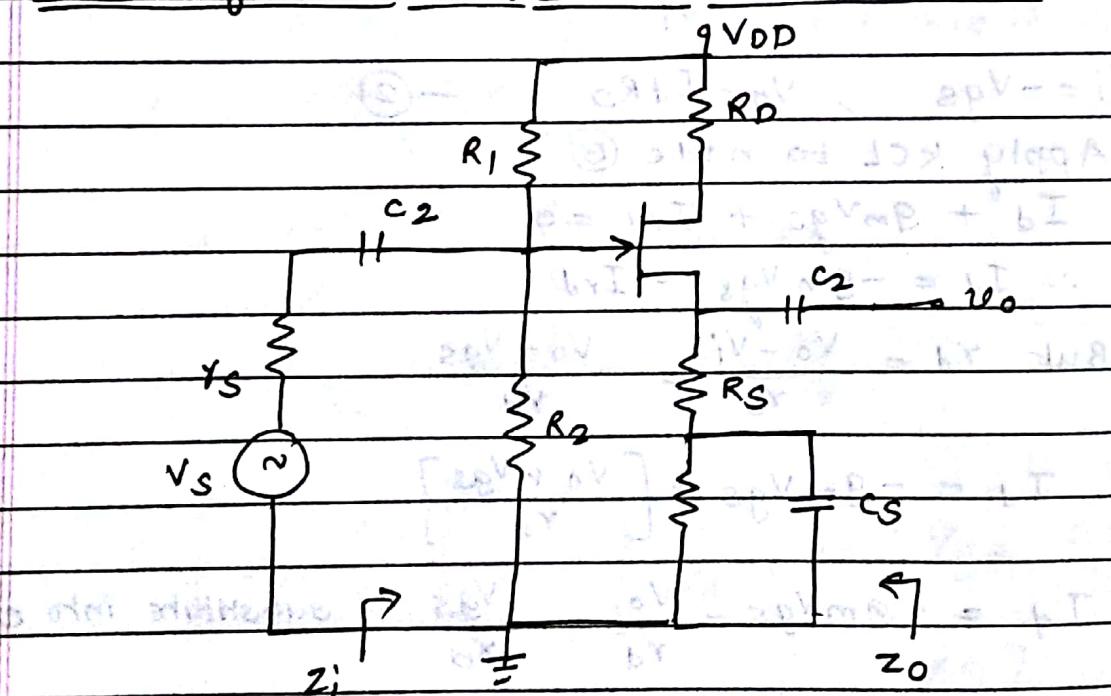
$$A_V = \frac{\left[ g_m R_D + \frac{R_D}{r_d} \right]}{\left[ 1 + \frac{R_D}{r_d} \right]}$$

$$\therefore A_V = \frac{g_m r_d R_D + R_D}{r_d + R_D}$$

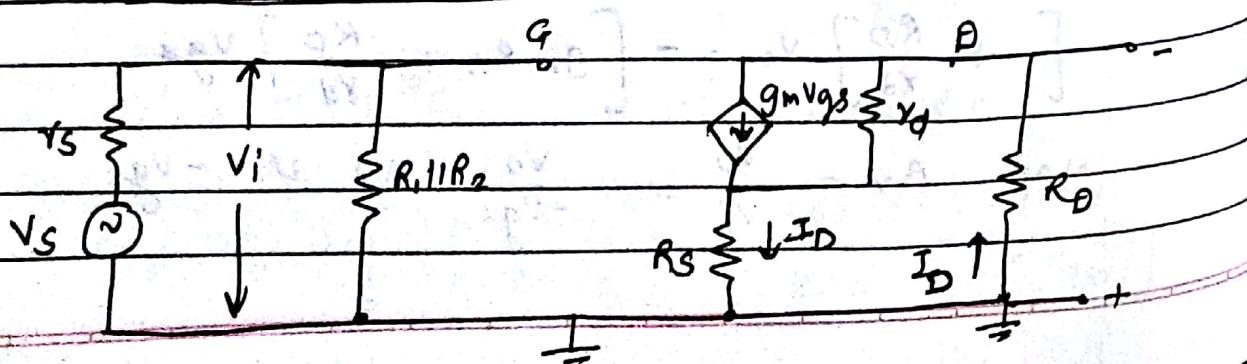
$$\text{for } r_d \gg R_D, \quad A_V = \frac{g_m r_d R_D}{r_d}$$

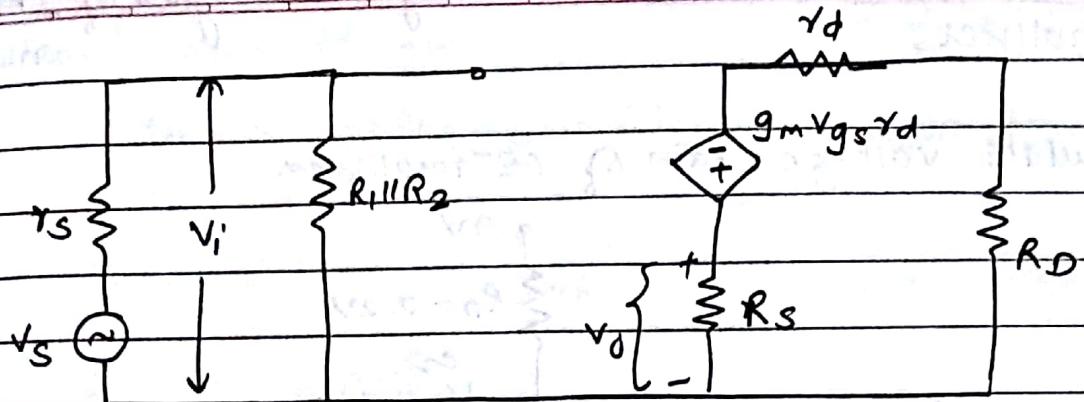
$$A_V = g_m R_D$$

\* Source follower with a drain resistance ( $R_D$ ) :-



Step ① AC equivalent circuit





AC equivalent ckt after replacing dependent current source by a voltage source

Expression for  $A_V$

$$V_o = \frac{R_S}{R_D + R_S + r_d} \times g_m r_d V_{gs}$$

$$\frac{V_o}{V_{gs}} = \frac{R_S \cdot g_m r_d}{R_D + R_S + r_d} = \frac{\mu R_S}{(R_D + R_S + r_d)}$$

$$\text{But } V_i = V_{gs} + V_o \quad \therefore V_{gs} = V_i - V_o$$

$$\therefore V_o = \frac{\mu R_S (V_i - V_o)}{R_D + R_S + r_d}$$

$$\therefore V_o (R_D + R_S + r_d) = \mu R_S V_i - \mu R_S V_o$$

$$V_o [R_D + r_d + (1 + \mu) R_S] = \mu R_S V_i$$

$$A_V = \frac{V_o}{V_i} = \frac{\mu R_S}{R_D + r_d + (1 + \mu) R_S}$$

$$A_{Vs} \Rightarrow \frac{V_i}{V_s}$$

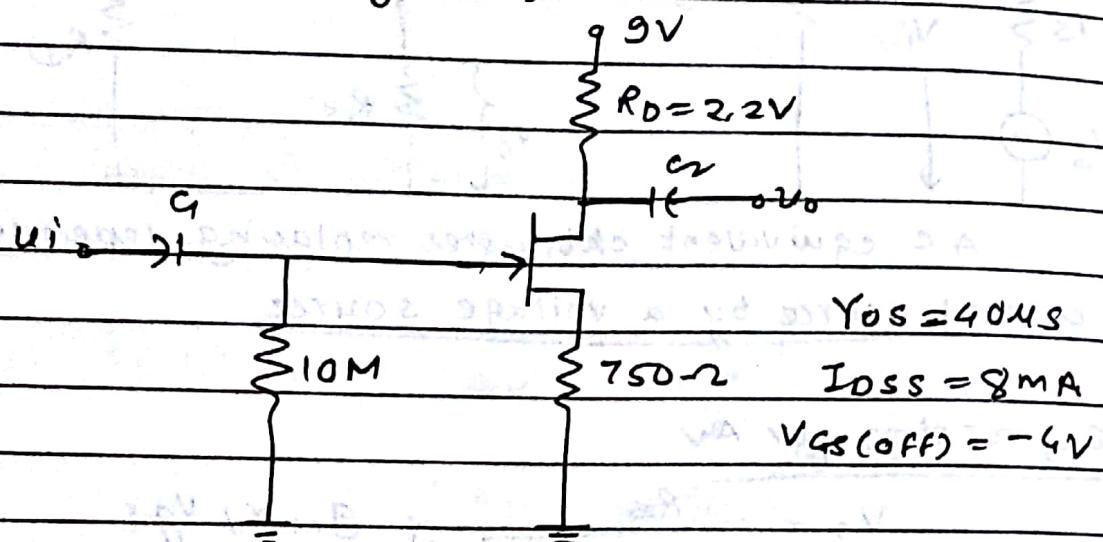
$$V_i = \frac{R_1 || R_2}{r_s + (R_1 || R_2)} \times V_s$$

$$\frac{V_i}{V_s} = \frac{R_1 || R_2}{r_s + (R_1 || R_2)}$$

$$A_{Vs} = \frac{V_o}{V_i} \times \frac{V_i}{V_s} = \frac{\mu R_S}{[r_d + R_D + (1 + \mu) R_S]} \times \frac{(R_1 || R_2)}{r_s + (R_1 || R_2)}$$

# Examples / Numericals on Small signals analysis of JFET Amplifiers

Ex1. Calculate voltage gain of FET amplifier.



Sol<sup>1</sup> - step ① calculate  $V_{GSQ}$  :-

$$V_{GSQ} = -I_D R_S = -0.75 I_D$$

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GSQ}}{V_p} \right]^2 = 8 \left[ 1 - \frac{(-0.75 I_D)^2}{(-4)} \right]$$

$$I_D = 8 \left[ 1 - \frac{0.75 I_D}{4} \right]^2 = 0.5 [4 - 0.75 I_D]^2$$

$$2I_D = 16 - 6I_D + 0.5625 I_D^2$$

$$0 = 16 - 8I_D + 0.5625 I_D^2$$

$$I_D = \frac{8 \pm \sqrt{(-8)^2 - (4 \times 0.5625 \times 16)}}{2 \times 0.5625} = \frac{8 \pm 5.29}{1.125}$$

$$I_D = 11.81 \text{ mA or } 2.4 \text{ mA}$$

for  $I_D = 11.81 \text{ mA}$ ,  $V_{DS}$  will be -ve  
 $\therefore$  Select  $I_D = 2.4 \text{ mA}$

$$V_{GSQ} = -0.75 \times 2.4 \times 10^{-3} = -1.8 \text{ V}$$

step ② calculate  $g_m$  -

$$g_{m0} = \frac{2 I_{DSS}}{|V_{pI}|} = \frac{2 \times 8 \times 10^{-3}}{1-41} = 4 \text{ mS}$$

$$g_m = g_{m0} \left[ 1 - \frac{V_{GSQ}}{V_p} \right] = 4 \times 10^{-3} \left[ 1 - \frac{(-1.8)}{-4} \right]$$

$$g_m = 2.2 \text{ mS}$$

step ③ calculate  $r_d$

$$r_d = \frac{1}{Y_{OS}} = \frac{1}{40 \times 10^{-6}} = 25 \text{ k}\Omega$$

step ④ calculate  $A_v$  -

$$A_v = -g_m R_D$$

$$1 + g_m R_S + \frac{R_D r_s}{r_d}$$

$$-2.2 \times 2.2$$

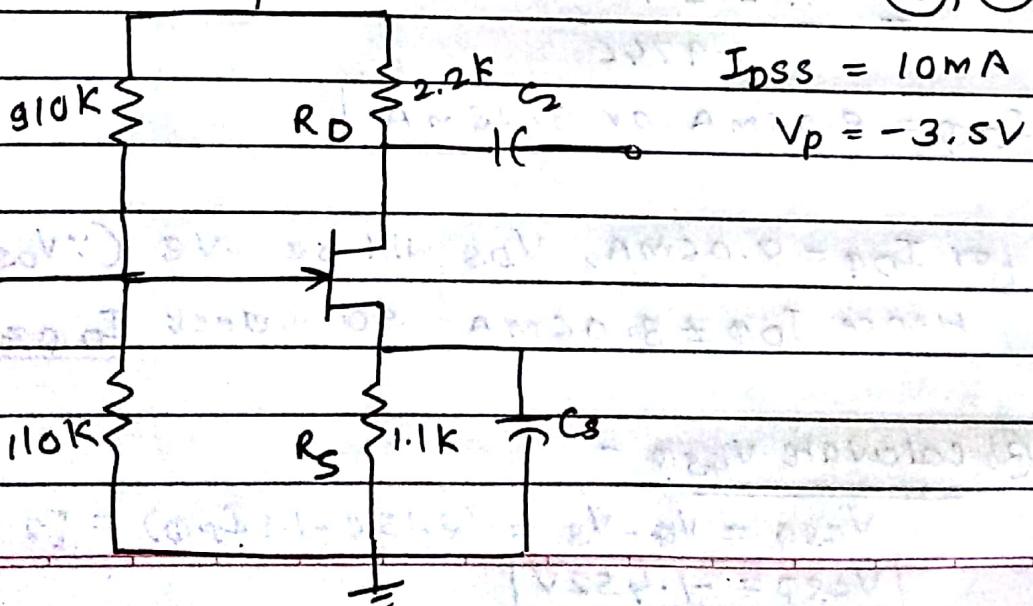
$$1 + (2.2 \times 0.75) + \left[ \frac{2.2 + 0.75}{2.5} \right]$$

$$A_v = -1.75$$

(Ex2) For JFET amplifier shown in fig, calculate  $A_v$ ,  $Z_i$ ,  $Z_o$

$$|V_{DD}| = 20 \text{ V}$$

(Ques 15, 10)



5017 ① calculate  $I_{DQ}$

$$V_{GS} = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{110}{90 + 110} \times 20 = 2.156V$$

$$V_S = I_{DQ} \times R_S = 1.1k \times I_{DQ}$$

$$V_{GSQ} = V_G - V_S = (2.156 - 1.1 I_{DQ})$$

$$I_{DQ} = I_{DS} \left[ 1 - \frac{V_{GSQ}}{V_P} \right]^2$$

$$= 10 \times 10^{-3} \left[ 1 - \frac{(2.156 - 1.1 I_{DQ})}{3.5} \right]^2$$

$$I_{DQ} = 10 \times 10^{-3} \left[ 1 + \frac{2.156 - 1.1 I_{DQ}}{3.5} \right]^2$$

$$= 10 \times 10^{-3} \left[ \frac{3.5 + 2.156 - 1.1 I_{DQ}}{3.5} \right]^2$$

$$= \frac{10mA}{12.25} [5.656 - 1.1 I_{DQ}]^2$$

$$= 0.816mA [32 - 12.5 I_{DQ} + 1.21 I_{DQ}^2]$$

$$= 26.112 - 10.2 I_{DQ} + 0.9873 I_{DQ}^2$$

$$0 = 26.112 - 11.2 I_{DQ} + 0.9873 I_{DQ}^2$$

$$I_{DQ} = \frac{11.2 \pm \sqrt{(-11.2)^2 - (4 \times 0.9873 \times 26.112)}}{2 \times 0.9873}$$

$$= 11.2 \pm 4.72$$

$$= 1.974mA$$

$$\boxed{I_{DQ} = 8.06mA \text{ or } 3.28mA}$$

for  $I_{DQ} = 8.06mA$ ,  $V_{DS}$  will be -ve ( $\because V_{DS} = V_{DD} - I_{DQ} \times (R_D + R_S)$ )  
Hence  $I_{DQ} \neq 8.06mA$  so select  $\boxed{I_{DQ} = 3.28mA}$

② calculate  $V_{GSQ}$  -

$$V_{GSQ} = V_G - V_S = (2.156 - 1.1 I_{DQ}) = [2.156 - (1.1 \times 3.28)]$$

$$\boxed{V_{GSQ} = -1.452V}$$

step ③ calculate  $g_m$  -

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}\Phi}{V_p} \right]$$

$$g_{m0} = \left| \frac{2 I_{DSS}}{V_p} \right| = \left| \frac{2 \times 10 \times 10^3}{3.5} \right| = 5.71 \text{ mS}$$

$$g_m = 5.71 \text{ mS} \left[ 1 - \frac{-1.952}{-3.5} \right] = \underline{\underline{3.39 \text{ mS}}}$$

step ④ calculate  $A_v$ ,  $Z_i$  &  $Z_o$  -

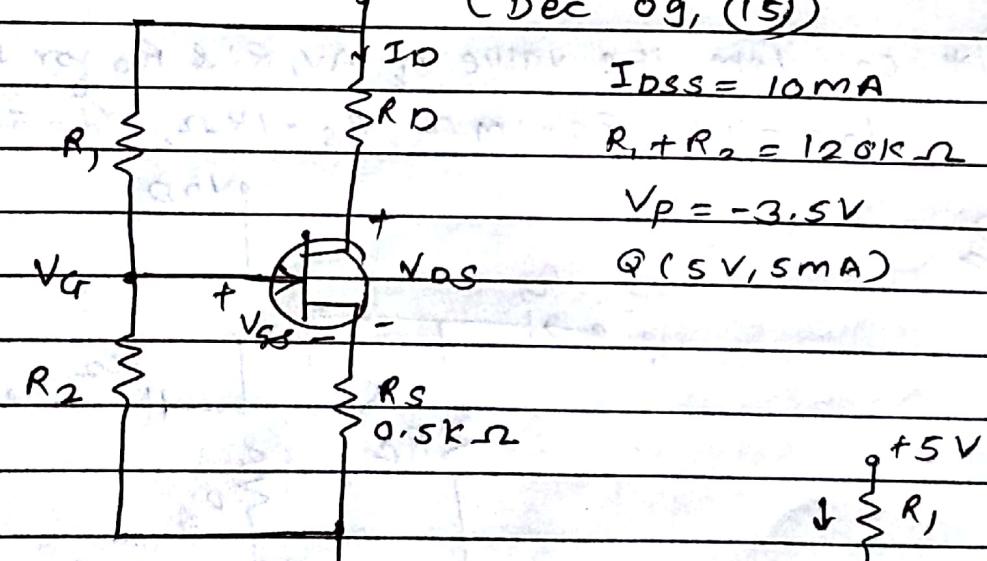
$$A_v = -g_m R_D = -3.39 \times 2.2 = \underline{\underline{-7.35}}$$

$$Z_i = R_1 \| R_2 = \frac{910 \times 110}{910 + 110} = \underline{\underline{98.13 \text{ k}\Omega}}$$

$$Z_o = R_D = 2.2 \text{ k}\Omega$$

Ex 3. The parameters of the transistor in the JFET CS amplifier shown in given figure are -  $I_{DSS} = 10 \text{ mA}$ ,  $V_p = -3.5 \text{ V}$ ,  $R_1 + R_2 = 120 \text{ k}\Omega$  & Q point is at  $I_{DQ} = 5 \text{ mA}$  &  $V_{DS} = 5 \text{ V}$ . Determine the values of  $R_1$ ,  $R_2$  &  $R_D$ .

(Dec og, 15)



$$I = \frac{5+5}{(R_1+R_2)} = \frac{10}{120 \times 10^3} = 83.33 \text{ mA}$$

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}\Phi}{V_p} \right]^2$$

$$\sqrt{0.5} = 1 + \frac{V_{GS}}{3.5}$$

$$V_{GS} = -1.025V$$

$$V_G = -5V + I_D R_S + V_{GS}$$

$$= -5 + (5 \times 0.5) - 1.025$$

$$= -3.525V$$

$$R_2 = \frac{V_G - (-5)}{I} = \frac{-3.525 + 5}{83.33 \times 10^{-6}} = 17.7k\Omega$$

$$R_1 + R_2 = 120\Omega + 17.7\Omega = 137.7\Omega$$

$$R_2 = 120 - 17.7 = 102.3k\Omega$$

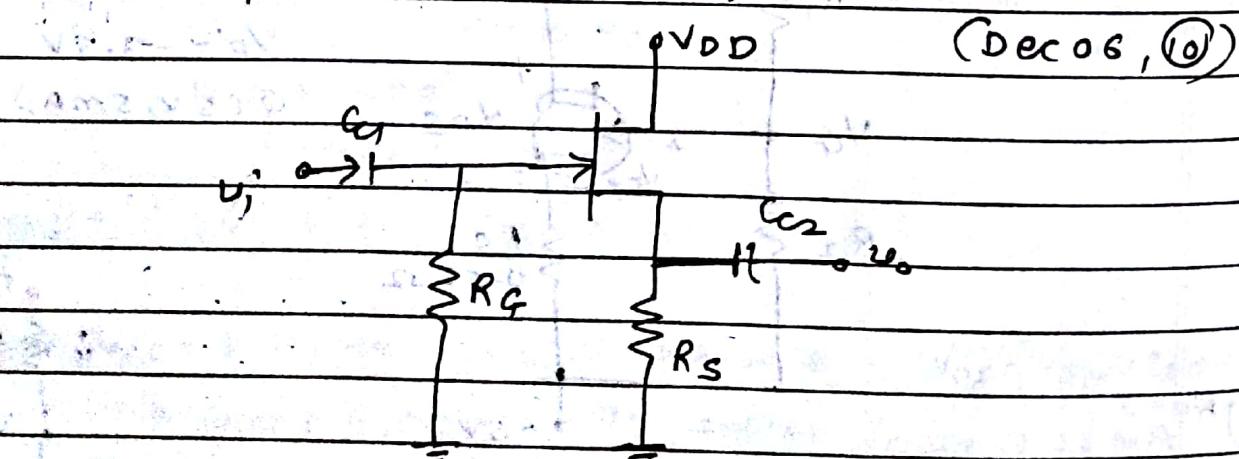
$$5 + 5 = I_D R_D + V_{DS} + I_D R_S$$

$$10 = 5R_D + 5 + (5 \times 0.5)$$

$$R_D = 0.5k\Omega$$

**EQU\*** calculate the value of  $A_V$ ,  $R_i$  &  $R_o$  for JFET,  $I_{DSS} = 8mA$ ,  $V_p = -4V$ ,  $R_G = 1M\Omega$ ,  $R_S = 1k\Omega$ ,  $r_d = 50k\Omega$

**CD**



$$\text{Q15) find } V_{GS} \Rightarrow V_{GS} = -I_D R_S = -1 I_D$$

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_p} \right]^2 = 8 \left[ 1 - \frac{(-I_D)^2}{4} \right]$$

$$= \frac{1}{2} [4 - I_D]^2 = \frac{1}{2} [16 - 8I_D + I_D^2]$$

$$I_D^2 - 10I_D + 16 = 0$$

$$I_D = 10 \pm \sqrt{(10)^2 - 4 \times 1 \times 16} = 8 \text{ mA or } I_D = 2 \text{ mA}$$

Select  $I_D = 2 \text{ mA}$ ,  $V_{GS} = -1 \times 2 = -2 \text{ V}$

$$g_m \Rightarrow g_{m0} = \frac{2I_{DSS}}{V_P} = \frac{2 \times 8}{4} = 4 \text{ mA/V}$$

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right] = 4 \left[ 1 - \frac{-2}{-4} \right] = 2 \text{ mA/V}$$

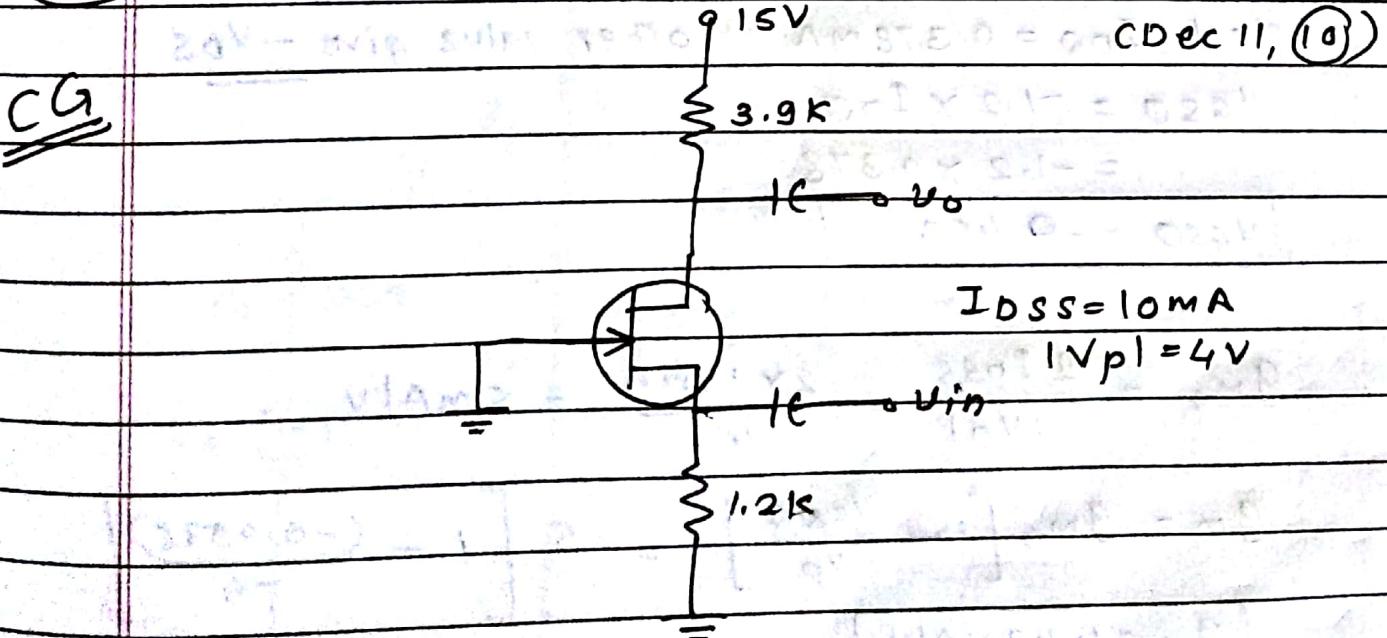
$$R_i = R_g = 1M\Omega$$

$$R_o = r_d \parallel R_s \parallel \frac{1}{g_m} = 50k \parallel 1k \parallel 0.5k$$

$$R_o = 337.9 \Omega \text{ or } 0.3379k$$

$$A_V = \frac{g_m(r_d \parallel R_s)}{1 + g_m(r_d \parallel R_s)} = \frac{2 \times 0.98}{1 + (2 \times 0.98)} = 0.662$$

Ex 5. Find  $A_V$ ,  $R_i$ , &  $R_o$  for the circuit shown.



Sol<sup>n</sup> step ① common gate amplifier.

$$I_{DQ} = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$$

$$\text{But } V_G = 0$$

$$\& V_S = R_S I_{DQ} = 1.2 I_{DQ}$$

$$V_{GS} = V_G - V_S$$

$$= 0 - 1.2 I_{DQ} = -1.2 I_{DQ}$$

$$I_{DQ} = 10 \left[ 1 - \frac{1.2 I_{DQ}}{4} \right]^2$$

$$= \frac{10}{16} [4 - 9.6 I_{DQ} + 1.44 I_{DQ}^2]$$

$$14.4 I_{DQ}^2 - 112 I_{DQ} + 40 = 0$$

$$I_{DQ} = \frac{112 \pm \sqrt{(-112)^2 - 4 \times 14.4 \times 40}}{2 \times 14.4}$$

$$= \frac{112 \pm 101.2}{28.8}$$

$$I_{DQ} = 7.4 \text{ mA or } 0.378 \text{ mA}$$

select  $I_{DQ} = 0.378 \text{ mA} \because$  other value give  $-V_{DS}$

$$V_{GSQ} = -1.2 \times I_{DQ}$$

$$= -1.2 \times 0.378$$

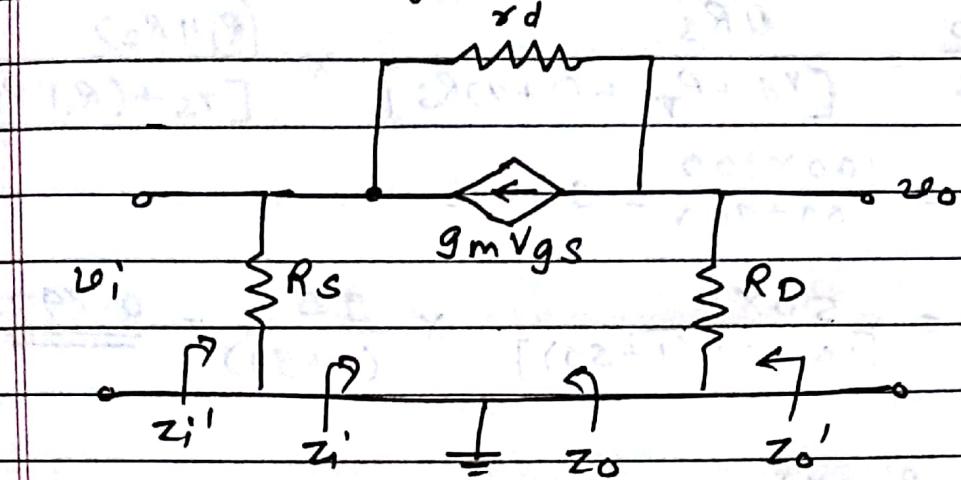
$$V_{GSQ} = -0.453 \text{ V}$$

$$g_{m0} = \frac{2 I_{DSS}}{|V_P|} = \frac{2 \times 10 \text{ mA}}{4} = 5 \text{ mA/V}$$

$$g_m = g_{m0} \left[ 1 - \frac{V_{GSQ}}{V_P} \right] = 5 \left[ 1 - \frac{(-0.453)}{4} \right]$$

$$g_m = 4.43 \text{ mA/V}$$

② Draw small signal equivalent



③ find  $Z_i'$  &  $Z_o'$

$$Z_i' = \infty$$

$$Z_o' = R_s \parallel \frac{1}{g_m} = 1.2 \text{ k}\Omega \parallel \left( \frac{1}{4.43 \times 10^{-3}} \right)$$

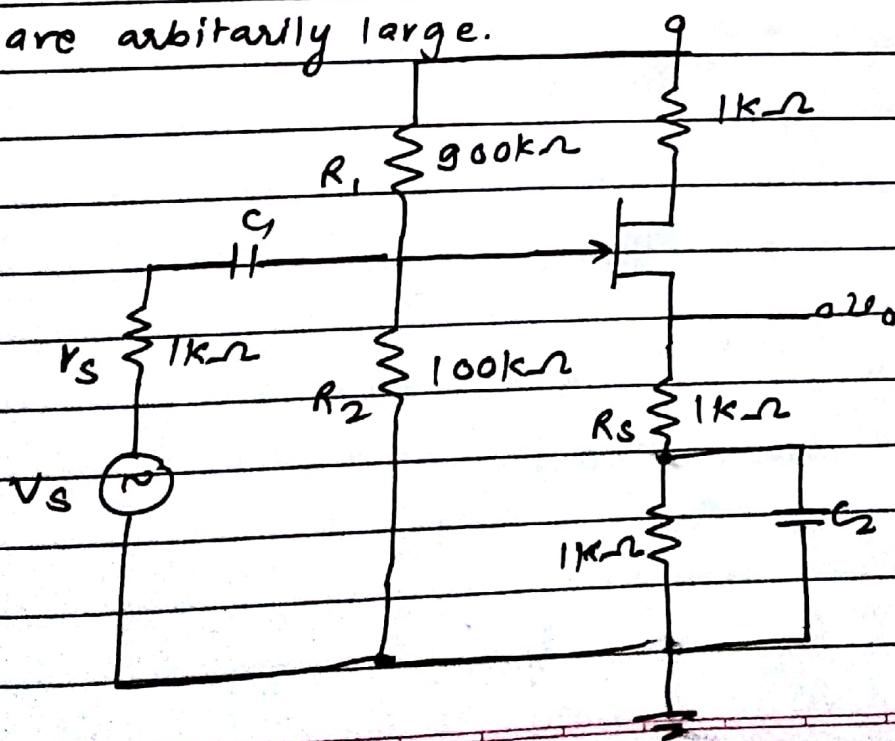
$$\boxed{Z_o' = 0.1894 \text{ k}\Omega \text{ or } 189.4 \Omega}$$

$$Z_o = \infty$$

$$\boxed{Z_o = R_D = 3.9 \text{ k}\Omega}$$

$$\boxed{A_V = g_m R_D = 4.43 \times 3.9 = 15}$$

Ex 6.3 For the FET shown,  $g_m = 5 \text{ mA/V}$  -  $r_d = 10 \text{ k}\Omega$ , calculate  $V_o/V_s$  &  $R_o$ . Assume that all the capacitors are arbitrarily large.



$$AV_S = \frac{V_O}{V_S} = \frac{\mu R_S}{[r_d + R_D + (1+\mu)R_S]} \times \frac{(R_1 || R_2)}{[r_s + (R_1 || R_2)]}$$

$$R_1 || R_2 = \frac{100 \times 900}{100 + 900} = 90 \text{ k}\Omega$$

$$\therefore AV_S = \frac{50 \times 1}{[10 + 1 + (1+50)]} \times \frac{90}{(1+90)} = 0.7975$$

$$R_o' = \frac{R_D + r_d}{1 + \mu} = \frac{1 + 10}{1 + 50} = 21 \text{ k}\Omega$$

$$R_o = R_o' || R_S = 216 || 1000 = 17.6 \text{ }\Omega$$