

* FET Biasing -

FOR BJT, $I_C = \beta I_B$ & $V_{BE} = 0.7V$ & $I_C \leq I_E$.

The link b/w g_{dp} & o_{dp} variables is provided by β .

β is the constant establishes a linear relationship b/w I_{C_L}

FOR FET, the relationship b/w g_{dp} & o_{dp} quantities is non-linear due to the squared term in Shockley's Eqn.

- Linear relationship result in straight line when plotted graph of one variable Vs the other, whereas nonlinear relationship (b/w I_D & V_{GS}) result in curves as obtained from the transfer characteristics of a JFET.

- Another distinct difference b/w analysis of BJT & FET transistors is that :-

The g_{dp} controlling variable for a BJT transistor is a current level, whereas for the FET, a voltage is the control variable.

The general relationships applied to the analysis of all FET

$$I_G \approx 0A$$

$$I_D = I_S$$

& for JFETs & depletion type MOSFETs, Shockley's eqn is applied to relate g_{dp} & o_{dp} (char) quantities.

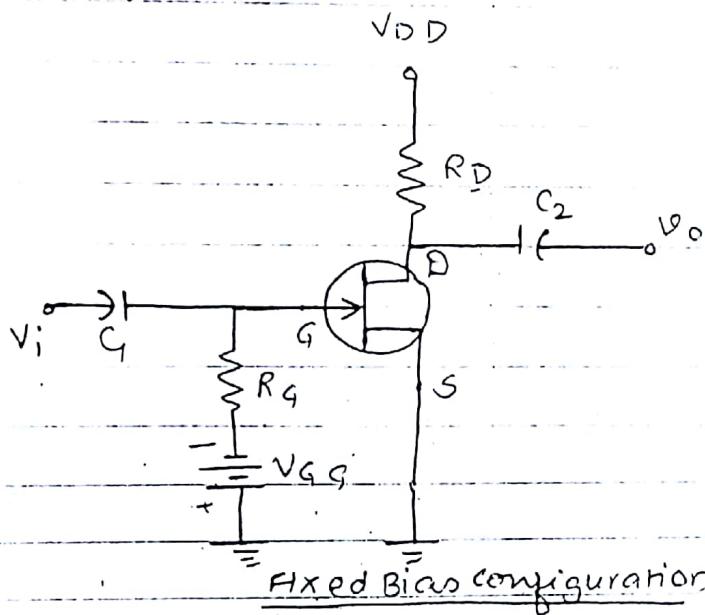
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

$$I_D = k (V_{GS} - V_T)^2$$

↳ for enhancement mode

① Fixed Bias Configuration :-

- It is one of the simplest biasing arrangement, for n-channel JFET.
- It is one of the few FET config that can be solved just as directly using either a mathematical or a graphical approach.



@ Mathematical Approach :-

DC Analysis :-

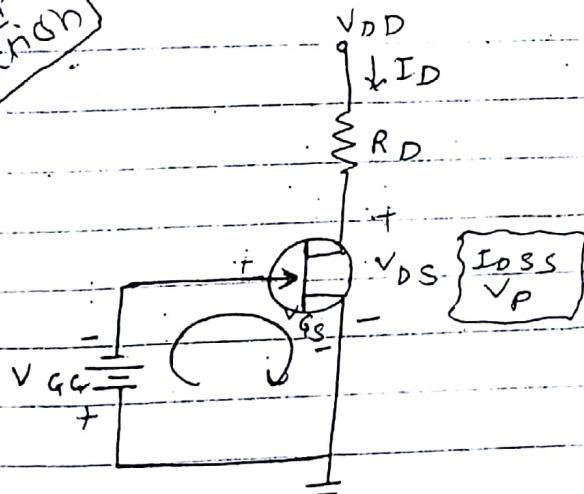
- C_1, C_2 are open ckt for dc analysis. & s.c for ac analysis
- R_G is present to ensure that V_i appears at the g/p to FET amplifier for ac analysis.

R_G For DC analysis :- $I_G \approx 0A$

$$V_{RG} = I_G R_G = 0 \times R_G = 0V$$

$\therefore V_{RG} \approx 0$ permits replacing R_G by s.c equivalent.

S.C
section



Network for dc analysis

- The resulting level of I_D is controlled by Schotckley's Eq?

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

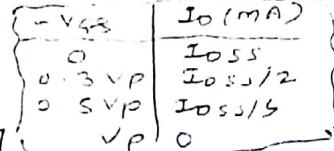
- Apply KVL in clockwise direction of the indicated loop,

$$-V_{GG} - V_{GS} = 0$$

$$\therefore V_{GS} = -V_{GG}$$

- since V_{GG} is a fixed desupply, the V_{GS} is fixed in magnitude resulting in config - 'Fixed Bias'

To draw Transfer curve $\Rightarrow I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$



(b) Graphical Approach

A graphical analysis requires a plot of Shockley's Eqn as shown in fig @

- choosing $V_{GS} = V_P/2$ will result in $I_D = I_{DSS}/4$ when plotted.

- For this analysis 3 pts defined by I_{DSS} , V_P & the intersection just described will be sufficient for plotting the curve.

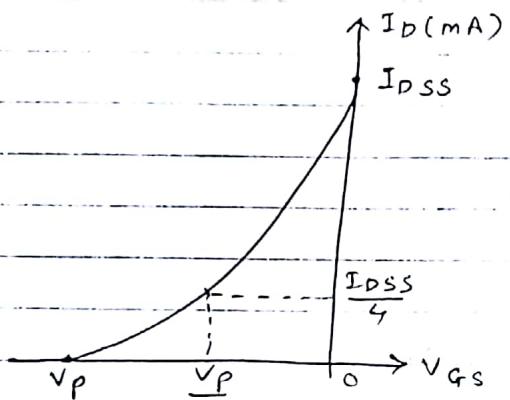


fig @ plotting shockley's Eqn

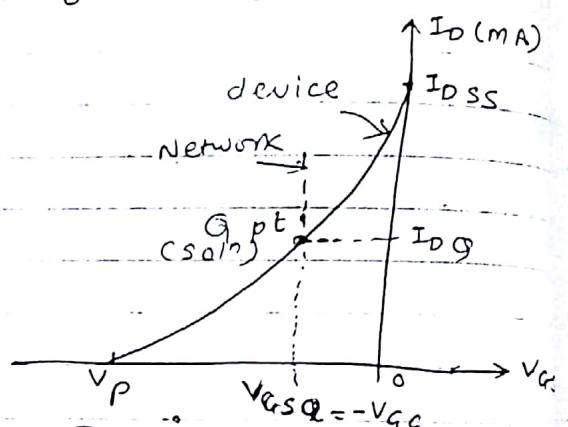
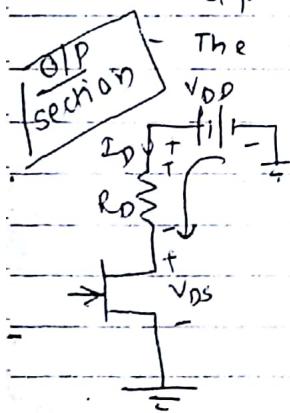


fig @ finding soln for fixed Bias config.

- The fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GS}$.
- At any pt on the vertical line, the level of V_{GS} is $-V_{GS}$. The level of I_D must simply be determined by this vertical line.
- The pt where the two curves intersect is the common soln to the config i.e. quiescent or operating pt.
- The I_{DQ} is determined by drawing a horizontal line from the Qpt to the vertical I_D axis.



The V_{DS} of op section by KVL, $\Rightarrow V_{DD} - I_D R_D - V_{DS} = 0$

$$\therefore V_{DS} = V_{DD} - I_D R_D$$

$$\& V_S = 0V$$

$$V_{DS} = V_D - V_S \quad \text{ie } V_D = V_{DS} + V_S = V_{DS} + 0V$$

$$\& V_D = V_{DD} - I_D R_D$$

$$\& V_{GS} = V_G - V_S$$

$$V_G = V_{GS} + V_S = V_{GS} + 0V$$

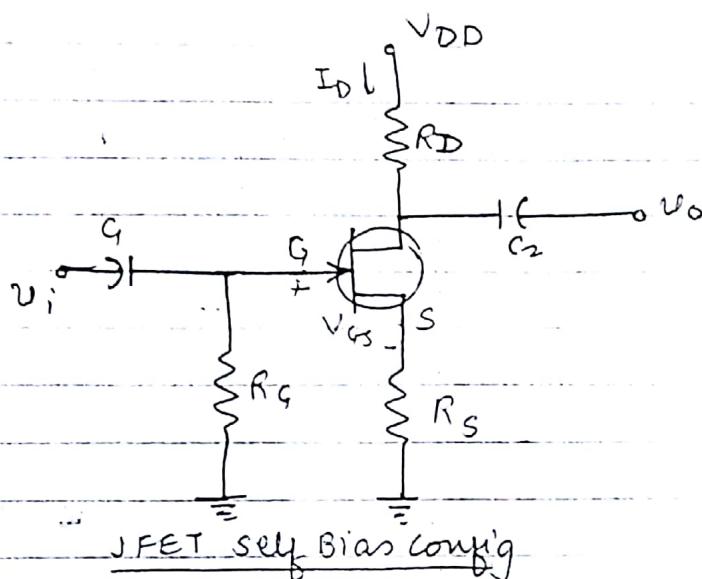
$$V_G = V_{GS}$$

disadvantage: As two power supplies are required it is not preferable.

② Self-Bias Configuration :-

This config eliminates the need for two dc suppliers.

- The controlling gate-to-source V_{GS} is now determined by V_{DS} across a resistor R_S introduced in source leg of the config. shown.



$$I_{RS} = I_S \text{ But } I_S = I_D$$

$$\therefore V_{RS} = I_D \cdot R_S$$

Apply KVL to i/p loop,

$$-V_{GS} - V_{RS} = 0$$

$$\therefore V_{GS} = -V_{RS} \quad \text{or} \quad V_{GS} = -I_D R_S \quad \text{--- (1)}$$

Here V_{GS} is a function of dependent I_D & not fixed in magnitude (like fixed bias config.)

Mathematical solution:-

Mathematical solution could be obtained by

substituting eqn ① into Shockley's Eqn

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

$$= I_{DSS} \left(1 - \frac{-I_D R_S}{V_p} \right)^2$$

$$I_D = I_{DSS} \left(1 + \frac{I_D R_S}{V_p} \right)^2$$

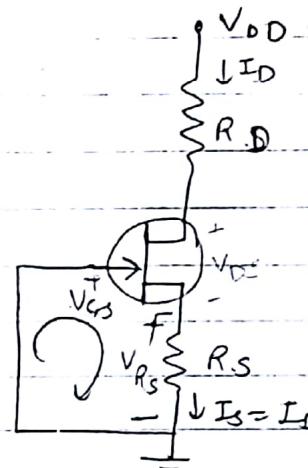
By performing the squaring process indicated & rearranging terms,

DC Analysis :-

capacitors are replaced

by o. c. & R_G 's

replaced by s. c. ($\because I_G = 0$)



DC equivalent of self Bias

We obtain an eqn as follows :-

$$I_D^2 + K_1 I_D + K_2 = 0$$

This quadratic eqn can be solved for the appropriate soln for I_D .

Graphical Approach :-

We first establish the transfer characteristic.

as shown in fig @

- since Eqn ①, defines the straight line on the same graph. For that we should know 2 pts.

1st pt case ① $I_D = 0A$ $V_{GS} = -I_D R_S = 0V \therefore$ one pt on the straight line is defined by $\{I_D = 0A \text{ & } V_{GS} = 0V\}$

2nd pt case ② second pt for eqn ① requires that a level of V_{GS} or I_D be chosen & corresponding levels of I_D & V_{GS} will then define another pt on the straight line

suppose we choose $I_D = \frac{I_{DSS}}{2}$ then $V_{GS} = -I_D R_S = \frac{-I_{DSS}}{2}$

\therefore 2nd pt on the straight line is defined by $\{I_D = \frac{I_{DSS}}{2} \text{ & } V_{GS} = \frac{-I_{DSS}}{2}\}$

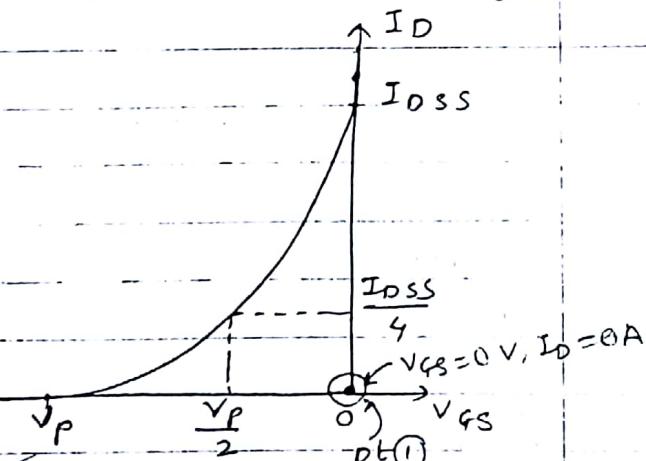


fig @ Defining pt on selfbias line

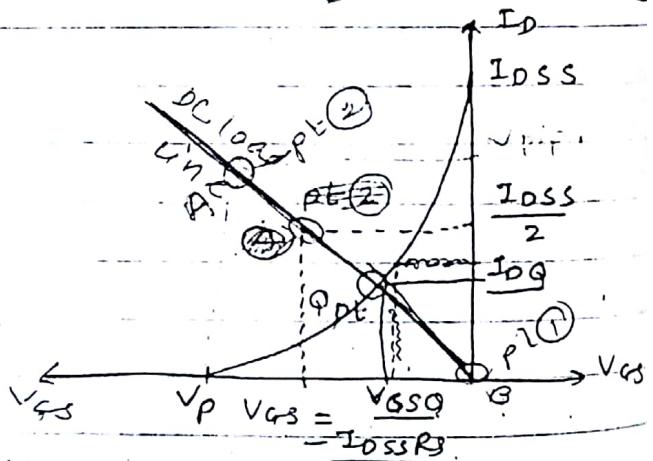


fig ⑥ sketching the selfbias line

- The Q pt obtained at the intersectn of straight line & devic characteristic curve.

o/p resp

Apply KVL to o/p ckt

$$V_{DD} - I_D R_D - V_{DS} - V_{RS} = 0$$

$$V_{RS} + V_{DS} + V_{RD} - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - V_{RS} - V_{RD} = V_{DD} - I_S R_S - I_D R_D$$

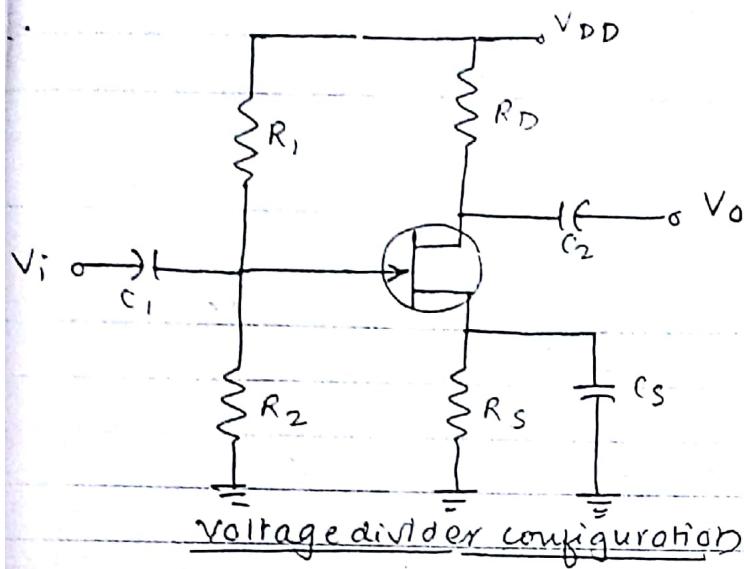
$$\text{But } I_D = I_S \therefore V_{DS} = V_{DD} - I_D (R_S + R_D)$$

$$V_S = I_D R_S, V_G = 0V$$

$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$

③ Voltage divider Biasing

The basic construction of this configuration is same as that of BJTs but the dc analysis of each is different.



DC Analysis :-

all the capacitors including bypass capacitor C_S can be replaced by 0.c equivalent.

Mathematical Approach) -

$$\therefore I_G = 0A,$$

$$KCL \text{ requires } I_{R_1} = I_{R_2}$$

$$\therefore V_G = V_{DD} \text{ across } R_2$$

By VDR we,

$$V_G = \frac{R_2 \cdot V_{DD}}{R_1 + R_2}$$

Apply KVL in the clockwise direction to indicated loop

$$V_G - V_{GS} - V_{RS} = 0$$

$$V_{GS} = V_G - V_{RS}$$

$$\text{Substituting } V_{RS} = I_S R_S = I_D R_S$$

$$V_{GS} = V_G - I_D R_S \quad \text{eqn ①}$$

Redrawn now for dc analysis

Graphical Analysis

- The eqn ① is still the eqn for a straight line. It requires two pts to be defined.

1st pt :- $I_D = 0 \text{ mA}$ into eqn ①,

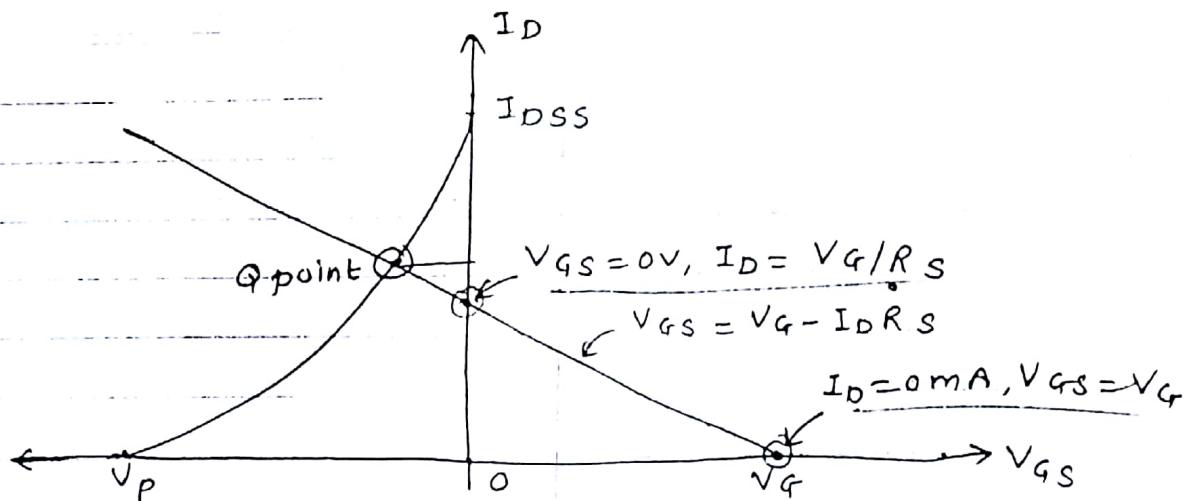
$$V_{GS} = V_G - (0 \text{ mA} \times R_S)$$

$$V_{GS} = V_G \mid I_D = 0 \text{ mA}$$

2nd pt - $V_{GS} = 0 \text{ V}$ put in eqn ①, $V_{GS} = V_G - I_D R_S$

$$0 = V_G - I_D R_S$$

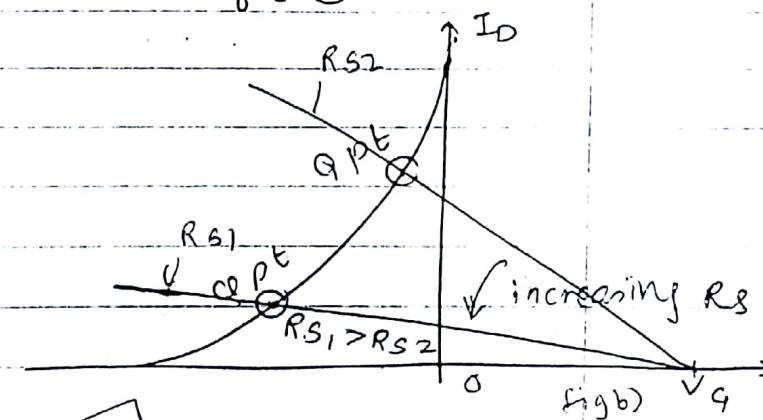
$$\therefore \left\{ I_D = \frac{V_G}{R_S} \mid V_{GS} = 0 \text{ V} \right.$$



fig@ sketching the N/W eqn for the Voltage divider config.

intersection on vertical axis is determined by $ID = \frac{VG}{RS}$ & V_G is fixed by I_D N/W.

If we increase values of RS , $\frac{ID}{V_G}$ will reduce the intersection shown in fig. (b)



Increasing value of RS result in lower quiescent values of ID & more -ve values of V_G .

effect of RS on results

O/p side

Apply KVL to o/p side

$$V_{DD} - I_{D1} R_D - I_{D2} R_S = 0 \quad V_{DD} - I_{D1} R_D + I_{D2} R_S = 0$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

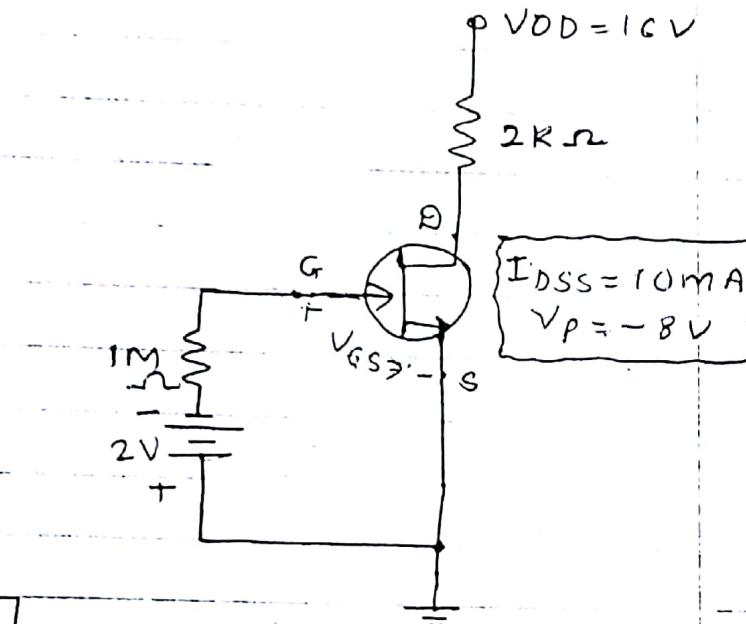
$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$

x1) Determine the following for the N/W given.

- (a) V_{GSQ}
- (b) I_{DQ}
- (c) V_{DS}
- (d) V_D
- (e) V_g
- (f) V_s



Sol :-

Mathematical Approach :-

$$a) V_{GSQ} = -V_{GG} = -2V$$

$$b) I_{DQ} = ID_{SS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{mA} \left(1 - \frac{-2V}{-8V}\right)^2$$

$$I_{DQ} = 5.625\text{mA}$$

$$c) V_{DS} = V_{DD} - I_{DQ} R_D = 16V - (5.625\text{mA})(2k\Omega)$$

$$V_{DS} = 4.75V$$

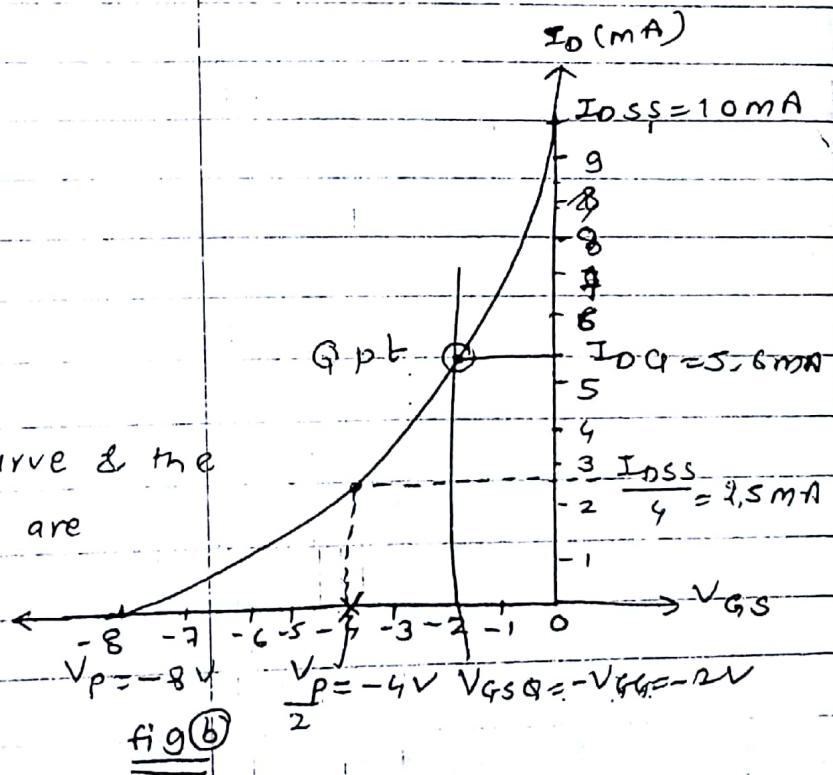
$$d) V_D = V_{DS} = 4.75V$$

$$e) V_g = V_{GS} = -2V$$

$$f) V_s = 0V$$

Graphical Approach :-

The resulting Shockley curve & the vertical line at $V_{GS} = -2V$ are provided in fig (b).



It is certainly difficult to read beyond the second place with significantly increasing the size of the fig, but a sol'n of s.g. from the graph of fig (b), is quite acceptable.

$$\therefore a) V_{GSQ} = -V_{GG} = \underline{-2V}$$

$$b) I_{DQ} = \underline{5.6mA}$$

$$c) V_{DS} = V_{DD} - I_{DRD}$$

$$= 16V - (5.6mA \times 2k\Omega)$$

$$= \underline{4.8V}$$

$$d) V_D = V_{DS} = \underline{4.8V}$$

$$e) V_G = V_{GS} = \underline{-2V}$$

$$f) V_S = \underline{0V}$$

The results clearly confirm the fact that the mathematical & graphical approaches generate so that are quite close.

Ex 2.) Determine the following for the n/w of given fig.

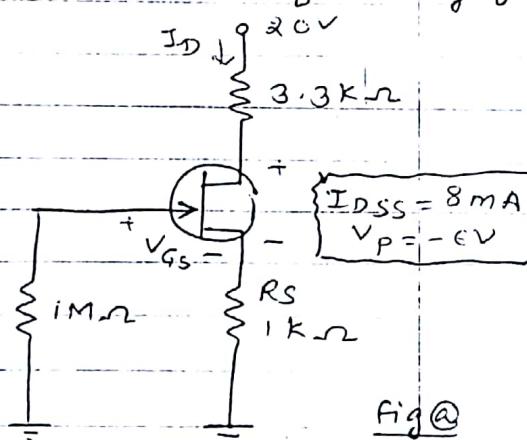


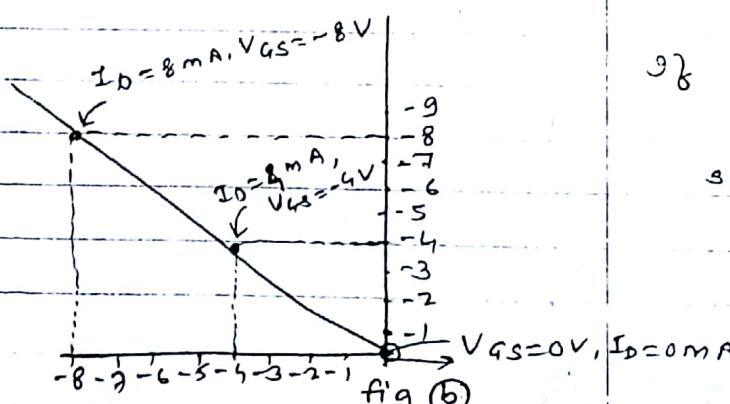
Fig @

- (a) V_{GSQ}
- (b) I_{DQ}
- (c) V_{DS}
- (d) V_S
- (e) V_G
- (f) V_D

Sol'n. a) $V_{GS} = -I_D R_S$ If we choose $I_D = 4mA$
 $= (-4mA \times 1k\Omega)$

$$V_{GS} = \underline{-4V}$$

If we plot this \rightarrow it is shown in fig (b)



If we choose $V_{GS} = V_P/2 = -3V$
 $I_D = I_{DSS}/4 = 2mA$
 so fig (c) is the plot of this.

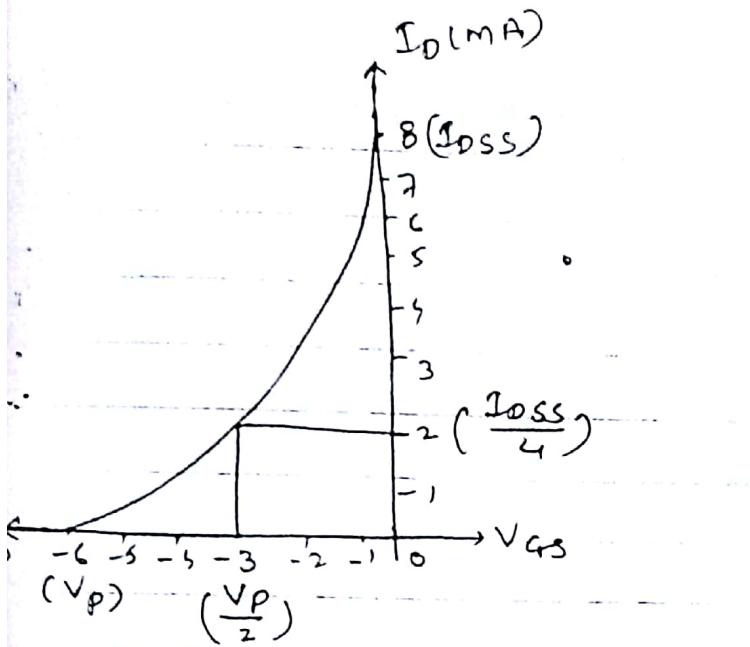


fig (c) sketching device characteristics for JFET

The solution is obtained by superimposing the new characteristic defined by fig (b) on the device characteristics of fig (c) & finding the point of intersection of the two as indicated in fig (d).

The resulting operating pt results in a quiescent value of gate to source voltage of $V_{GSQ} = -2.6V$

(b) At quiescent pt

$$I_{DQ} = 2.6 \text{ mA}$$

$$\begin{aligned} (c) \quad V_{DS} &= V_{DD} - I_D (R_s + R_D) \\ &= 20V - [(2.6 \text{ mA}) \\ &\quad (1k\Omega + 3.3k\Omega)] \end{aligned}$$

$$V_{DS} = 8.82V$$

fig (d) Determining op pt for N/W of given fig.

$$(d) \quad V_S = I_{DR_s} = (2.6 \text{ mA}) (1k\Omega) = 2.6V$$

$$(e) \quad V_G = 0V$$

$$(f) \quad V_D = V_{DS} + V_S = 8.82V + 2.6V = 11.42V$$

$$(g) \quad \text{or } V_D = V_{DD} - I_D R_D = 20V - (2.6 \text{ mA} \times 3.3k\Omega) = 11.42V$$

Ex3- find the quiescent point for the N/W of given fig Q

if @ $R_s = 100 \Omega$ (b) $R_s = 10 k\Omega$

$R_s = 100 \Omega$
 $I_D = 4 \text{ mA}, V_{GS} = -0.4 \text{ V}$

$R_s = 10 k\Omega$
 $V_{GS} = -4 \text{ V}, I_D = 0.4 \text{ mA}$

$V_{GSQ} \approx -4.6 \text{ V}$

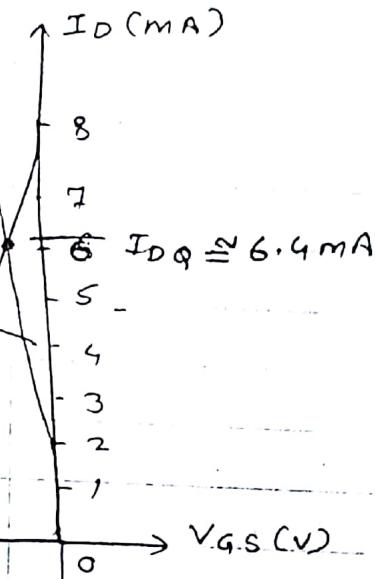


fig @

(a) With I_D scale, $I_{DQ} \approx 6.4 \text{ mA}$

from eqn $V_{GS} = -I_D R_s$ $V_{GSQ} \approx -0.64 \text{ V}$

(b) With V_{GS} scale, $V_{GSQ} \approx -4.6 \text{ V}$

from eqn $V_{GS} = -I_D R_s$, $I_{DQ} \approx 0.46 \text{ mA}$

In particular, note how lower levels of R_s bring the load line of the N/W, closer to the I_D axis, whereas increasing levels of R_s bring the loadline closer to V_{GS} axis.

0	I_{DSS}
0.3V _P	$I_{DSS}/4$
0.5V _P	$I_{DSS}/2$
V _P	0

Ex 4. Determine the following for the N/W given in fig (a)

- (a) I_{DQ} & V_{GSQ} (b) V_D (c) V_s (d) V_{DS} (e) V_{DG}

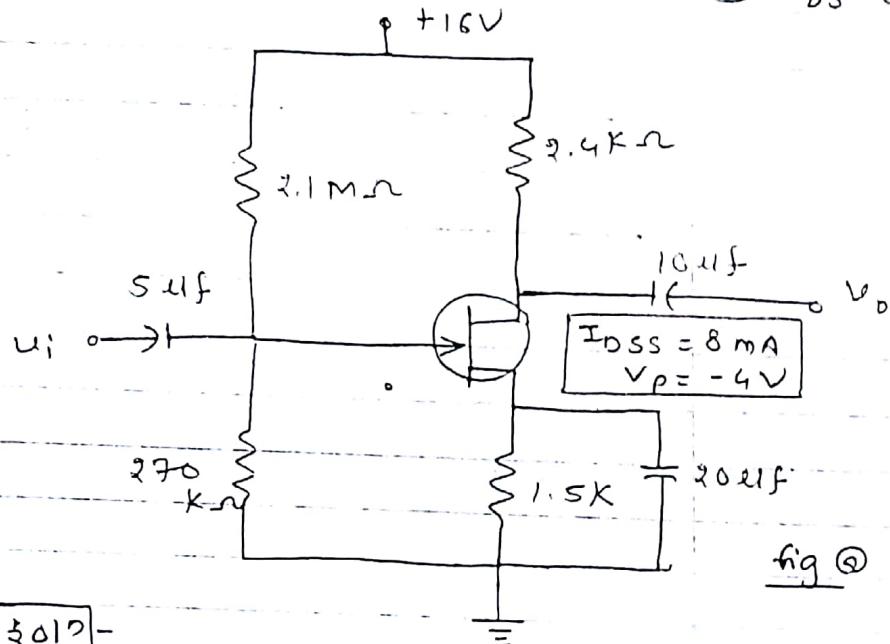


fig (a)

\$017-

For the transfer characteristics if $I_D = I_{DSS}/4 = 8 \text{ mA}/4 = 2 \text{ mA}$
then $V_{GS} = V_P/2 = -4 \text{ V}/2 = -2 \text{ V}$.

The resulting curve representing Shockley's Eqn appears as shown in fig (b)

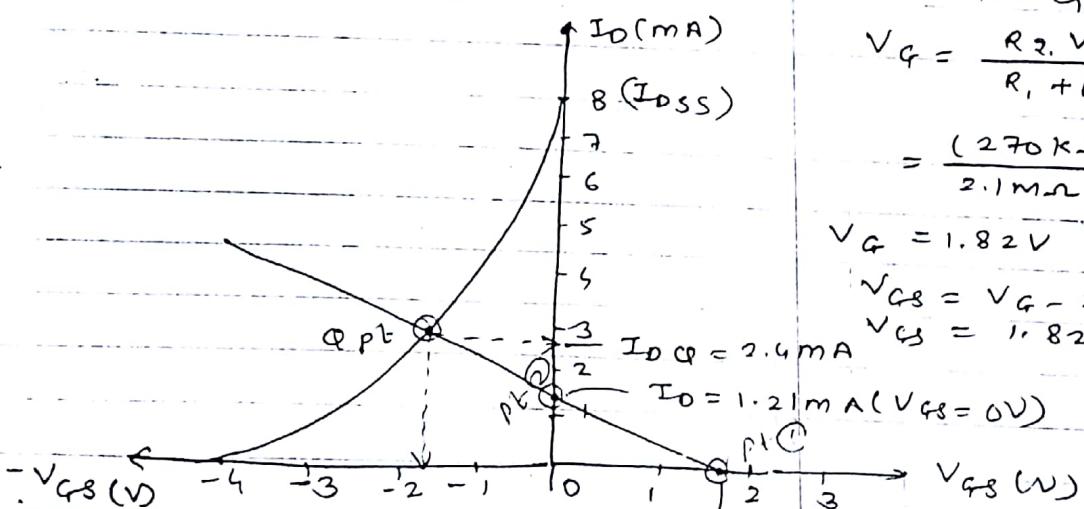


fig (b) determining Q_{pt} ($V_G = 1.82 \text{ V}$)
($I_D = 0 \text{ mA}$)

$$V_{GS} = 1.82 \text{ V} - I_D (1.5 \text{ k}\Omega)$$

$$\text{if } I_D = 0 \text{ mA} \quad V_{GS} = +1.82 \text{ V}$$

$$\text{if } V_{GS} = 0 \text{ V}, \quad I_D = \frac{1.82 \text{ V}}{1.5 \text{ k}\Omega} = 1.21 \text{ mA}$$

pt ① ($I_D = 0 \text{ mA}, V_G = 1.82 \text{ V}$)

pt ② ($V_{GS} = 0 \text{ V}, I_D = 1.21 \text{ mA}$)

The resulting bias line appears on fig (b) with Q_{pt} value -

or $I_{DQ} = 2.4 \text{ mA} \quad V_{GSQ} = -1.8 \text{ V}$

⑥ $V_D = V_{DD} - I_D R_D$
 $= 16V - (2.4mA \times 2.4k\Omega)$
 $\underline{V_D = 10.24V}$

⑦ $V_S = I_D R_S = (2.4mA \times 1.5k\Omega) = \underline{3.6V}$

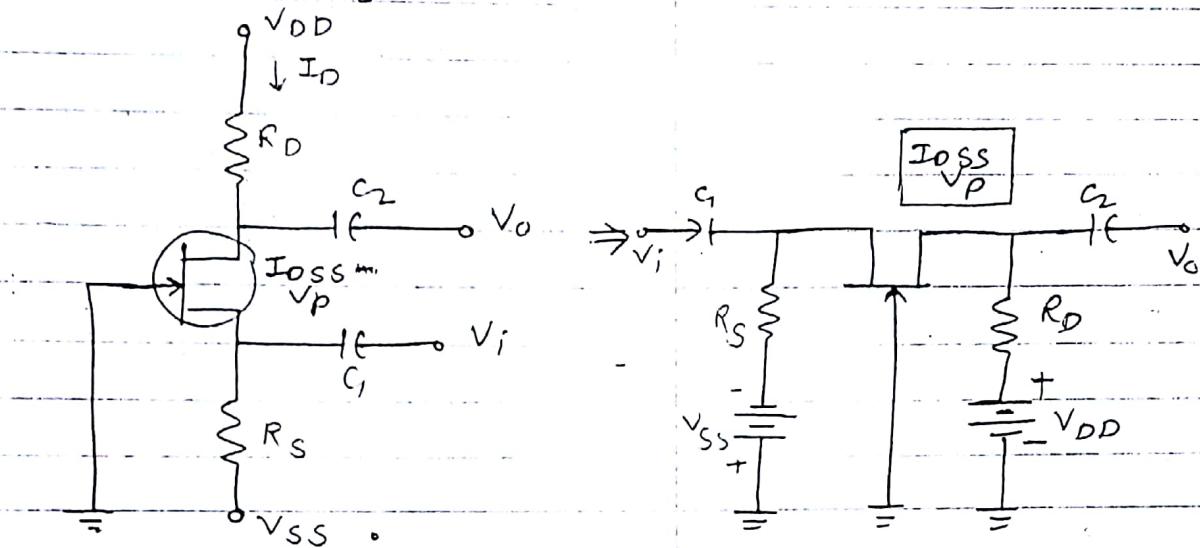
⑧ $V_{DS} = V_{DD} - I_D (R_D + R_S)$
 $= 16V - (2.4mA) (2.4k\Omega + 1.5k\Omega)$
 $\underline{V_{DS} = 6.64V}$

OR $V_{DS} = V_D - V_S = 10.24V - 3.6V$
 $\underline{V_{DS} = 6.64V}$

⑨ $V_{DG} = V_D - V_G$
 $= 10.24V - 1.82V$
 $\underline{V_{DG} = 8.42V}$

④ Common Gate Configuration:-

In this configuration, gate terminal is grounded & input signal typically applied to the source terminal & the output signal obtained at the drain terminal as shown in fig @.



fig@ Two versions of the common gate configuration

The N/W eqⁿ can be determined using fig (b)

Applying KVL in the direction shown in fig (b)

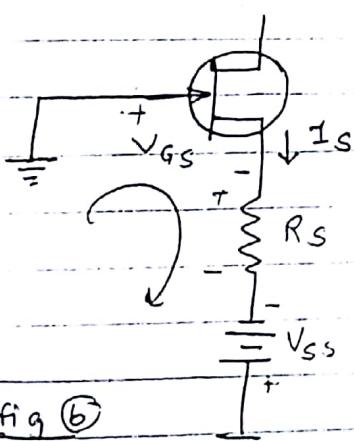


fig (b)

determining the N/W eqⁿ for the config. of fig @

$$-V_{GS} - I_s R_S + V_{SS} = 0$$

$$V_{GS} = V_{SS} - I_s R_S$$

$$I_s = I_D$$

$$V_{GS} = V_{SS} - I_D R_S \quad \text{--- (1)}$$

Applying the condⁿ $I_D = 0 \text{ mA}$ to eqⁿ (1),

$$V_{GS} = V_{SS} - (0 \times R_S)$$

$$V_{GS} = V_{SS} / I_D = 0 \text{ mA}$$

Applying the condⁿ $V_{GS} = 0 \text{ V}$ to eqⁿ (1),

$$0 = V_{SS} - I_D R_S$$

$I_D = \frac{V_{SS}}{R_S}$	$ $	$V_{GS} = 0 \text{ V}$
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The resulting load line appears in fig @ intersecting the transfer curve for JFET as shown.

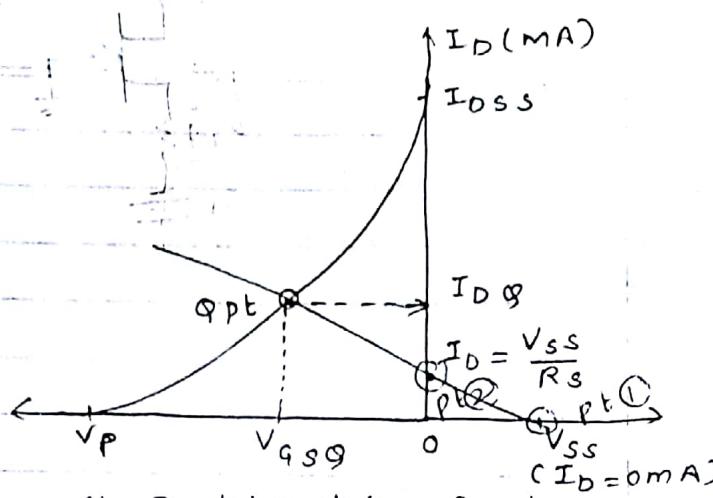


Fig @ determining Q pt
for the N/W of fig ⑥

Applying KVL across both sources of fig @,

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS}$$

$$\text{substituting } I_S = I_D$$

$$V_{DD} + V_{SS} - V_{DS} = I_D (R_D + R_S)$$

$$\therefore V_{DS} = V_{DD} + V_{SS} - I_D (R_D + R_S)$$

$$\text{with } V_D = V_{DD} - I_D R_D$$

$$V_S = -V_{SS} + I_D R_S$$

* Special case $V_{GS0} = 0V$ -

because of its relative simplicity is the configuration of fig shown.

- Note that direct connection of the gate & source terminals to ground resulting in $V_{GS} = 0V$.
- It specifies that for any dc condn the gate to source voltage must be zero volts.
- This will result in a vertical load line at $V_{GS0} = 0V$ as shown.

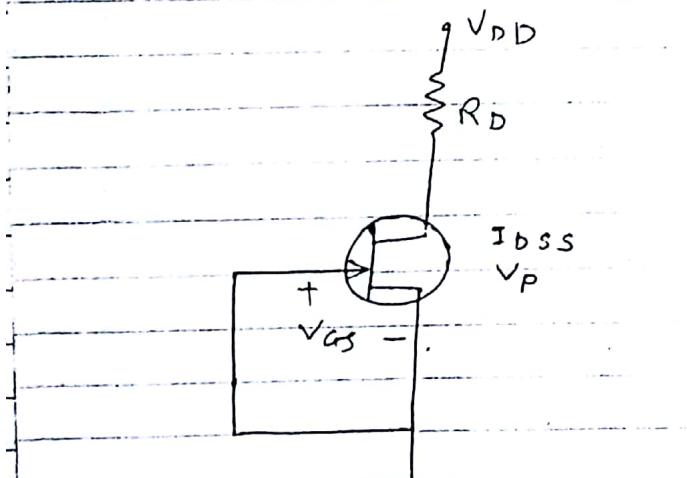
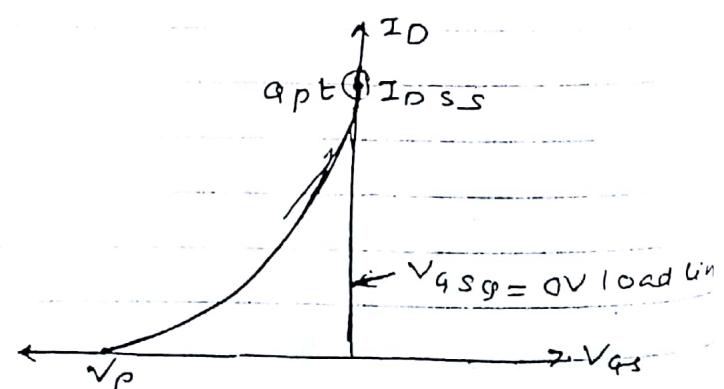


fig @ special case $V_{GS0} = 0V$ config.

Since the transfer curve of a JFET will cross the vertical axis at I_{DSS} , the drain current for the N/W is set at that value.



Finding Q pt for the N/W of fig @

$$I_{DQ} = I_{DS}$$

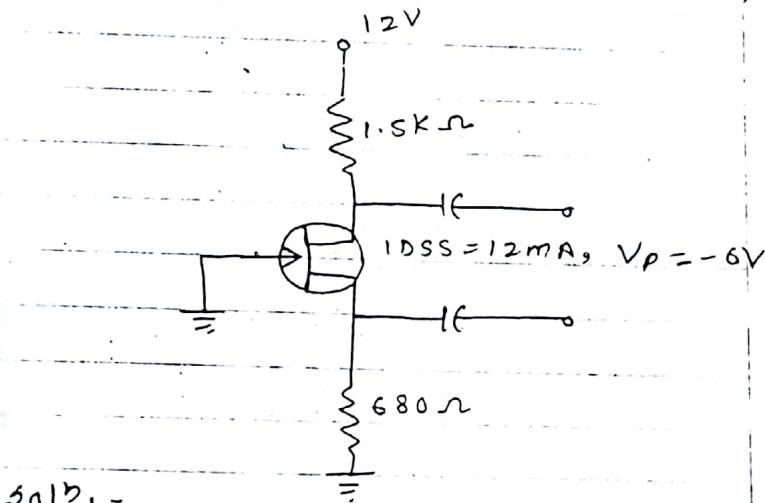
Apply KVL

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$\text{with } V_D = V_{DS} \text{ & } V_S = 0V$$

- Ex 1) Determine the following for the common gate configuration of fig shown.
 a) V_{GS} b) I_{DQ} c) V_D d) V_g e) V_s f) V_{DS}



V_{GS} (V)	I_D (mA)
0	I_{DS}
$0.3V_p$	$I_{DS}/2$
$0.5V_p$	$I_{DS}/4$
V_p	0

Soln. -

Even though V_{SS} is not present in this common gate config, the eqns derived above can still be used by simply substituting $V_{SS} = 0V$ into each eqn in which it appears.

- a) For the transfer characteristics

$$V_{GS} = V_{SS} - I_D R_S = 0 - I_D R_S$$

$$V_{GS} = -I_D R_S \quad \text{if } I_D = 0, V_{GS} = 0 \quad \text{pt ①} \quad (\text{at } I_D = 0, V_{GS} = 0)$$

For this eqn the origin is one point on the load line while the other must be determined at some arbitrary pt.

choosing $I_D = 6mA$ & solving for V_{GS} will result in

$$V_{GS} = -I_D R_S = -(6mA \times 680\Omega) = -4.08V$$

as shown in fig. pt ②, ($I_D = 6mA, V_{GS} = -4.08V$)

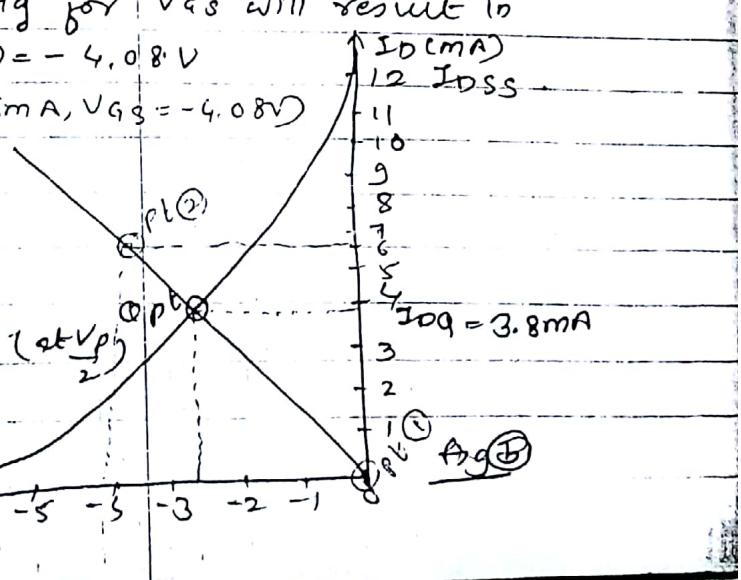
The device transfer curve is sketched using

$$I_D = \frac{I_{DS}}{4} = \frac{12mA}{4} = 3mA \left(\text{at } V_p \right)$$

$$\therefore V_{GS} \approx 0.3V_p = 0.3(-6V)$$

$$= -1.8V \quad \text{(at } I_D = \frac{I_{DS}}{2} \text{)}$$

$$(V_p)$$



\therefore resulting soln is

(b) from fig (b)

$$V_{GSQ} \approx -2.6 V$$

$$I_{DQ} \approx 3.8 \text{ mA}$$

(c) $V_D = V_{DD} - I_D R_D$
 $= 12V - (3.8 \text{ mA} \times 1.5 \text{ k}\Omega)$

$$\underline{\underline{V_D = 6.3 V}}$$

(d) $\underline{\underline{V_G = 0 V}}$

(e) $V_S = I_D R_S = (3.8 \text{ mA})(680 \Omega) = \underline{\underline{2.58 V}}$

(f) $V_{DS} = V_D - V_S$
 $= 6.3 V - 2.58 V$

$$\underline{\underline{V_{DS} = 3.72 V}}$$

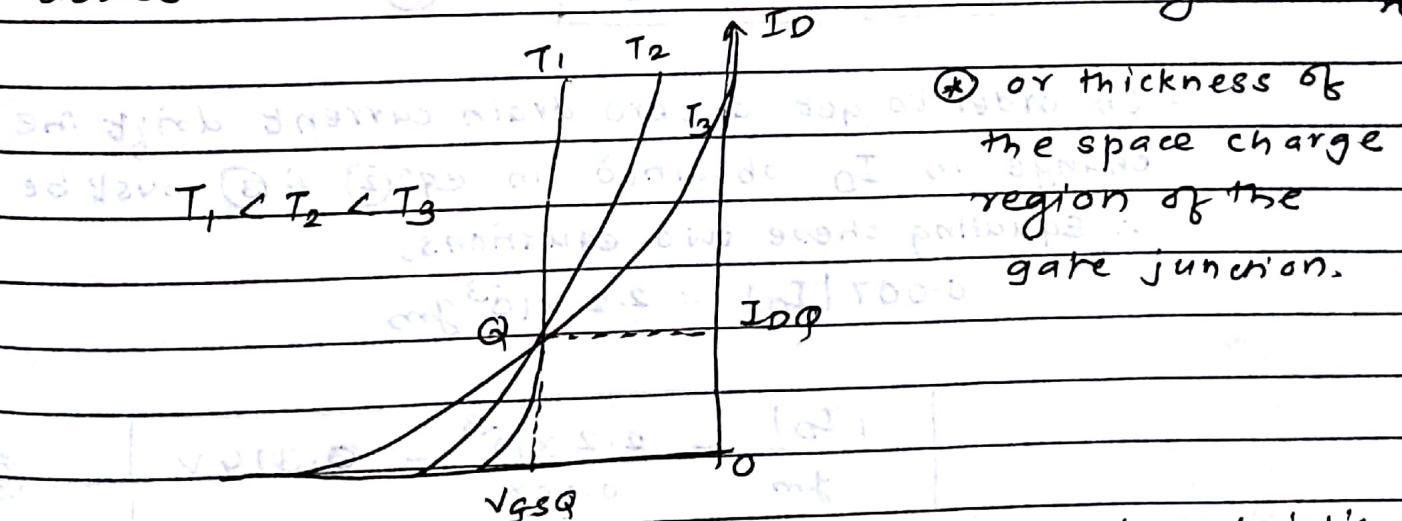
* Biasing JFET for zero current drift :-

- Transfer characteristic of JFET drifts with variation of temperature.
- Fig. shows transfer characteristics of n-channel JFET as a function of temperature.
- From the fig, it is seen that there is a value of V_{GS} for which I_D does not change with temperature. Hence it is possible to bias a JFET for zero drain current drift with respect to temperature.
- When temperature increases, the mobility decreases.

$$M = V/E$$

- The variation or drift of transfer characteristic can be explained with the help of two factors that affect drain current when temperature changes.

- ① First factor is the decrease in majority-carrier mobility with temperature.
- ② Second factor is reduction in channel width with rise in temperature. The barrier potential across the channel reduces with increasing temperature.



- From fig, it can be seen that transfer characteristics shift with changes in temperature.

But there exist a value of V_{GS} (θ) for which $I_D = I_{D\theta}$ does not change with temperature. This point θ is called as the zero drain current drift point. It is therefore possible to bias a FET for zero drain current drift.

- If we change gate voltage ΔV_{GS} then drain current also changes

$$\Delta I_D = g_m \Delta V_{GS} \quad (1)$$

But V_{GS} changes at 2.2 mV per increase of 1°C .

Hence the change in I_D due to change in V_{GS} for 1°C change in temperature is given by,

$$\Delta I_D = g_m \times 2.2 \times 10^3 \text{ V} \quad (2)$$

- Also change in I_D per 1°C increase in temperature, due to change in the mobility of charge carriers is given by,

$$\Delta I_D = 0.7 \% |I_D|$$

$$\Delta I_D = 0.007 |I_D| \quad (3)$$

- In order to get a zero drain current drift the change in I_D obtained in eqn (2) & (3) must be equal.
∴ Equating these two equations,

$$0.007 |I_D| = 2.2 \times 10^3 g_m$$

$$\frac{|I_D|}{g_m} = \frac{2.2 \times 10^3}{0.007} = 0.314 \text{ V} \quad (4)$$

Substitute

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2 \quad \text{and } g_m = \frac{-2 I_{DSS}}{V_p} \left(1 + \frac{V_{GS}}{V_p} \right)$$

in eqn (4) to get,

$$|V_{pl}| - |V_{gs}| = 0.63V$$

—(5)

If V_p is known, eqn (5) gives value of V_{gs} for zero drift.

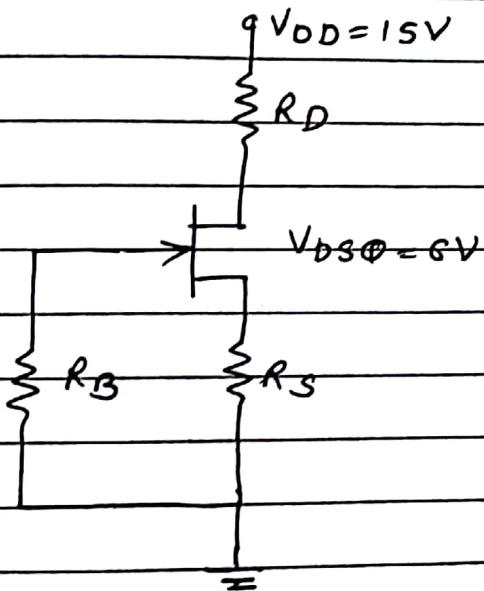
$$|V_{gs}| = |V_{pl}| - 0.63V$$

—(6)

Thus by adjusting the value of V_{gs} to satisfy eqn (6), it is possible to bias an FET for zero drift.

Ex1. Design the zero temperature drift bias circuit to provide $V_{DSQ} = 6V$. Use FET with $I_{DSS} = 8mA$ & $V_p = -4V$ & $V_{DD} = 15V$

Soln- Assume ckt has self bias configuration.



① cond' to be satisfied to obtain a zero temperature drift is

$$\begin{aligned} |V_{gs}| &= |V_p| - 0.63 \\ &= 4 - 0.63 \\ &= -3.37V \end{aligned}$$

② $I_{DQ} \Rightarrow$

$$\begin{aligned} I_{DQ} &= I_{DSS} \left[1 - \frac{|V_{gs}|}{|V_p|} \right]^2 \\ &= 8 \left[1 - \frac{-3.37}{-4} \right]^2 \end{aligned}$$

$$I_{DQ} = 0.1985mA$$

③ $V_{gs} = -I_{DQ}R_S$ for self bias

$$R_S = -\frac{V_{gs}}{I_{DQ}} = \frac{3.37}{0.1985} = 16.98k\Omega$$

⑤ select $R_B = 1M\Omega$

$$⑥ R_D = 30.22k\Omega$$

$$R_S = 16.98k\Omega$$

$$R_B = 1M\Omega$$

④ Apply KVL to drain current.

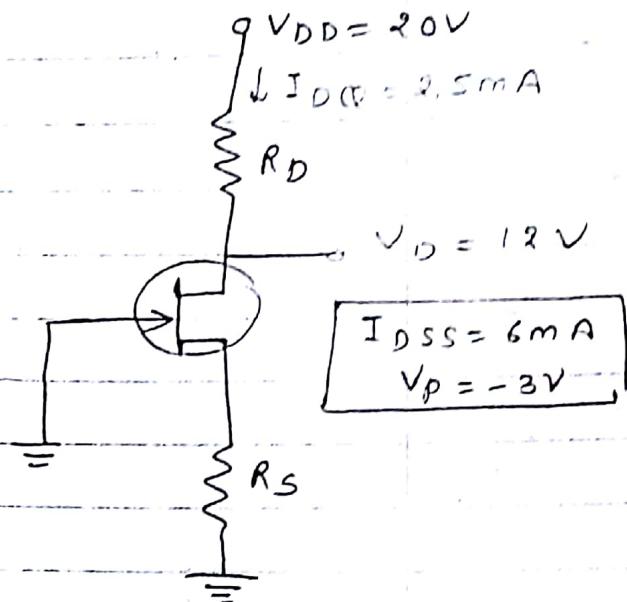
$$V_{DD} = I_{DQ}R_D + V_{DSQ} + I_{DQ}R_S$$

$$= (0.1985 \times R_D) + 6 + 3$$

$$R_D = 30.22k\Omega$$

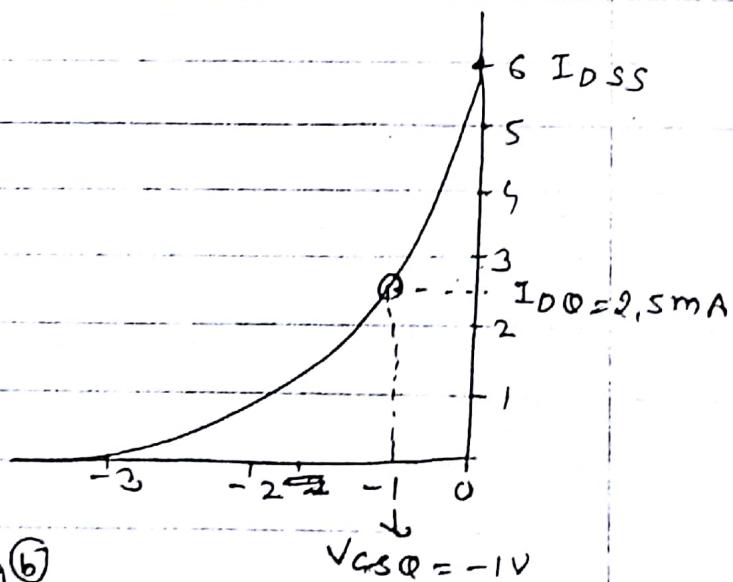
Design Examples

(Ex1) For the Nlw of given fig, the levels of V_{DD} & I_{DQ} are specified. determine the required levels of R_D & R_S . What are the closest standard commercial values?



$$R_D = \frac{V_{RD}}{I_{DQ}} = \frac{V_{DD} - V_D}{I_{DQ}} = \frac{20V - 12V}{2.5mA} = 3.2k$$

Plotting the transfer curve in fig(6) & drawing a horizontal line at $I_{DQ} = 2.5mA$ result in $V_{GSQ} = -1V$ & applying $V_{GS} = -I_{DQ}R_S$ establishes the level of R_S .



$$R_S = \frac{-(V_{GSQ})}{I_{DQ}} = \frac{-(-1V)}{2.5mA} = 0.4k$$

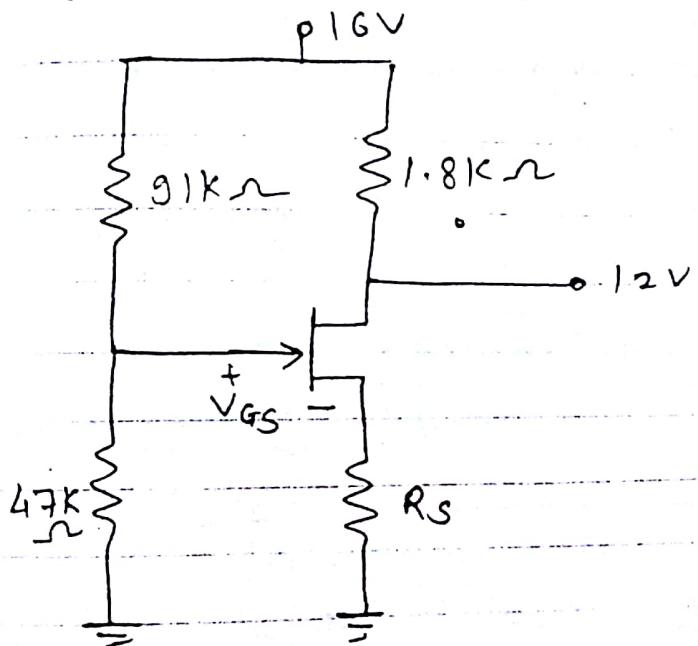
∴ Nearest std values are

$$\boxed{R_D = 3.2k\Omega \Rightarrow 3.3k\Omega}$$

$$\boxed{R_S = 0.4k\Omega \Rightarrow 0.39k\Omega}$$

Determining V_{GSQ} for Nlw of given fig.

(Q2) For the voltage divider bias configuration of given fig, if $V_D = 12V$ & $V_{GSQ} = -2V$. Determine value of R_S .



Ans:-

$$V_G = \frac{R_2 \cdot V_{DD}}{R_1 + R_2} = \frac{47k \times 16V}{(47+91k)}$$

$$V_G = 5.44V$$

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{16V - 12V}{1.8k\Omega} = 2.22mA$$

$$V_{GS} = V_G - I_D R_S$$

$$-2V = 5.44V - (2.22mA \times R_S)$$

$$R_S = \frac{7.44V}{2.22mA} = 3.35k\Omega$$

$$\therefore R_S = 3.3k\Omega \text{ (std)}$$