

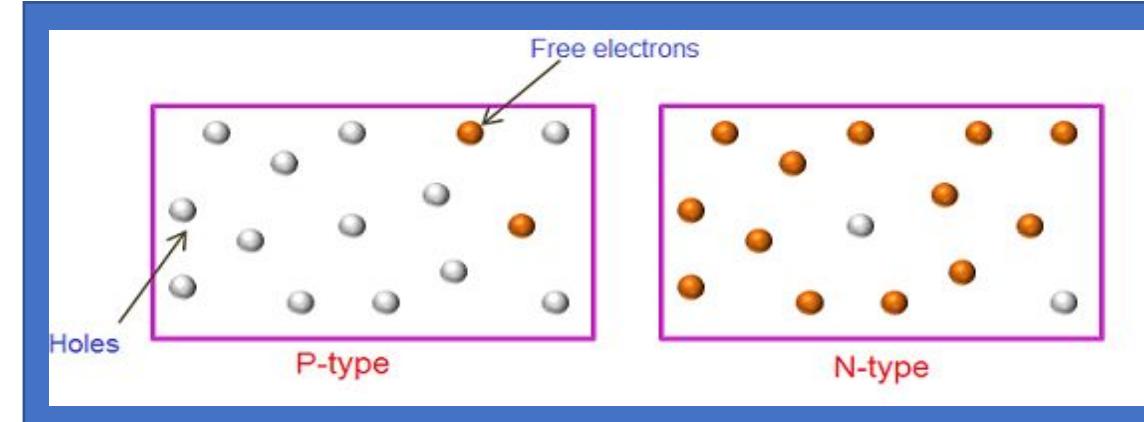
CHAPTER 1- INTRODUCTION OF ELECTRONIC DEVICES

-MRS RASIIKA B. NAIK

POINTS TO BE COVERED IN TODAYS CLASS

- DC Load Line analysis
- Common Base Configuration
- Input Output Characteristics of CB configuration
- Common Collector Configuration
- Input Output Characteristics of CC configuration
- Comparison of CE, CB and CC

PN JUNCTION



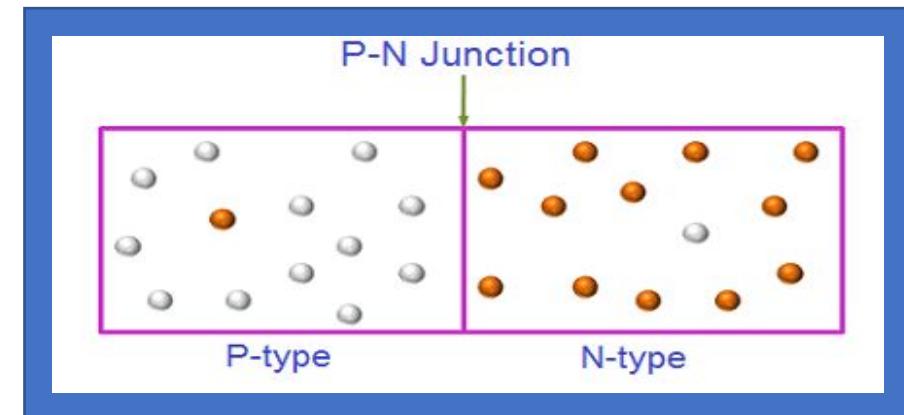
• n-type semiconductor

- ✓ formed by adding pentavalent impurities (like Phosphorus (P), Arsenic (As), Antimony (Sb)) to the intrinsic semiconductor.
- ✓ electrons are the majority carriers while holes are the minority carriers.

• p-type semiconductor

- ✓ formed by adding trivalent impurities (like Boron (B), Gallium (G), Indium(In), Aluminium(Al)) to the intrinsic semiconductor.
- ✓ holes are the majority carriers while electrons are the minority carriers.

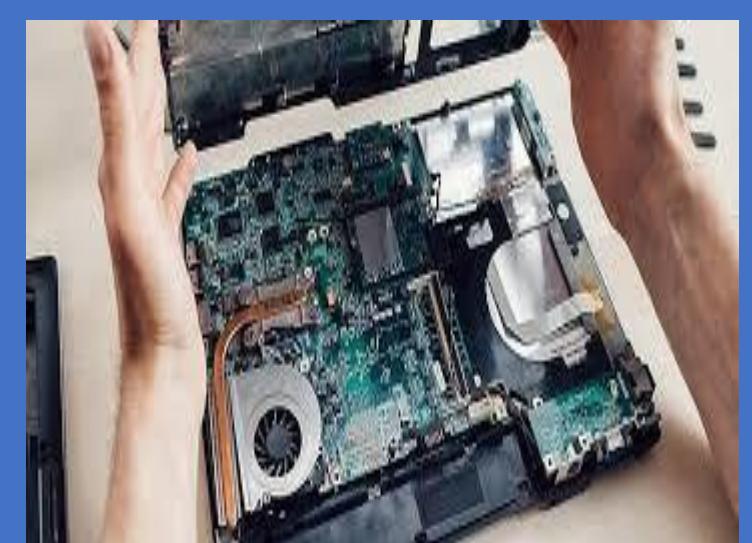
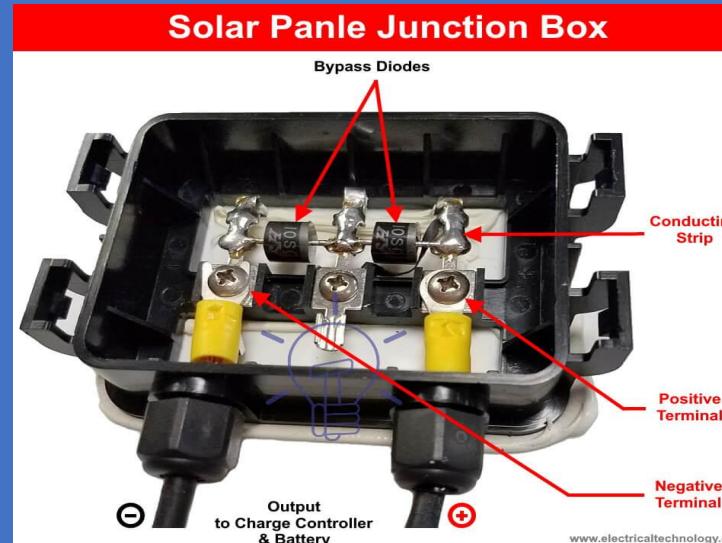
FORMATION OF P-N JUNCTION



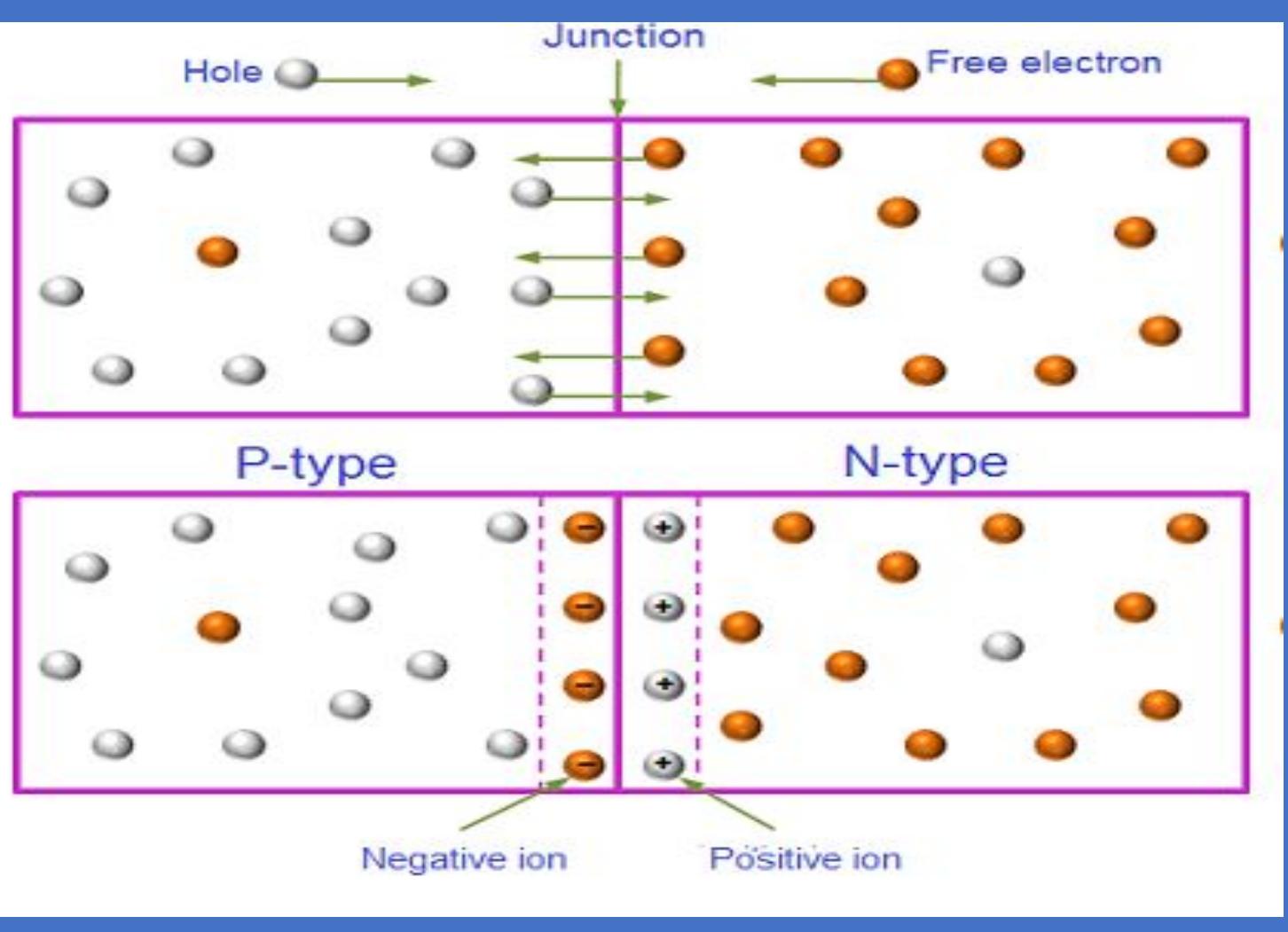
- when an n-type semiconductor is joined with the p-type semiconductor, a p-n junction is formed.
- The region where the p-type and n-type semiconductors are joined is called p-n junction.
- It is also defined as the boundary between p-type and n-type semiconductor.
- This p-n junction forms a most popular semiconductor device known as diode.
- The credit of discovery of the p-n junction goes to American physicist Russel Ohl of Bell Laboratories.

WHY ARE WE STUDYING DIODES/SEMICONDUCTOR DEVICES?

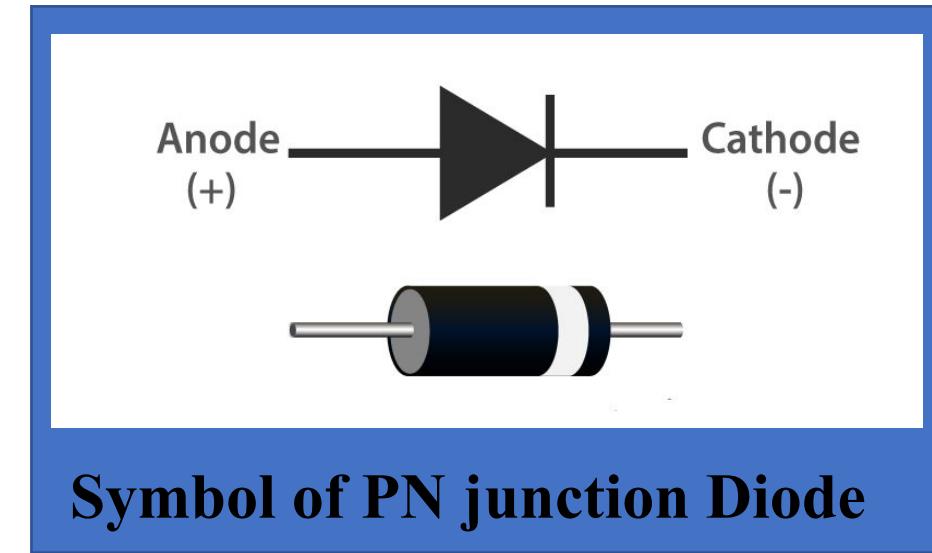
- Diodes are the simplest form of all the semiconductor devices.
- Semiconductor devices are the fundamental building blocks of all the electronic devices such as computers, control systems, ATM (Automated Teller Machine), mobile phones, amplifiers, etc.
- The various applications of diodes include computers, power supplies, television, radios and so on.



PN JUNCTION DIODE



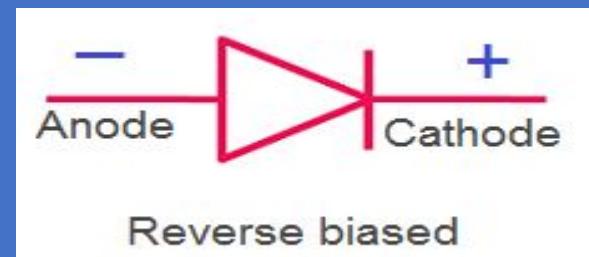
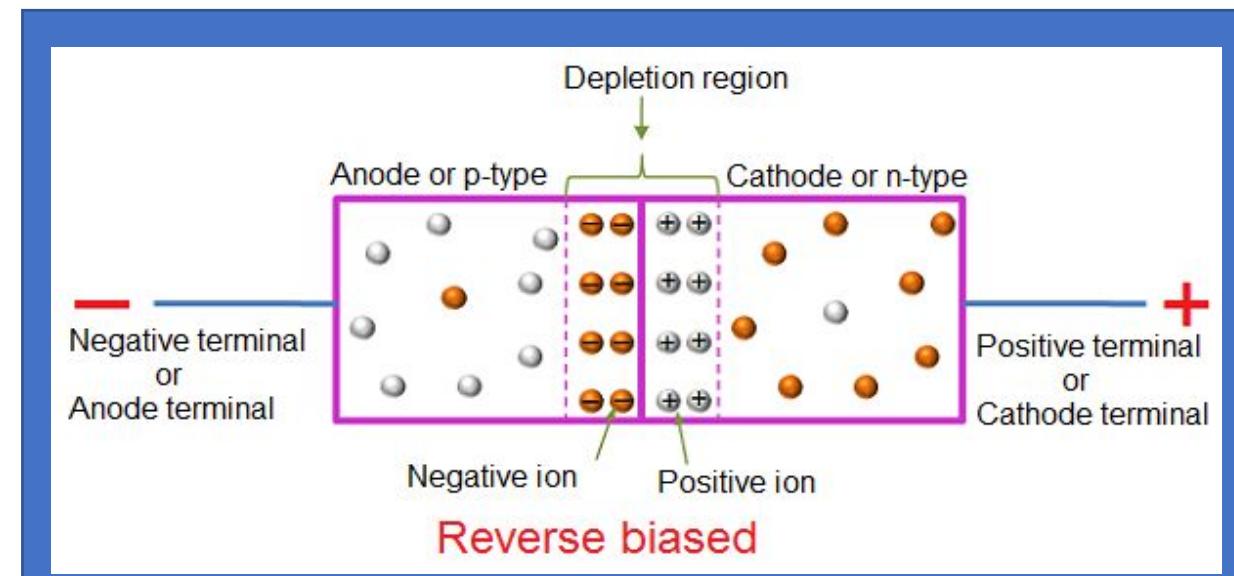
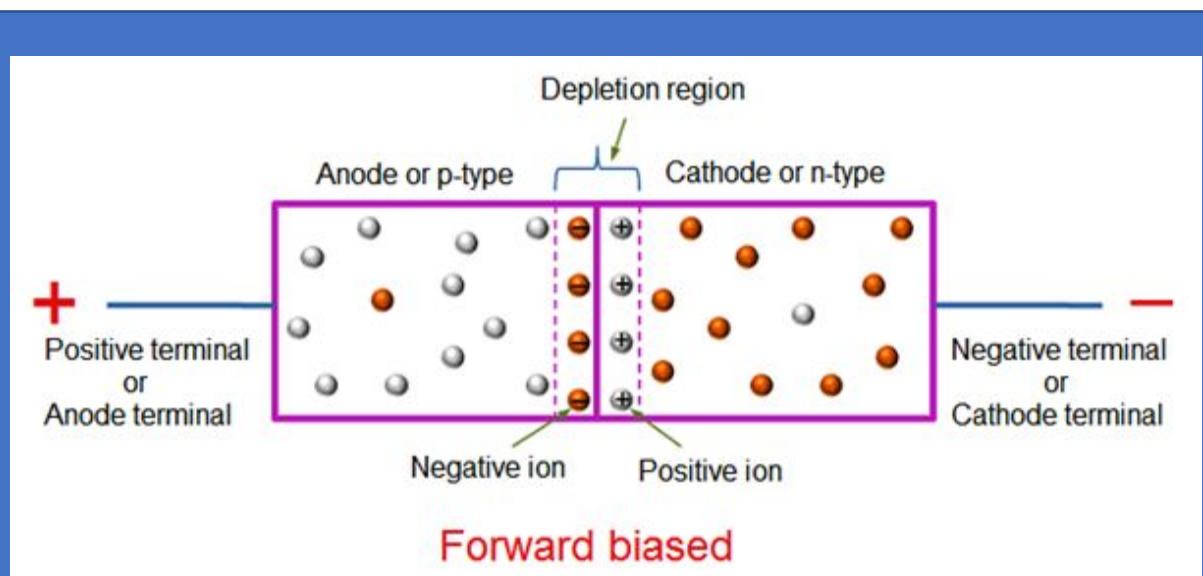
Zero biased or Unbiased PN junction Diode



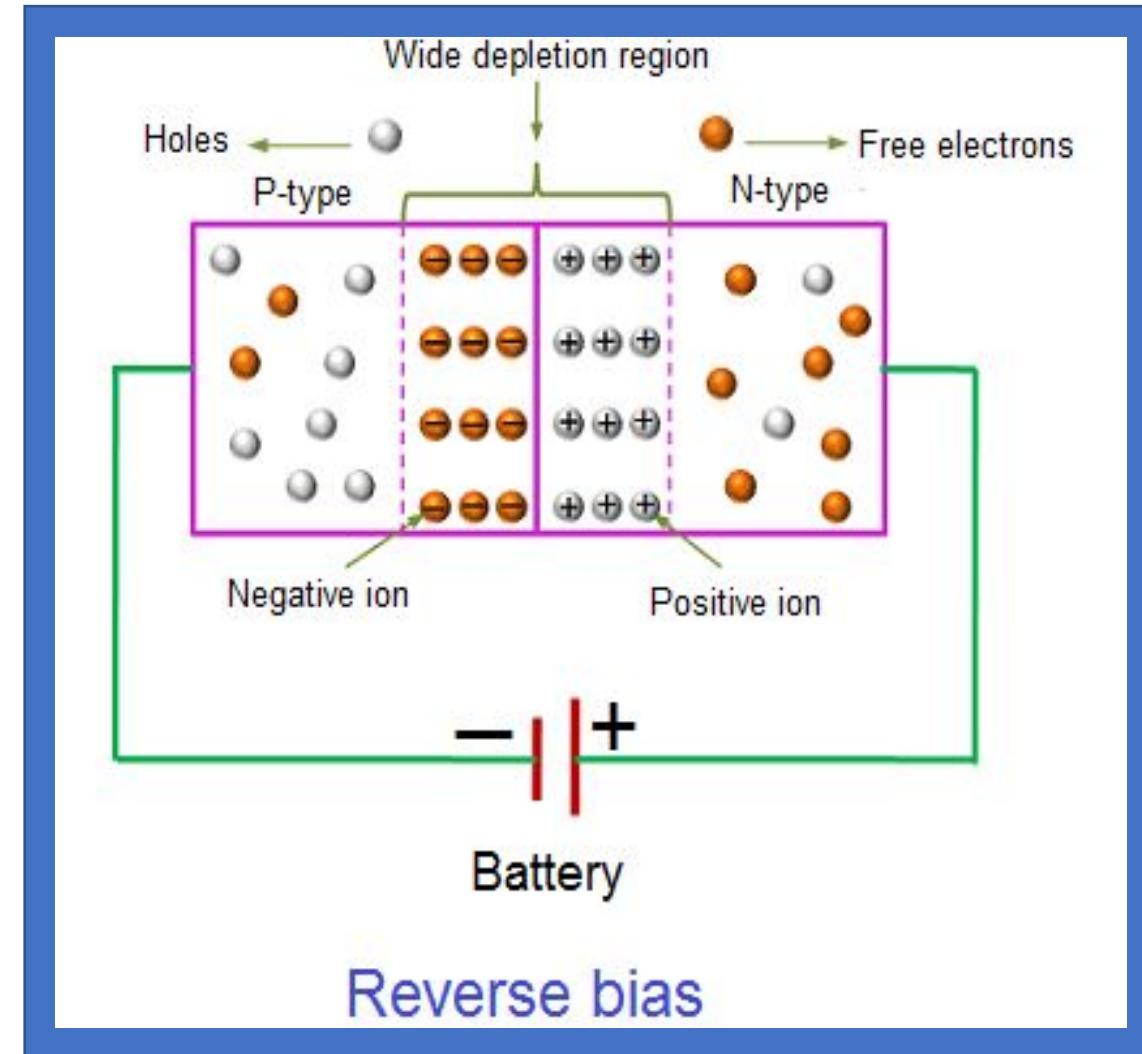
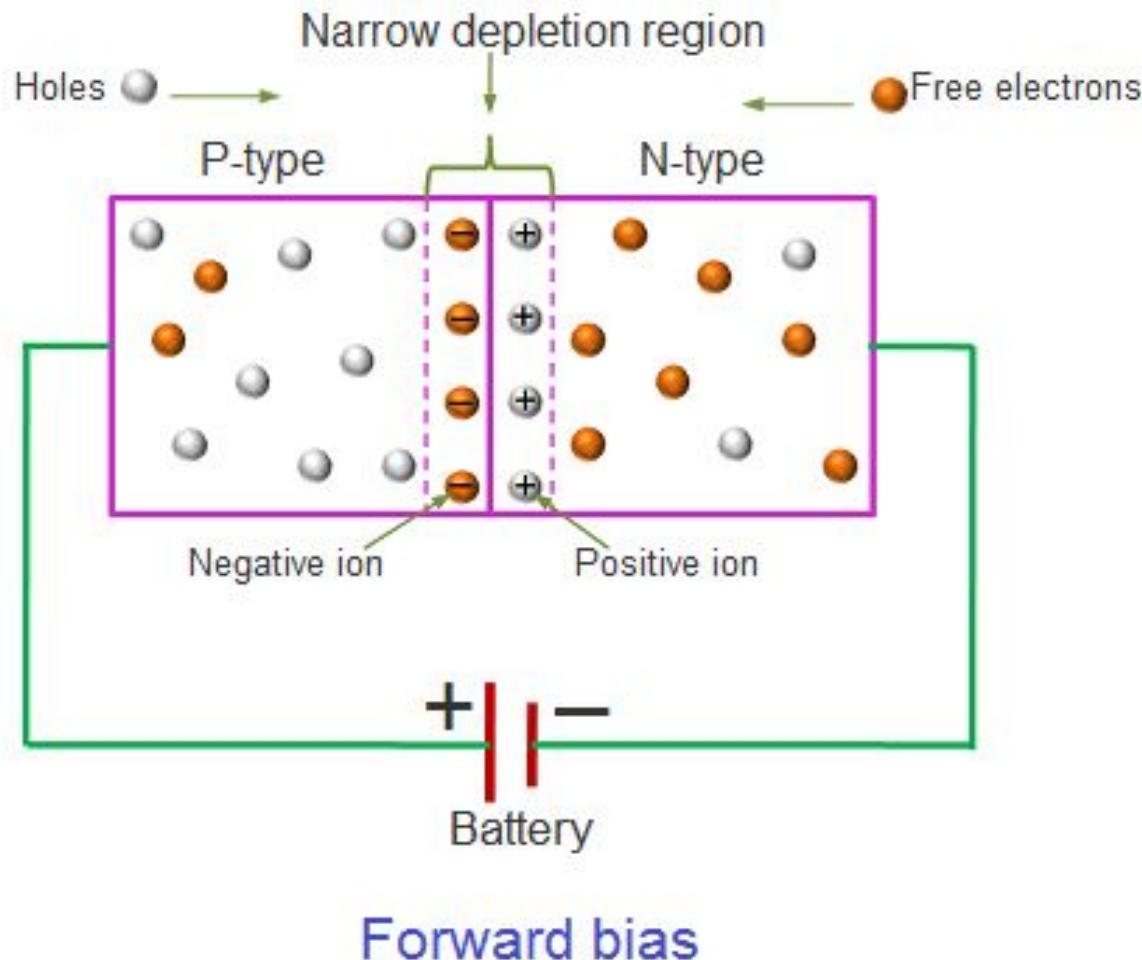
What is Depletion Region ??

BIASING OF P-N JUNCTION DIODE

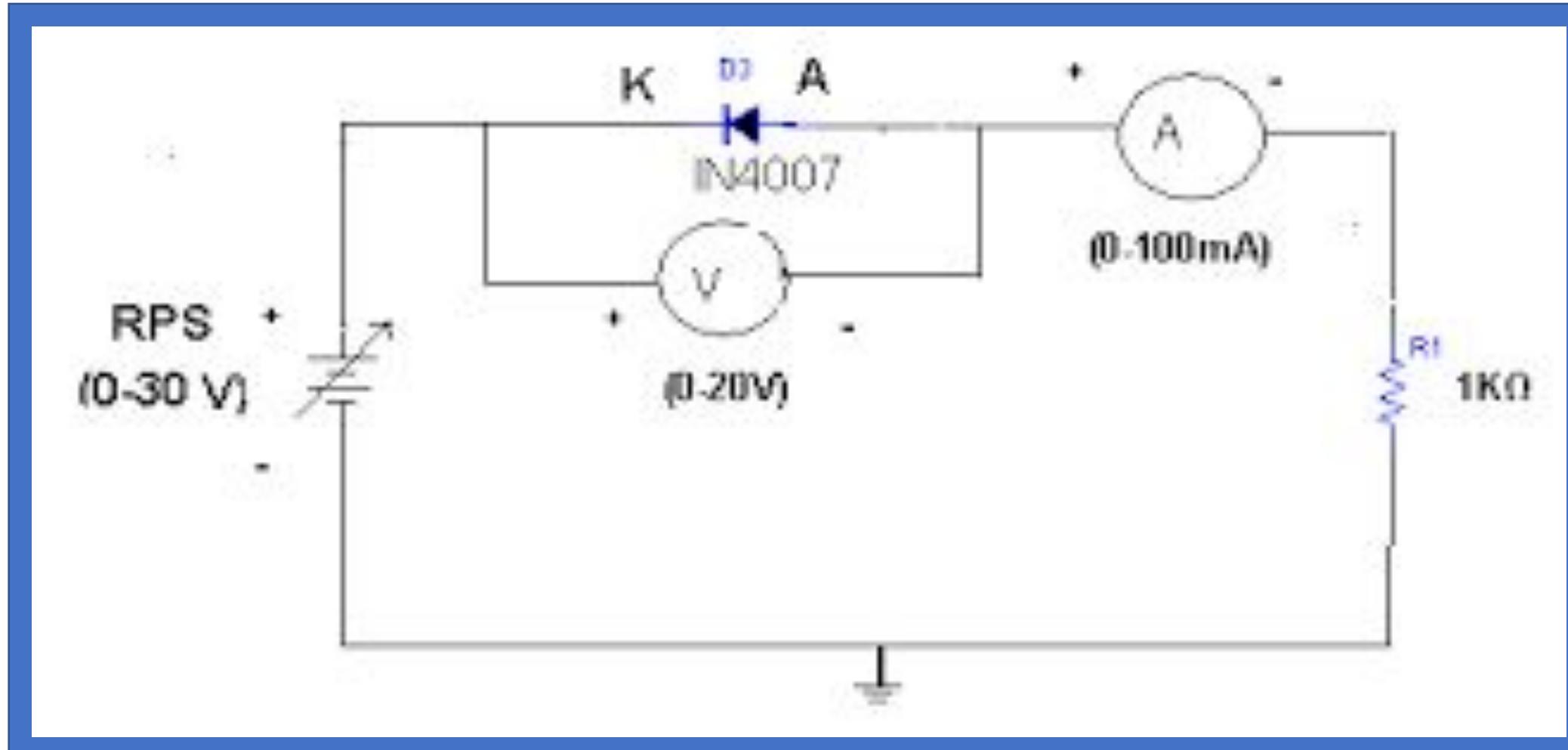
- The process of applying the external voltage to a p-n junction semiconductor diode is called biasing.
- External voltage to the p-n junction diode is applied in any of the two methods: forward biasing or reverse biasing.



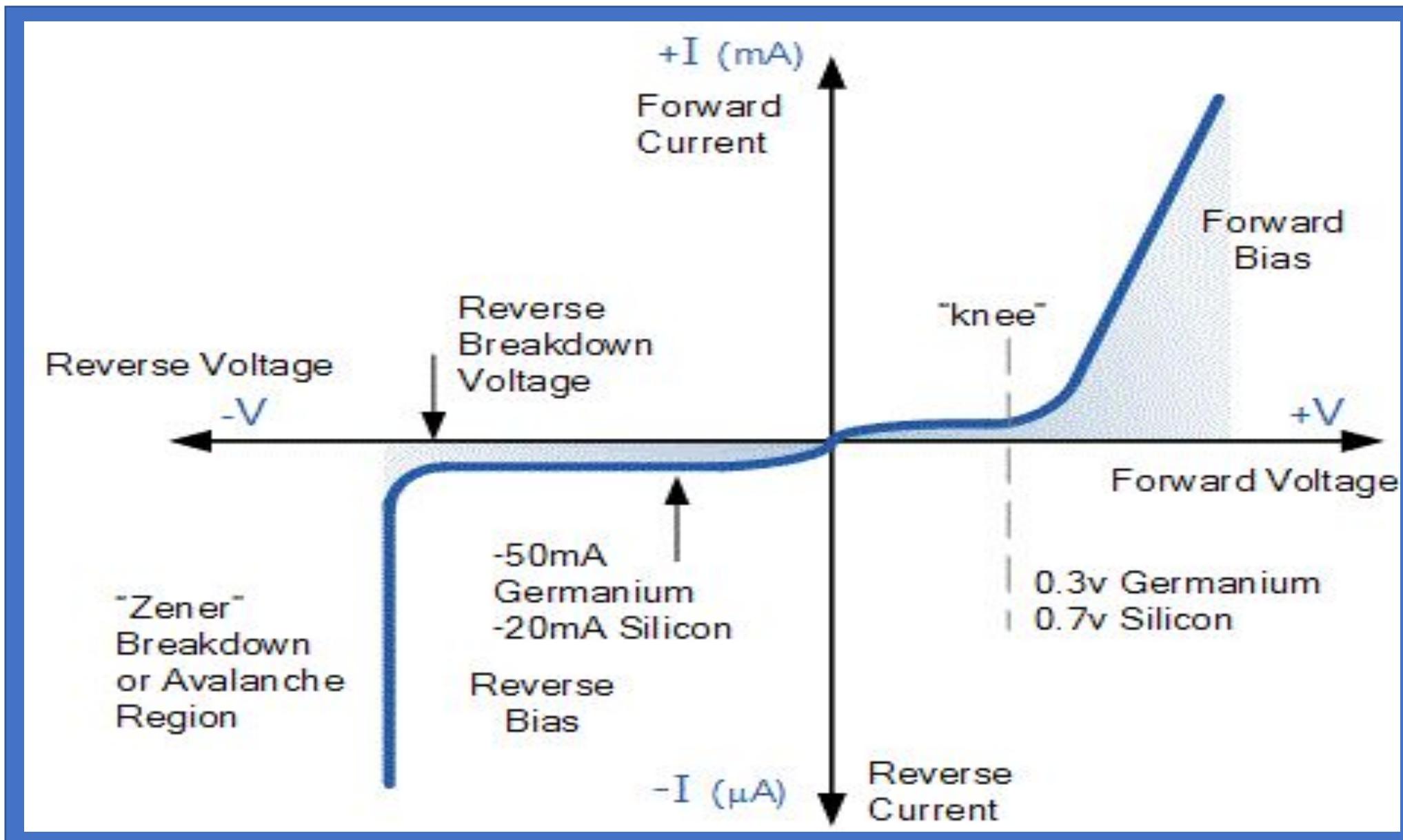
FORWARD BIAS AND REVERSE BIAS



CIRCUIT ARRANGEMENT TO PLOT VI CHARACTERISTICS OF DIODE



VI CHARACTERISTICS OF PN JUNCTION DIODE



DIODE CURRENT EQUATION

$$I_D = I_S(e^{qV_D / NkT} - 1)$$

Where,

I_D = Diode current in amps

I_S = Saturation current in amps
(typically 1×10^{-12} amps)

e = Euler's constant (~ 2.718281828)

q = charge of election (1.6×10^{-19} coulombs)

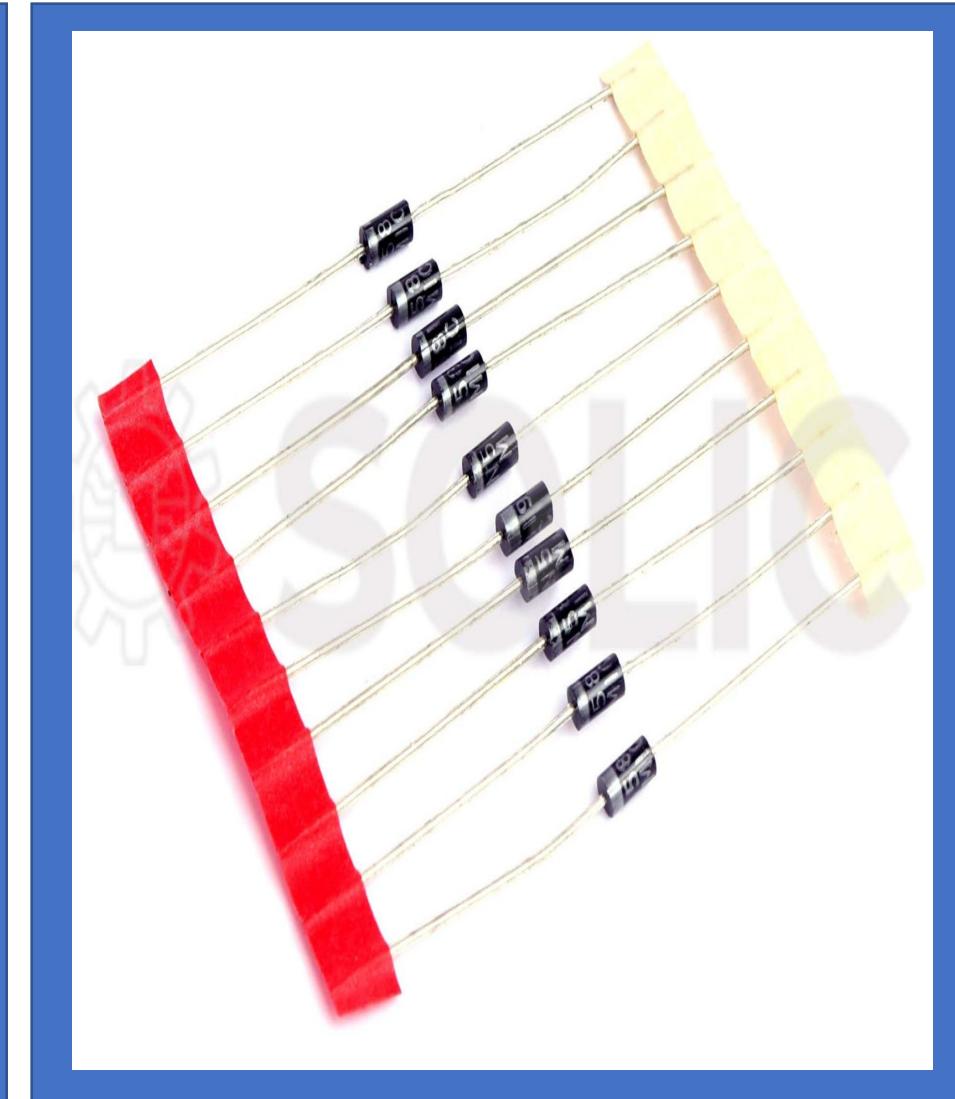
V_D = Voltage applied across diode in volts

N = "Nonideality" or "Emission" coefficient
(typically between 1 and 2)

k = Boltzmann's constant (1.38×10^{-23})

T = Junction Temperature in Kelvins

HOW TO TEST THE DIODE?



TYPES OF DIODES

Gunn Diode



PIN Diode



Step Recovery Diode



Laser Diode



Photo Diode



Tunnel Diode

Schottky Diode

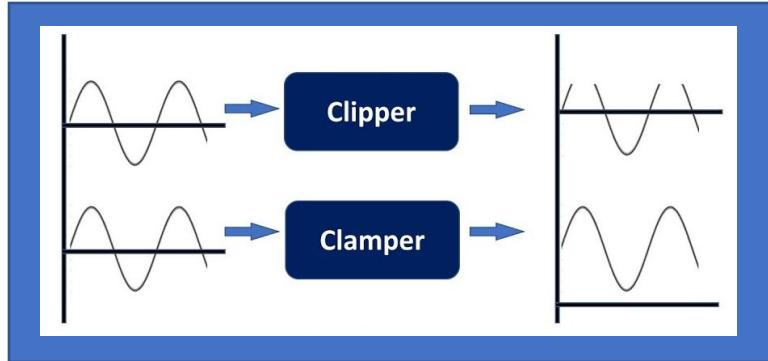


Varactor Diode

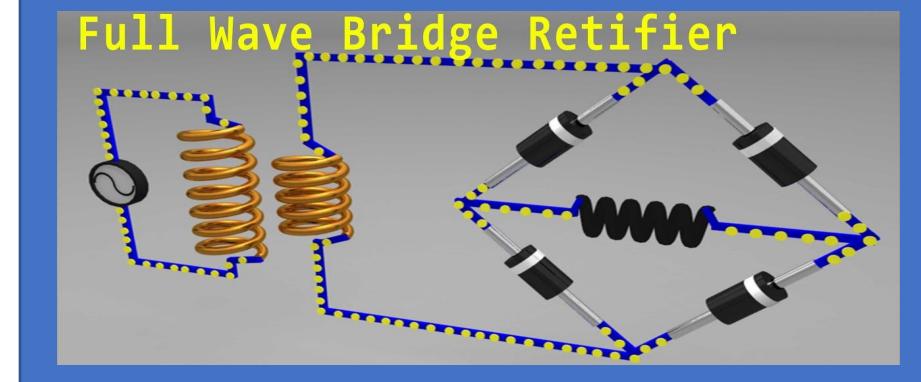
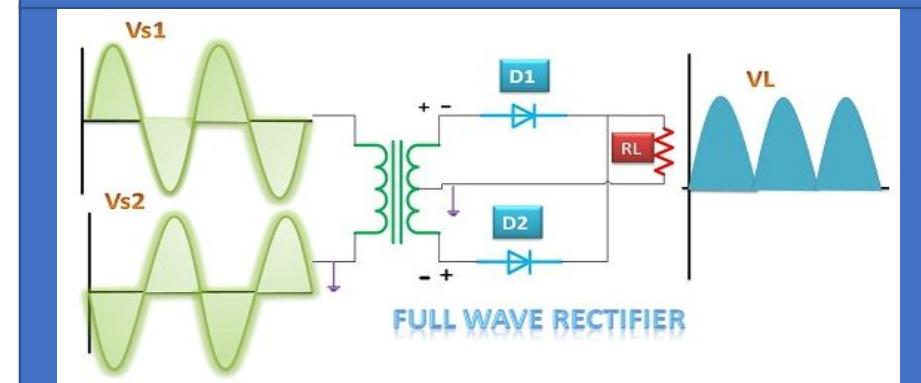
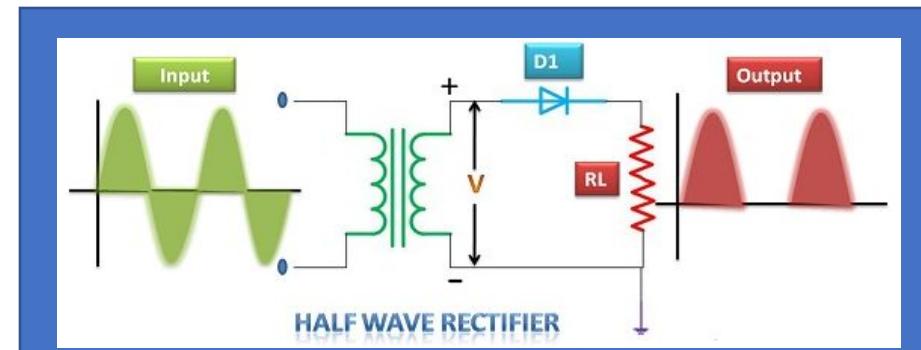


Zener Diode

APPLICATIONS OF DIODE



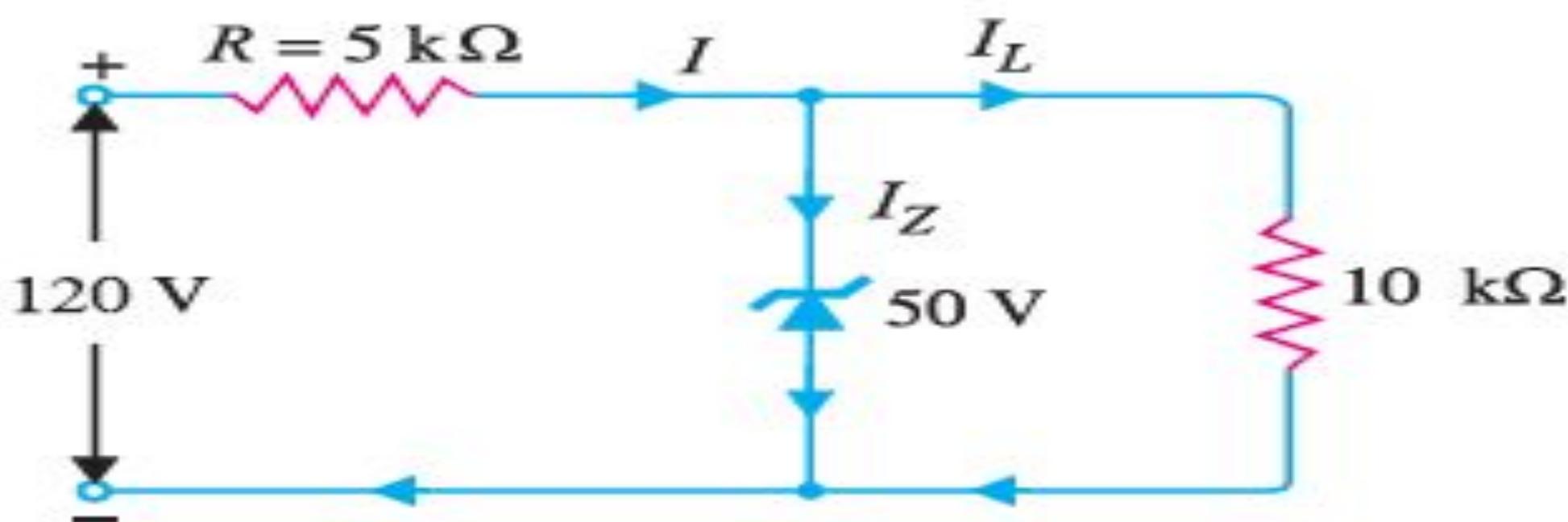
- **Clipper Clampers**-clips or clamps the waveform
- **Rectifiers:**
 - Converts AC voltage into DC voltage
 - A HWR allows current to flow during half the AC cycle.
 - A FWR allows current to flow during both half AC cycles.
- **Transistors:**
 - Used to amplify small signals



NUMERICAL ON ZENER DIODE

Ex. 1) For the circuit shown in given Figure

- find : (i) the output voltage
(ii) the voltage drop across series resistance
(iii) the current through zener diode.



SOLUTION OF EX 1

If you remove the zener diode in Fig. 1, the voltage V across the open-circuit is

$$V = \frac{R_L E_i}{R + R_L} = \frac{10 \times 120}{5 + 10} = 80 \text{ V}$$

Since voltage across zener diode is greater than V_Z ($= 50 \text{ V}$), the zener is in the “on” state. It can, therefore, be represented by a battery of 50 V

$$\text{Output voltage} = V_Z = 50 \text{ V}$$

$$\text{Voltage drop across } R = \text{Input voltage} - V_Z = 120 - 50 = 70 \text{ V}$$

$$\text{Load current, } I_L = V_Z/R_L = 50 \text{ V}/10 \text{ k}\Omega = 5 \text{ mA}$$

$$\text{Applying Kirchhoff's first law, } I = I_L + I_Z$$

$$\text{Current through } R, I = \frac{70 \text{ V}}{5 \text{ k}\Omega} = 14 \text{ mA}$$

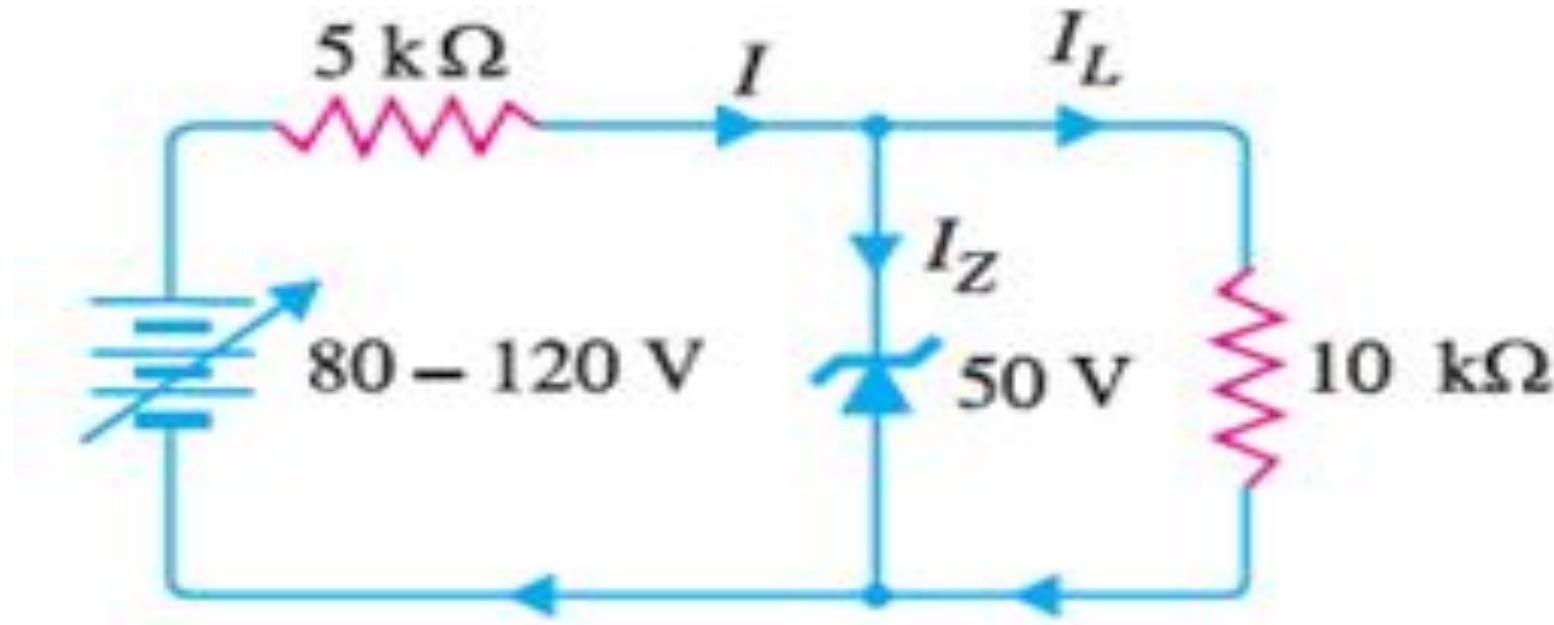
∴

$$\text{Zener current, } I_Z = I - I_L = 14 - 5 = 9 \text{ mA}$$

NUMERICAL ON ZENER DIODE

Ex.2) For the circuit given

(i),find the maximum and minimum values of zener diode current.



SOLUTION OF EX 2

Maximum zener current: The zener will conduct maximum current when the input voltage is maximum i.e. 120 V. Under such conditions :

$$\text{Voltage across } 5 \text{ k}\Omega = 120 - 50 = 70 \text{ V}$$

$$\text{Current through } 5 \text{ k}\Omega, I = \frac{70 \text{ V}}{5 \text{ k}\Omega} = 14 \text{ mA}$$

$$\text{Load current, } I_L = \frac{50 \text{ V}}{10 \text{ k}\Omega} = 5 \text{ mA}$$

Applying Kirchhoff's first law, $I = I_L + I_Z$

$$\therefore \text{Zener current, } I_Z = I - I_L = 14 - 5 = 9 \text{ mA}$$

SOLUTION OF EX 2

Minimum Zener current: The zener will conduct minimum current when the input voltage is minimum i.e. 80 V. Under such conditions, we have,

$$\text{Voltage across } 5 \text{ k}\Omega = 80 - 50 = 30 \text{ V}$$

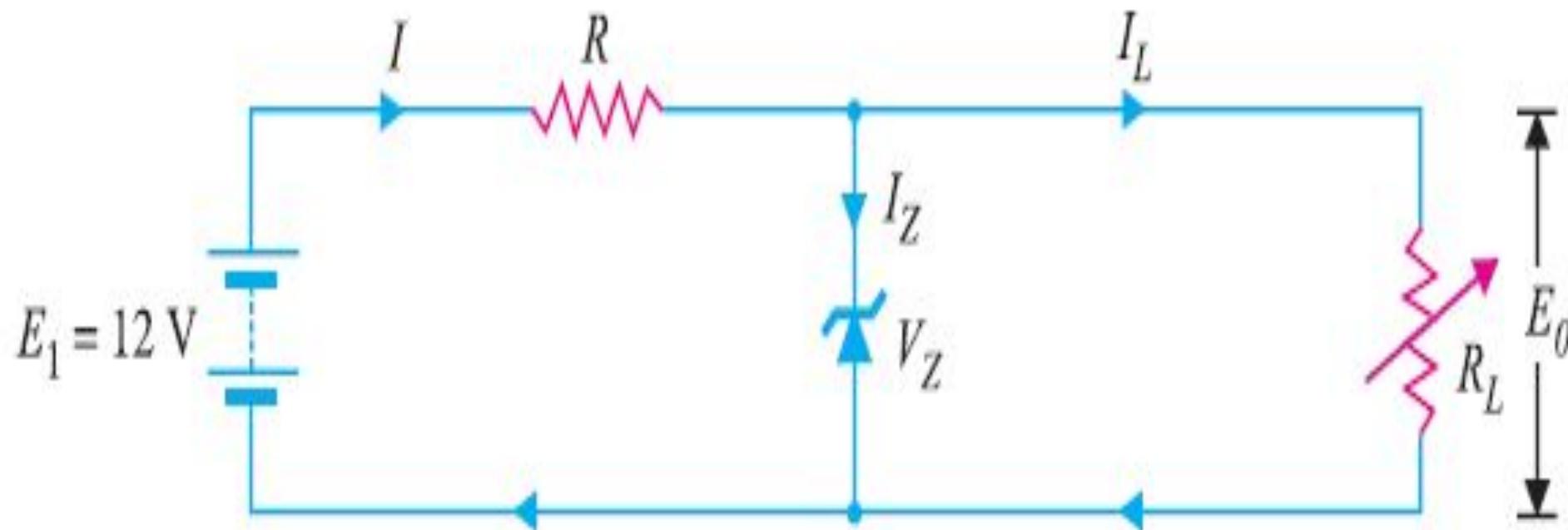
$$\text{Current through } 5 \text{ k}\Omega, I = \frac{30 \text{ V}}{5 \text{ k}\Omega} = 6 \text{ mA}$$

$$\text{Load current, } I_L = 5 \text{ mA}$$

$$\therefore \text{Zener current, } I_Z = I - I_L = 6 - 5 = 1 \text{ mA}$$

NUMERICAL ON ZENER DIODE

Ex. 3) A 7.2 V zener is used in the circuit shown in Fig. 3 and the load current is to vary from 12 to 100 mA. Find the value of series resistance R to maintain a voltage of 7.2 V across the load. The input voltage is constant at 12V and the minimum zener current is 10 mA.



SOLUTION OF EX 3

$$E_i = 12 \text{ V}; \quad V_Z = 7.2 \text{ V}$$

$$R = \frac{E_i - E_0}{I_Z + I_L}$$

The voltage across R is to remain constant at $12 - 7.2 = 4.8 \text{ V}$ as the load current changes from 12 to 100 mA. The minimum zener current will occur when the load current is maximum.

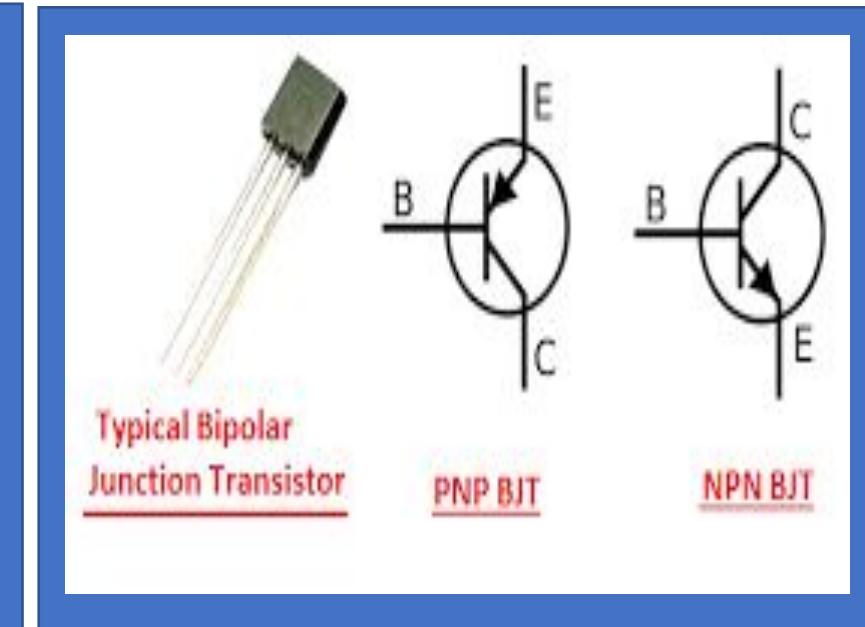
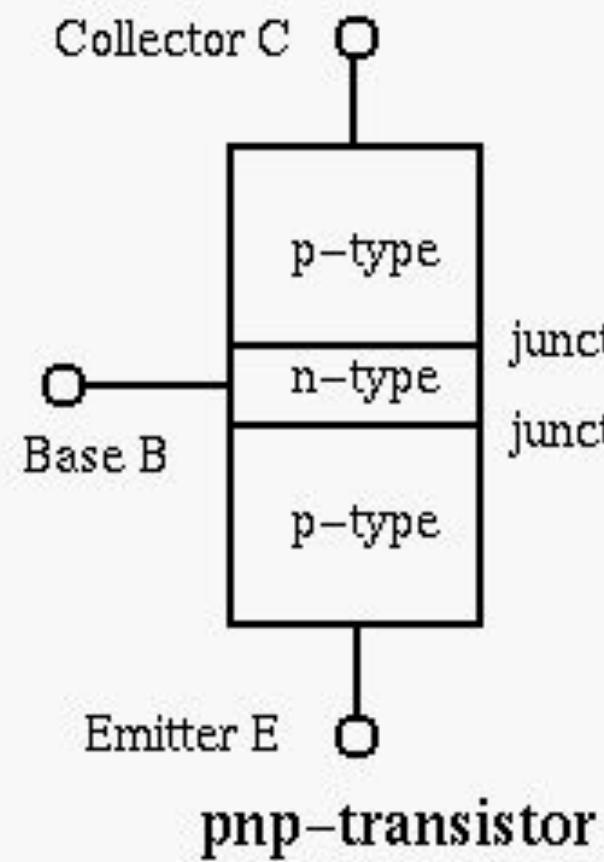
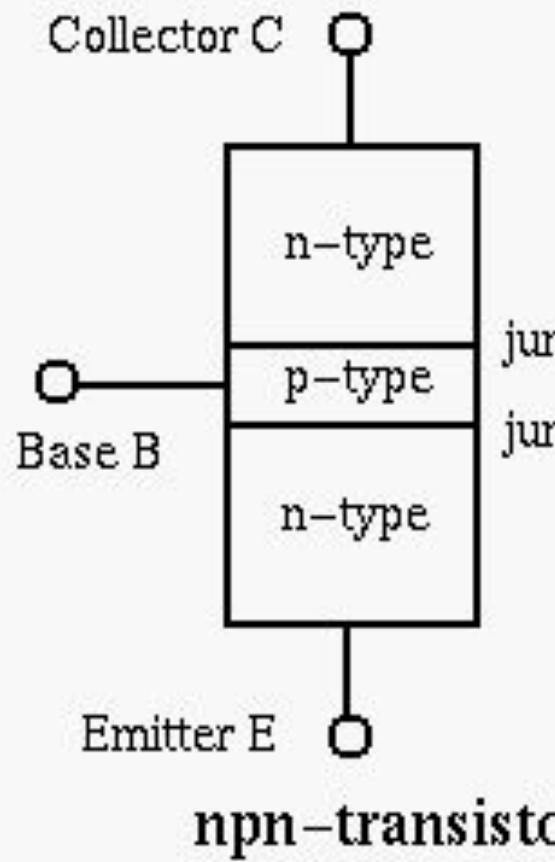
$$R = \frac{E_i - E_0}{(I_Z)_{\min} + (I_L)_{\max}} = \frac{12 \text{ V} - 7.2 \text{ V}}{(10 + 100) \text{ mA}} = \frac{4.8 \text{ V}}{110 \text{ mA}} = 43.5 \Omega$$

If $R = 43.5 \Omega$ is inserted in the circuit, the output voltage will remain constant over the regulating range. As the load current I_L decreases, the zener current I_Z will increase to such a value that $I_Z + I_L = 110 \text{ mA}$.

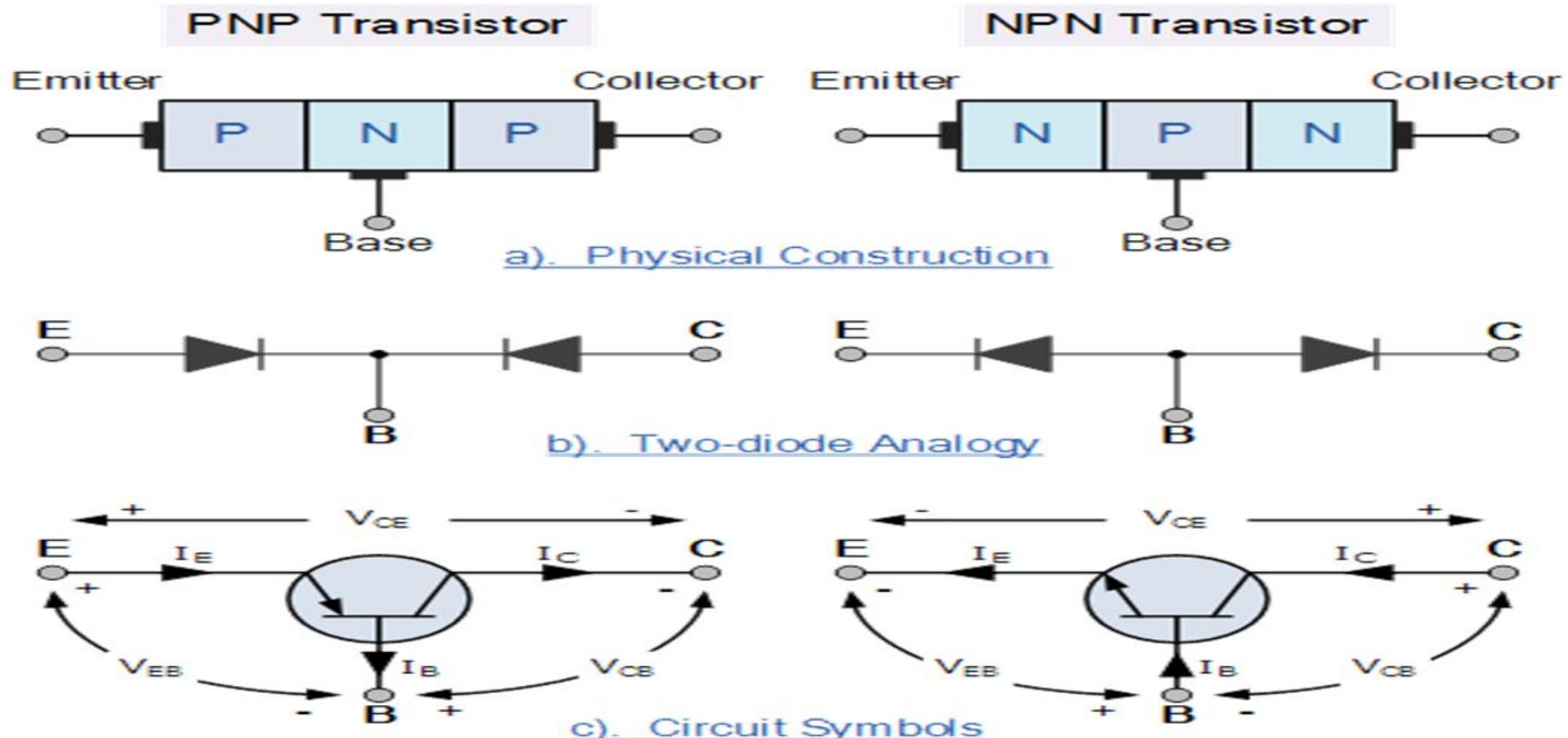
Note that if load resistance is open-circuited, then $I_L = 0$ and zener current becomes 110 mA.

BIPOLAR JUNCTION TRANSISTOR (BJT)

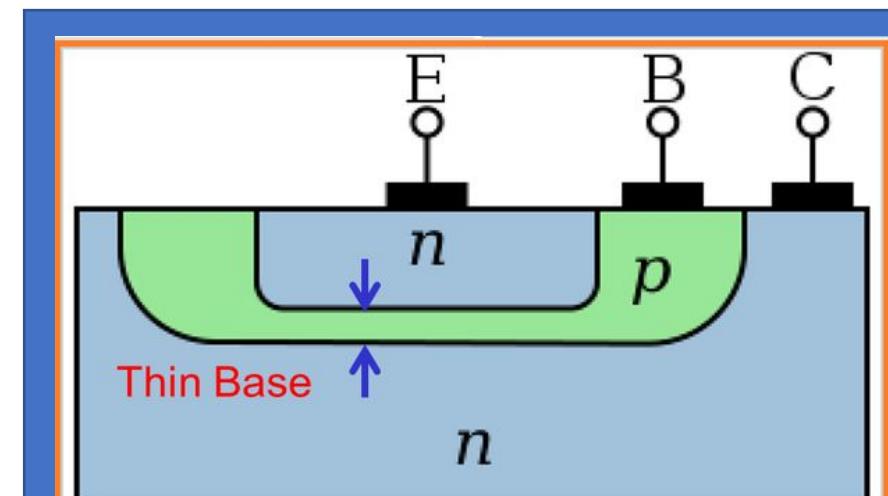
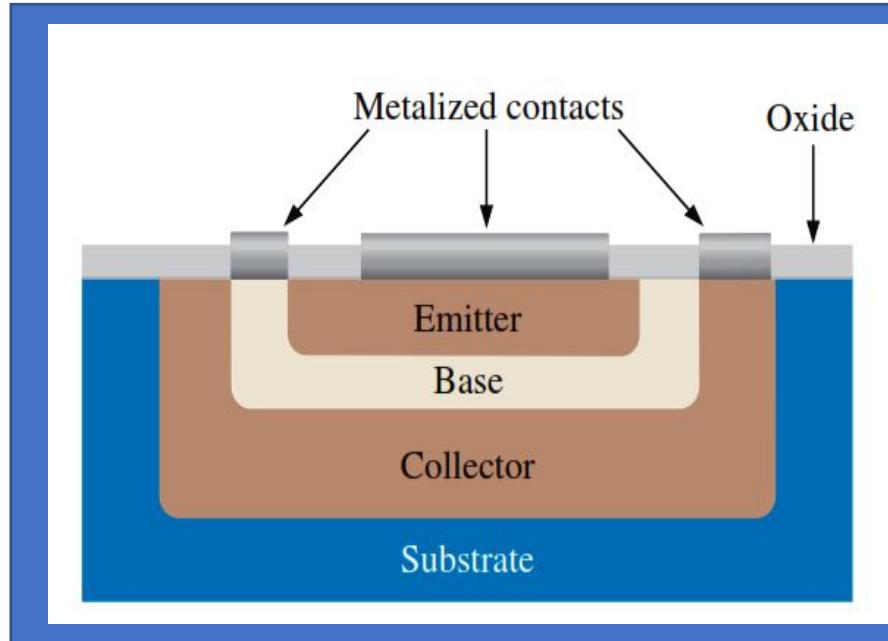
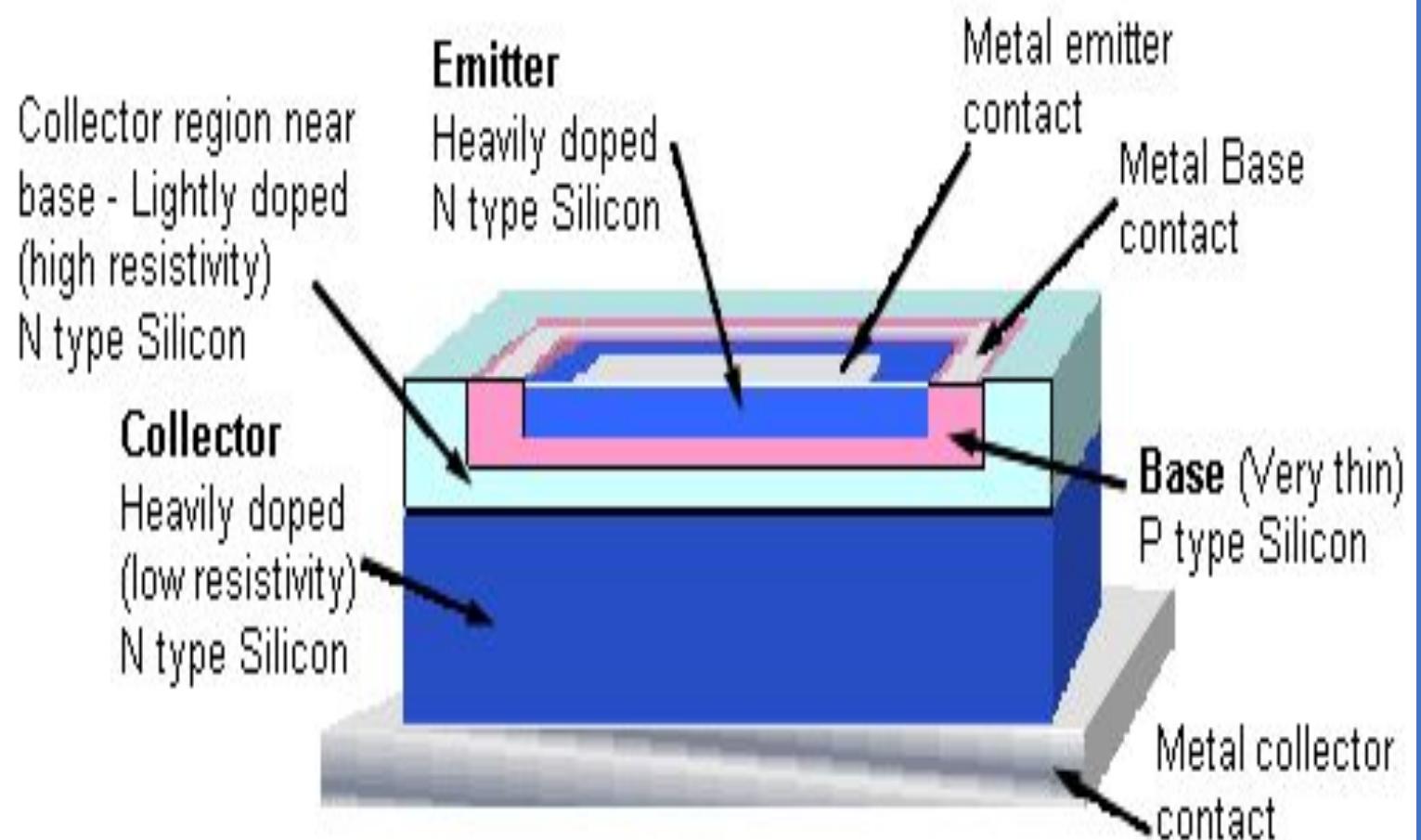
BJT is a semiconductor device which can be used for switching or amplification



TWO DIODE ANALOGY OF TRANSISTORS

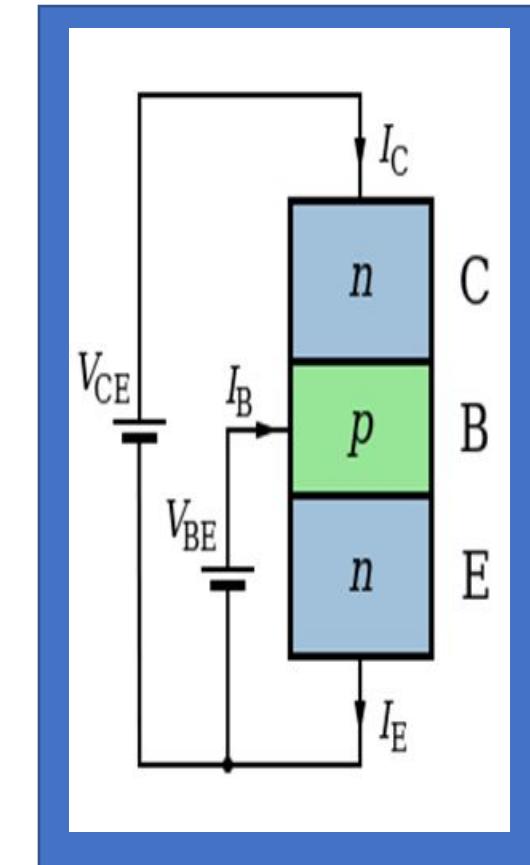
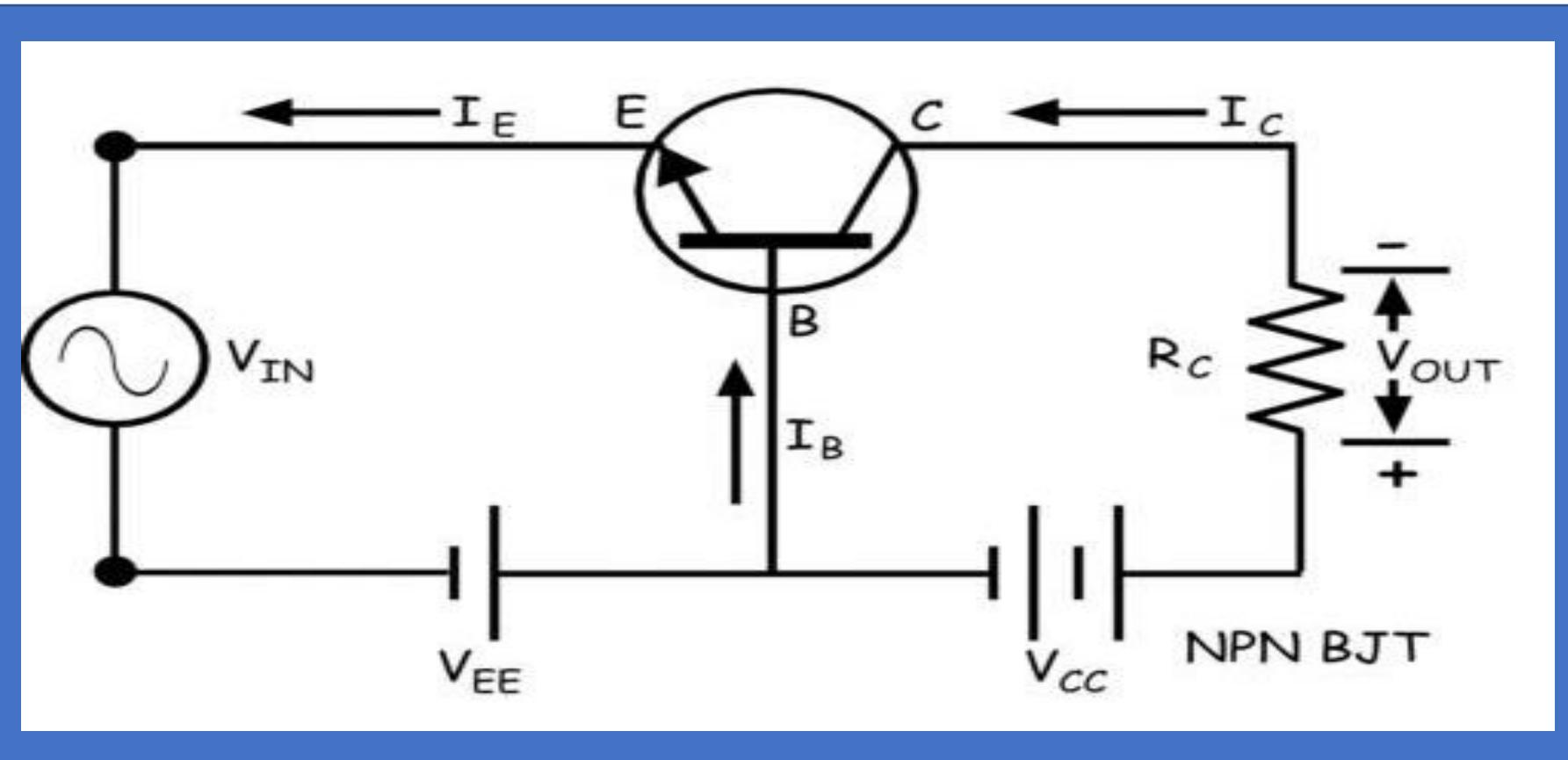


CONSTRUCTION OF BJT



Simplified cross section of a planar *NPN* bipolar junction transistor

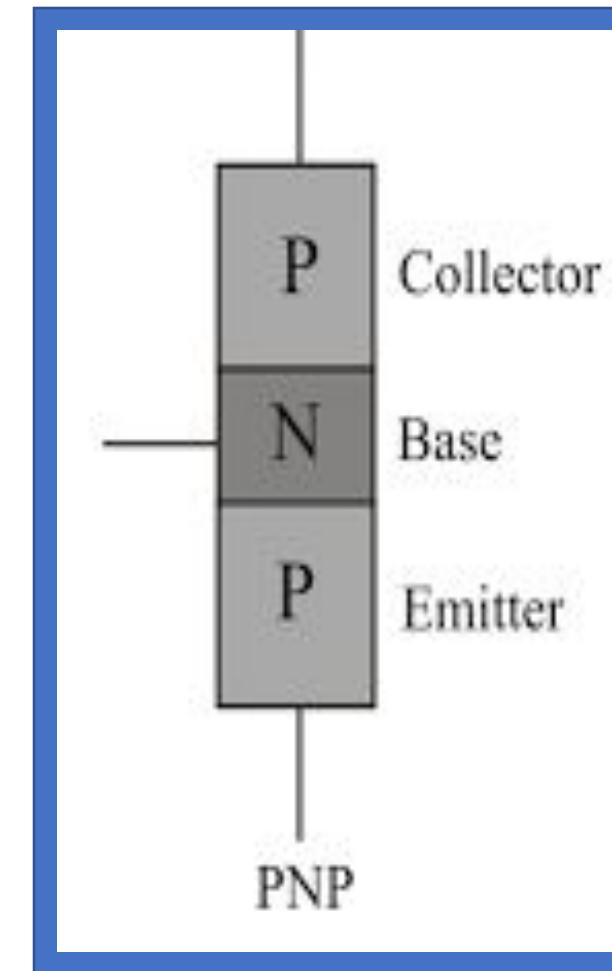
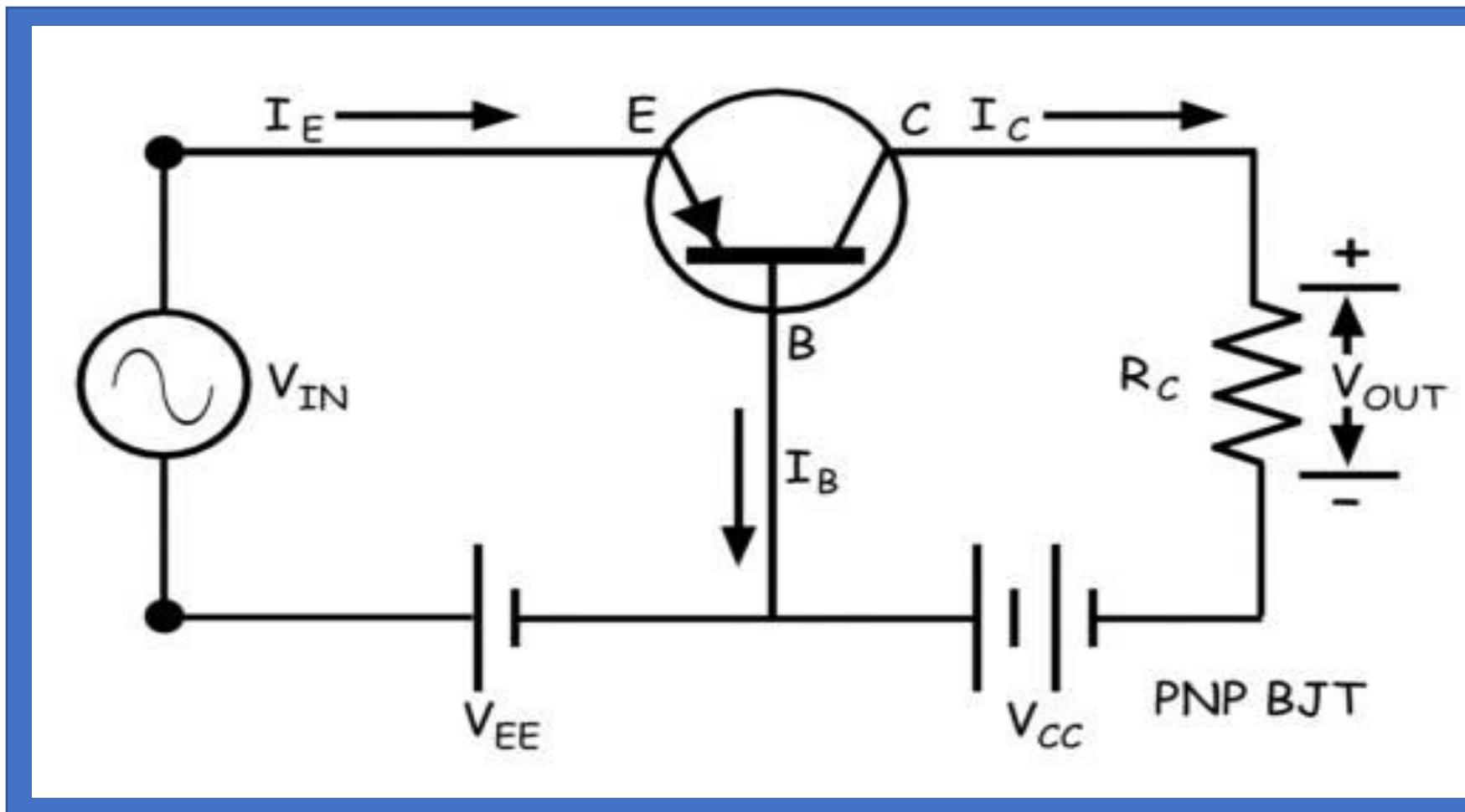
WORKING OF NPN TRANSISTOR



NPN Transistor : EB junction-Forward Biased

CB junction-Reverse Biased

WORKING OF PNP TRANSISTOR



PNP Transistor : EB junction-Reverse Biased

CB junction- Forward Biased

Operating regions of BJT

Cut off region

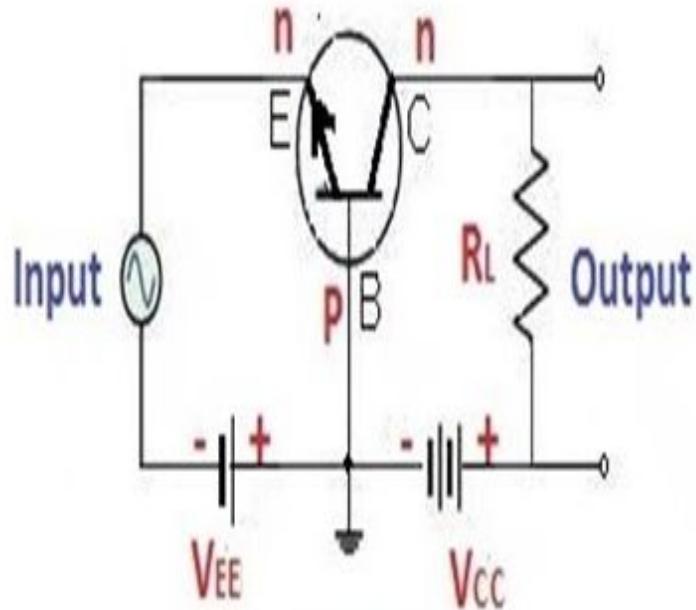
Linear region

Saturation region

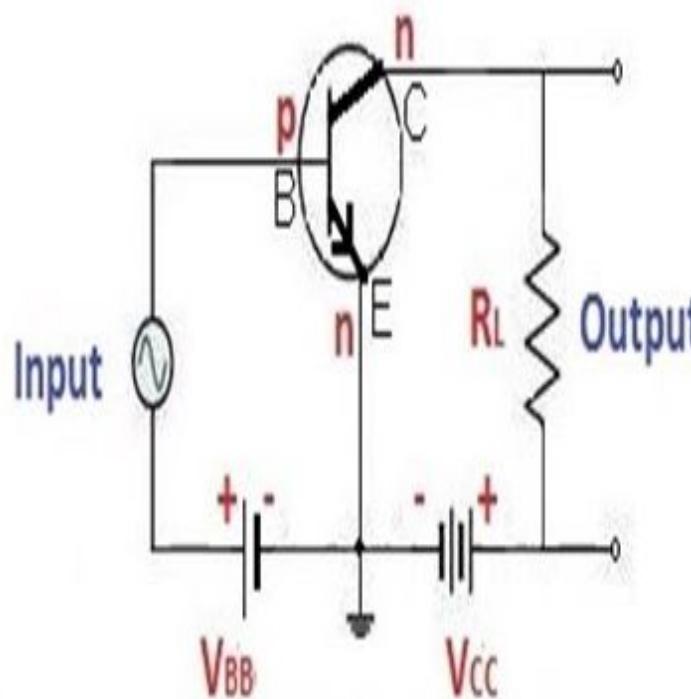


- ✓ Active Region – the transistor operates as an amplifier and $I_c = \beta * I_b$
- ✓ Saturation – the transistor is “Fully-ON” operating as a switch and $I_c = I_{\text{saturation}}$
- ✓ Cut-off – the transistor is “Fully-OFF” operating as a switch and $I_c = 0$

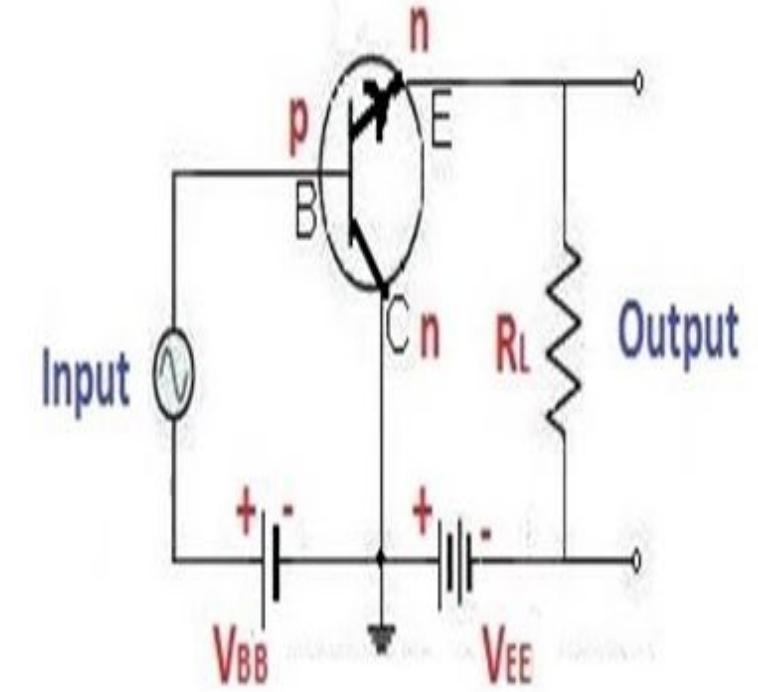
CONFIGURATIONS OF BJT



COMMON - BASE

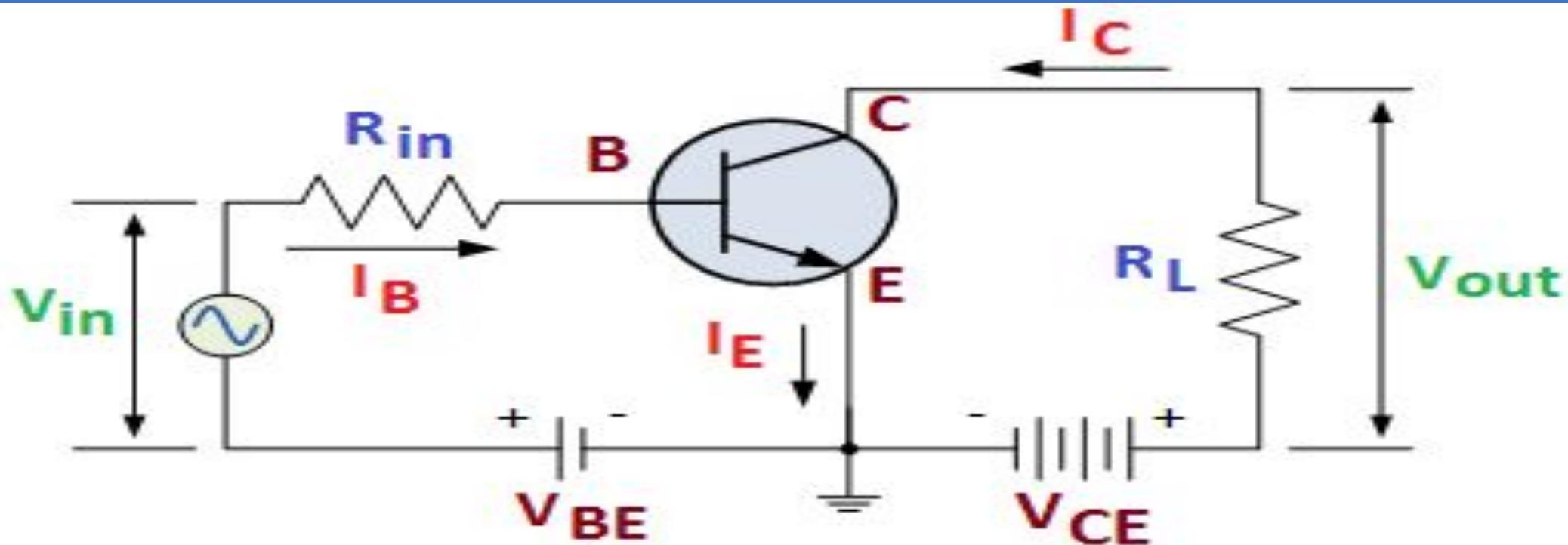


COMMON - Emitter



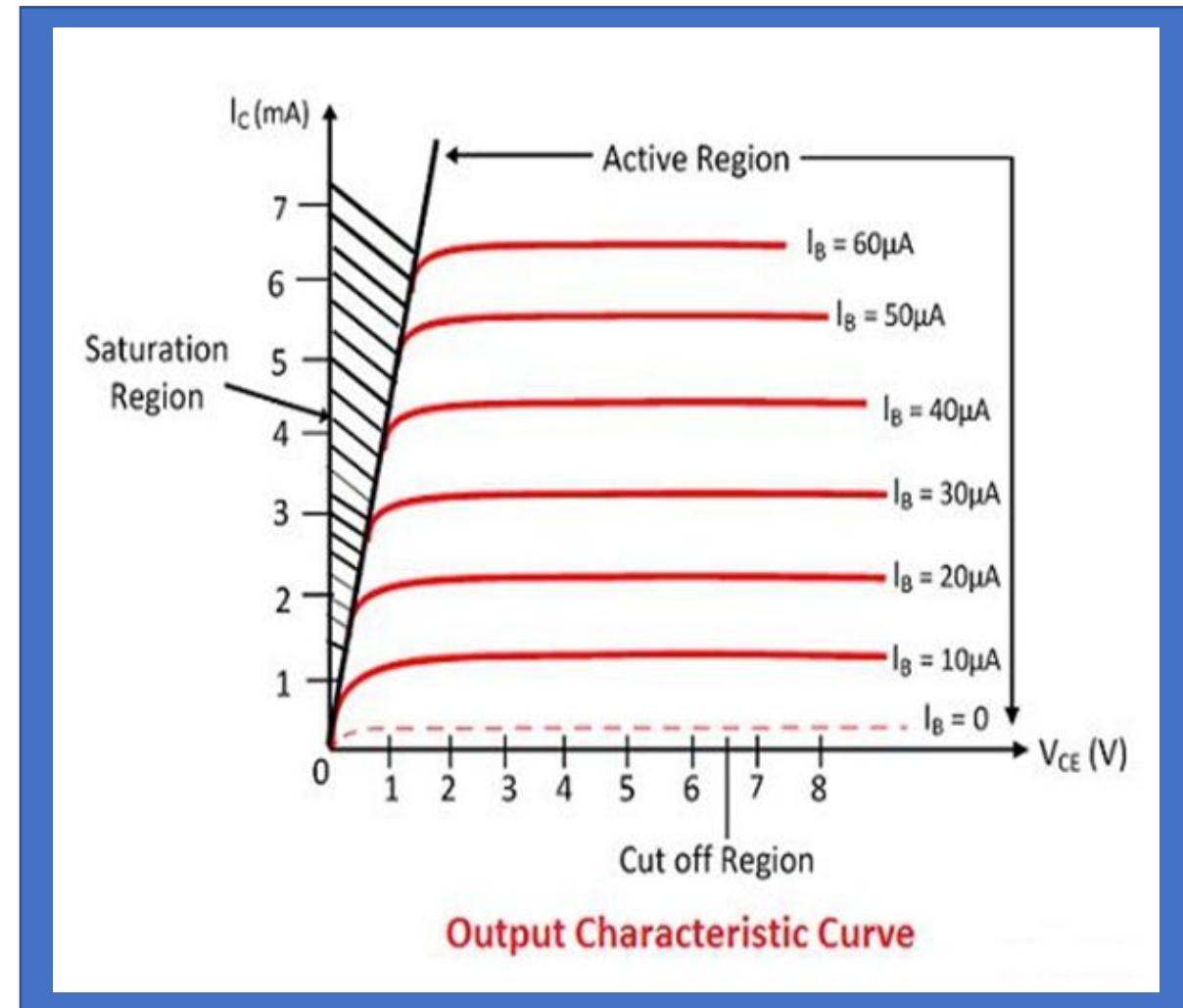
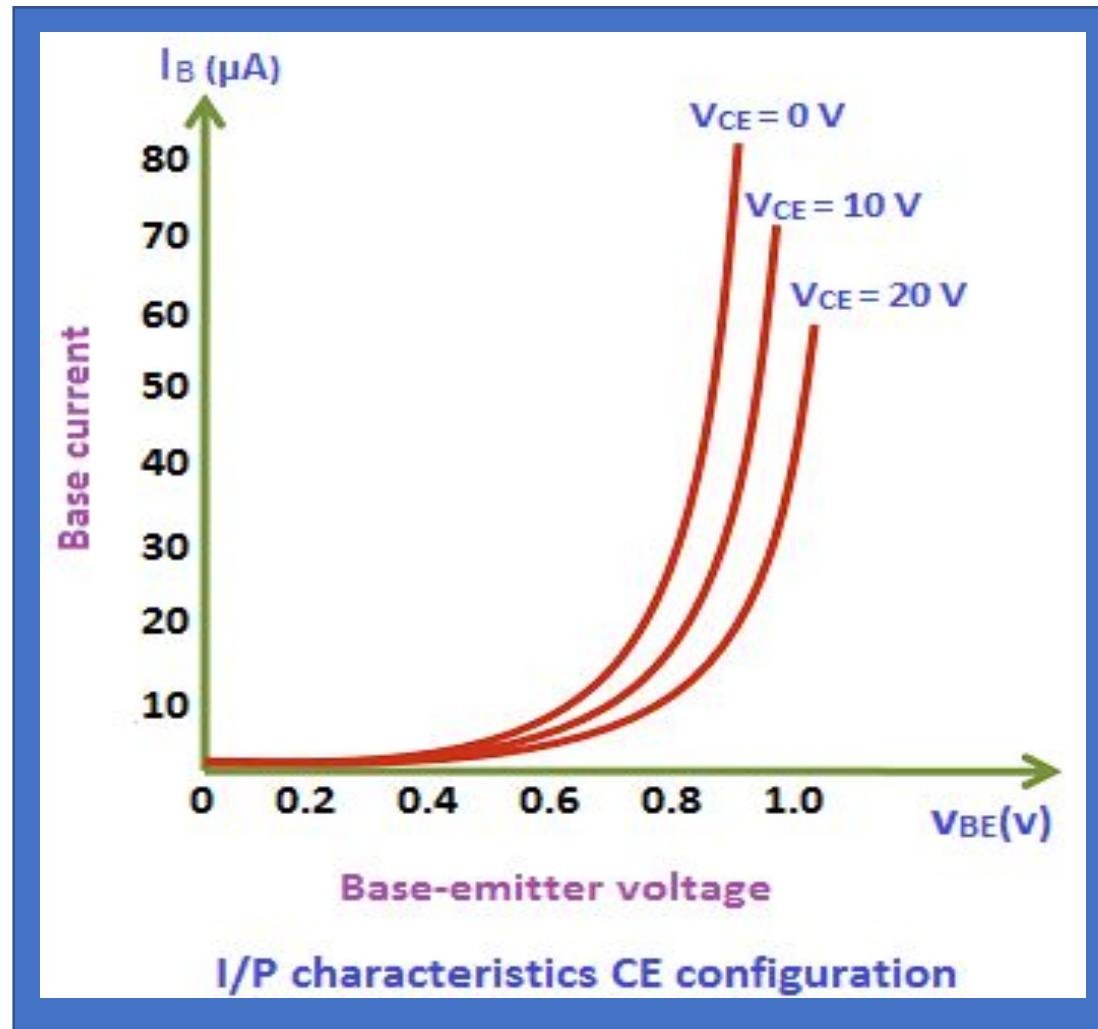
COMMON - COLLECTOR

COMMON Emitter CONFIGURATION



Common Emitter Configuration

INPUT OUTPUT CHARACTERISTICS OF CE AMPLIFIER



NUMERICAL ON DIODE CURRENT EQUATION

Q.1) Calculate the forward bias current of a Si diode when forward bias voltage of 0.4V is applied, the reverse saturation current is 1.17×10^{-9} A and the thermal voltage is 25.2mV.

SOLUTION OF Q.1)

- Equation for diode current $I = I_0 \times (e^{(V/\eta V_T)} - 1)$
- where I_0 = reverse saturation current
 η = ideality factor
 V_T = thermal voltage
 V = applied voltage
- Since in this question ideality factor is not mentioned it can be taken as one.
- $I_0 = 1.17 \times 10^{-9} A$, $V_T = 0.0252 V$, $\eta = 1$, $V = 0.4 V$
- Therefore, $I = 1.17 \times 10^{-9} \times e^{0.4/0.025} - 1 = 9.156 mA$.

NUMERICAL ON DIODE CURRENT EQUATION

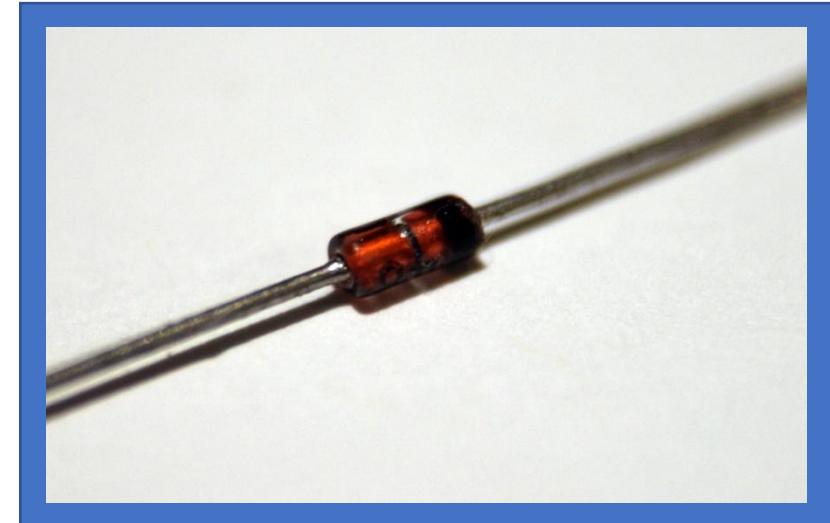
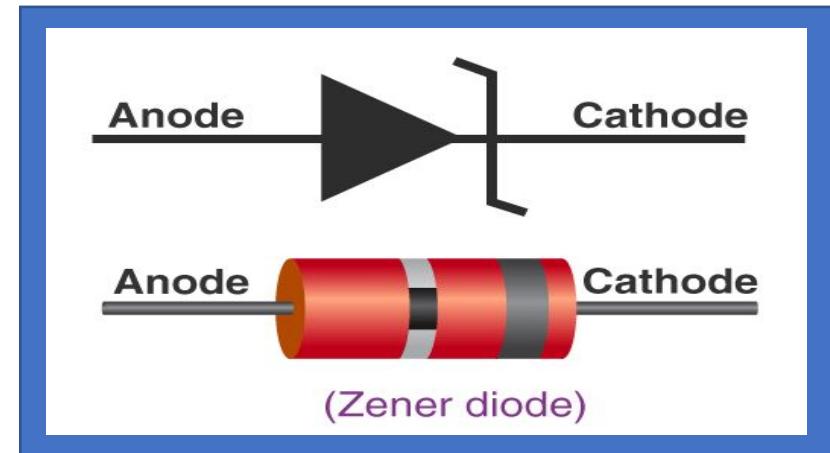
Q.2) Calculate the reverse saturation current of a diode if the current at 0.2V forward bias is 0.1mA at a temperature of 25°C and the ideality factor is 1.5.

SOLUTION OF Q.2)

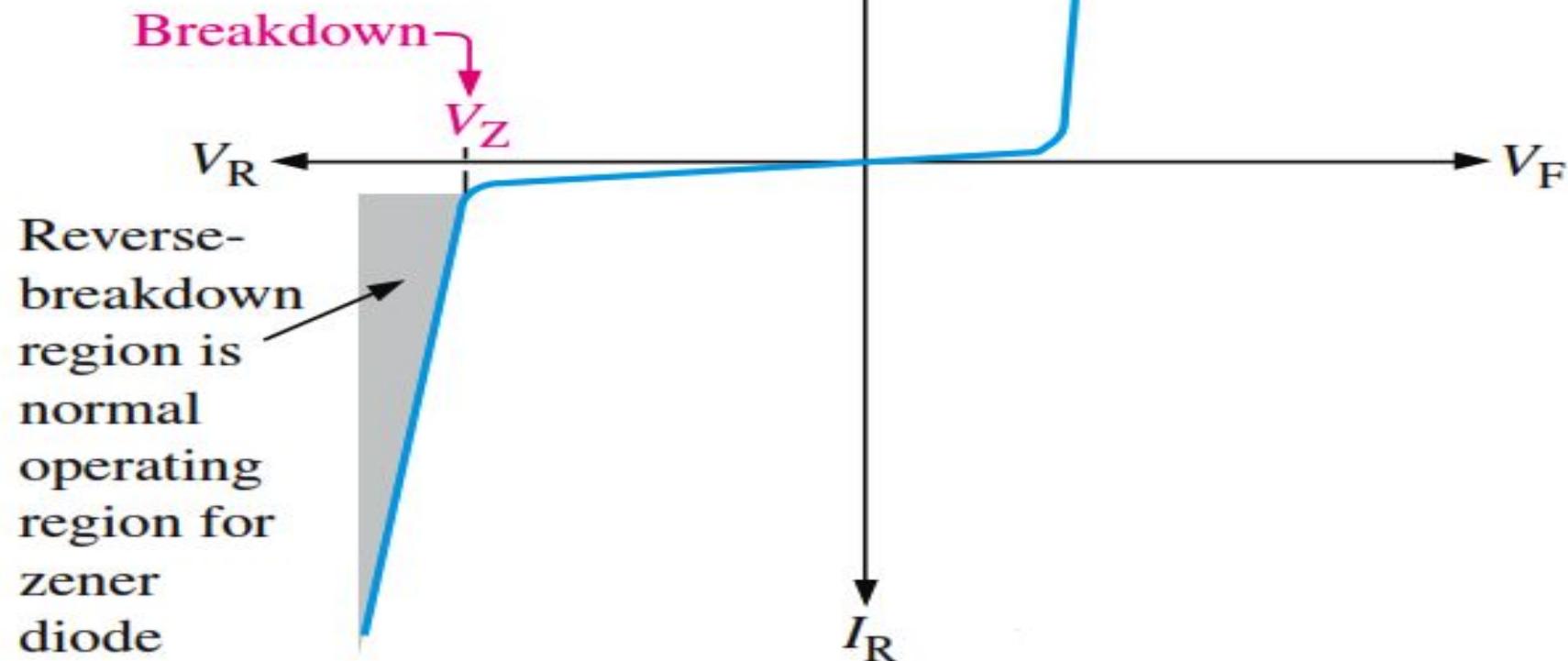
- Explanation:
- Equation for diode current $I = I_0 \times (e^{(V/\eta V_T)} - 1)$
- where I_0 = reverse saturation current
 η = ide^e or
 V_T = thermal ge
 V = applied voltage
- Here, $I = 0.1\text{mA}$, $\eta = 1.5$, $V = 0.2\text{V}$, $V_T = T_K/11600$
Therefore, V_T at $T = 25 + 273 = 298$ is $298/11600 = 0.0256\text{V}$.
Therefore, $I_0 = 0.00055\text{mA} = 5.5 \times 10^{-7}\text{A}$.

ZENER DIODE

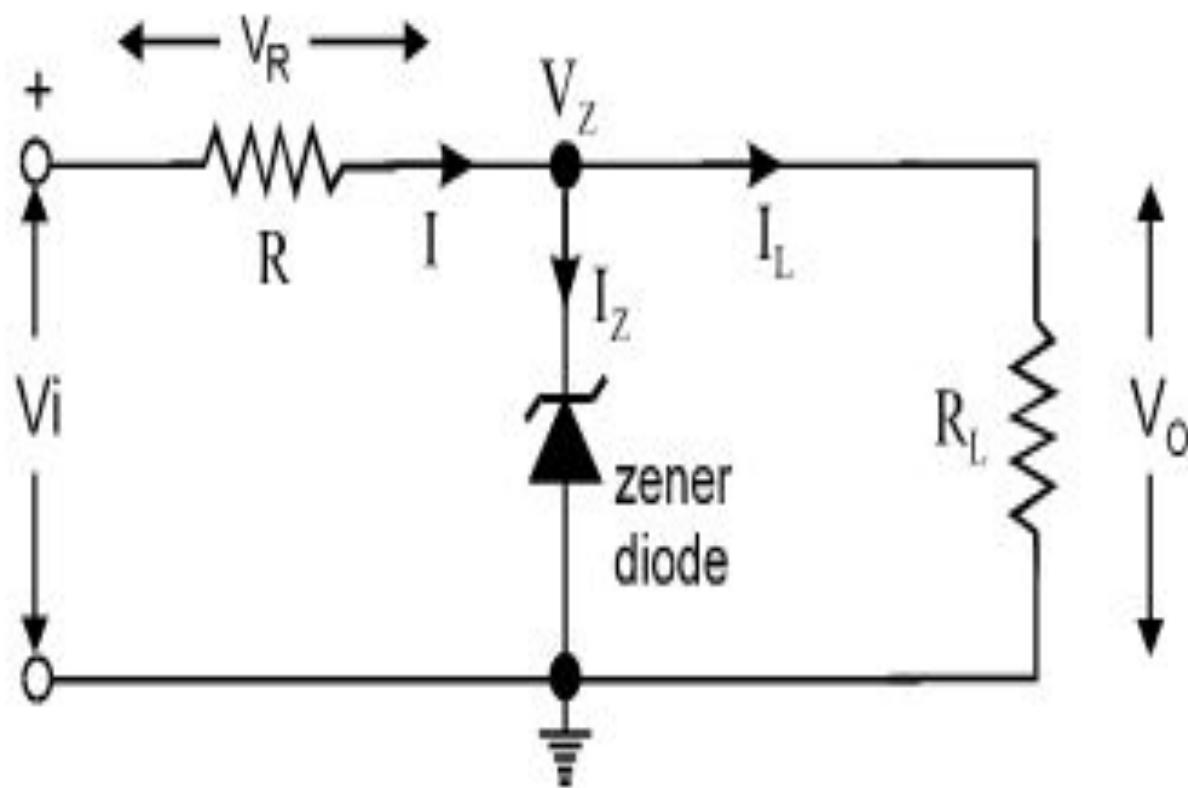
- A special type of device designed to operate in the reverse breakdown region.
- is always connected in reverse direction because it is specifically designed to work in reverse direction.
- mainly used to protect electronic circuits from over voltage.



VI CHARACTERISTICS OF ZENER DIODE



ZENER DIODE AS A VOLTAGE REGULATOR



- Zener maintains constant voltage and current to load connected parallel with it.
- Input unregulated voltage is dropped by series resistance R
- Increased current is conducted by Zener diode

Voltage Regulation



Load regulation is a measure of the ability of regulator to maintain constant dc V_{out} despite changes in load current due to a varying load resistance.

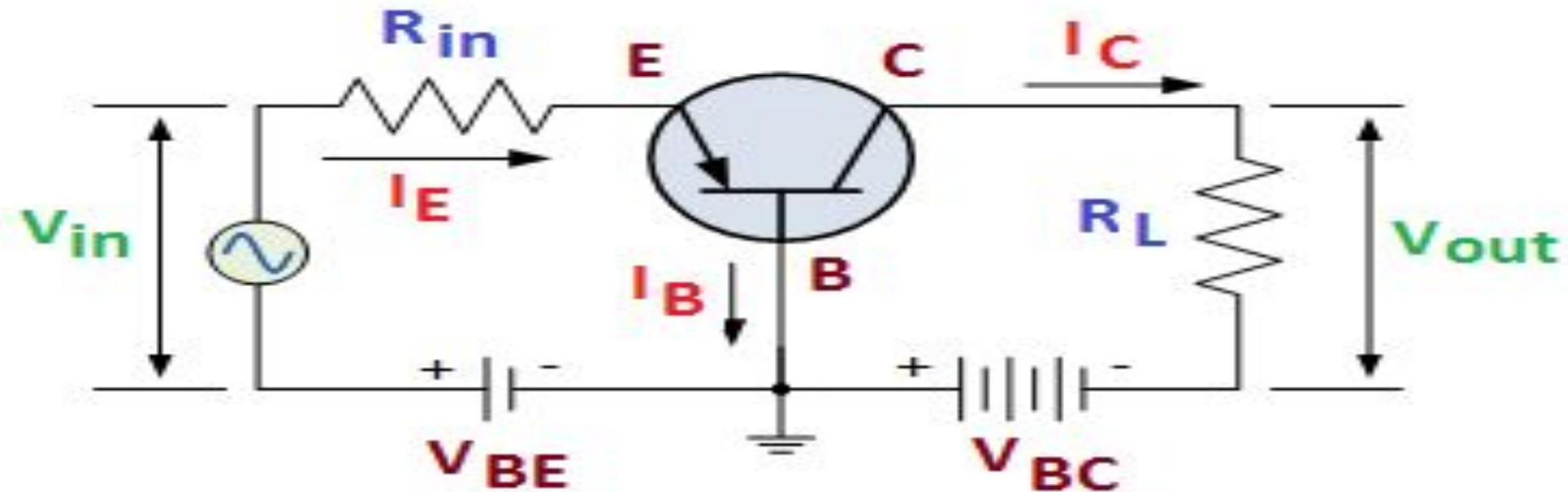
Ideally the load regulation is 0 %, and the formula is:

Load Regulation =

$$\left(\frac{V_{NL} - V_{FL}}{V_{FL}} \right) 100 \text{ \%}$$

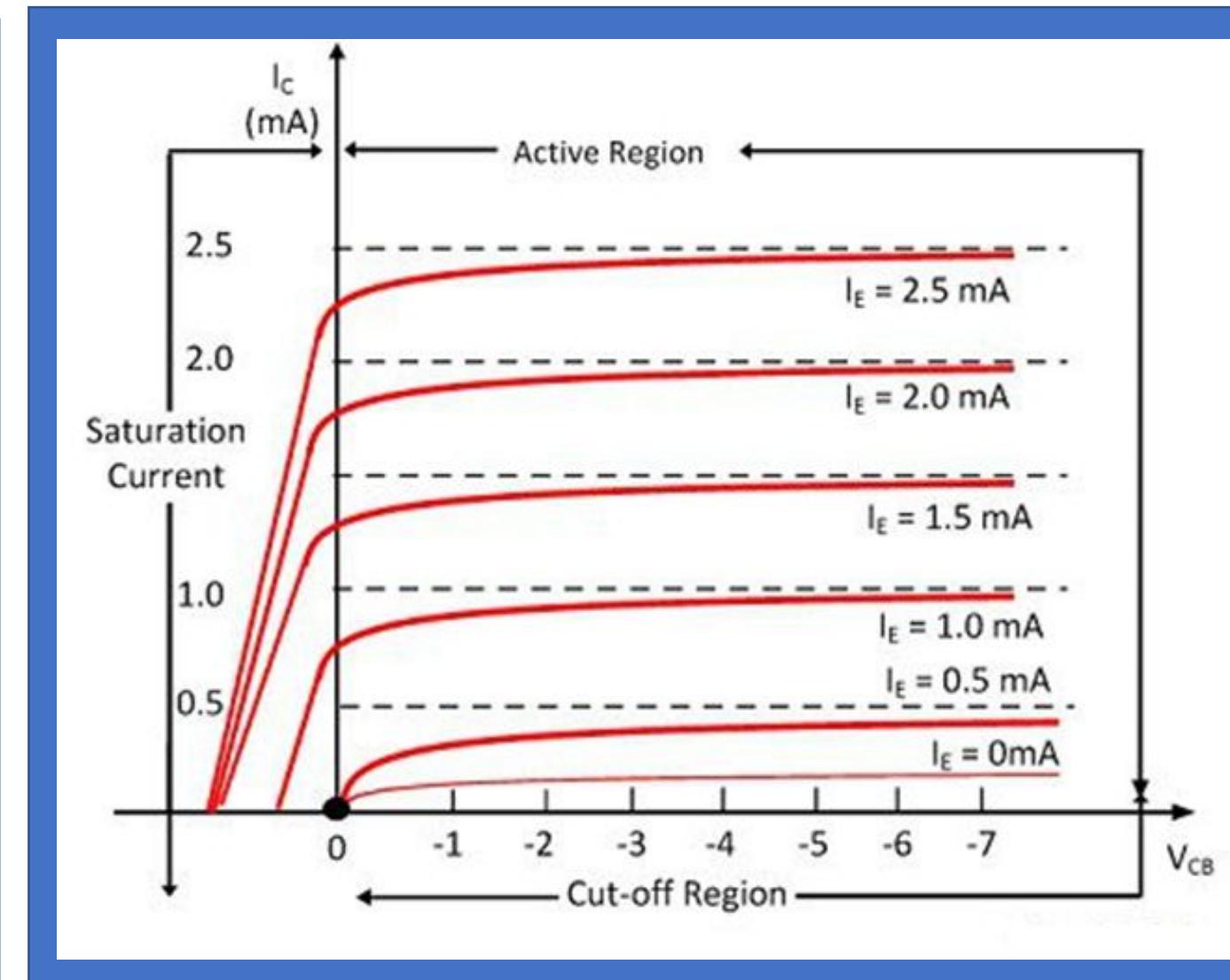
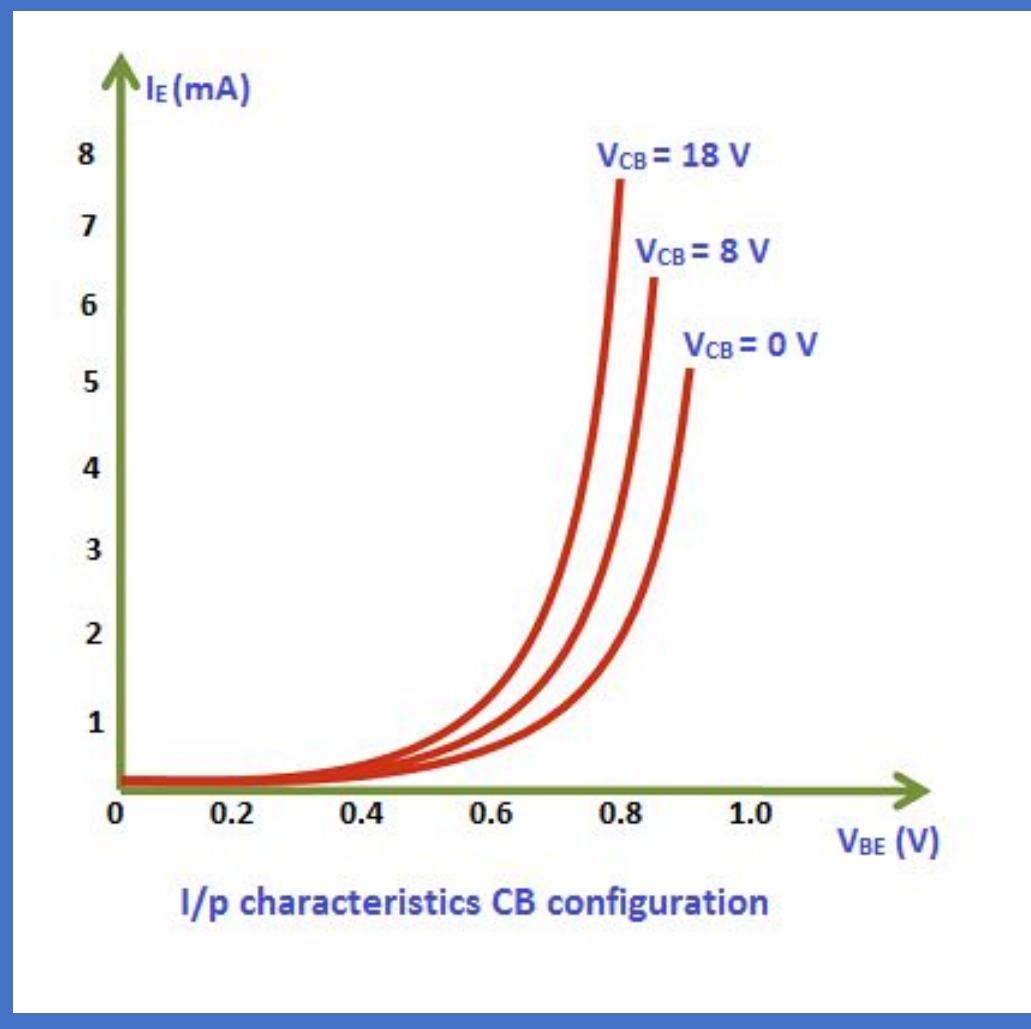
The load regulation also can be expressed as a percentage change in output voltage for each mA change in load current (%/mA).

COMMON BASE CONFIGURATION

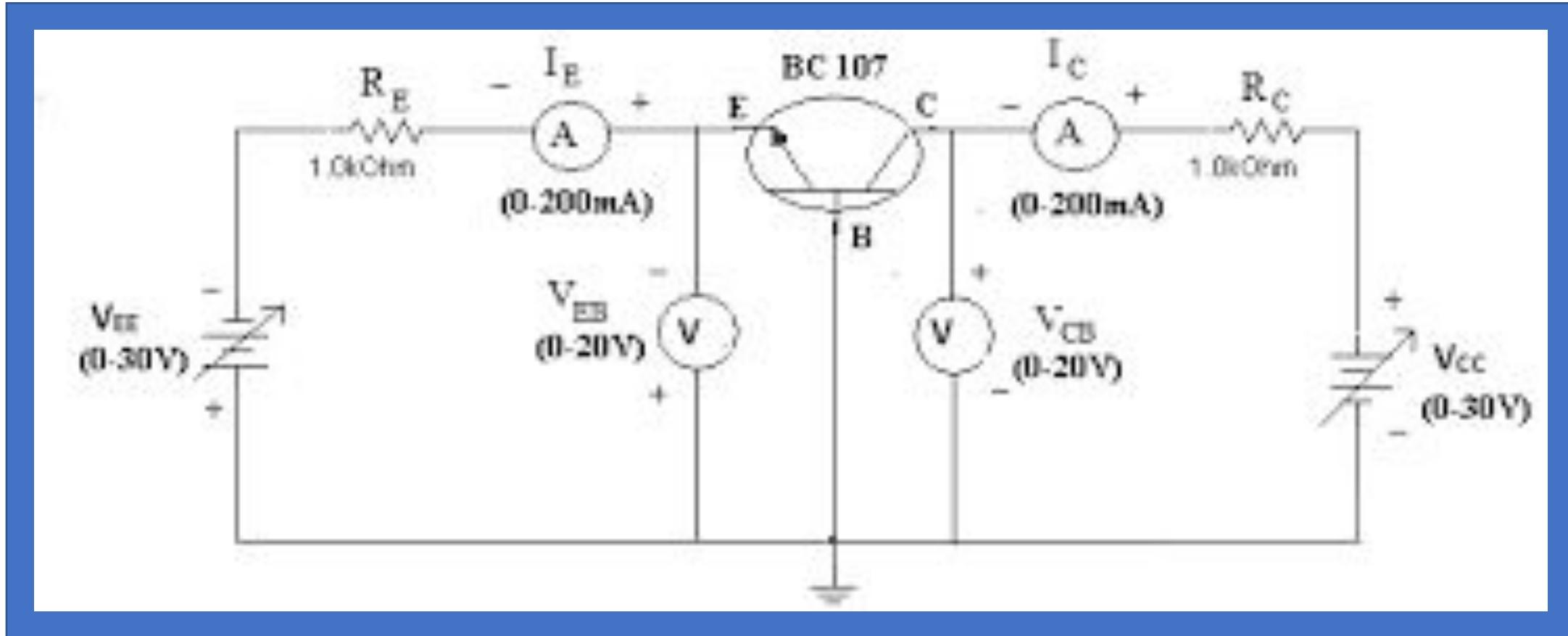


Common Base Configuration

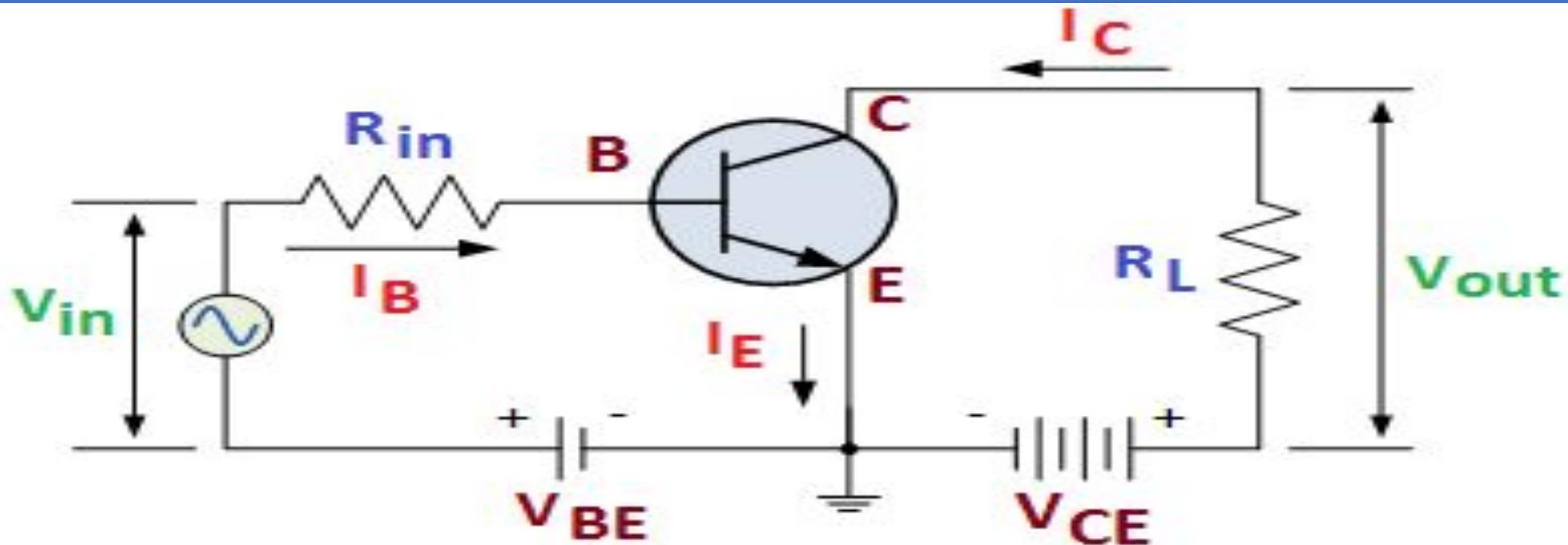
INPUT OUTPUT CHARACTERISTICS OF CB AMPLIFIER



CIRCUIT ARRANGEMENT TO FIND INPUT AND OUTPUT CHARACTERISTICS

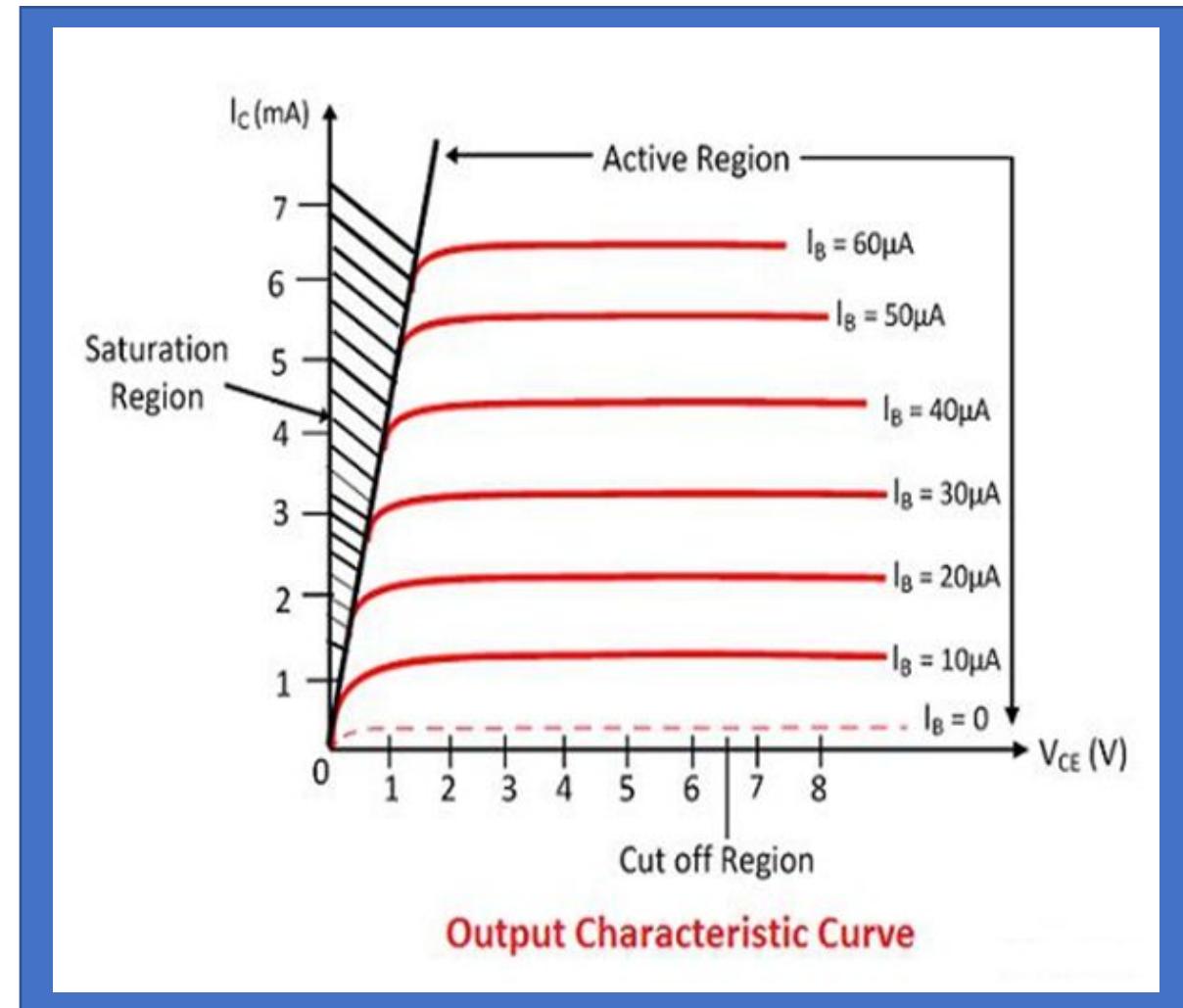
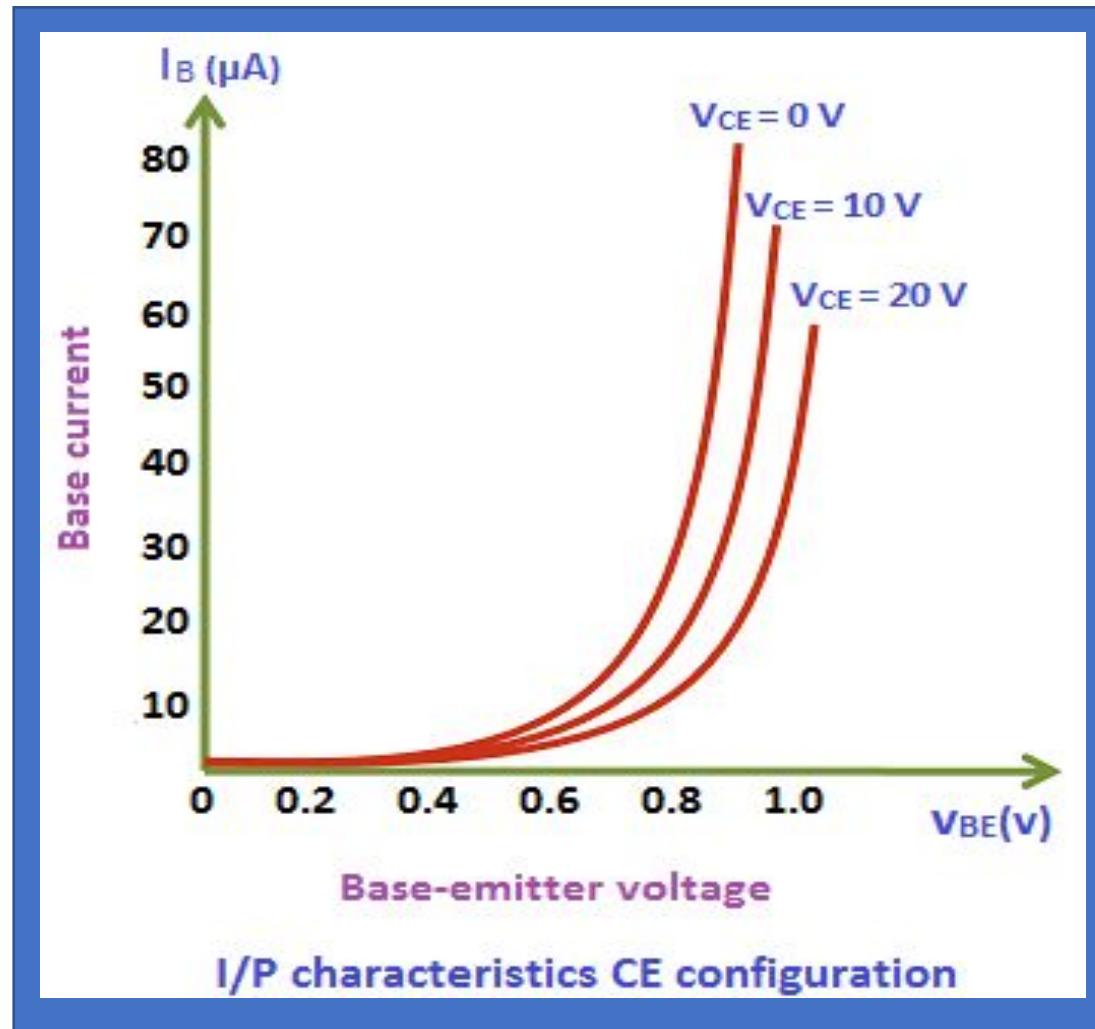


COMMON Emitter CONFIGURATION

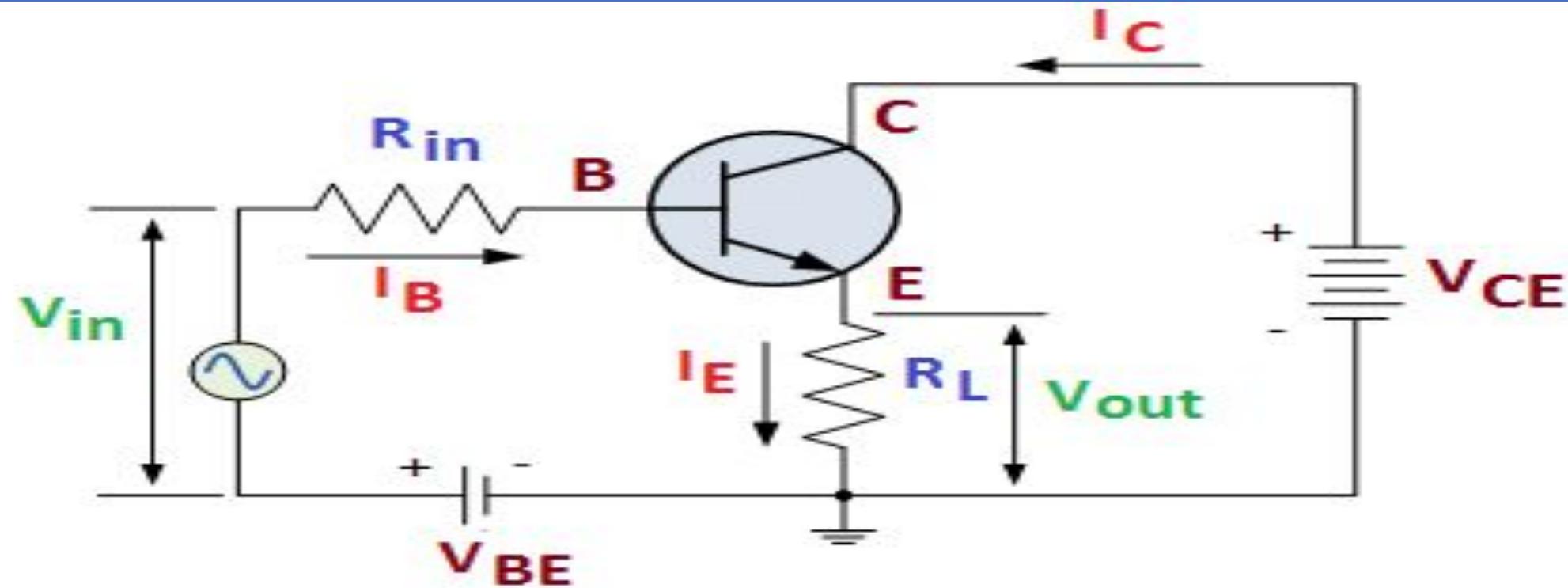


Common Emitter Configuration

INPUT OUTPUT CHARACTERISTICS OF CE AMPLIFIER

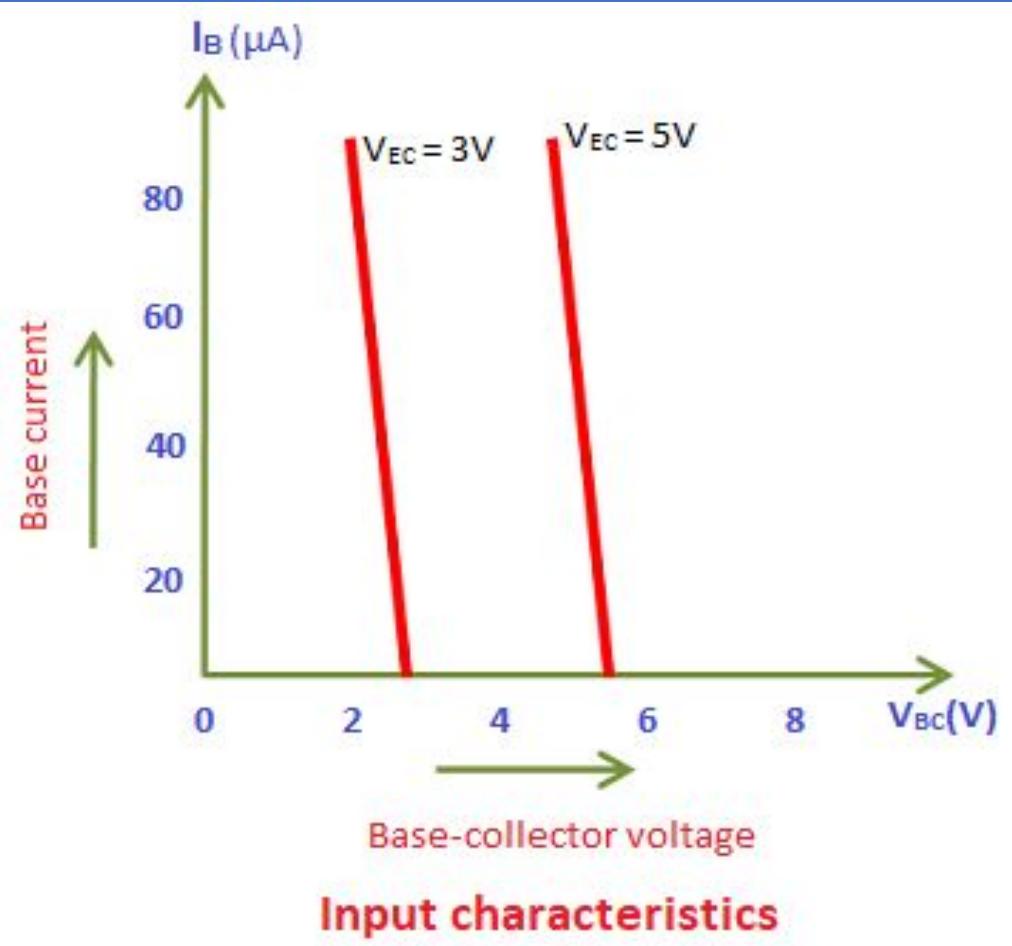


COMMON COLLECTOR CONFIGURATION

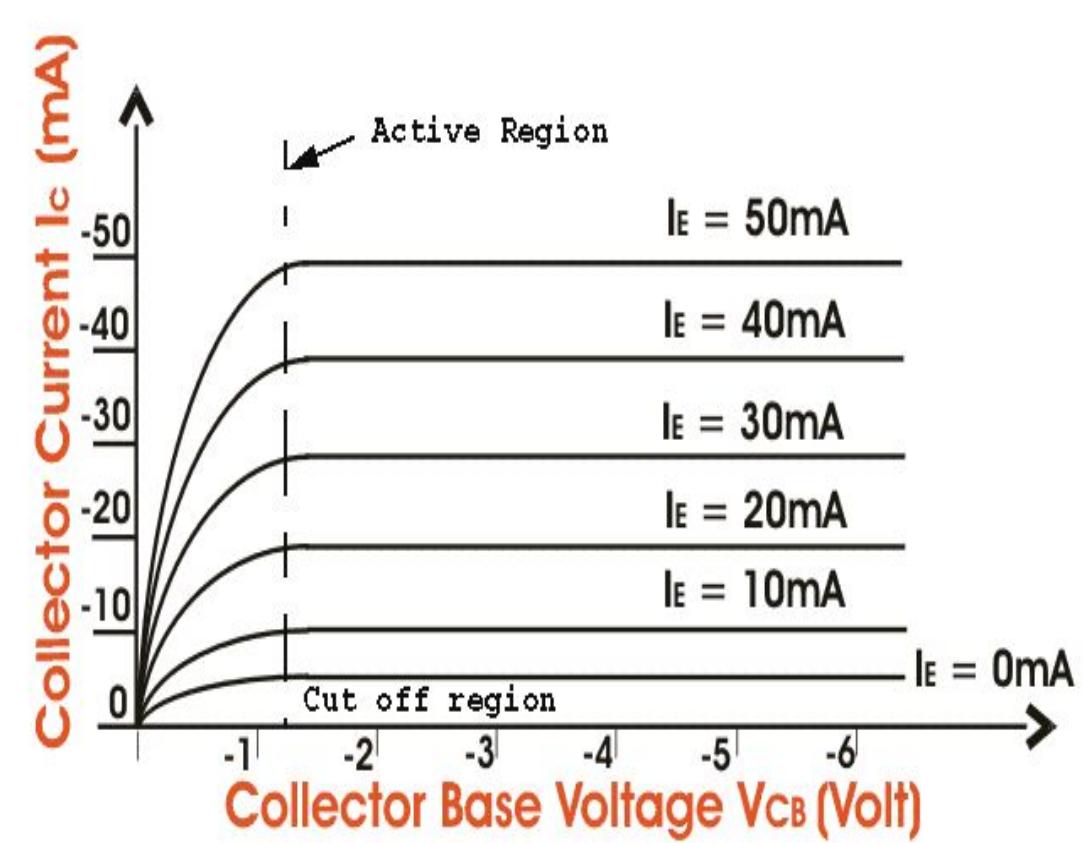


Common Collector Configuration

INPUT OUTPUT CHARACTERISTICS OF CC AMPLIFIER



Input characteristics



CURRENT AMPLIFICATION FACTOR

In CC- Current Amplification Factor (γ_{dc})

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

$$I_E = I_C + I_B$$

$$\Delta I_E = \Delta I_C + \Delta I_B$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

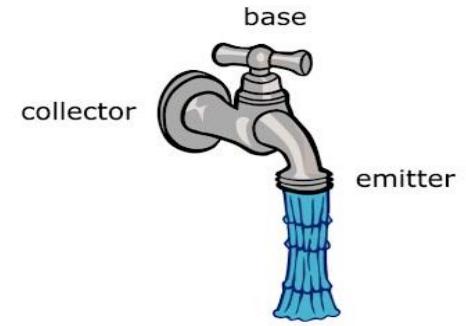
$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

$$\gamma = \frac{\Delta I_E / \Delta I_E}{\Delta I_E / \Delta I_E - \Delta I_C / \Delta I_E}$$

$$\gamma = \frac{1}{1 - \Delta I_C / \Delta I_E}$$

$$\gamma = \frac{1}{1 - \alpha}$$

CURRENT AMPLIFICATION FACTOR



In CB- Current Amplification Factor (α_{dc}):

For a transistor with common base configuration it is defined as the ratio of static (d.c.) collector current I_C to the static emitter current I_E at a constant collector voltage with respect to base.

$$\alpha_{dc} = \left(\frac{I_C}{I_E} \right)_{[V_{CB}=\text{constant}]}$$

$$\beta_{dc} = \left(\frac{I_C}{I_E} \right)_{[V_{CE}=\text{constant}]}$$

In CE- For a transistor with common emitter configuration it is defined as the ratio of static collector current I_C to the static base current I_B at a constant collector voltage with respect to emitter.

RELATION BETWEEN α_{DC} AND β_{DC} :

We know that

$$I_E = I_B + I_C$$

Dividing both sides by I_C , we get

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

or, $\frac{1}{\alpha_{dc}} = \frac{1}{\beta_{dc}} + 1$

$$\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}}$$

or, $\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}$

COLLECTOR CURRENT IN TERMS OF LEAKAGE CURRENT

$$I_C = \alpha I_\beta + I_{CBO}$$

$$I_E = I_C + I_B = (\alpha I_\beta + I_{CBO}) + I_B$$

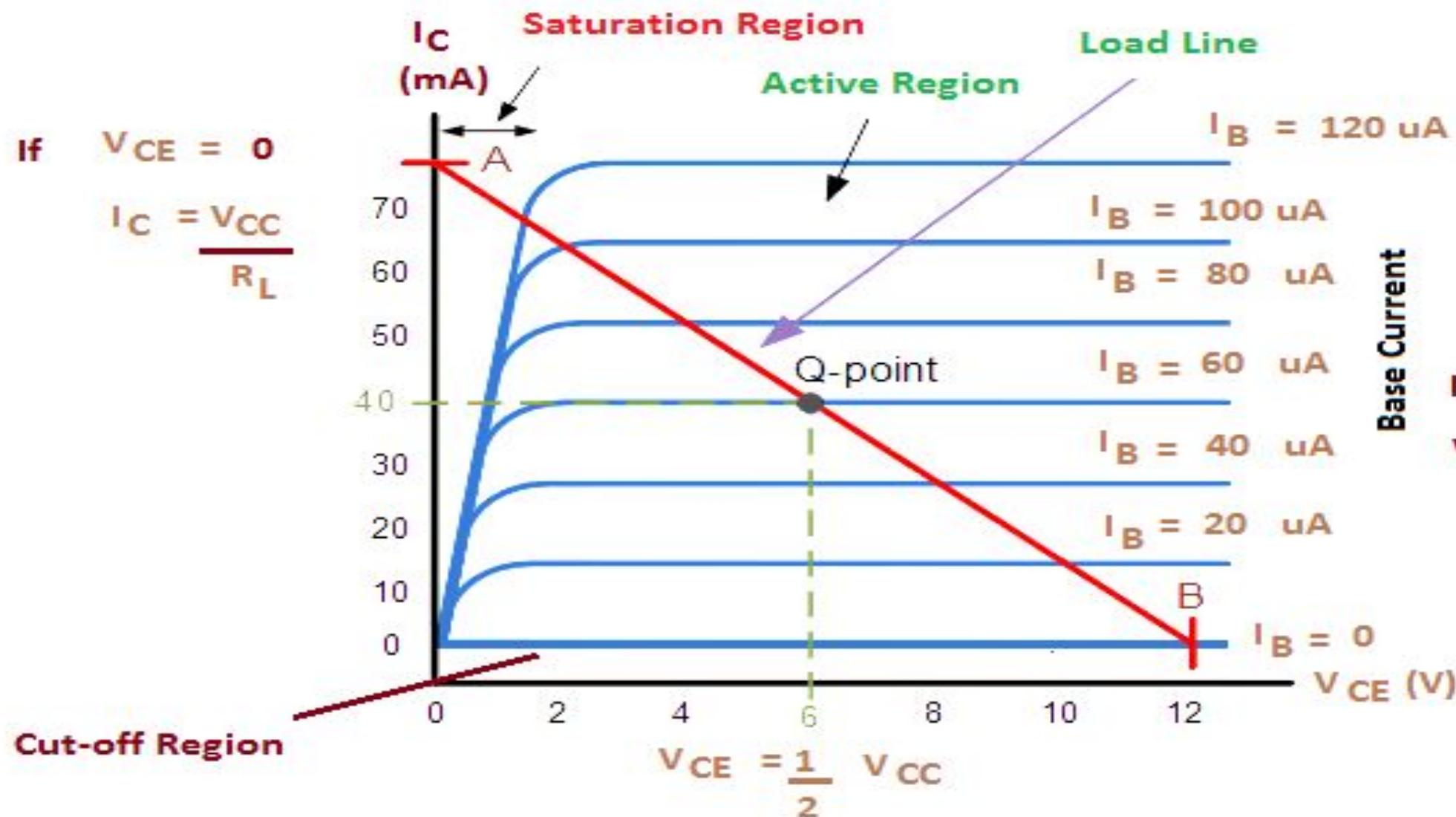
$$I_E(1 - \alpha) = I_\beta + I_{CBO}$$

$$\begin{aligned} I_E &= I_B \left(\frac{1}{1 - \alpha} \right) + I_{CBO} \left(\frac{1}{1 - \alpha} \right) \\ &= (\beta + 1)I_B + (\beta + 1)I_{CBO} \end{aligned}$$

Comparison of configurations

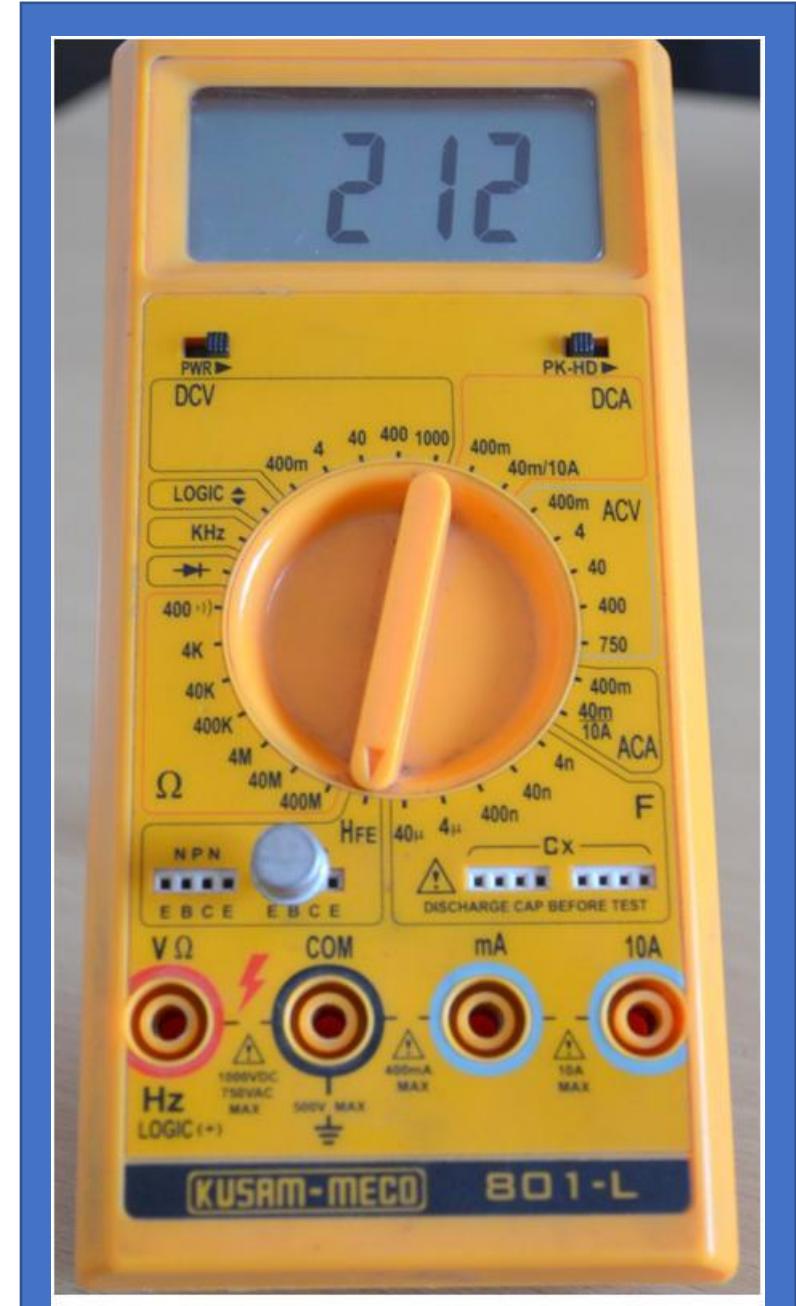
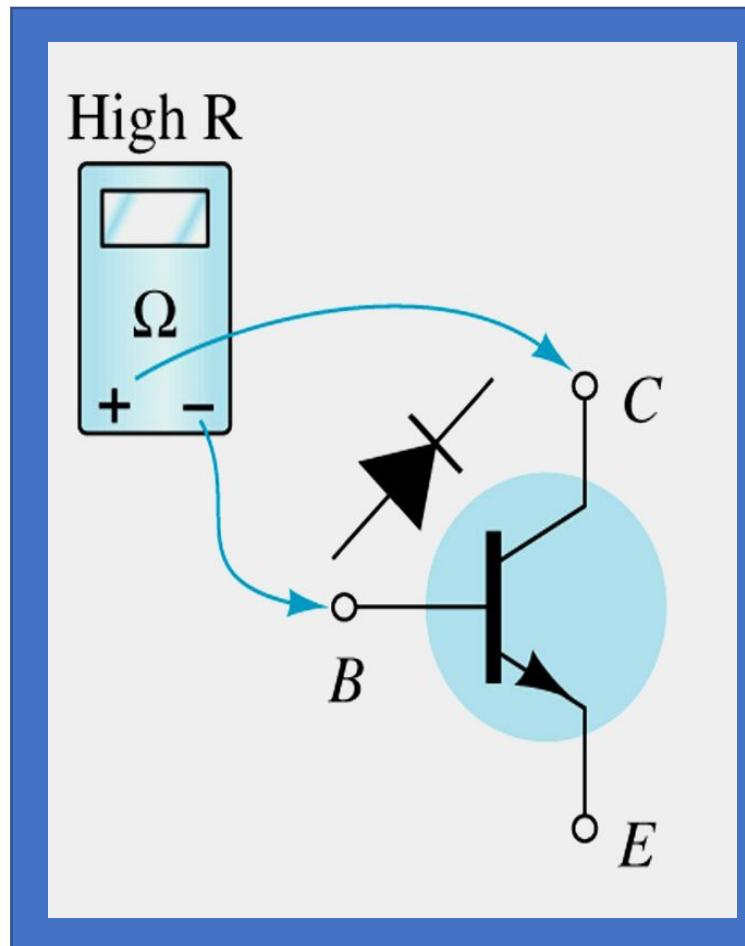
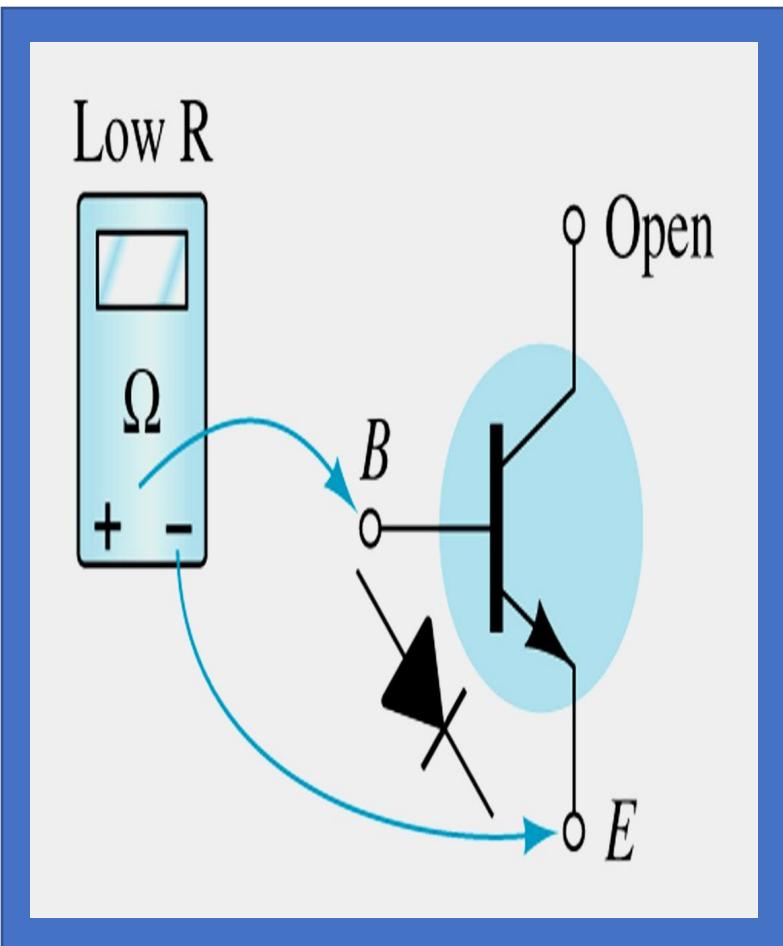
Sr. No.	Parameter	CB	CE	CC
1.	Common terminal between input and output	Base	Emitter	Collector
2.	Input current	I_E	I_B	I_B
3.	Output current	I_C	I_C	I_E
4.	Current gain	$\alpha_{dc} = I_C / I_E$	$\beta_{dc} = I_C / I_B$	$\gamma_{dc} = I_E / I_B$
5.	Input voltage	V_{EB}	V_{BE}	V_{BC}
6.	Output voltage	V_{CB}	V_{CE}	V_{BC}
7.	Voltage gain	Medium	Medium	Less than 1
8.	Input resistance	Very low (20Ω)	Low ($1k\Omega$)	High ($500 k\Omega$)
9.	Output resistance	Very high ($1M\Omega$)	High ($40 K\Omega$)	Low (50Ω)
10.	Applications	As preamplifier	Audio amplifier	For impedance matching

DC LOAD LINE



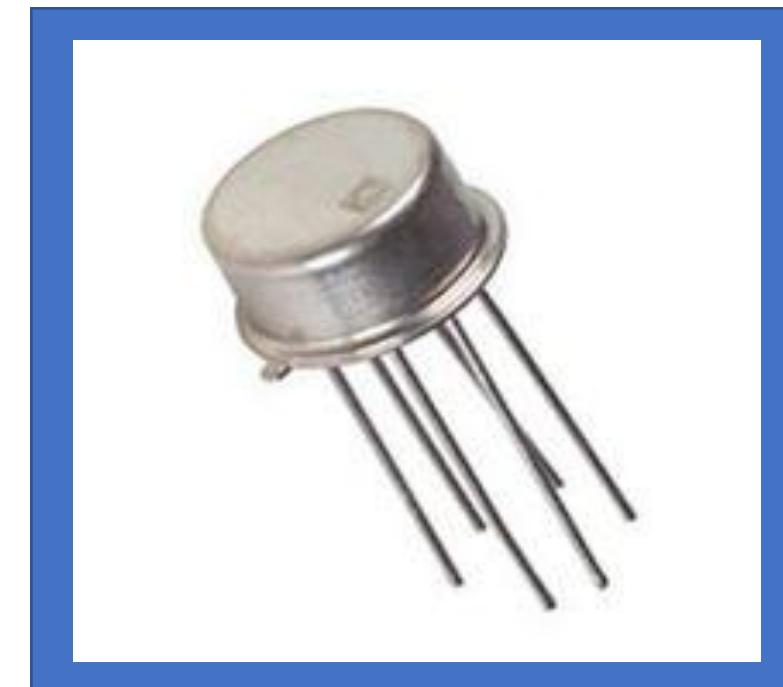
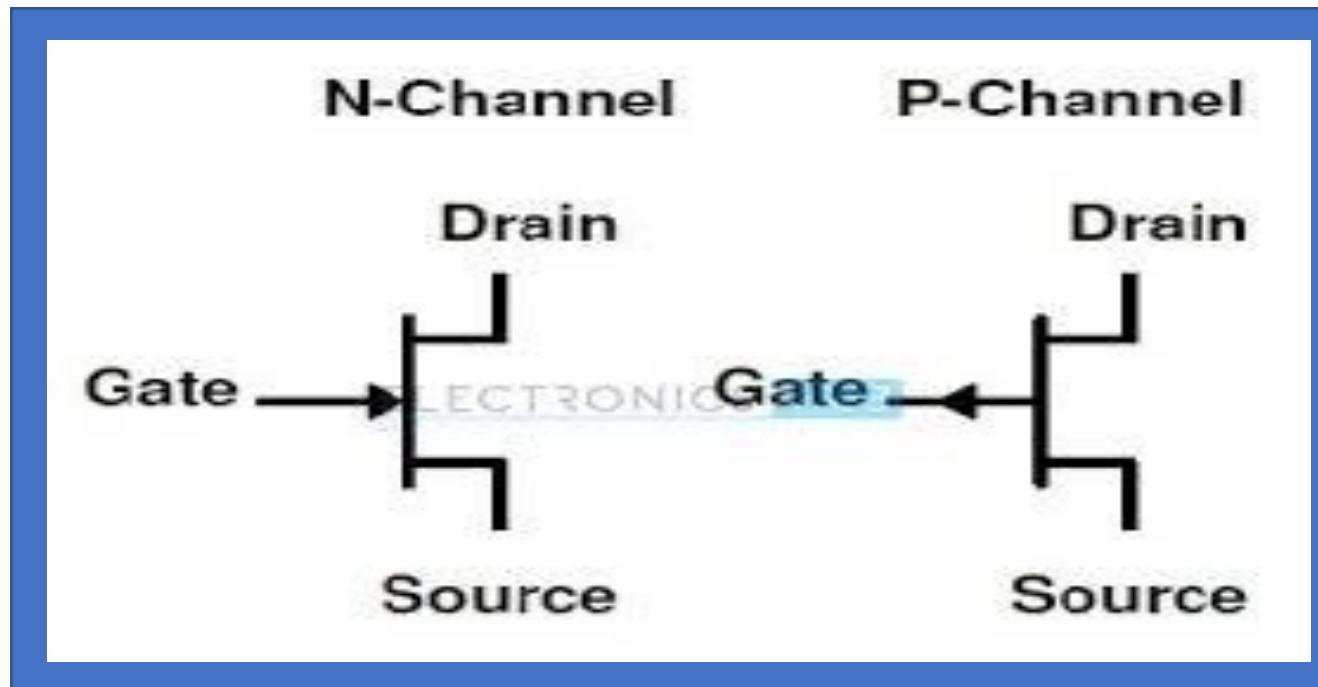
Transistor Testing

Using DMM: some DMM's will measure β_{DC} or hfe.

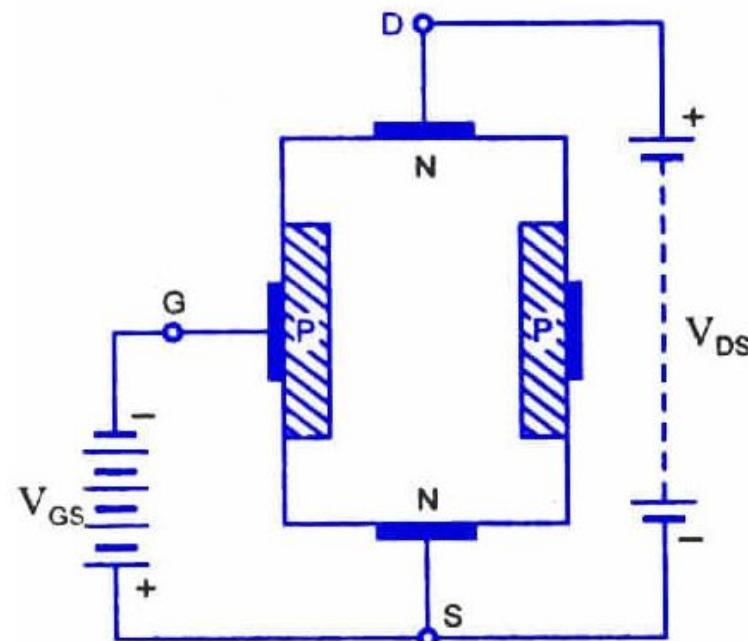


JUNCTION FIELD EFFECT TRANSISTORS (JFET)

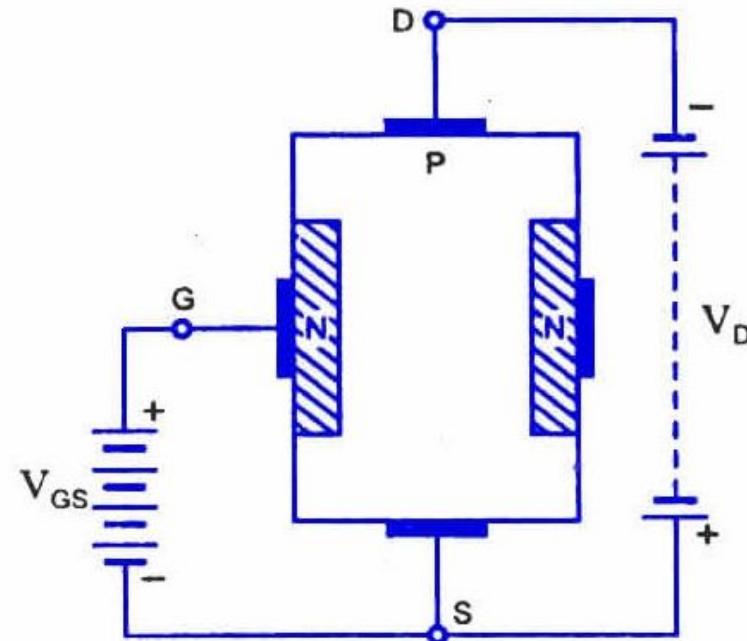
- FET is a semiconductor device which depends for its operation on the control of current by an electric field.



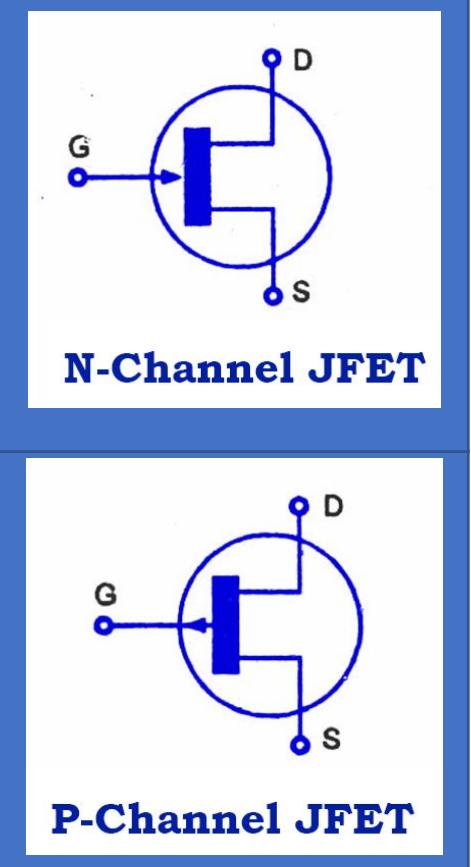
JUNCTION FIELD EFFECT TRANSISTOR (JFET)



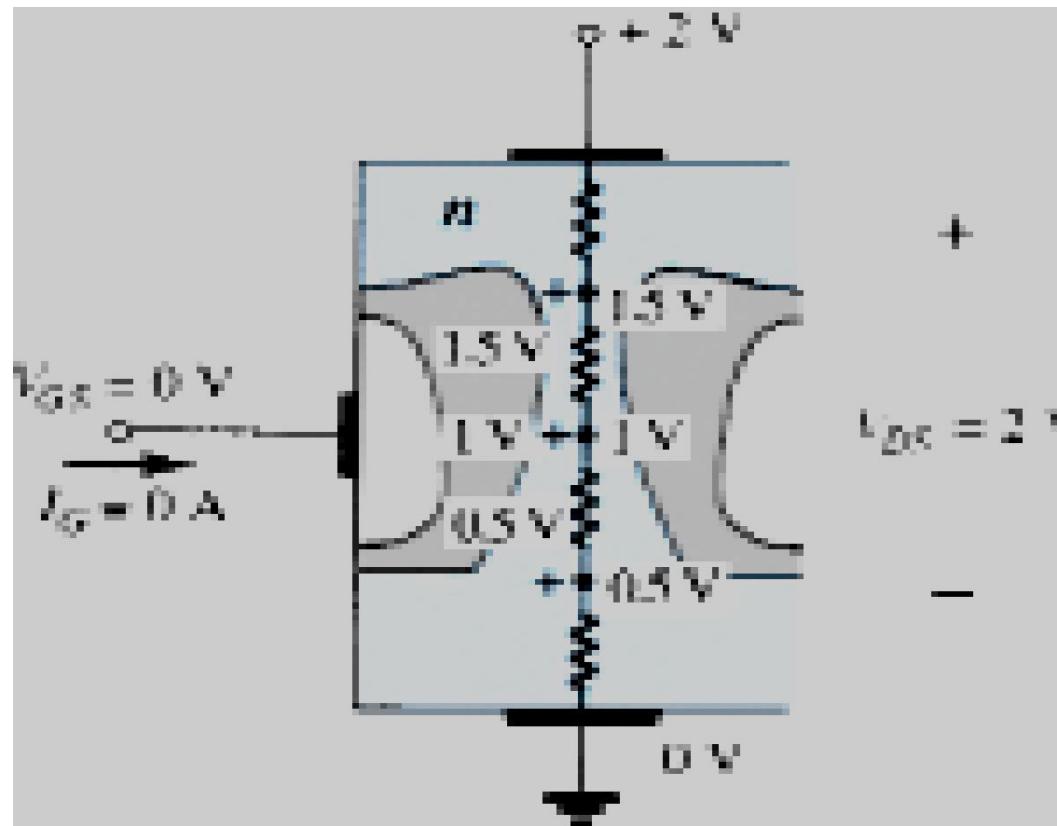
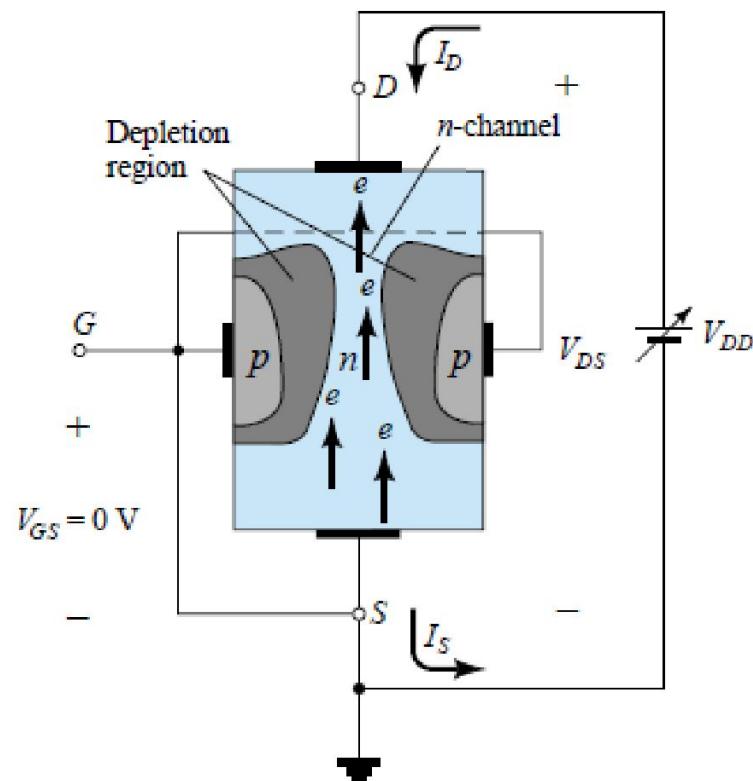
N-Channel JFET



P-Channel JFET

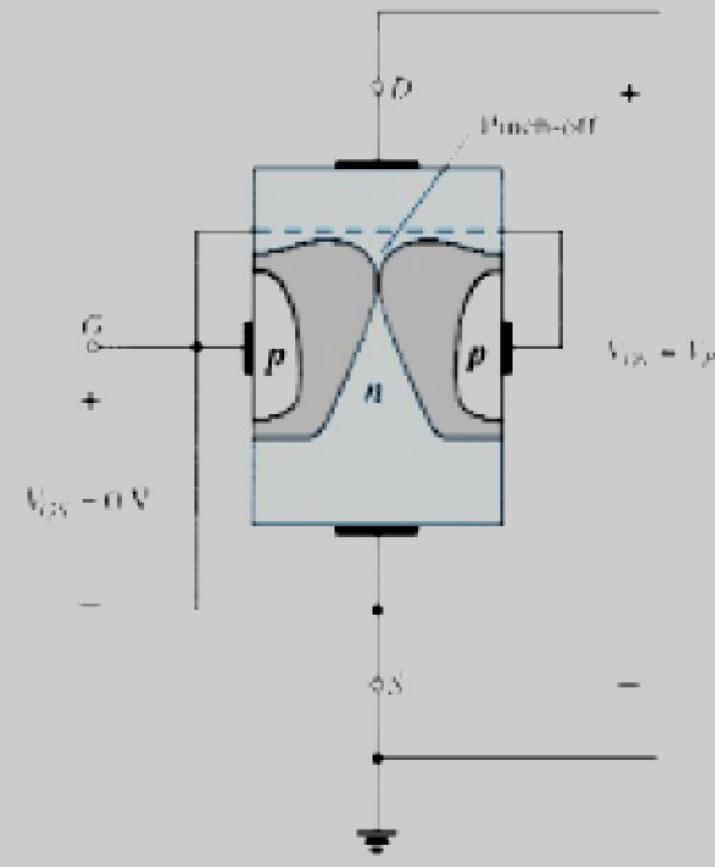
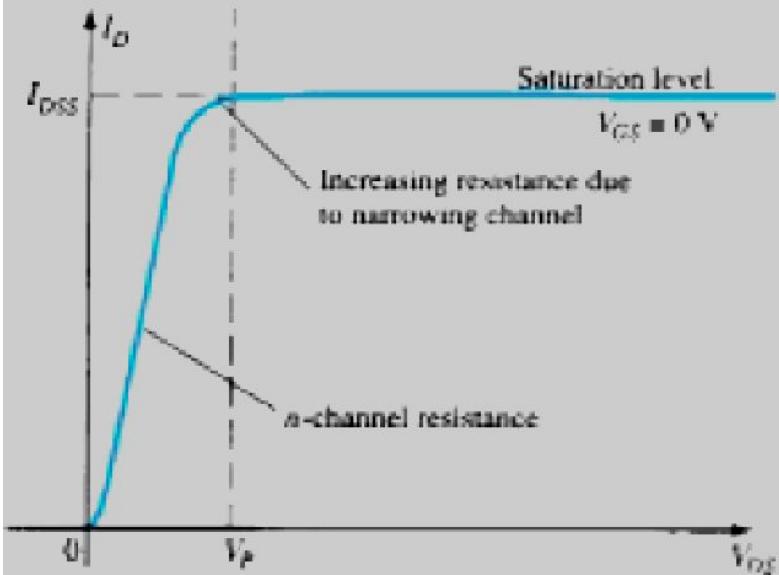


Construction and Characteristics of JFETs

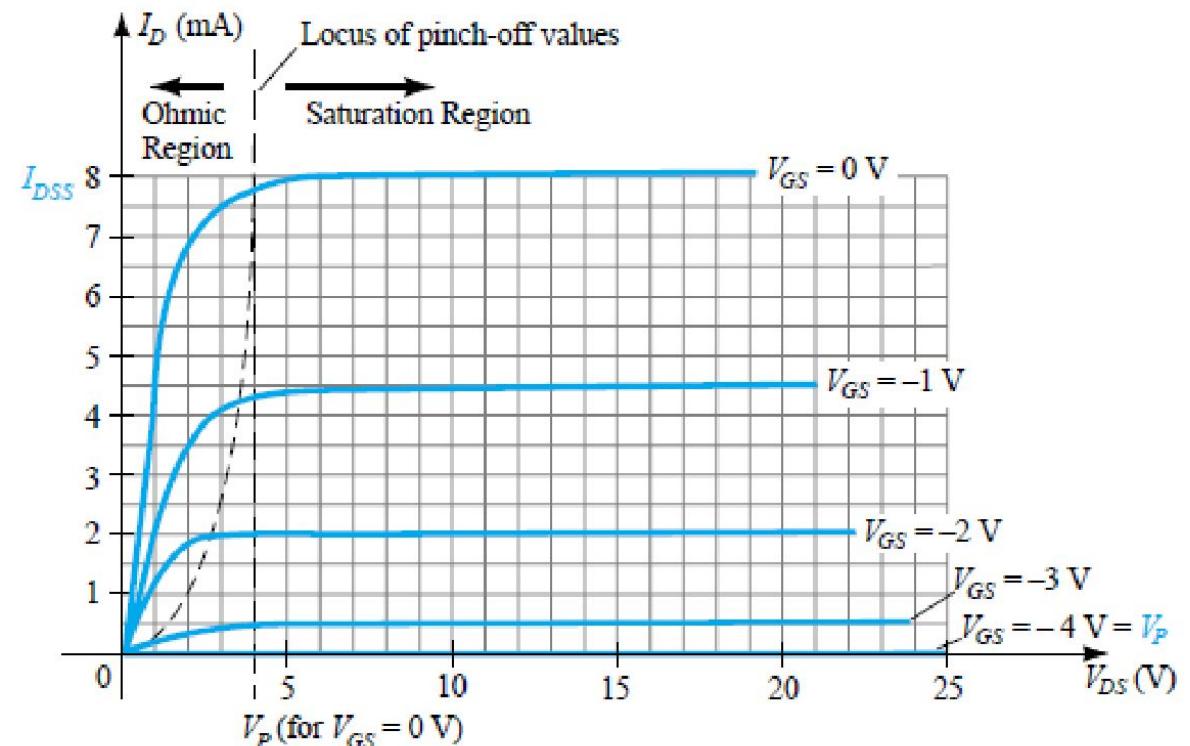
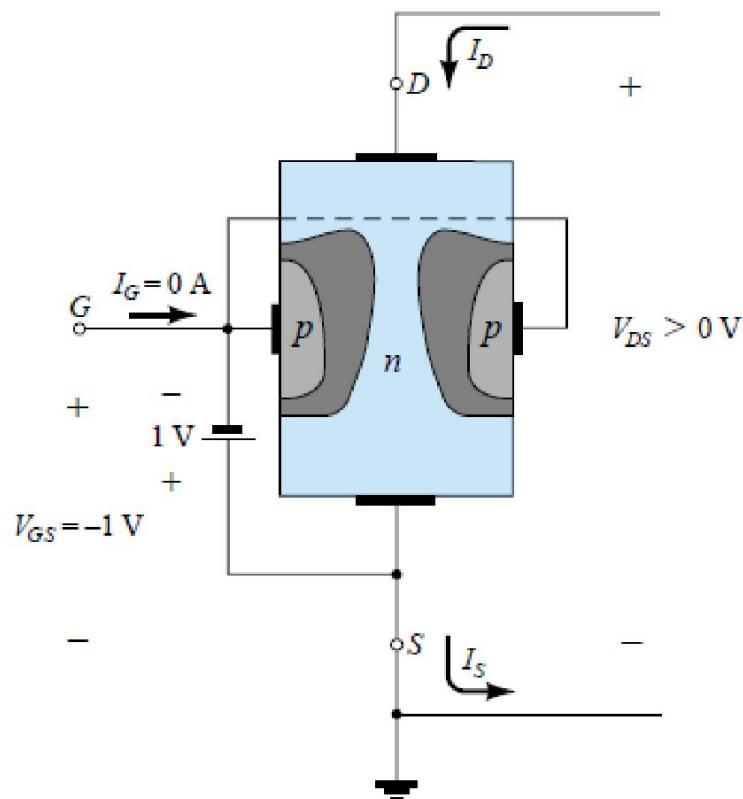


Varying reverse-bias
potentials across the *p-n* junction
of an *n*-channel JFET.

Pinch-OFF



Construction and Characteristics of JFETs

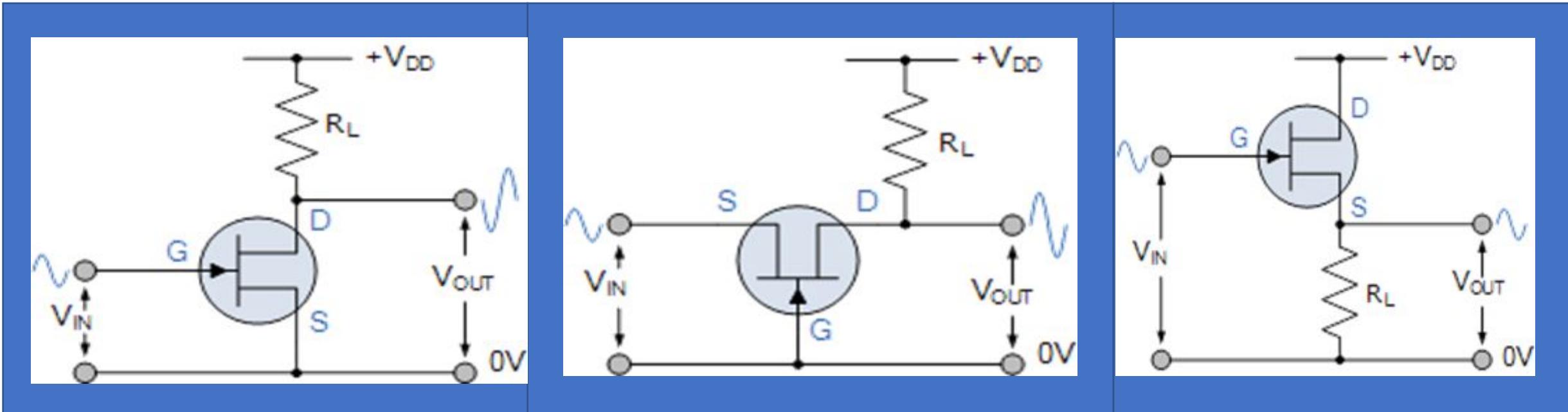


n-Channel JFET characteristics with I_{DSS} 8 mA and V_P 4 V.

Water Analogy for the JFET control mechanisms



CONFIGURATIONS OF JFET



Common Source

Common Gate

Common Drain

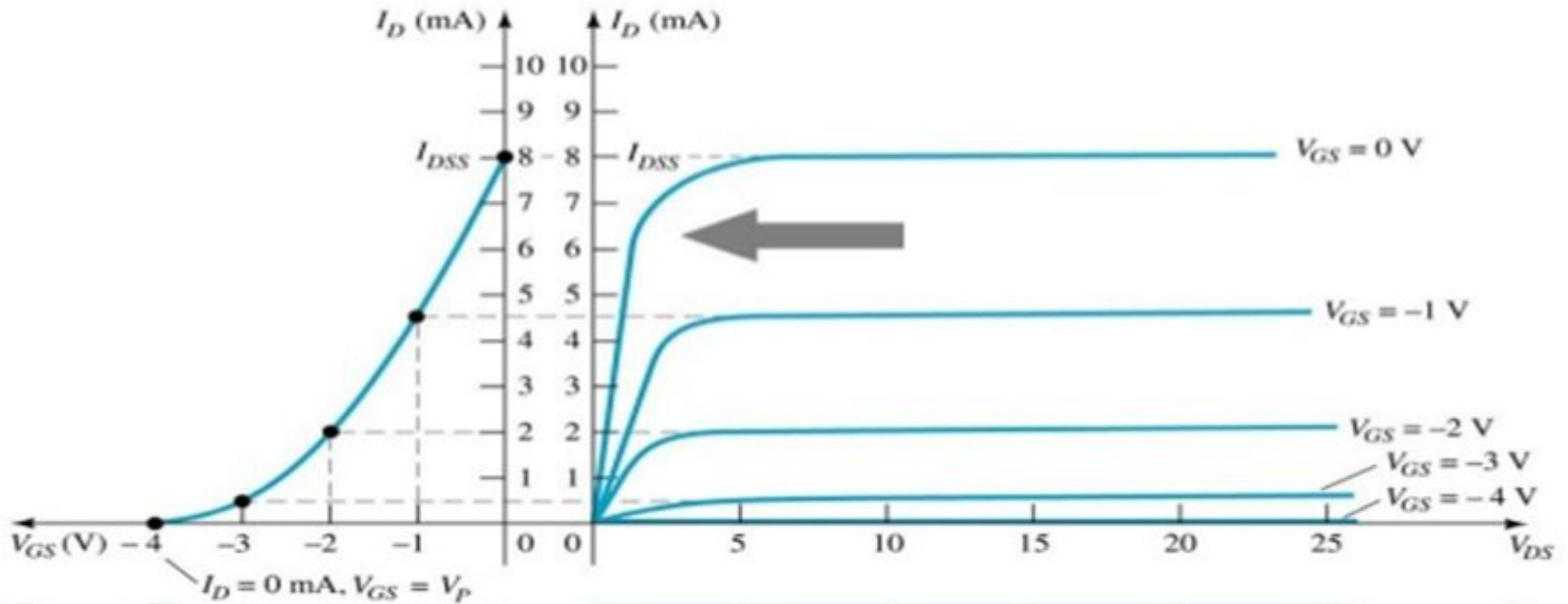
Shockley's Equation $I_D = I_{DSS} \{1 - V_{GS}/V_{p-off}\}^2$

OPERATING REGIONS OF JFET

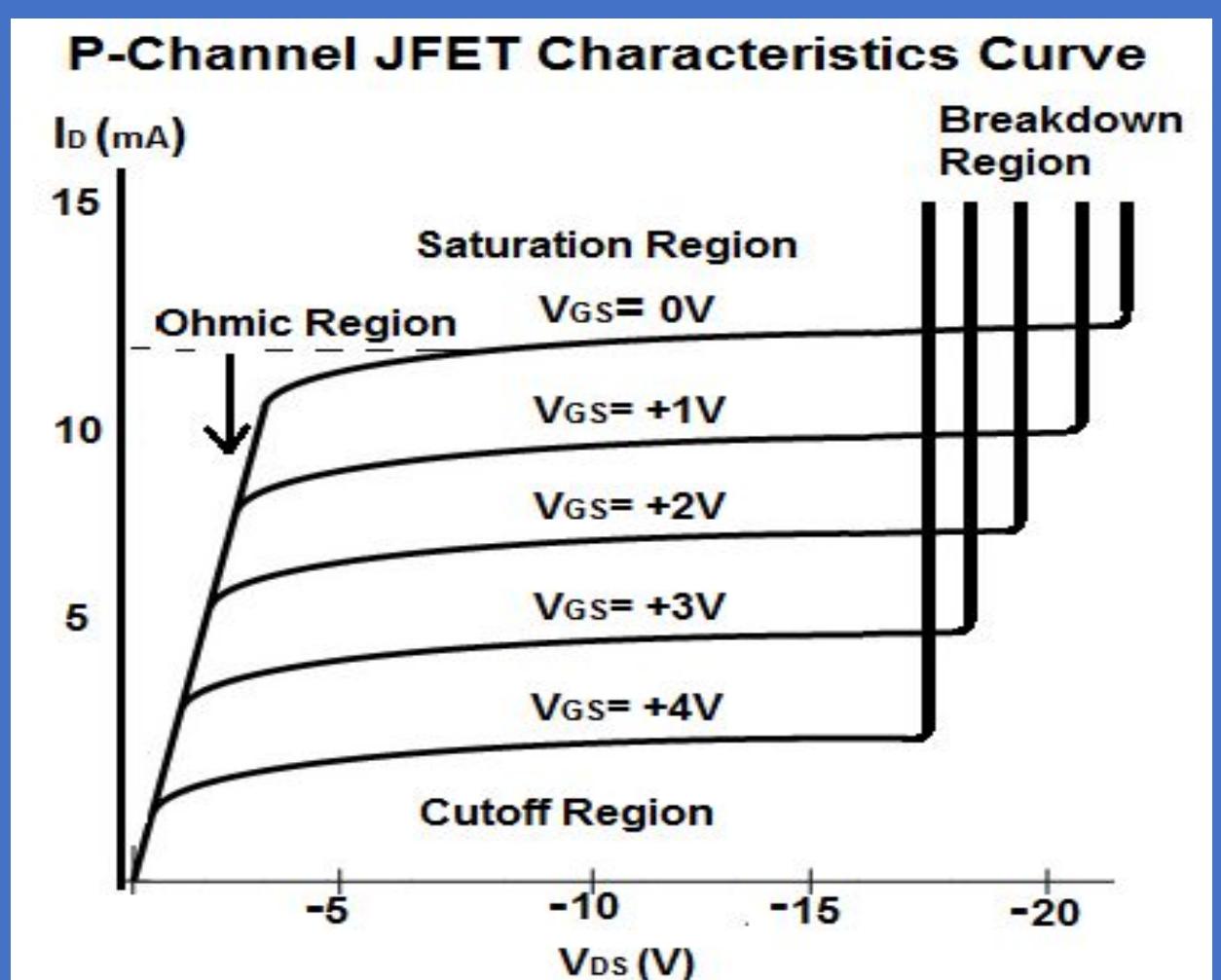
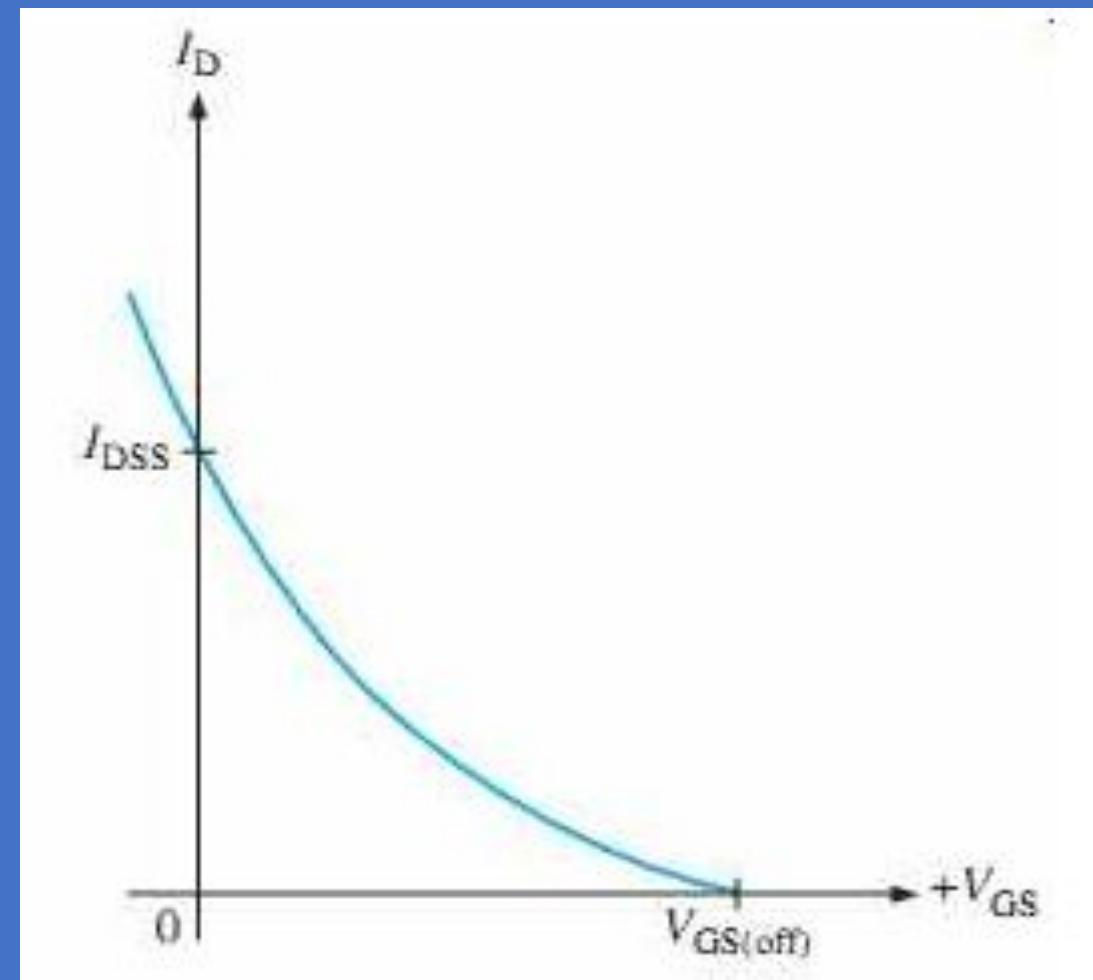
- **Ohmic Region** – When $V_{GS} = 0$ the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.
- **Cut-off Region** – This is also known as the pinch-off region when the Gate voltage, V_{GS} , is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.
- **Saturation or Active Region** – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.
- **Breakdown Region** – The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.

TRANSFER CHARACTERISTICS OF N CHANNEL JFET

Transfer Curve



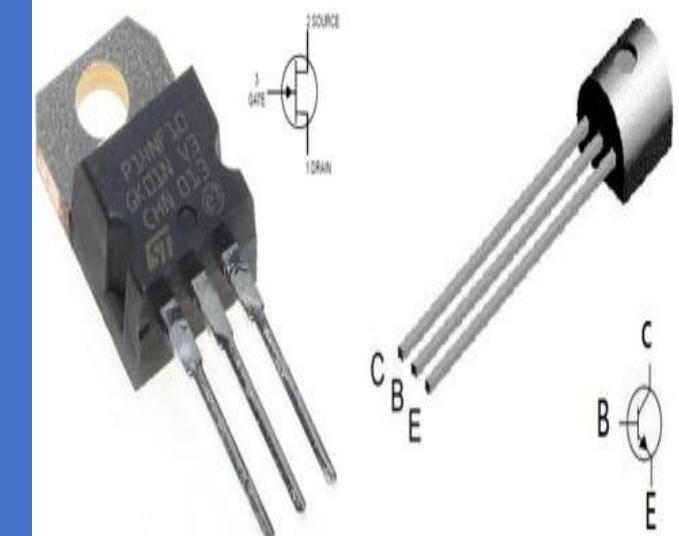
TRANSFER CHARACTERISTICS OF P CHANNEL JFET



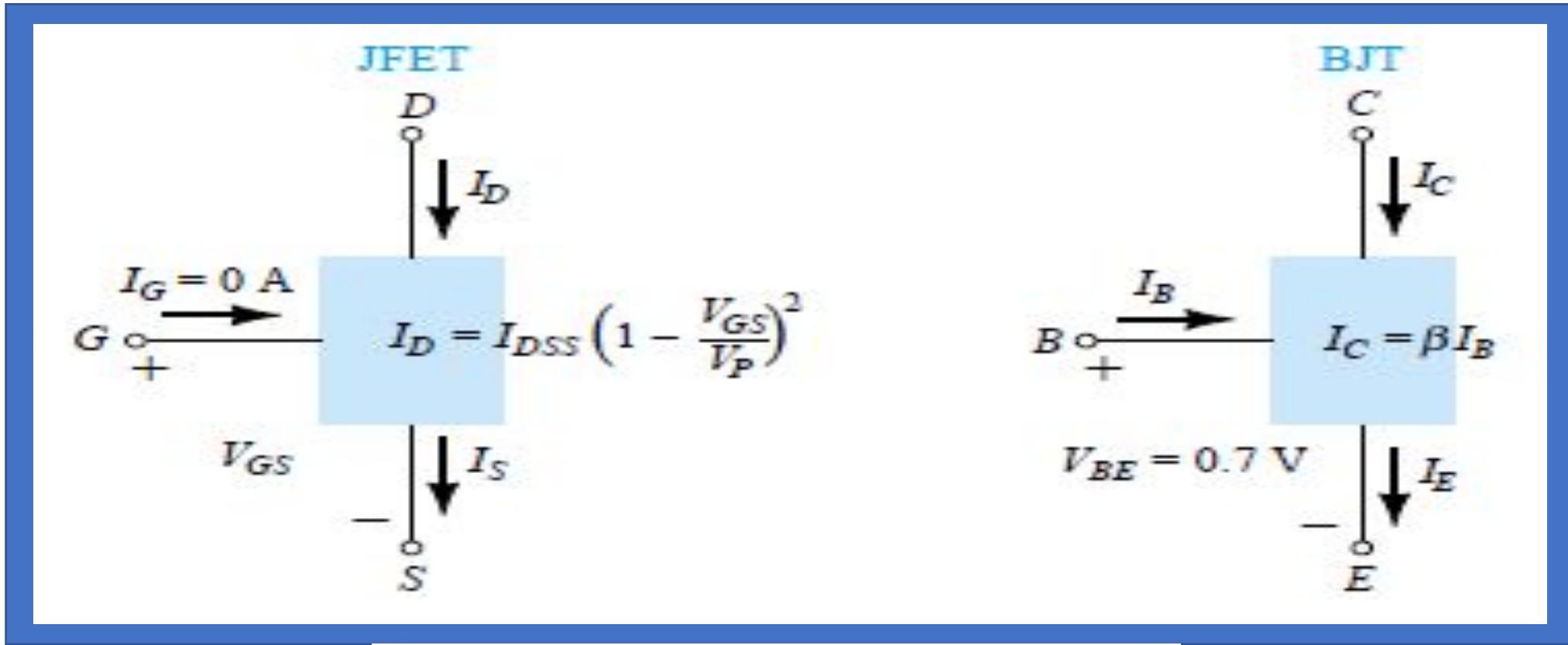
DIFFERENCE BETWEEN BJT AND FET

	JFET	BJT
1.	Unipolar device (current conduction is only due to one type of majority carrier either electron or hole).	Bipolar device (current condition, by both types of carriers, i.e., majority and minority-electrons and holes)
2.	The operation depends on the control of a junction depletion width under reverse bias.	The operation depends on the injection of minority carriers across a forward biased junction.
3.	Voltage driven device. The current through the two terminals is controlled by a voltage at the third terminal (gate).	Current driven device. The current through the two terminals is controlled by a current at the third terminal (base).
4.	Low noise level.	High noise level.
5.	High input impedance (due to reverse bias).	Low input impedance (due to forward bias).
6.	Gain is characterised by transconductance.	Gain is characterized by voltage gain.
7.	Better thermal stability.	Less thermal stability.

Difference Between BJT and FET



JFET AND BJT



JFET	BJT
$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$	$I_C = \beta I_B$
$I_D = I_S$	$I_C \cong I_E$
$I_G \cong 0 \text{ A}$	$V_{BE} \cong 0.7 \text{ V}$

IMPORTANT EQUATIONS FOR DC ANALYSIS OF FET

$$I_G \approx 0 \text{ A}$$

$$I_D = I_S$$

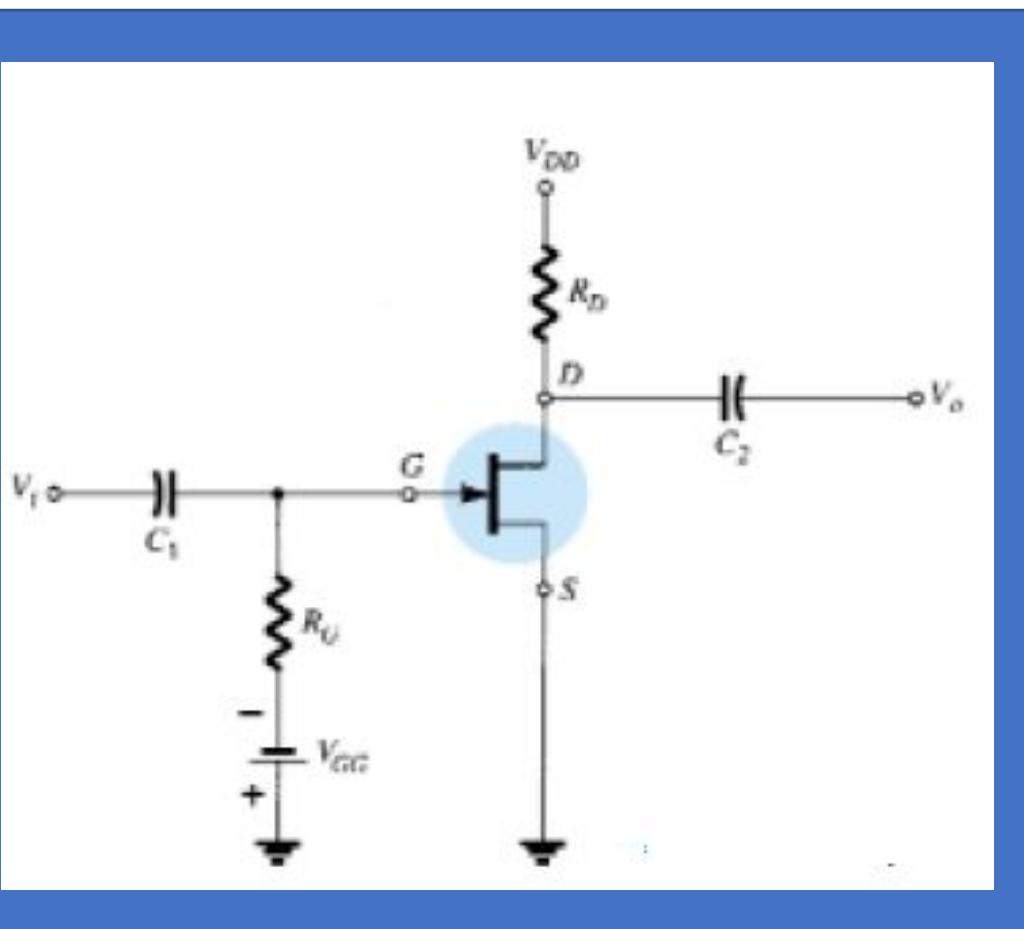
$$I_D = I_{DSS} \left(\frac{1 - V_{GS}}{V_P} \right)^2$$

TABLE V_{GS} versus I_D Using Shockley's Equation

V_{GS}	I_D
0	I_{DSS}
$0.3 V_P$	$I_{DSS}/2$
$0.5 V_P$	$I_{DSS}/4$
V_P	0 mA

FIXED BIAS CONFIGURATION

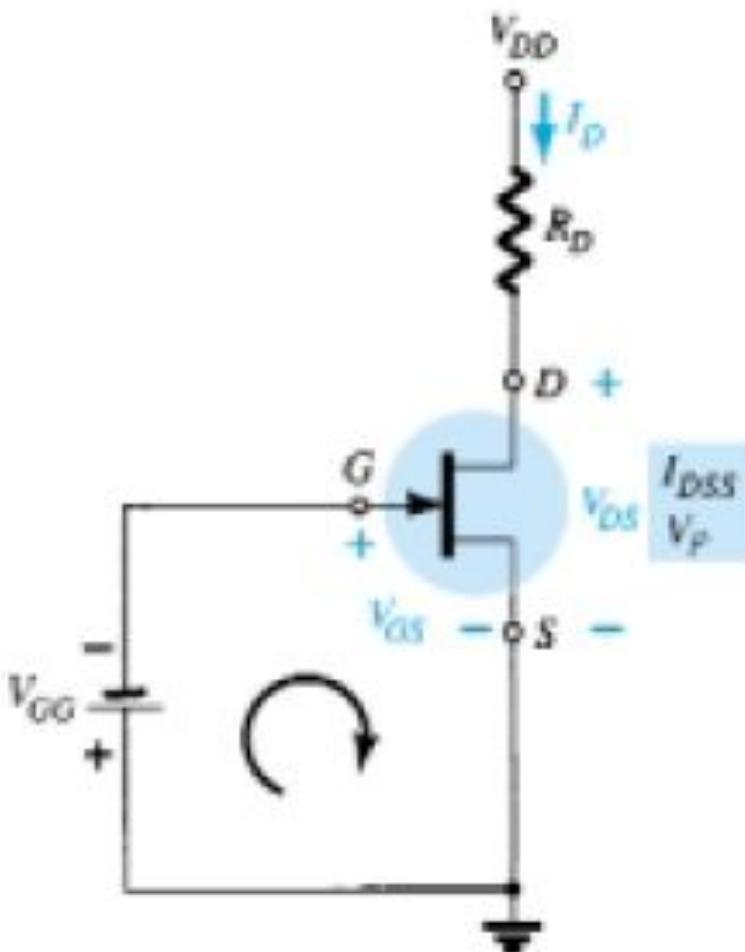
The simplest of biasing arrangements for the *n*-channel JFET appears in Fig. Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or graphical approach.



$$I_G \approx 0 \text{ A}$$

$$V_{RG} = I_G R_G = (0 \text{ A}) R_G = 0 \text{ V}$$

FIXED BIAS CONFIGURATION



$$-V_{GG} - V_{GS} = 0$$

$$V_{GS} = -V_{GG}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the notation “fixed-bias configuration.”

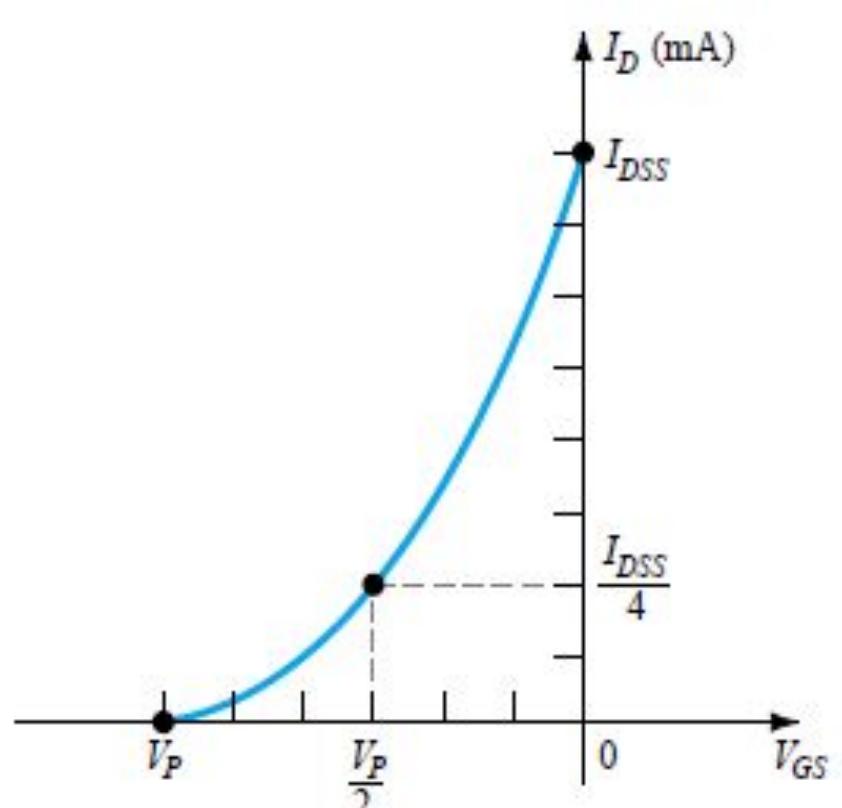
The resulting level of drain current I_D is now controlled by Shockley’s equation:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

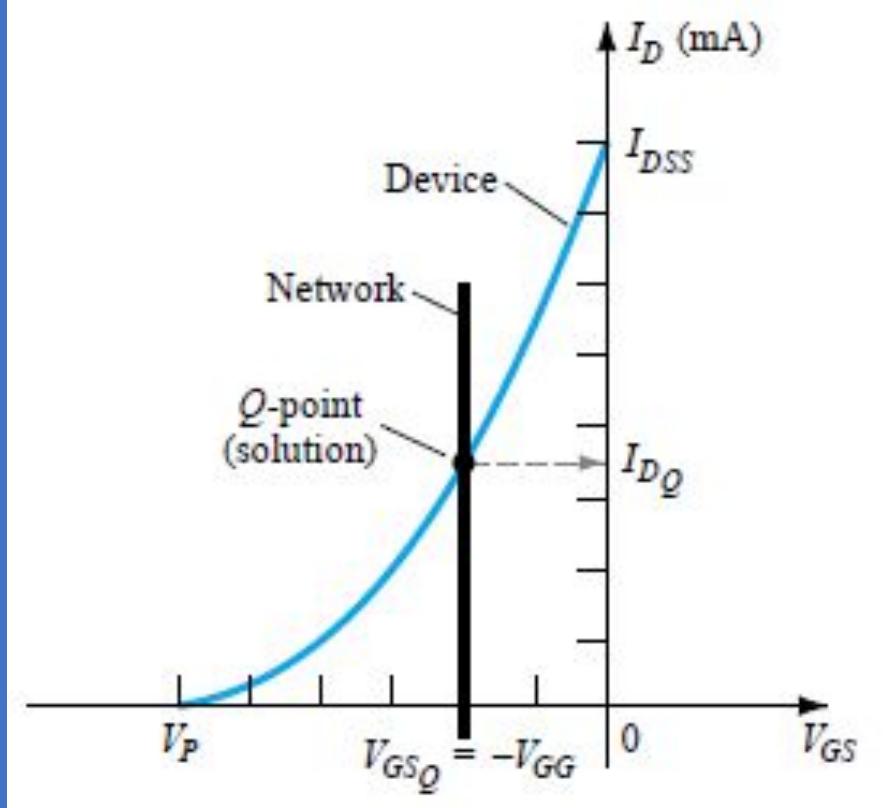
Since V_{GS} is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley’s equation and the resulting level of I_D calculated. This is one of the few instances in which a mathematical solution to a FET configuration is quite direct.

GRAPHICAL ANALYSIS OF FIXED BIAS CONFIGURATION

A graphical analysis would require a plot of Shockley's equation as shown in Fig.



Plotting Shockley's equation.



Finding the solution for the fixed-bias configuration.

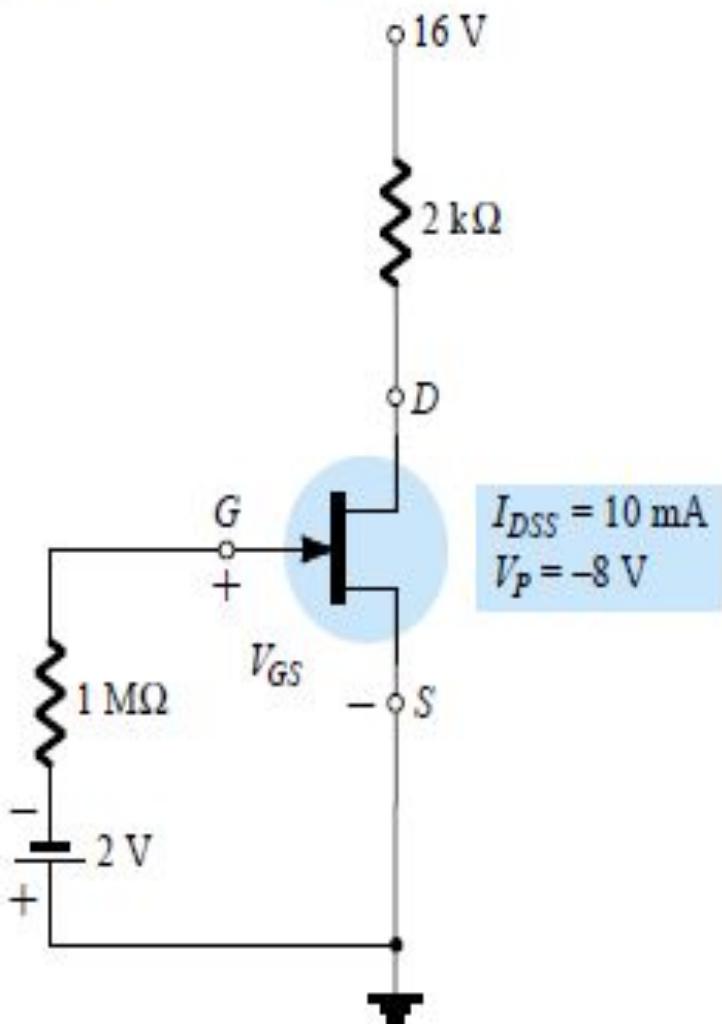
GRAPHICAL ANALYSIS OF FIXED BIAS CONFIGURATION

In Fig. 6.4 the fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$. At any point on the vertical line, the level of V_{GS} is $-V_{GG}$ —the level of I_D must simply be determined on this vertical line. The point where the two curves intersect is the common solution to the configuration—commonly referred to as the *quiescent* or *operating point*. The subscript Q will be applied to drain current and gate-to-source voltage to identify their levels at the Q -point. Note in Fig. 6.4 that the quiescent level of I_D is determined by drawing a horizontal line from the Q -point to the vertical I_D axis as shown in Fig.

EXAMPLE 1

Determine the following for the network of Fig.

- (a) V_{GSQ}
- (b) I_{DQ}
- (c) V_{DS}
- (d) V_D
- (e) V_G
- (f) V_S .



Solution

Mathematical Approach:

$$(a) V_{GSQ} = -V_{GG} = -2 \text{ V}$$

$$(b) I_{DQ} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10 \text{ mA} \left(1 - \frac{-2 \text{ V}}{-8 \text{ V}}\right)^2 = 10 \text{ mA} (1 - 0.25)^2 = 10 \text{ mA} (0.75)^2 = 10 \text{ mA} (0.5625) = 5.625 \text{ mA}$$

$$(c) V_{DS} = V_{DD} - I_D R_D = 16 \text{ V} - (5.625 \text{ mA})(2 \text{ k}\Omega) = 16 \text{ V} - 11.25 \text{ V} = 4.75 \text{ V}$$

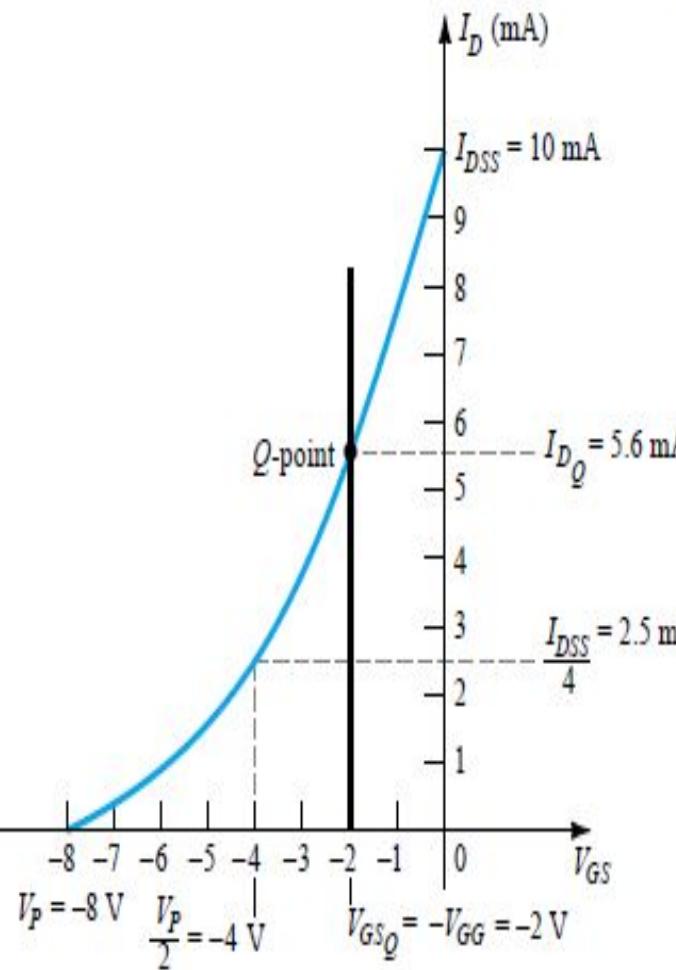
$$(d) V_D = V_{DS} = 4.75 \text{ V}$$

$$(e) V_G = V_{GS} = -2 \text{ V}$$

$$(f) V_S = 0 \text{ V}$$

GRAPHICAL APPROACH

The resulting Shockley curve and the vertical line at $V_{GS} = -2$ V are provided in Fig. 6.7. It is certainly difficult to read beyond the second place without significantly in-



creasing the size of the figure, but a solution of 5.6 mA from the graph of Fig. 6.7 is quite acceptable. Therefore, for part (a),

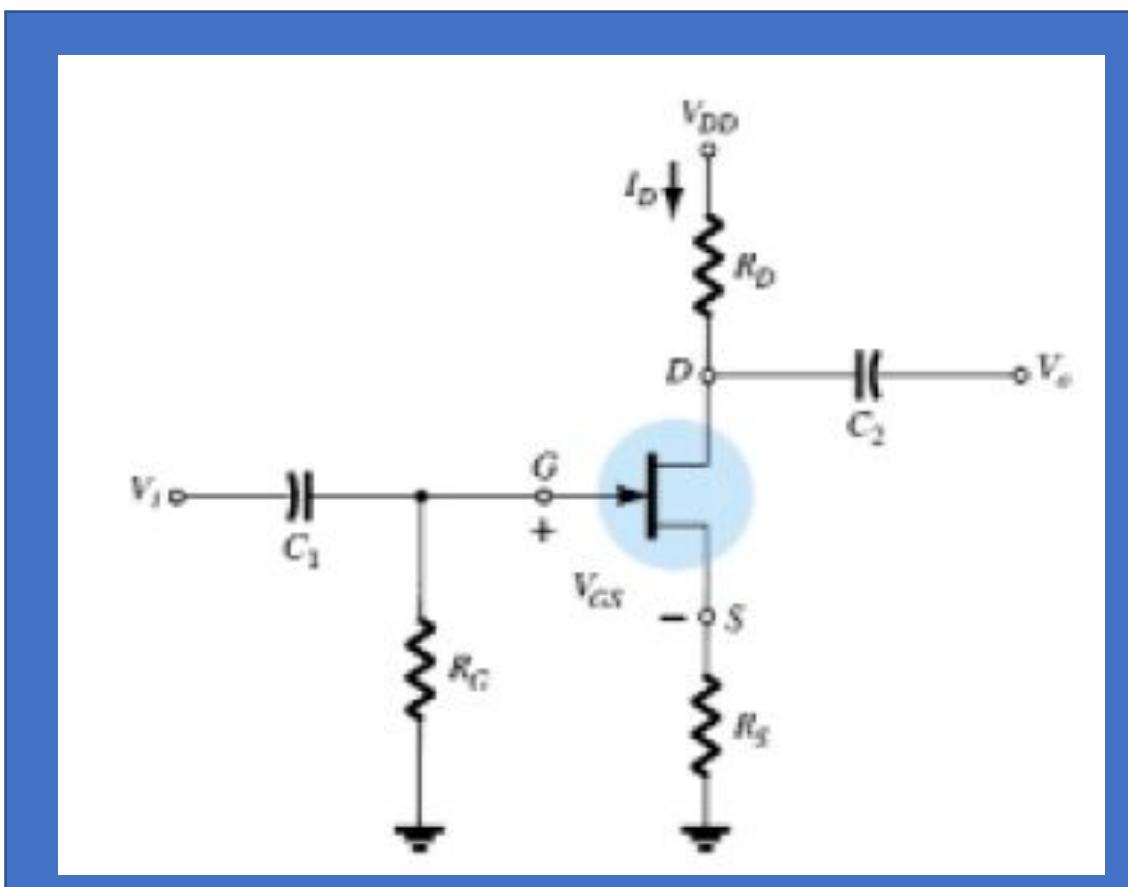
$$V_{GSQ} = -V_{GG} = -2 \text{ V}$$

- (b) $I_{DQ} = 5.6 \text{ mA}$
- (c) $V_{DS} = V_{DD} - I_D R_D = 16 \text{ V} - (5.6 \text{ mA})(2 \text{ k}\Omega)$
 $= 16 \text{ V} - 11.2 \text{ V} = 4.8 \text{ V}$
- (d) $V_D = V_{DS} = 4.8 \text{ V}$
- (e) $V_G = V_{GS} = -2 \text{ V}$
- (f) $V_S = 0 \text{ V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

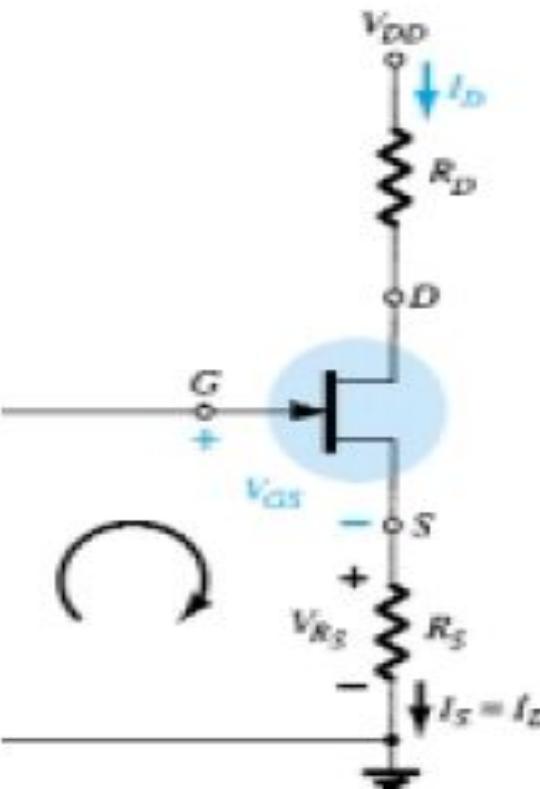
SELF BIAS CONFIGURATION

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in Fig.



DC ANALYSIS OF SELF BIAS

For the dc analysis, the capacitors can again be replaced by “open circuits” and the resistor R_G replaced by a short-circuit equivalent since $I_G = 0$ A.



DC analysis of the self-bias configuration.

The current through R_S is the source current I_S , but $I_S = I_D$ and

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of Fig. 6.9, we find that

$$-V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = -V_{R_S}$$

or

$$V_{GS} = -I_D R_S$$

Note in this case that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.

MATHEMATICAL APPROACH OF SELF BIAS

A mathematical solution could be obtained simply by substituting Eq. into Shockley's equation as shown below:

$$\begin{aligned}I_D &= I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \\&= I_{DSS} \left(1 - \frac{-I_D R_S}{V_P}\right)^2 \\&\text{or} \\I_D &= I_{DSS} \left(1 + \frac{I_D R_S}{V_P}\right)^2\end{aligned}$$

By performing the squaring process indicated and rearranging terms, an equation of the following form can be obtained:

$$I_D^2 + K_1 I_D + K_2 = 0$$

The quadratic equation can then be solved for the appropriate solution for I_D .

GRAPHICAL APPROACH

The graphical approach requires that we first establish the device transfer characteristics as shown in Fig. 6.10. Since Eq. (6.10) defines a straight line on the same graph,

Find two points on the graph

$$I_D = 0 \text{ A}$$

$$V_{GS} = -I_D R_S = (0 \text{ A})R_S = 0 \text{ V.}$$

$$I_D = \frac{I_{DSS}}{2}$$

$$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

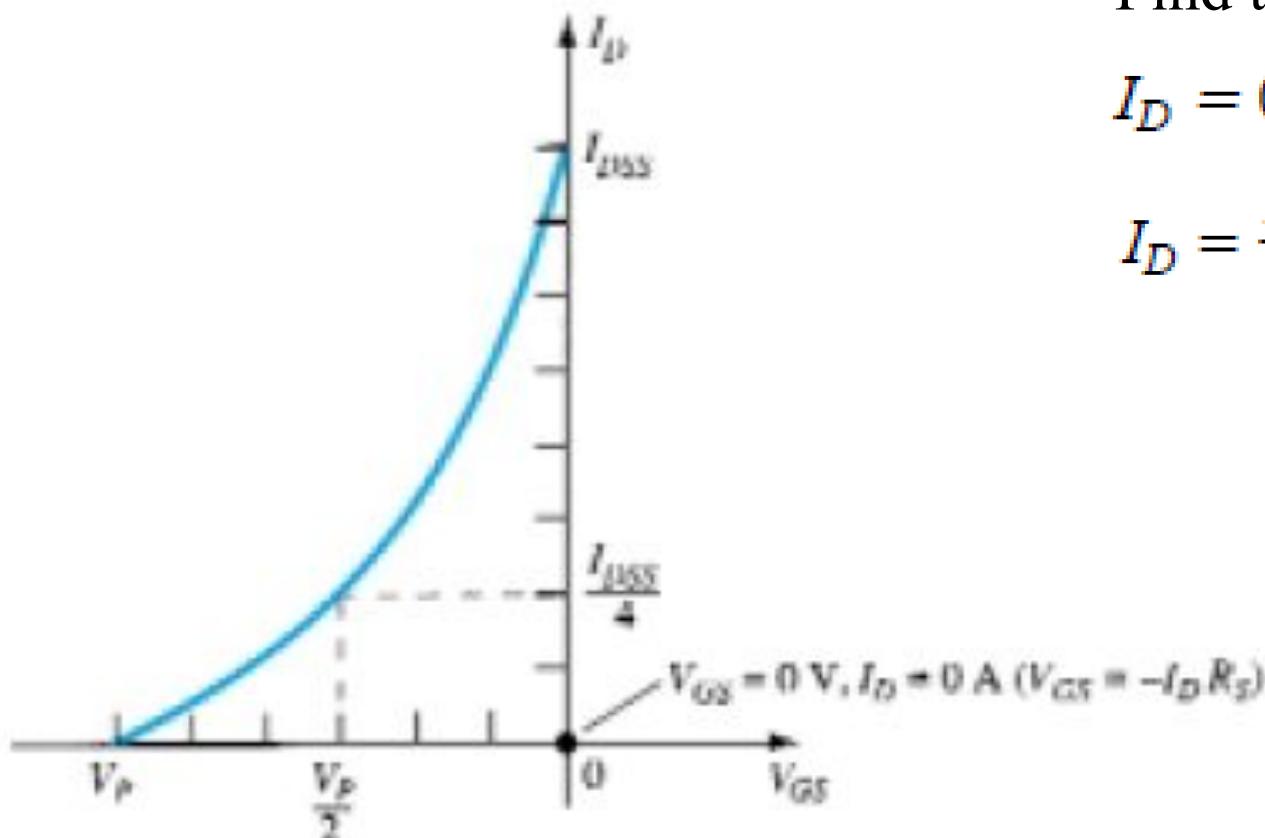
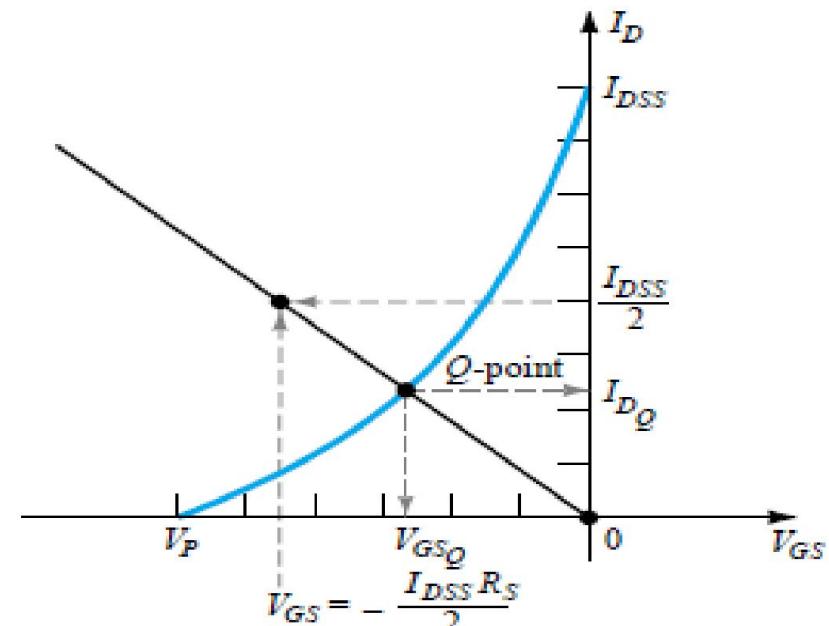


Figure 6.10 Defining a point on the self-bias line.



DC ANALYSIS OF SELF BIAS

The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

but

$$I_D = I_S$$

and

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

In addition:

$$V_S = I_D R_S$$

$$V_G = 0 \text{ V}$$

and

$$V_D = V_{DS} + V_S = V_{DD} - V_{R_D}$$

REFLECTION SPOT



testmoz.com/4954046

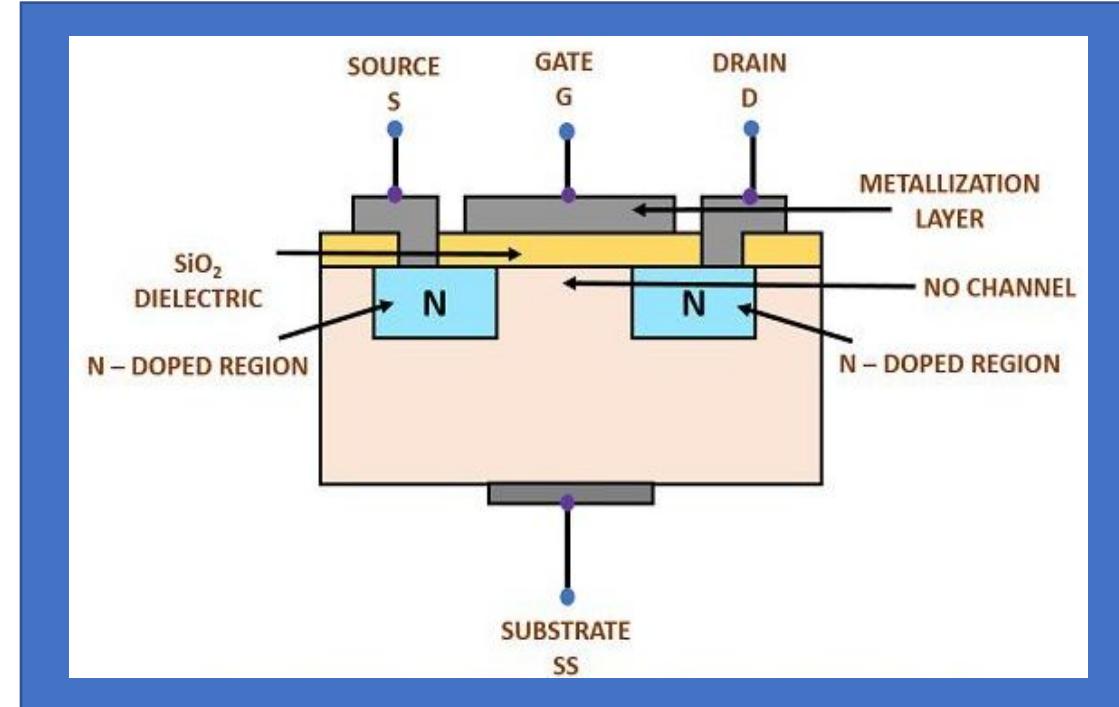
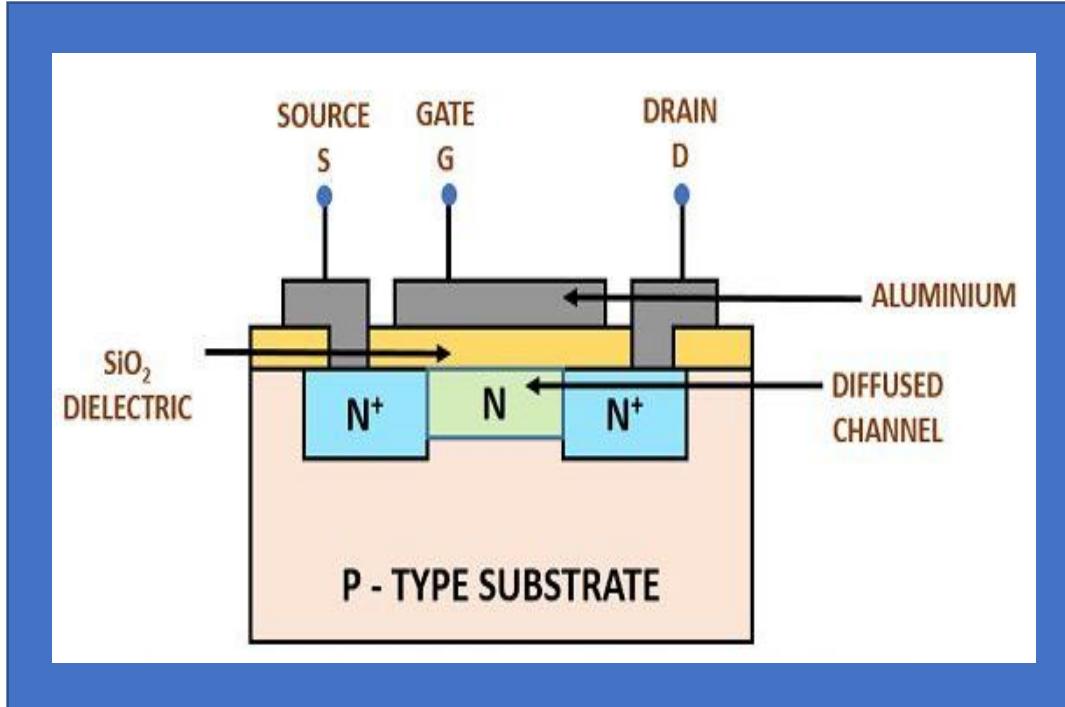
<https://www.youtube.com/watch?v=uea-BxQR71A>

https://www.youtube.com/watch?v=lEy5_reYj2Y

METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS (MOSFET)



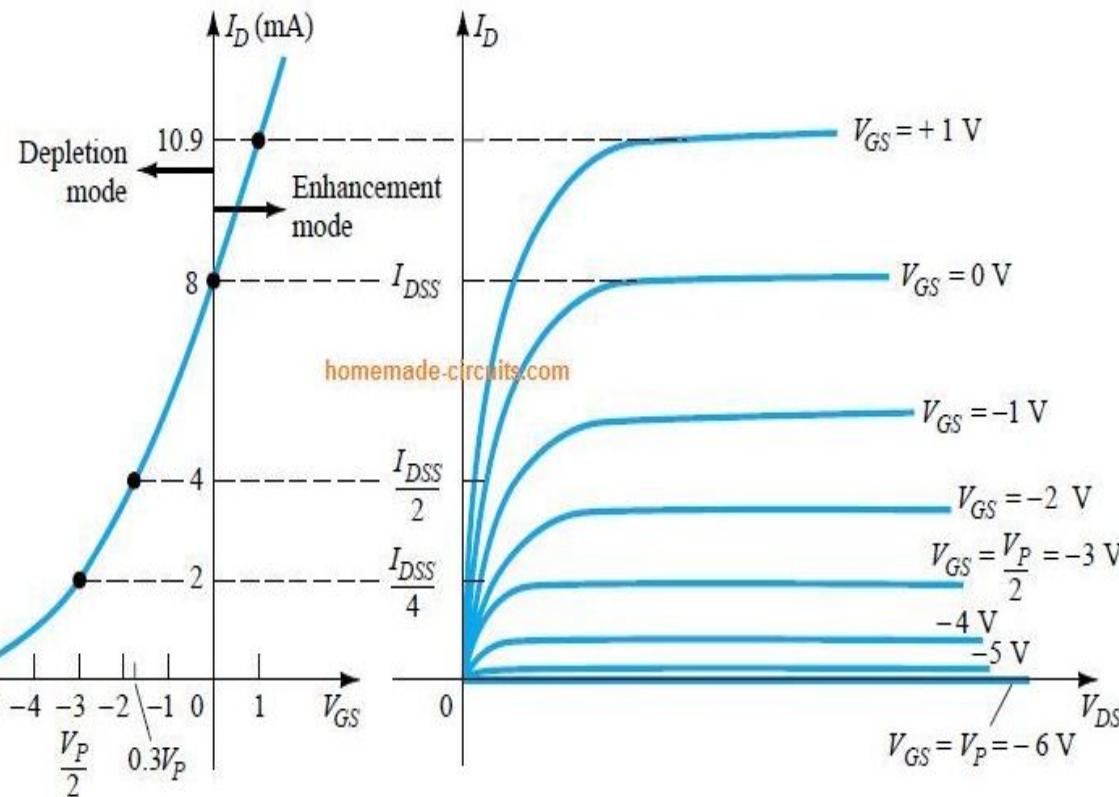
MOSFET



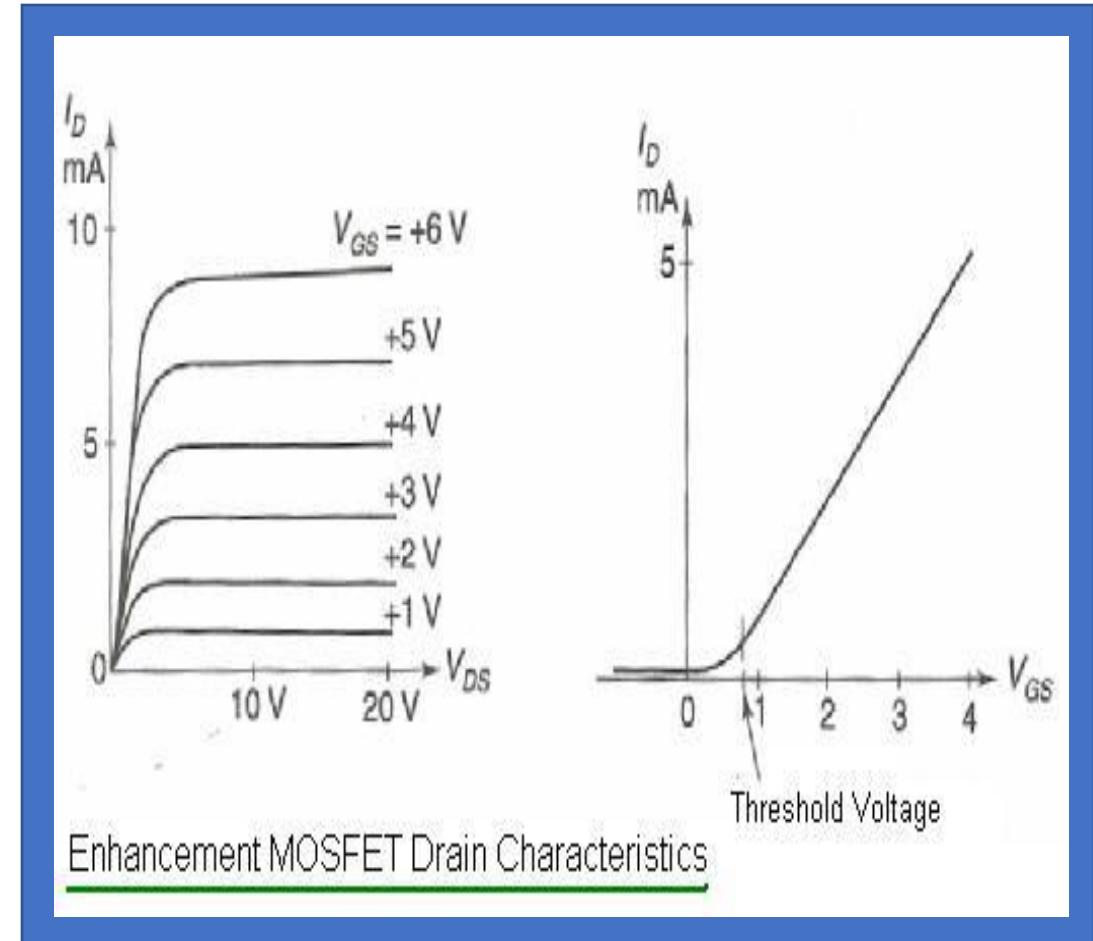
D-MOSFET – requires the Gate-Source voltage, (V_{GS}) to switch the device “OFF”. The depletion mode MOSFET is equivalent to a “**Normally Closed**” switch.

E-MOSFET – requires a Gate-Source voltage, (V_{GS}) to switch the device “ON”. The enhancement mode MOSFET is equivalent to a “**Normally Open**” switch.

DRAIN AND TRANSFER CHARACTERISTICS OF D-MOSFET AND E-MOSFET



Depletion MOSFET



Enhancement MOSFET

IMPORTANT EQUATIONS

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2$$

JFET/D-MOSFET transfer characteristic

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)$$

Transconductance

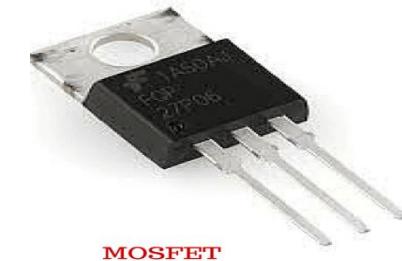
$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(\text{off})}|}$$

Transconductance at $V_{GS} = 0$

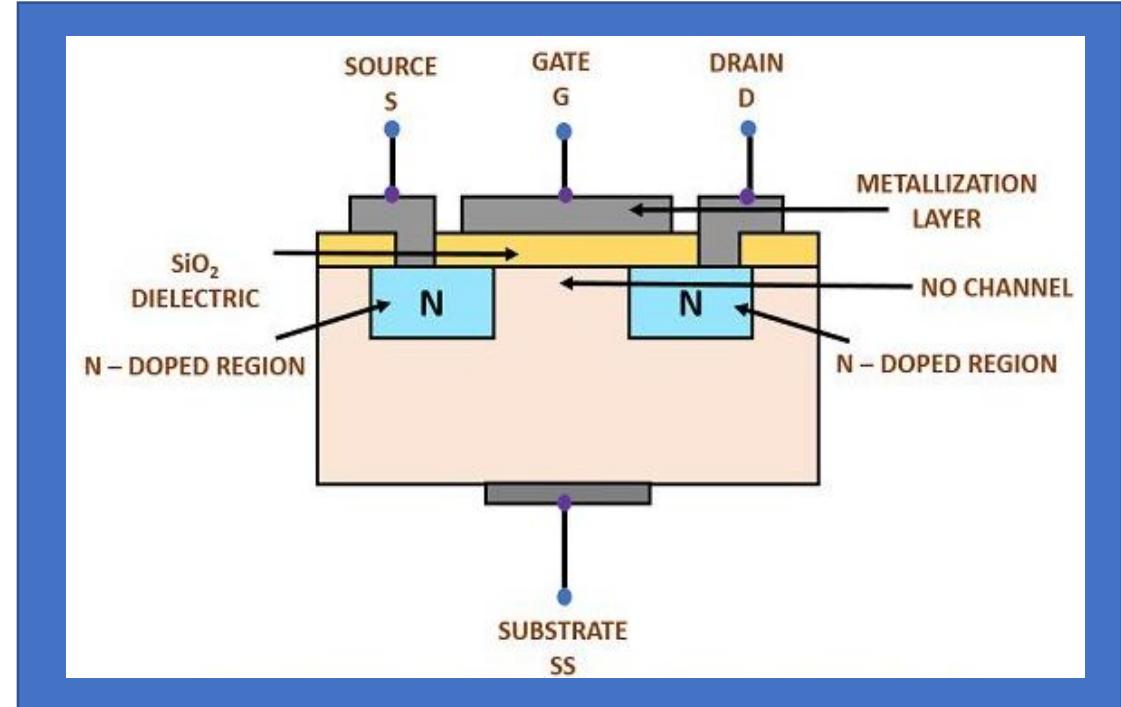
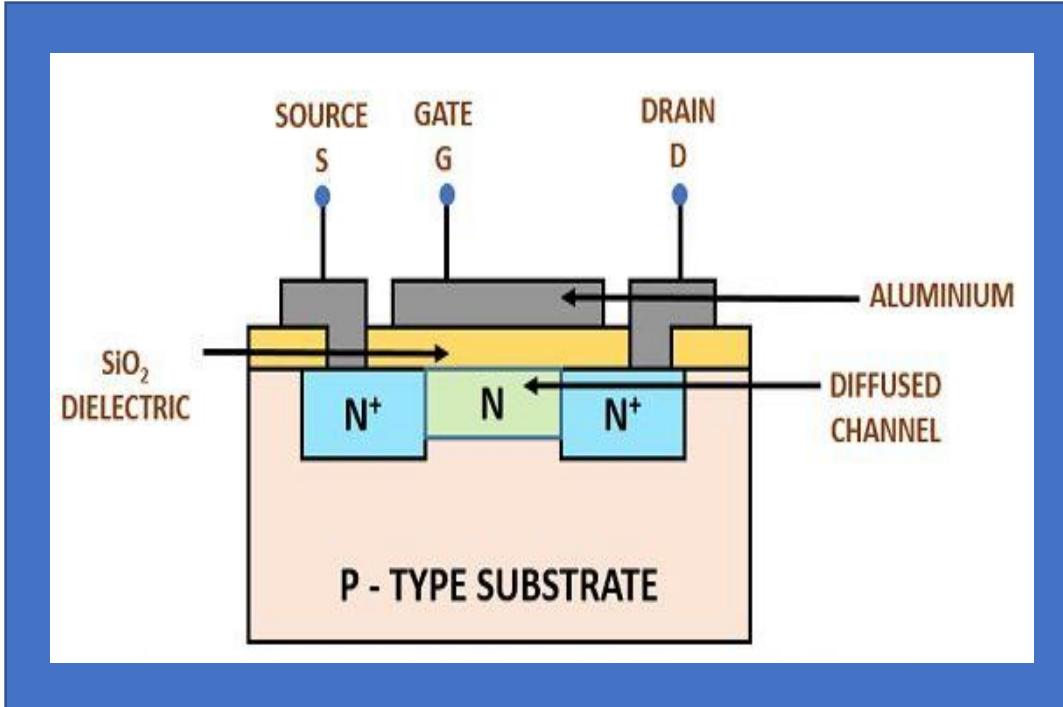
$$I_D = K(V_{GS} - V_{GS(\text{th})})^2$$

E-MOSFET transfer characteristic

METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS (MOSFET)



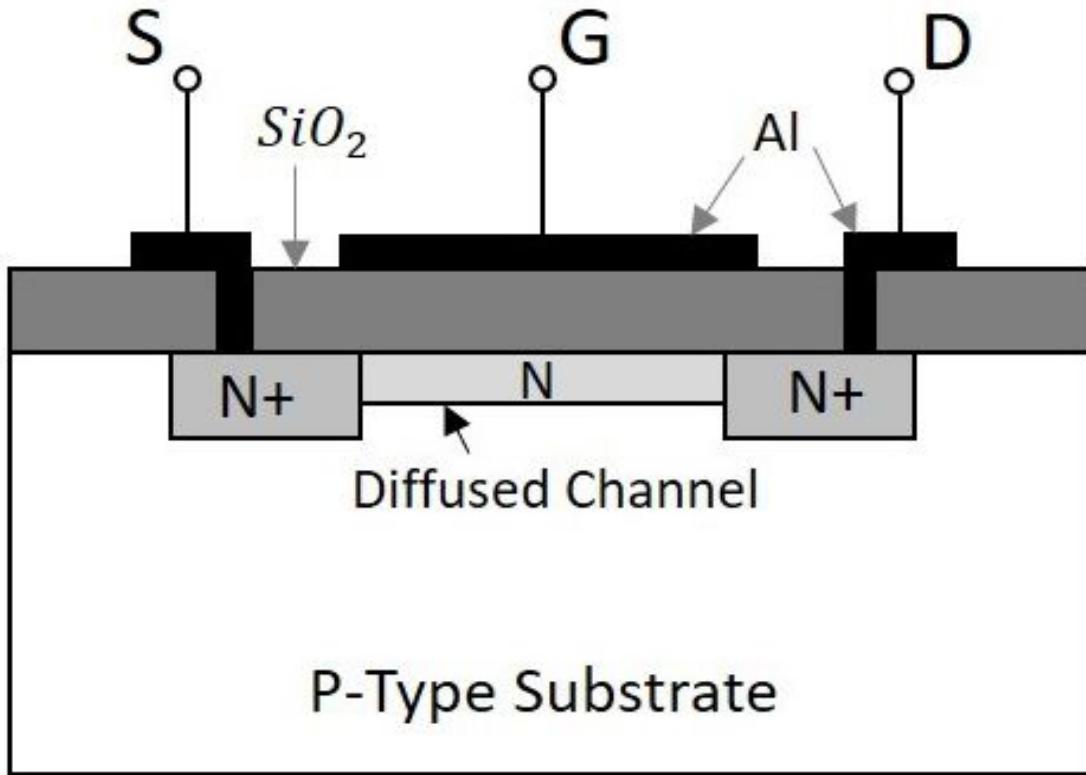
MOSFET



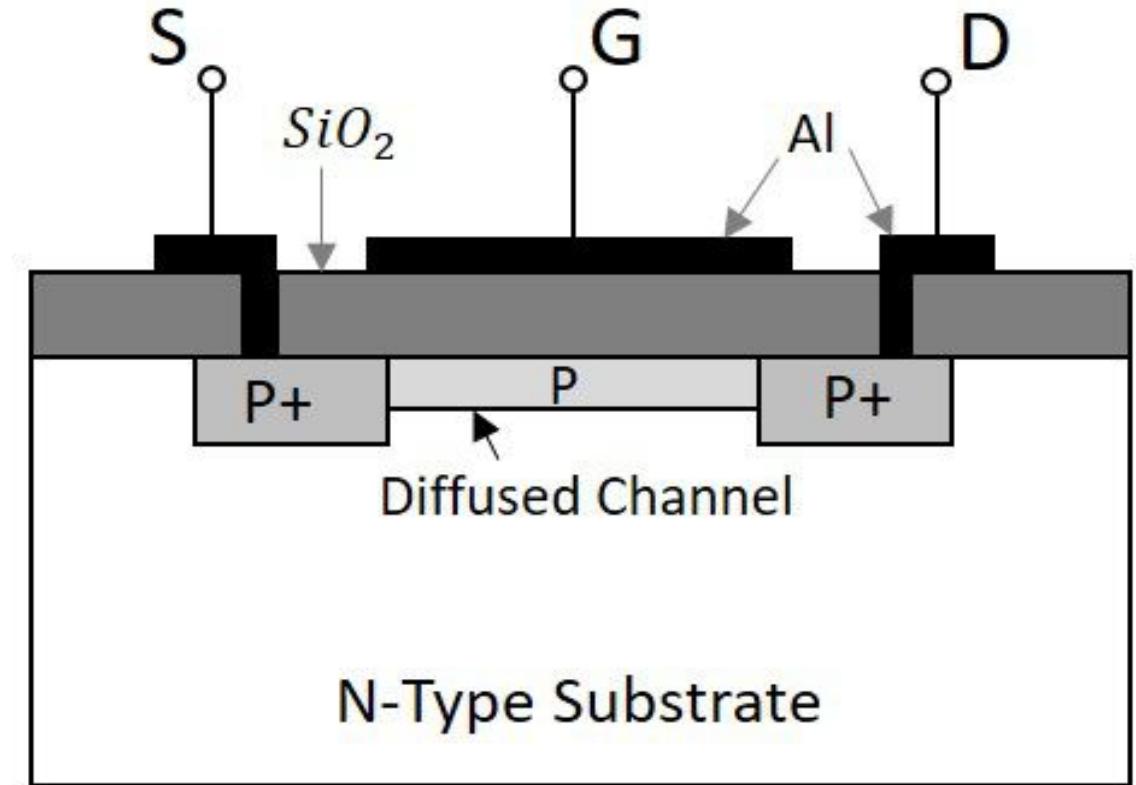
D-MOSFET – requires the Gate-Source voltage, (V_{GS}) to switch the device “OFF”. The depletion mode MOSFET is equivalent to a “**Normally Closed**” switch.

E-MOSFET – requires a Gate-Source voltage, (V_{GS}) to switch the device “ON”. The enhancement mode MOSFET is equivalent to a “**Normally Open**” switch.

CONSTRUCTION OF DMOSFET N CHANNEL AND P CHANNEL

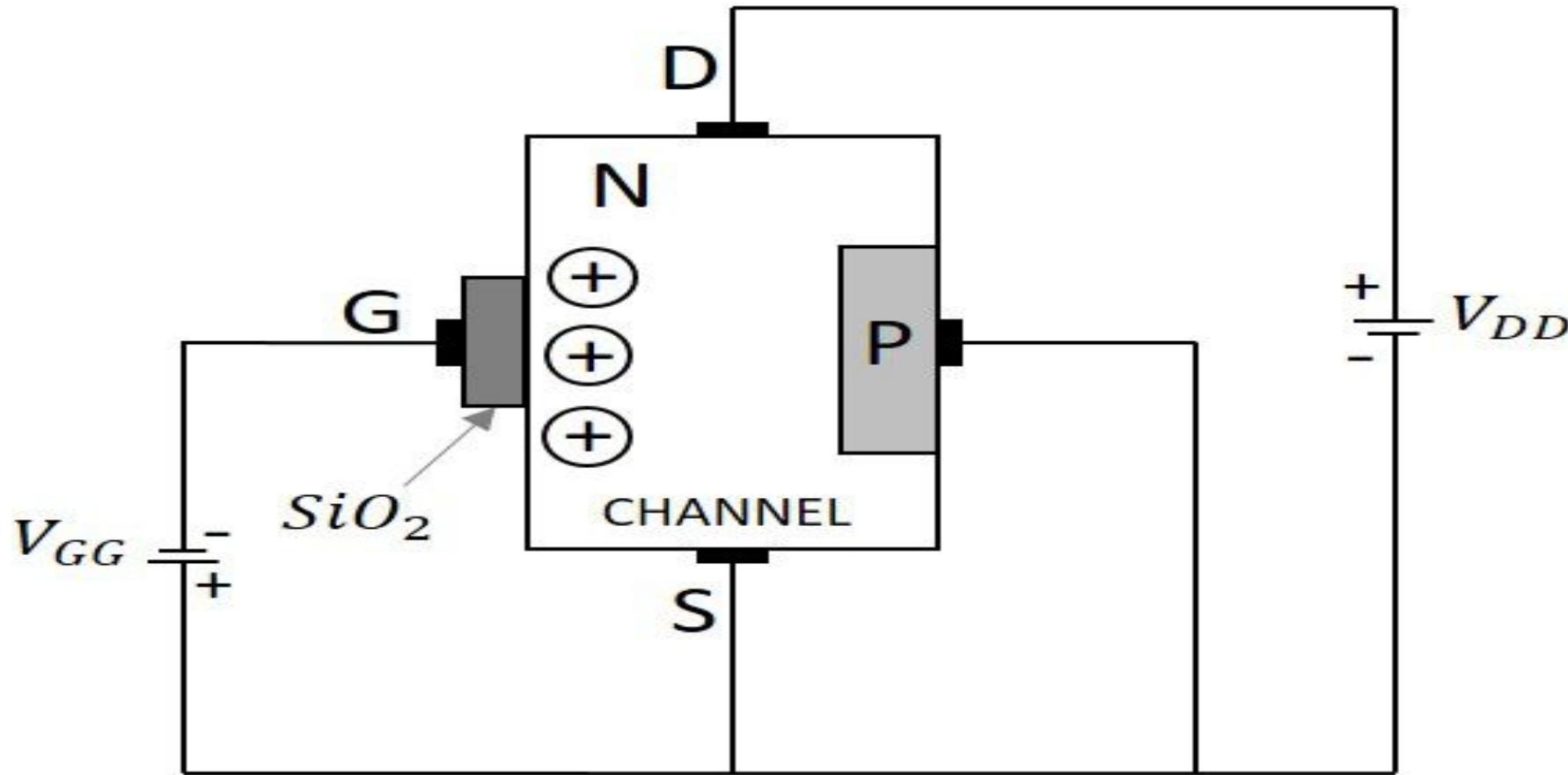


Structure of N-channel MOSFET



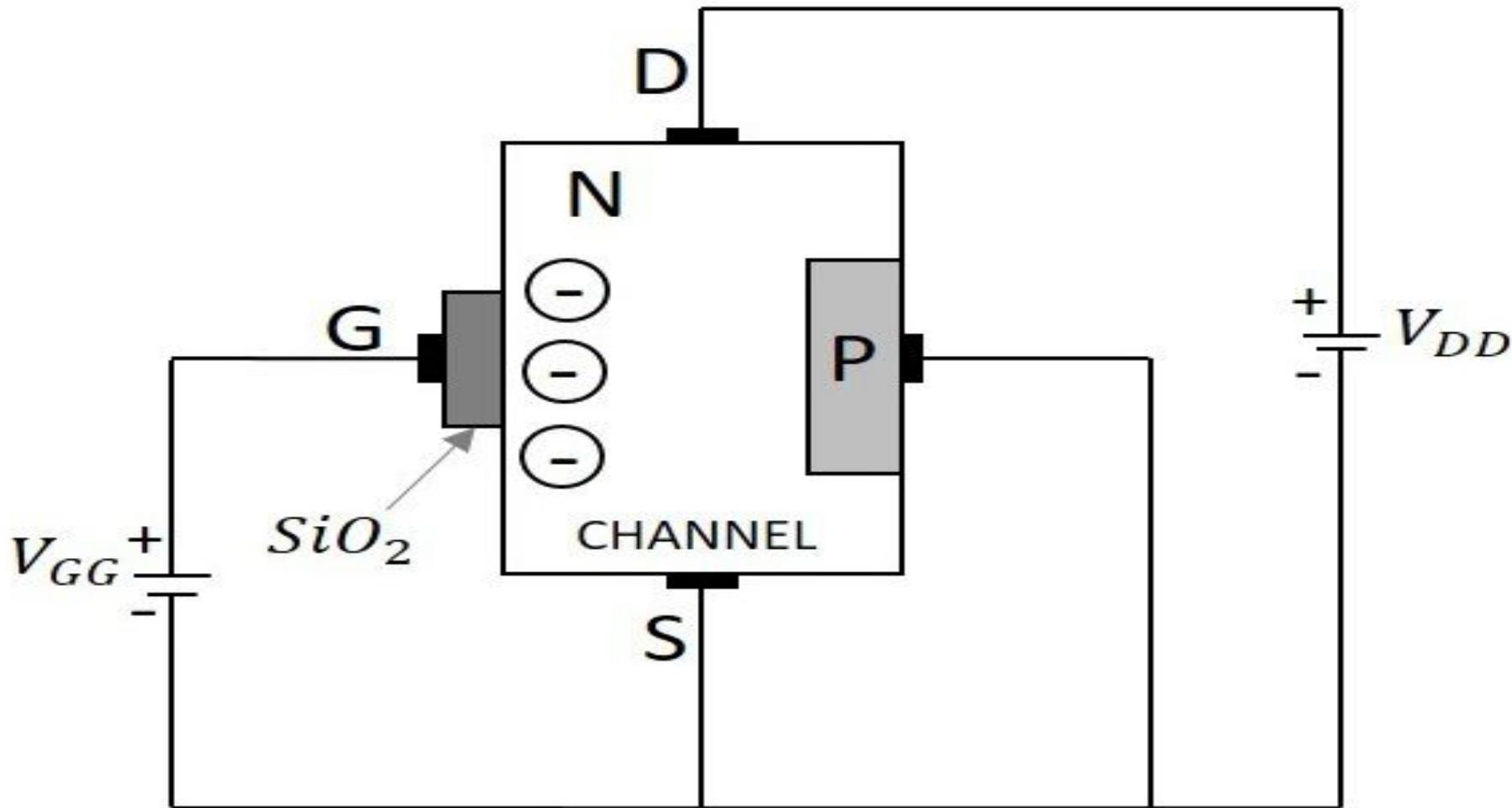
Structure of P-channel MOSFET

WORKING OF N CHANNEL DMOSFET



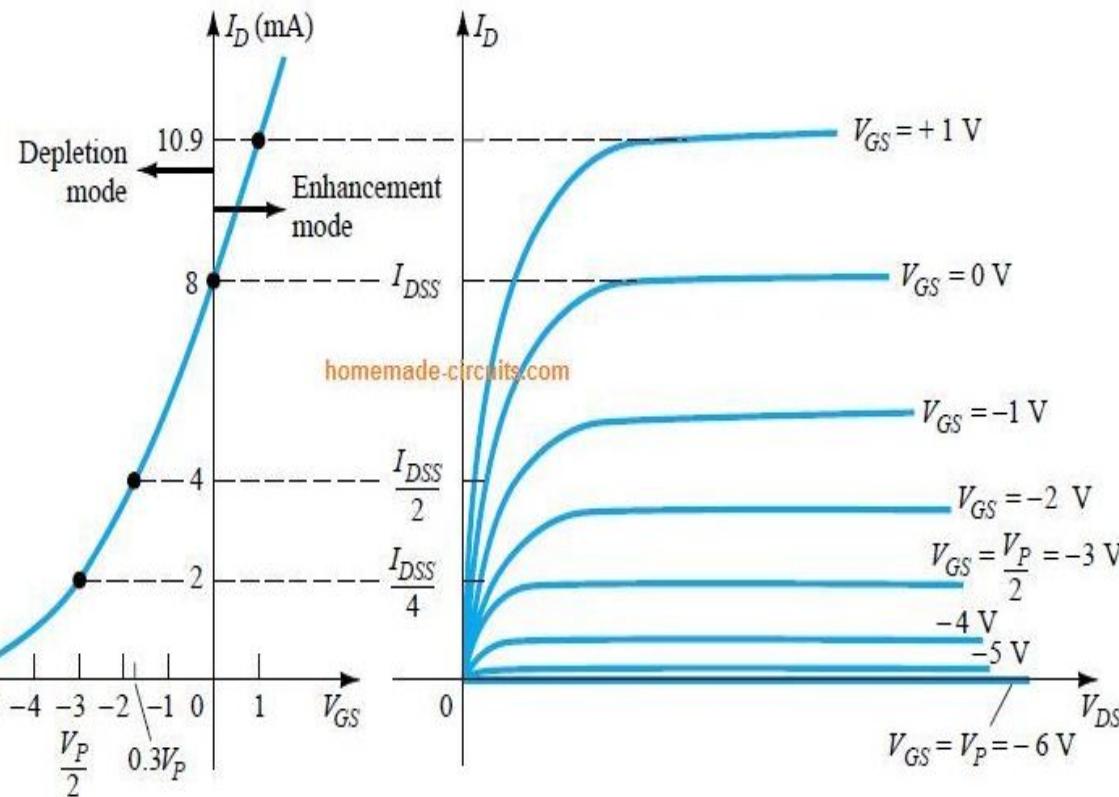
Working of MOSFET in depletion mode

WORKING OF EMOSFET

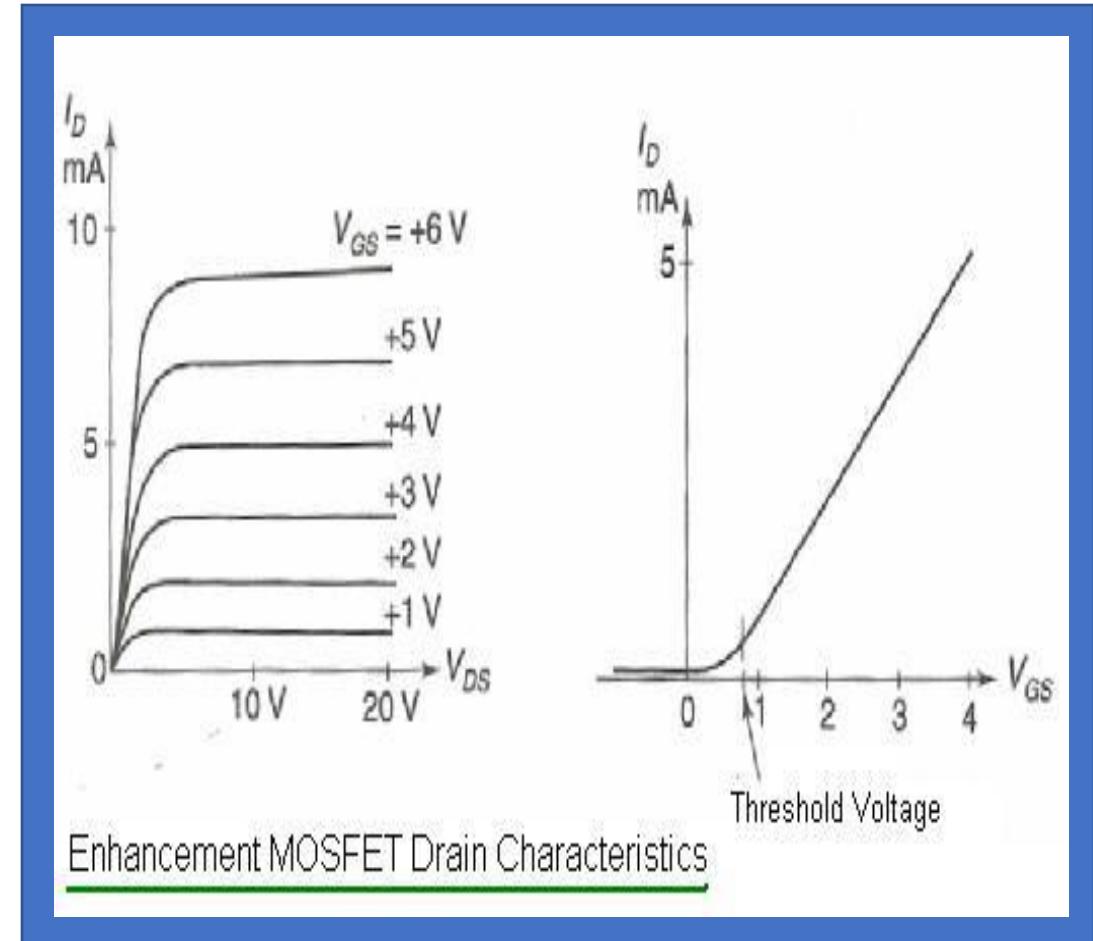


Working of MOSFET in Enhancement mode

DRAIN AND TRANSFER CHARACTERISTICS OF D-MOSFET AND E-MOSFET



Depletion MOSFET



Enhancement MOSFET

IMPORTANT EQUATIONS

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2$$

JFET/D-MOSFET transfer characteristic

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)$$

Transconductance

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(\text{off})}|}$$

Transconductance at $V_{GS} = 0$

$$I_D = K(V_{GS} - V_{GS(\text{th})})^2$$

E-MOSFET transfer characteristic

COMPARISON BETWEEN BJT, FET AND MOSFET

TERMS	BJT	FET	MOSFET
Device type	Current controlled	Voltage controlled	Voltage Controlled
Current flow	Bipolar	Unipolar	Unipolar
Terminals	Not interchangeable	Interchangeable	Interchangeable
Operational modes	No modes	Depletion mode only	Both Enhancement and Depletion modes
Input impedance	Low	High	Very high
Output resistance	Moderate	Moderate	Low
Operational speed	Low	Moderate	High
Noise	High	Low	Low
Thermal stability	Low	Better	High

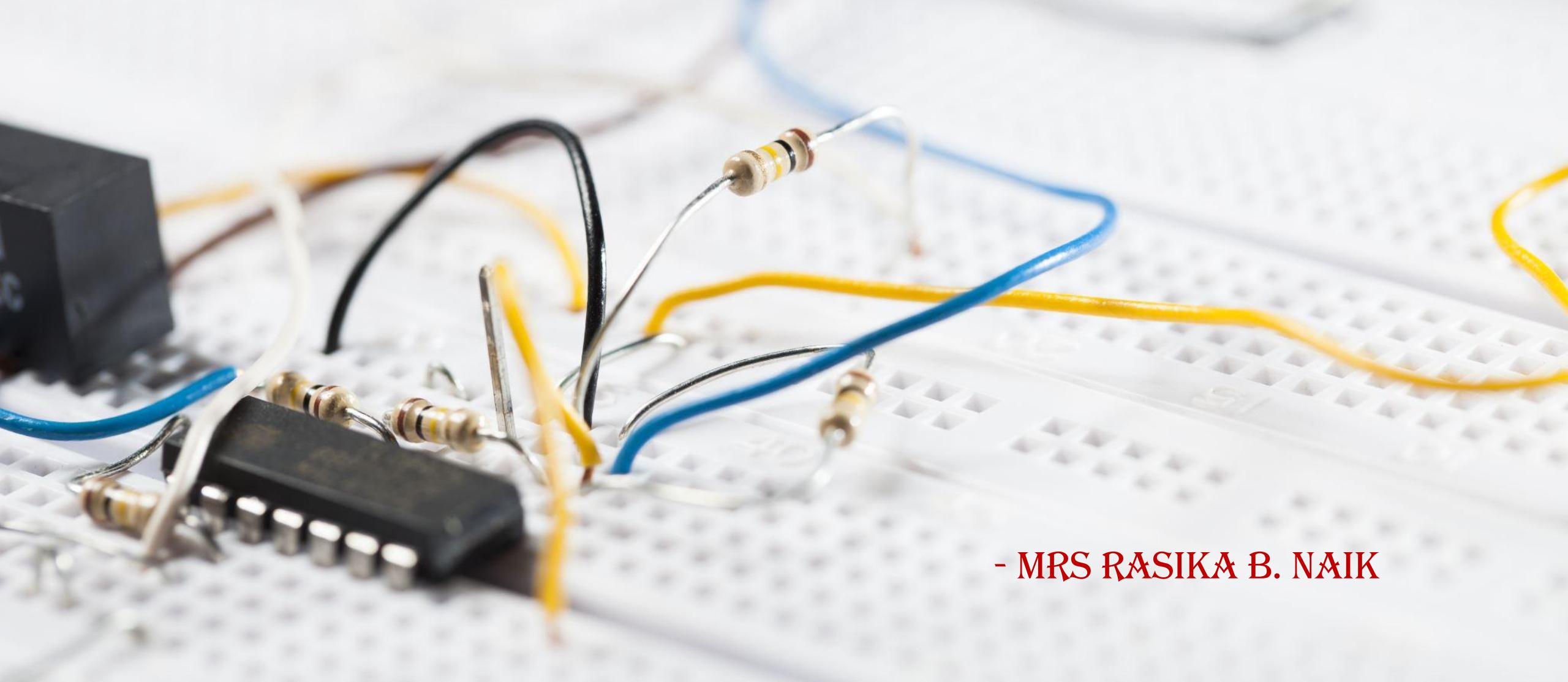
<https://www.youtube.com/watch?v=stM8dgcY1CA>



testmoz.com/5056314

CHAPTER 2

BIASING CIRCUITS OF BJTS AND MOSFETS



- MRS RASIIKA B. NAIK

INTRODUCTION – BIASING

- The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system.
- The amplifier increases the strength of a weak signal by transferring the energy from the applied DC source to the weak input ac signal.
- The analysis or design of any electronic amplifier therefore has two components:
 - The dc portion and
 - The ac portion
- During the design stage, the choice of parameters for the required dc levels will affect the ac response.

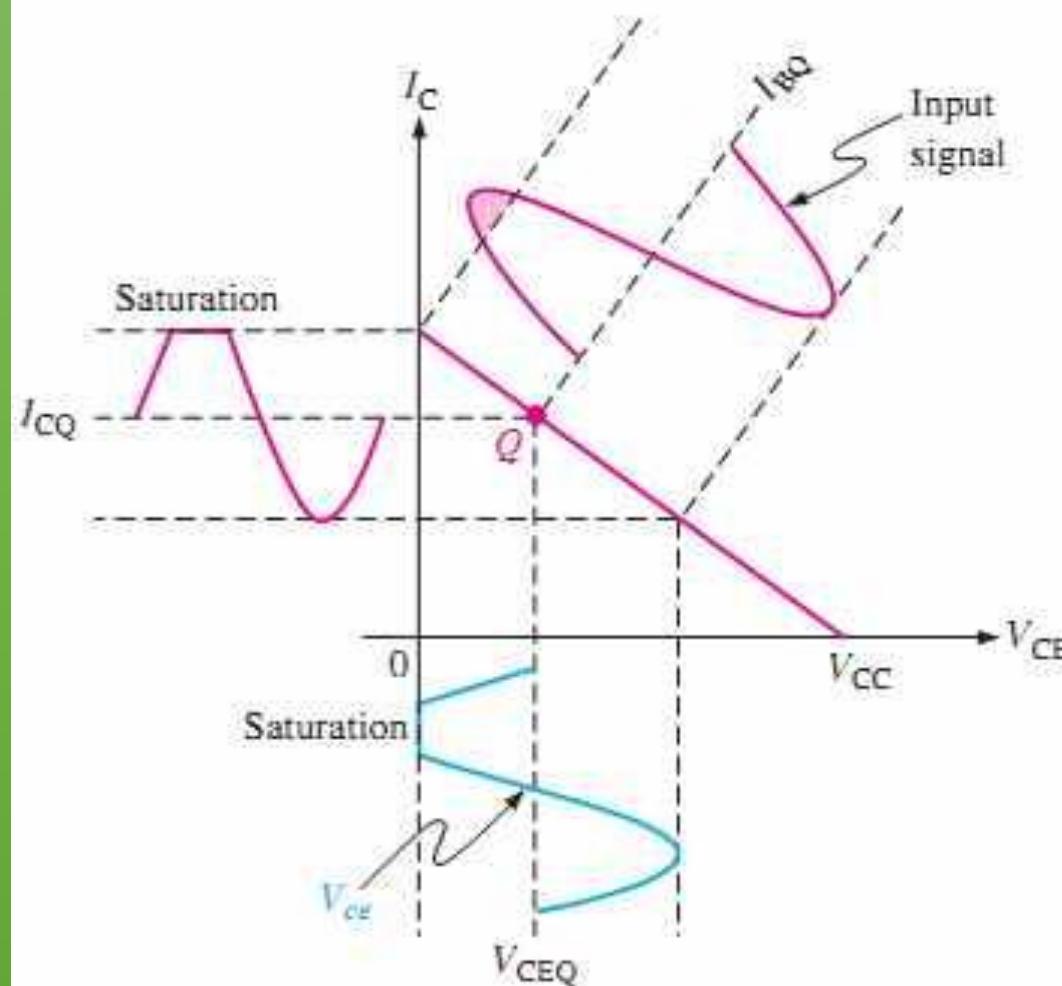
BIASING

- Application of dc voltages to establish a fixed level of current and voltage is called Biasing.
- A transistor must be properly biased in order to operate as an amplifier.
- DC biasing is used to establish fixed dc values for the transistor currents and voltages called the dc operating point or quiescent point (Q-point).

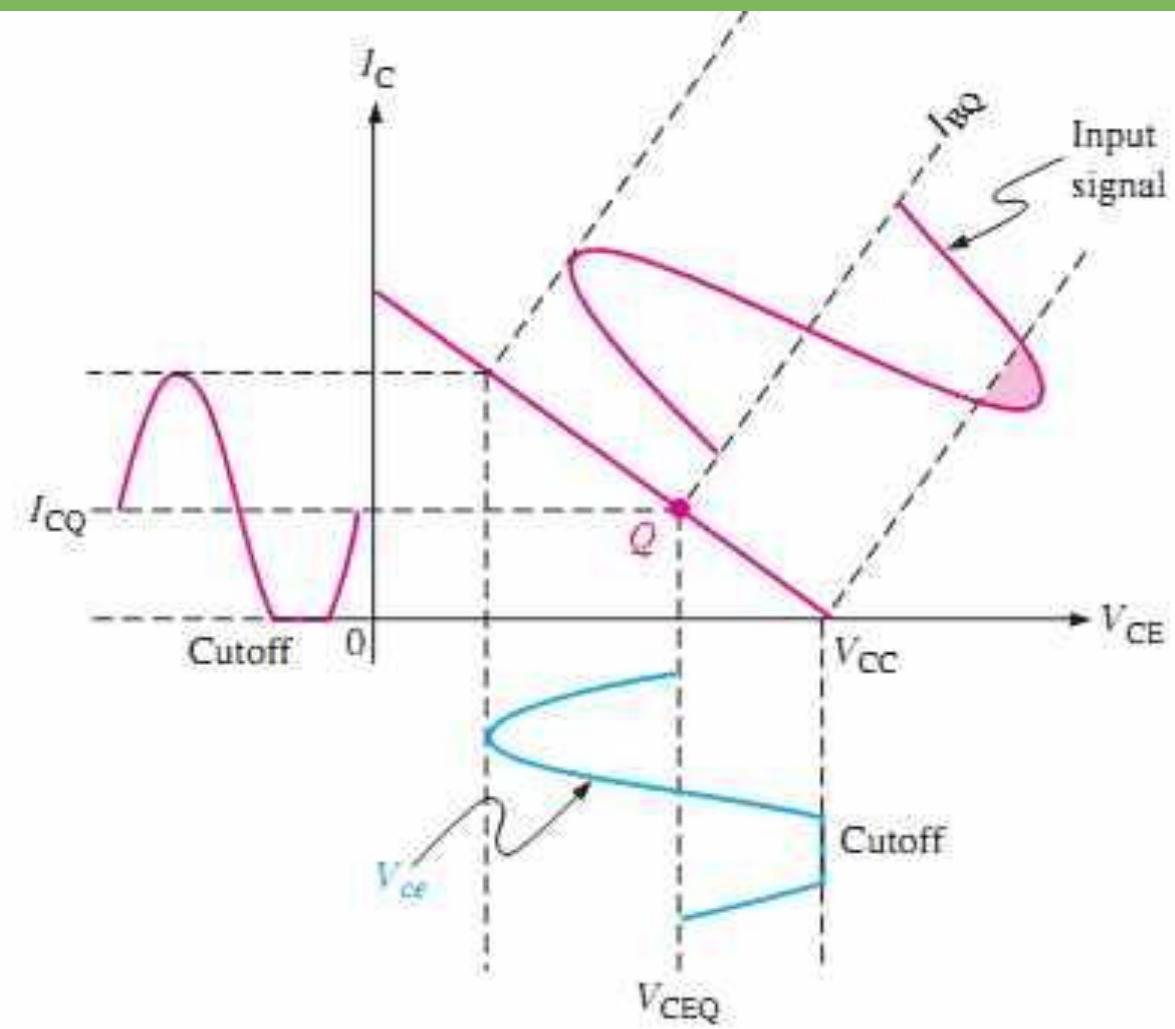
Purpose of the DC biasing circuit

- To turn the device “ON”
- To place it in operation in the region of its characteristic where the device operates most linearly .
- Proper biasing circuit which it operate in linear region and circuit have centered Q-point or midpoint biased
- Improper biasing cause
 - Distortion in the output signal
 - Produce limited or clipped at output signal

EFFECT OF IMPROPER BIASING

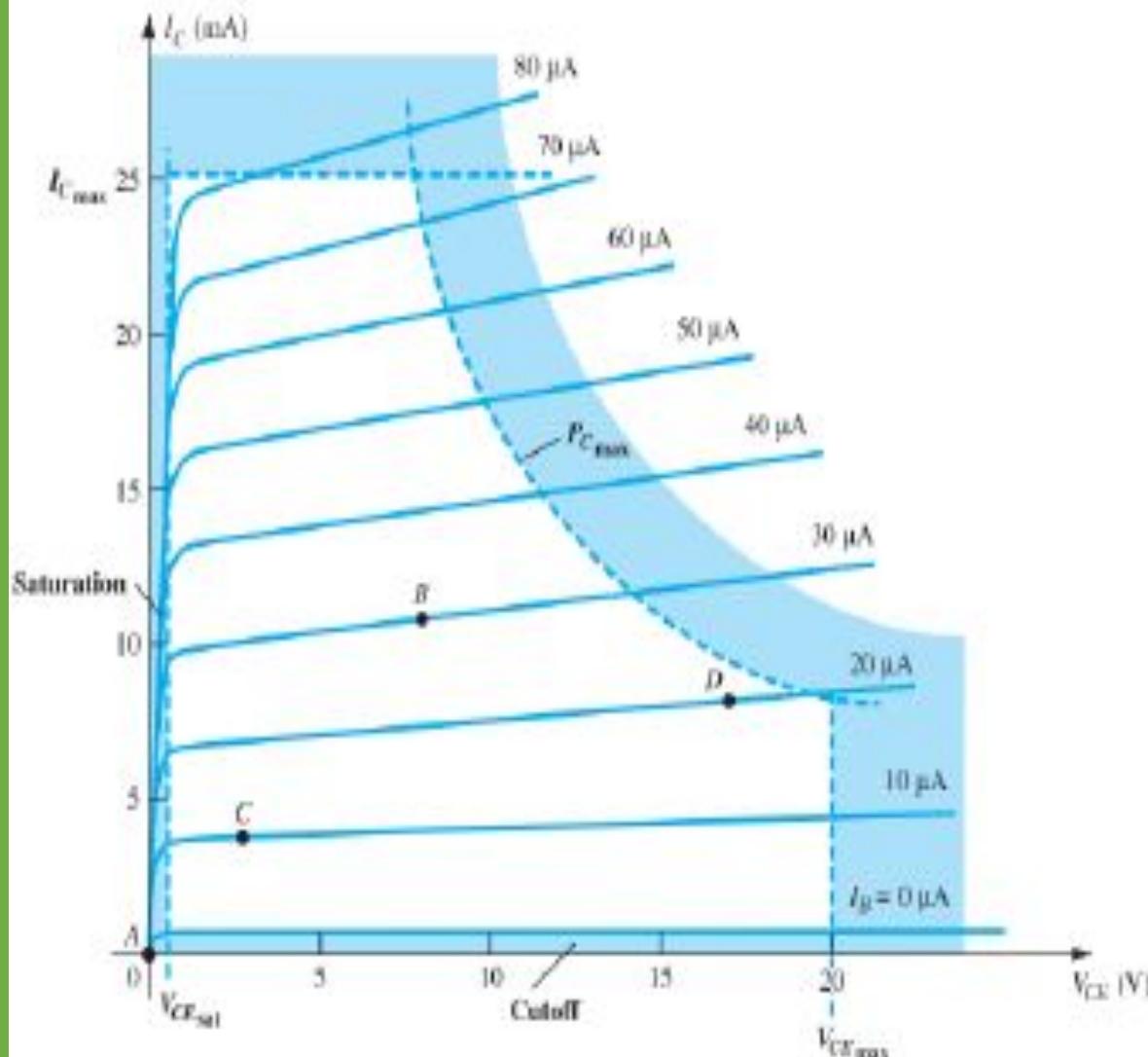


(a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.



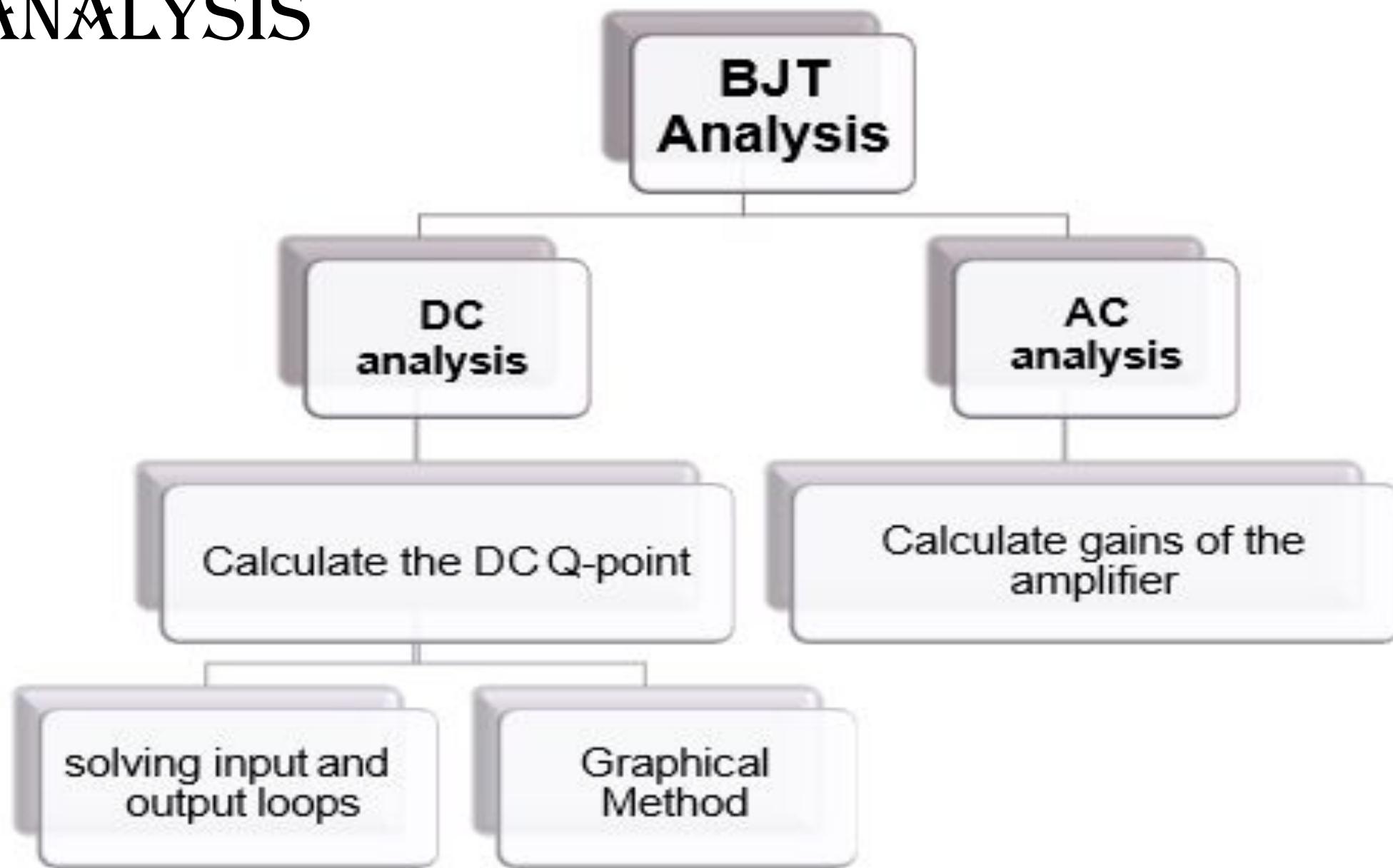
(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.

OPERATING POINT



EMITTER JUNCTION	COLLECTOR JUNCTION	REGION OF OPERATION
Forward biased	Forward biased	Saturation region
Forward biased	Reverse biased	Active region
Reverse biased	Reverse biased	Cut off region

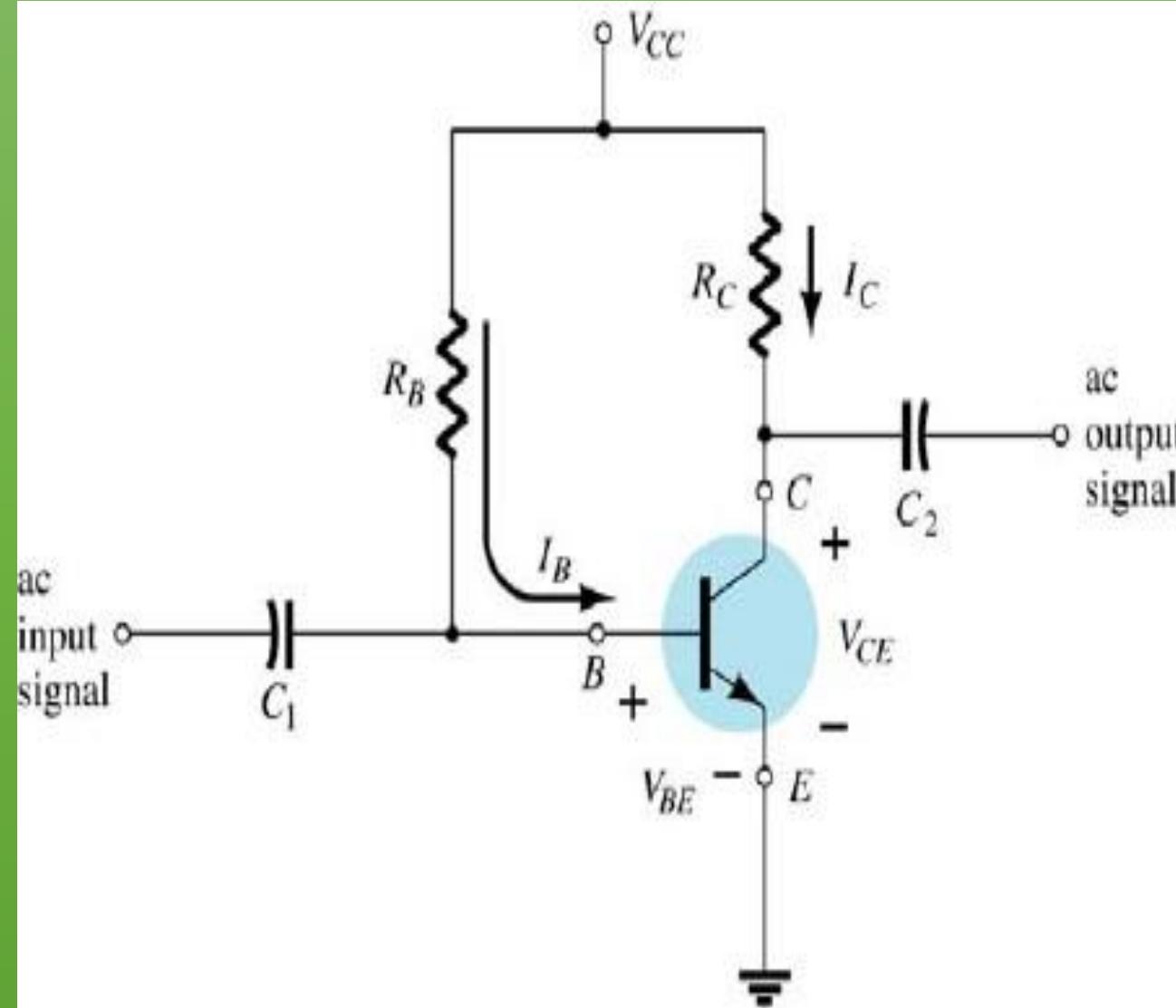
BJT ANALYSIS



DC BIASING CIRCUITS

- Fixed-bias circuit
- Emitter bias circuit
- Voltage divider bias circuit
- Collector to base feedback circuit

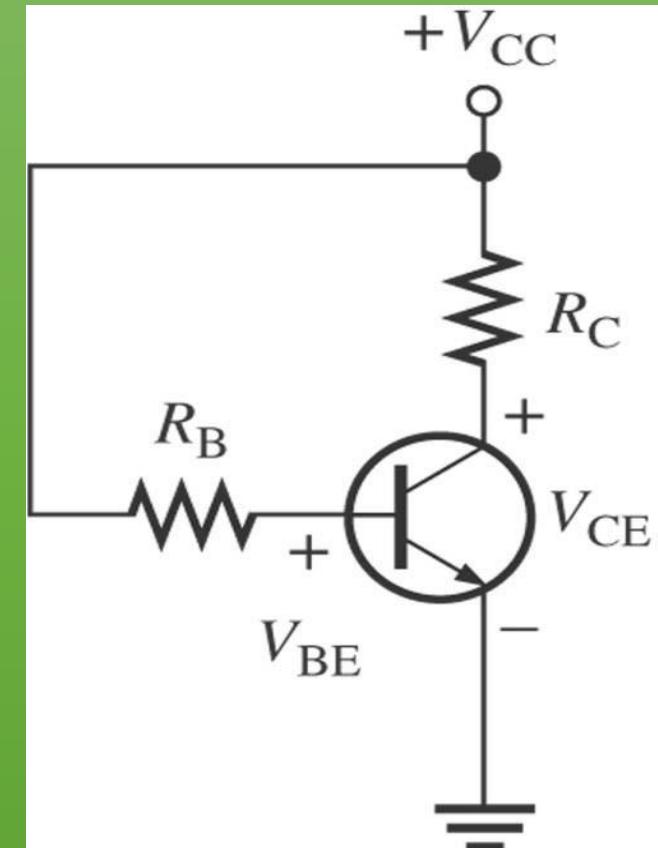
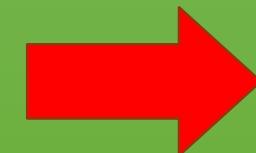
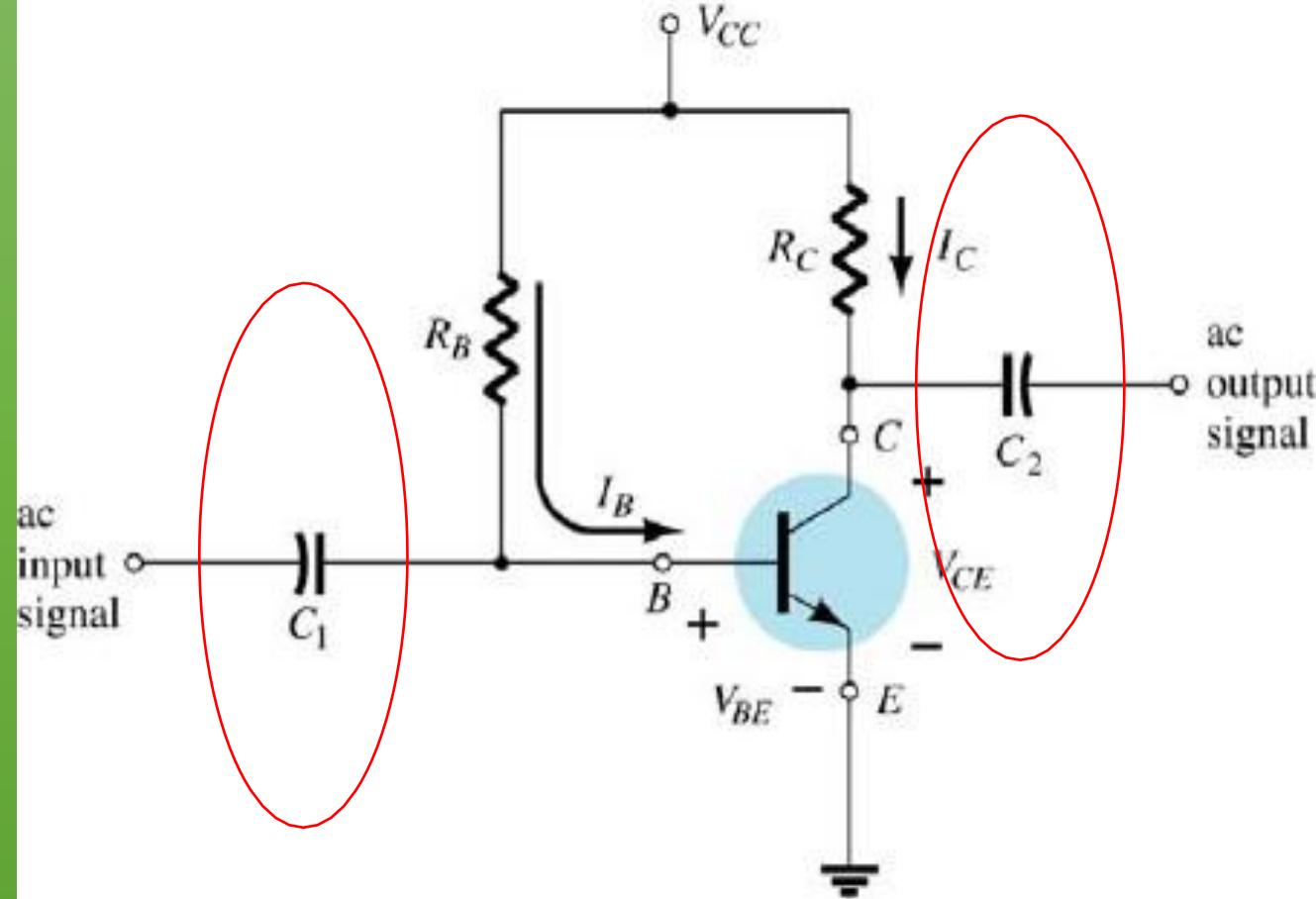
FIXED BIAS CIRCUIT



- ✓ This is common emitter (CE) configuration
- ✓ 1st step: Locate capacitors and replace them with an open circuit
- ✓ 2nd step: Locate 2 main loops which;
 - BE loop (input loop)
 - CE loop(output loop)

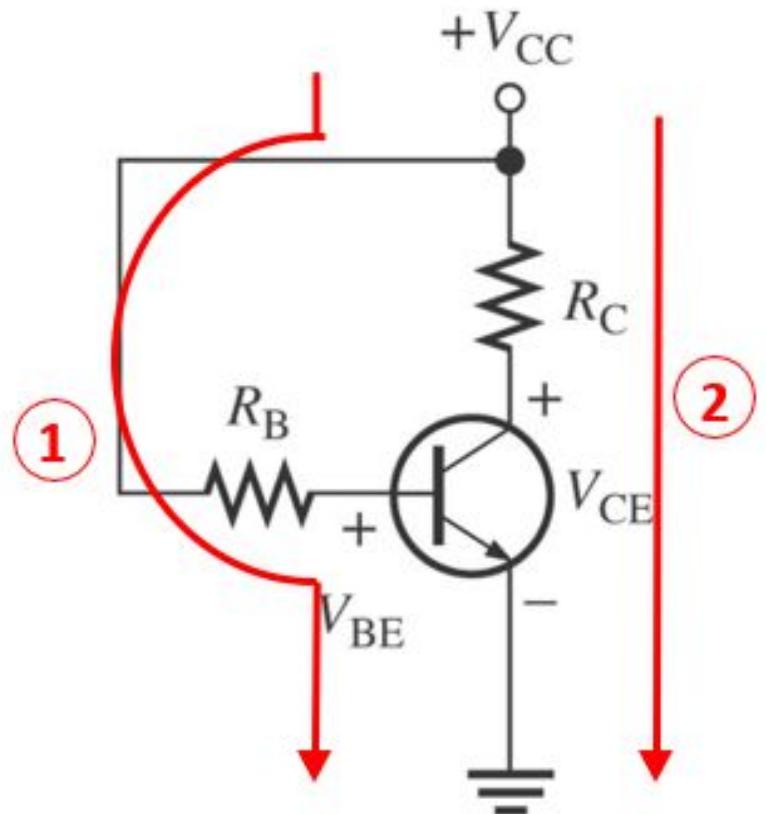
FIXED BIAS CIRCUIT

1st step: Locate capacitors and replace them with an open circuit

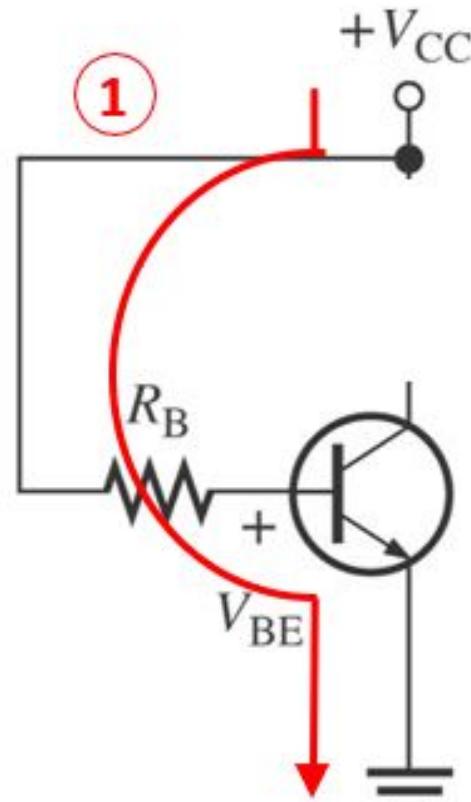


FIXED BIAS CIRCUIT

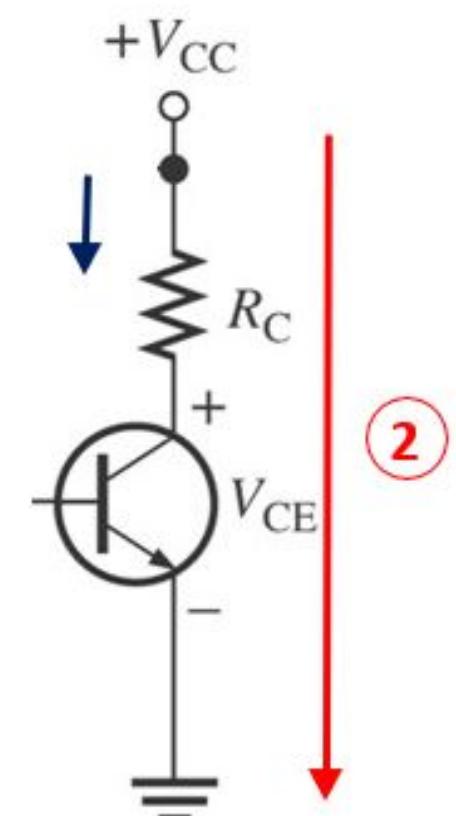
2nd step: Locate 2 main loops



BE Loop

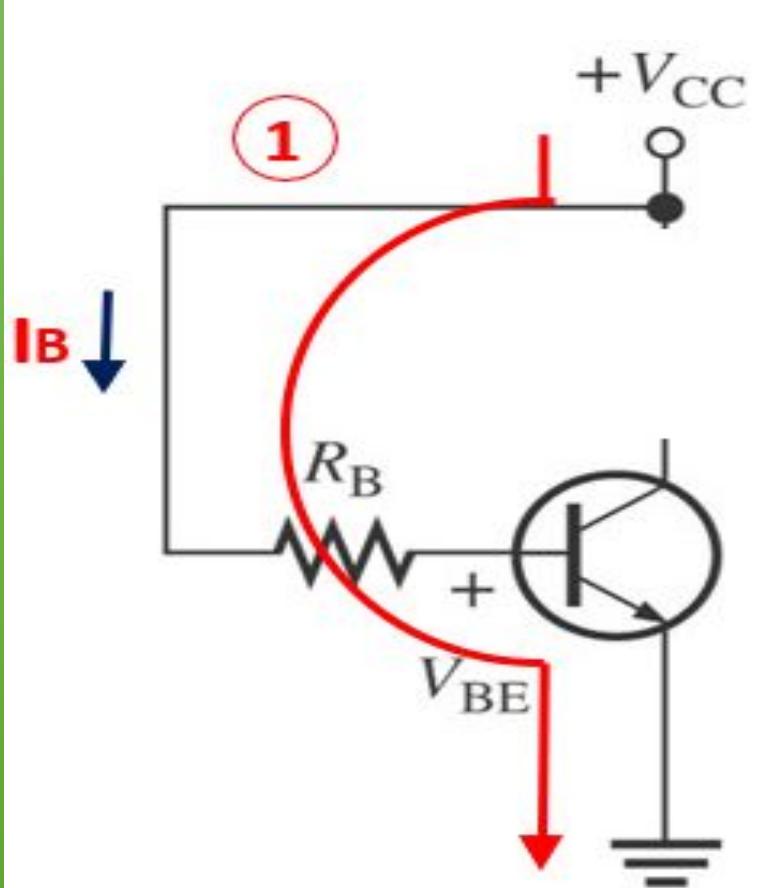


CE Loop



FIXED BIAS CIRCUIT

BE Loop Analysis



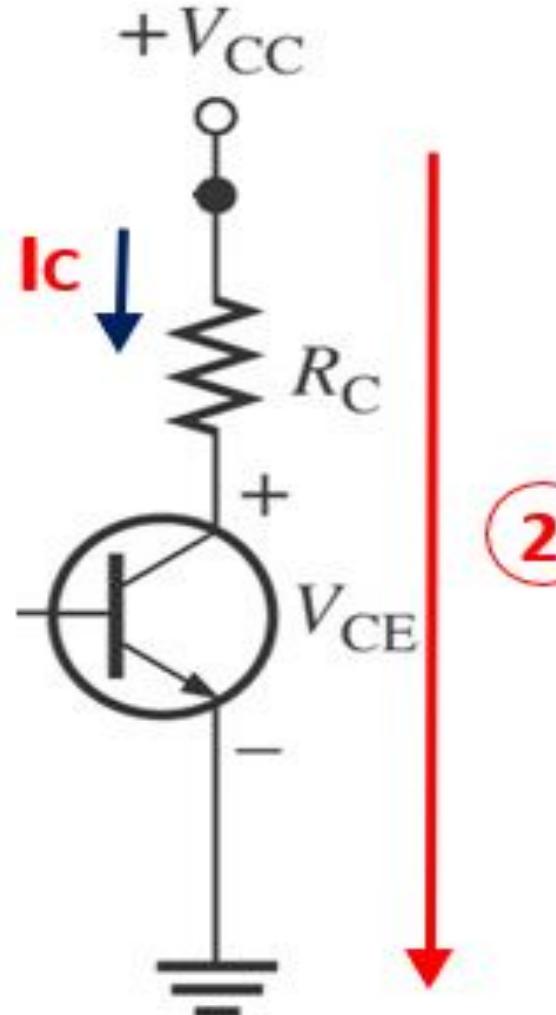
■ From KVL;

$$-V_{CC} + I_B R_B + V_{BE} = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \text{(A)}$$

FIXED BIAS CIRCUIT

CE Loop Analysis



■ From KVL;

$$-V_{CC} + I_C R_C + V_{CE} = 0$$

$$\therefore V_{CE} = V_{CC} - I_C R_C$$

■ As we know;

$$I_C = \beta I_B \quad \textcircled{B}$$

■ Substituting \textcircled{A} with \textcircled{B}

$$I_C = \beta_{DC} \left| \left(\frac{V_{CC} - V_{BE}}{R_B} \right) \right|$$

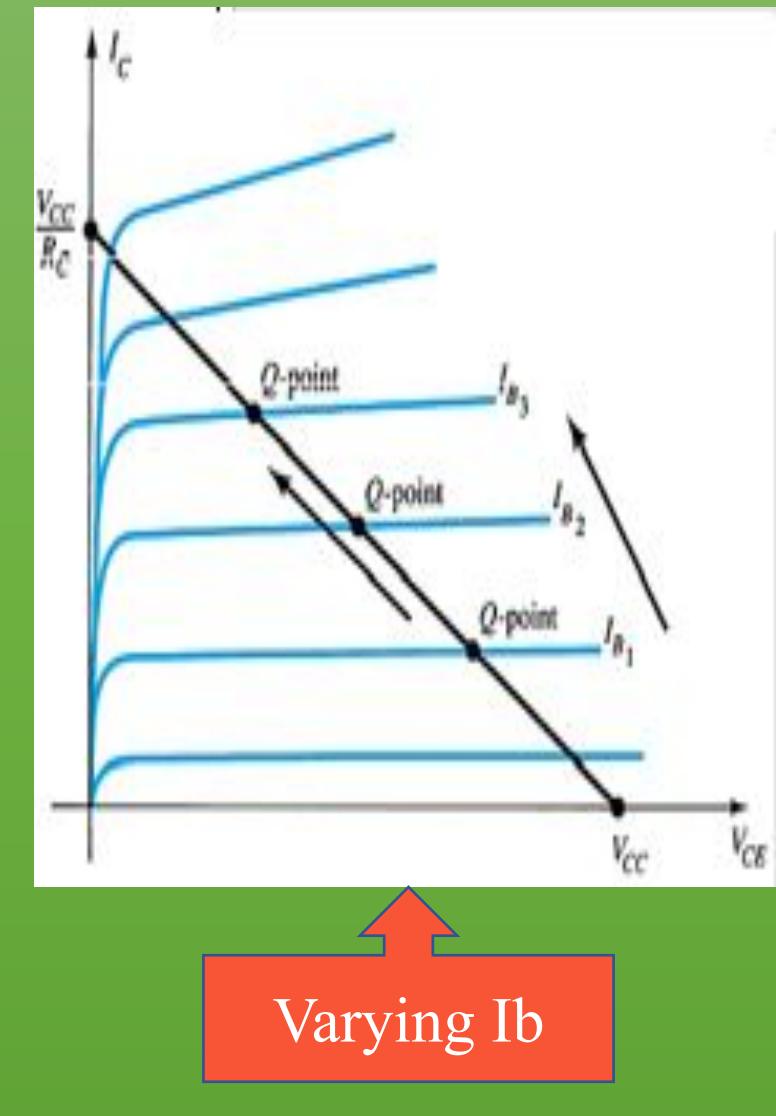
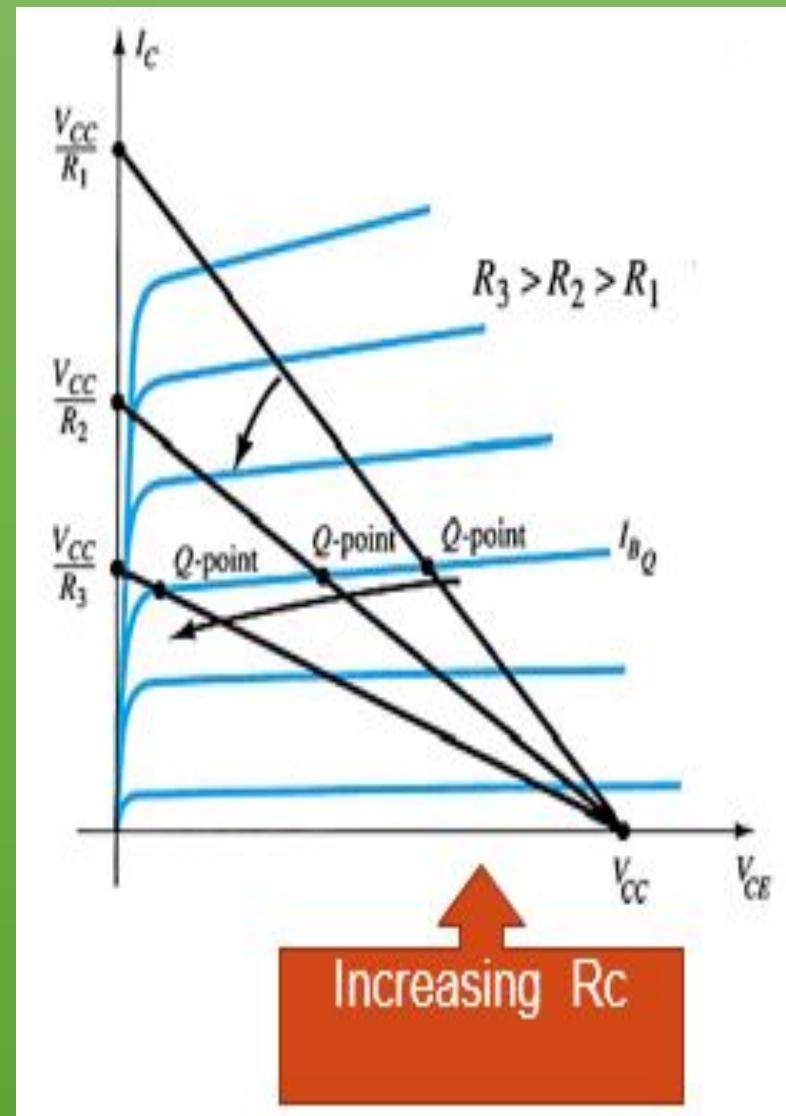
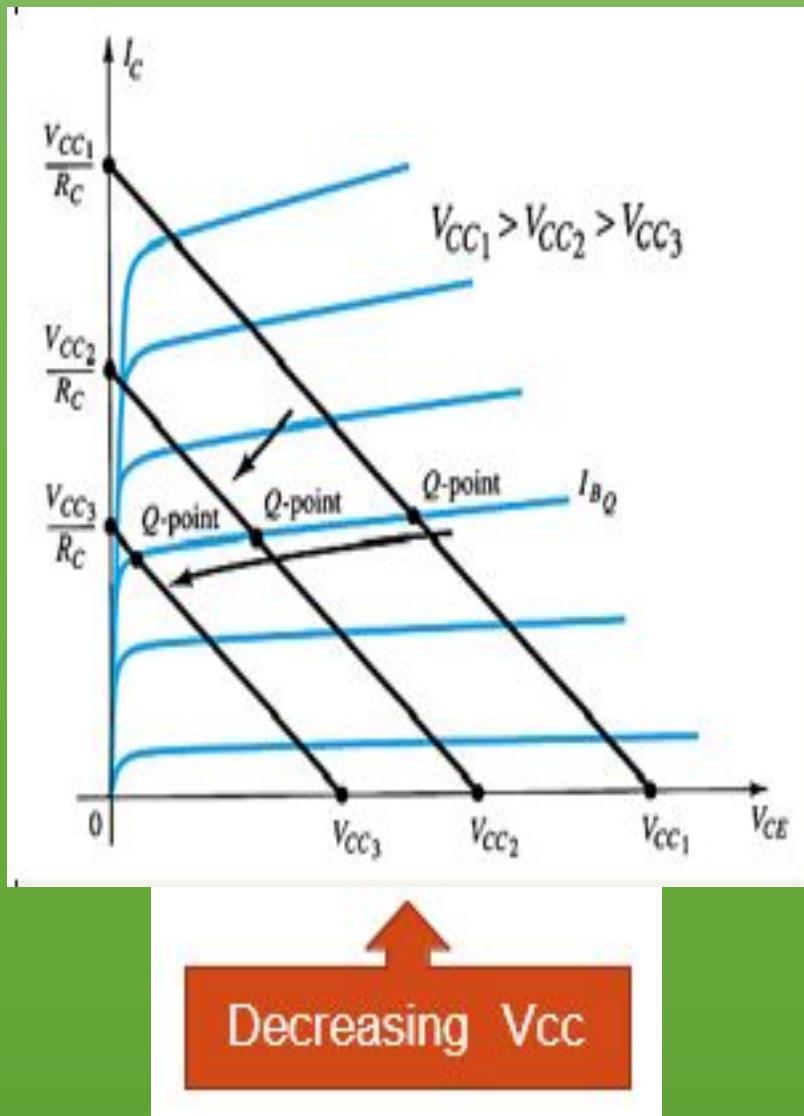
Note that R_C does not affect the value of I_C .

FIXED BIAS CIRCUIT

DISADVANTAGE

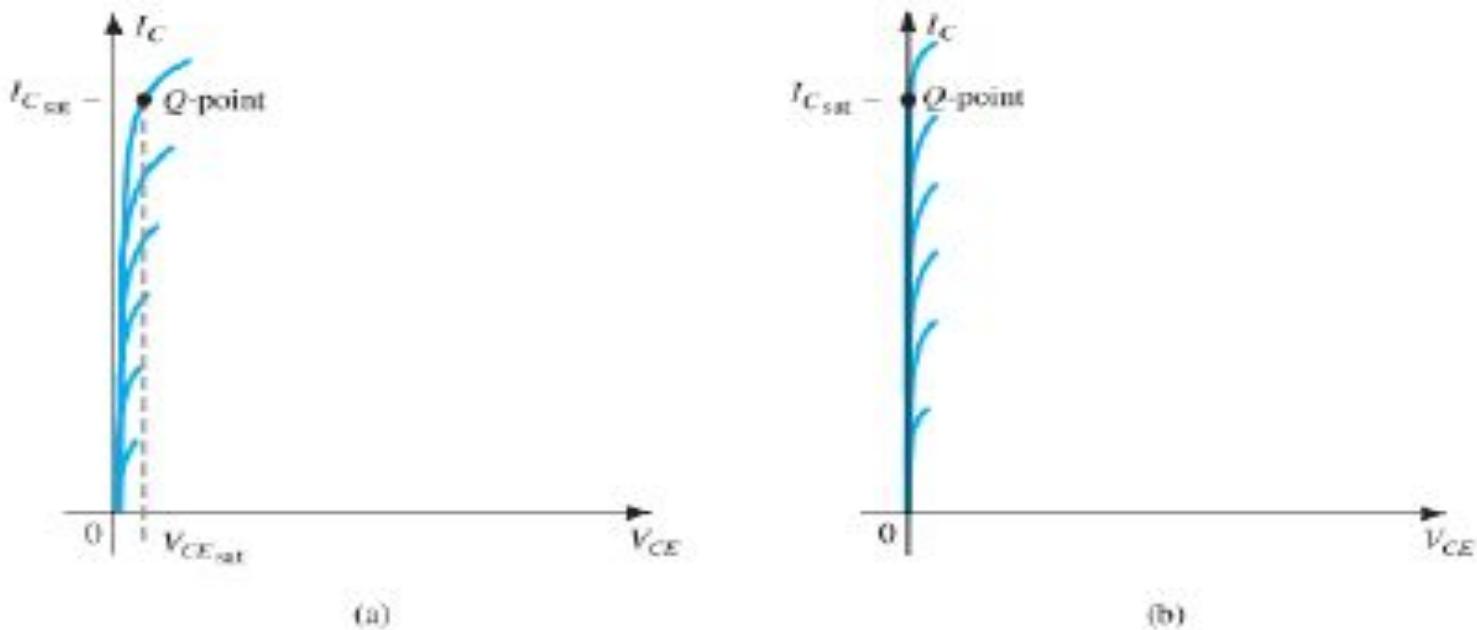
- Unstable – because it is too dependent on β and produce width change of Q-point
- For improved bias stability , add emitter resistor to dc bias.

EFFECT OF CIRCUIT VALUES ON Q POINT

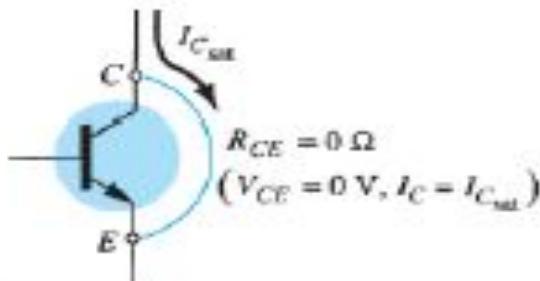


• Transistor Saturation

- Saturation regions:
 - Actual
 - approximate.

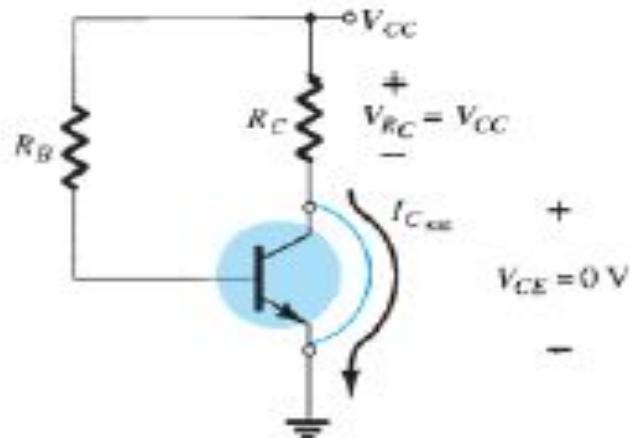


- Determining $I_{C_{sat}}$



$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{0 \text{ V}}{I_{C_{sat}}} = 0 \Omega$$

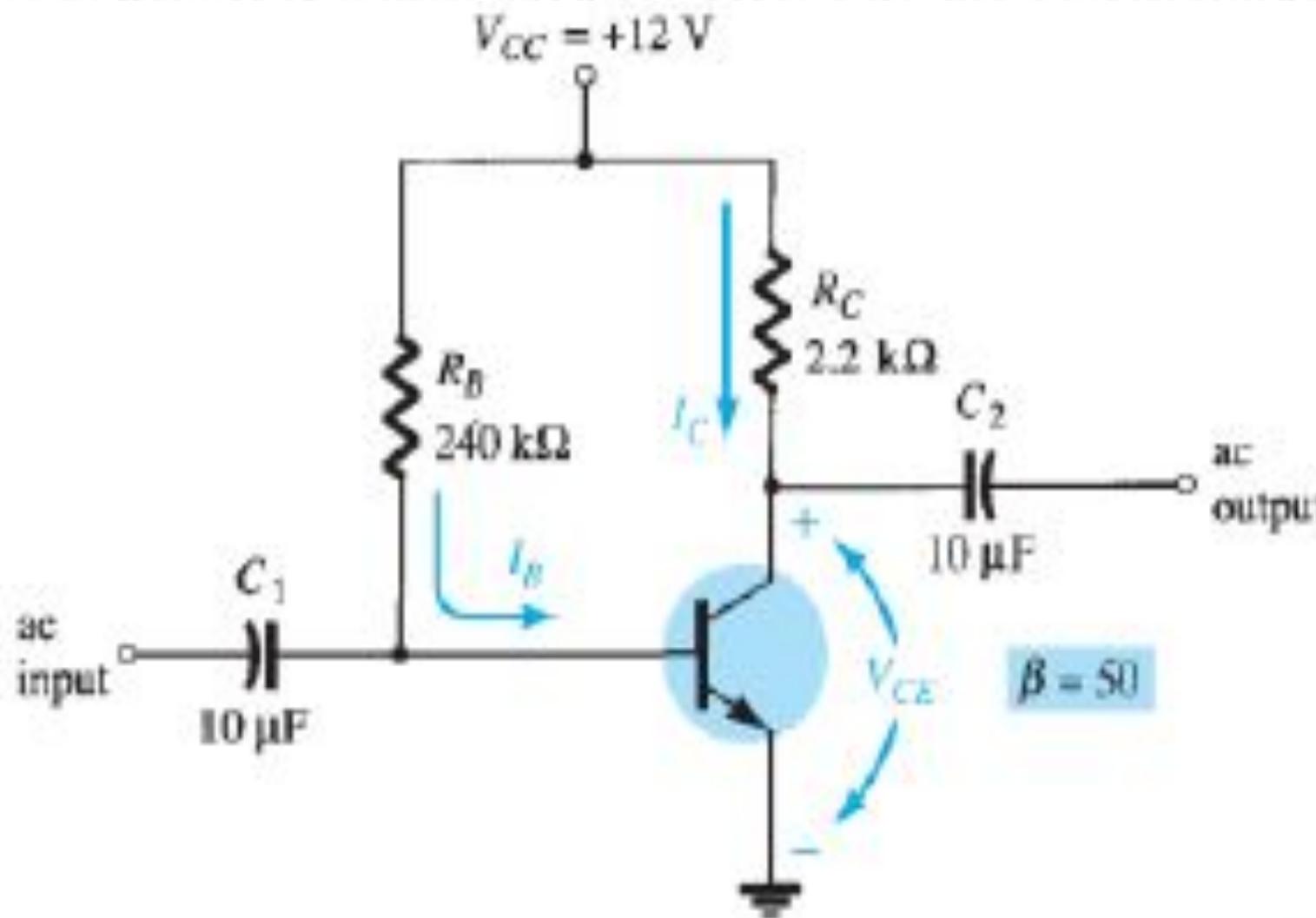
- Determining $I_{C_{sat}}$ for the fixed-bias configuration.



$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$

EXAMPLE 1

Determine the following for the fixed-bias configuration



- a. I_{BQ} and I_{CQ} .
- b. V_{CEQ} .
- c. V_B and V_C .
- d. V_{BC} .

Solution:

a. $I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega} = 47.08 \mu\text{A}$

$I_{CQ} = \beta I_{BQ} = (50)(47.08 \mu\text{A}) = 2.35 \text{ mA}$

b. $V_{CEQ} = V_{CC} - I_C R_C$
 $= 12 \text{ V} - (2.35 \text{ mA})(2.2 \text{ k}\Omega)$
 $= 6.83 \text{ V}$

c. $V_B = V_{BE} = 0.7 \text{ V}$

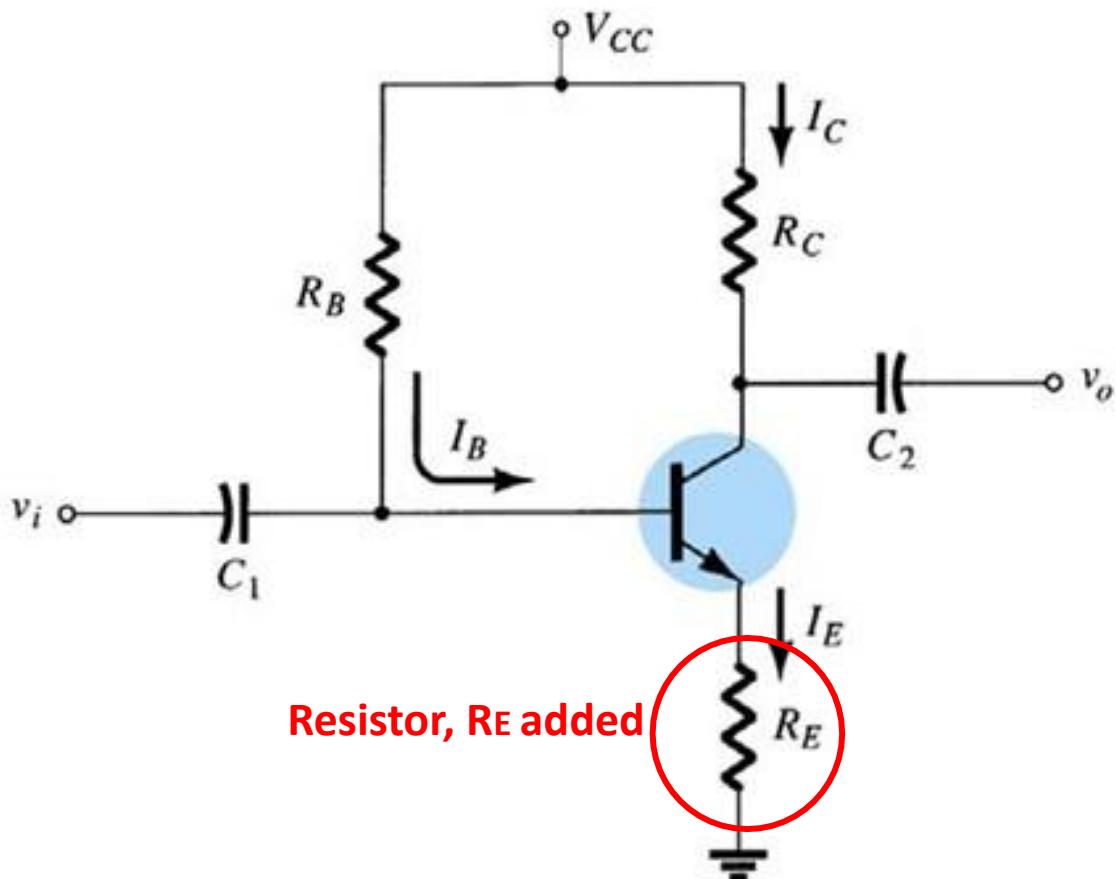
$V_C = V_{CE} = 6.83 \text{ V}$

d. Using double-subscript notation yields

$$\begin{aligned}V_{BC} &= V_B - V_C = 0.7 \text{ V} - 6.83 \text{ V} \\&= -6.13 \text{ V}\end{aligned}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

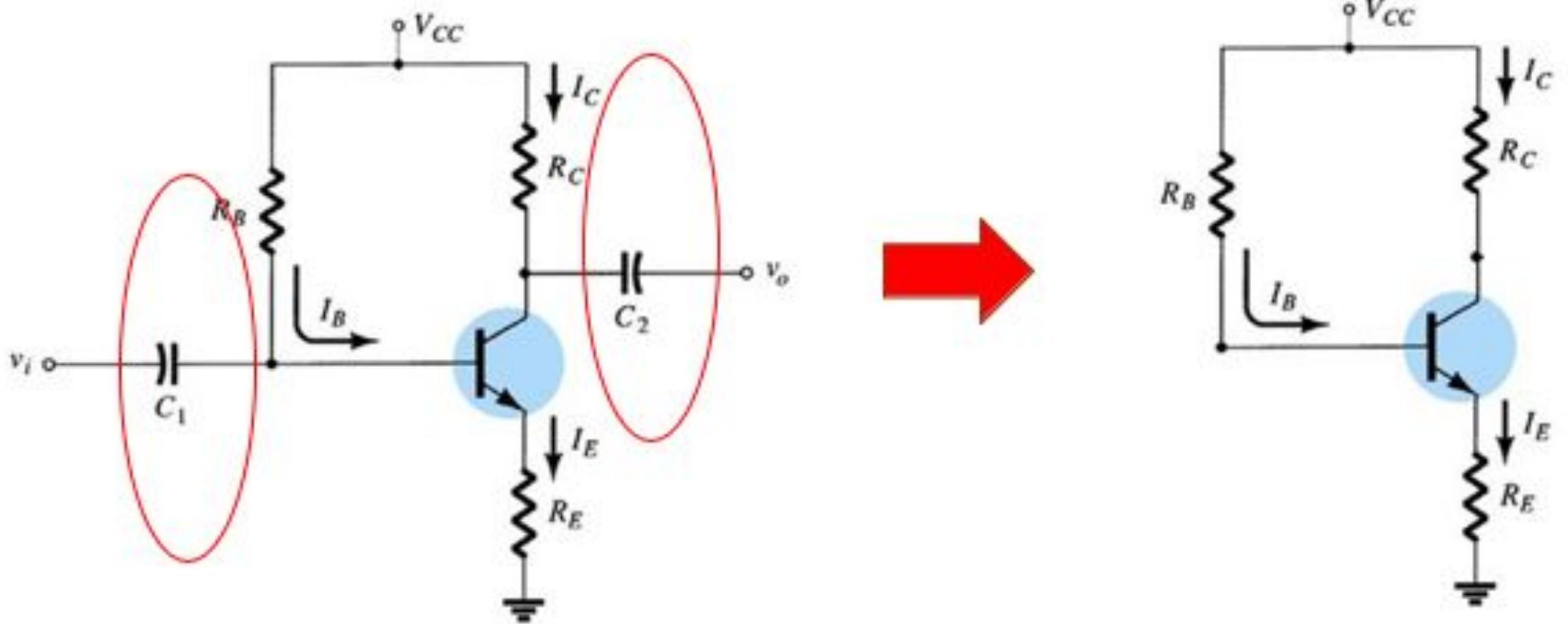
EMITTER BIAS CIRCUIT



- An emitter resistor, R_E is added to improve stability
- 1st step: Locate capacitors and replace them with an open circuit
- 2nd step: Locate 2 main loops
 - BE loop
 - CE loop

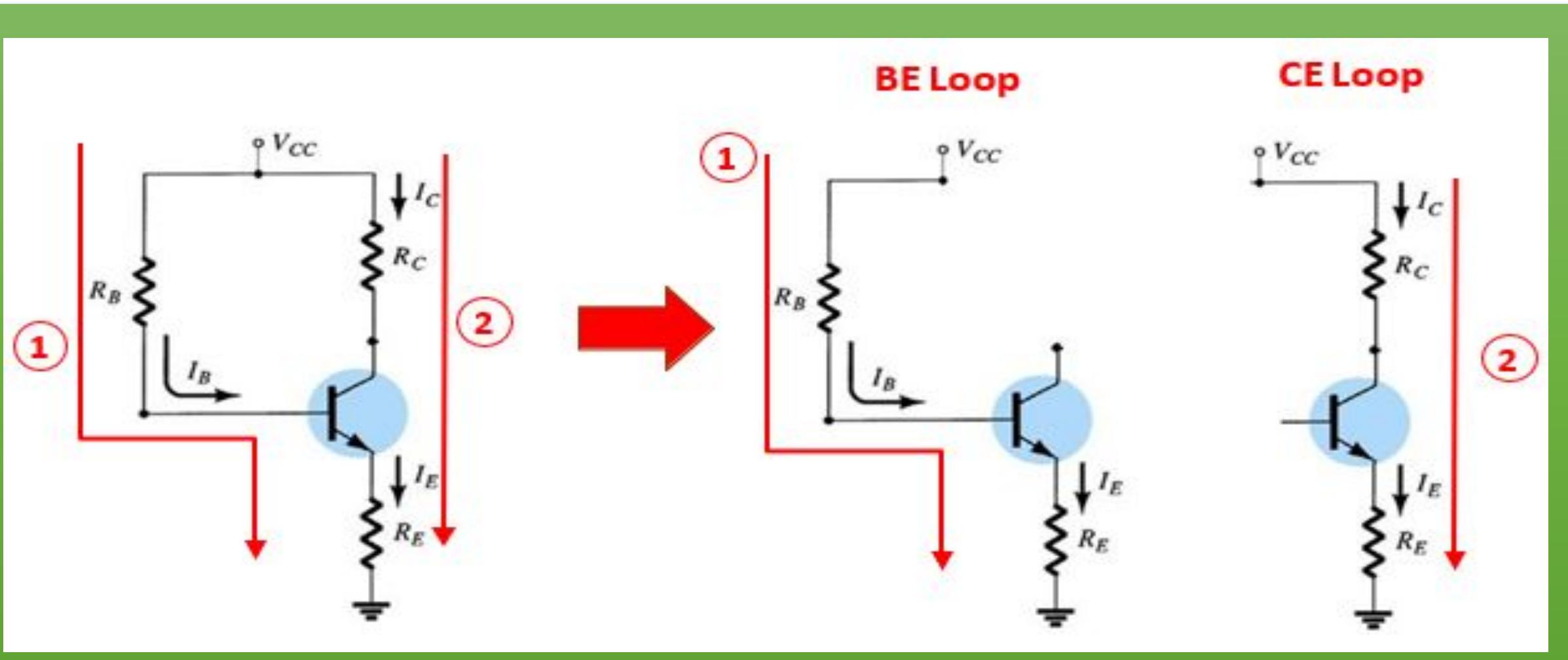
EMITTER BIAS CIRCUIT

- ✓ 1st step: Locate capacitors and replace them with an open circuit



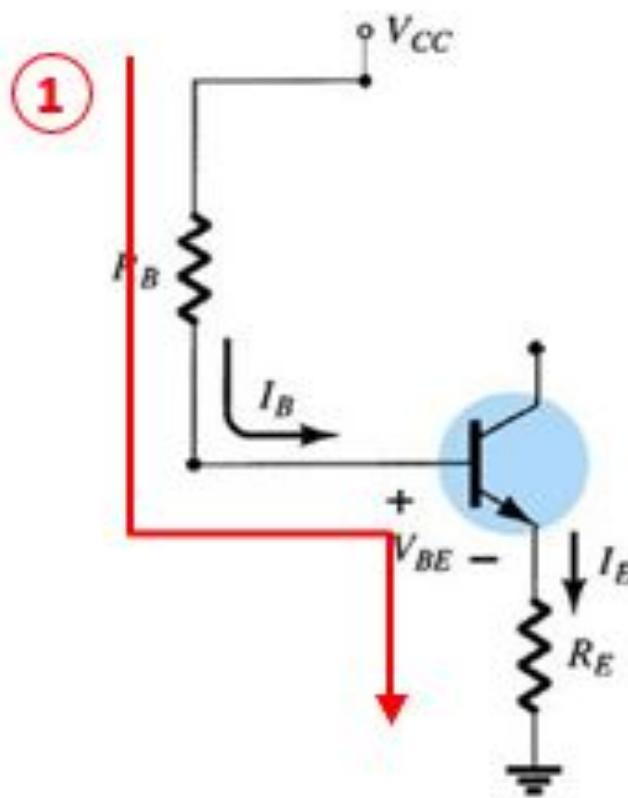
EMITTER BIAS CIRCUIT

2nd step: Locate 2 main loops.



EMITTER BIAS CIRCUIT

✓ BE Loop Analysis



■ From kvl;

$$-V_{CC} + I_B R_B + V_{BE} + I_E R_E = 0$$

Recall; $I_E = (\beta+1)I_B$

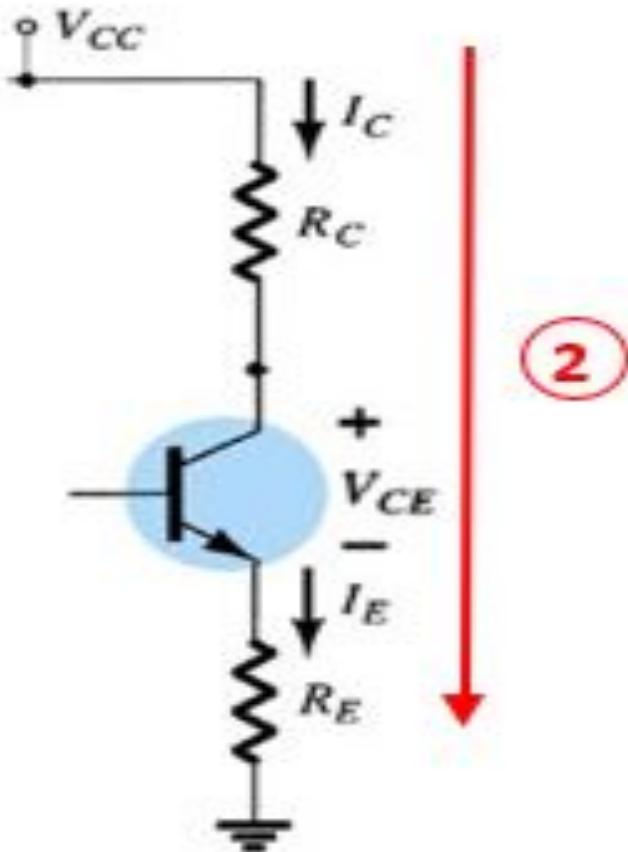
Substitute for I_E

$$-V_{CC} + I_B R_B + V_{BE} + (\beta+1)I_B R_E = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_E}$$

EMITTER BIAS CIRCUIT

✓ CE Loop Analysis



■ From KVL;

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$

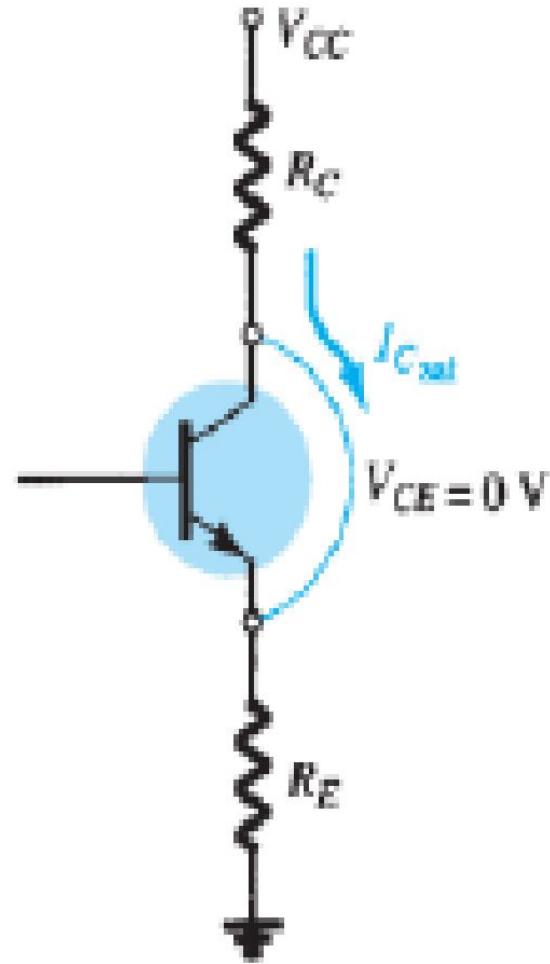
■ Assume;

$$I_E \approx I_C$$

■ Therefore;

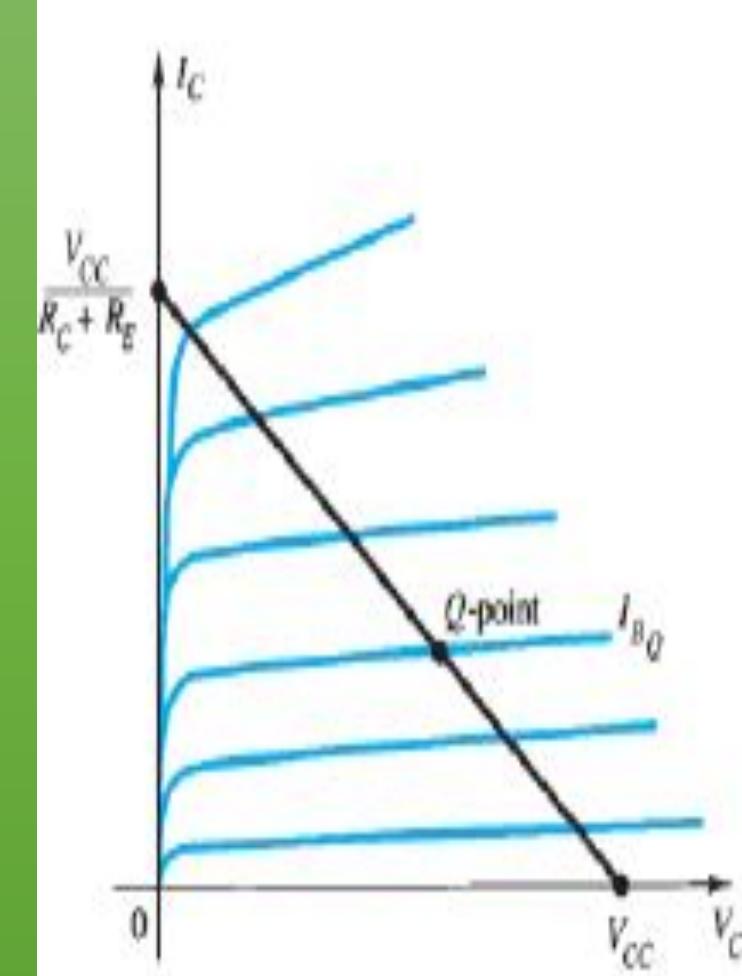
$$\therefore V_{CE} = V_{CC} - I_C (R_C + R_E)$$

SATURATION LEVEL



$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

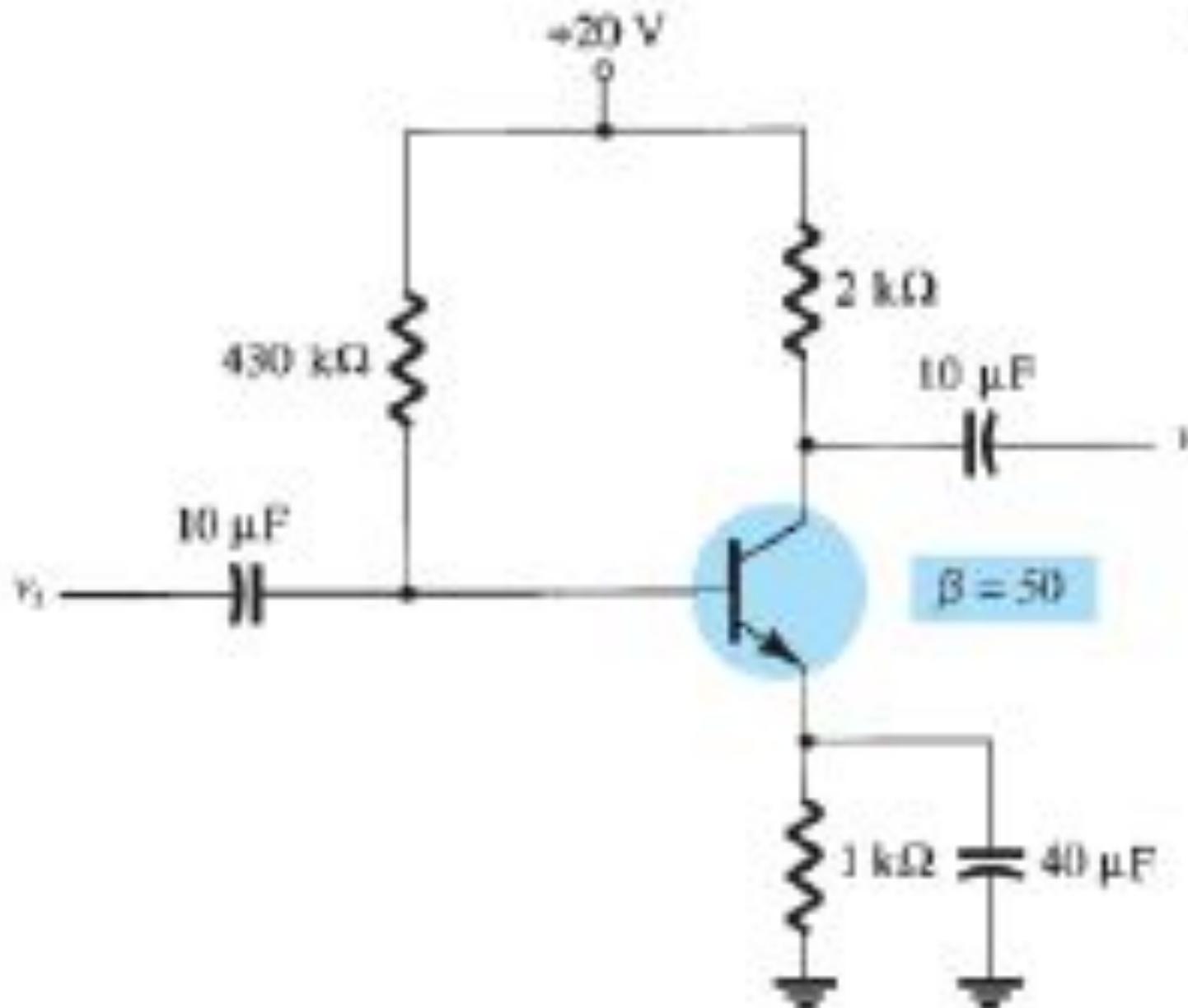
LOAD LINE ANALYSIS



$$V_{CE} = V_{CC} \Big| I_C = 0 \text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C + R_E} \Big| V_{CE} = 0 \text{ V}$$

EXAMPLE 2



For the emitter-bias network:

- a. I_B .
- b. I_C .
- c. V_{CE} .
- d. V_C .
- e. V_E .
- f. V_B .
- g. V_{BE} .

SOLUTION

a.

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20 \text{ V} - 0.7 \text{ V}}{430 \text{ k}\Omega + (51)(1 \text{ k}\Omega)}$$
$$= \frac{19.3 \text{ V}}{481 \text{ k}\Omega} = 40.1 \mu\text{A}$$

b. $I_C = \beta I_B$

$$= (50)(40.1 \mu\text{A})$$

$$\approx 2.01 \text{ mA}$$

c.

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega + 1 \text{ k}\Omega) = 20 \text{ V} - 6.03 \text{ V}$$
$$= 13.97 \text{ V}$$

d. $V_C = V_{CC} - I_C R_C$

$$= 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega) = 20 \text{ V} - 4.02 \text{ V}$$

$$= 15.98 \text{ V}$$

SOLUTION CONTINUED...

$$\begin{aligned} \text{c. } V_E &= V_C - V_{CE} \\ &= 15.98 \text{ V} - 13.97 \text{ V} \\ &= \mathbf{2.01 \text{ V}} \end{aligned}$$

$$\begin{aligned} \text{or } V_E &= I_E R_E \approx I_C R_E \\ &= (2.01 \text{ mA})(1 \text{ k}\Omega) \\ &= \mathbf{2.01 \text{ V}} \end{aligned}$$

$$\begin{aligned} \text{f. } V_B &= V_{BE} + V_E \\ &= 0.7 \text{ V} + 2.01 \text{ V} \\ &= \mathbf{2.71 \text{ V}} \end{aligned}$$

$$\begin{aligned} \text{g. } V_{BC} &= V_B - V_C \\ &= 2.71 \text{ V} - 15.98 \text{ V} \\ &= \mathbf{-13.27 \text{ V}} \text{ (reverse-biased as required)} \end{aligned}$$

IMPROVED BIAS STABILITY

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature, and transistor beta, change.

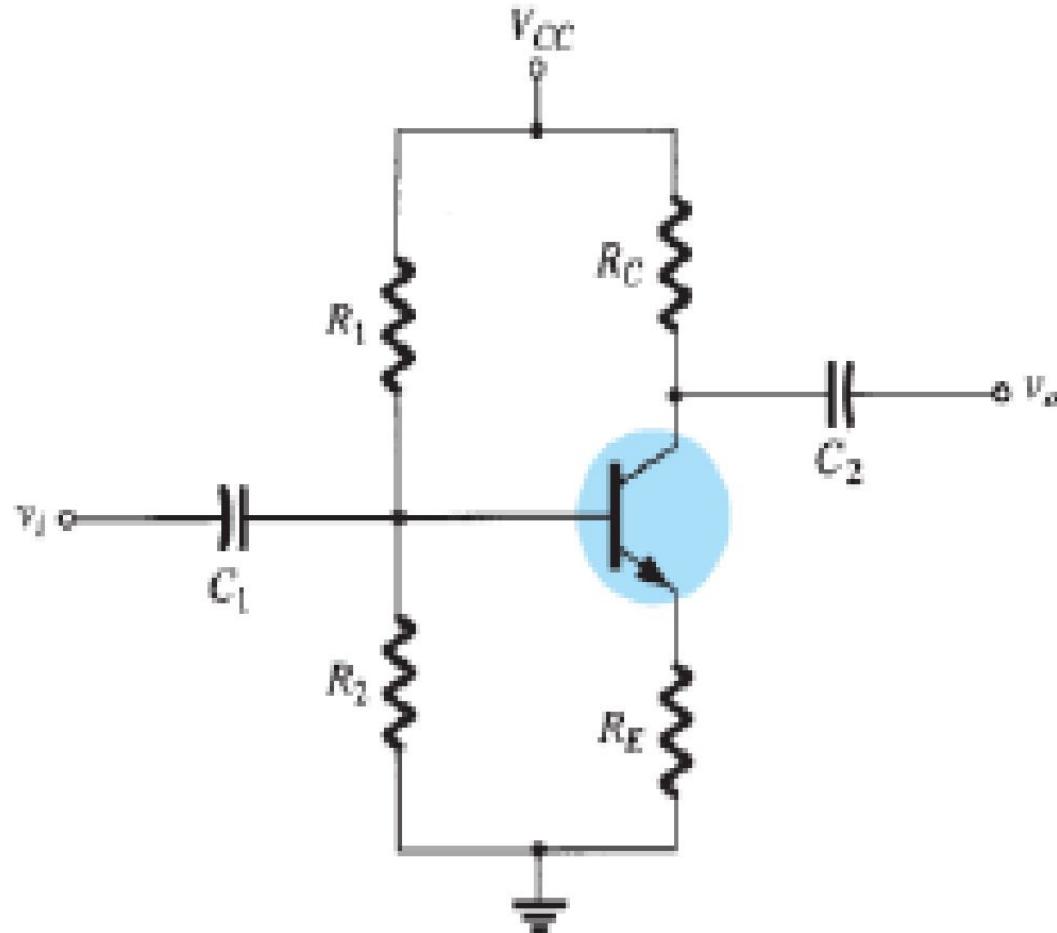
β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	47.08	2.35	6.83
100	47.08	4.71	1.64

For Fixed Bias Circuit

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	40.1	2.01	13.97
100	36.3	3.63	9.11

For Emitter Bias Circuit

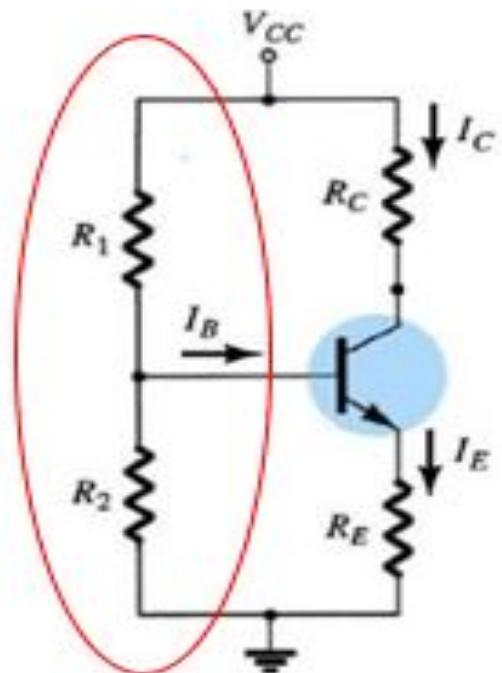
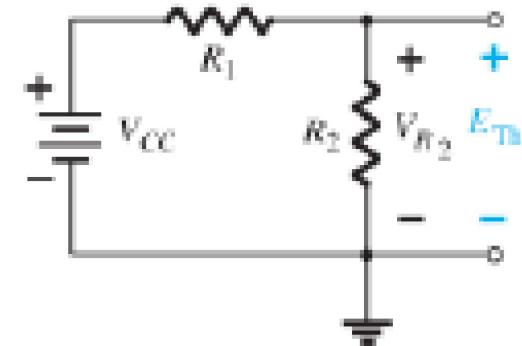
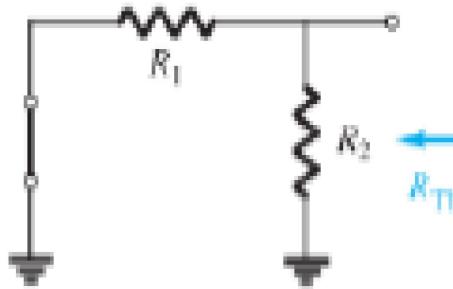
VOLTAGE DIVIDER BIAS OR POTENTIAL DIVIDER BIAS



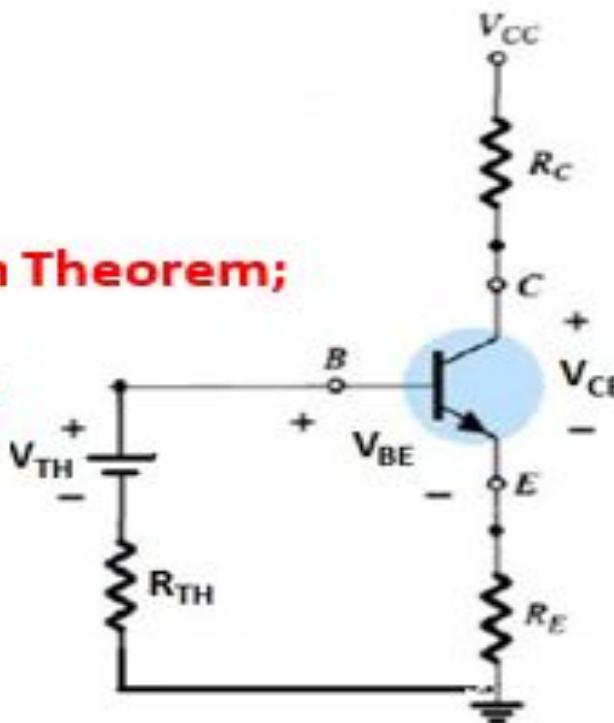
- Two methods of analyzing a voltage divider bias circuit are:
 - **Exact method** : can be applied to any voltage divider circuit
 - **Approximate method** : direct method, saves time and energy

$$\beta R_E \geq 10R_2$$

EXACT METHOD



Thevenin Theorem;



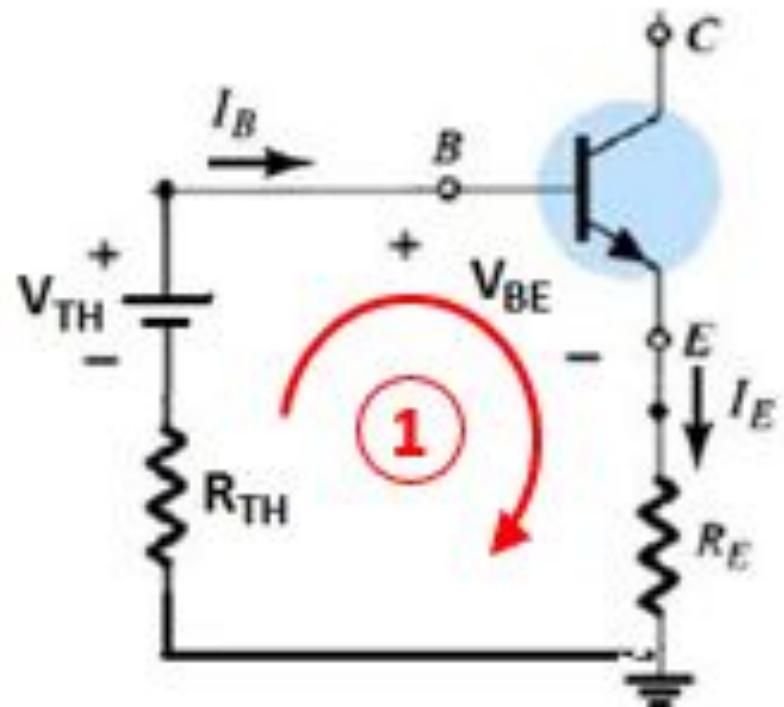
From Thevenin Theorem;

$$R_{TH} = R_1 // R_2 = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$

Simplified Circuit

EXACT METHOD



■ From KVL;

$$-V_{TH} + I_B R_{TH} + V_{BE} + I_E R_E = 0$$

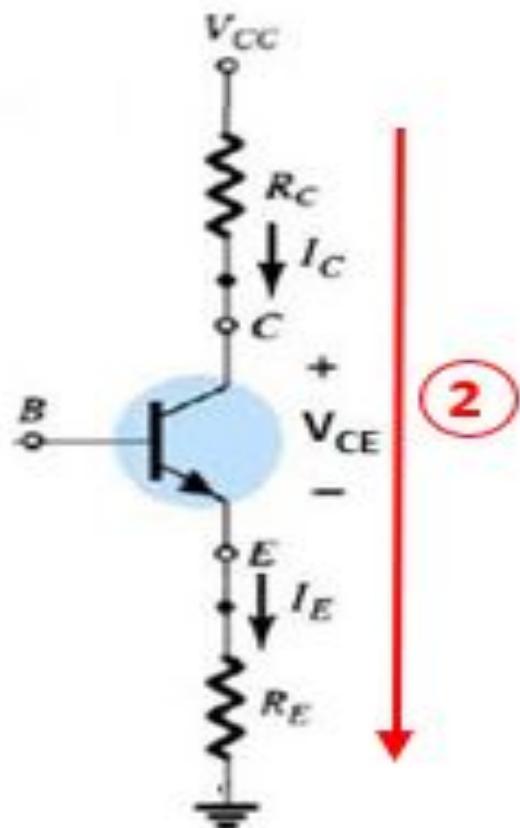
Recall; $I_E = (\beta + 1)I_B$

Substitute for I_E

$$-V_{TH} + I_B R_{TH} + V_{BE} + (\beta + 1)I_B R_E = 0$$

$$\therefore I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E}$$

EXACT METHOD



■ From KVL;

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$

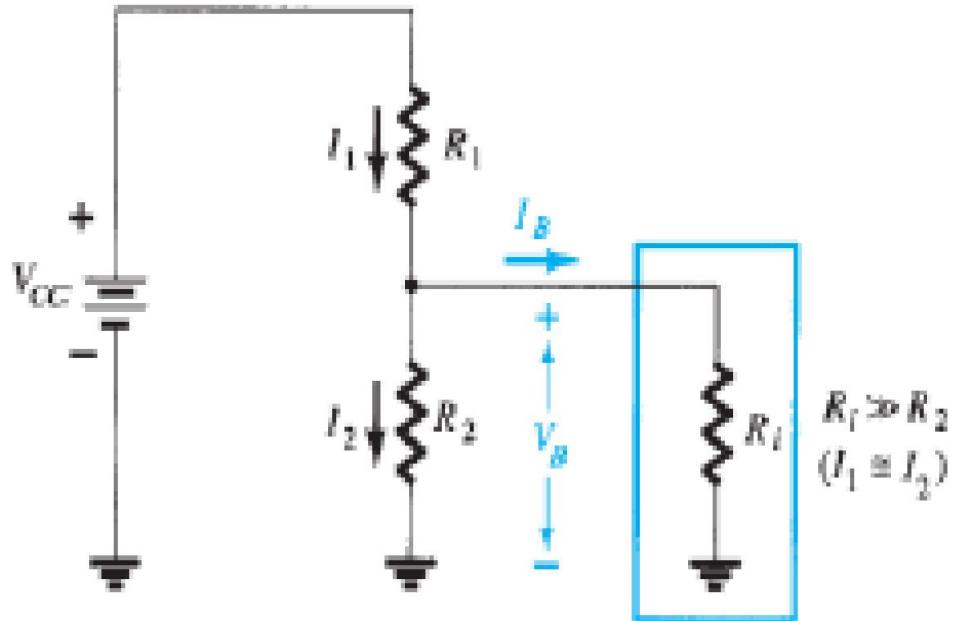
■ Assume;

$$I_E \approx I_C$$

■ Therefore;

$$\therefore V_{CE} = V_{CC} - I_C (R_C + R_E)$$

APPROXIMATE ANALYSIS



the reflected resistance between base and emitter is defined by $R_i = (\beta + 1)R_E$. If R_i is much larger than the resistance R_2 , the current I_B will be much smaller than I_2 (current always seeks the path of least resistance) and I_2 will be approximately equal to I_1 . If we accept the approximation that I_B is essentially zero amperes compared to I_1 or I_2 , then $I_1 = I_2$ and R_1 and R_2 can be considered series elements. The voltage across R_2 , which is actually the base voltage, can be determined using the voltage-divider rule (hence the name for the configuration). That is,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Since $R_i = (\beta + 1)R_E \cong \beta R_E$ the condition that will define whether the approximate approach can be applied will be the following:

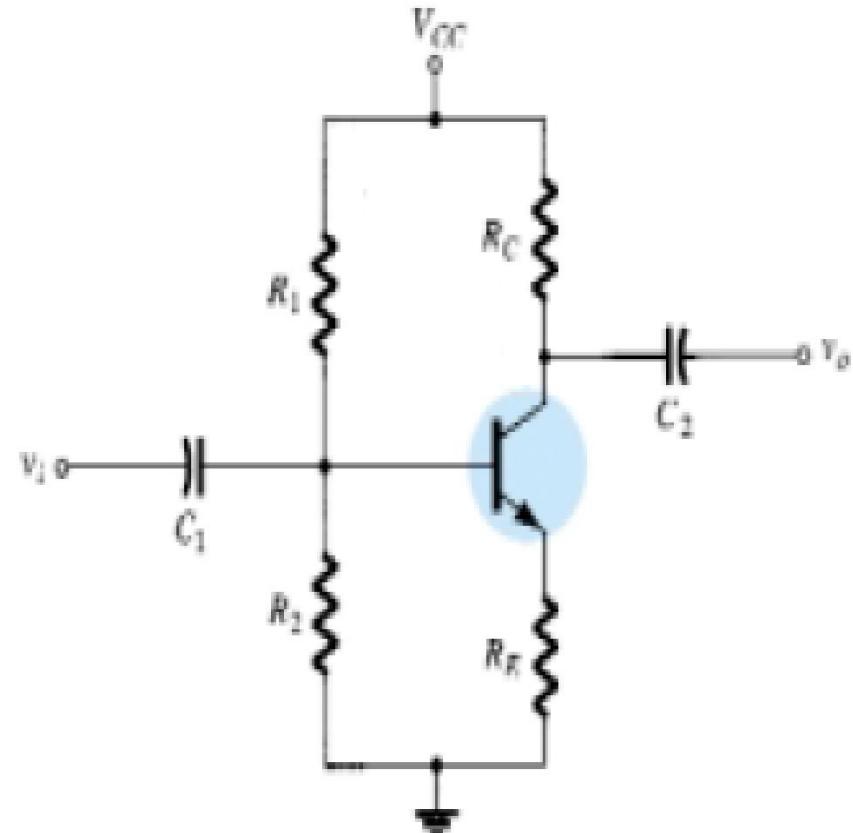
$$\beta R_E \geq 10R_2$$

In other words, if β times the value of R_E is at least 10 times the value of R_2 , the approximate approach can be applied with a high degree of accuracy.

APPROXIMATE ANALYSIS

Once V_B is determined, the level of V_E can be calculated from

$$V_E = V_B - V_{BE}$$



and the emitter current can be determined from

$$I_E = \frac{V_E}{R_E}$$

and

$$I_{C_Q} \cong I_E$$

The collector-to-emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

but since $I_E \cong I_C$,

$$\beta R_E \geq 10 R_2$$

$$V_{CE_Q} = V_{CC} - I_C (R_C + R_E)$$

TRANSISTOR SATURATION IN VOLTAGE DIVIDER BIAS

The output collector emitter circuit loop of Voltage divider bias circuit is same as that of Emitter bias, so the resulting equation for saturation current (when $V_{CE}=0$)

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E}$$

LOAD LINE ANALYSIS

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of Emitter Bias circuit with,

$$I_C = \frac{V_{CC}}{R_C + R_E} \Big| V_{CE}=0 \text{ V}$$

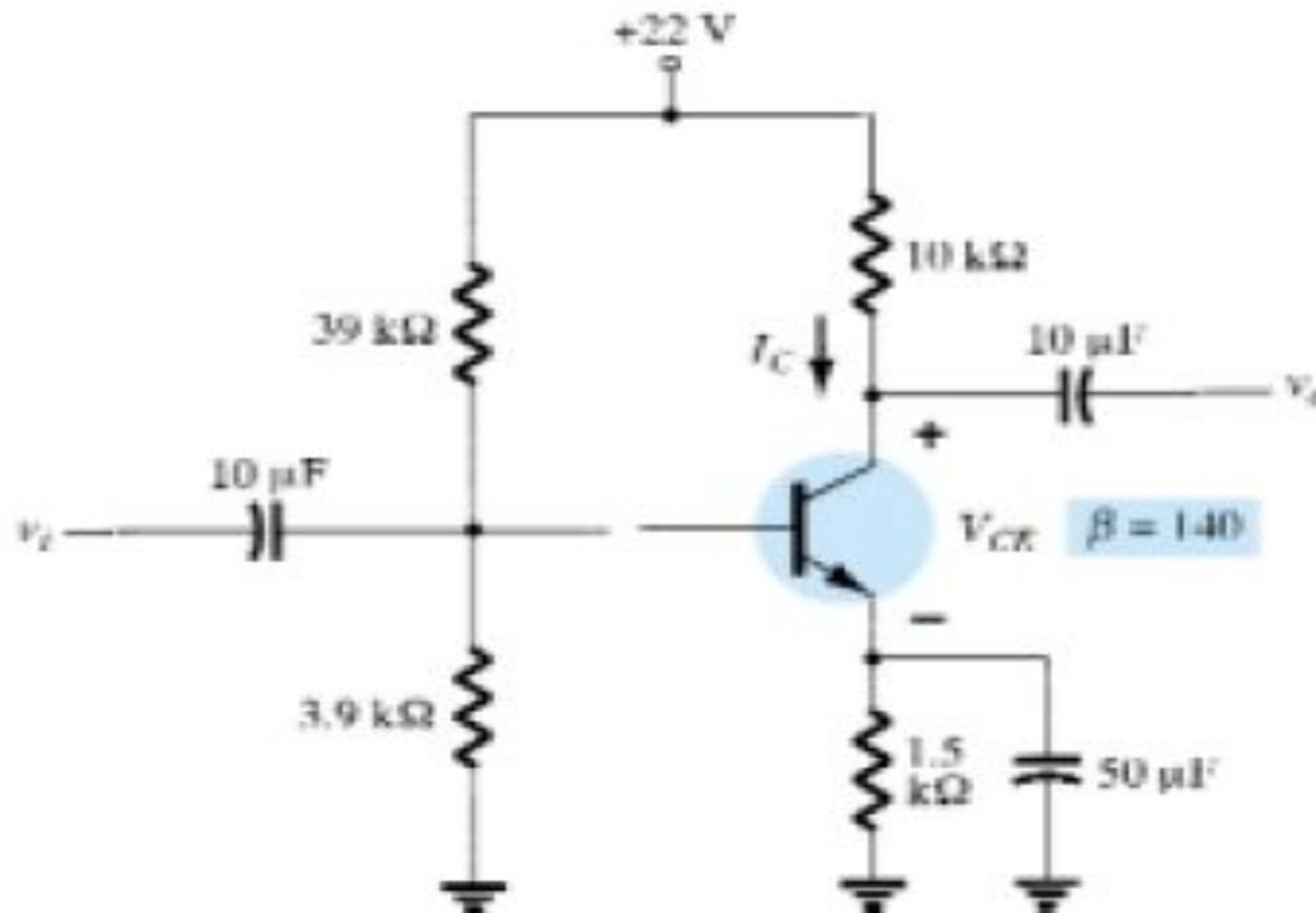
and

$$V_{CE} = V_{CC} \Big| I_C=0 \text{ mA}$$

The level of I_B is of course determined by a different equation for the voltage-divider bias and the emitter-bias configurations.

EXAMPLE 1

Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of Fig.



SOLUTION

EXACT ANALYSIS

$$R_{\text{Th}} = R_1 \parallel R_2$$
$$= \frac{(39 \text{ k}\Omega)(3.9 \text{ k}\Omega)}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} = 3.55 \text{ k}\Omega$$

$$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2}$$
$$= \frac{(3.9 \text{ k}\Omega)(22 \text{ V})}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} = 2 \text{ V}$$

$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E}$$
$$= \frac{2 \text{ V} - 0.7 \text{ V}}{3.55 \text{ k}\Omega + (141)(1.5 \text{ k}\Omega)} = \frac{1.3 \text{ V}}{3.55 \text{ k}\Omega + 211.5 \text{ k}\Omega}$$
$$= 6.05 \mu\text{A}$$

$$I_C = \beta I_B$$
$$= (140)(6.05 \mu\text{A})$$
$$= 0.85 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 22 \text{ V} - (0.85 \text{ mA})(10 \text{ k}\Omega + 1.5 \text{ k}\Omega)$$
$$= 22 \text{ V} - 9.78 \text{ V}$$
$$= 12.22 \text{ V}$$

SOLUTION

$$\beta R_E \geq 10R_2$$

$$(140)(1.5 \text{ k}\Omega) \geq 10(3.9 \text{ k}\Omega)$$

$$210 \text{ k}\Omega \geq 39 \text{ k}\Omega \text{ (satisfied)}$$

APPROXIMATE ANALYSIS

$$\begin{aligned}V_B &= \frac{R_2 V_{CC}}{R_1 + R_2} \\&= \frac{(3.9 \text{ k}\Omega)(22 \text{ V})}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} \\&= 2 \text{ V}\end{aligned}$$

$$\begin{aligned}V_E &= V_B - V_{BE} \\&= 2 \text{ V} - 0.7 \text{ V} \\&= 1.3 \text{ V}\end{aligned}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3 \text{ V}}{1.5 \text{ k}\Omega} = 0.867 \text{ mA}$$

compared to 0.85 mA with the exact analysis. Finally,

$$\begin{aligned}V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\&= 22 \text{ V} - (0.867 \text{ mA})(10 \text{ k}\Omega + 1.5 \text{ k}\Omega) \\&= 22 \text{ V} - 9.97 \text{ V} \\&= 12.03 \text{ V}\end{aligned}$$

EXAMPLE 2

Repeat the same example with value of Beta reduced to half i.e. 70

Solution

This example is not a comparison of exact versus approximate methods but a testing of how much the *Q*-point will move if the level of β is cut in half. R_{Th} and E_{Th} are the same:

$$R_{Th} = 3.55 \text{ k}\Omega, \quad E_{Th} = 2 \text{ V}$$

$$\begin{aligned} I_B &= \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} \\ &= \frac{2 \text{ V} - 0.7 \text{ V}}{3.55 \text{ k}\Omega + (71)(1.5 \text{ k}\Omega)} = \frac{1.3 \text{ V}}{3.55 \text{ k}\Omega + 106.5 \text{ k}\Omega} \\ &= 11.81 \mu\text{A} \end{aligned}$$

$$\begin{aligned} I_{C_o} &= \beta I_B \\ &= (70)(11.81 \mu\text{A}) \\ &= 0.83 \text{ mA} \end{aligned}$$

$$\begin{aligned} V_{CE_o} &= V_{CC} - I_C(R_C + R_E) \\ &= 22 \text{ V} - (0.83 \text{ mA})(10 \text{ k}\Omega + 1.5 \text{ k}\Omega) \\ &= 12.46 \text{ V} \end{aligned}$$

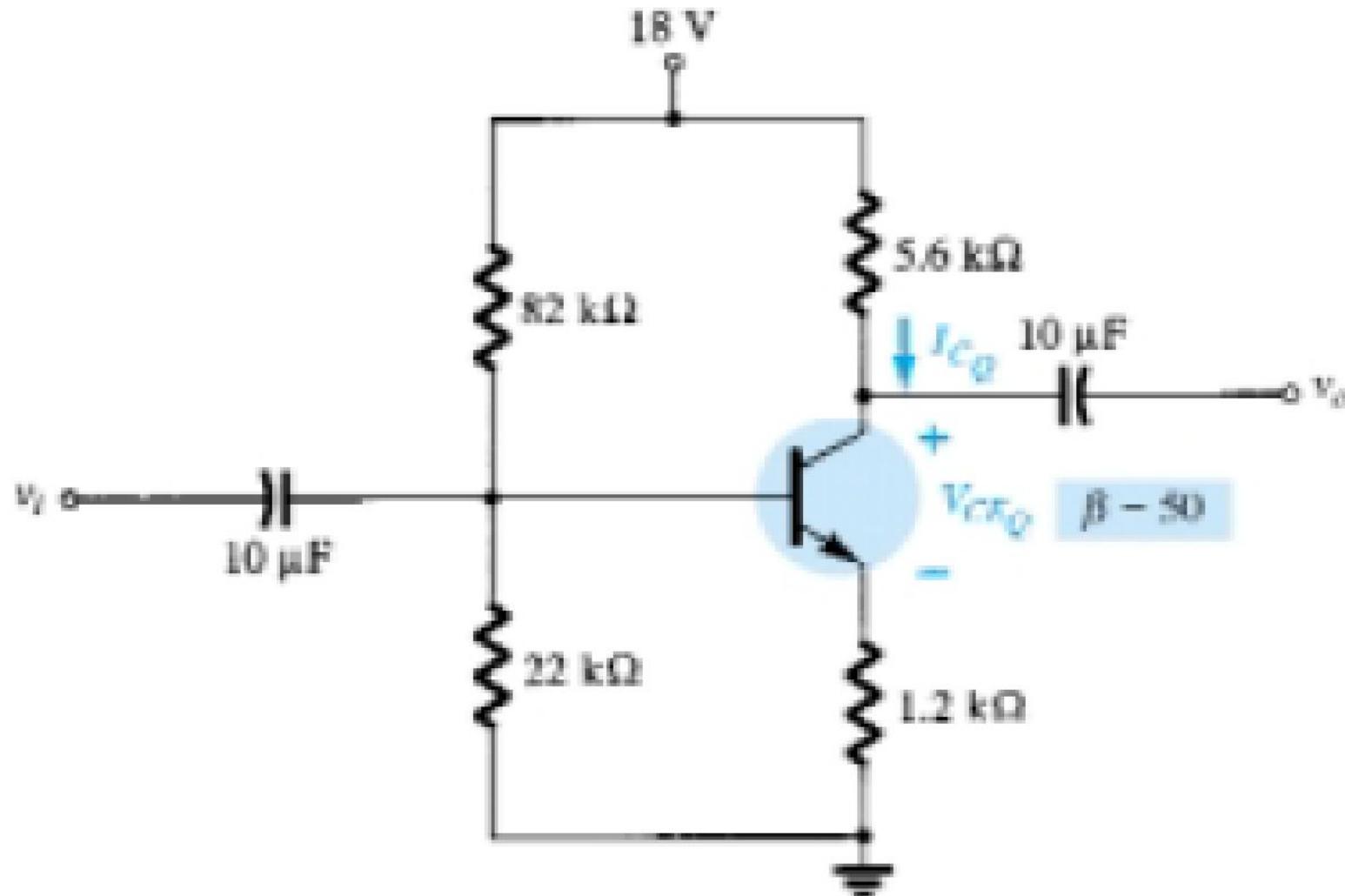
RESULT COMPARISON WHEN BETA CHANGES

β	I_{CQ} (mA)	V_{CEQ} (V)
140	0.85	12.22
70	0.83	12.46

The results clearly show the relative insensitivity of the circuit to the change in β . Even though β is drastically cut in half, from 140 to 70, the levels of I_{CQ} and V_{CEQ} are essentially the same.

EXAMPLE 3

Determine the levels of I_{CQ} and V_{CEQ} for the voltage-divider configuration of Fig. using the exact and approximate techniques and compare solutions.



SOLUTION

In this we can check the difference in the solution if we ignore the condition of approximate analysis or if the condition of approximate analysis is not satisfied.

Exact Analysis

$$\beta R_E \geq 10R_2$$

$$(50)(1.2 \text{ k}\Omega) \geq 10(22 \text{ k}\Omega)$$

$$60 \text{ k}\Omega \not\geq 220 \text{ k}\Omega \text{ (not satisfied)}$$

$$R_{Th} = R_1 \parallel R_2 = 82 \text{ k}\Omega \parallel 22 \text{ k}\Omega = 17.35 \text{ k}\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22 \text{ k}\Omega(18 \text{ V})}{82 \text{ k}\Omega + 22 \text{ k}\Omega} = 3.81 \text{ V}$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{3.81 \text{ V} - 0.7 \text{ V}}{17.35 \text{ k}\Omega + (51)(1.2 \text{ k}\Omega)} = \frac{3.11 \text{ V}}{78.55 \text{ k}\Omega}$$
$$= 39.6 \mu\text{A}$$

$$I_{CQ} = \beta I_B = (50)(39.6 \mu\text{A}) = 1.98 \text{ mA}$$

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$$
$$= 18 \text{ V} - (1.98 \text{ mA})(5.6 \text{ k}\Omega + 1.2 \text{ k}\Omega)$$
$$= 4.54 \text{ V}$$

SOLUTION

Approximate Analysis

$$V_B = E_{Th} = 3.81 \text{ V}$$

$$V_E = V_B - V_{BE} = 3.81 \text{ V} - 0.7 \text{ V} = 3.11 \text{ V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{3.11 \text{ V}}{1.2 \text{ k}\Omega} = 2.59 \text{ mA}$$

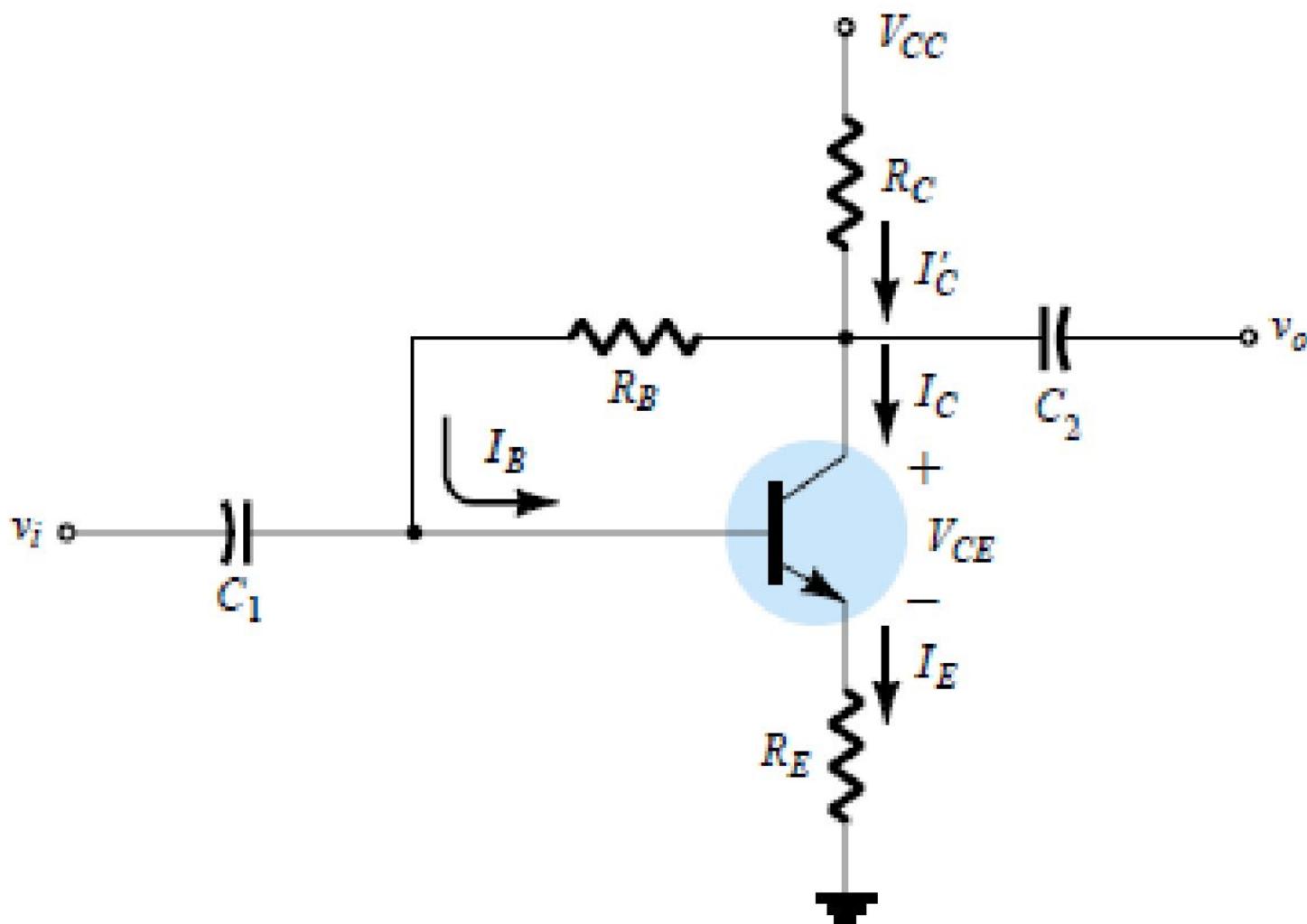
$$\begin{aligned}V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\&= 18 \text{ V} - (2.59 \text{ mA})(5.6 \text{ k}\Omega + 1.2 \text{ k}\Omega) \\&= 3.88 \text{ V}\end{aligned}$$

RESULT COMPARISON

	I_{CQ} (mA)	V_{CEQ} (V)
Exact	1.98	4.54
Approximate	2.59	3.88

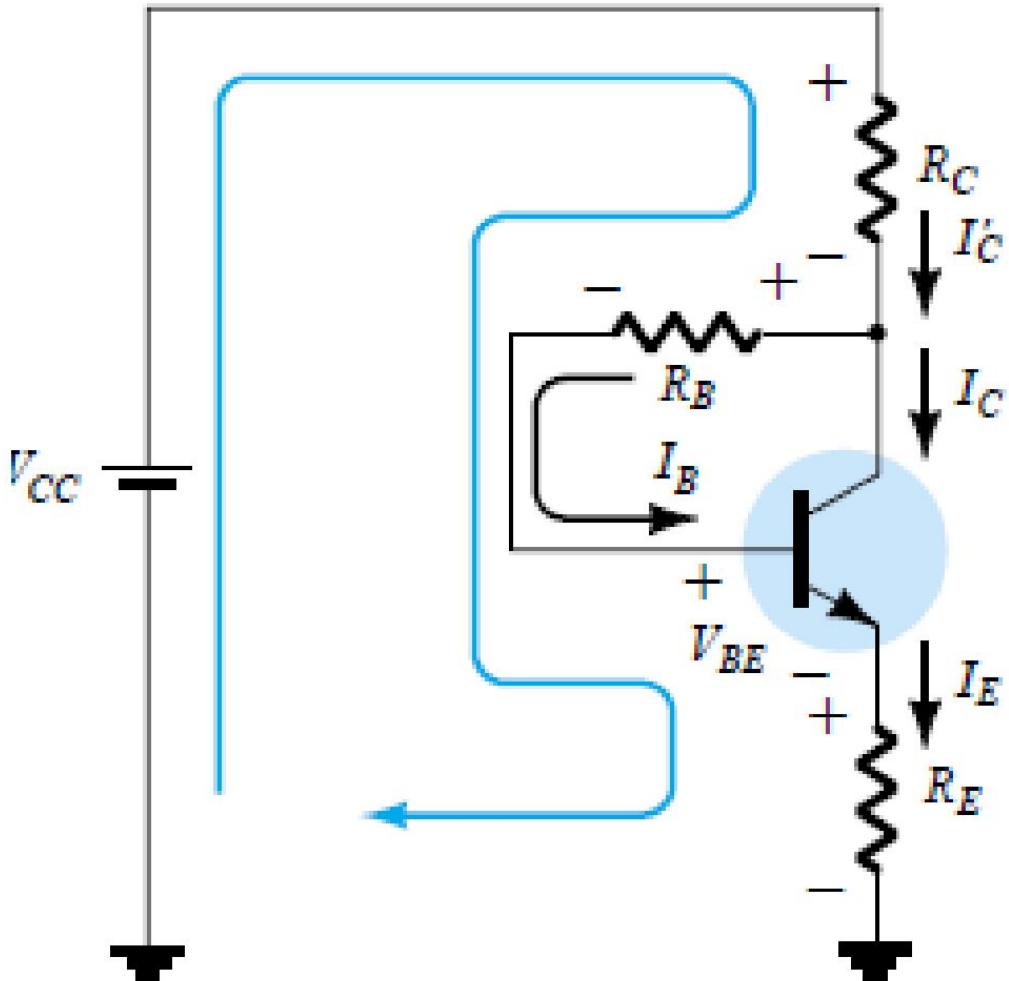
The results reveal the difference between exact and approximate solutions. I_{CQ} is about 30% greater with the approximate solution, while V_{CEQ} is about 10% less. The results are notably different in magnitude, but even though βR_E is only about three times larger than R_2 , the results are still relatively close to each other.

COLLECTOR FEEDBACK BIAS/ DC BIAS WITH VOLTAGE FEEDBACK



Improved level of stability can also be obtained by introducing feedback path from collector to base.

DC ANALYSIS



Base Emitter Loop

Applying KVL to input loop,

$$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

It is important to note that the current through R_C is not I_C but I'_C (where $I'_C = I_C + I_B$). However, the level of I_C and I'_C far exceeds the usual level of I_B and the approximation $I'_C \cong I_C$ is normally employed. Substituting $I'_C \cong I_C = \beta I_B$ and $I_E \cong I_C$ will result in

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

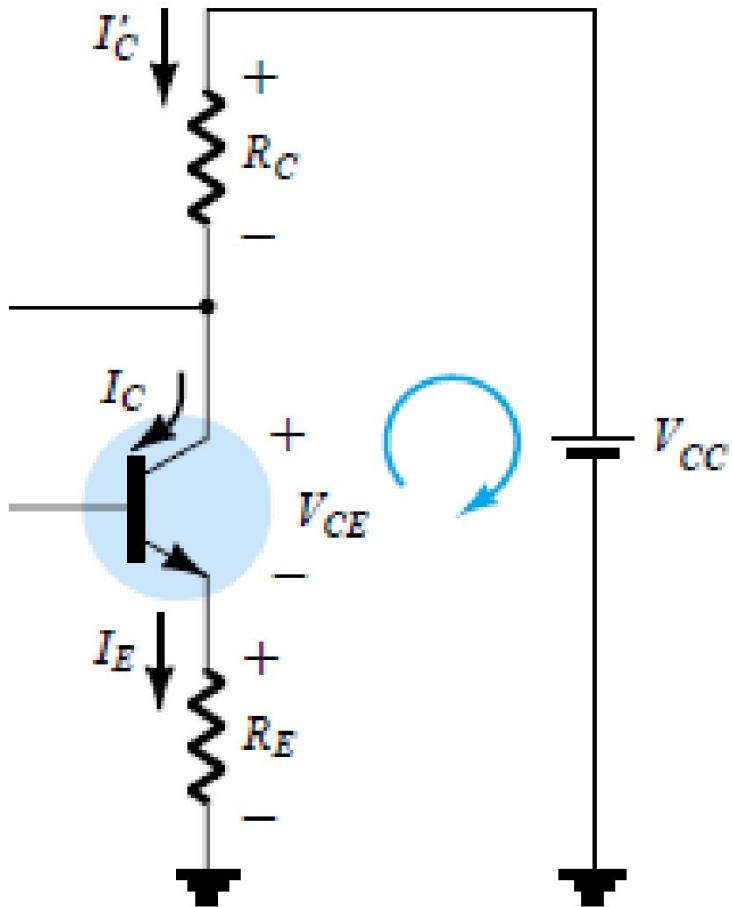
Gathering terms, we have

$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_B = 0$$

and solving for I_B yields

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

DC ANALYSIS



Applying KVL to input loop,

$$I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I'_C \cong I_C$ and $I_E \cong I_C$, we have

$$I_C (R_C + R_E) + V_{CE} - V_{CC} = 0$$

and

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

which is exactly as obtained for the emitter-bias and voltage-divider bias configurations.

Collector Emitter Loop

SATURATION

Using the approximation $I'_C = I_C$, the equation for the saturation current is the same as obtained for the voltage-divider and emitter-bias configurations. That is,

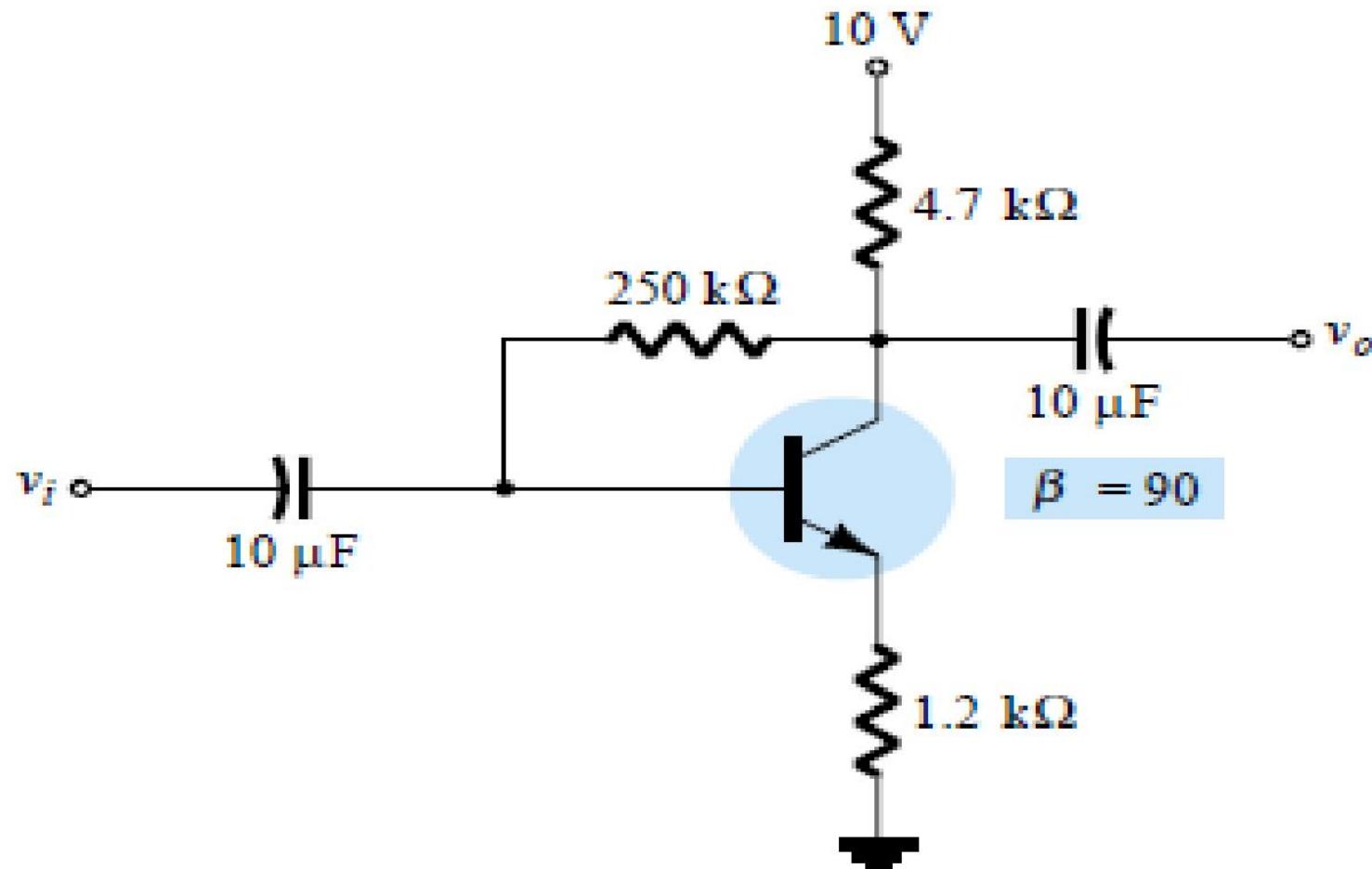
$$I_{C_{\text{sat}}} = I_{C_{\text{max}}} = \frac{V_{CC}}{R_C + R_E}$$

LOAD LINE ANALYSIS

Continuing with the approximation $I'_C = I_C$ will result in the same load line defined for the voltage-divider and emitter-biased configurations. The level of I_{B_Q} will be defined by the chosen bias configuration.

EXAMPLE 4

Determine the quiescent levels of I_{C_O} and V_{CE_O} for the network of Fig.



SOLUTION

$$\begin{aligned}I_B &= \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} \\&= \frac{10 \text{ V} - 0.7 \text{ V}}{250 \text{ k}\Omega + (90)(4.7 \text{ k}\Omega + 1.2 \text{ k}\Omega)} \\&= \frac{9.3 \text{ V}}{250 \text{ k}\Omega + 531 \text{ k}\Omega} = \frac{9.3 \text{ V}}{781 \text{ k}\Omega} \\&= 11.91 \text{ }\mu\text{A}\end{aligned}$$

$$\begin{aligned}I_{CQ} &= \beta I_B = (90)(11.91 \text{ }\mu\text{A}) \\&= 1.07 \text{ mA}\end{aligned}$$

$$\begin{aligned}V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\&= 10 \text{ V} - (1.07 \text{ mA})(4.7 \text{ k}\Omega + 1.2 \text{ k}\Omega) \\&= 10 \text{ V} - 6.31 \text{ V} \\&= 3.69 \text{ V}\end{aligned}$$

EXAMPLE 5

Repeat the same example with Beta = 135

SOLUTION

$$\begin{aligned} I_B &= \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \\ &\frac{10 \text{ V} - 0.7 \text{ V}}{250 \text{ k}\Omega + (135)(4.7 \text{ k}\Omega + 1.2 \text{ k}\Omega)} \\ &= \frac{9.3 \text{ V}}{250 \text{ k}\Omega + 796.5 \text{ k}\Omega} = \frac{9.3 \text{ V}}{1046.5 \text{ k}\Omega} \\ &= 8.89 \mu\text{A} \end{aligned}$$

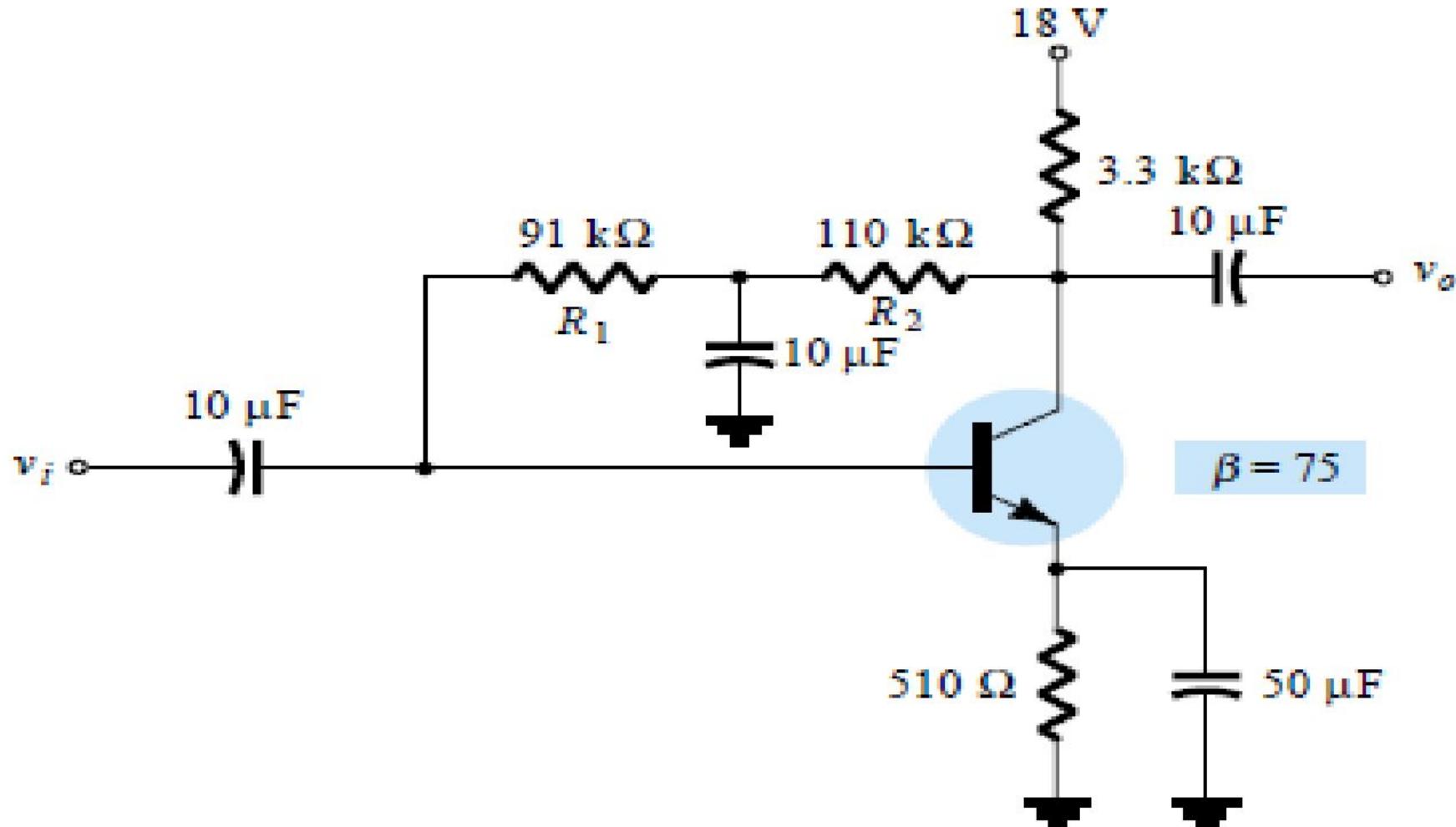
$$\begin{aligned} I_{CQ} &= \beta I_B \\ &= (135)(8.89 \mu\text{A}) \\ &= 1.2 \text{ mA} \end{aligned}$$

$$\begin{aligned} V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\ &= 10 \text{ V} - (1.2 \text{ mA})(4.7 \text{ k}\Omega + 1.2 \text{ k}\Omega) \\ &= 10 \text{ V} - 7.08 \text{ V} \\ &= 2.92 \text{ V} \end{aligned}$$

Even though the level of β increased 50%, the level of I_{C_Q} only increased 12.1% while the level of V_{CE_Q} decreased about 20.9%. If the network were a fixed-bias design, a 50% increase in β would have resulted in a 50% increase in I_{C_Q} and a dramatic change in the location of the Q -point.

EXTRA NUMERICAL

Determine the dc level of I_B and V_C for the network of Fig.



SOLUTION

$$\begin{aligned}I_B &= \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} \\&= \frac{18 \text{ V} - 0.7 \text{ V}}{(91 \text{ k}\Omega + 110 \text{ k}\Omega) + (75)(3.3 \text{ k}\Omega + 0.51 \text{ k}\Omega)} \\&= \frac{17.3 \text{ V}}{201 \text{ k}\Omega + 285.75 \text{ k}\Omega} = \frac{17.3 \text{ V}}{486.75 \text{ k}\Omega} \\&= 35.5 \mu\text{A}\end{aligned}$$

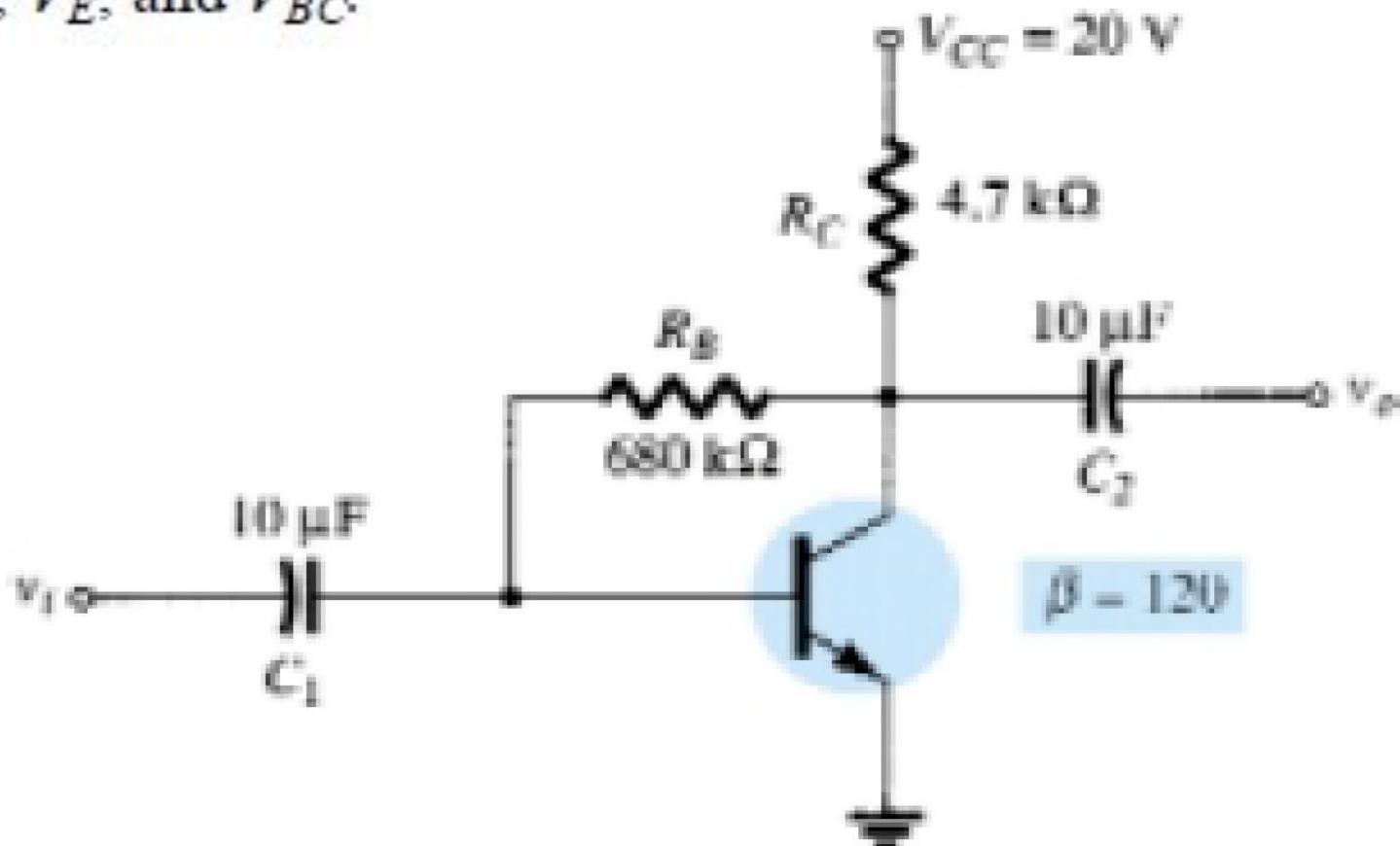
$$\begin{aligned}I_C &= \beta I_B \\&= (75)(35.5 \mu\text{A}) \\&= 2.66 \text{ mA}\end{aligned}$$

$$\begin{aligned}V_C &= V_{CC} - I'_C R_C \cong V_{CC} - I_C R_C \\&= 18 \text{ V} - (2.66 \text{ mA})(3.3 \text{ k}\Omega) \\&= 18 \text{ V} - 8.78 \text{ V} \\&= 9.22 \text{ V}\end{aligned}$$

EXAMPLE

For the network of Fig.

- Determine I_{C_Q} and V_{CEQ} .
- Find V_B , V_C , V_E , and V_{BC} .



SOLUTION

The absence of R_E reduces the reflection of resistive levels to simply that of R_C and the equation for I_B reduces to

$$\begin{aligned}I_B &= \frac{V_{CC} - V_{BE}}{R_B + \beta R_C} \\&= \frac{20 \text{ V} - 0.7 \text{ V}}{680 \text{ k}\Omega + (120)(4.7 \text{ k}\Omega)} = \frac{19.3 \text{ V}}{1.244 \text{ M}\Omega} \\&= 15.51 \text{ }\mu\text{A}\end{aligned}$$

$$\begin{aligned}I_{CQ} &= \beta I_B = (120)(15.51 \text{ }\mu\text{A}) \\&= 1.86 \text{ mA}\end{aligned}$$

$$\begin{aligned}V_{CEQ} &= V_{CC} - I_C R_C \\&= 20 \text{ V} - (1.86 \text{ mA})(4.7 \text{ k}\Omega) \\&= 11.26 \text{ V}\end{aligned}$$

$$V_B = V_{BE} = 0.7 \text{ V}$$

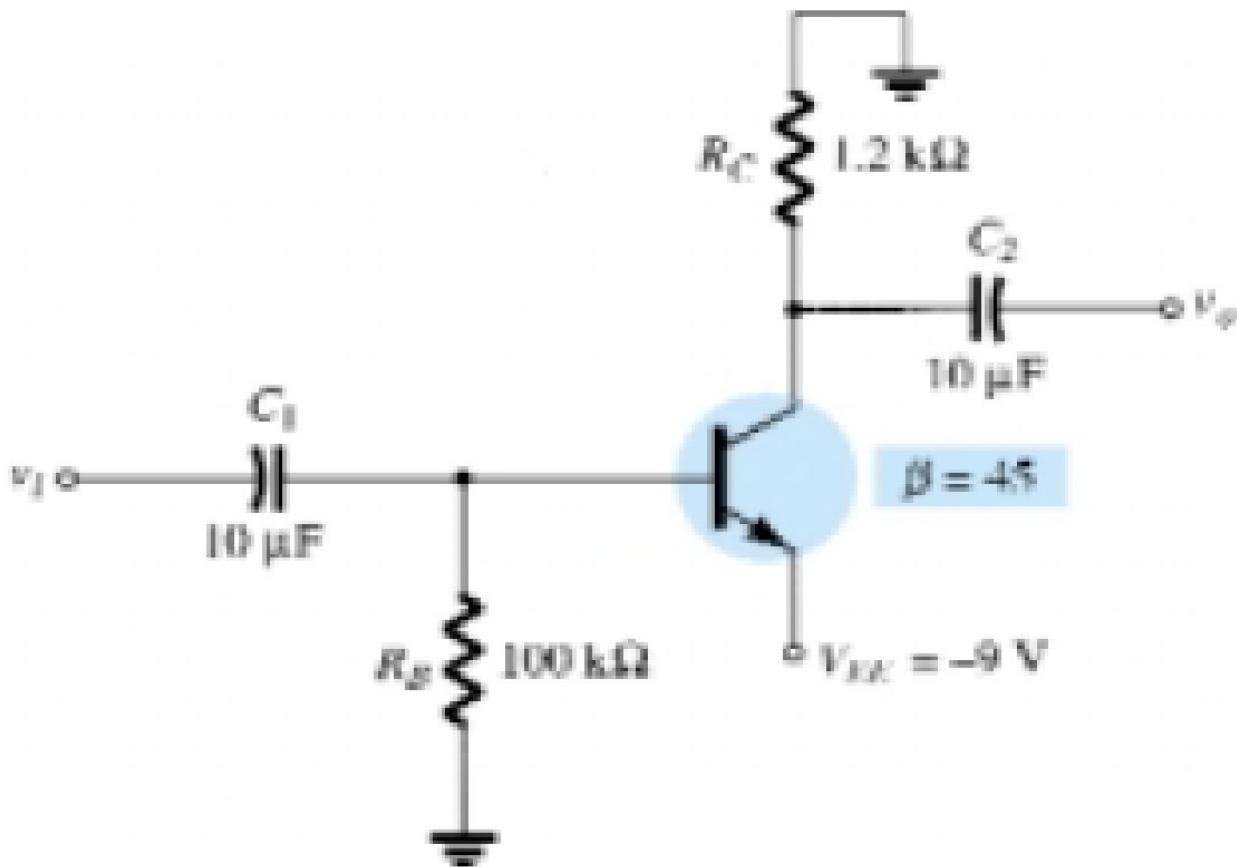
$$V_C = V_{CE} = 11.26 \text{ V}$$

$$V_E = 0 \text{ V}$$

$$\begin{aligned}V_{BC} &= V_B - V_C = 0.7 \text{ V} - 11.26 \text{ V} \\&= -10.56 \text{ V}\end{aligned}$$

EXAMPLE

Determine V_C and V_B for the network of Fig.



SOLUTION

Applying Kirchhoff's voltage law in the clockwise direction for the base-emitter loop will result in

$$-I_B R_B - V_{BE} + V_{EE} = 0$$

and

$$I_B = \frac{V_{EE} - V_{BE}}{R_B}$$

$$\begin{aligned} I_B &= \frac{9 \text{ V} - 0.7 \text{ V}}{100 \text{ k}\Omega} \\ &= \frac{8.3 \text{ V}}{100 \text{ k}\Omega} \\ &= 83 \text{ }\mu\text{A} \end{aligned}$$

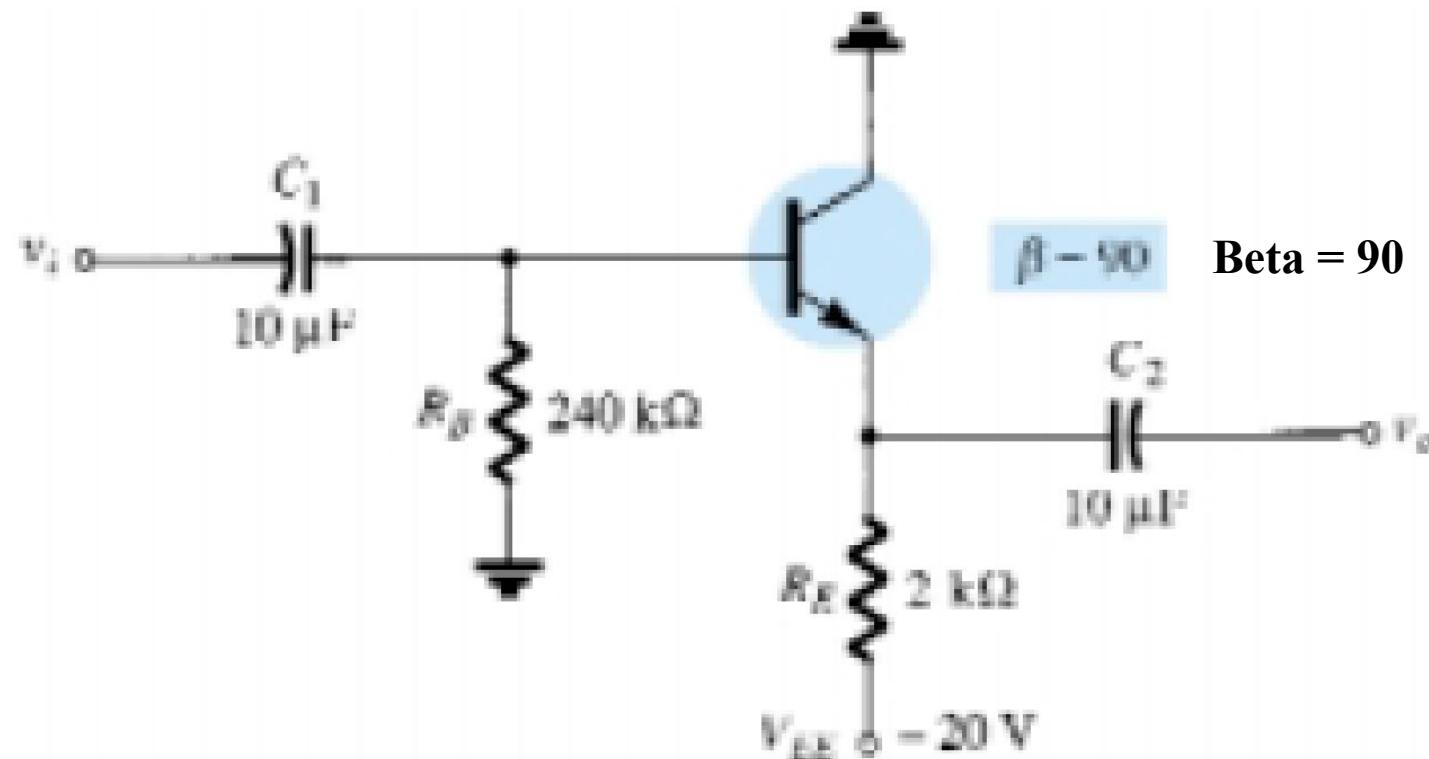
$$\begin{aligned} I_C &= \beta I_B \\ &= (45)(83 \text{ }\mu\text{A}) \\ &= 3.735 \text{ mA} \end{aligned}$$

$$\begin{aligned} V_C &= -I_C R_C \\ &= -(3.735 \text{ mA})(1.2 \text{ k}\Omega) \\ &= -4.48 \text{ V} \end{aligned}$$

$$\begin{aligned} V_B &= -I_B R_B \\ &= -(83 \text{ }\mu\text{A})(100 \text{ k}\Omega) \\ &= -8.3 \text{ V} \end{aligned}$$

EXAMPLE

Determine V_{CEQ} and I_E for the network of Fig.



SOLUTION

Applying Kirchhoff's voltage law to the input circuit will result in

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

but

$$I_E = (\beta + 1)I_B$$

and

$$V_{EE} - V_{BE} - (\beta + 1)I_B R_E - I_B R_B = 0$$

with

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$I_B = \frac{20 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega + (91)(2 \text{ k}\Omega)}$$

$$= \frac{19.3 \text{ V}}{240 \text{ k}\Omega + 182 \text{ k}\Omega} = \frac{19.3 \text{ V}}{422 \text{ k}\Omega}$$

$$= 45.73 \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (90)(45.73 \mu\text{A})$$

$$= 4.12 \text{ mA}$$

Applying Kirchhoff's voltage law to the output circuit, we have

$$-V_{EE} + I_E R_E + V_{CE} = 0$$

but

$$I_E = (\beta + 1)I_B$$

and

$$V_{CE_Q} = V_{EE} - (\beta + 1)I_B R_E$$

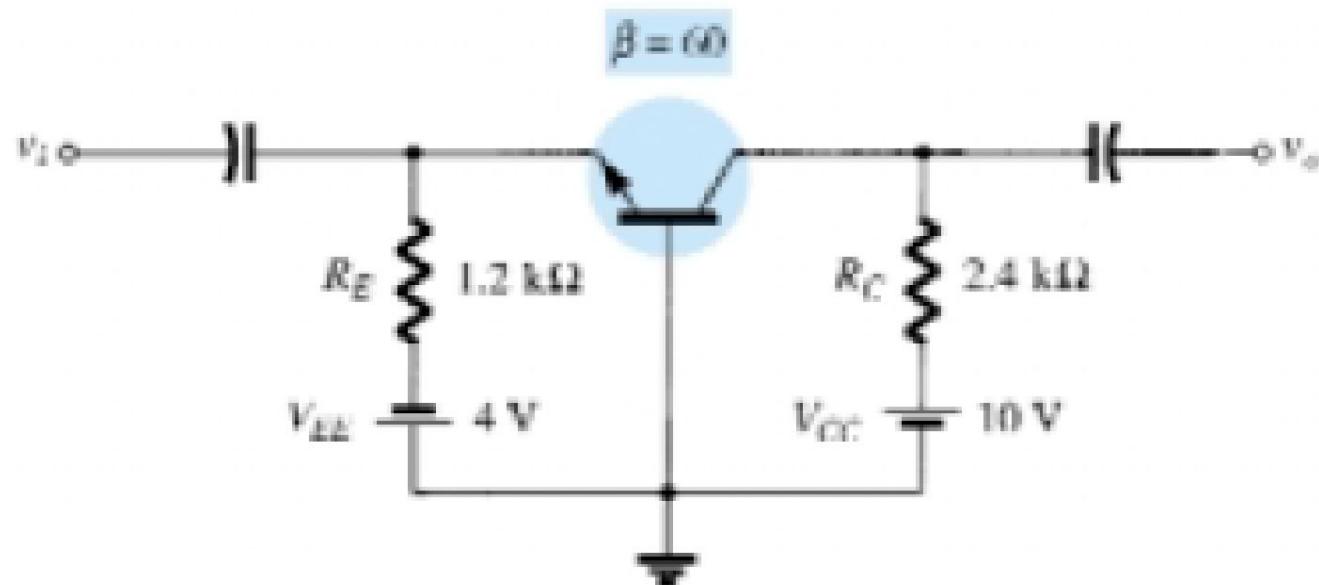
$$= 20 \text{ V} - (91)(45.73 \mu\text{A})(2 \text{ k}\Omega)$$

$$= 11.68 \text{ V}$$

$$I_E = 4.16 \text{ mA}$$

EXAMPLE

Determine the voltage V_{CB} and the current I_B for the common-base configuration of Fig.



SOLUTION

Applying Kirchhoff's voltage law to the input circuit yields

$$-V_{EE} + I_E R_E + V_{BE} = 0$$

and

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

Substituting values, we obtain

$$I_E = \frac{4 \text{ V} - 0.7 \text{ V}}{1.2 \text{ k}\Omega} = 2.75 \text{ mA}$$

Applying Kirchhoff's voltage law to the output circuit gives

$$-V_{CB} + I_C R_C - V_{CC} = 0$$

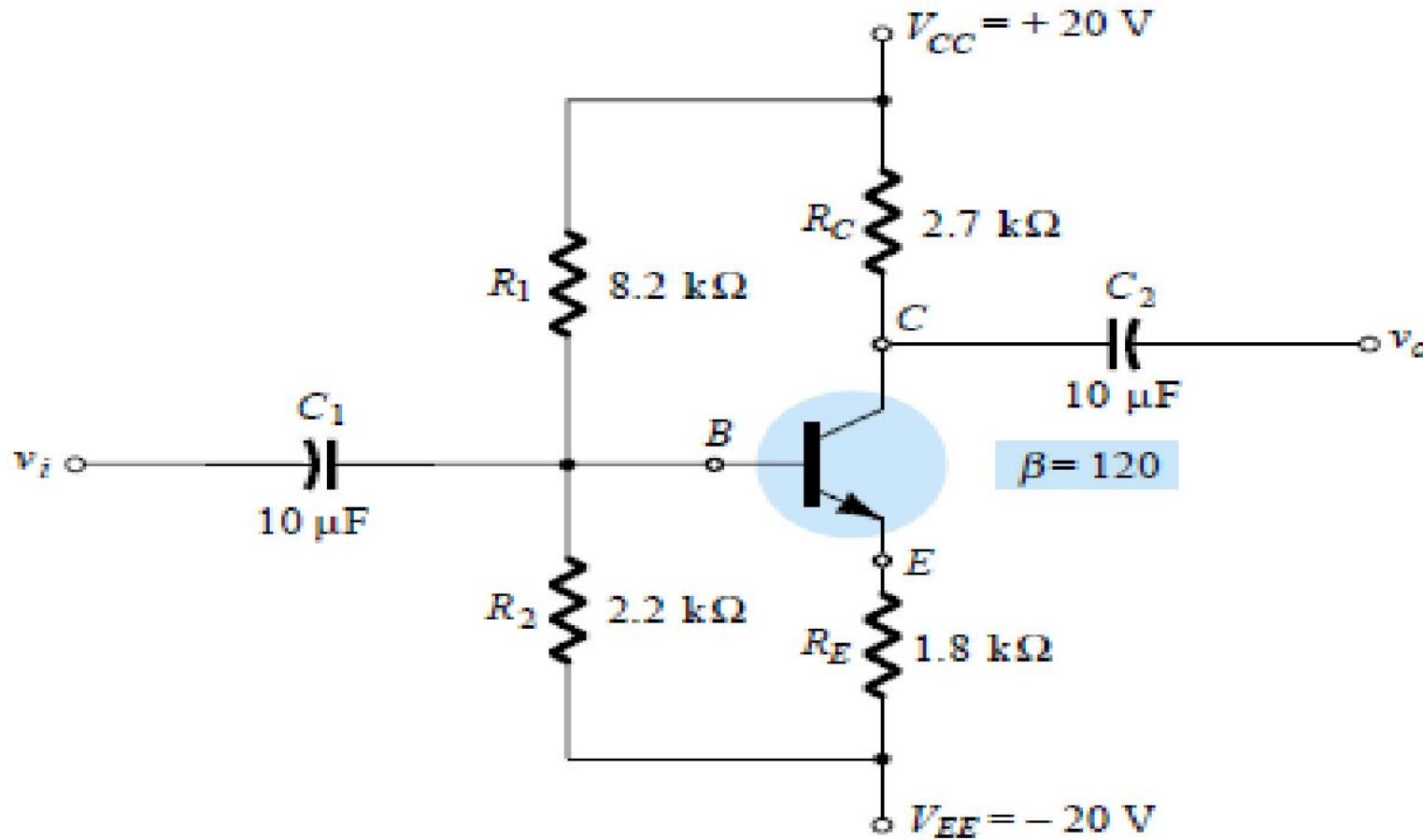
and

$$\begin{aligned} V_{CB} &= V_{CC} - I_C R_C \text{ with } I_C \cong I_E \\ &= 10 \text{ V} - (2.75 \text{ mA})(2.4 \text{ k}\Omega) \\ &= 3.4 \text{ V} \end{aligned}$$

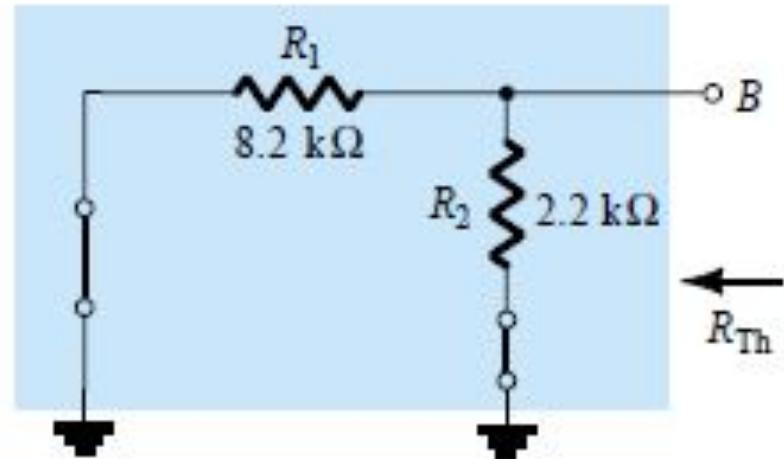
$$\begin{aligned} I_B &= \frac{I_C}{\beta} \\ &= \frac{2.75 \text{ mA}}{60} \\ &= 45.8 \mu\text{A} \end{aligned}$$

EXAMPLE

Determine V_C and V_B for the network of Fig.

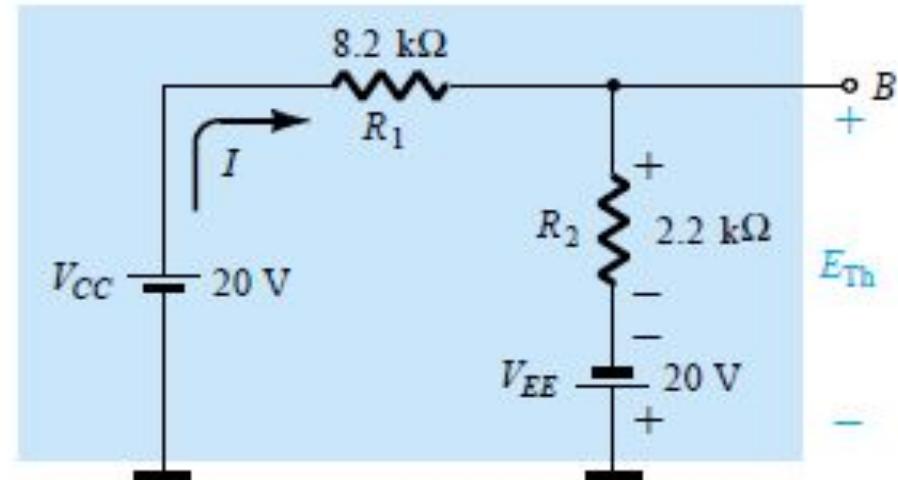


SOLUTION



Determining R_{Th} :

$$R_{Th} = 8.2 \text{ k}\Omega \parallel 2.2 \text{ k}\Omega = 1.73 \text{ k}\Omega$$



Determining E_{Th} :

$$I = \frac{V_{CC} + V_{EE}}{R_1 + R_2} = \frac{20 \text{ V} + 20 \text{ V}}{8.2 \text{ k}\Omega + 2.2 \text{ k}\Omega} = \frac{40 \text{ V}}{10.4 \text{ k}\Omega}$$

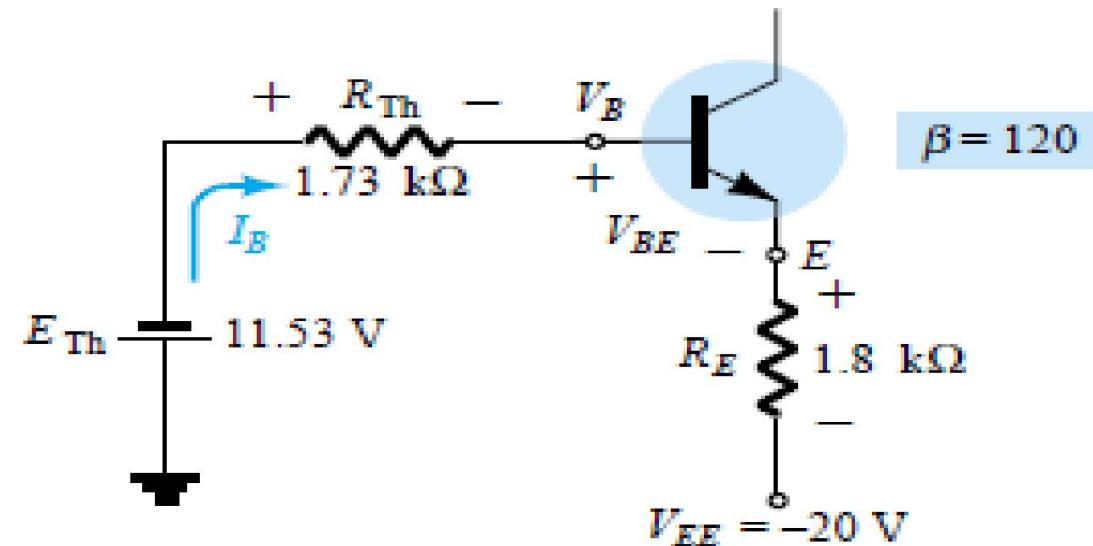
$$= 3.85 \text{ mA}$$

$$E_{Th} = IR_2 - V_{EE}$$

$$= (3.85 \text{ mA})(2.2 \text{ k}\Omega) - 20 \text{ V}$$

$$= -11.53 \text{ V}$$

SOLUTION CONTINUED..



The network can then be redrawn as shown in Fig. 4.46, where the application of Kirchhoff's voltage law will result in

$$-E_{\text{Th}} - I_B R_{\text{Th}} - V_{BE} - I_E R_E + V_{EE} = 0$$

Substituting $I_E = (\beta + 1)I_B$ gives

$$V_{EE} - E_{\text{Th}} - V_{BE} - (\beta + 1)I_B R_E - I_B R_{\text{Th}} = 0$$

and

$$I_B = \frac{V_{EE} - E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E}$$

SOLUTION CONTINUED..

$$\begin{aligned}I_B &= \frac{V_{EE} - E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} \\&= \frac{20 \text{ V} - 11.53 \text{ V} - 0.7 \text{ V}}{1.73 \text{ k}\Omega + (121)(1.8 \text{ k}\Omega)} \\&= \frac{7.77 \text{ V}}{219.53 \text{ k}\Omega} \\&= 35.39 \text{ }\mu\text{A}\end{aligned}$$

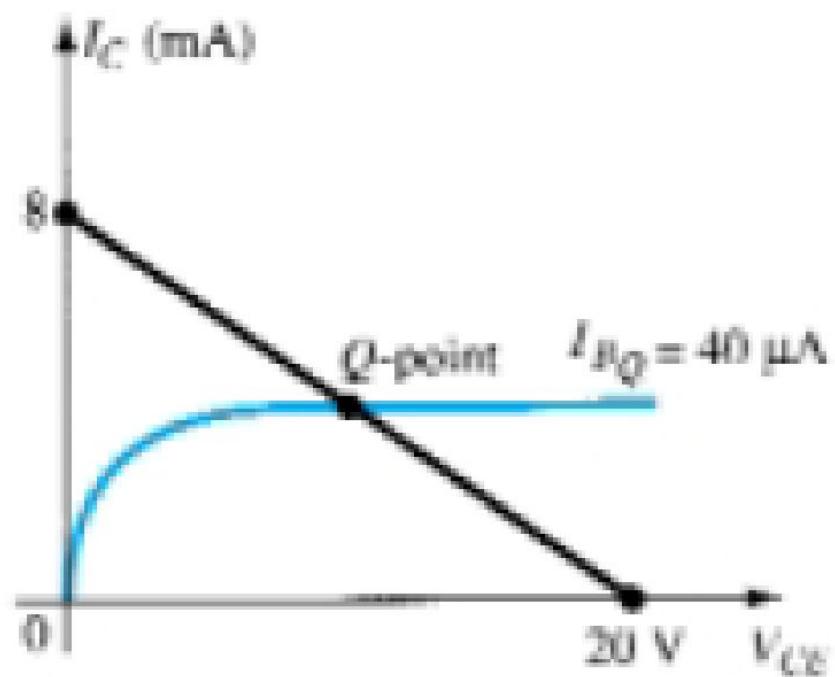
$$\begin{aligned}I_C &= \beta I_B \\&= (120)(35.39 \text{ }\mu\text{A}) \\&= 4.25 \text{ mA}\end{aligned}$$

$$\begin{aligned}V_C &= V_{CC} - I_C R_C \\&= 20 \text{ V} - (4.25 \text{ mA})(2.7 \text{ k}\Omega) \\&= 8.53 \text{ V} \\V_B &= -E_{Th} - I_B R_{Th} \\&= -(11.53 \text{ V}) - (35.39 \text{ }\mu\text{A})(1.73 \text{ k}\Omega) \\&= -11.59 \text{ V}\end{aligned}$$

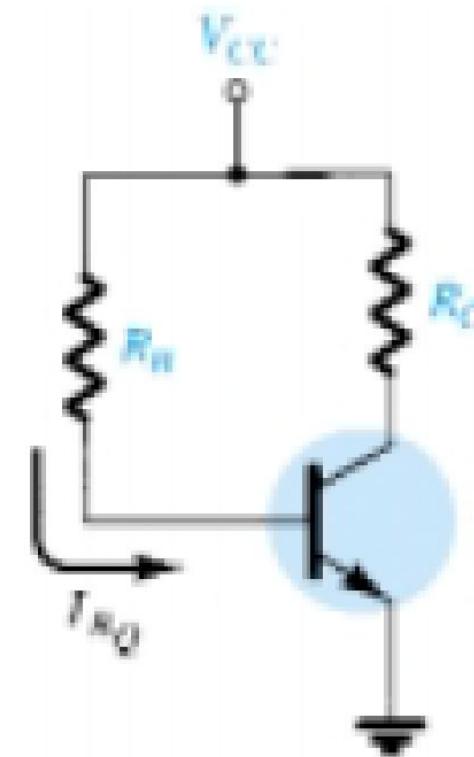
DESIGN PROBLEMS

EXAMPLE

Given the device characteristics of Fig. a, determine V_{CC} , R_B , and R_C for the fixed-bias configuration of Fig. b.



(a)



(b)

SOLUTION

From the load line

$$V_{CC} = 20 \text{ V}$$

$$I_C = \frac{V_{CC}}{R_C} \Big|_{V_{CE} = 0 \text{ V}}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{8 \text{ mA}} = 2.5 \text{ k}\Omega$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$\begin{aligned} &= \frac{20 \text{ V} - 0.7 \text{ V}}{40 \text{ }\mu\text{A}} = \frac{19.3 \text{ V}}{40 \text{ }\mu\text{A}} \\ &= 482.5 \text{ k}\Omega \end{aligned}$$

SOLUTION CONTINUED..

Standard resistor values:

$$R_C = 2.4 \text{ k}\Omega$$

$$R_B = 470 \text{ k}\Omega$$

Using standard resistor values gives

$$I_B = 41.1 \mu\text{A}$$

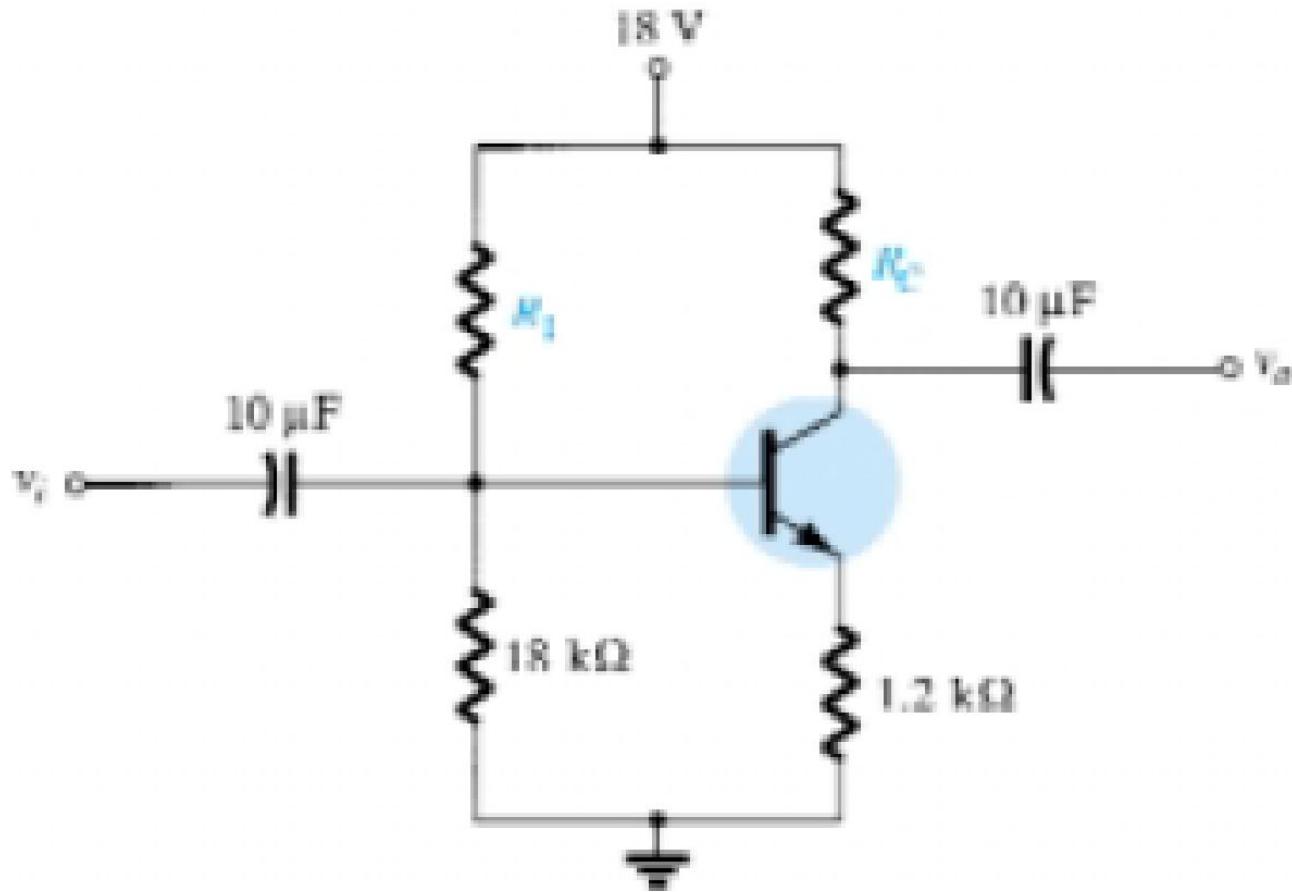
which is well within 5% of the value specified.

Standard Resistor Values (-5%)

1	10	100	1.0K	10K	100K	1.0M
1.1	11	110	1.1K	11K	110K	1.1M
1.2	12	120	1.2K	12K	120K	1.2M
1.3	13	130	1.3K	13K	130K	1.3M
1.5	15	150	1.5K	15K	150K	1.5M
1.6	16	160	1.6K	16K	160K	1.6M
1.8	18	180	1.8K	18K	180K	1.8M
2	20	200	2.0K	20K	200K	2.0M
2.2	22	220	2.2K	22K	220K	2.2M
2.4	24	240	2.4K	24K	240K	2.4M
2.7	27	270	2.7K	27K	270K	2.7M
3	30	300	3.0K	30K	300K	3.0M
3.3	33	330	3.3K	33K	330K	3.3M
3.6	36	360	3.6K	36K	360K	3.6M
3.9	39	390	3.9K	39K	390K	3.9M
4.3	43	430	4.3K	43K	430K	4.3M
4.7	47	470	4.7K	47K	470K	4.7M
5.1	51	510	5.1K	51K	510K	5.1M
5.6	56	560	5.6K	56K	560K	5.6M
6.2	62	620	6.2K	62K	620K	6.2M
6.8	68	680	6.8K	68K	680K	6.8M
7.5	75	750	7.5K	75K	750K	7.5M
8.2	82	820	8.2K	82K	820K	8.2M
9.1	91	910	9.1K	91K	910K	9.1M

EXAMPLE

Given that $I_{CQ} = 2 \text{ mA}$ and $V_{CEQ} = 10 \text{ V}$, determine R_1 and R_C for the network of Fig.



SOLUTION

$$V_E = I_E R_E \cong I_C R_E$$

$$= (2 \text{ mA})(1.2 \text{ k}\Omega) = 2.4 \text{ V}$$

$$V_B = V_{BE} + V_E = 0.7 \text{ V} + 2.4 \text{ V} = 3.1 \text{ V}$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = 3.1 \text{ V}$$

$$\frac{(18 \text{ k}\Omega)(18 \text{ V})}{R_1 + 18 \text{ k}\Omega} = 3.1 \text{ V}$$

$$324 \text{ k}\Omega = 3.1R_1 + 55.8 \text{ k}\Omega$$

$$3.1R_1 = 268.2 \text{ k}\Omega$$

$$R_1 = \frac{268.2 \text{ k}\Omega}{3.1} = 86.52 \text{ k}\Omega$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_C}{I_C}$$

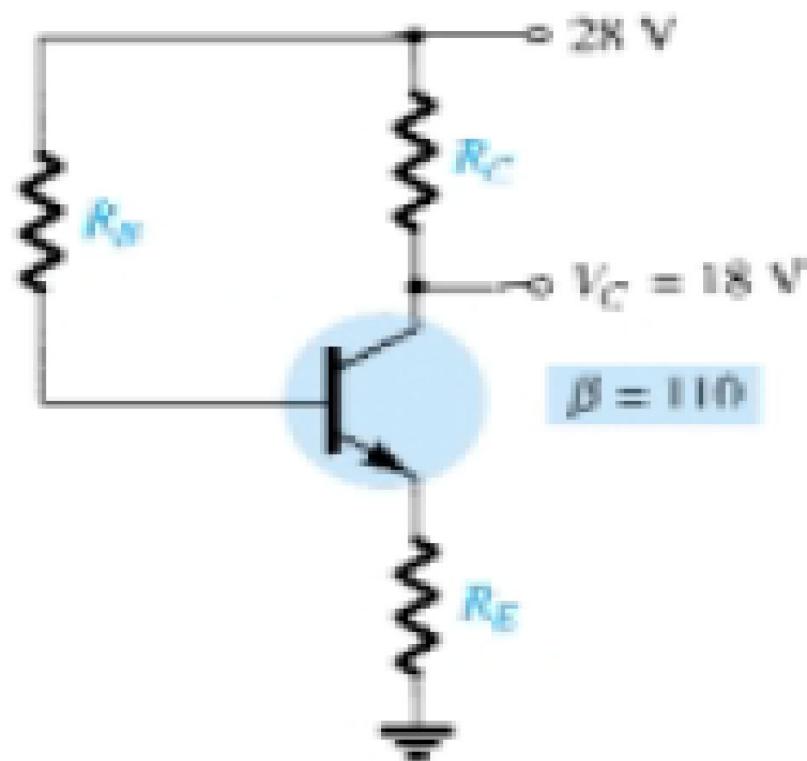
$$V_C = V_{CE} + V_E = 10 \text{ V} + 2.4 \text{ V} = 12.4 \text{ V}$$

$$R_C = \frac{18 \text{ V} - 12.4 \text{ V}}{2 \text{ mA}}$$
$$= 2.8 \text{ k}\Omega$$

The nearest standard commercial values to R_1 are 82 and 91 k Ω . However, using the series combination of standard values of 82 k Ω and 4.7 k Ω = 86.7 k Ω would result in a value very close to the design level.

EXAMPLE

The emitter-bias configuration of Fig. has the following specifications: $I_{CQ} = \frac{1}{2}I_{C_{\text{sat}}}$, $I_{C_{\text{sat}}} = 8 \text{ mA}$, $V_C = 18 \text{ V}$, and $\beta = 110$. Determine R_C , R_E , and R_B . Beta = 110



SOLUTION

$$I_{C_Q} = \frac{1}{2} I_{C_{sat}} = 4 \text{ mA}$$

$$R_C = \frac{V_{R_C}}{I_{C_Q}} = \frac{V_{CC} - V_C}{I_{C_Q}}$$
$$= \frac{28 \text{ V} - 18 \text{ V}}{4 \text{ mA}} = 2.5 \text{ k}\Omega$$

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

$$R_C + R_E = \frac{V_{CC}}{I_{C_{sat}}} = \frac{28 \text{ V}}{8 \text{ mA}} = 3.5 \text{ k}\Omega$$

$$R_E = 3.5 \text{ k}\Omega - R_C$$
$$= 3.5 \text{ k}\Omega - 2.5 \text{ k}\Omega$$
$$= 1 \text{ k}\Omega$$

$$I_{B_Q} = \frac{I_{C_Q}}{\beta} = \frac{4 \text{ mA}}{110} = 36.36 \mu\text{A}$$

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$R_B + (\beta + 1)R_E = \frac{V_{CC} - V_{BE}}{I_{B_Q}}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_{B_Q}} - (\beta + 1)R_E$$

$$= \frac{28 \text{ V} - 0.7 \text{ V}}{36.36 \mu\text{A}} - (111)(1 \text{ k}\Omega)$$

$$= \frac{27.3 \text{ V}}{36.36 \mu\text{A}} - 111 \text{ k}\Omega$$

$$= 750 \text{ k}\Omega$$

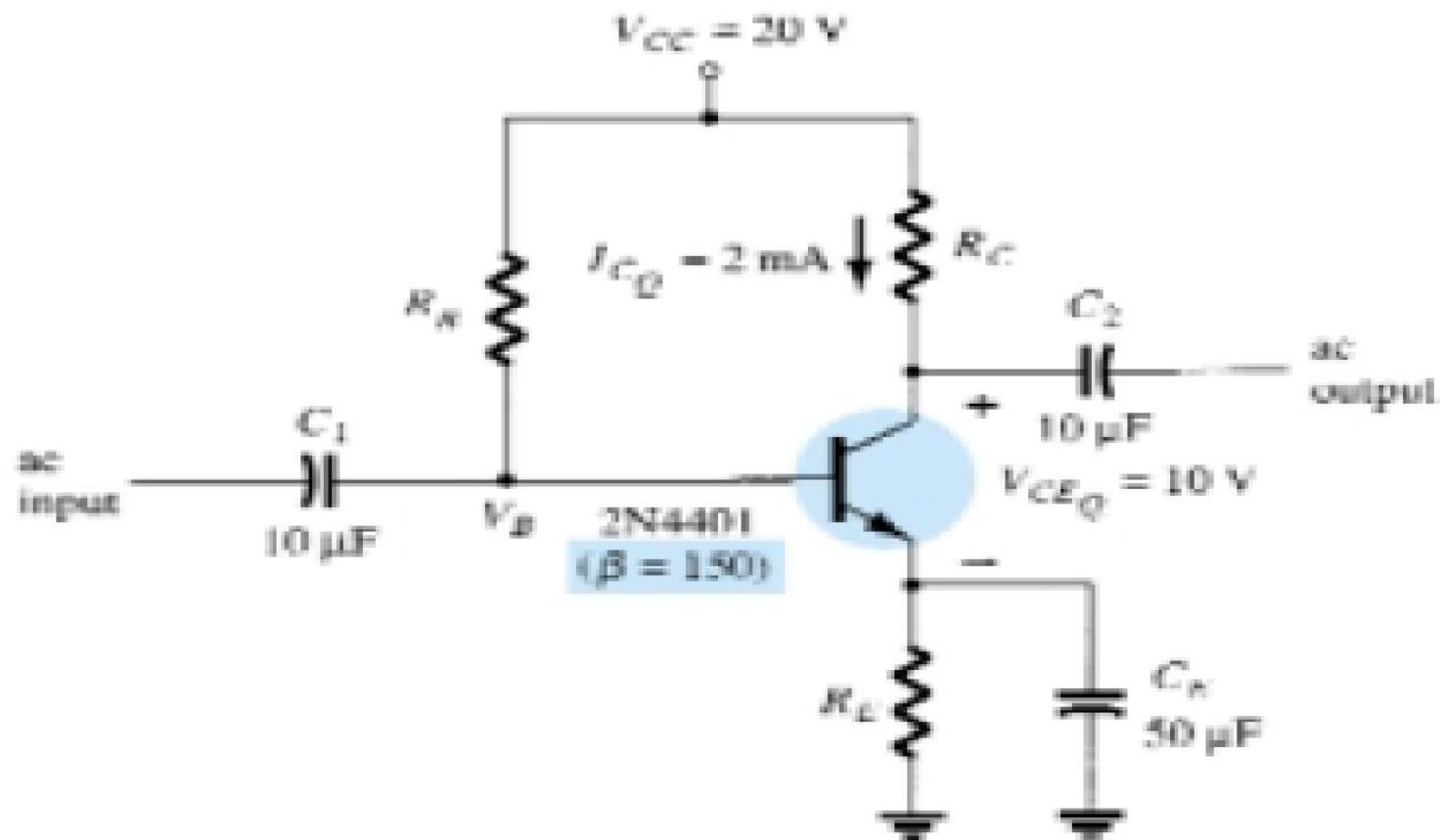
$$R_C = 2.4 \text{ k}\Omega$$

$$R_E = 1 \text{ k}\Omega$$

$$R_B = 620 \text{ k}\Omega$$

EXAMPLE

Determine the resistor values for the network of Fig. for the indicated operating point and supply voltage.



SOLUTION

$$V_E = \frac{1}{10}V_{CC} = \frac{1}{10}(20 \text{ V}) = 2 \text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2 \text{ V}}{2 \text{ mA}} = 1 \text{ k}\Omega$$

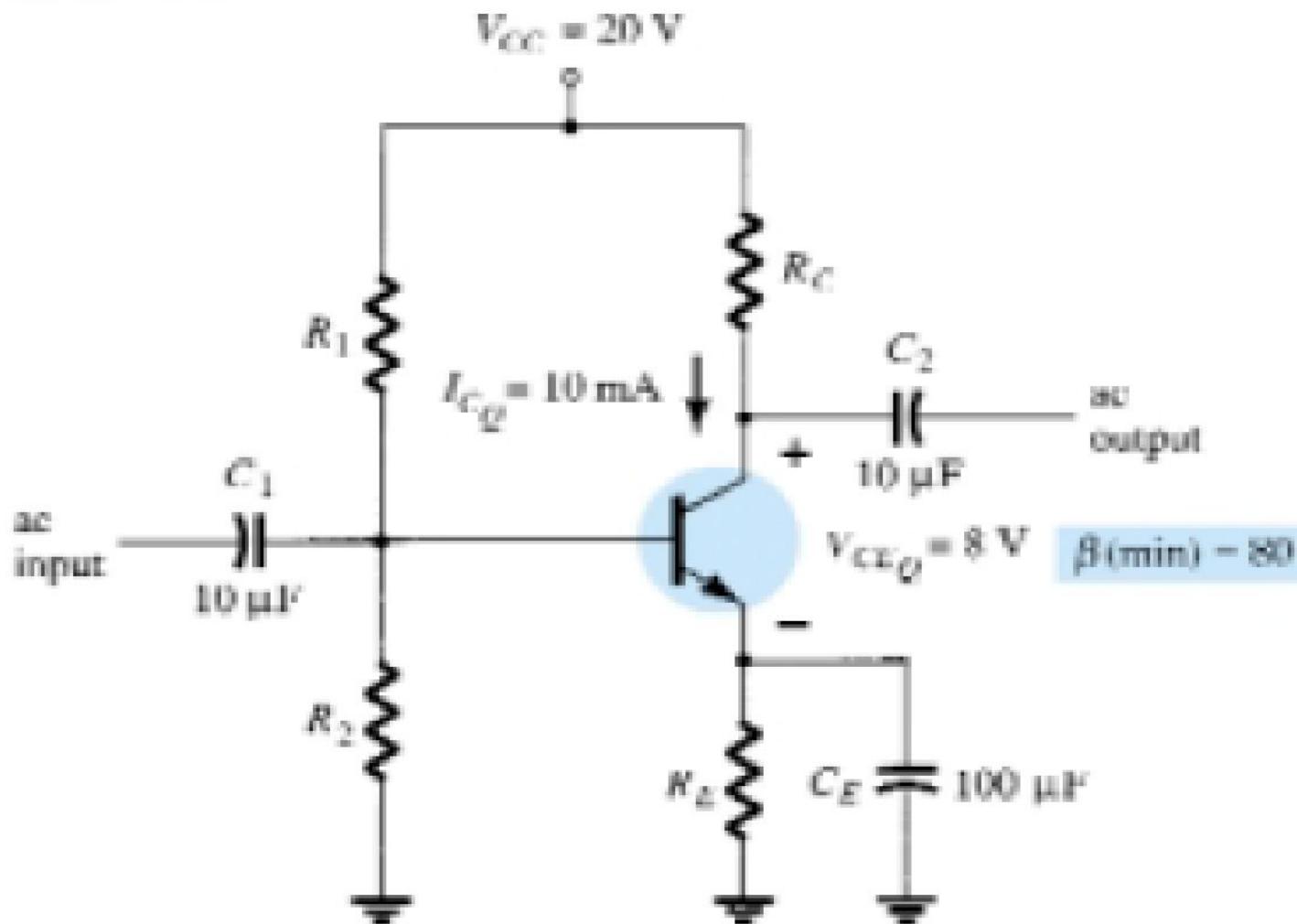
$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20 \text{ V} - 10 \text{ V} - 2 \text{ V}}{2 \text{ mA}} = \frac{8 \text{ V}}{2 \text{ mA}}$$
$$= 4 \text{ k}\Omega$$

$$I_B = \frac{I_C}{\beta} = \frac{2 \text{ mA}}{150} = 13.33 \text{ }\mu\text{A}$$

$$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V} - 2 \text{ V}}{13.33 \text{ }\mu\text{A}}$$
$$\cong 1.3 \text{ M}\Omega$$

EXAMPLE

Determine the levels of R_C , R_E , R_1 , and R_2 for the network of Fig. for the operating point indicated.



SOLUTION

$$V_E = \frac{1}{10}V_{CC} = \frac{1}{10}(20 \text{ V}) = 2 \text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2 \text{ V}}{10 \text{ mA}} = 200 \Omega$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C}$$

$$= \frac{20 \text{ V} - 8 \text{ V} - 2 \text{ V}}{10 \text{ mA}} = \frac{10 \text{ V}}{10 \text{ mA}}$$

$$= 1 \text{ k}\Omega$$

$$V_B = V_{BE} + V_E = 0.7 \text{ V} + 2 \text{ V} = 2.7 \text{ V}$$

$$R_2 \leq \frac{1}{10}\beta R_E$$

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$\begin{aligned} R_2 &\leq \frac{1}{10}(80)(0.2 \text{ k}\Omega) \\ &= 1.6 \text{ k}\Omega \end{aligned}$$

$$V_B = 2.7 \text{ V} = \frac{(1.6 \text{ k}\Omega)(20 \text{ V})}{R_1 + 1.6 \text{ k}\Omega}$$

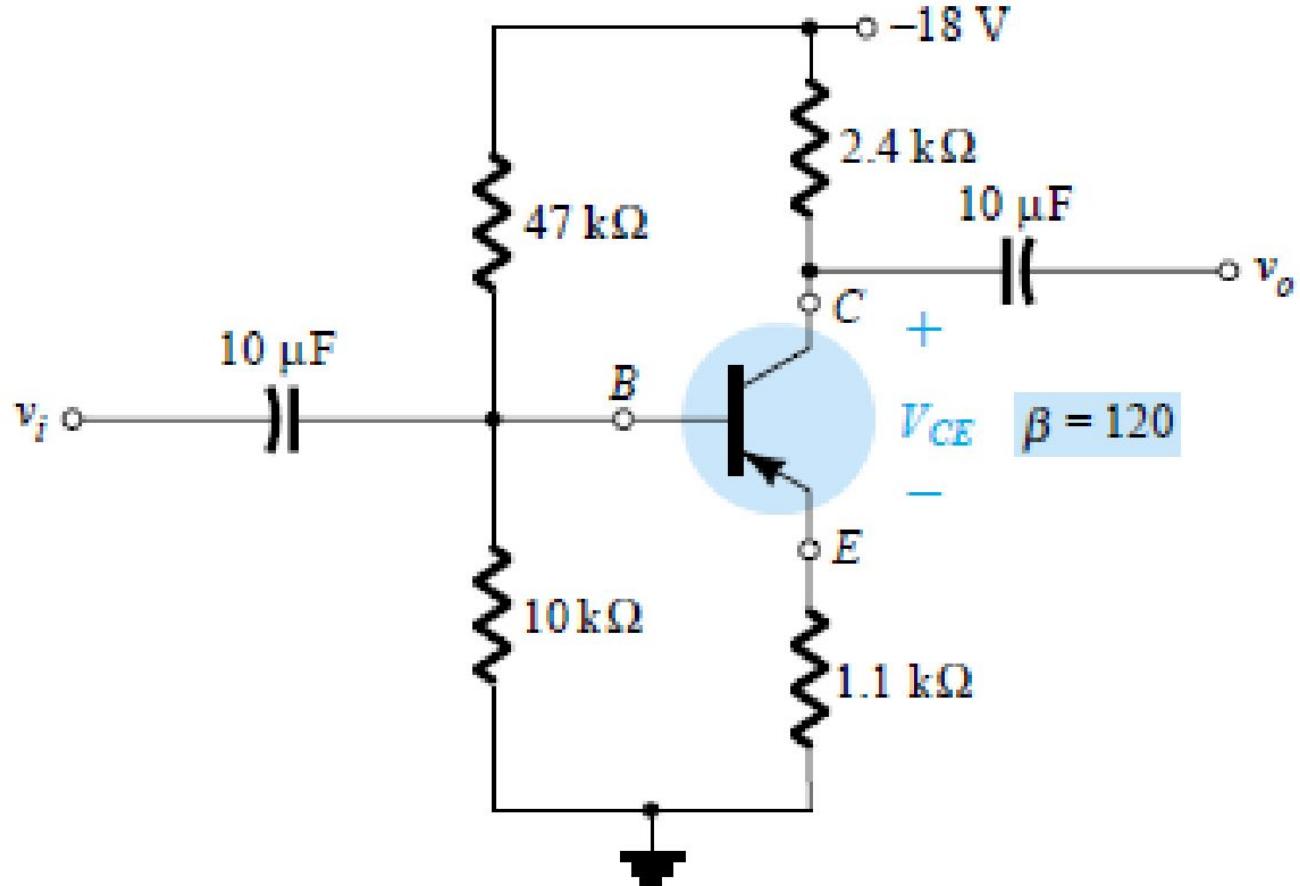
$$2.7R_1 + 4.32 \text{ k}\Omega = 32 \text{ k}\Omega$$

$$2.7R_1 = 27.68 \text{ k}\Omega$$

$$R_1 = 10.25 \text{ k}\Omega \quad (\text{use } 10 \text{ k}\Omega)$$

EXAMPLE ON PNP TRANSISTOR

Determine V_{CE} for the voltage-divider bias configuration of Fig.



SOLUTION

$$\beta R_E \geq 10R_2$$

$$(120)(1.1 \text{ k}\Omega) \geq 10(10 \text{ k}\Omega)$$

$$132 \text{ k}\Omega \geq 100 \text{ k}\Omega \text{ (satisfied)}$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(10 \text{ k}\Omega)(-18 \text{ V})}{47 \text{ k}\Omega + 10 \text{ k}\Omega} = -3.16 \text{ V}$$

Applying Kirchhoff's voltage law around the base-emitter loop yields

$$+V_B - V_{BE} - V_E = 0$$

$$V_E = V_B - V_{BE}$$

$$\begin{aligned} V_E &= -3.16 \text{ V} - (-0.7 \text{ V}) \\ &= -3.16 \text{ V} + 0.7 \text{ V} \\ &= -2.46 \text{ V} \end{aligned}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.46 \text{ V}}{1.1 \text{ k}\Omega} = 2.24 \text{ mA}$$

For the collector-emitter loop:

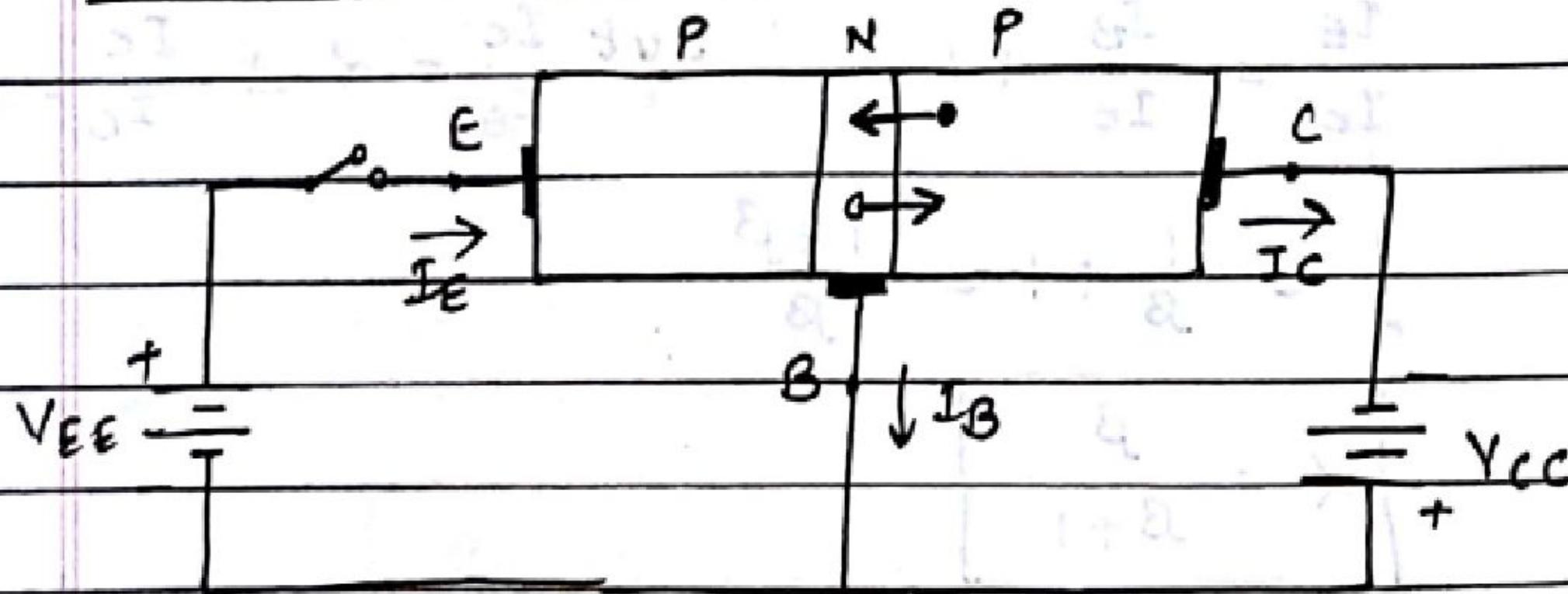
$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

Substituting $I_E \cong I_C$ and gathering terms, we have

$$V_{CE} = -V_{CC} + I_C(R_C + R_E)$$

$$\begin{aligned} V_{CE} &= -18 \text{ V} + (2.24 \text{ mA})(2.4 \text{ k}\Omega + 1.1 \text{ k}\Omega) \\ &= -18 \text{ V} + 7.84 \text{ V} \\ &= -10.16 \text{ V} \end{aligned}$$

* Leakage current in Common Base BJT -



- let switch 'S' be opened. It disconnects emitter from the base & hence the E-B junction of transistor is open circuited.

- Thus, there is no I_E . so there is no I_B or I_C . However it may noted that CB junction of transistor is reverse biased due to the holes injected from emitter. But this junction is forward biased due to the thermally generated minority carriers.
- The minority carriers diffuse across the CB junction & hence produce a certain value of current known as leakage current.
- This current is called leakage current from collector to base with emitter open & designated by I_{CBO} . It is also known as reverse saturation current or collector cut off current (I_{CO}).
- Thus I_{CBO} or I_{CO} is similar to reverse saturation current in PN junction.

- Total collector current

$$I_C = \alpha I_E + I_{CO}$$

$$\alpha = (I_C - I_{CO}) / I_E$$

but $I_E = I_B + I_C$

$$\alpha = \frac{I_C - I_{CO}}{(I_B + I_C)}$$

$$I_C = \alpha (I_B + I_C) + I_{CO}$$

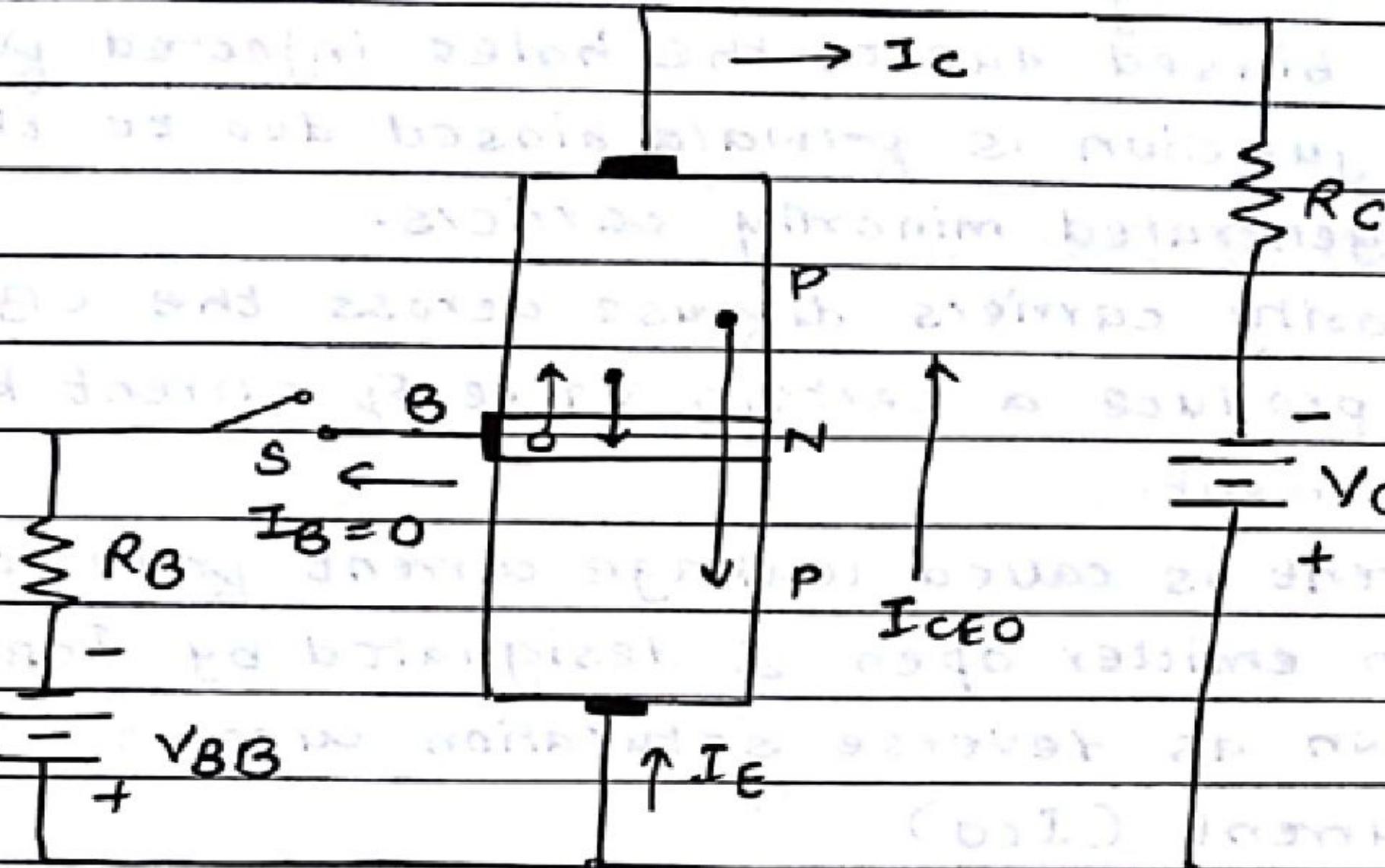
$$= \alpha I_B + \alpha I_C + I_{CO}$$

$$(1-\alpha) I_C = \alpha I_B + I_{CO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CO}}{1-\alpha}$$

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

* Leakage current in Common Emitter BJT :-



- If switch is open then base is disconnected from the emitter. Hence BE junction of transistor is open & $\therefore I_B$ is zero.

- Under this condition leakage current flows (through) from emitter to collector terminal. The current is designated as I_{CEO} .

- This leakage is not just due to the thermally generated carriers across the collector base junction but also due to movement of electrons across the base emitter junction.

$$\begin{aligned} \text{Total } I_{CEO} &= I_{CO} + \beta I_{CO} \\ &= (1 + \beta) I_{CO} \end{aligned}$$

$$\text{Total } I_C = \beta I_B + I_{CEO}$$

$$I_C = \beta I_B + (1 + \beta) I_{CO}$$

- This implies that leakage current in CE configuration is β times larger than CB transistor.

STABILITY FACTOR

The stability of a system is a measure of the sensitivity of a network to variations in its parameters. In any amplifier employing a transistor the collector current I_C is sensitive to each of the following parameters:

β : increases with increase in temperature

$|V_{BE}|$: decreases about 7.5 mV per degree Celsius ($^{\circ}\text{C}$) increase in temperature

I_{CO} (reverse saturation current): doubles in value for every 10°C increase in temperature

STABILITY FACTOR

Stability Factors, $S(I_{CO})$, $S(V_{BE})$, and $S(\beta)$

A stability factor, S , is defined for each of the parameters affecting bias stability as listed below:

$$S = S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}$$

$$S' = S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

$$S'' = S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

Derivation / Expression for the stability factor 's'

$$s = \frac{\Delta I_c}{\Delta I_{c0}} \quad | \text{constant } V_{BE} \text{ & } \beta_{dc}$$

For a CE configuration, we know that

$$\begin{aligned} I_c &= \beta_{dc} I_B + I_{cE0} \\ &= \beta_{dc} I_B + (1 + \beta_{dc}) I_{cB0} \end{aligned}$$

changes in I_c is given by

$$\Delta I_c = \beta_{dc} \Delta I_B + (1 + \beta_{dc}) \Delta I_{cB0}$$

dividing both the sides by ΔI_c ,

$$\frac{\Delta I_C}{\Delta I_c} = \beta_{dc} \left[\frac{\Delta I_B}{\Delta I_c} \right] + (1 + \beta_{dc}) \left[\frac{\Delta I_{CBO}}{\Delta I_c} \right]$$

$$1 - \beta_{dc} \left[\frac{\Delta I_B}{\Delta I_c} \right] = (1 + \beta_{dc}) \left[\frac{\Delta I_{CBO}}{\Delta I_c} \right]$$

$$\therefore \frac{\Delta I_{CBO}}{\Delta I_c} = \frac{1 - \beta_{dc} \left[\frac{\Delta I_B}{\Delta I_c} \right]}{(1 + \beta_{dc})}$$

But $s = \frac{\Delta I_c}{\Delta I_{CBO}}$

$$\therefore s = \frac{(1 + \beta_{dc})}{1 - \beta_{dc} \left[\frac{\Delta I_B}{\Delta I_c} \right]}$$

STABILITY FACTOR FOR FIXED BIAS

For Fixed Bias ckt,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

BUT V_{CC} , V_{BE} & R_B all
are fixed, so I_B cannot
change.

$\therefore \Delta I_B = 0$ put in eqⁿ(1),

$$S = (1 + \beta_{dc})$$

- for fixed Bias config.

Expression for stability factor 's' for fixed Bias -

$$s' = \left| \frac{\partial I_C}{\partial V_{BE}} \right| \text{ const } I_{C0} \& \beta_{dc}$$

we know for CE,

$$I_C = \beta_{dc} I_B + (1 + \beta_{dc}) I_{C0} \quad \text{--- (1)}$$

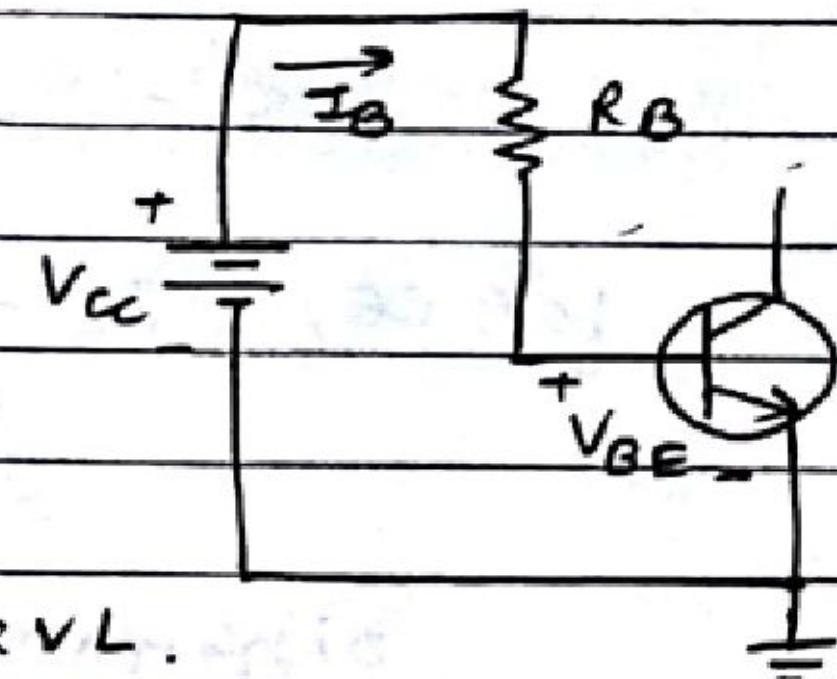
we need to put value of I_B ,

which we can get by applying KVL.

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \text{Put in eqn (1)}$$

$$I_C = \beta_{dc} \left[\frac{V_{CC} - V_{BE}}{R_B} \right] + (1 + \beta_{dc}) I_{C0}$$



$$I_c = \beta_{dc} \left[\frac{V_{cc} - V_{BE}}{R_B} \right] + (1 + \beta_{dc}) I_{cbo}$$

But I_{c0} & I_{cbo} are same.

$$I_c R_B = \beta_{dc} V_{cc} - \beta_{dc} V_{BE} + (1 + \beta_{dc}) I_{cbo} R_B$$

Differentiate this eqn w.r.t V_{BE} ,

$$R_B \cdot \frac{\partial I_c}{\partial V_{BE}} = 0 - \beta_{dc} + 0$$

$$R_B \cdot S' = -\beta_{dc}$$

$$S' = \frac{-\beta_{dc}}{R_B}$$

-ve sign indicates that

I_c decreases as temperature

L②

increases due to reduction in
 V_{BE} at increased temp.

Relation between s & s' -

$$s = (1 + \beta_{dc})$$

from eq' ② $\beta_{dc} = -s' R_B$

$$s = 1 - s' R_B \quad \text{or} \quad s' = \frac{(1-s)}{R_B}$$

Expression for stability factor s'' for a fixed Bias d

$$s'' = \frac{\partial I_c}{\partial \beta_{dc}} \quad | \quad I_{c0} \text{ & } V_{BE} \text{ constant}$$

for CE, $I_c = \beta_{dc} I_B + (1 + \beta_{dc}) I_{cbo}$

$$= \beta_{dc} I_B + \beta_{dc} I_{cbo} + I_{cbo}$$

Differentiate both sides w.r.t β_{dc} ,

$$\frac{\partial I_c}{\partial \beta_{dc}} = I_B + I_{cbo} + 0$$

neglecting I_{cbo} , we get,

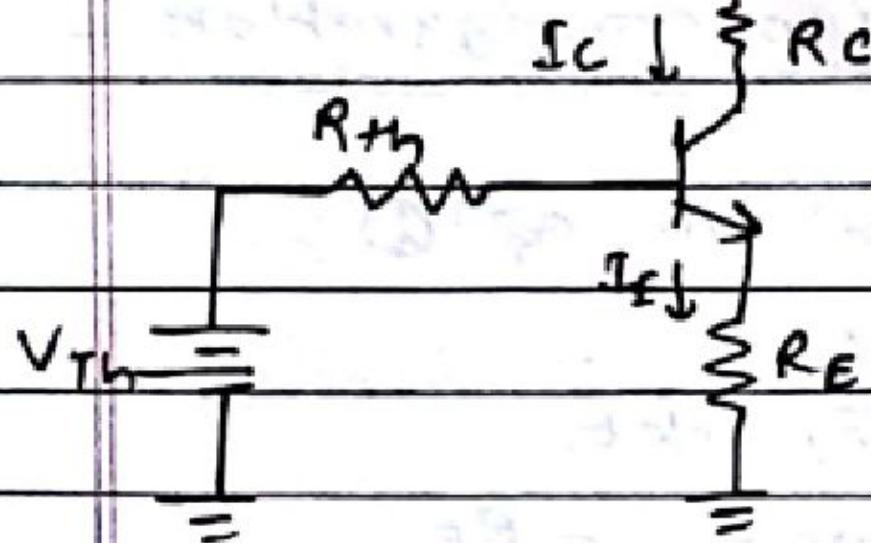
$$s'' = \frac{\partial I_c}{\partial \beta_{dc}} = \frac{I_b}{\beta_{dc}} = \frac{I_c}{\beta_{dc}}$$

$$s' = \frac{I_c}{\beta_{dc}}$$

out of s , s' & s'' the stability factor s is significantly higher than the remaining two.

* stability factor for voltage divider Bias circuit -

To obtain value of $\frac{\Delta I_B}{\Delta I_C}$



Apply KVL,

$$V_{TH} = I_B R_B + V_{BE} + (I_C + I_B) R_E$$

If we consider V_{BE} to be independent of I_C ,
we can differentiate this
eq' w.r.t I_C ,

Thevenin's equivalent ckt

for voltage divider bias

$$\therefore \alpha = R_B \frac{\partial I_B}{\partial I_C} + 0 + R_E + R_E \frac{\partial I_B}{\partial I_C}$$

$$0 = \frac{\partial I_B}{\partial I_C} (R_B + R_E) + R_E$$

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{(R_B + R_E)}$$

$$\frac{\Delta I_B}{\Delta I_C} = -\frac{R_E}{(R_B + R_E)}$$

put in eq^①,

$$s = \frac{(1 + \beta_{dc})}{1 - \beta_{dc} \left[\frac{\Delta I_B}{\Delta I_C} \right]}$$

$$s = \frac{1 + \beta_{dc}}{1 - \beta_{dc} \left[\frac{-R_E}{R_B + R_E} \right]}$$

$$s = \frac{1 + \beta_{dc}}{1 + \beta_{dc} \left[\frac{R_E}{R_B + R_E} \right]} = \frac{(1 + \beta_{dc})(R_B + R_E)}{R_B + R_E + \beta_{dc} R_E}$$

$$= \frac{(1 + \beta_{dc})(R_B + R_E)}{R_B + (1 + \beta_{dc}) R_E}$$

divide N & D by R_E

$$s = (1 + \beta_{dc}) \frac{1 + (R_B/R_E)}{(1 + \beta_{dc}) + (R_B/R_E)}$$

- The value of s depends on the ratio (R_B/R_E).
If (R_B/R_E) is small then the value of $s=1$ & if the ratio $(R_B/R_E) \rightarrow \infty$ then $s \in (1+\beta_{dc})$. Thus self bias ckt is more stable for smaller values of the ratio (R_B/R_E)
- If the ratio (R_B/R_E) is fixed then s increases with increase in the value of β_{dc} . Thus stability decreases with increase in β_{dc} .
- s is independent of β_{dc} for small values of β_{dc}
- Smaller values of R_B give better stabilization.

* *

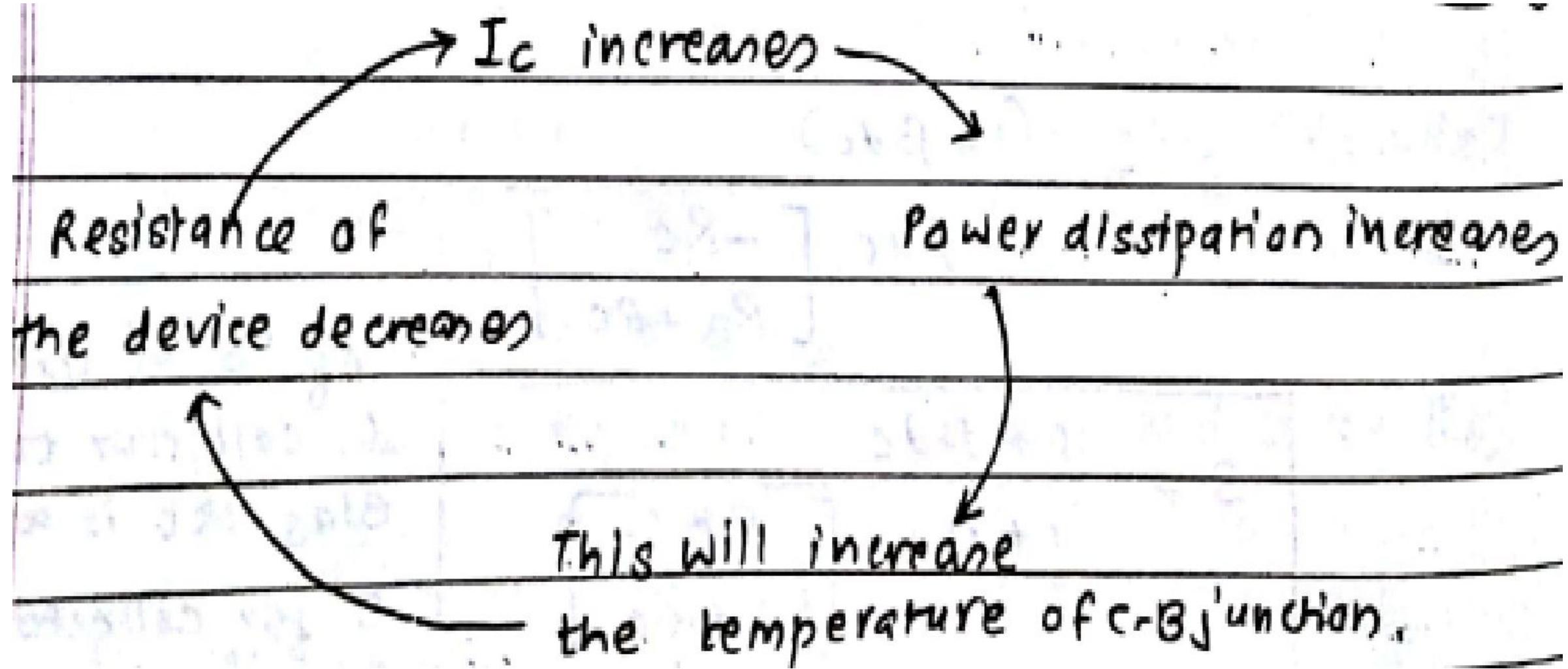
Thermal Runaway -

The maximum power that a transistor can dissipate without getting damaged depends largely on the maximum temperature that a collector base junction can withstand.

The rise in the collector base junction takes place due to two reasons :-

1. Due to increase in the ambient temperature
2. Due to the internal heating

PROCESS OF THERMAL RUNAWAY



out of them the internal heating process is cumulative as explained below :-

1. An increase in collector current I_C increases the power dissipated in the collector base junction of the transistor.
2. This will increase the temperature of C-B junction.
3. As the transistor has a negative temperature coefficient of resistivity, increased junction temperature reduces the resistance.
4. The reduced resistance will increase the collector current further.

This becomes a cumulative process which will finally damage the transistor due to excessive internal heating. This process is known as "Thermal Runaway".

* How to avoid thermal runaway?

- Never exceed the collector current beyond a certain maximum value specified by the manufacturer.
- Never exceed the internal power dissipation above the maximum permissible level/value.
- Use heat sink.

* Bias compensation -

The collector to base bias circuit & voltage divider circuit are examples of feedback amplifiers.

- Due to the negative feedback present in these ckt, the amplification of the AC signal is reduced drastically.

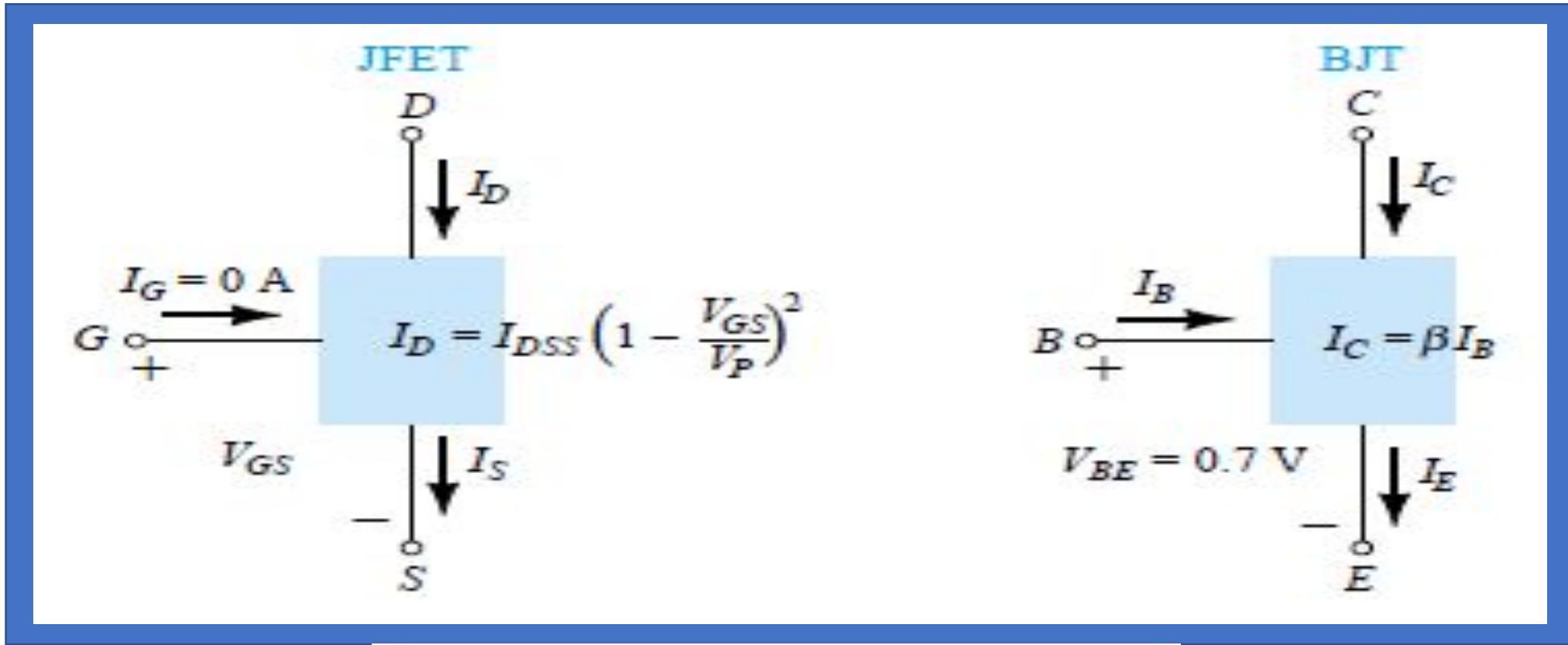
- If this loss of signal cannot be tolerated then the compensation techniques are used to reduce the drift in the operating point.

Very often both stabilization & compensation techniques are used to provide maximum bias & thermal stabilization.

Types of compensation techniques are -

1. compensation for changes in V_{BE} &
2. compensation for changes in I_C .

JFET AND BJT



JFET	BJT
$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$	$I_C = \beta I_B$
$I_D = I_S$	$I_C \cong I_E$
$I_G \cong 0 \text{ A}$	$V_{BE} \cong 0.7 \text{ V}$

IMPORTANT EQUATIONS FOR DC ANALYSIS OF FET

$$I_G \approx 0 \text{ A}$$

$$I_D = I_S$$

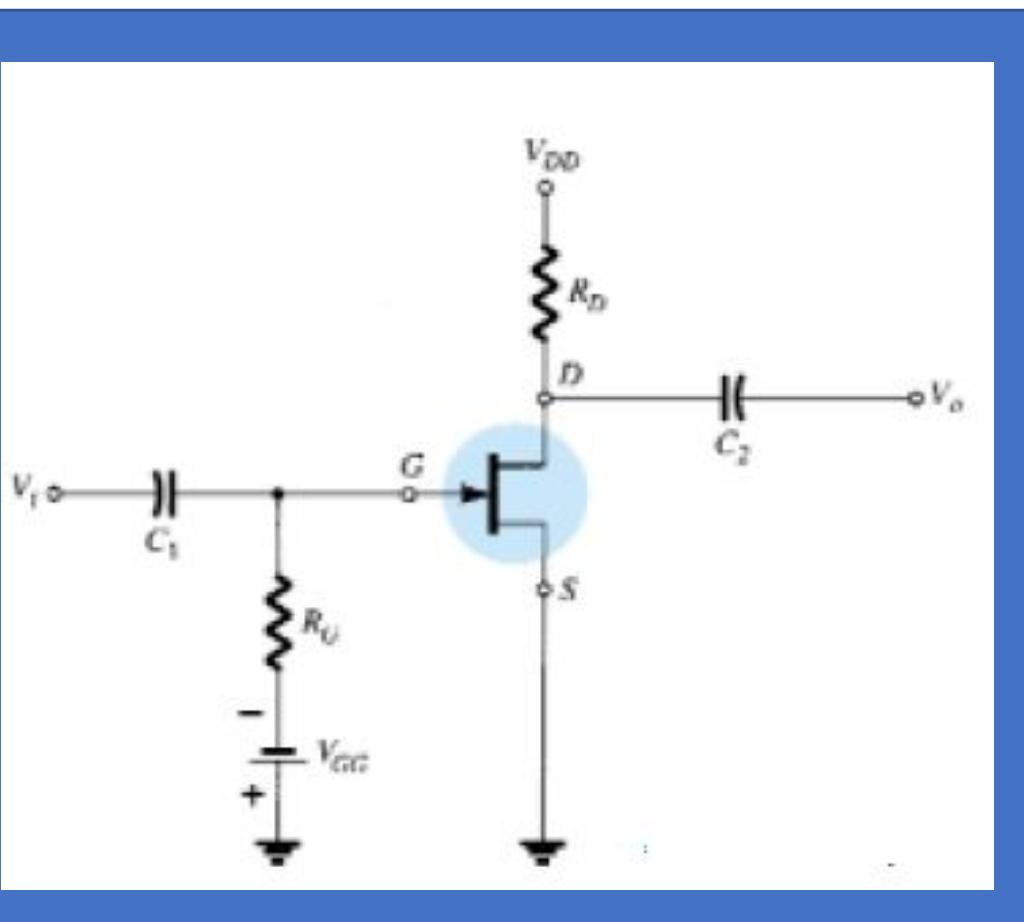
$$I_D = I_{DSS} \left(\frac{1 - V_{GS}}{V_P} \right)^2$$

TABLE V_{GS} versus I_D Using Shockley's Equation

V_{GS}	I_D
0	I_{DSS}
$0.3 V_P$	$I_{DSS}/2$
$0.5 V_P$	$I_{DSS}/4$
V_P	0 mA

FIXED BIAS CONFIGURATION

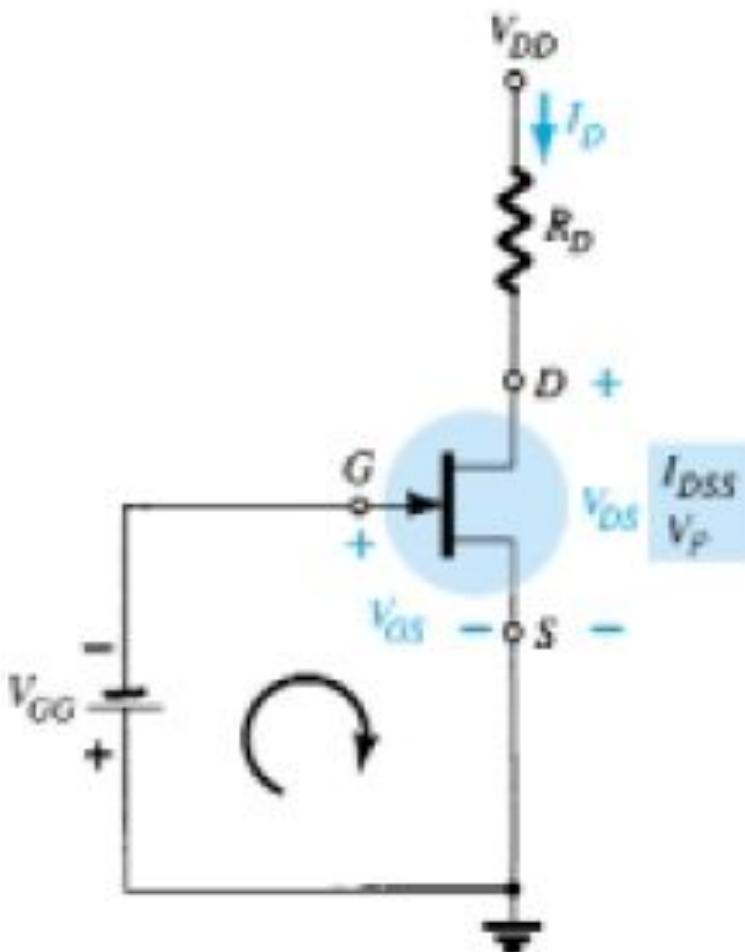
The simplest of biasing arrangements for the *n*-channel JFET appears in Fig. Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or graphical approach.



$$I_G \approx 0 \text{ A}$$

$$V_{RG} = I_G R_G = (0 \text{ A}) R_G = 0 \text{ V}$$

FIXED BIAS CONFIGURATION



$$-V_{GG} - V_{GS} = 0$$

$$V_{GS} = -V_{GG}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the notation “fixed-bias configuration.”

The resulting level of drain current I_D is now controlled by Shockley’s equation:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Since V_{GS} is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley’s equation and the resulting level of I_D calculated. This is one of the few instances in which a mathematical solution to a FET configuration is quite direct.

FIXED BIAS CONFIGURATION

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+ V_{DS} + I_D R_D - V_{DD} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0 \text{ V}$$

$$V_{DS} = V_D - V_S$$

$$V_D = V_{DS} + V_S = V_{DS} + 0 \text{ V}$$

$$V_D = V_{DS}$$

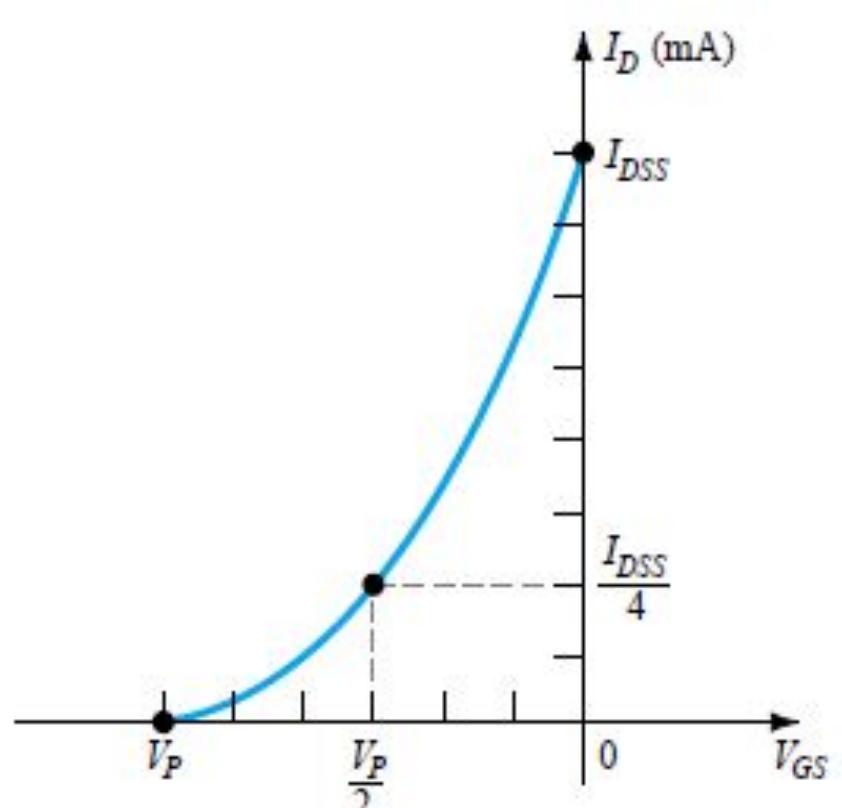
$$V_{GS} = V_G - V_S$$

$$V_G = V_{GS} + V_S = V_{GS} + 0 \text{ V}$$

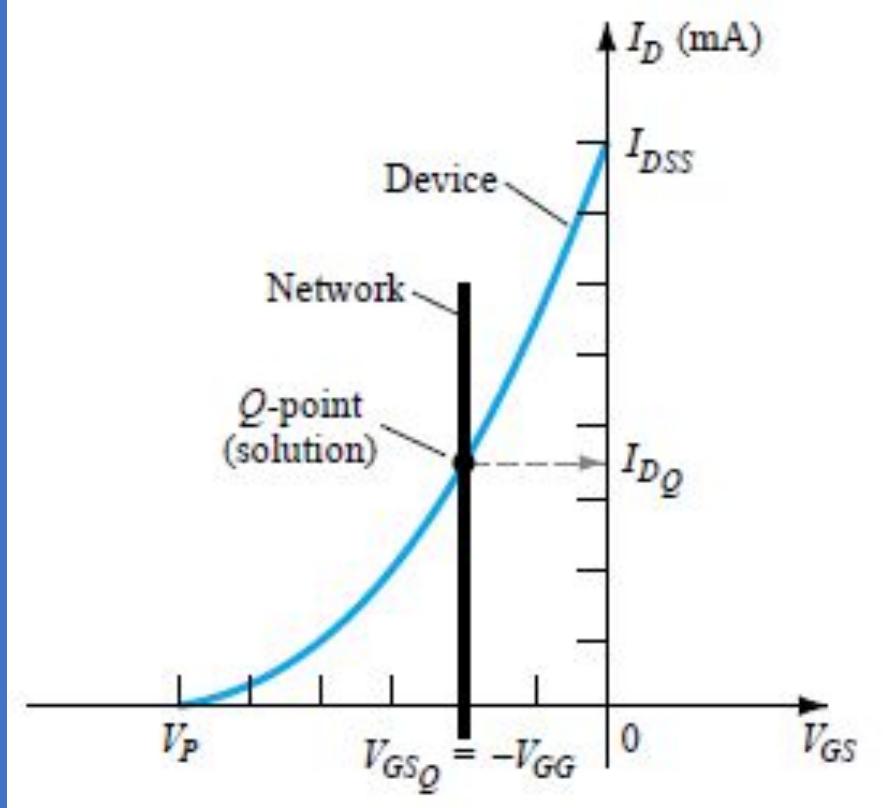
$$V_G = V_{GS}$$

GRAPHICAL ANALYSIS OF FIXED BIAS CONFIGURATION

A graphical analysis would require a plot of Shockley's equation as shown in Fig.



Plotting Shockley's equation.



Finding the solution for the fixed-bias configuration.

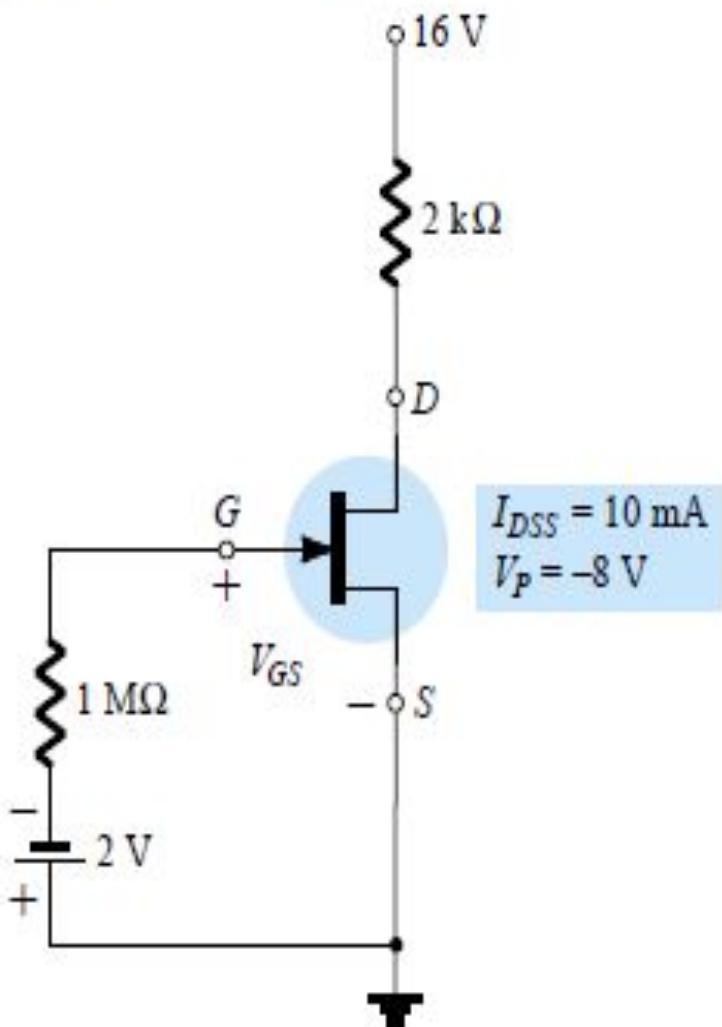
GRAPHICAL ANALYSIS OF FIXED BIAS CONFIGURATION

In Fig. 6.4 the fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$. At any point on the vertical line, the level of V_{GS} is $-V_{GG}$ —the level of I_D must simply be determined on this vertical line. The point where the two curves intersect is the common solution to the configuration—commonly referred to as the *quiescent* or *operating point*. The subscript Q will be applied to drain current and gate-to-source voltage to identify their levels at the Q -point. Note in Fig. 6.4 that the quiescent level of I_D is determined by drawing a horizontal line from the Q -point to the vertical I_D axis as shown in Fig.

EXAMPLE 1

Determine the following for the network of Fig.

- (a) V_{GSQ}
- (b) I_{DQ}
- (c) V_{DS}
- (d) V_D
- (e) V_G
- (f) V_S .



Solution

Mathematical Approach:

$$(a) V_{GSQ} = -V_{GG} = -2 \text{ V}$$

$$(b) I_{DQ} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10 \text{ mA} \left(1 - \frac{-2 \text{ V}}{-8 \text{ V}}\right)^2 = 10 \text{ mA} (1 - 0.25)^2 = 10 \text{ mA} (0.75)^2 = 10 \text{ mA} (0.5625) = 5.625 \text{ mA}$$

$$(c) V_{DS} = V_{DD} - I_D R_D = 16 \text{ V} - (5.625 \text{ mA})(2 \text{ k}\Omega) = 16 \text{ V} - 11.25 \text{ V} = 4.75 \text{ V}$$

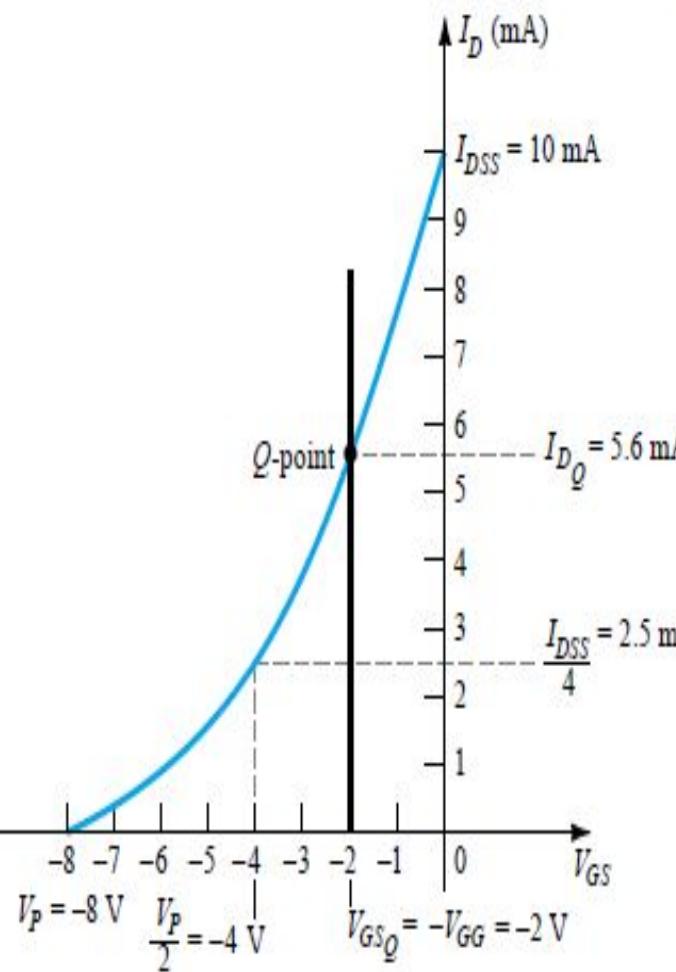
$$(d) V_D = V_{DS} = 4.75 \text{ V}$$

$$(e) V_G = V_{GS} = -2 \text{ V}$$

$$(f) V_S = 0 \text{ V}$$

GRAPHICAL APPROACH

The resulting Shockley curve and the vertical line at $V_{GS} = -2$ V are provided in Fig. 6.7. It is certainly difficult to read beyond the second place without significantly in-



Graphical solution
for the network

creasing the size of the figure, but a solution of 5.6 mA from the graph of Fig. 6.7 is quite acceptable. Therefore, for part (a),

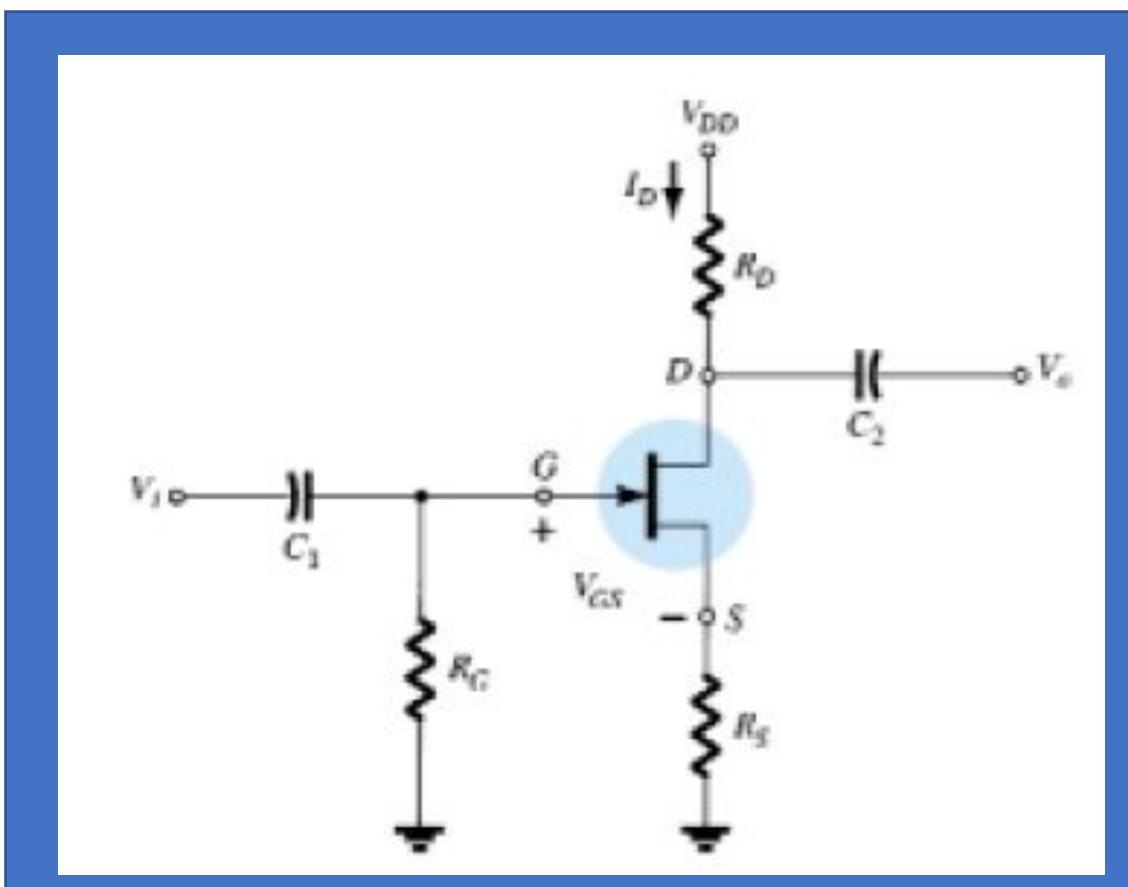
$$V_{GSQ} = -V_{GG} = -2 \text{ V}$$

- (b) $I_{DQ} = 5.6 \text{ mA}$
- (c) $V_{DS} = V_{DD} - I_D R_D = 16 \text{ V} - (5.6 \text{ mA})(2 \text{ k}\Omega)$
 $= 16 \text{ V} - 11.2 \text{ V} = 4.8 \text{ V}$
- (d) $V_D = V_{DS} = 4.8 \text{ V}$
- (e) $V_G = V_{GS} = -2 \text{ V}$
- (f) $V_S = 0 \text{ V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

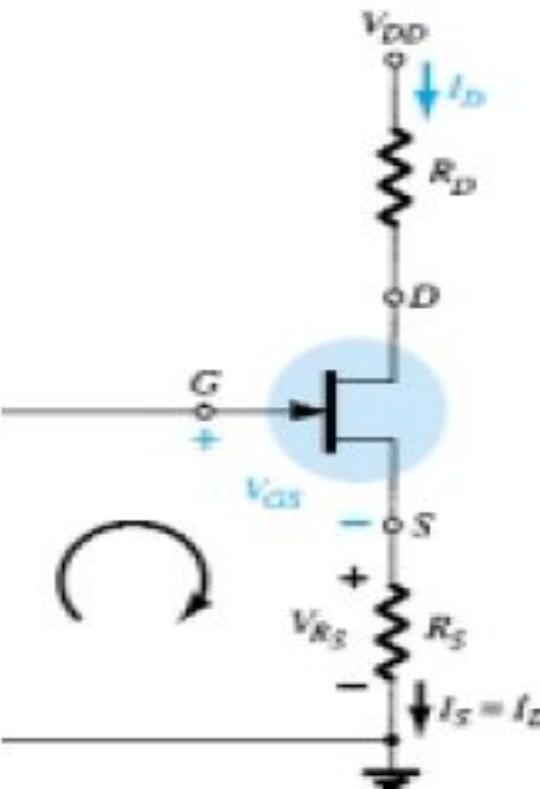
SELF BIAS CONFIGURATION

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in Fig.



DC ANALYSIS OF SELF BIAS

For the dc analysis, the capacitors can again be replaced by “open circuits” and the resistor R_G replaced by a short-circuit equivalent since $I_G = 0$ A.



The current through R_S is the source current I_S , but $I_S = I_D$ and

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of Fig. 6.9, we find that

$$-V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = -V_{R_S}$$

or

$$V_{GS} = -I_D R_S$$

Note in this case that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.

MATHEMATICAL APPROACH OF SELF BIAS

A mathematical solution could be obtained simply by substituting Eq. into Shockley's equation as shown below:

$$\begin{aligned}I_D &= I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \\&= I_{DSS} \left(1 - \frac{-I_D R_S}{V_P} \right)^2 \\&\text{or} \\I_D &= I_{DSS} \left(1 + \frac{I_D R_S}{V_P} \right)^2\end{aligned}$$

By performing the squaring process indicated and rearranging terms, an equation of the following form can be obtained:

$$I_D^2 + K_1 I_D + K_2 = 0$$

The quadratic equation can then be solved for the appropriate solution for I_D .

GRAPHICAL APPROACH

The graphical approach requires that we first establish the device transfer characteristics as shown in Fig. 6.10. Since Eq. (6.10) defines a straight line on the same graph,

Find two points on the graph

$$I_D = 0 \text{ A}$$

$$V_{GS} = -I_D R_S = (0 \text{ A})R_S = 0 \text{ V.}$$

$$I_D = \frac{I_{DSS}}{2}$$

$$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

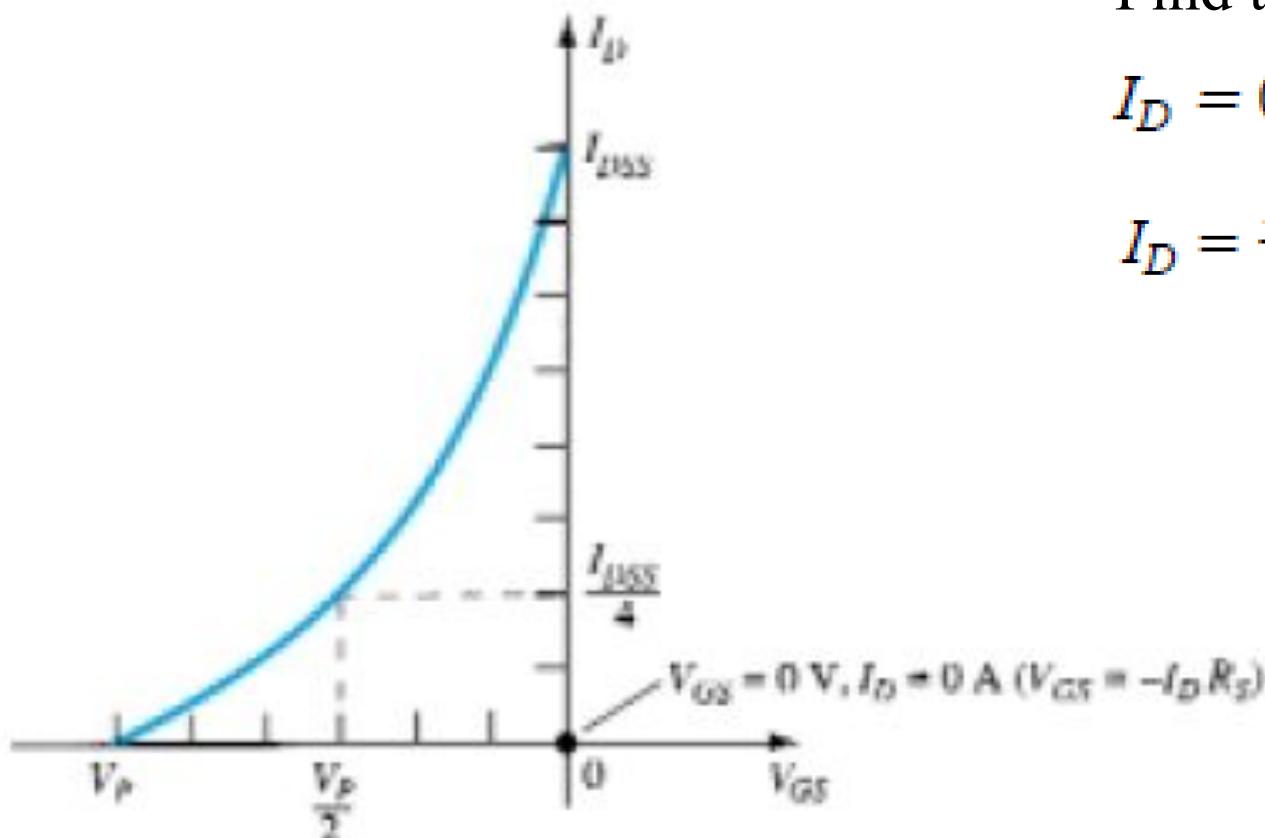
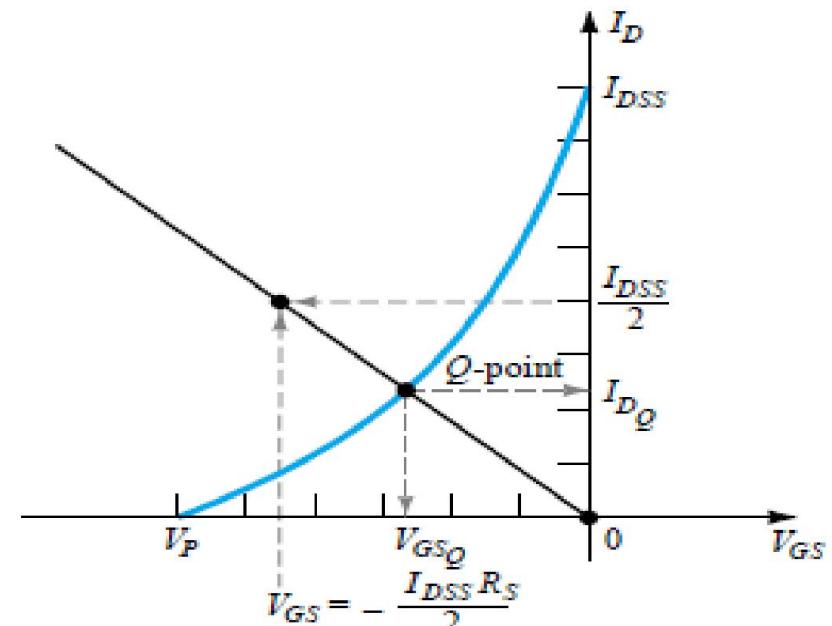


Figure 6.10 Defining a point on the self-bias line.



DC ANALYSIS OF SELF BIAS

The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

but

$$I_D = I_S$$

and

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

In addition:

$$V_S = I_D R_S$$

$$V_G = 0 \text{ V}$$

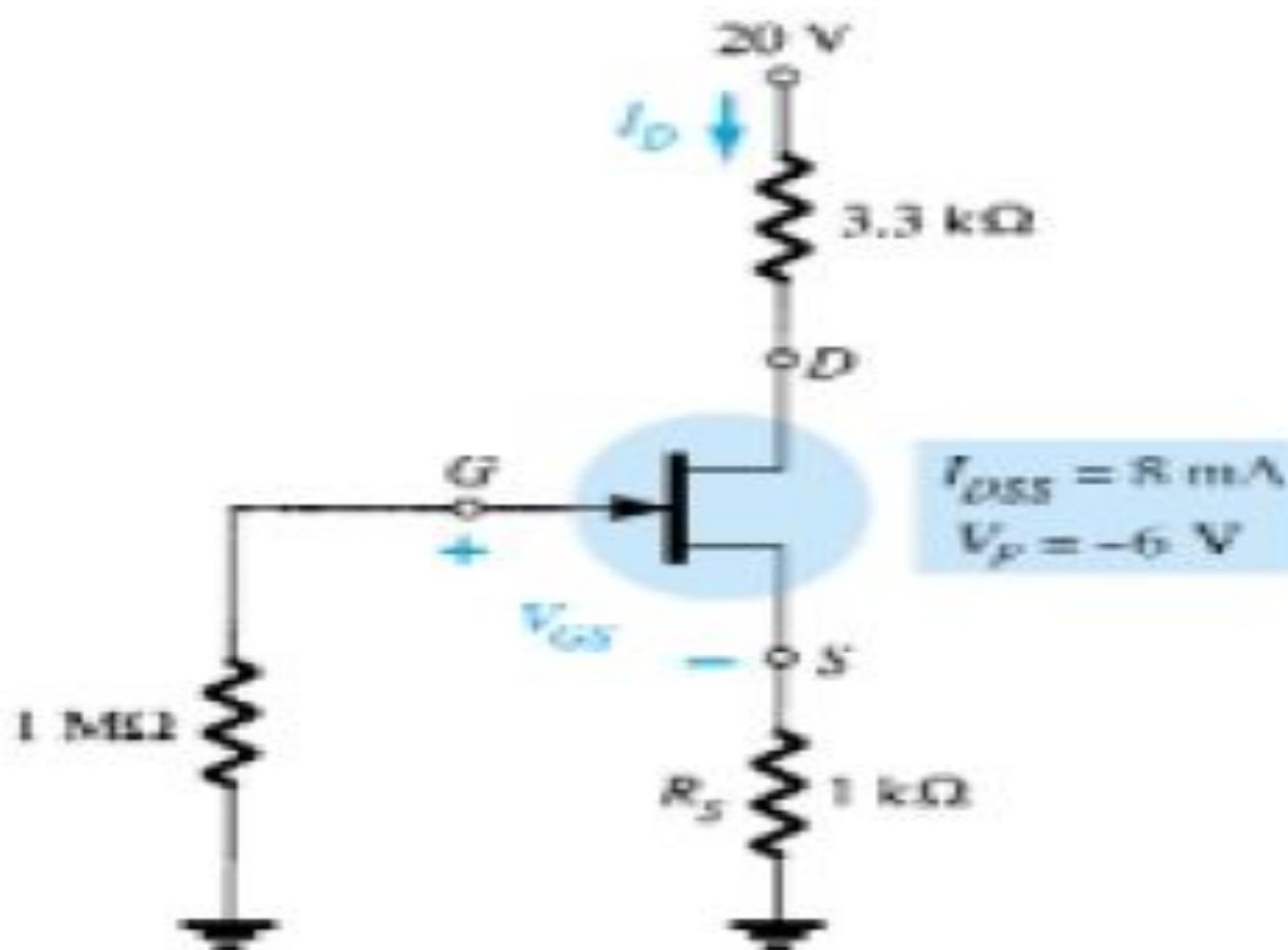
and

$$V_D = V_{DS} + V_S = V_{DD} - V_{R_D}$$

EXAMPLE 2

Determine the following for the network of Fig.

- (a) V_{GSQ} .
- (b) I_{DQ} .
- (c) V_{DS} .
- (d) V_S .
- (e) V_G .
- (f) V_D .



SOLUTION

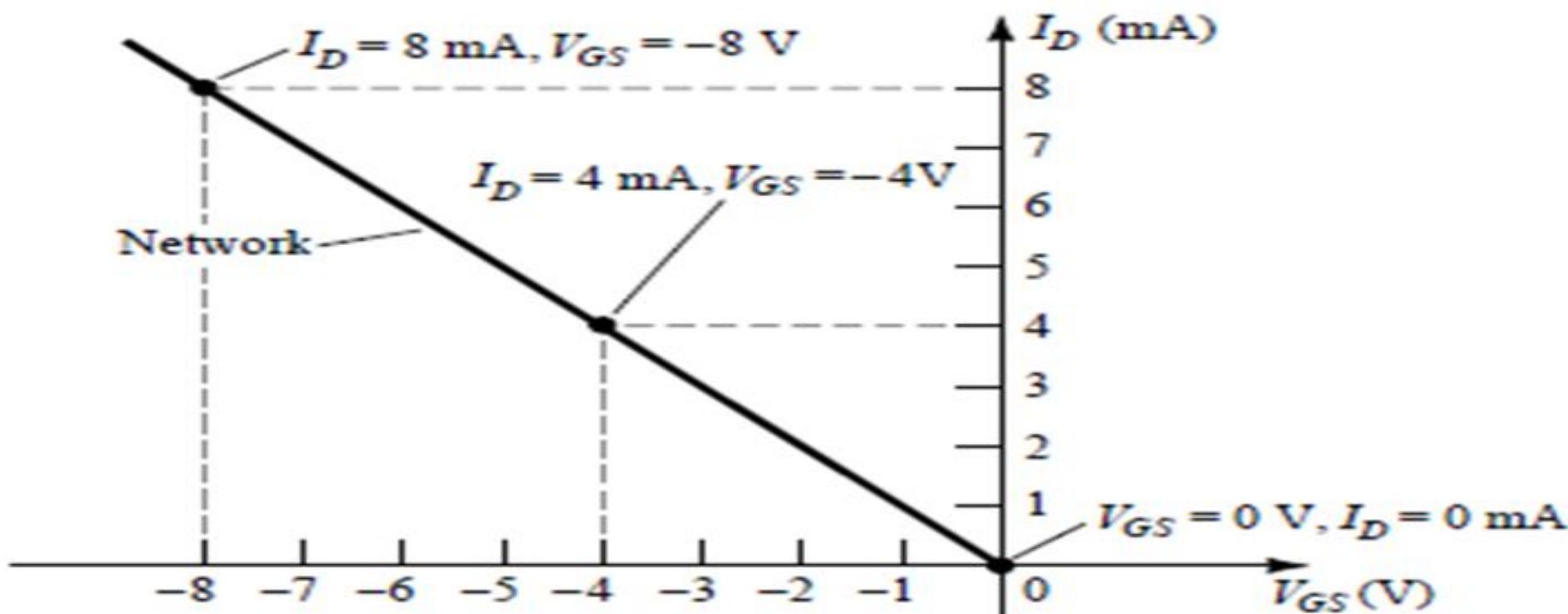
(a) The gate-to-source voltage is determined by

$$V_{GS} = -I_D R_S$$

Choosing $I_D = 4 \text{ mA}$, we obtain

$$V_{GS} = -(4 \text{ mA})(1 \text{ k}\Omega) = -4 \text{ V}$$

The result is the plot of Fig. 6.13 as defined by the network.



SOLUTION CONTINUED...

$$V_{GSQ} = -2.6 \text{ V}$$

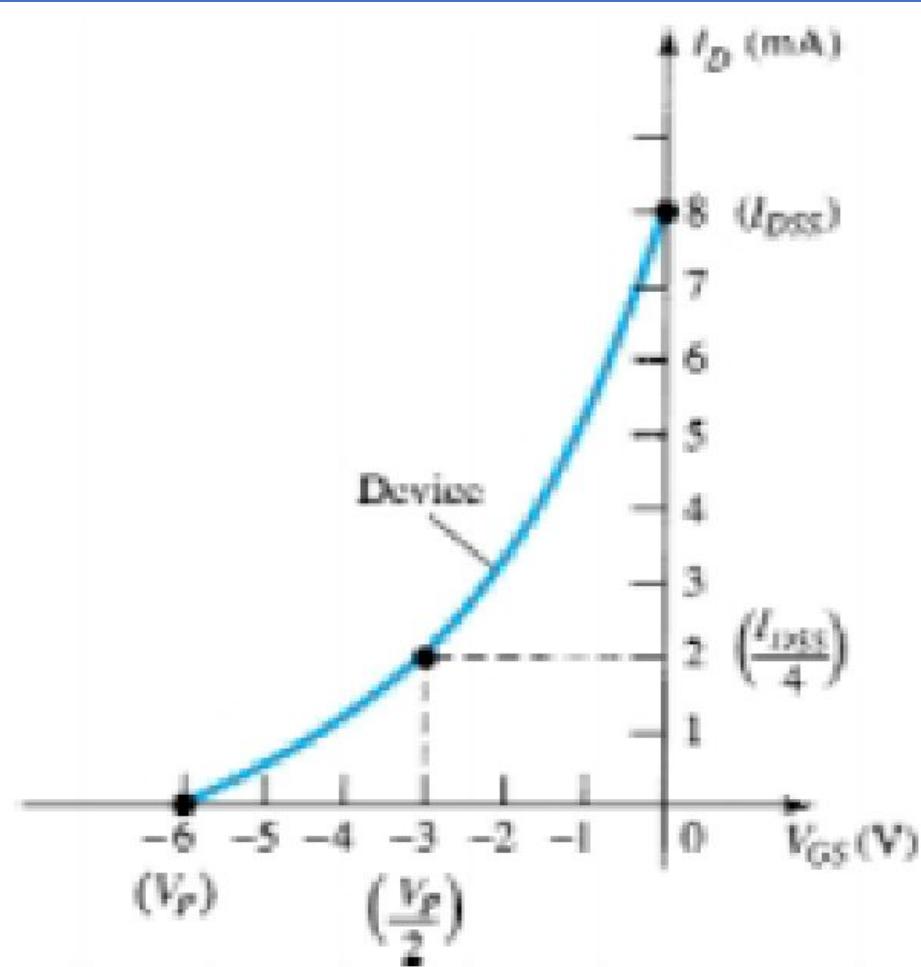


Figure 6.14 Sketching the device characteristics for the JFET of Fig. 6.12.

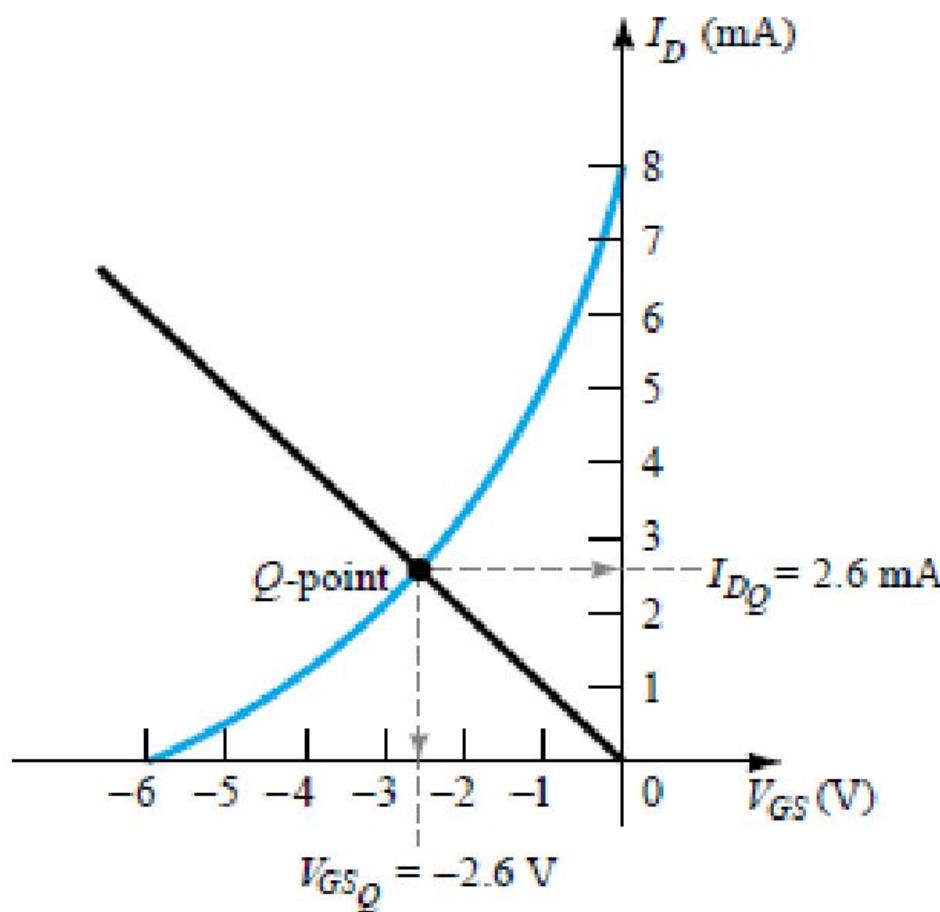


Figure 6.15 Determining the Q -point for the network of Fig. 6.12.

SOLUTION CONTINUED...

(b) At the quiescent point:

$$I_{DQ} = 2.6 \text{ mA}$$

(c)

$$\begin{aligned}V_{DS} &= V_{DD} - I_D(R_S + R_D) \\&= 20 \text{ V} - (2.6 \text{ mA})(1 \text{ k}\Omega + 3.3 \text{ k}\Omega) \\&= 20 \text{ V} - 11.18 \text{ V} \\&= 8.82 \text{ V}\end{aligned}$$

(d)

$$\begin{aligned}V_S &= I_D R_S \\&= (2.6 \text{ mA})(1 \text{ k}\Omega) \\&= 2.6 \text{ V}\end{aligned}$$

(e)

$$V_G = 0 \text{ V}$$

(f)

$$V_D = V_{DS} + V_S = 8.82 \text{ V} + 2.6 \text{ V} = 11.42 \text{ V}$$

or

$$V_D = V_{DD} - I_D R_D = 20 \text{ V} - (2.6 \text{ mA})(3.3 \text{ k}\Omega) = 11.42 \text{ V}$$

EXAMPLE 3

Find the quiescent point for the network of Fig. 6.12 if:

- (a) $R_S = 100 \Omega$.
- (b) $R_S = 10 \text{ k}\Omega$.

Solution

Note Fig. 6.16.

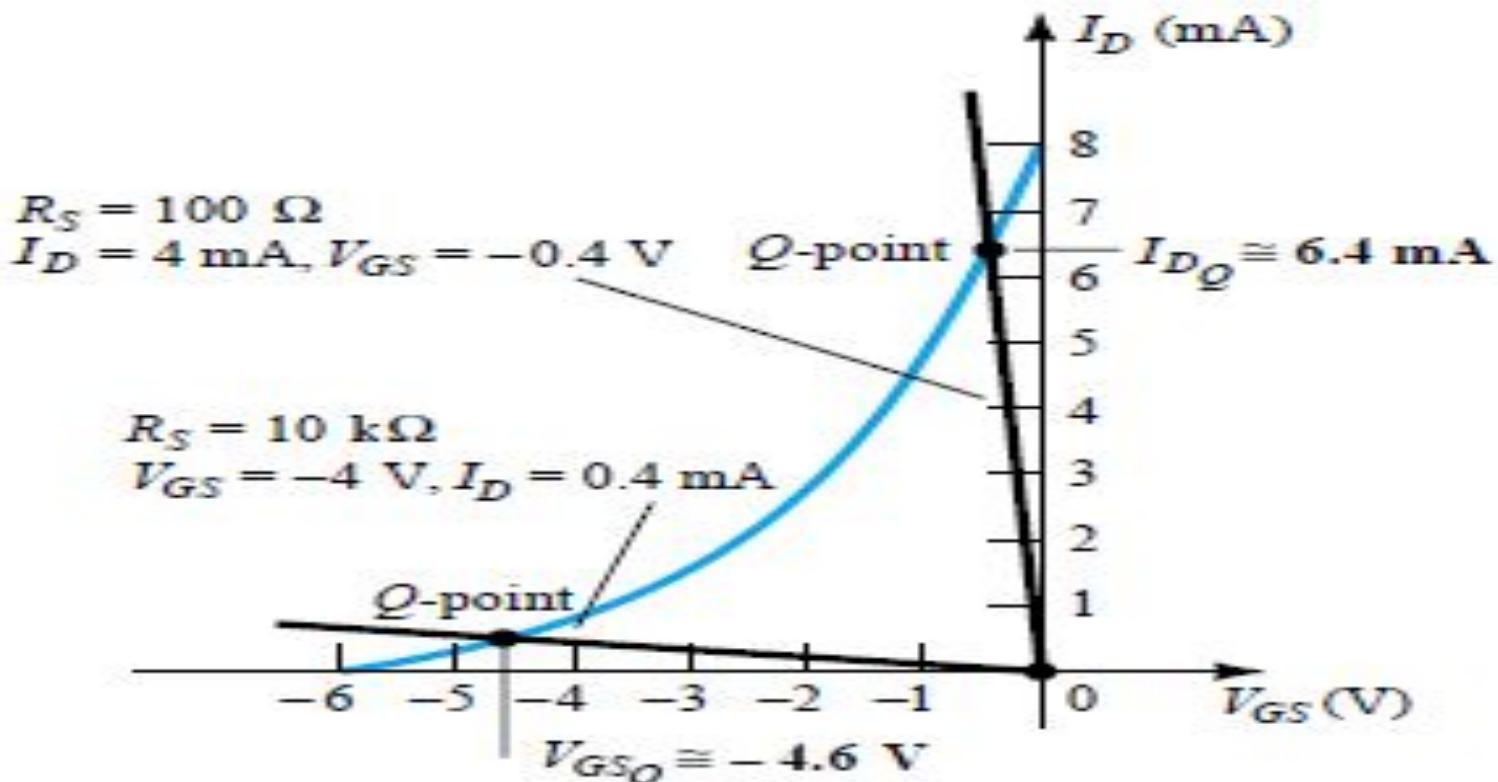


Figure 6.16

SOLUTION

(a) With the I_D scale,

$$I_{DQ} \approx 6.4 \text{ mA}$$

$$V_{GSQ} \approx -0.64 \text{ V}$$

(b) With the V_{GS} scale,

$$V_{GSQ} \approx -4.6 \text{ V}$$

$$I_{DQ} \approx 0.46 \text{ mA}$$

In particular, note how lower levels of R_S bring the load line of the network closer to the I_D axis while increasing levels of R_S bring the load line closer to the V_{GS} axis.

EXAMPLE 4

Determine the following for the common-gate configuration of Fig. 6.17.

- (a) V_{GSQ} .
- (b) I_{DQ} .
- (c) V_D .
- (d) V_G .
- (e) V_S .
- (f) V_{DS} .

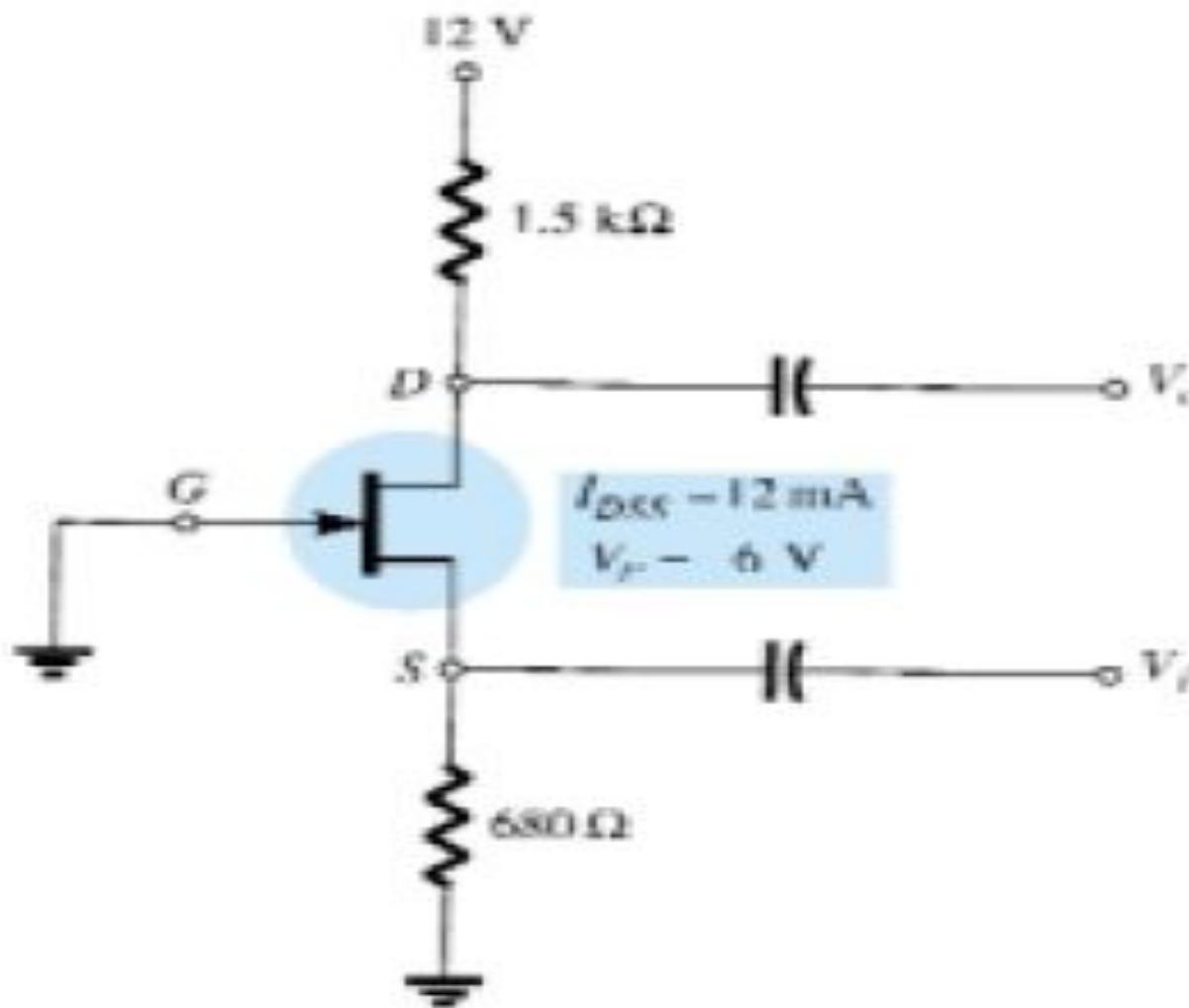


Figure 6.17

SOLUTION

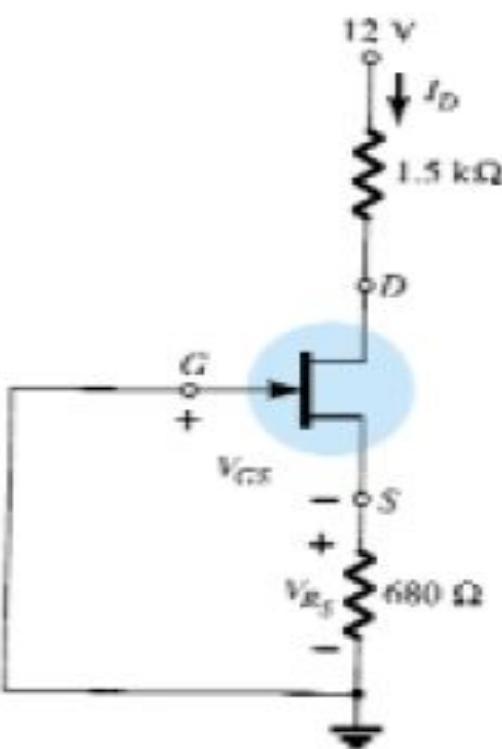


Figure 6.18 Sketching the dc equivalent of the network of Fig.

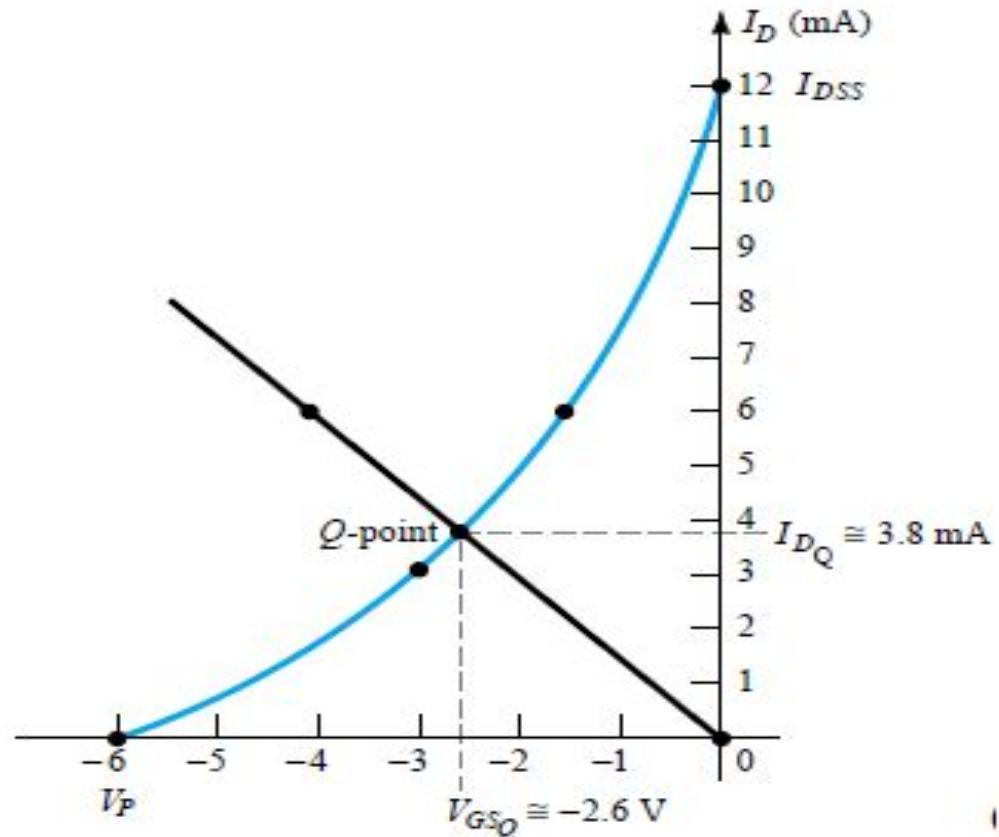


Figure 6.19 Determining the *Q*-point for the network of Fig.

- (a) The transfer characteristics and load line appear in Fig. 6.19. In this case, the second point for the sketch of the load line was determined by choosing (arbitrarily) $I_D = 6 \text{ mA}$ and solving for V_{GS} . That is,

$$V_{GS} = -I_D R_S = -(6 \text{ mA})(680 \Omega) = -4.08 \text{ V}$$

as shown in Fig. 6.19. The device transfer curve was sketched using

$$I_D = \frac{I_{DSS}}{4} = \frac{12 \text{ mA}}{4} = 3 \text{ mA}$$

SOLUTION CONTINUED...

and the associated value of V_{GS} :

$$V_{GS} = \frac{V_P}{2} = -\frac{6 \text{ V}}{2} = -3 \text{ V}$$

as shown on Fig. 6.19. Using the resulting quiescent point of Fig. 6.19 results in

$$V_{GSO} \cong -2.6 \text{ V}$$

(b)

$$I_{DQ} \cong 3.8 \text{ mA}$$

(c) $V_D = V_{DD} - I_D R_D$
 $= 12 \text{ V} - (3.8 \text{ mA})(1.5 \text{ k}\Omega) = 12 \text{ V} - 5.7 \text{ V}$
 $= 6.3 \text{ V}$

(d) $V_G = 0 \text{ V}$

(e) $V_S = I_D R_S = (3.8 \text{ mA})(680 \text{ }\Omega)$
 $= 2.58 \text{ V}$

(f) $V_{DS} = V_D - V_S$
 $= 6.3 \text{ V} - 2.58 \text{ V}$
 $= 3.72 \text{ V}$

VOLTAGE DIVIDER BIAS

The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers as demonstrated by Fig. 6.20. The basic construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0 \text{ A}$ for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. Recall that I_B provided the link between input and output circuits for the BJT voltage-divider configuration while V_{GS} will do the same for the FET configuration.

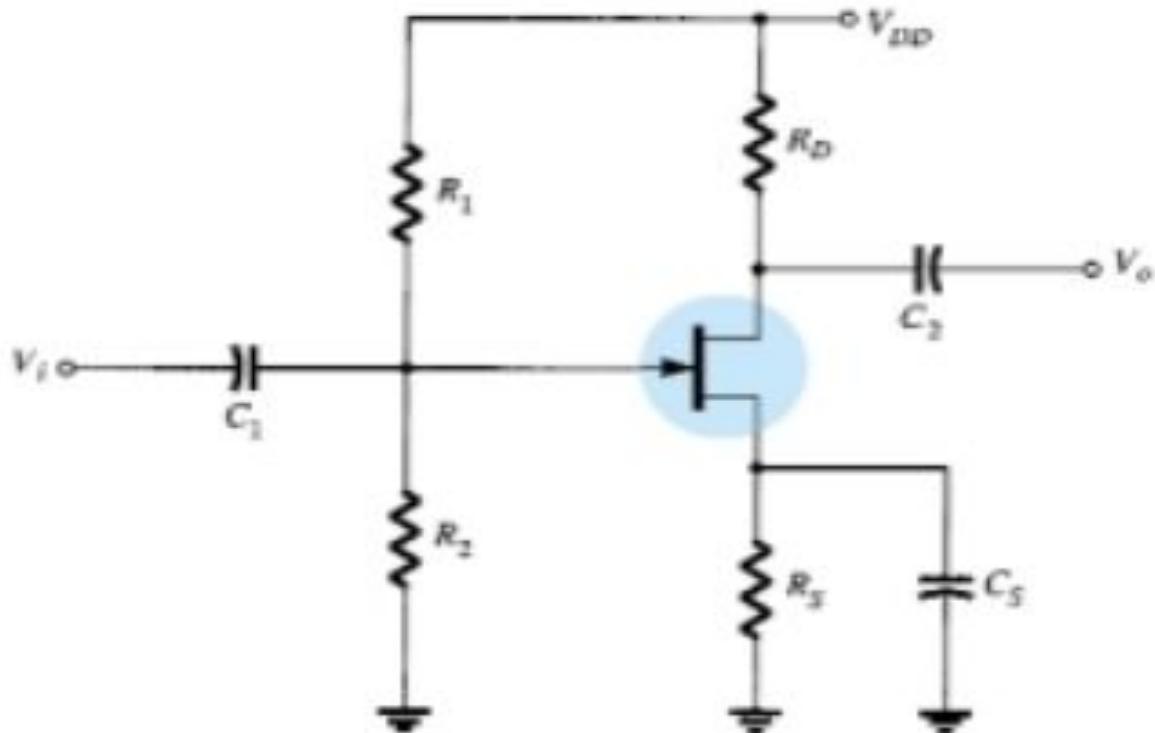


Figure 6.20 Voltage-divider bias arrangement.

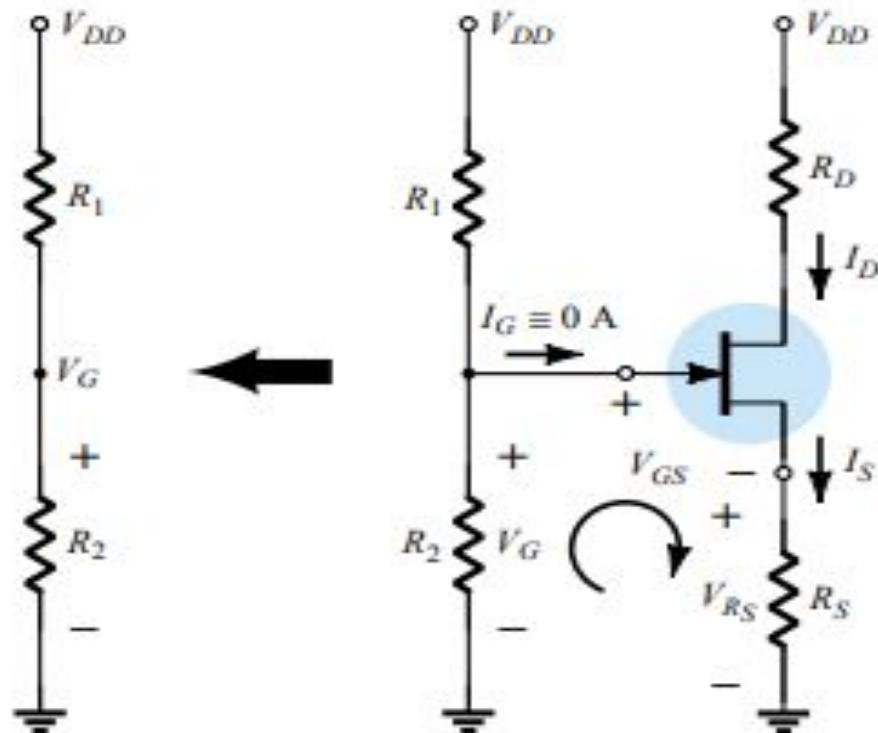


Figure 6.21 Redrawn network of Fig. 6.20 for dc analysis.

VOLTAGE DIVIDER BIAS

The network of Fig. 6.20 is redrawn as shown in Fig. 6.21 for the dc analysis. Note that all the capacitors, including the bypass capacitor C_S , have been replaced by an “open-circuit” equivalent. In addition, the source V_{DD} was separated into two equivalent sources to permit a further separation of the input and output regions of the network. Since $I_G = 0$ A, Kirchhoff’s current law requires that $I_{R_1} = I_{R_2}$ and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G . The voltage V_G , equal to the voltage across R_2 , can be found using the voltage-divider rule as follows:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Applying Kirchhoff’s voltage law in the clockwise direction to the indicated loop of Fig. 6.21 will result in

$$V_G - V_{GS} - V_{RS} = 0$$

and

$$V_{GS} = V_G - V_{RS}$$

Substituting $V_{RS} = I_S R_S = I_D R_S$, we have

$$V_{GS} = V_G - I_D R_S$$

VOLTAGE DIVIDER BIAS

If we therefore select I_D to be 0 mA, we are in essence stating that we are somewhere on the horizontal axis. The exact location can be determined simply by substituting $I_D = 0$ mA into Eq. (6.16) and finding the resulting value of V_{GS} as follows:

$$\begin{aligned}V_{GS} &= V_G - I_D R_S \\&= V_G - (0 \text{ mA}) R_S\end{aligned}$$

and

$$V_{GS} = V_G|_{I_D=0 \text{ mA}}$$

The result specifies that whenever we plot Eq. (6.16), if we choose $I_D = 0$ mA, the value of V_{GS} for the plot will be V_G volts. The point just determined appears in Fig. 6.22.

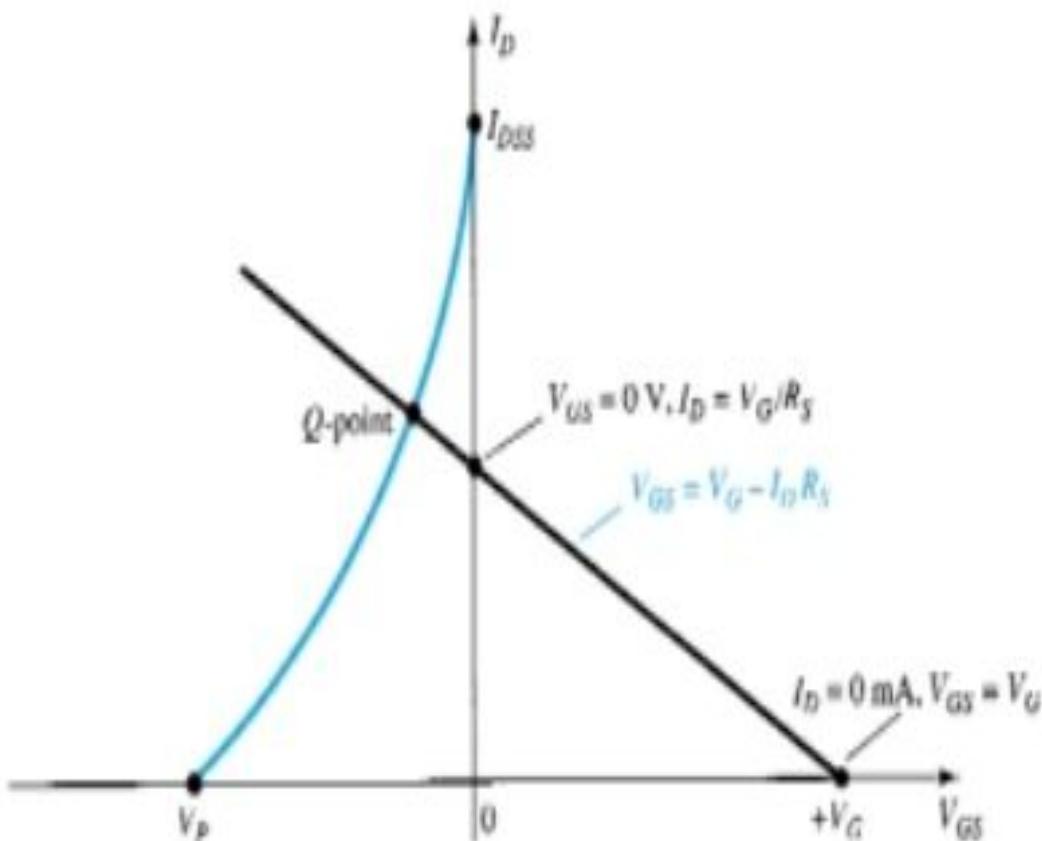


Figure 6.22 Sketching the network equation for the voltage-divider configuration.

VOLTAGE DIVIDER BIAS

For the other point, let us now employ the fact that at any point on the vertical axis $V_{GS} = 0 \text{ V}$ and solve for the resulting value of I_D :

$$V_{GS} = V_G - I_D R_S$$

$$0 \text{ V} = V_G - I_D R_S$$

$$I_D = \frac{V_G}{R_S} \Big|_{V_{GS} = 0 \text{ V}}$$

and

The result specifies that whenever we plot Eq. (6.16), if $V_{GS} = 0 \text{ V}$, the level of I_D is determined by Eq. (6.18). This intersection also appears on Fig. 6.22.

Since the intersection on the vertical axis is determined by $I_D = V_G/R_S$ and V_G is fixed by the input network, increasing values of R_S will reduce the level of the I_D intersection as shown in Fig. 6.23. It is fairly obvious from Fig. 6.23 that:

Increasing values of R_S result in lower quiescent values of I_D and more negative values of V_{GS} .

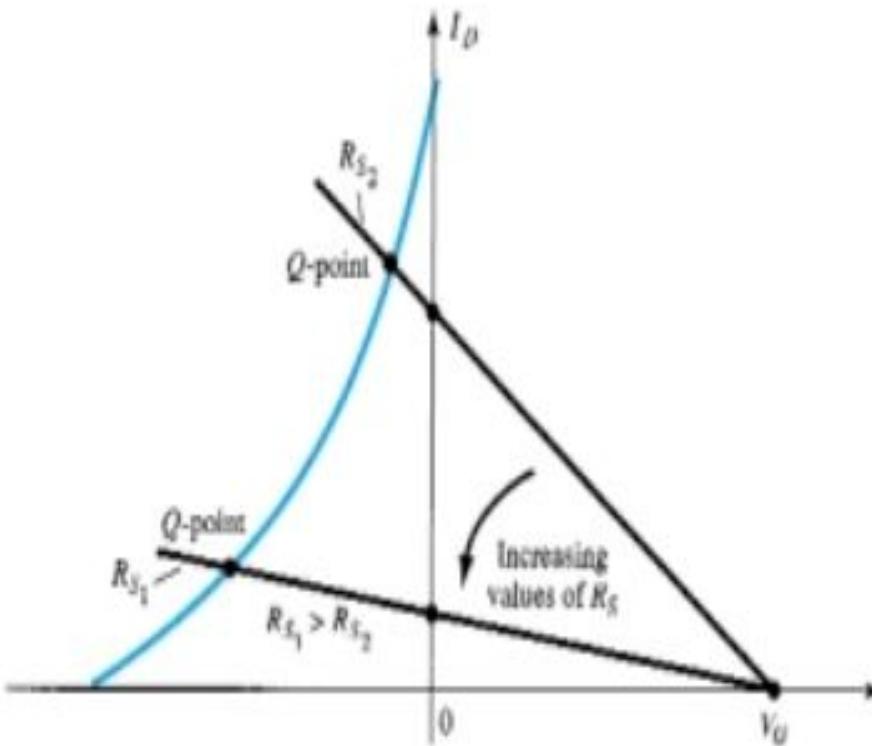


Figure 6.23 Effect of R_S on the resulting Q -point.

VOLTAGE DIVIDER BIAS

Once the quiescent values of I_{DQ} and V_{GSQ} are determined, the remaining network analysis can be performed in the usual manner. That is,

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$

EXAMPLE 1

Determine the following for the network of Fig. 6.24.

- (a) I_{DQ} and V_{GSQ} .
- (b) V_D .
- (c) V_S .
- (d) V_{DS} .
- (e) V_{DG} .

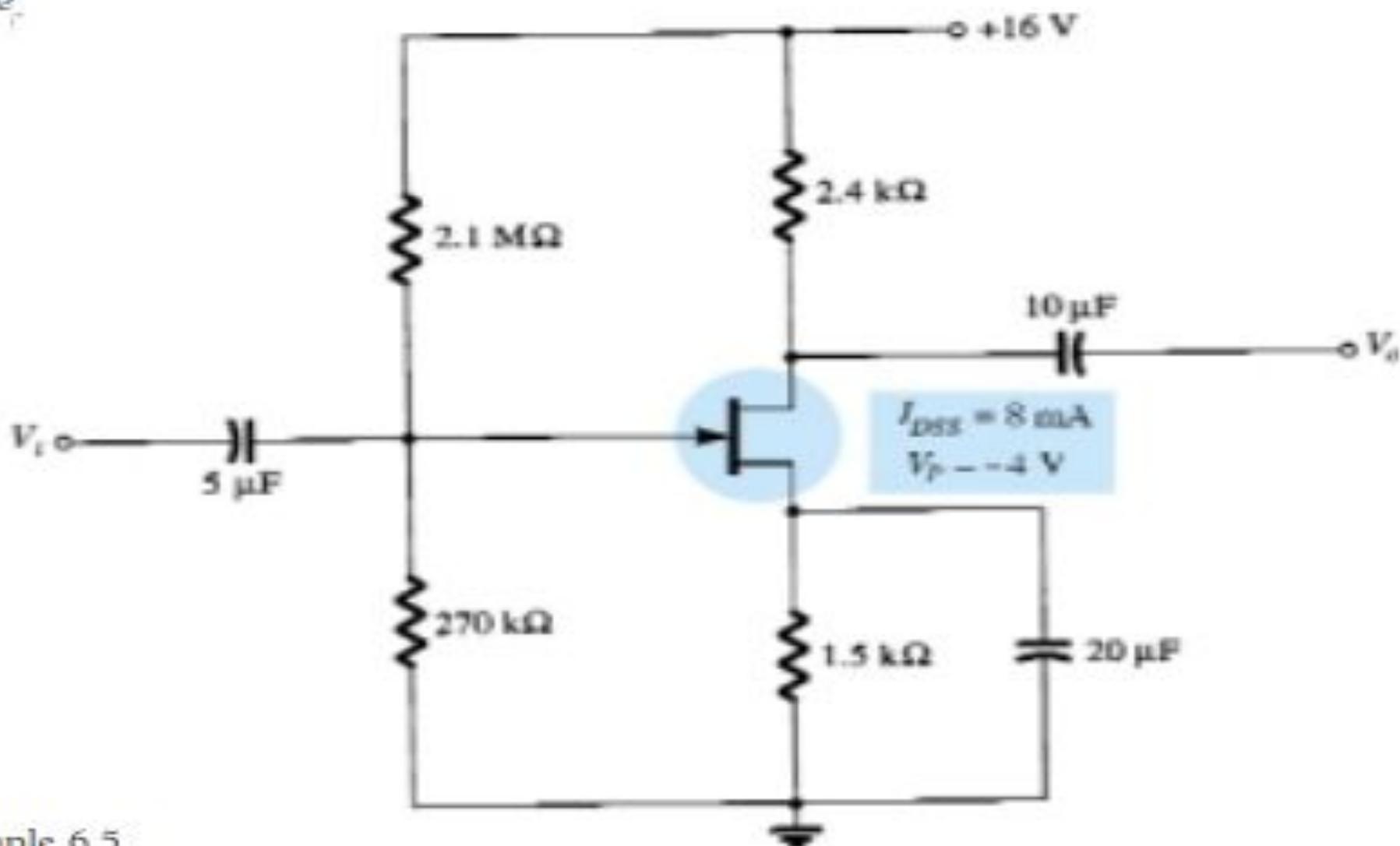


Figure 6.24 Example 6.5.

SOLUTION

- (a) For the transfer characteristics, if $I_D = I_{DSS}/4 = 8 \text{ mA}/4 = 2 \text{ mA}$, then $V_{GS} = V_p/2 = -4 \text{ V}/2 = -2 \text{ V}$. The resulting curve representing Shockley's equation appears in Fig. 6.25. The network equation is defined by

$$\begin{aligned}V_G &= \frac{R_2 V_{DD}}{R_1 + R_2} \\&= \frac{(270 \text{ k}\Omega)(16 \text{ V})}{2.1 \text{ M}\Omega + 0.27 \text{ M}\Omega} \\&= 1.82 \text{ V}\end{aligned}$$

and

$$\begin{aligned}V_{GS} &= V_G - I_D R_S \\&= 1.82 \text{ V} - I_D (1.5 \text{ k}\Omega)\end{aligned}$$

When $I_D = 0 \text{ mA}$:

$$V_{GS} = +1.82 \text{ V}$$

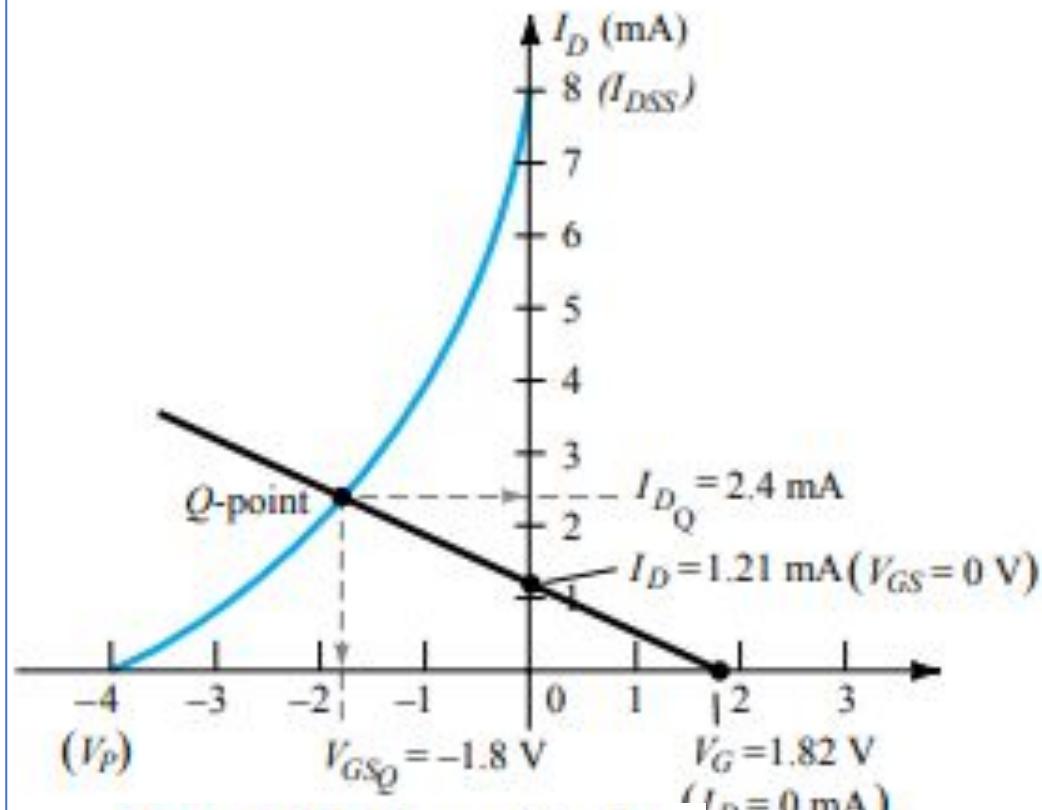


Figure 6.25 Determining the Q -point for the network of Fig. 6.24.

SOLUTION

When $V_{GS} = 0 \text{ V}$:

$$I_D = \frac{1.82 \text{ V}}{1.5 \text{ k}\Omega} = 1.21 \text{ mA}$$

The resulting bias line appears on Fig. 6.25 with quiescent values of

$$I_{DQ} = 2.4 \text{ mA}$$

and

$$V_{GSQ} = -1.8 \text{ V}$$

(b)
$$\begin{aligned} V_D &= V_{DD} - I_D R_D \\ &= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega) \\ &= 10.24 \text{ V} \end{aligned}$$

(c)
$$\begin{aligned} V_S &= I_D R_S = (2.4 \text{ mA})(1.5 \text{ k}\Omega) \\ &= 3.6 \text{ V} \end{aligned}$$

(d)
$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_D + R_S) \\ &= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega + 1.5 \text{ k}\Omega) \\ &= 6.64 \text{ V} \end{aligned}$$

or
$$\begin{aligned} V_{DS} &= V_D - V_S = 10.24 \text{ V} - 3.6 \text{ V} \\ &= 6.64 \text{ V} \end{aligned}$$

(e) Although seldom requested, the voltage V_{DG} can easily be determined using

$$\begin{aligned} V_{DG} &= V_D - V_G \\ &= 10.24 \text{ V} - 1.82 \text{ V} \\ &= 8.42 \text{ V} \end{aligned}$$

EXAMPLE

Determine the following for the network of Fig. 6.26.

- (a) I_{DQ} and V_{GSQ}
- (b) V_{DS}
- (c) V_D
- (d) V_S

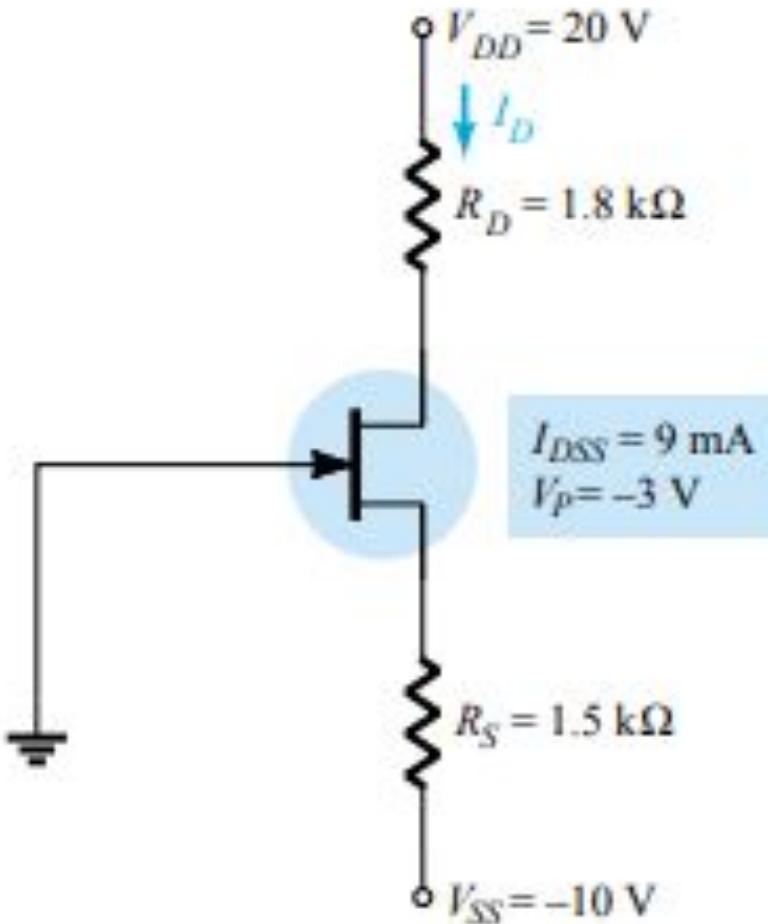


Figure 6.26 Example 6.6.

SOLUTION

(a) An equation for V_{GS} in terms of I_D is obtained by applying Kirchhoff's voltage law to the input section of the network as redrawn in Fig. 6.27.

$$-V_{GS} - I_S R_S + V_{SS} = 0$$

or

$$V_{GS} = V_{SS} - I_S R_S$$

but

$$I_S = I_D$$

and

$$V_{GS} = V_{SS} - I_D R_S \quad (6.23)$$

The result is an equation very similar in format to Eq. (6.16) that can be superimposed on the transfer characteristics using the procedure described for Eq. (6.16). That is, for this example,

$$V_{GS} = 10 \text{ V} - I_D(1.5 \text{ k}\Omega)$$

For $I_D = 0 \text{ mA}$,

$$V_{GS} = V_{SS} = 10 \text{ V}$$

For $V_{GS} = 0 \text{ V}$,

$$0 = 10 \text{ V} - I_D(1.5 \text{ k}\Omega)$$

and

$$I_D = \frac{10 \text{ V}}{1.5 \text{ k}\Omega} = 6.67 \text{ mA}$$

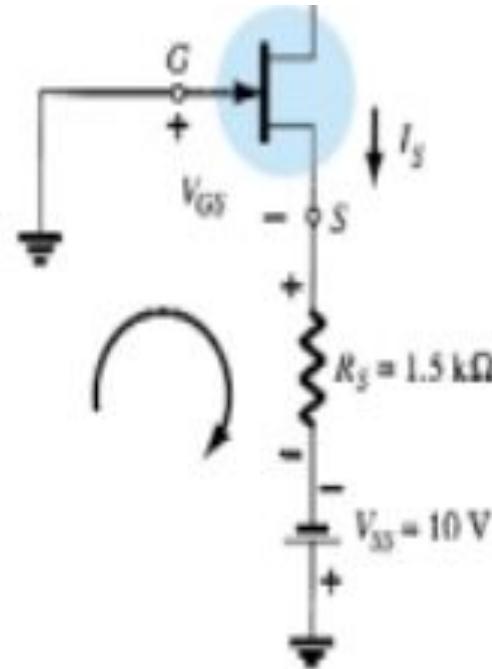
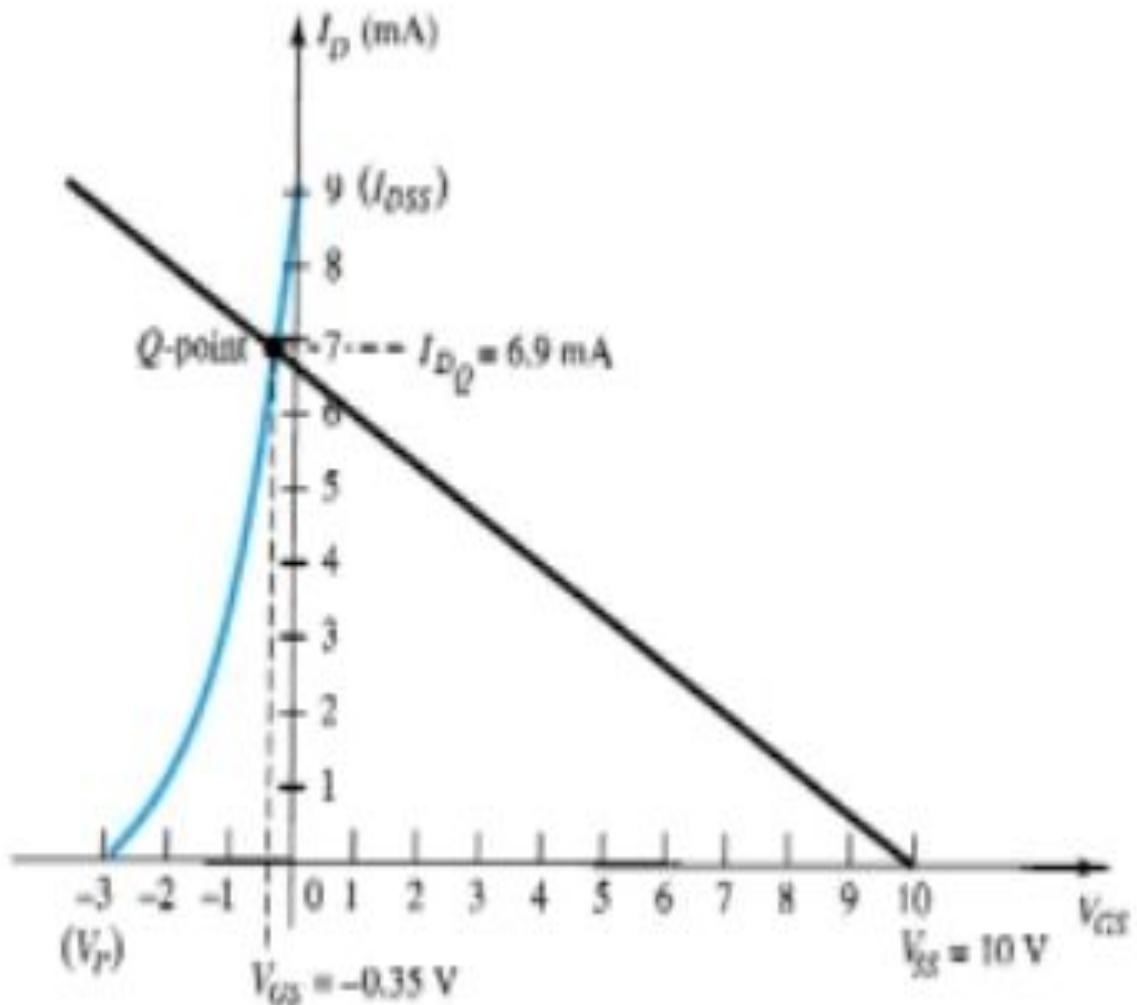


Figure 6.27 Determining the network equation for the configuration of Fig. 6.26.

SOLUTION

The transfer characteristics are sketched using the plot point established by $V_{GS} = V_P/2 = -3 \text{ V}/2 = -1.5 \text{ V}$ and $I_D = I_{DSS}/4 = 9 \text{ mA}/4 = 2.25 \text{ mA}$, as also appearing on Fig. 6.28. The resulting operating point establishes the following quiescent levels:



$$I_{DQ} = 6.9 \text{ mA}$$

$$V_{GSQ} = -0.35 \text{ V}$$

(b) Applying Kirchhoff's voltage law to the output side of Fig. 6.26 will result in

$$-V_{SS} + I_S R_S + V_{DS} + I_D R_D - V_{DD} = 0$$

Substituting $I_S = I_D$ and rearranging gives

$$V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$$

which for this example results in

$$\begin{aligned} V_{DS} &= 20 \text{ V} + 10 \text{ V} - (6.9 \text{ mA})(1.8 \text{ k}\Omega + 1.5 \text{ k}\Omega) \\ &= 30 \text{ V} - 22.77 \text{ V} \\ &= 7.23 \text{ V} \end{aligned}$$

$$\begin{aligned} (c) \quad V_D &= V_{DD} - I_D R_D \\ &= 20 \text{ V} - (6.9 \text{ mA})(1.8 \text{ k}\Omega) = 20 \text{ V} - 12.42 \text{ V} \\ &= 7.58 \text{ V} \end{aligned}$$

$$\begin{aligned} (d) \quad V_{DS} &= V_D - V_S \\ \text{or} \quad V_S &= V_D - V_{DS} \\ &= 7.58 \text{ V} - 7.23 \text{ V} \\ &= 0.35 \text{ V} \end{aligned}$$

IMPORTANT EQUATIONS FOR DC ANALYSIS OF MOSFET

For D-MOSFET

$$I_D = I_{DSS} \left(\frac{1 - V_{GS}}{V_P} \right)^2$$

For E-MOSFET

$$I_D = k(V_{GS} - V_T)^2$$

BIASING OF E-MOSFET

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution quite different from the preceding sections. First and foremost, recall that for the *n*-channel enhancement-type MOSFET, the drain current is zero for levels of gate-to-source voltage less than the threshold level $V_{GS(Th)}$, as shown in Fig. 6.35.

levels of V_{GS} greater than $V_{GS(Th)}$, the drain current is defined by

$$I_D = k(V_{GS} - V_{GS(Th)})^2 \quad (6.25)$$

TRANSFER CHARACTERISTICS OF N-CHANNEL EMOSFET

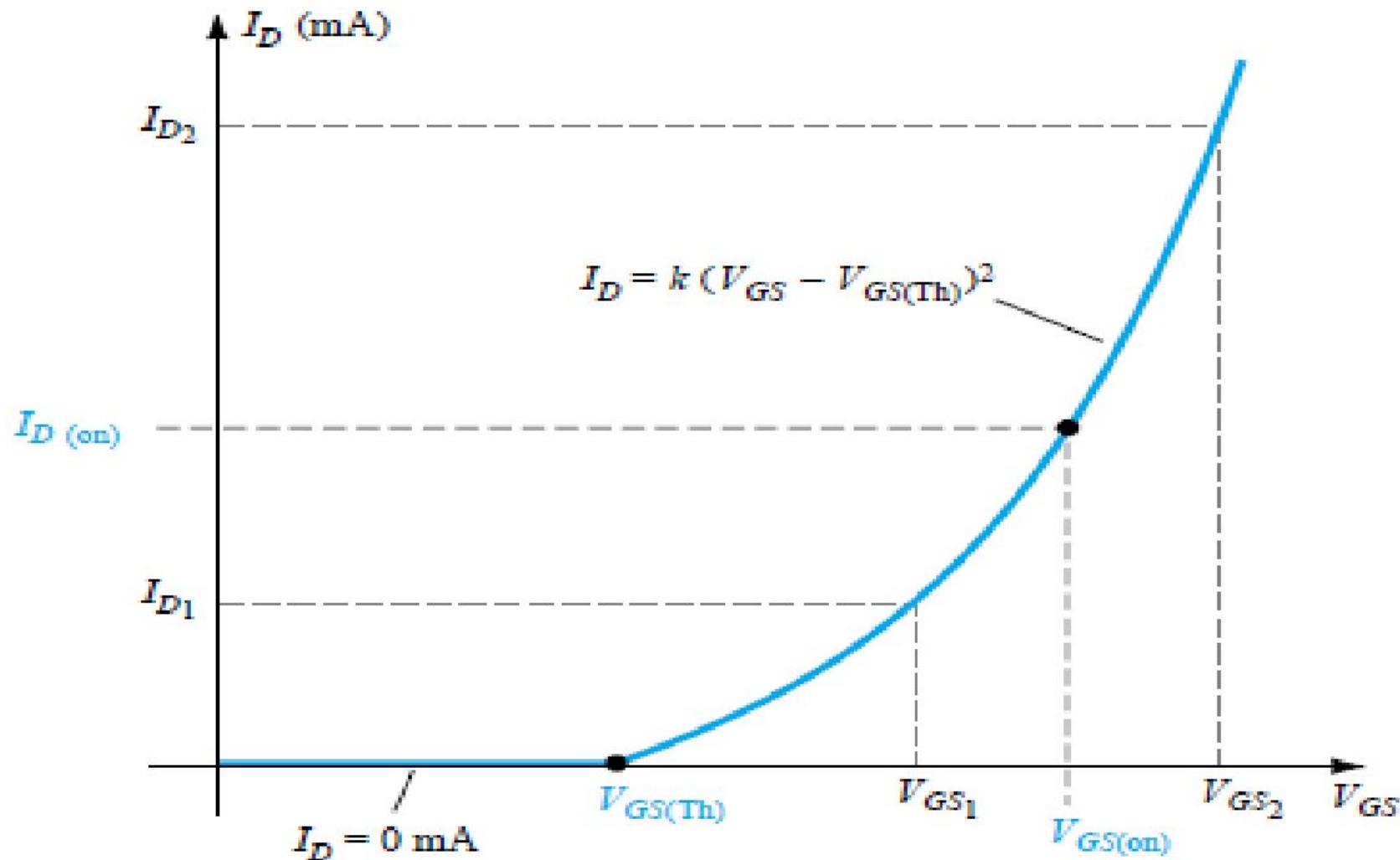


Figure 6.35 Transfer characteristics of an n-channel enhancement-type MOSFET.

BIASING OF E-MOSFET

Since specification sheets typically provide the threshold voltage and a level of drain current ($I_{D(on)}$) and its corresponding level of $V_{GS(on)}$, two points are defined immediately as shown in Fig. 6.35. To complete the curve, the constant k of Eq. (6.25) must be determined from the specification sheet data by substituting into Eq. (6.25) and solving for k as follows:

$$I_D = k(V_{GS} - V_{GS(Th)})^2$$

$$I_{D(on)} = k(V_{GS(on)} - V_{GS(Th)})^2$$

and

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2} \quad (6.26)$$

Once k is defined, other levels of I_D can be determined for chosen values of V_{GS} . Typically, a point between $V_{GS(Th)}$ and $V_{GS(on)}$ and one just greater than $V_{GS(on)}$ will provide a sufficient number of points to plot Eq. (6.25) (note I_{D1} and I_{D2} on Fig. 6.35).

1. DRAIN TO GATE BIAS

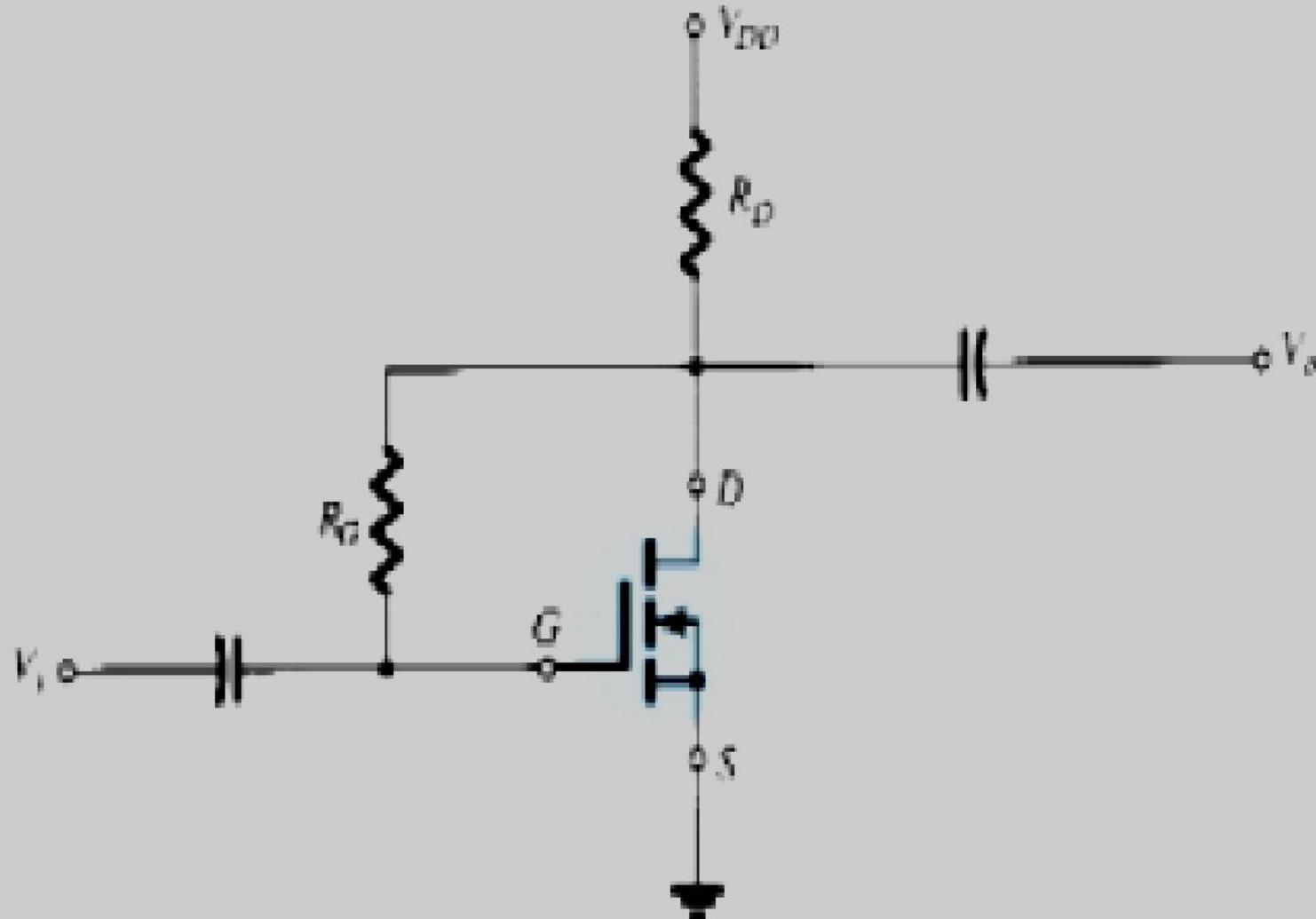


Figure 6.36 Feedback biasing arrangement.

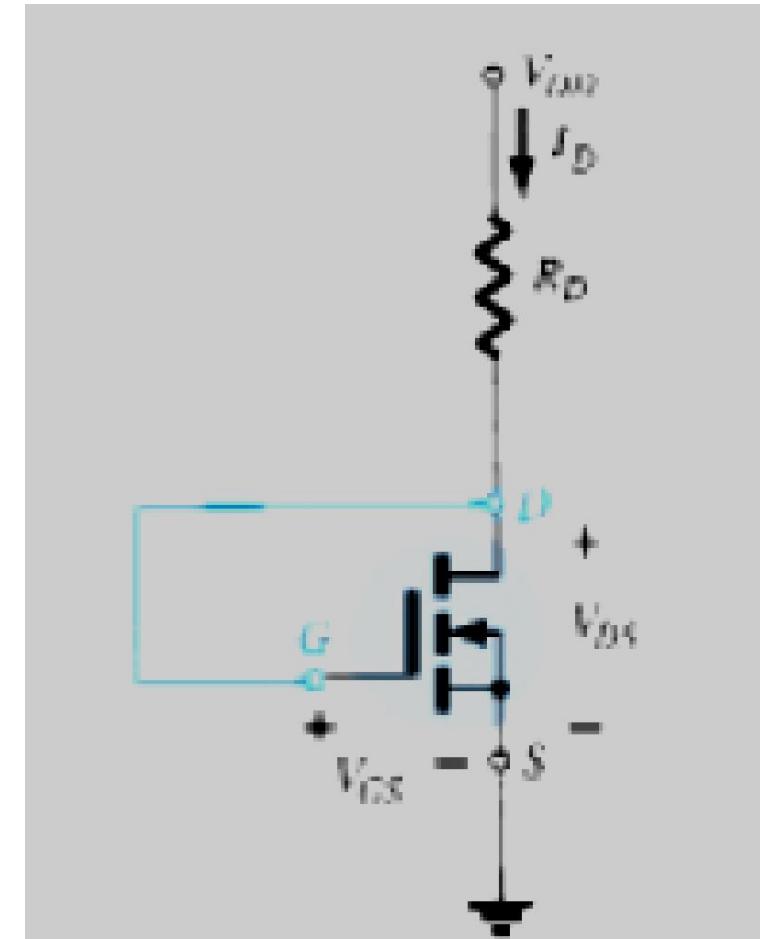


Figure 6.37 DC equivalent of the network of Fig. 6.36.

1. DRAIN TO GATE BIAS

A popular biasing arrangement for enhancement-type MOSFETs is provided in Fig. 6.36. The resistor R_G brings a suitably large voltage to the gate to drive the MOSFET “on.” Since $I_G = 0$ mA and $V_{RG} = 0$ V, the dc equivalent network appears as shown in Fig. 6.37.

A direct connection now exists between drain and gate, resulting in

$$V_D = V_G$$

and

$$V_{DS} = V_{GS} \quad (6.27)$$

For the output circuit,

$$V_{DS} = V_{DD} - I_D R_D$$

which becomes the following after substituting Eq. (6.27):

$$V_{GS} = V_{DD} - I_D R_D \quad (6.28)$$

The result is an equation that relates the same two variables as Eq. (6.25), permitting the plot of each on the same set of axes.

1. DRAIN TO GATE BIAS

Since Eq. (6.28) is that of a straight line, the same procedure described earlier can be employed to determine the two points that will define the plot on the graph. Substituting $I_D = 0 \text{ mA}$ into Eq. (6.28) gives

$$V_{GS} = V_{DD}|_{I_D = 0 \text{ mA}} \quad (6.29)$$

Substituting $V_{GS} = 0 \text{ V}$ into Eq. (6.28), we have

$$I_D = \frac{V_{DD}}{R_D} \Big|_{V_{GS} = 0 \text{ V}} \quad (6.30)$$

The plots defined by Eqs. (6.25) and (6.28) appear in Fig. 6.38 with the resulting operating point.

1. DRAIN TO GATE BIAS

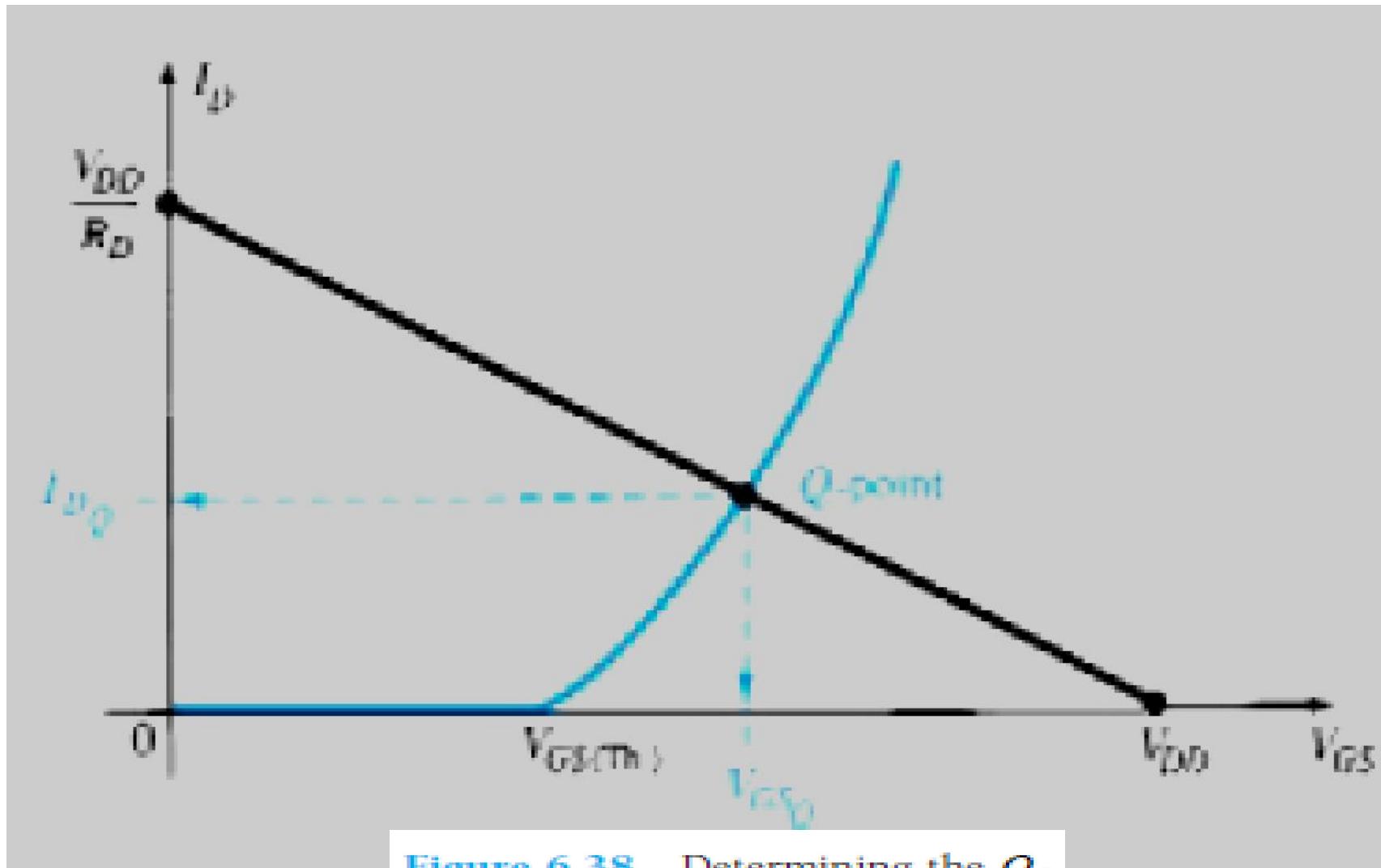


Figure 6.38 Determining the *Q*-point for the network of Fig.

EXAMPLE

Determine I_{DQ} and V_{DSQ} for the enhancement-type MOSFET of Fig. 6.39.

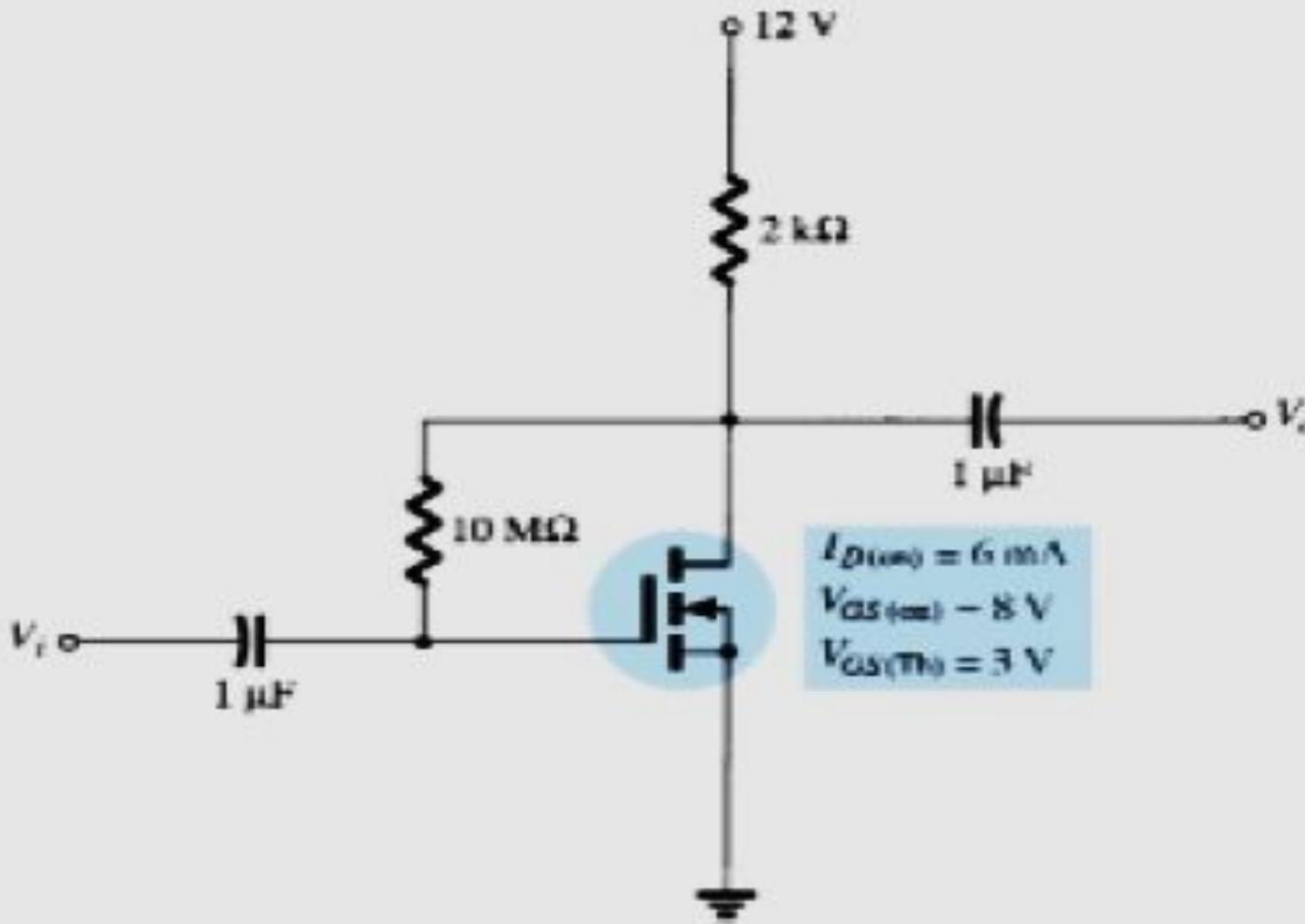


Figure 6.39 Example 6.11.

SOLUTION

Plotting the Transfer Curve:

Two points are defined immediately as shown in Fig. 6.40. Solving for k :

$$\begin{aligned}\text{Eq. (6.26): } k &= \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2} \\ &= \frac{6 \text{ mA}}{(8 \text{ V} - 3 \text{ V})^2} = \frac{6 \times 10^{-3}}{25} \text{ A/V}^2 \\ &= 0.24 \times 10^{-3} \text{ A/V}^2\end{aligned}$$

For $V_{GS} = 6 \text{ V}$ (between 3 and 8 V):

$$\begin{aligned}I_D &= 0.24 \times 10^{-3}(6 \text{ V} - 3 \text{ V})^2 = 0.24 \times 10^{-3}(9) \\ &= 2.16 \text{ mA}\end{aligned}$$

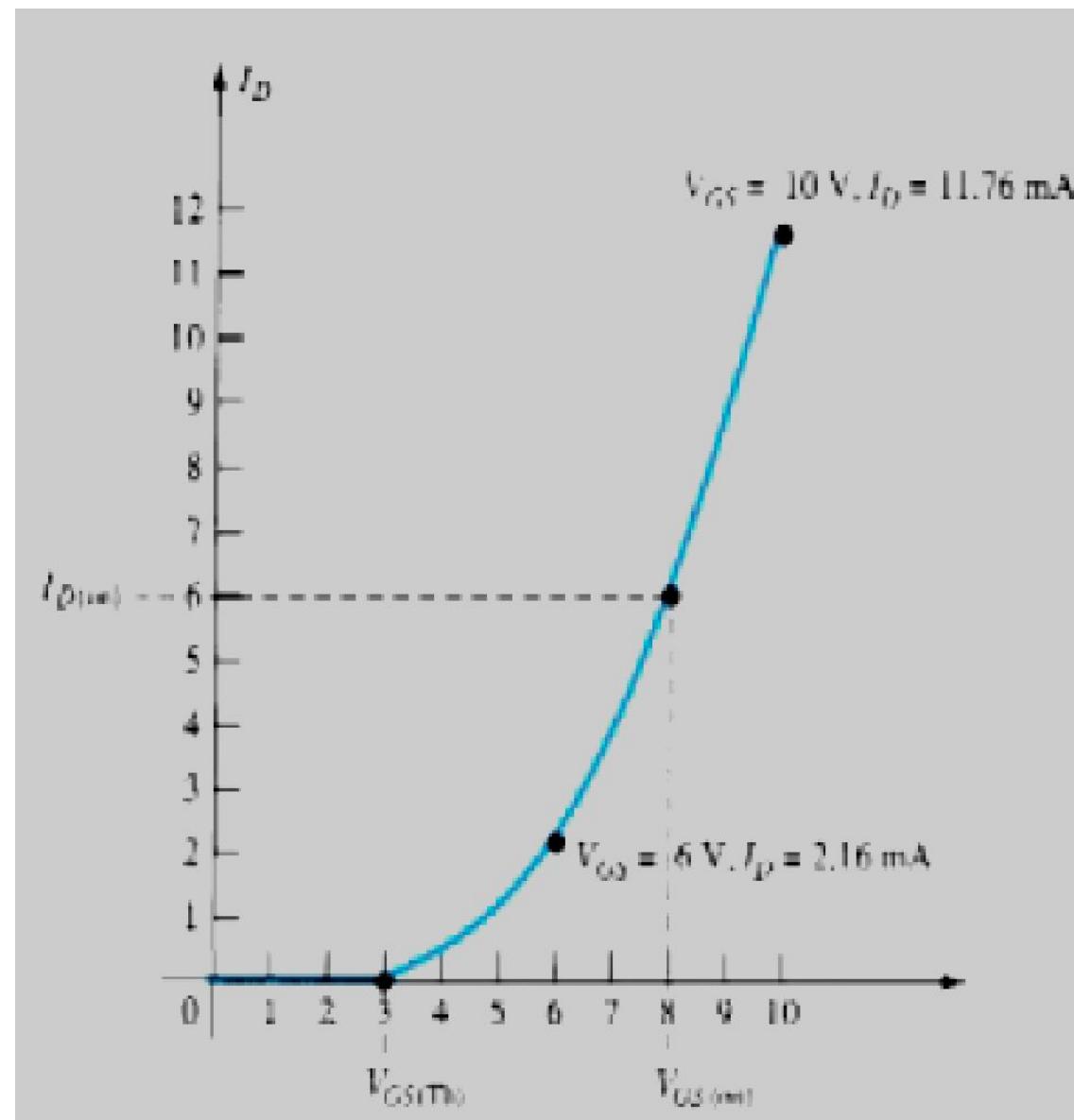


Figure 6.40 Plotting the transfer curve for the MOSFET of Fig.

SOLUTION

as shown on Fig. 6.40. For $V_{GS} = 10$ V (slightly greater than $V_{GS(Th)}$):

$$\begin{aligned}I_D &= 0.24 \times 10^{-3}(10 \text{ V} - 3 \text{ V})^2 = 0.24 \times 10^{-3}(49) \\&= 11.76 \text{ mA}\end{aligned}$$

as also appearing on Fig. 6.40. The four points are sufficient to plot the full curve for the range of interest as shown in Fig. 6.40.

For the Network Bias Line:

$$\begin{aligned}V_{GS} &= V_{DD} - I_D R_D \\&= 12 \text{ V} - I_D(2 \text{ k}\Omega)\end{aligned}$$

$$\text{Eq. (6.29): } V_{GS} = V_{DD} = 12 \text{ V} \Big|_{I_D = 0 \text{ mA}}$$

$$\text{Eq. (6.30): } I_D = \frac{V_{DD}}{R_D} = \frac{12 \text{ V}}{2 \text{ k}\Omega} = 6 \text{ mA} \Big|_{V_{GS} = 0 \text{ V}}$$

The resulting bias line appears in Fig. 6.41.

At the operating point:

$$I_{DQ} = 2.75 \text{ mA}$$

$$V_{GSQ} = 6.4 \text{ V}$$

and

$$V_{DSQ} = V_{GSQ} = 6.4 \text{ V}$$

with

SOLUTION

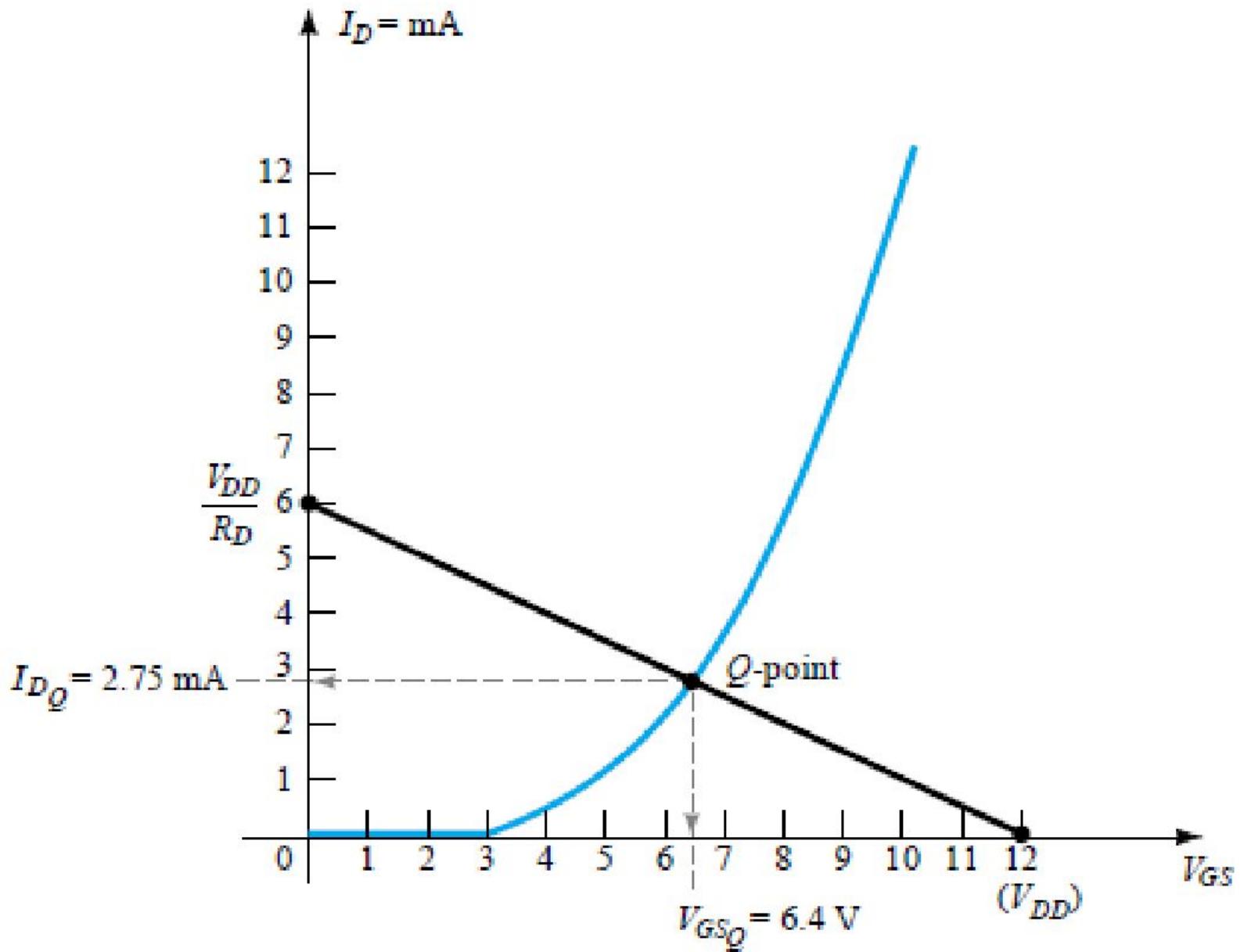


Figure 6.41 Determining the *Q*-point for the network of Fig. 6.39.

2. POTENTIAL DIVIDER BIAS

A second popular biasing arrangement for the enhancement-type MOSFET appears in Fig. 6.42. The fact that $I_G = 0 \text{ mA}$ results in the following equation for V_{GG} as derived from an application of the voltage-divider rule:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \quad (6.31)$$

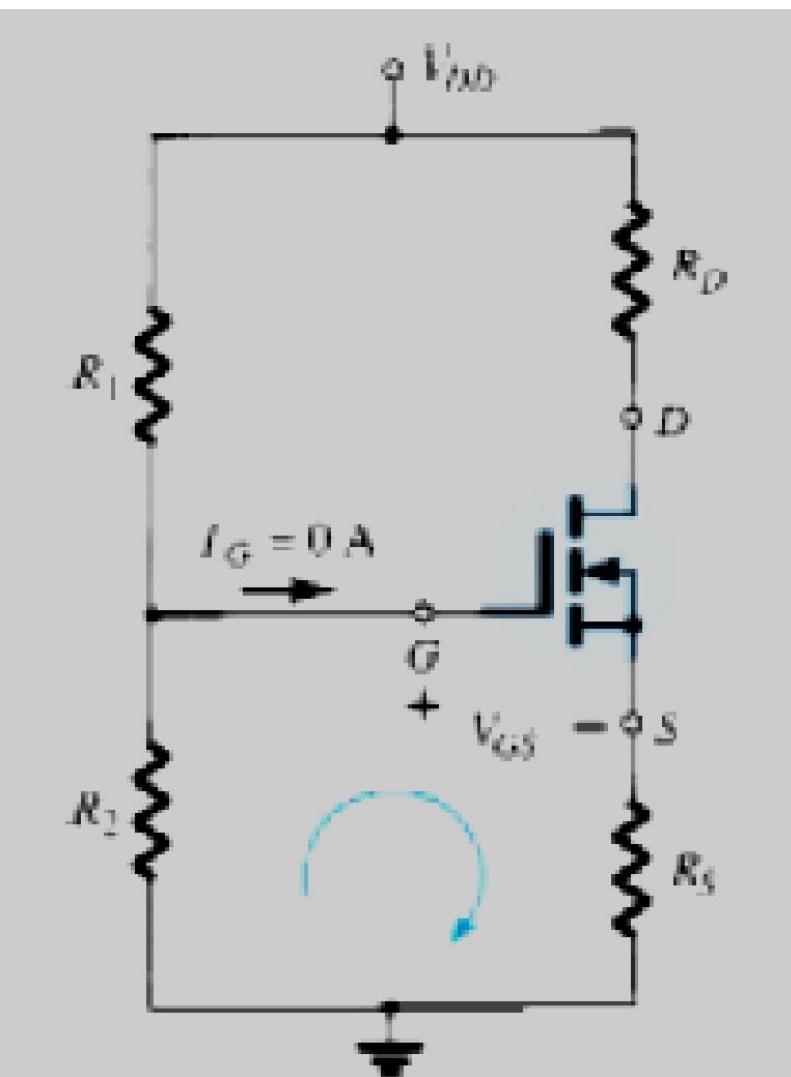


Figure 6.42 Voltage-divider biasing arrangement for an n-channel enhancement MOSFET.

2. POTENTIAL DIVIDER BIAS

Applying Kirchhoff's voltage law around the indicated loop of Fig. 6.42 will result in

$$+V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

or

$$V_{GS} = V_G - I_D R_S \quad (6.32)$$

For the output section:

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

or

$$V_{DS} = V_{DD} - I_D(R_S + R_D) \quad (6.33)$$

Since the characteristics are a plot of I_D versus V_{GS} and Eq. (6.32) relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection. Once I_{DQ} and V_{GSQ} are known, all the remaining quantities of the network such as V_{DS} , V_D , and V_S can be determined.

EXAMPLE

Determine I_{DQ} , V_{GSQ} , and V_{DS} for the network of Fig. 6.43.

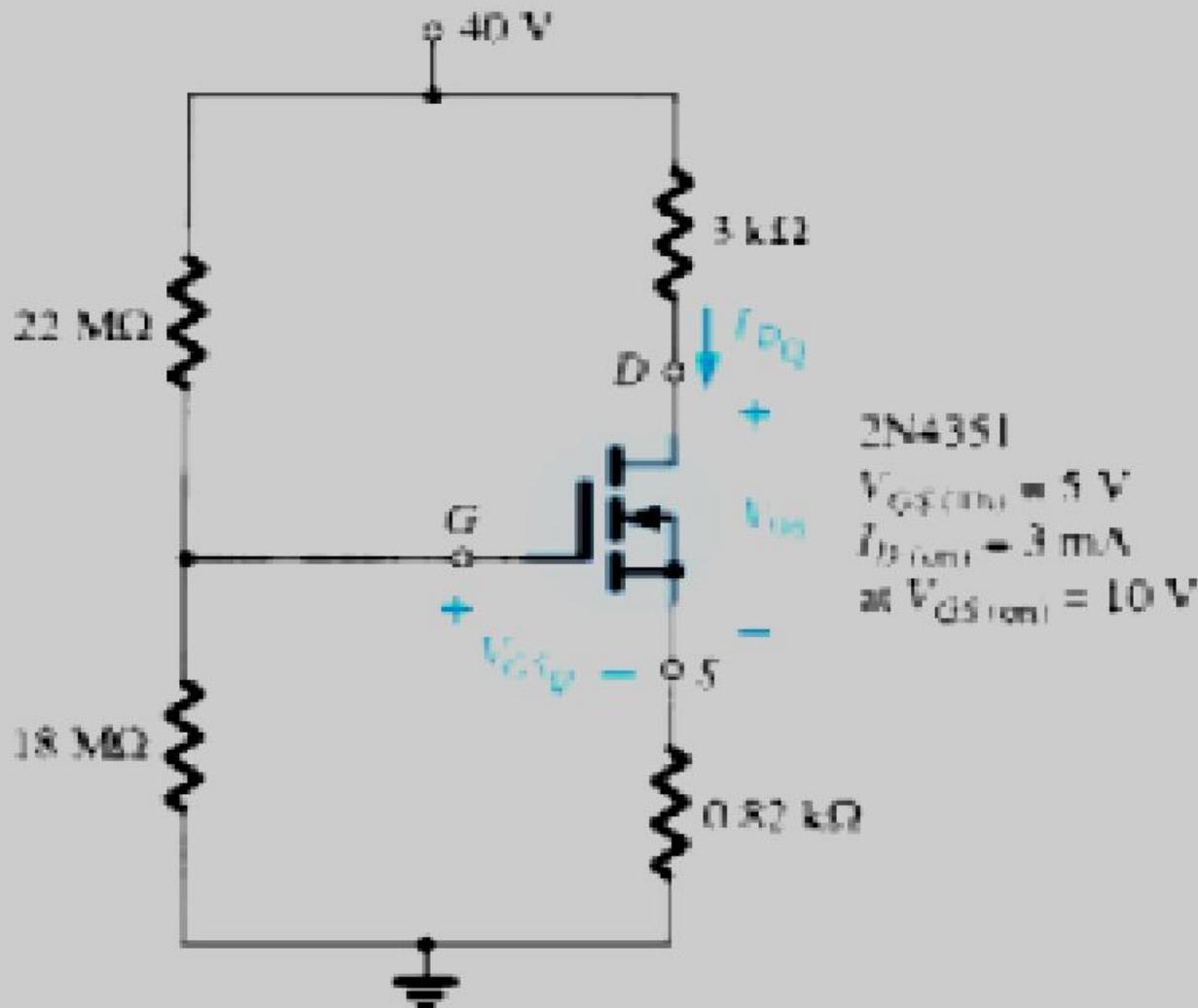


Figure 6.43 Example 6.12.

SOLUTION

Network:

$$\text{Eq. (6.31): } V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18 \text{ M}\Omega)(40 \text{ V})}{22 \text{ M}\Omega + 18 \text{ M}\Omega} = 18 \text{ V}$$

$$\text{Eq. (6.32): } V_{GS} = V_G - I_D R_S = 18 \text{ V} - I_D(0.82 \text{ k}\Omega)$$

When $I_D = 0 \text{ mA}$,

$$V_{GS} = 18 \text{ V} - (0 \text{ mA})(0.82 \text{ k}\Omega) = 18 \text{ V}$$

as appearing on Fig. 6.44. When $V_{GS} = 0 \text{ V}$,

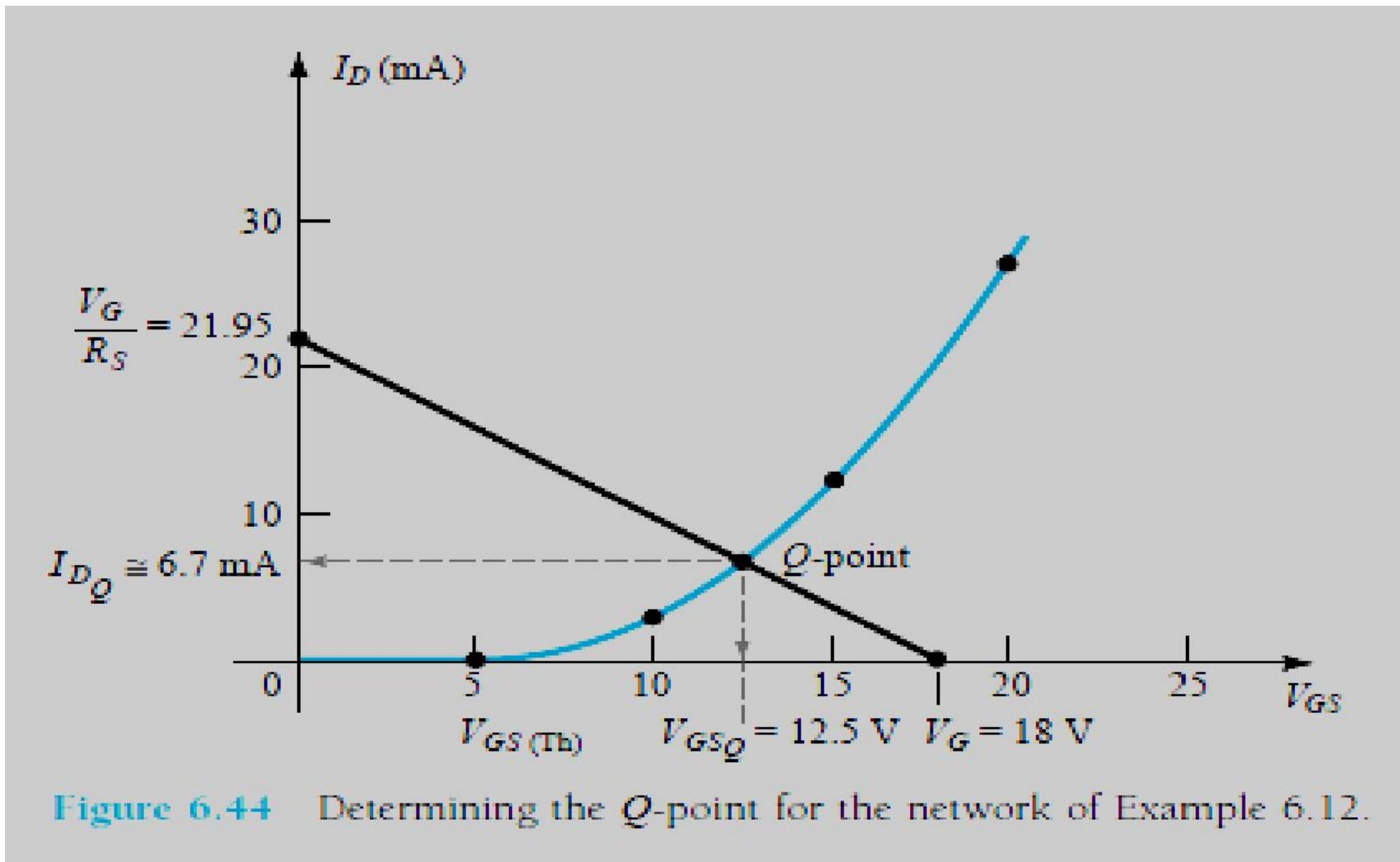
$$V_{GS} = 18 \text{ V} - I_D(0.82 \text{ k}\Omega)$$

$$0 = 18 \text{ V} - I_D(0.82 \text{ k}\Omega)$$

$$I_D = \frac{18 \text{ V}}{0.82 \text{ k}\Omega} = 21.95 \text{ mA}$$

as appearing on Fig. 6.44.

SOLUTION



SOLUTION

Device:

$$V_{GS(\text{Th})} = 5 \text{ V}, \quad I_{D(\text{on})} = 3 \text{ mA} \text{ with } V_{GS(\text{on})} = 10 \text{ V}$$

$$\begin{aligned}\text{Eq. (6.26): } k &= \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2} \\ &= \frac{3 \text{ mA}}{(10 \text{ V} - 5 \text{ V})^2} = 0.12 \times 10^{-3} \text{ A/V}^2\end{aligned}$$

and

$$\begin{aligned}I_D &= k(V_{GS} - V_{GS(\text{Th})})^2 \\ &= 0.12 \times 10^{-3}(V_{GS} - 5)^2\end{aligned}$$

which is plotted on the same graph (Fig. 6.44). From Fig. 6.44,

$$I_{D_Q} \approx 6.7 \text{ mA}$$

$$V_{GSQ} = 12.5 \text{ V}$$

$$\begin{aligned}\text{Eq. (6.33): } V_{DS} &= V_{DD} - I_D(R_S + R_D) \\ &= 40 \text{ V} - (6.7 \text{ mA})(0.82 \text{ k}\Omega + 3.0 \text{ k}\Omega) \\ &= 40 \text{ V} - 25.6 \text{ V} \\ &= 14.4 \text{ V}\end{aligned}$$

Example

Determine V_{GS} and V_{DS} for the E-MOSFET circuit in figure below. Assume this particular MOSFET has minimum values of $I_{D(on)} = 200 \text{ mA}$ at $V_{GS} = 4 \text{ V}$ and $V_{GS(th)} = 2 \text{ V}$.

Solution

Find K using the minimum value of $I_{D(on)}$:

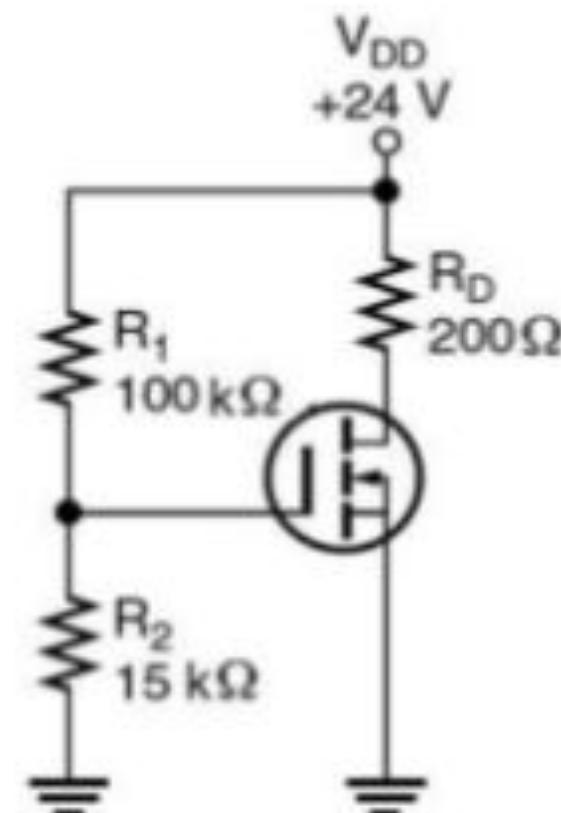
$$K = I_{D(on)} / (V_{GS} - V_{GS(th)})^2 = 200 \text{ mA} / (4\text{V} - 2\text{V})^2 \\ = 50 \text{ mA/V}^2$$

Now calculate I_D for $V_{GS} = 3.13 \text{ V}$:

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (50 \text{ mA/V}^2)(3.13 \text{ V} - 2 \text{ V})^2 \\ = 63.8 \text{ mA}$$

Finally, calculate V_{DS} :

$$V_{DS} = V_{DD} - I_D R_D = 24 \text{ V} - (63.8 \text{ mA})(200 \Omega) = \mathbf{11.2 \text{ V}}$$



For the circuit shown in Fig. , assume that $R_1 = 30 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$, $R_D = 40 \text{ k}\Omega$, $V_{DD} = 10 \text{ V}$, $V_T = 1 \text{ V}$, $V_{GS} = 2 \text{ V}$ and $K = 0.1 \text{ mA/V}^2$. Find I_D and V_{DS} .

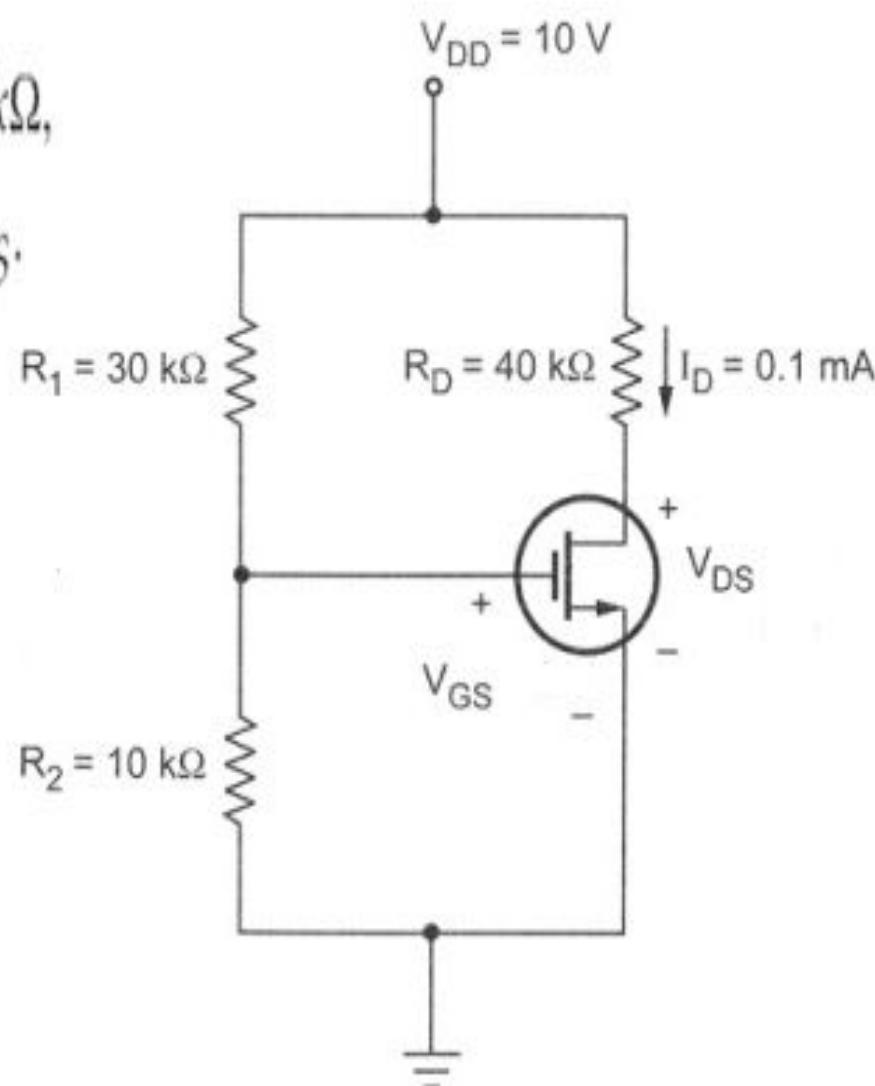


Fig.

TABLE 6.1 FET Bias Configurations

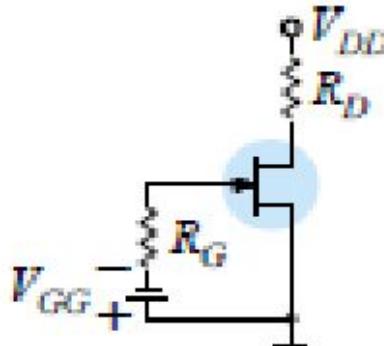
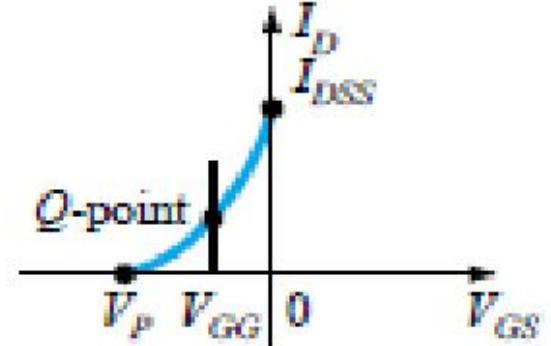
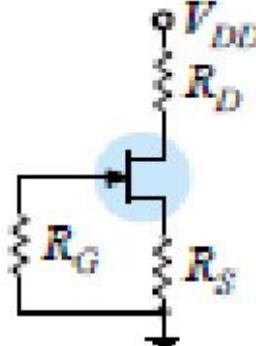
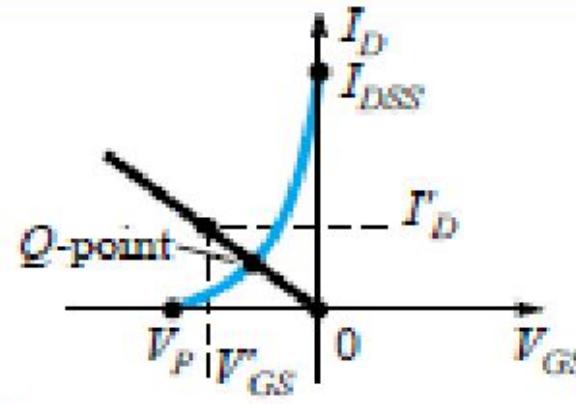
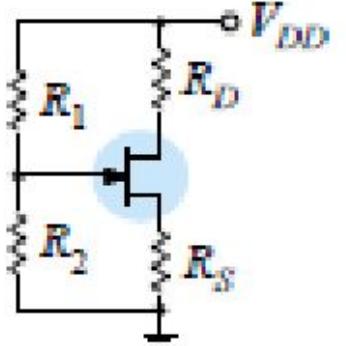
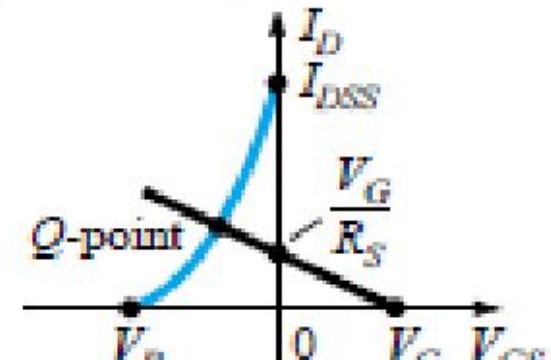
Type	Configuration	Pertinent Equations	Graphical Solution
JFET Fixed-bias		$V_{GSQ} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	

TABLE 6.1 FET Bias Configurations

Type	Configuration	Pertinent Equations	Graphical Solution
Enhancement type MOSFET Feedback configuration		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement-type MOSFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	