

* Comparison of three configurations of BJT -

Parameters	common Base	common Emitter	common Collector
I/I _P Resistance	Low	Low	High
o/I _P Resistance	High	High	Low
current Gain	< 1	20 to 300	50 to 500
Voltage gain	>150	>500	< 1
Application	For High freq amplifier	For Audio amplifier	For impedance matching

* Biasing of BJT -

The basic function of transistor is to perform amplification. Necessary requirement during amplification is that magnitude of signal should increase & there should be no change in signal shape.

- The process of rising the strength of weak signal without any change in its original shape is known as faithful amplification.
- Basic condition for faithful amplification is BE junction must be forward bias & BC junction must be reverse biased during amplification.

- It is necessary to fulfil this condition & this is done by proper biasing.

The proper flow of zero signal collector current & the maintenance of proper V_{CE} during passage of signal is known as transistor biasing.

- This is achieved with bias battery & associative circuit element. The performance of transistor depends on dc bias condition.

* Operating point -

Biasing means applying

For transistor amplification to dc voltages to establish a fixed level of current & voltage.

- For transistor amplifier the resulting dc current & voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal.

- Because the operating point is a fixed point on the characteristics, it is also called the quiescent point (Q point).

- By definition, quiescent means quiet, still, inactive.

- The biasing circuit can be designed to set the device operation at ' Q ' point within the active region.

- The DC bias should remain constant so that there will be no shifting in operating point but there are certain factors such as temperature variation & unit to unit manufacturing.

Variation of β :-

It is seen that transistor of same type may have different value of several parameter.

- If transistor in given circuit is replaced by another transistor of same type, transistor parameter changes considerably.

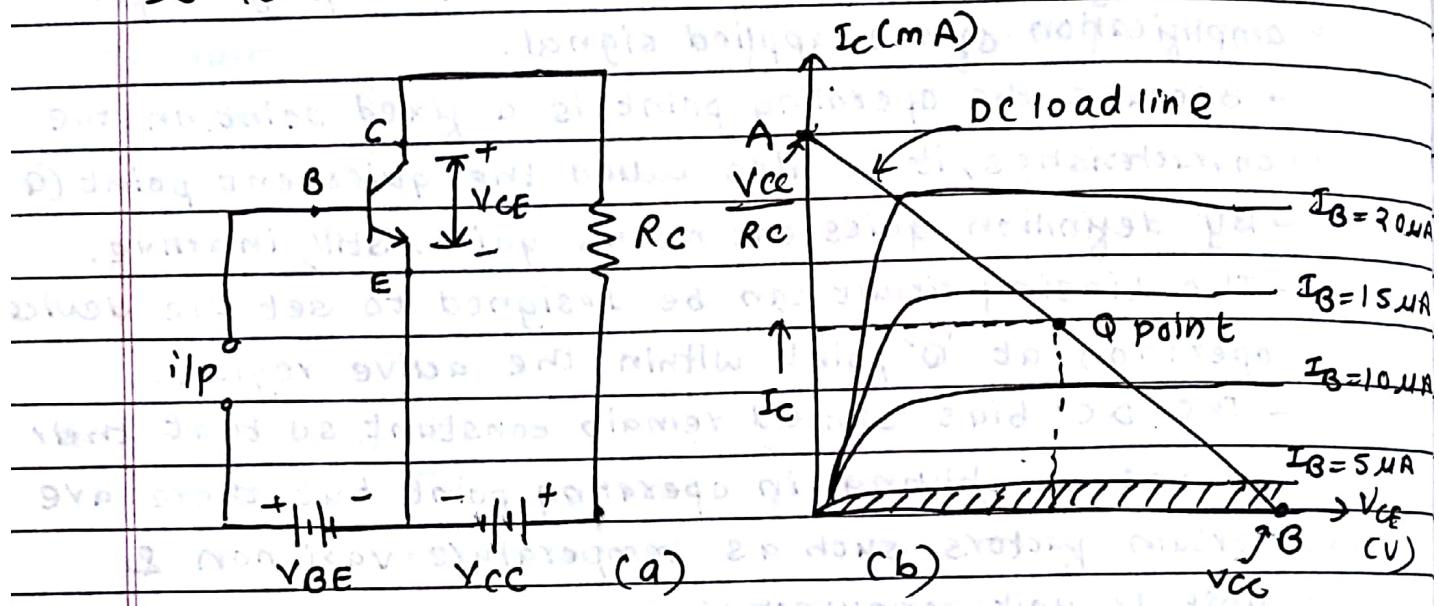
- If β changes, it may shift operating point.

* Load Line -

The straight line drawn on the characteristics of transistor amplifier circuit which gives the value of collector current I_C & collector to emitter voltage V_{CE} corresponding to either DC or AC i/p conditions is called load line.

DC load line -

The straight line drawn on o/p characteristics of transistor amplifier which gives the DC values of collector current I_C & collector to emitter voltage V_{CE} corresponding to zero signal ie DC conditions, is called DC load line.



- consider CE configuration with NPN transistor circuit.

- In this circuit when zero i/p signal is applied, DC conditions remains unchanged.

- o/p characteristics is shown in figure (b).

- The value of V_{CE} at anytime 't' is given by,

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C = \left(\frac{-1}{R_C} \right) V_{CE} + \frac{V_{CC}}{R_C}$$

Comparing this equation with the equation of straight line, $y = mx + c$ $\therefore m = -\frac{1}{R_C}$

- so the slope of this line depends on load resistance.

- To plot load line, we need two end points of straight line. These two points are locations,

case(i) when collector current I_c is zero, then V_{CE} is max & is equal to V_{CC}

$$\therefore V_{CE} = V_{CC} - I_c R_C$$

$$V_{CE(\max)} = V_{CC} \quad \because I_c = 0$$

This gives first point 'B' having co-ordinates $(V_{CC}, 0)$ on the x-axis as shown in figure (b)

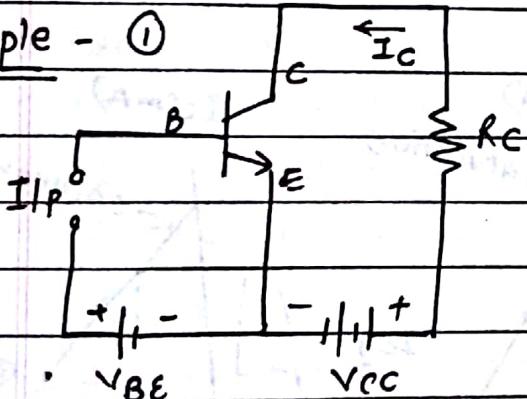
case(ii) When V_{CE} is zero, then collector current is max & is equal to V_{CC}/R_C

$$\therefore V_{CE} = V_{CC} - I_c R_C \text{ but } V_{CE} = 0$$

$$I_{C(\max)} = \frac{V_{CC}}{R_C}$$

This given second point 'A' having co-ordinates $(0, \frac{V_{CC}}{R_C})$ on 'y' axis as shown in fig (b)

Example - ①



For the circuit shown, draw DC load line.

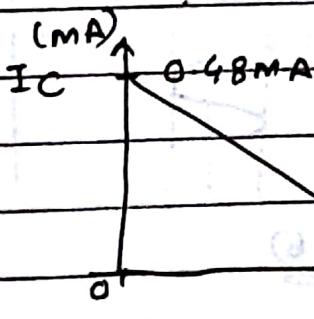
$$2019 - V_{CE} = V_{CC} - I_c R_C$$

case(i) $I_c = 0$

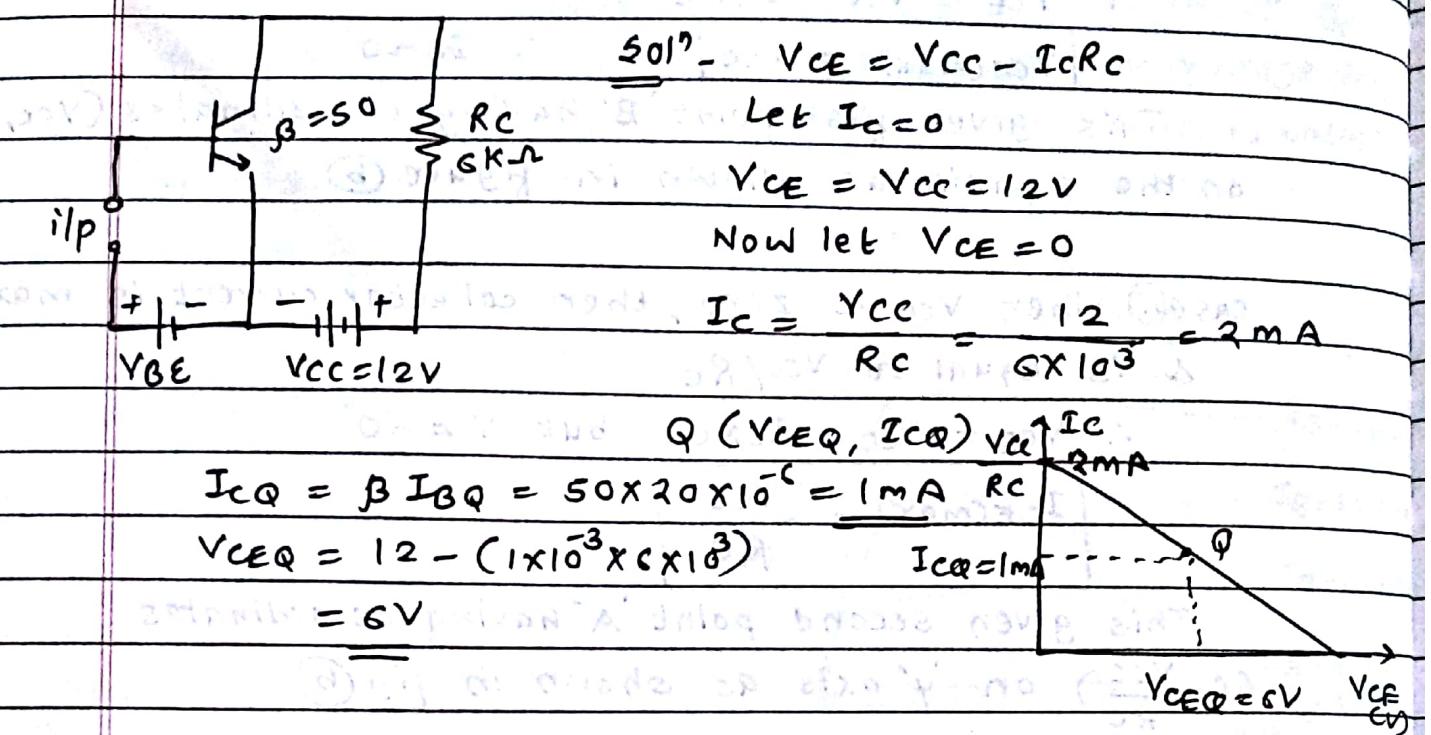
$$V_{CE(\max)} = V_{CC} = 12V$$

case(ii) $V_{CE} = 0$

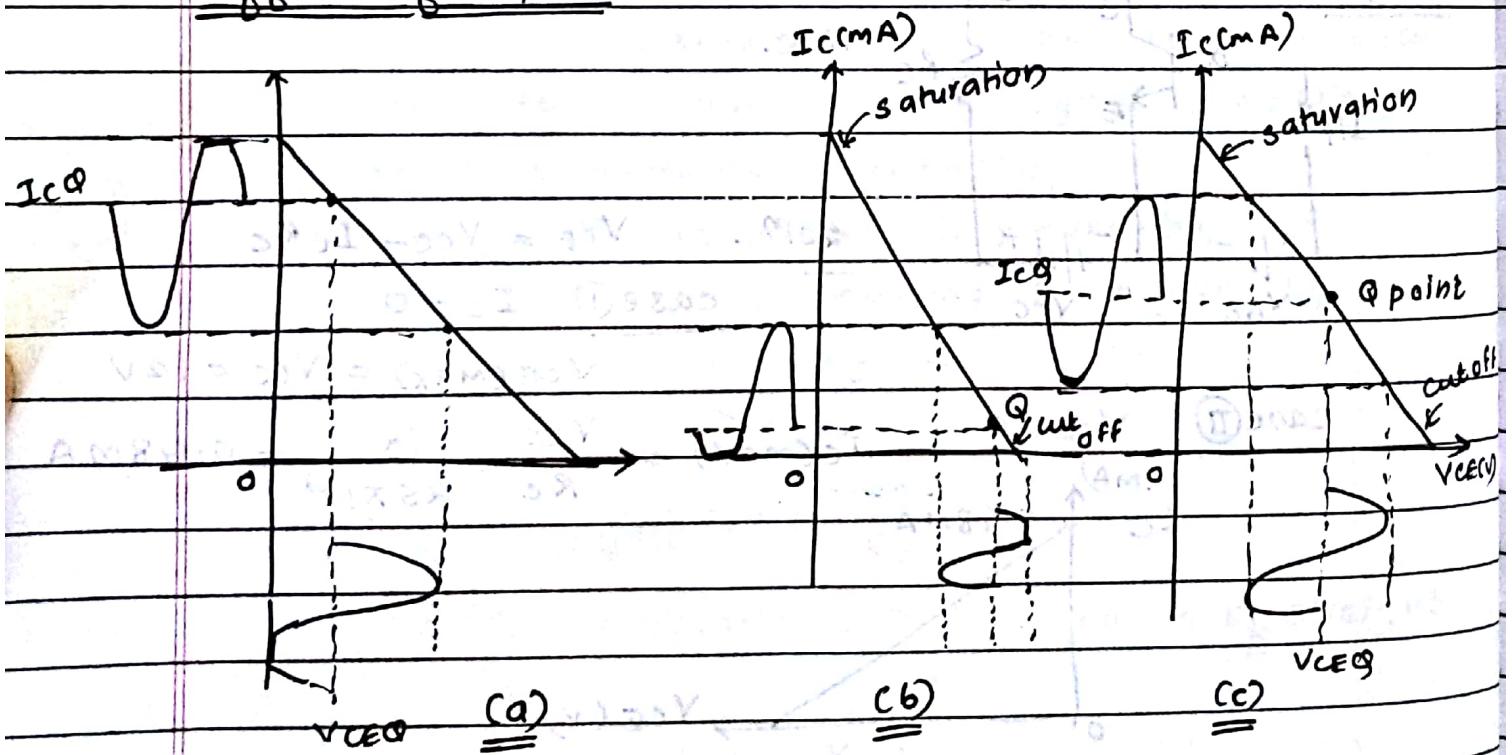
$$I_{C(\max)} = \frac{V_{CC}}{R_C} = \frac{12}{25 \times 10^3} = 0.48mA$$



iii) Draw DC load line, where will be Q point if zero signal
 $I_B = 20\text{mA}$ & $\beta = 50$ ie $I_{BQ} = 20\text{mA}$



* Effect of Q point :-



- It has been observed that under certain condition of QP, the location of Q point on the load line may cause one peak of o/p signal to be clipped.

- If Q point is located near the saturation point as shown in fig @. In this case during -ve half cycle of the i/p, transistor is driven into saturation.

As a result of this, the -ve peak of the i/p signal is clipped at the o/p.

- Consider Q point located near the cut off point as shown in fig (b), the transistor is driven into cut off. therefore, +ve peak of the input signal is clipped at the o/p.

- If Q point is located at the center of the load line as shown in fig (c), we get undistorted signal at the o/p.

* Transistor Biasing Techniques :-

In transistor amplifier circuits, the biasing is done with two power supplies V_{BB} & V_{CC} .

- The V_{BB} is used for biasing of E-B junction & V_{CC} supply for biasing both the junction of transistor.

- Following are the different biasing techniques of BJT.

1. Fixed Bias configuration

2. Emitter Bias configuration

3. collector- feedback configuration

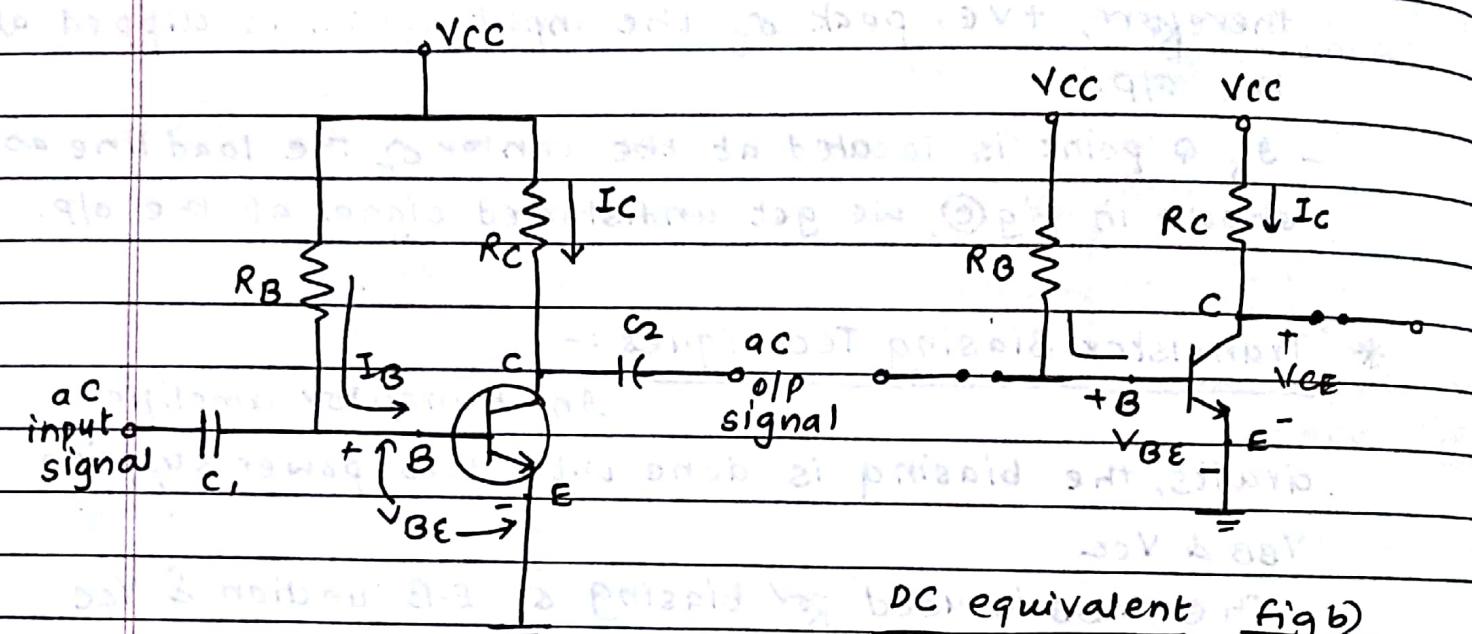
4. Voltage Divider Bias configuration

5. common Base configuration.

① Fixed Bias Configuration

This is the simplest transistor dc bias configuration.

- Even though the network employs an npn transistor, the equations & calculations apply equally well to a pnp transistor configuration merely by changing all current directions & voltage polarities.



DC equivalent (fig b)

Fixed Bias ckt (fig a)

DC Analysis :- for dc analysis, replace capacitors with an open circuit equivalent (\because for dc, $X_c = \frac{1}{2\pi f C} = \infty$)
- dc supply V_{cc} can be separated into two supplies (for analysis purposes only) as shown in fig b) to permit a separation of i/p & o/p ckt's.
It also reduces the linkage between the two to the base current I_B .

Base-Emitter Loop -

considering first base-emitter circuit loop as shown in fig.

Apply KVL in clockwise direction for the loop, $+V_{cc} - I_B R_B - V_{BE} = 0$



$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

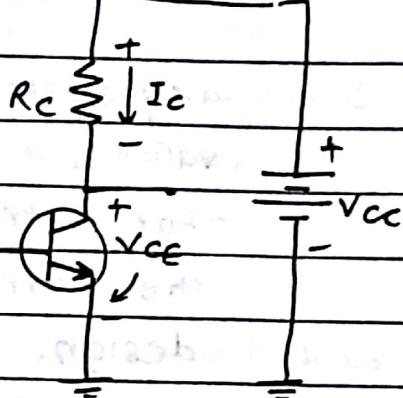
Collector-Emitter loop -

The collector current is related directly to I_B through $I_C = \beta I_B$

Apply KVL to top loop, in clockwise direction,

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$



Collector-emitter loop

$$\text{As we know, } V_{CE} = V_C - V_E, \text{ But } V_E = 0, \therefore V_{CE} = V_C$$

$$\& V_{BE} = V_B - V_E \quad \& V_E = 0, \quad V_{BE} = V_B$$

Ex ① Determine the following for the fixed bias configuration.

a. I_{BQ} & I_{CQ}

b. V_{CEQ}

c. V_B & V_C

d. V_{BC}

Sol-

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12V - 0.7V}{240k\Omega} = 47.08\mu A$$

$$I_{CQ} = \beta I_{BQ} = (50) \times (47.08\mu A) = 2.35mA$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 12V - (2.35mA \times 2.2k\Omega)$$

$$= 6.83V$$

$$V_B = V_{BE} = 0.7V$$

$$V_C = V_{CE} = 6.83V$$

$$V_{BC} = V_B - V_C = 0.7V - 6.83V$$

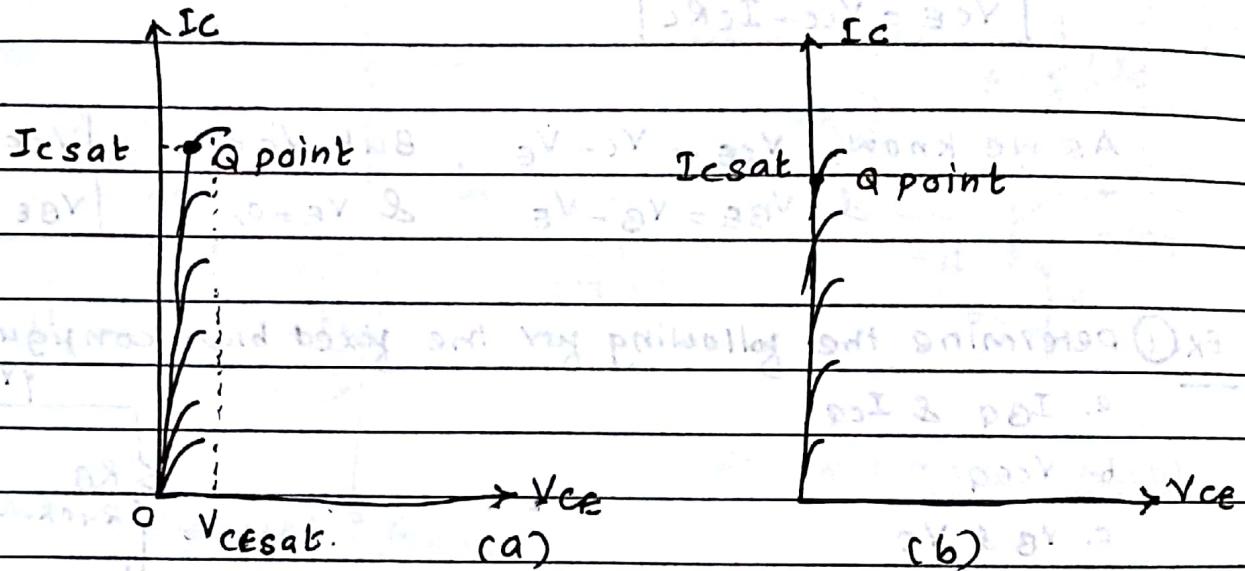
$$V_{BC} = -6.13V$$

-ve sign indicates BC junction is reverse biased, as it should be for linear amplification.

* Transistor saturation -

The term saturation is applied to any system where levels have reached their maximum values.

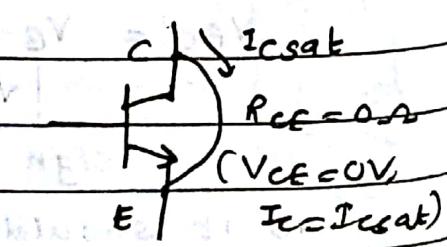
- For a transistor operating in the saturation region, the current is a maximum value for the particular design.
- Highest saturation level is defined by the maximum collector current as provided by the specification sheet.



saturation regions a) Actual b) Approximate

- In fig b) we approximate the curves in fig a), as a quick, direct method for determining the saturation levels.
- In fig b), the current is relatively high & the voltage V_{CE} is assumed to 0V.
- Applying Ohm's law, we can determine the resistance between collector & emitter terminals as follows -

$$R_{CE} = \frac{V_{CE} - 0V}{I_C} = \frac{0V}{I_{CSAT}} = 0\Omega$$



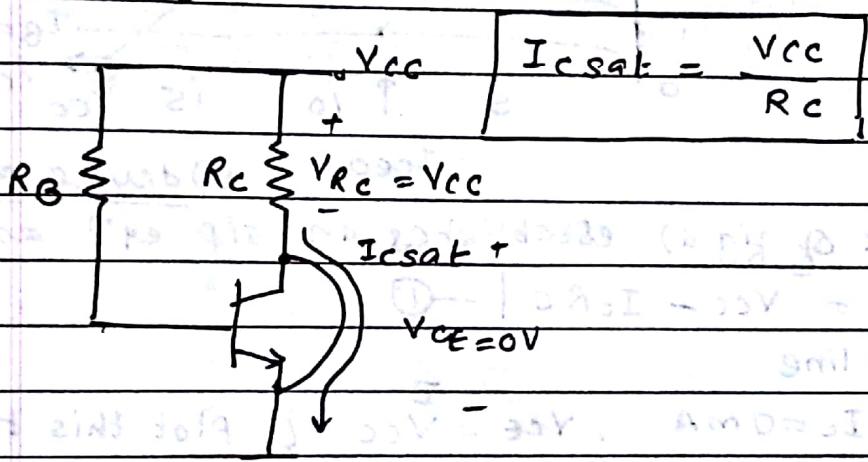
Determining I_{CSAT}

- To know the approximate maximum collector current (saturation level) for a particular design, simply insert a short circuit equivalent between collector & emitter of the transistor & calculate the resulting collector current:

- In short, set $V_{CE} = 0V$.

- For the fixed bias configuration, the short circuit has been applied, causing the voltage across R_C to be applied voltage, V_{CC}

The resulting saturation current for fixed bias configuration is



Determining I_{CSAT} for fixed bias configuration.

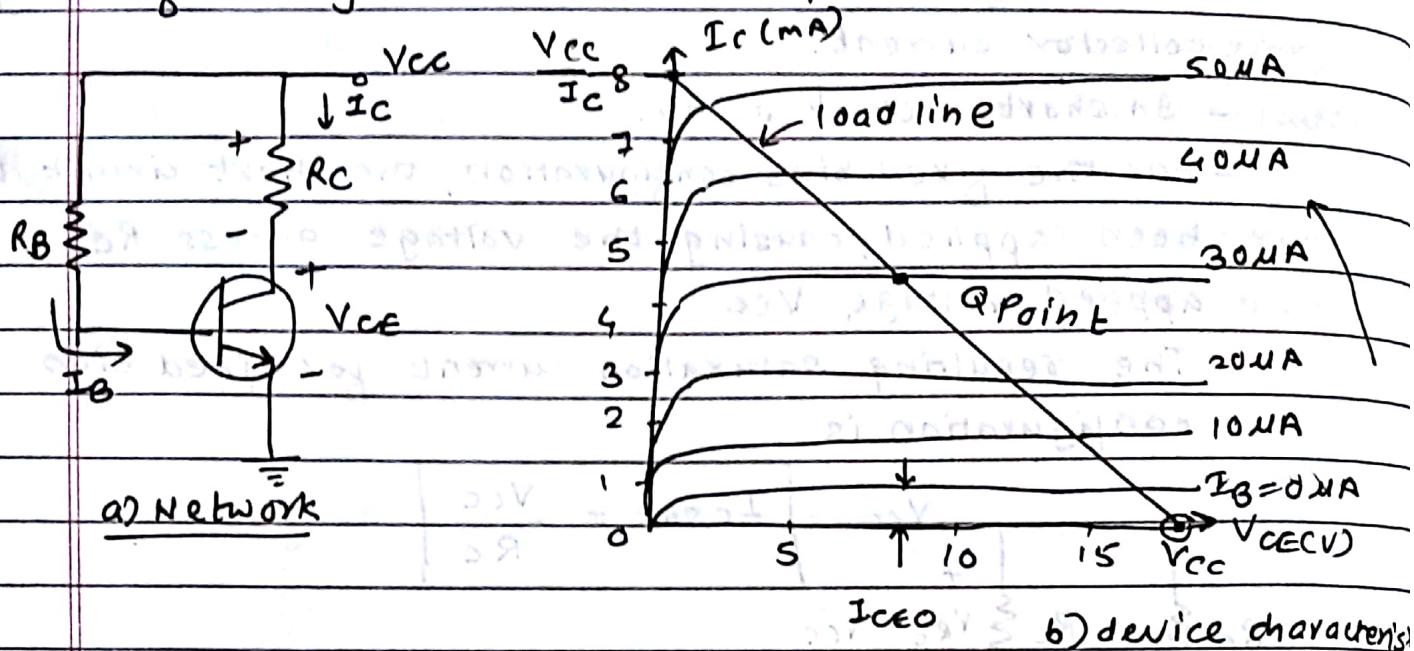
- Once I_{CSAT} is known, we have some idea of the maximum possible collector current for the chosen design and the level to stay below if we expect linear amplification.

* Determine the saturation level for the network in previous example.

$$I_{CSAT} = \frac{V_{CC}}{R_C} = \frac{12V}{2.2k\Omega} = 5.45mA$$

* Load Line Analysis -

The characteristics of the BJT are superimposed on a plot of the network equation defined by the same axis parameters.



- The network of fig a) establishes an op eq as

$$V_{CE} = V_{CC} - I_C R_C \quad \text{--- (1)}$$

To plot load line

Put $I_C = 0\text{mA}$, $V_{CE} = V_{CC}$ } plot this two
& Put $V_{CE} = 0\text{V}$, $I_C = \frac{V_{CC}}{R_C}$ } point on device
characteristics.

- We can draw the straight line established by these two points.

- The resulting line on the graph is called load line because it is defined by the load resistor R_C .

- If the level of I_B is changed by varying the value of R_B , the Q point moves up or down the load line as shown in fig c).

- If V_{CC} is held fixed & R_C increased, the load line will shift as shown in fig d).

- If I_B is held fixed, the Q point will move as shown in the same fig.

- If R_C is fixed, & V_{CC} decreased, the load line shifts

as shown in fig e)

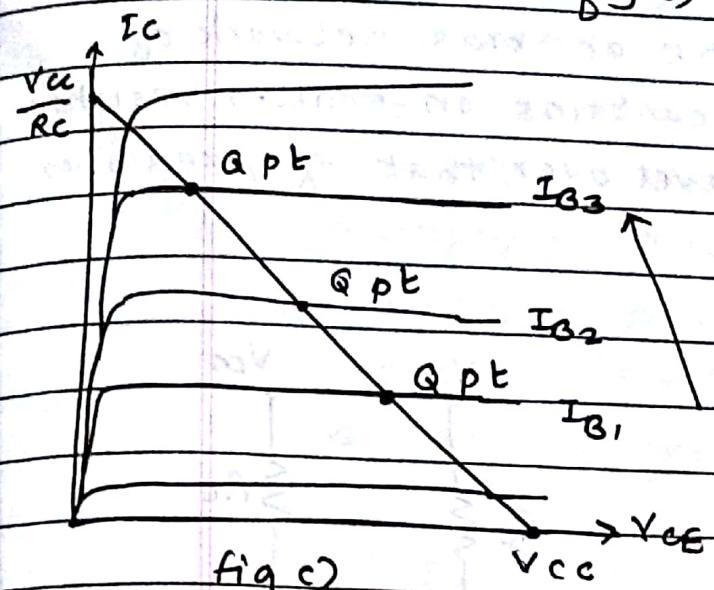


fig c)

Movement of Q pt with increasing level of I_B

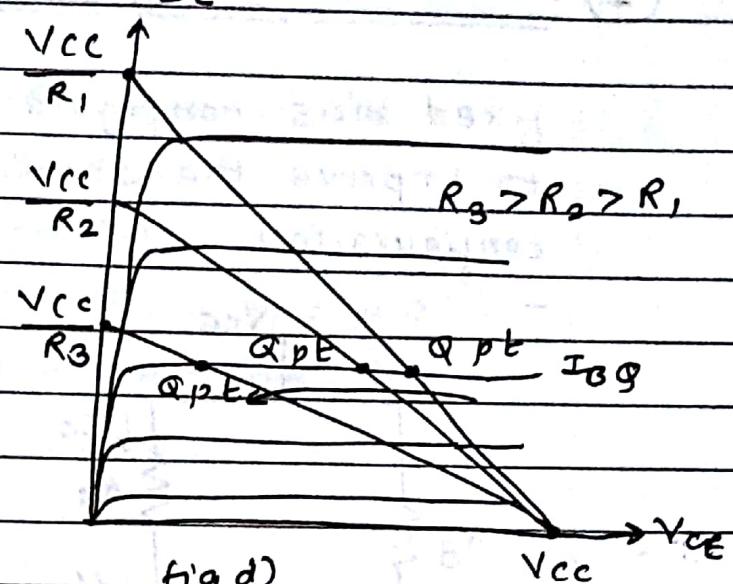


fig d)

Effect of an increasing level of R_C on load line & Q pt

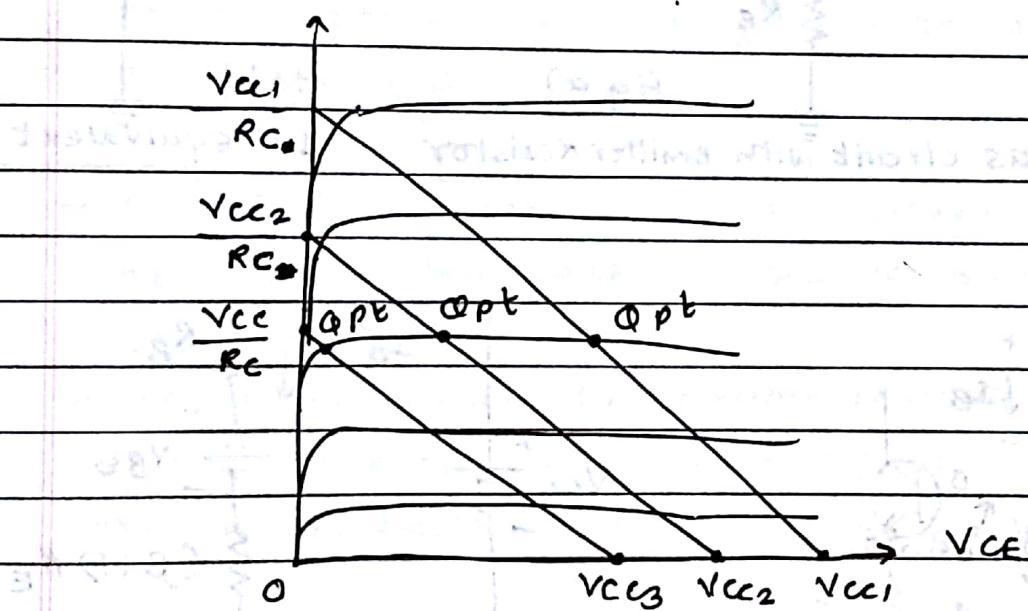


fig e)

Effect of lower values of V_{CC} on the load line & Q point

2. Emitter-Bias configuration -

The dc bias network of fixed bias configuration contains an emitter resistor to improve the stability level over that of fixed bias configuration.

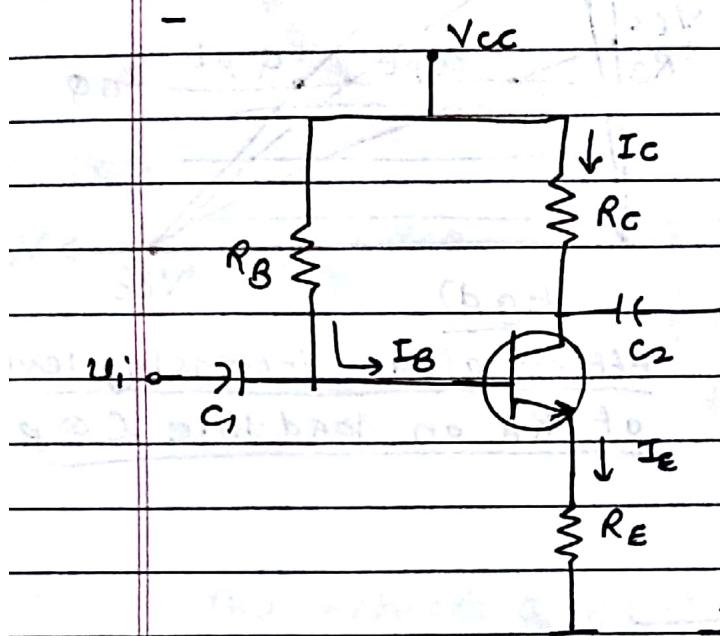
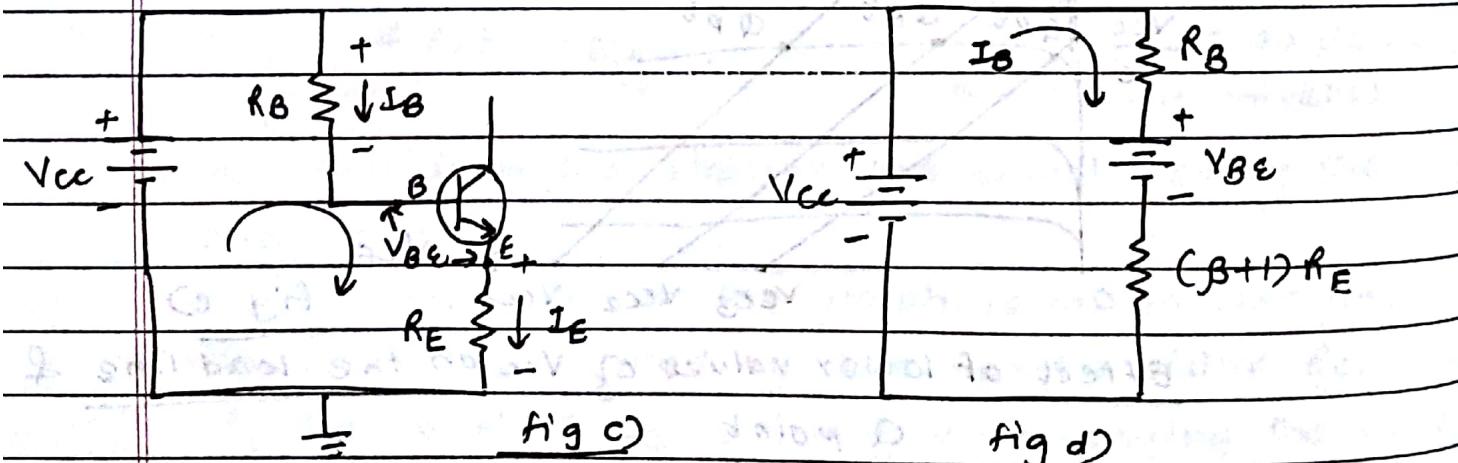
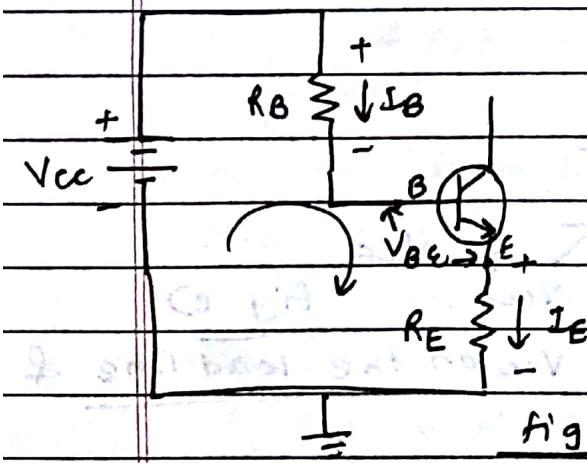
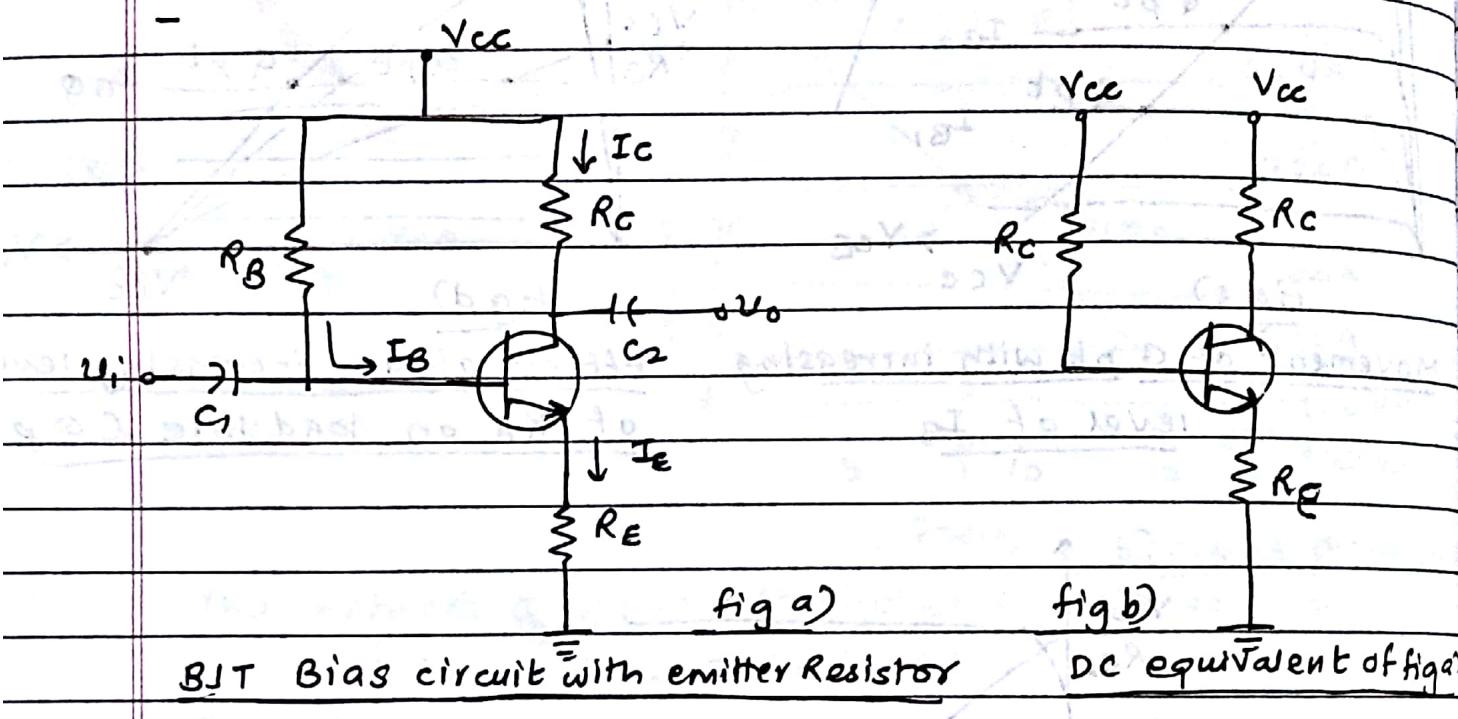


fig a)



BIP loop or Base Emitter loop :-

The Base-emitter loop of network in fig a) can be redrawn as shown in fig c) writing KVL in clockwise direction,

$$V_{cc} - I_B R_B - V_{BE} - I_E R_E = 0 \quad \text{--- (1)}$$

But $I_E = (\beta + 1) I_B$
putting this in eqn ①,

$$V_{CE} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$
$$- I_B (R_B + (\beta + 1) R_E) + V_{CE} - V_{BE} = 0$$

multiplying through by (-1),

$$I_B (R_B + (\beta + 1) R_E) - V_{CE} + V_{BE} = 0$$

$$I_B (R_B + (\beta + 1) R_E) = V_{CE} - V_{BE}$$

& solving for I_B ,

$$I_B = \frac{V_{CE} - V_{BE}}{R_B + (\beta + 1) R_E}$$

- The only difference between this eqn for I_B & that obtained for the fixed bias configuration is the term $(\beta + 1) R_E$.

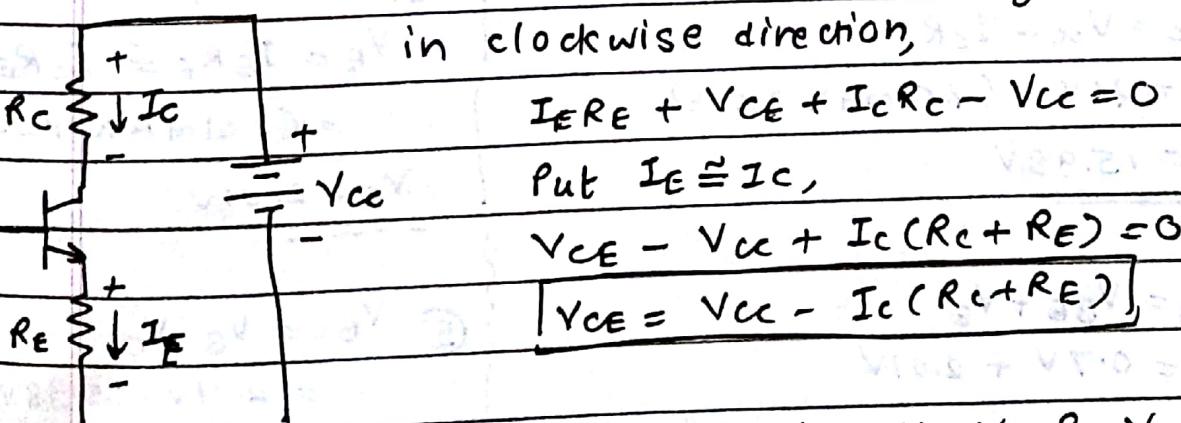
- Aside from base-to-emitter voltage V_{BE} , the resistor R_E is reflected back to the i/p base current by a factor $(\beta + 1)$.

- In other words, the emitter resistor, which is part of the collector-emitter loop, appears as $(\beta + 1) R_E$ in the base-emitter loop.

$$R_i = (\beta + 1) R_E$$

o/p loop or Collector-emitter loop -

Apply KVL to o/p loop



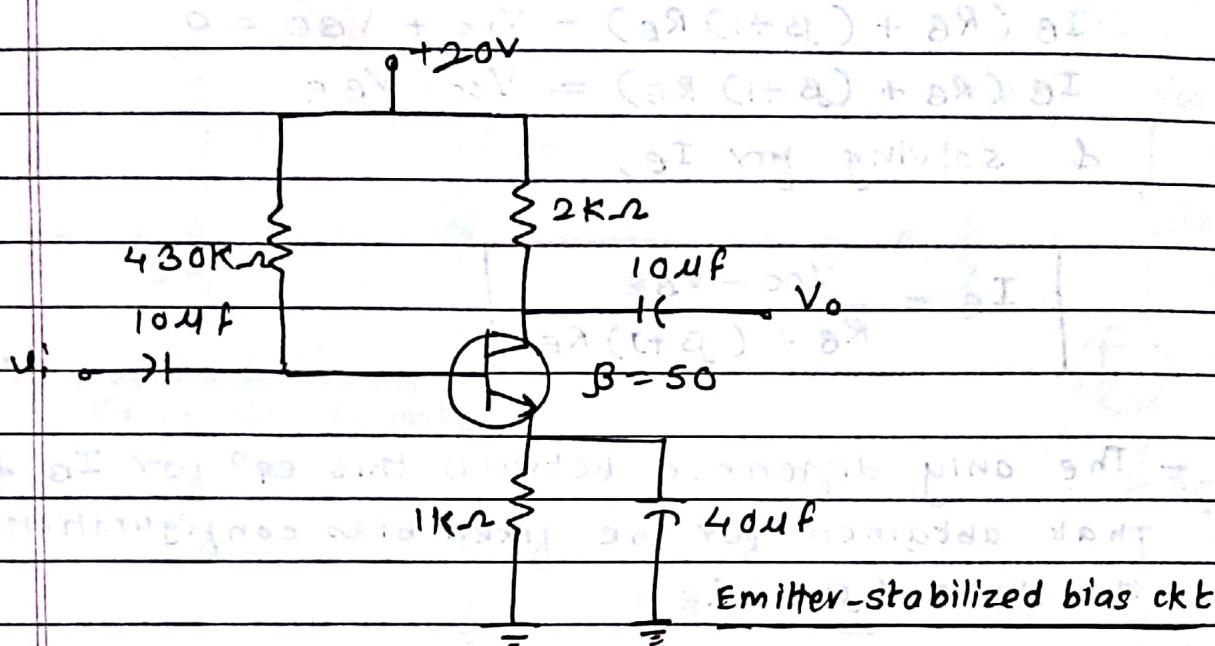
$$V_E = I_E R_E, \quad V_{CE} = V_C - V_E \quad \& \quad V_C = V_{CE} + V_E$$

$$\text{or } V_C = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_B R_B \quad \text{or} \quad V_B = V_{BE} + V_E$$

Ex2. For the emitter bias network given figure, determine

- a) I_B b) I_c c) V_{CE} d) V_C e) V_E f) V_B g) V_{BC}



$$\textcircled{a} \quad I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20V - 0.7V}{430k\Omega + (50)(1k\Omega)} = 40.1\text{mA}$$

$$\textcircled{b} \quad I_c = \beta I_B = (50)(40.1\text{mA}) = 2.01\text{mA}$$

$$\textcircled{c} \quad V_{CE} = V_{CC} - I_c (R_E + R_E) \quad \textcircled{d} \quad V_E = V_C - V_{CE}$$

$$= 20V - (2.01\text{mA})(2k\Omega + 1k\Omega) = 15.98V - 13.97V$$

$$V_{CE} = 13.97V \quad V_E = 2.01V$$

$$\textcircled{e} \quad V_C = V_{CC} - I_c R_C \\ = 20V - (2.01\text{mA} \times 2k\Omega)$$

$$V_C = 15.98V$$

$$\textcircled{f} \quad V_E = I_E R_E \approx I_c R_E \\ = (2.01\text{mA} \times 1k\Omega)$$

$$V_E = 2.01V$$

$$\textcircled{g} \quad V_B = V_{BE} + V_E \\ = 0.7V + 2.01V$$

$$V_B = 2.71V$$

$$\textcircled{h} \quad V_{BC} = V_B - V_C \\ = 2.71V - 15.98V$$

$$V_{BC} = -13.27V \quad (\text{R.B.E})$$

Ex3)

* Prepare a table & compare the bias voltage & currents of the circuits of examples/numerical solved for fixed bias configuration & emitter bias configuration, for the given values of $\beta = 50$ & for a new value of $\beta = 100$. compare the changes in I_c & V_{CE} for the same increase in β .

Sol:- Repeating above two examples for $\beta = 100$,

for Fixed Bias	β	$I_B(μA)$	$I_c(mA)$	$V_{CE}(V)$
	50	47.08	2.35	6.83
	100	47.08	4.71	3.64

- BJT collector current is seen to change by 100% due to the 100% change in the value of β .

The value of I_B is the same, V_{CE} decreased by 76%.

From previous solved example,

β	$I_B(μA)$	$I_c(mA)$	$V_{CE}(V)$
50	40.1	2.01	13.97
100	36.3	3.63	9.11

- BJT collector current increases by about 81% due to the 100% increase in β .

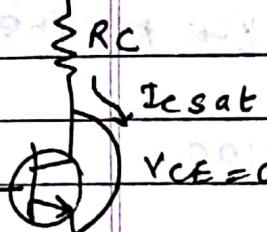
- I_B is decreased, helping maintain the value of I_c or at least reducing the overall change in I_c due to change in β .

- The change in V_{CE} has dropped to about 35%.

- Therefore Emitter Bias configuration is more stable than Fixed Bias configuration, for the same change in β .

* Saturation level :-

Apply a short circuit between the collector emitter terminals as shown & calculate resulting collector current.



$$I_{c\text{sat}} = \frac{V_{cc}}{R_c + R_E}$$

$V_{CE} = 0V$

Addition of the emitter bias resistor reduces the collector saturation level below that obtained with fixed bias configuration using the same collector resistor.

- * Determine the saturation current for the previous example (of Emitter Bias config.)

$$\Rightarrow I_{c\text{sat}} = \frac{V_{cc}}{R_c + R_E} = \frac{20V}{2k\Omega + 1k\Omega} = 20V = 20mA$$

$$I_{c\text{sat}} = 6.67mA$$

This is about 3 times the level of I_{c0} for example of emitter bias configuration.

* Load line Analysis :-

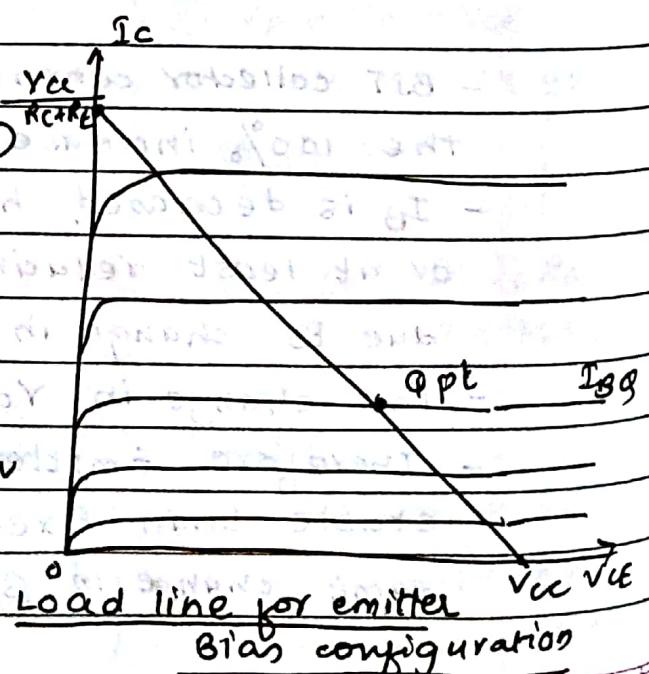
$$V_{CE} = V_{cc} - I_C (R_C + R_E)$$

case①, $I_C = 0mA$, $V_{CE} = V_{cc}$

$$V_{CE} = V_{cc} | I_C = 0mA$$

case②, $V_{CE} = 0$

$$I_C = \frac{V_{cc}}{(R_C + R_E)} | V_{CE} = 0V$$



3. Voltage Divider Bias configuration -

- In previous bias configuration, bias current I_{CQ} & V_{CEQ} were a function of current gain β of the transistor.

- Because β is temperature sensitive, especially for silicon transistors & the actual value of β is usually not well defined, it would be desirable to develop a bias ckt that is less dependent on, or in fact independent of, the transistor beta (β).

- The voltage divider configuration is such a network.

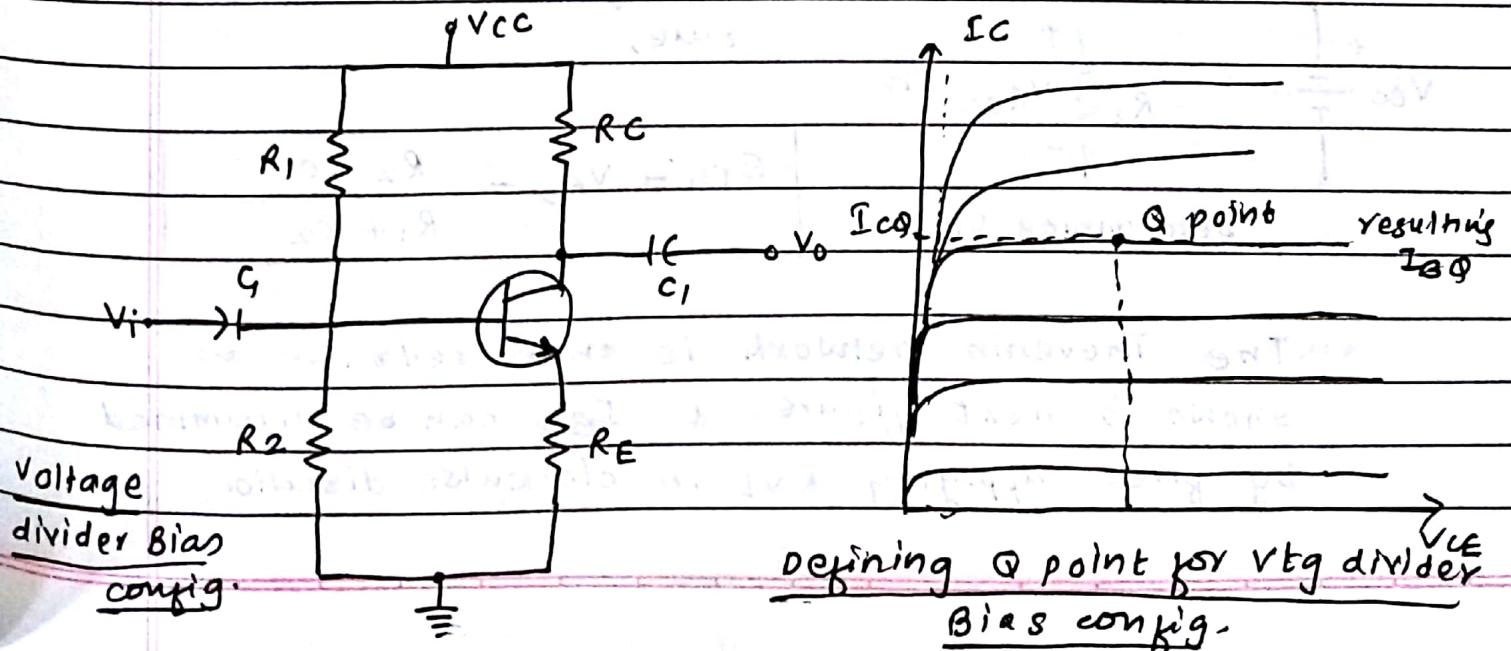
- To analyze the voltage divider bias configuration, there are two methods.

1. Exact Method - which can be applied to any voltage divider configuration.

2. Approximate Method - can be applied only if specific conditions are satisfied.

- The approximate approach permits a more direct analysis with a savings in time & energy.

- The approximate approach can be applied to the majority of situations & therefore should be examined with the same interest as the exact method.



* Exact Analysis -

For dc analysis -

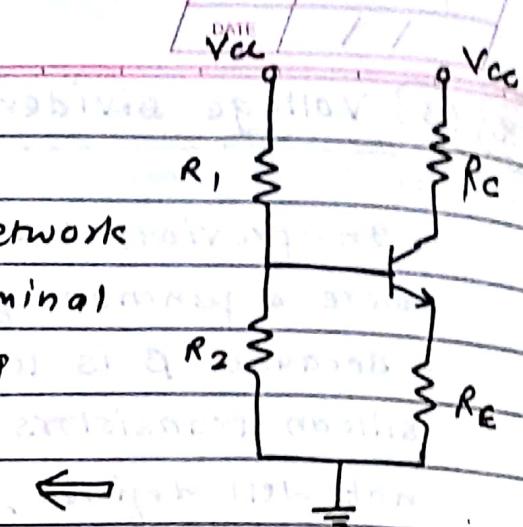
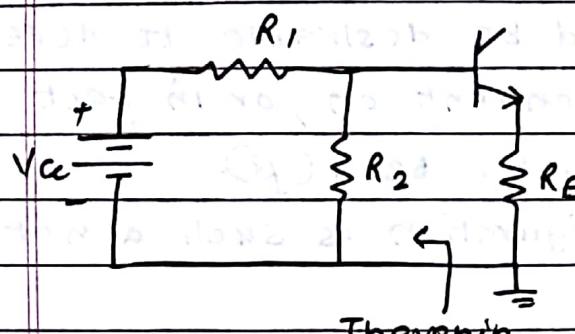
The thevenin

equivalent network for the network

to the left of the base terminal

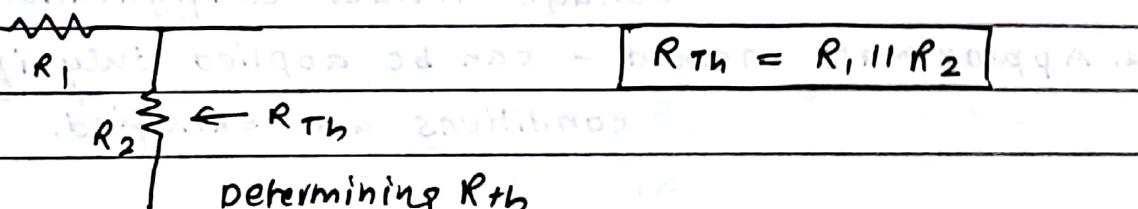
can be found in the following

manner



DC component of voltage
divider config.

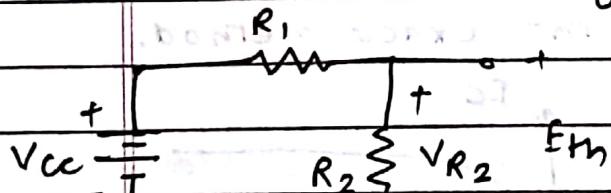
R_{th} - The voltage source is replaced by a short circuit equivalent as shown below.



Determining R_{th}

E_{th} - The voltage source Vcc is returned to the network & the open circuit Thevenin voltage of fig shown determined as follows -

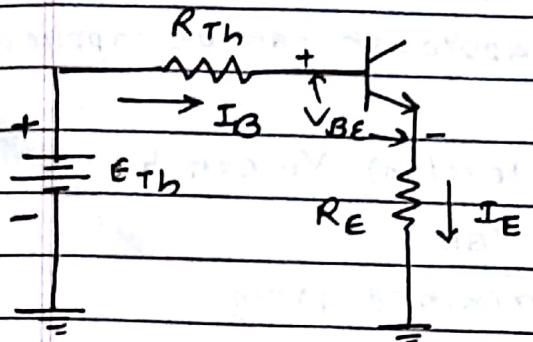
Applying voltage divider rule,



$$E_{th} = V_{R_2} = \frac{R_2 \cdot V_{cc}}{R_1 + R_2}$$

The Thevenin network is then redrawn as shown in next figure. & I_Q can be determined by first applying KVL in clockwise direction,

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$



Putting $I_E = (\beta + 1) I_B$ &
solving for I_B ,

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$

Inserting Thevenin Equivalent

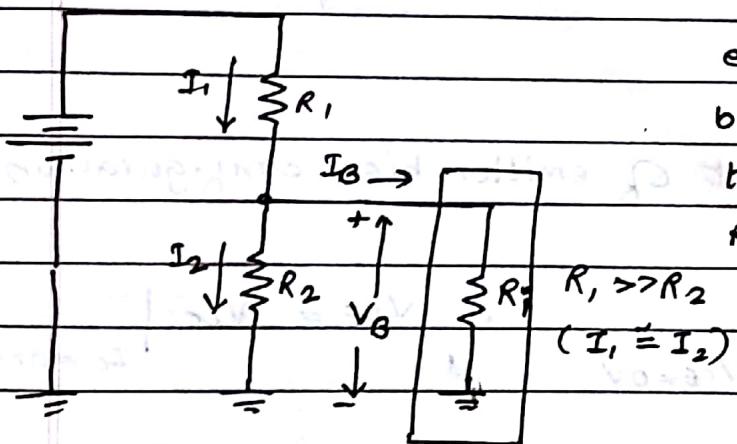
$$\& I_C = \beta I_B$$

$$\& V_{CE} = V_{CC} - I_C (R_C + R_E)$$

The remaining equations for V_E , V_C & V_B are also the same as obtained for the emitter bias configuration.

* Approximate Analysis -

The Resistance R_i is the equivalent resistance between base & ground for the transistor, with emitter resistor R_E .



The reflected resistance between B & E is defined by

Partial Bias ckt for calculating the approximate base vdg V_B

$$R_i = (\beta + 1) R_E$$

if $R_1 \gg R_2$,

$I_B \ll c I_2$ (current

always seeks the path of least resistance) & $I_2 \approx I_1$, or $I_1 = I_2$. & R_1 & R_2 can be considered series elements, - voltage across R_2 , which is actually the base voltage, can be determined using the voltage divider Rule,

$$V_B = \frac{R_2 \cdot V_{CC}}{R_1 + R_2}$$

- Because $R_i = (\beta + 1) R_E \approx \beta R_E$ condition that will define whether the approximate approach can be applied with a high degree of accuracy.

- once V_B is determined, the level of V_E can be calculated from, $V_E = V_B - V_{BE}$
 & emitter current can be determined from

$$I_E = \frac{V_E}{R_E} \text{ & } I_CQ = I_E$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

but : $I_E \approx I_C$

$$V_{CEQ} = V_{CC} - I_C (R_C + R_E)$$

* Transistor Saturation -

$$I_{CSAT} = I_{C MAX} = \frac{V_{CC}}{R_C + R_E}$$

* Load Line Analysis -

same as that of emitter bias configuration.

$$I_E = \frac{V_{CC}}{R_C + R_E} \quad \& \quad V_{CE} = V_{CC} - I_C R_C \quad I_C = 0MA$$

IE = 0 Consider first quiescent point, suppose

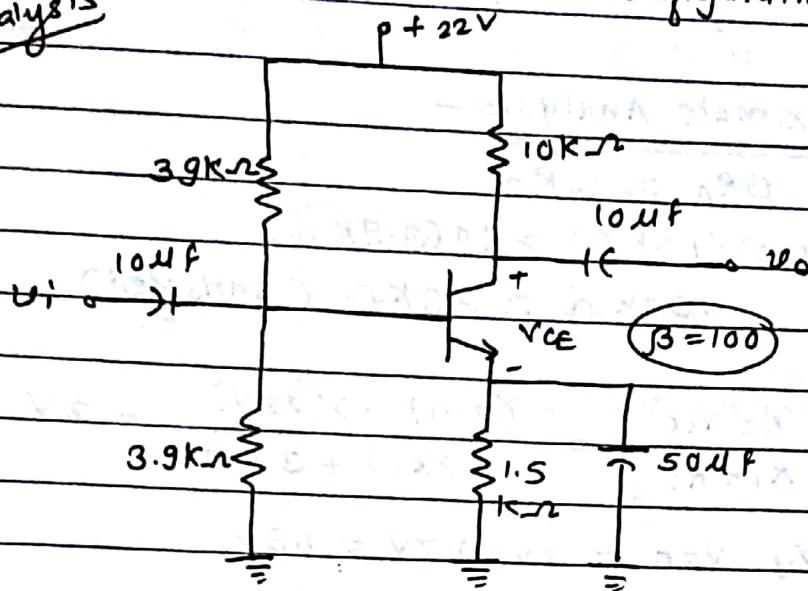
emitter bias voltage is zero and $I_E = I_C = 0$

then we get voltage of collector as zero option -

load voltage option not given because of no load

Ex4 Determine the dc bias voltage V_{CE} & the current I_C for the voltage divider bias configuration of fig shown.

Direct analysis



Soln -

$$R_{TH} = R_1 \parallel R_2 = (3.9k\Omega) (3.9k\Omega) = 3.55k\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$E_{Th} = \frac{(3.9k\Omega)(22V)}{3.9k\Omega + 3.9k\Omega} = 2V$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{2V - 0.7V}{3.55k\Omega + (100)(1.5k\Omega)}$$

$$I_B = 8.38 \mu A$$

$$I_C = \beta I_B = (100)(8.38) = 0.84mA$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= 22V - (0.84mA)(10k\Omega + 1.5k\Omega)$$

$$V_{CE} = 12.34V$$

Ex 5

DATE / / /

* Repeat the analysis of previous example using the approximate analysis technique & compare solutions for I_{CQ} & V_{CEQ}

Soln Using Approximate Analysis -

$$B R_E \geq 10 R_L$$

$$(100)(1.5k\Omega) \geq 10(3.9k\Omega)$$

$$150k\Omega \geq 39k\Omega \text{ (satisfied)}$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9k\Omega)(22V)}{39k\Omega + 3.9k\Omega} = 2V$$

$$V_E = V_B - V_{BE} = 2V - 0.7V = 1.3V$$

$$I_{CQ} \approx I_E = \frac{V_E}{R_E} = \frac{1.3V}{1.5k\Omega} = 0.867mA$$

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$$

$$= 22V - (0.867mA)(10k\Omega + 1.5k\Omega)$$

$$V_{CEQ} = 12.03V$$

* How Q point will move if β is reduced?

→ Repeat the exact analysis of ex no. 4 if β is reduced to 50 & compare solutions for I_{CQ} & V_{CEQ}

$$R_{Th} = 3.55k\Omega \quad E_{Th} = 2V$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{2V - 0.7V}{3.55k\Omega + (51)(1.5k\Omega)} = 16.24mA$$

$$I_{CQ} = \beta I_B = (50)(16.24mA) = 0.81mA$$

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E) = 22V - (0.81mA)(10k\Omega + 1.5k\Omega)$$

β	I_{CQ} (mA)	V_{CEQ} (V)
100	0.84mA	12.34V
50	0.81mA	12.69V

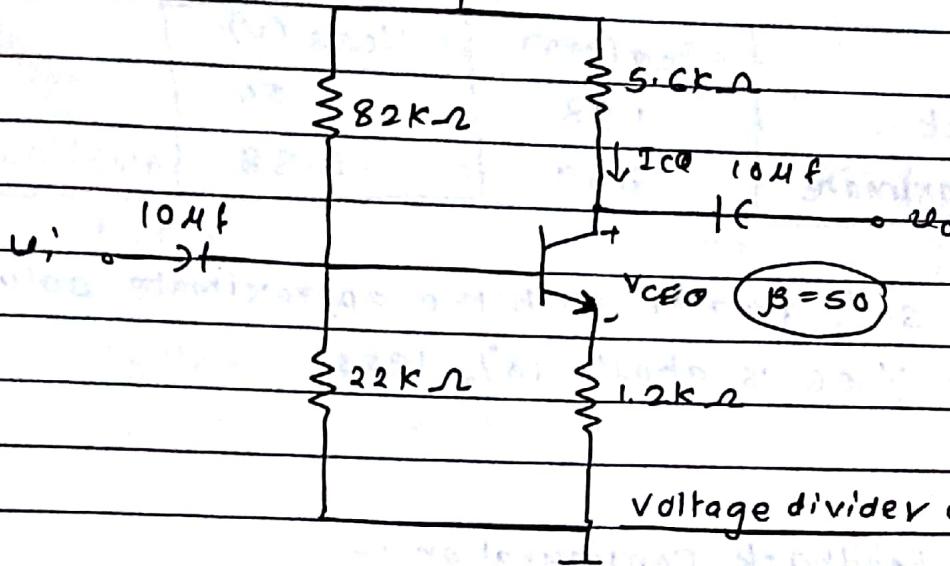
This shows the relative insensitivity of the circuit to the change in β .

* Example to show difference in sol'n if cond'n/criterion of approx. sol'n is ignored.

Ex 6:

Determine the levels of I_{CQ} & V_{CEQ} for the voltage divider configuration of fig. shown using the exact & approximate techniques & compare solutions.

p18V



Voltage divider configuration

Sol'n - Exact Analysis - $\beta R_E \geq 10 R_2$

$$(50)(1.2\text{k}\Omega) \geq 10(22\text{k}\Omega)$$

$60\text{k}\Omega \neq 220\text{k}\Omega$ (not satisfied)

$$R_{Th} = R_1 || R_2 = 82\text{k}\Omega || 22\text{k}\Omega = 17.35\text{k}\Omega$$

$$E_{Th} = \frac{R_2 V_{cc}}{R_1 + R_2} = \frac{22\text{k}\Omega (18\text{V})}{82\text{k}\Omega + 22\text{k}\Omega} = 3.81\text{V}$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_m + (\beta + 1)R_E} = \frac{3.81\text{V} - 0.7\text{V}}{17.35\text{k}\Omega + (51)(1.2\text{k}\Omega)} = 39.6\text{mA}$$

$$I_{CQ} = \beta I_B = (50)(39.6\text{mA}) = 1.98\text{mA}$$

$$V_{CEQ} = V_{cc} - I_C(R_C + R_E) \\ = 18\text{V} - (1.98\text{mA})(5.6\text{k}\Omega + 1.2\text{k}\Omega)$$

$$V_{CEQ} = 4.54\text{V}$$

Approximate Analysis -

$$V_B = E_{Th} = 3.81\text{V}$$

$$V_E = V_B - V_{BE} = 3.81\text{V} - 0.7\text{V} = 3.11\text{V}$$

$$I_{CQ} = I_E = \frac{V_E}{R_E} = \frac{3.11\text{V}}{1.2\text{k}\Omega} = 2.59\text{mA}$$

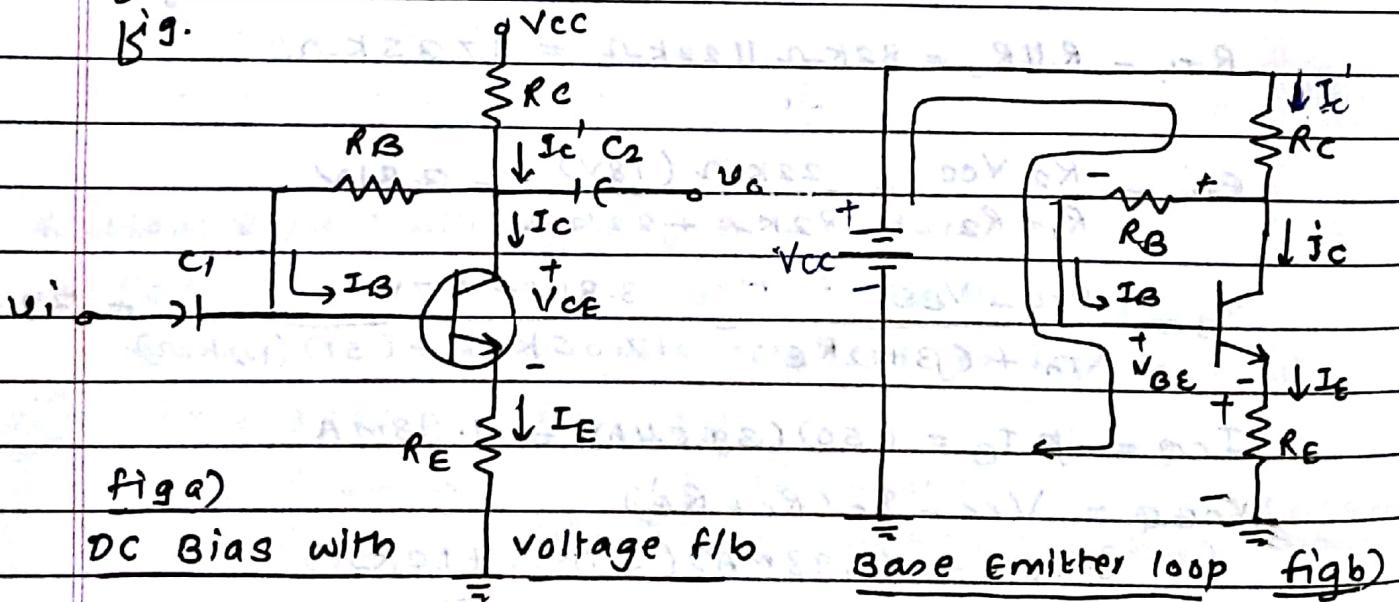
$$\begin{aligned}
 V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\
 &= 18V - (2.59mA)(5.6k\Omega + 1.2k\Omega) \\
 V_{CEQ} &= 3.88V
 \end{aligned}$$

	I_{CQ} (mA)	V_{CEQ} (V)
Exact	1.98	4.54
Approximate	2.59	3.88

I_{CQ} is 30% greater with the approximate solution whereas V_{CEQ} is about 10% less.

3. Collector Feedback Configuration :-

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in next fig.



Base Emitter loop / Input loop -

Apply KVL around the indicated loop in clockwise direction

$$V_{CC} - I_C' R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

But $I_C' = I_C + I_B$ so, $I_C' \approx I_C = \beta I_B$ &
 $I_E \approx I_C$

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_B = 0$$

solving for I_B ,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta (R_C + R_E)}$$

Collector-Emitter loop -

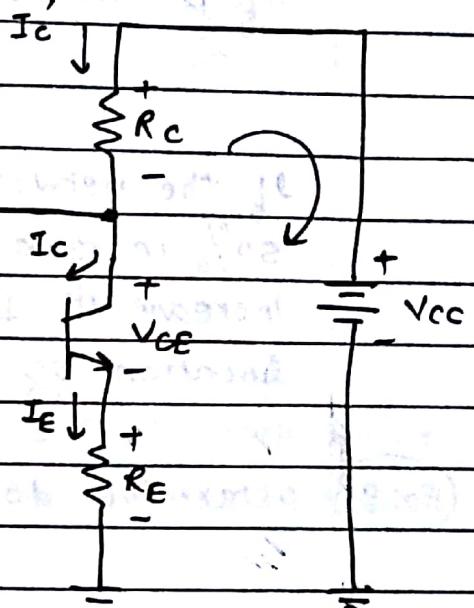
Apply KVL around indicated loop in clockwise direction,

$$I_E R_E + V_{CE} + I_C' R_C - V_{CC} = 0$$

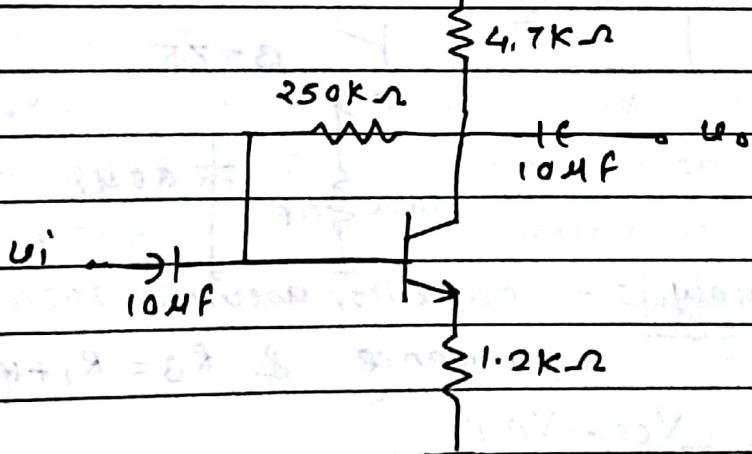
$$\therefore I_C' \approx I_C \text{ & } I_E \approx I_C$$

$$I_C (R_C + R_E) + V_{CE} - V_{CC} = 0$$

$$V_{CEQ} = V_{CC} - I_C (R_C + R_E)$$



Ex.7. Determine the quiescent levels of I_{CQ} & V_{CEQ} for the network shown.



$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta (R_C + R_E)} = \frac{10V - 0.7V}{250k\Omega + (90)(4.7k\Omega + 1.2k\Omega)}$$

$$I_B = 11.91 \mu A$$

$$I_{CQ} = \beta I_B = (90)(11.91 \mu A) = 1.07 \text{ mA}$$

$$V_{CEQ} = V_{CC} - I_C (R_C + R_E) = 10V - (1.07 \text{ mA})(4.7k\Omega + 1.2k\Omega)$$

$$V_{CEQ} = 3.69 \text{ V}$$

EX-8) Repeat above example using $\beta = 135$

Soln $I_B = 8.894 \text{ A}$

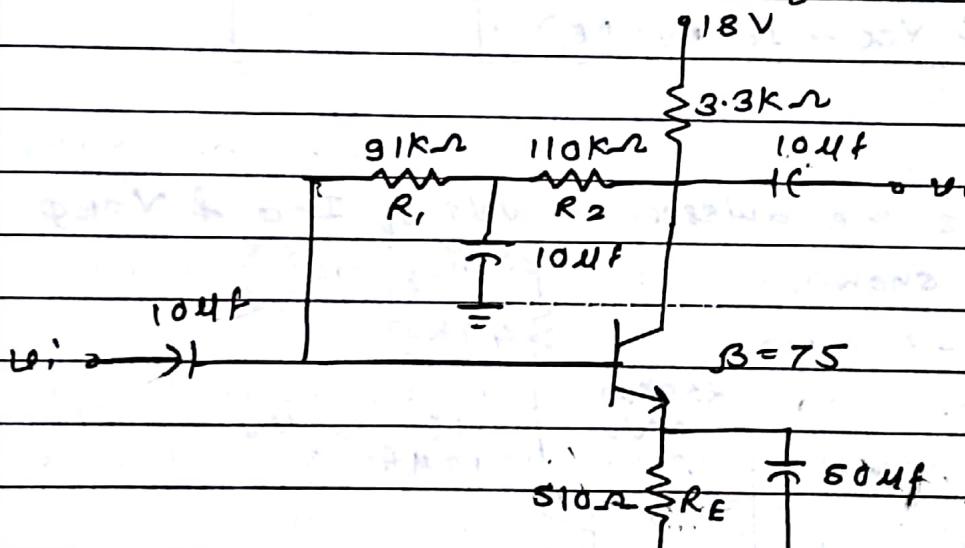
$$I_{CQ} = 1.2 \text{ mA}$$

$$V_{CEQ} = 2.92 \text{ V}$$

If β increased 50%, I_{CQ} only increased 12.1%.
 V_{CEQ} decreased abt 20.9%.

If the network uses fixed bias configuration,
50% increase in β would have resulted in a 50%
increase in I_{CQ} & a dramatic change in the
location of Q' pt.

Ex 9. Determine dc level of I_B & I_c for the network shown.



Soln for DC analysis - capacitor assumes open circuit equivalence & $R_B = R_1 + R_2$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

$$= \frac{18V - 0.7V}{(91k\Omega + 110k\Omega) + (75)(3.3k\Omega + 0.51k\Omega)}$$

$$I_B = 35.5 \text{ mA}$$

$$I_C = \beta I_B = 75 \times 35.5 \text{ mA} = 2.66 \text{ mA}$$

$$\begin{aligned}
 V_C &= V_{CC} - I_c' R_C \\
 &= V_{CC} - I_c R_C \\
 &= 18V (2.25mA \times 3.3k\Omega) \\
 V_C &= 9.22V
 \end{aligned}$$

* Saturation conditions -

using approximation, $I_c' = I_c$

$$I_{CSAT} = I_{CMAX} = \frac{V_{CC}}{R_C + R_E}$$

* Load line Analysis -

continuing with approximation $I_c' = I_c$ results in the same load line defined for the voltage divider & emitter biased configuration.

Ex10. Given the network of fig a) & the BJT characteristics of fig b)

- Draw the load line for the network on the characteristic.
- Determine the dc beta in the center region of the characteristics. Define the chosen point as the \oplus .
- Using the dc beta calculated in part b), find the dc value of I_B .

- d) Find I_{CQ} & I_{CEQ}

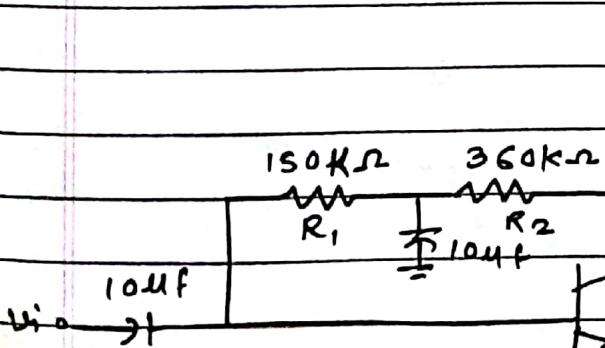


fig a)

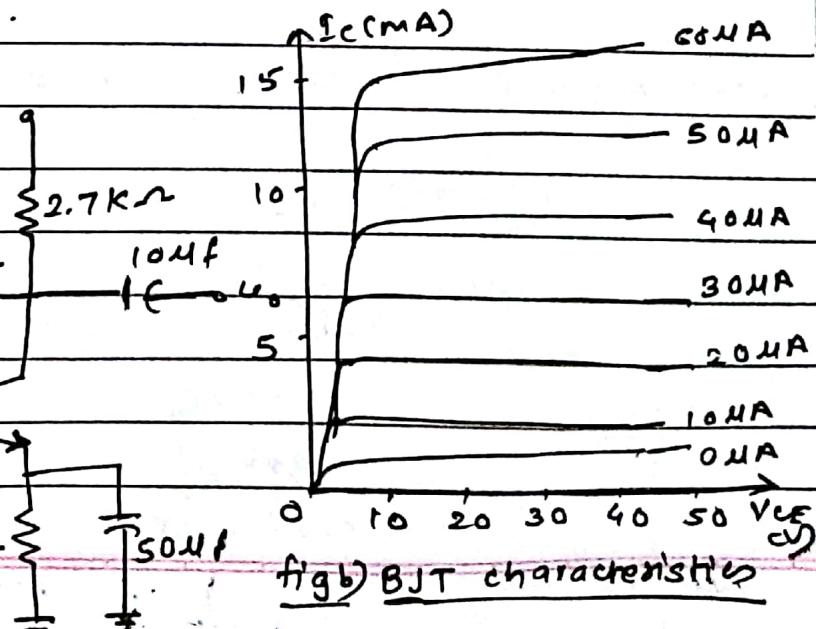


fig b) BJT characteristics

Sol^b (a) The load line is drawn on fig b) as determined by the following intersections.

$$V_{CE} = 0, I_C = \frac{V_{CC}}{R_C + R_E} = \frac{3\text{V}}{2.7\text{k}\Omega + 33\text{k}\Omega} = 11.88\text{mA}$$

$$I_C = 0, V_{CE} = V_{CC} = 3\text{V}$$

(b) $I_B = 25\mu\text{A}$ & V_{CE} about 17V

$$\beta = \frac{I_{CQ}}{I_{BQ}} = \frac{6.2\text{mA}}{25\mu\text{A}} = 248$$

$$(c) I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{3\text{V} - 0.7\text{V}}{510\text{k}\Omega + 248(2.7\text{k}\Omega + 33\text{k}\Omega)} = \frac{2.3\text{V}}{510\text{k}\Omega + 751.44\text{k}\Omega} = 35.3\text{V}$$

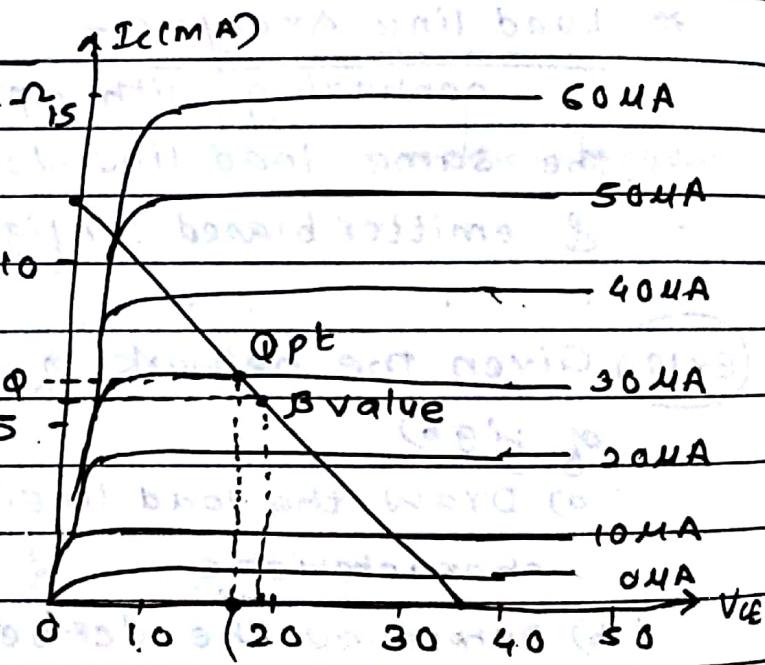
$$I_B = 28\mu\text{A}$$

Defining Q point I_{CQ}
for voltage divider
bias configuration

from fig,

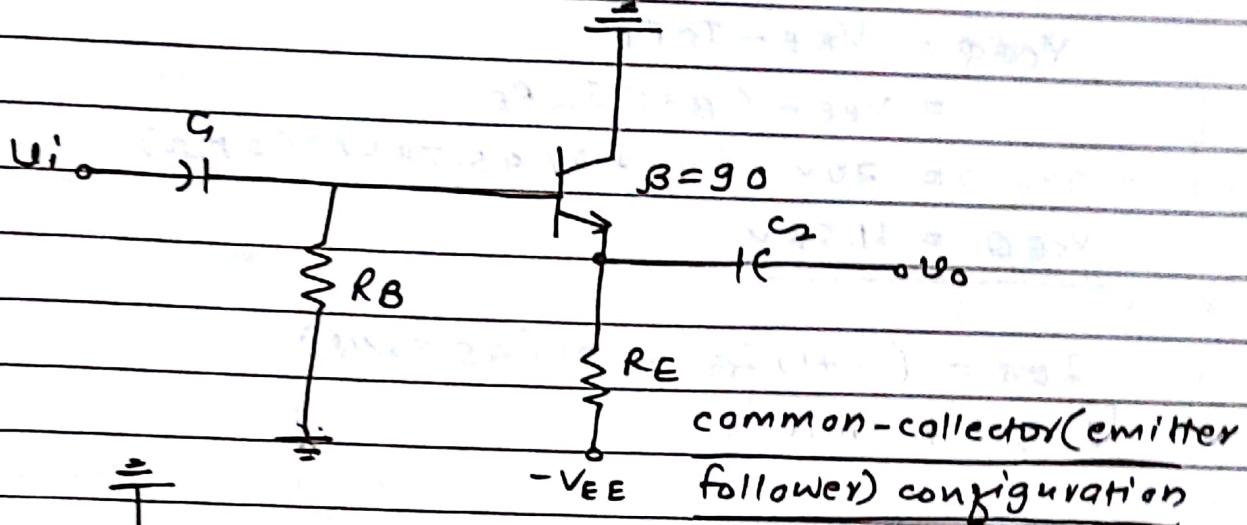
$$I_{CQ} = 6.9\text{mA}$$

$$V_{CEQ} = 15\text{V}$$



4. Emitter-Follower configuration -

In this configuration output is taken out from emitter terminal.
Emitter follower means common collector.

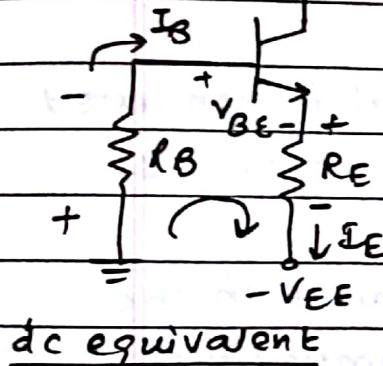


Apply KVL to i/p circuit,

$$- I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$\text{using } I_E = (\beta + 1) I_B$$

$$I_B R_B + (\beta + 1) I_B R_E = V_{EE} - V_{BE}$$



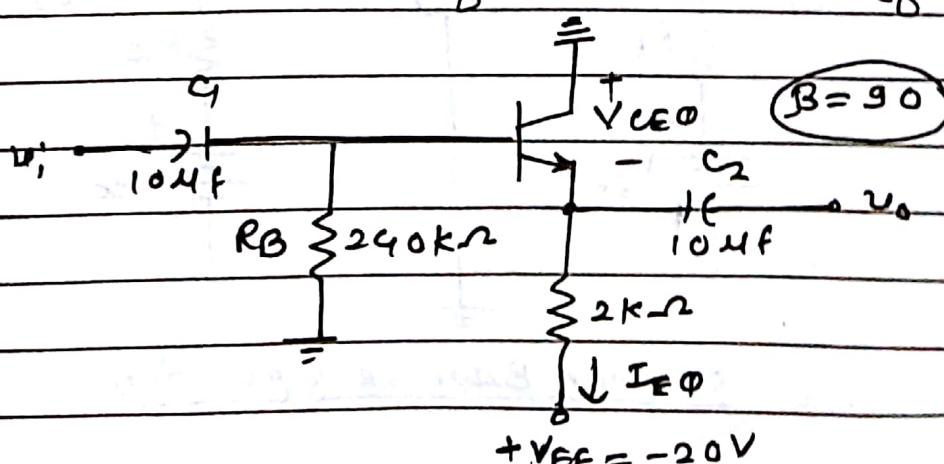
$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E}$$

Apply KVL to o/p loop,

$$- V_{CE} - I_E R_E + V_{EE} = 0$$

$$V_{CE} = V_{EE} - I_E R_E$$

Ex.11 Determine $V_{CE\phi}$ & $I_{E\phi}$ for the network of fig shown.



$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta+1)R_E} = \frac{20V - 0.7V}{24\text{k}\Omega + (90+1)\text{k}\Omega}$$

$$\underline{I_B = 45.73 \text{ mA}}$$

$$V_{CEQ} = V_{EE} - I_B R_E$$

$$= V_{EE} - (\beta+1) I_B R_E$$

$$= 20V - (90+1)(45.73 \text{ mA})(2\text{k}\Omega)$$

$$\underline{V_{CEQ} = 11.68V}$$

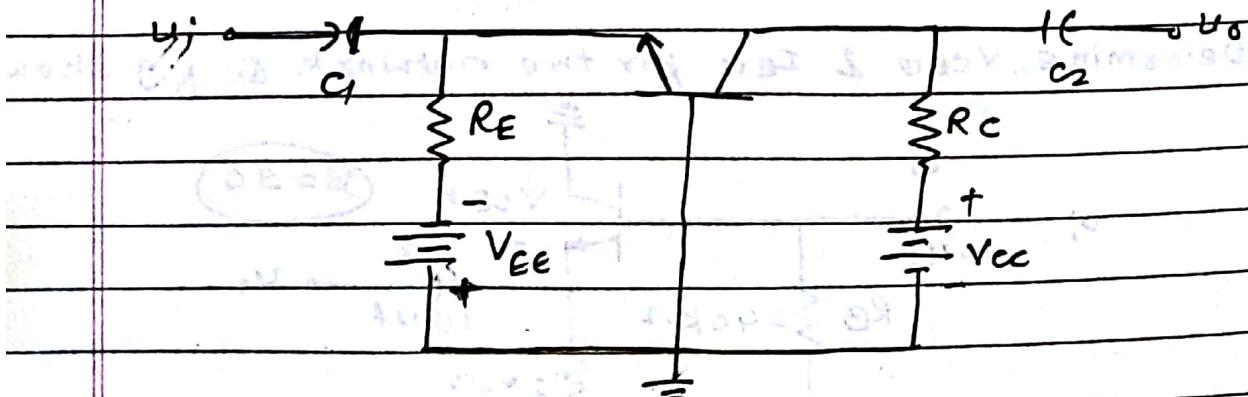
$$I_{EQ} = (\beta+1) I_B = 91(45.73 \text{ mA})$$

$$\boxed{I_{EQ} = 4.16 \text{ mA}}$$

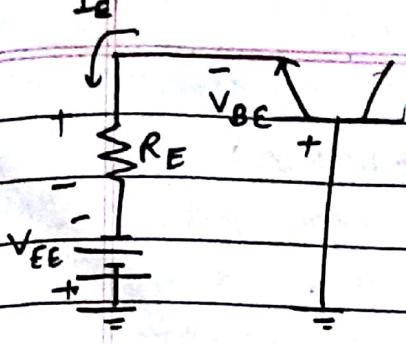
(5) common Base configuration -

Applied signal is connected to the emitter terminal & the base is at or just above, ground potential.

- It is fairly popular configuration because in the ac domain it has a very low input impedance, high o/p impedance & good gain.
- Two supplies are used in this configuration & the base is the common terminal between the i/p emitter terminal & o/p collector terminal.



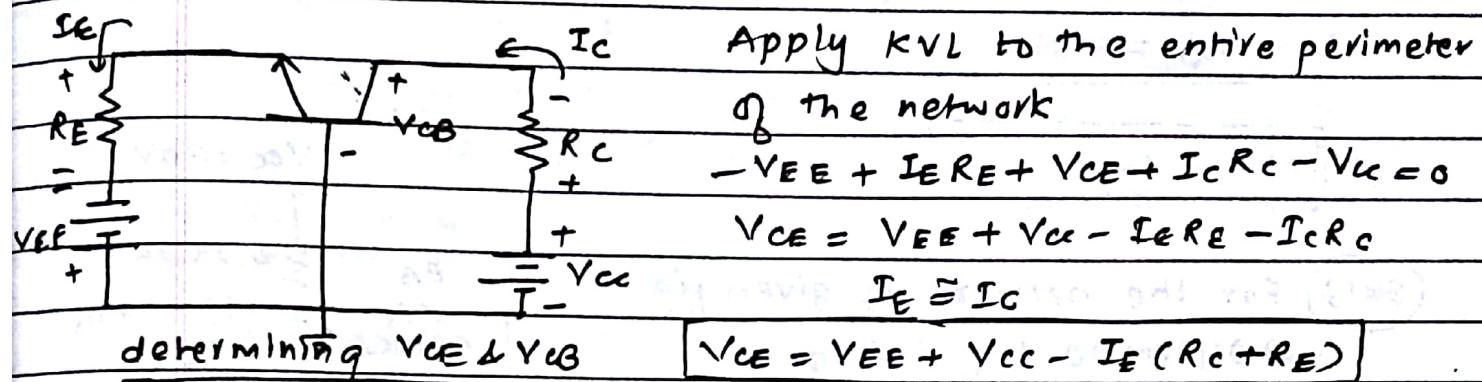
common Base configuration



Apply KVL
 $-VEE + I_E R_E + V_{BE} = 0$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

BIPOLAR EQUIVALENT



Apply KVL to o/p loop,

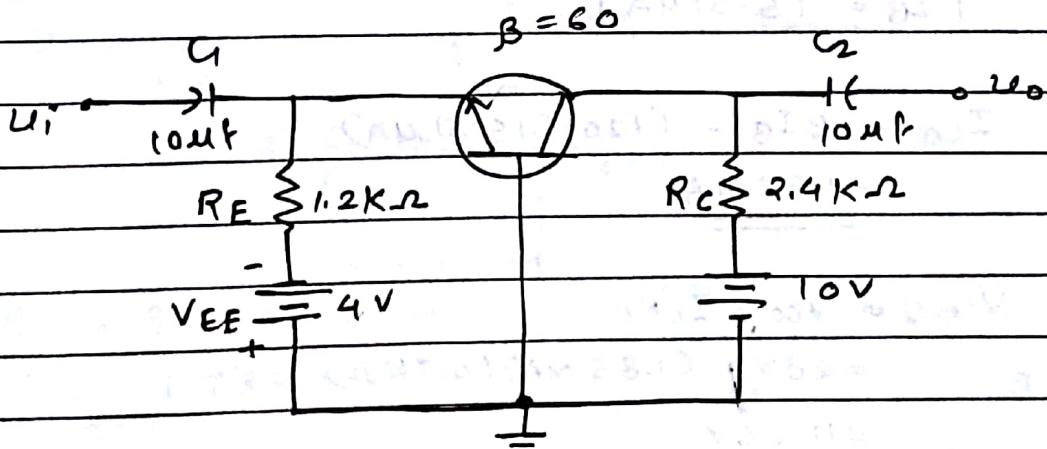
$$V_{CB} + I_c R_C - V_{CC} = 0$$

$$V_{CB} = V_{CC} - I_c R_C \quad \text{but } I_c \approx I_E$$

$$V_{CB} = V_{CC} - I_E R_C$$

Ex 12. Determine the currents I_E & I_B & voltages V_{CE} & V_{CB}

for common Base configuration shown.



$$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{4V - 0.7V}{1.2k\Omega} = 2.75mA$$

$$I_B = \frac{I_E}{\beta + 1} = \frac{2.75mA}{61} = 45.08\mu A$$

$$V_{CE} = V_{EE} + V_{CC} - I_E (R_C + R_E)$$

$$= 4V + 10V - (2.75mA)(2.4k\Omega + 1.2k\Omega)$$

$$\underline{V_{CE} = 4.1V}$$

$$V_{CB} = V_{CC} - I_C R_C = V_{CC} - \beta I_B R_C$$

$$= 10V - (60)(45.08mA) (24k\Omega)$$

$$\underline{V_{CB} = 3.51V}$$

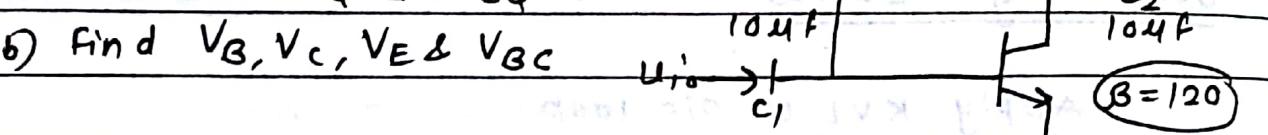
* Mixed Examples

$$V_{CC} = 20V$$

EX13) For the network of given fig.

a) Determine I_{CQ} & V_{CEQ}

b) Find V_B , V_C , V_E & V_{BC}



Soln - absence of R_E reduces the reflection of resistive levels to simply collector feedback with that of R_C & equation for I_B reduces to,

$$a) I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C} = \frac{20V - 0.7V}{680k\Omega + (120)(4.7k\Omega)}$$

$$I_B = 15.51mA$$

$$I_{CQ} = \beta I_B = (120)(15.51mA)$$

$$= 1.86mA$$

$$V_{CEQ} = V_{CC} - I_C R_C$$

$$= 20V - (1.86mA)(4.7k\Omega)$$

$$= 11.26V$$

$$b) V_B = V_{BE} = 0.7V \quad V_{BE} = V_B - V_C = 0.7V - 11.26V$$

$$V_C = V_{CE} = 11.26V \quad \underline{V_{BE} = -10.56V}$$

$$V_E = 0V$$

Ex.14) Determine V_C & V_B for the network

Soln? Apply KVL in clockwise direction

for BE loop results in,

$$-I_B R_B - V_{BE} + V_{EE} = 0$$

$$I_B = \frac{V_{EE} - V_{BE}}{R_B}$$

$$= \frac{9V - 0.7V}{100k\Omega} = \frac{8.3V}{100k\Omega}$$

$$I_B = 83.4A$$

$$R_C \approx 1.2k\Omega$$

$$C_2 \quad 1F \quad 10uF$$

$$B = 45$$

$$R_B \approx 100k\Omega$$

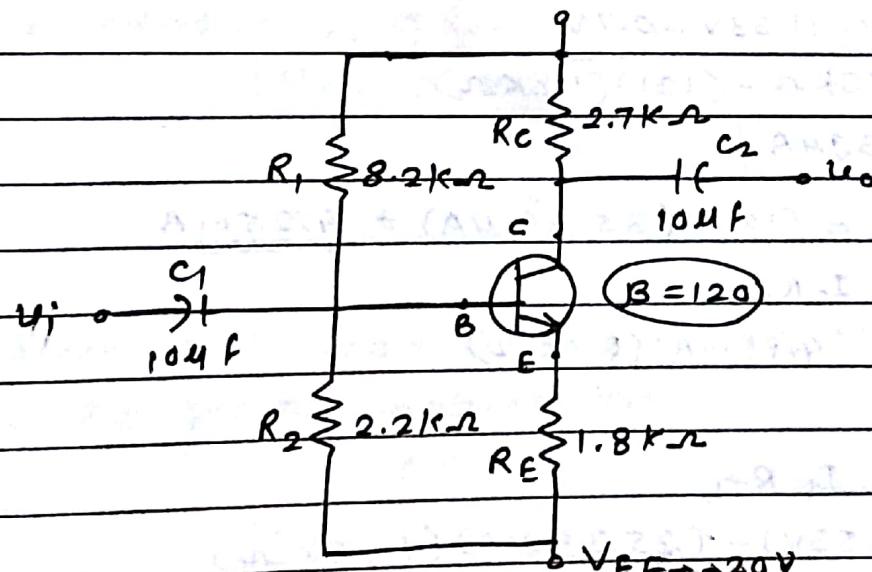
$$V_{EE} = -9V$$

$$I_C = B I_B = (45)(83.4A) = 3.735mA$$

$$V_C = -I_C R_C = -(3.735mA)(1.2k\Omega) = -4.48V$$

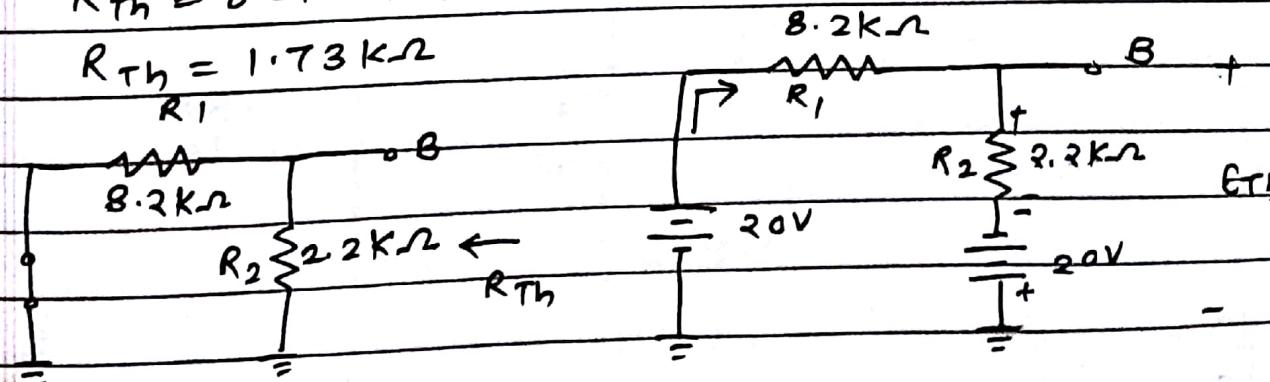
$$V_B = -I_B R_B = -(83.4A)(100k\Omega) = -8.3V$$

Ex.15) Determine V_C & V_B for the network of shown in fig.



$$\text{Soln} \quad R_{Th} = 8.2k\Omega || 2.2k\Omega$$

$$R_{Th} = 1.73k\Omega$$



E_{Th}

$$I = \frac{V_{cc} + V_{EE}}{R_1 + R_2} = \frac{20V + 2.0V}{8.2k\Omega + 2.2k\Omega} = 3.85mA$$

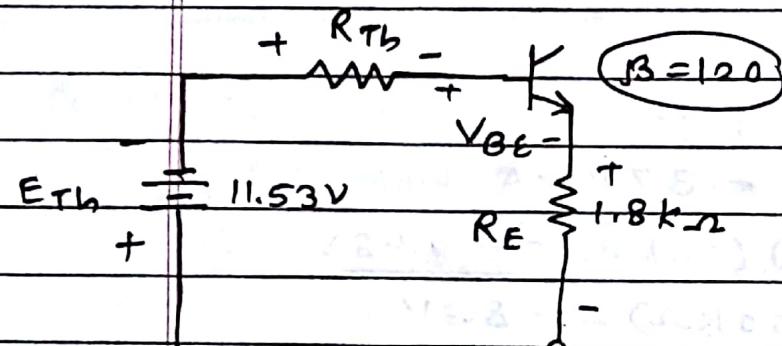
$$E_{Th} = IR_2 - V_{EE}$$

$$= (3.85mA)(2.2k\Omega) - 20V$$

$$E_{Th} = -11.53V$$

Network can be redrawn as shown -

Apply KVL



$$-E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E + V_{EE20}$$

substituting $I_E = (\beta + 1) I_B$ gives

$$V_{EE} - E_{Th} - V_{BE} - (\beta + 1) I_B R_E -$$

$$I_E R_{Th} = 0$$

$$I_B = \frac{V_{EE} - E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$

$$= \frac{20V - 11.53V - 0.7V}{1.73k\Omega + (121)(1.8k\Omega)}$$

$$= 35.39mA$$

$$I_C = \beta I_B = (120)(35.39mA) = 4.25mA$$

$$V_C = V_{cc} - I_C R_C$$

$$= 20V - (4.25mA)(2.7k\Omega)$$

$$= 8.53V$$

$$V_Q = -E_{Th} - I_B R_{Th}$$

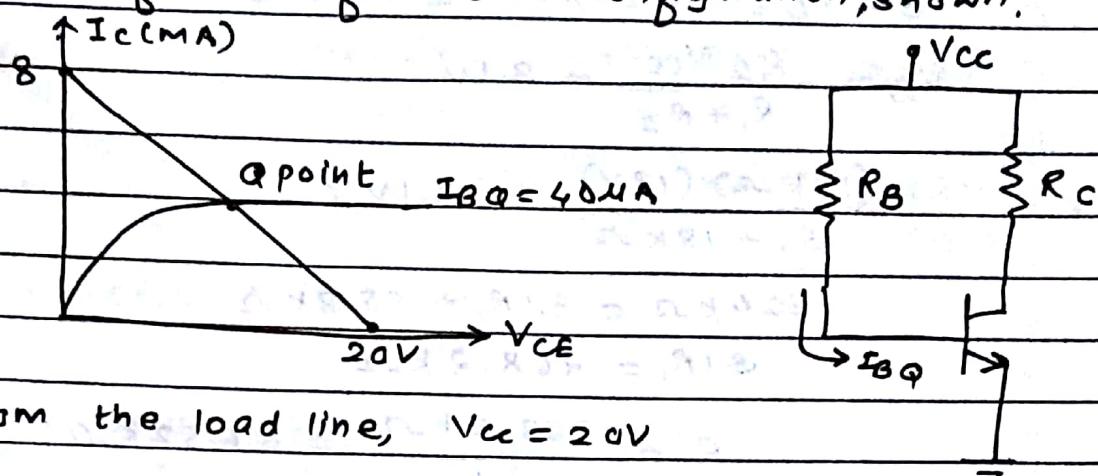
$$= -(11.53V) - (35.39mA)(1.73k\Omega)$$

$$= -11.59V$$

Designing Problems

Page No.	11
Date	

Ex 16) Given the characteristics of given fig, determine V_{cc} , R_B & R_C for the fixed bias configuration, shown.



Soln From the load line, $V_{cc} = 20V$

$$I_c = \frac{V_{cc}}{R_C} \quad |_{V_{CE}=0V}$$

$$R_C = \frac{V_{cc}}{I_c} = \frac{20V}{8MA} = 2.5k\Omega$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}, \quad R_B = \frac{V_{cc} - V_{BE}}{I_B} = \frac{20V - 0.7V}{40MA} = 482.5k\Omega$$

$$R_B = 482.5k\Omega$$

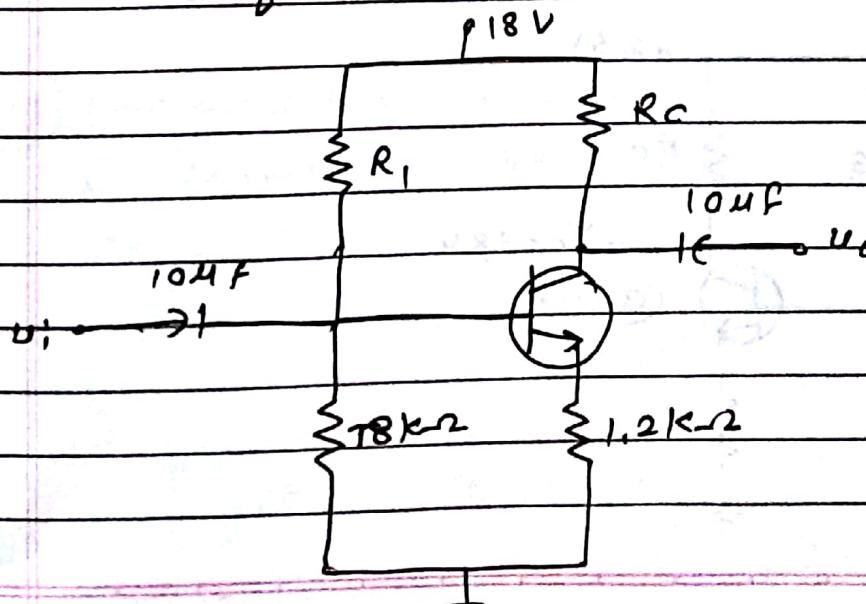
standard values of Resistor are,

$$R_C = 2.4k\Omega$$

$$R_B = 470k\Omega$$

$$I_B = 41.1mA$$

Ex 17) Given that $I_{cq} = 2MA$ & $V_{ceq} = 10V$ determine R_1 & R_C for the network shown.



$$SOL_1 \quad V_E = I_E R_E \approx I_C R_E = (QMA) (1.2k\Omega) = 2.4V$$

$$V_B = V_BE + V_E = 0.7V + 2.4V = 3.1V$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = 3.1V$$

$$\frac{(18k\Omega)(18V)}{R_1 + 18k\Omega} = 3.1V$$

$$324k\Omega = 3.1R_1 + 55.8k\Omega$$

$$3.1R_1 = 268.2k\Omega$$

$$R_1 = \frac{268.2k\Omega}{3.1} = 86.52k\Omega$$

$$R_C = \frac{V_{RC}}{I_C} = \frac{V_{CC} - V_C}{I_C}$$

$$V_C = V_{CE} + V_E = 10V + 2.4V = 12.4V$$

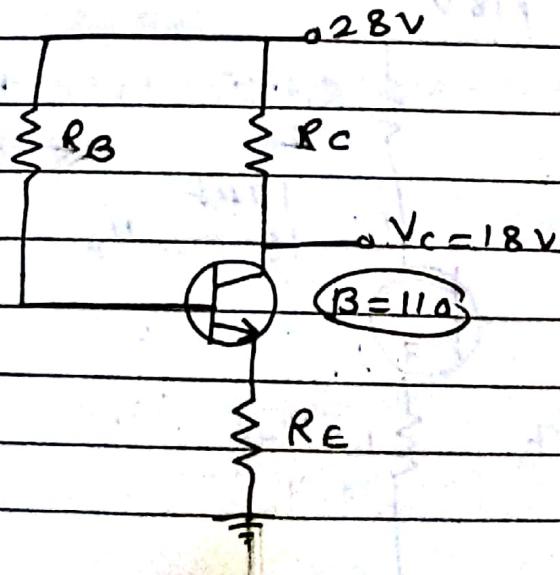
$$R_C = \frac{18V - 12.4V}{2mA} = 2.8mA$$

Standard values, $R_1 = 82\Omega$ & $91k\Omega$ (nearest)

using series comb' of $82k\Omega$ & $4.7k\Omega = 86.7k\Omega$

would result in a value very close to the design value/level.

EX18: The emitter bias configuration of given figure has the following specifications $I_{CQ} = \frac{1}{2} I_{sat}$, $I_{Csat} = 8mA$, $V_C = 18V$ & $\beta = 110$. Determine R_C , R_E & R_B



$$I_{CQ} = \frac{1}{2} I_{CSAT} = 4 \text{ mA}$$

$$R_C = \frac{V_{RC}}{I_{CQ}} = \frac{V_{CC} - I_C}{I_{CQ}} = \frac{28V - 18V}{4 \text{ mA}} = 2.5 \text{ k}\Omega$$

$$I_{CSAT} = \frac{V_{CC}}{R_E + R_E} \rightarrow R_E + R_E = \frac{V_{CC}}{I_{CSAT}} = \frac{28V}{8 \text{ mA}} = 3.5 \text{ k}\Omega$$

$$R_E = 3.5 \text{ k}\Omega - R_C = 1 \text{ k}\Omega$$

$$I_{BO} = \frac{I_{CQ}}{\beta} = \frac{4 \text{ mA}}{110} = 36.36 \text{ mA}$$

$$I_{BO} = \frac{V_{OC} - V_{BE}}{R_B + (\beta + 1)R_E} \rightarrow$$

$$R_B + (\beta + 1)R_E = \frac{V_{CC} - V_{BE}}{I_{BO}}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_{CQ}} = (\beta + 1)R_E$$

$$= \frac{28V - 0.7V}{36.36 \text{ mA}} = (111)(1 \text{ k}\Omega)$$

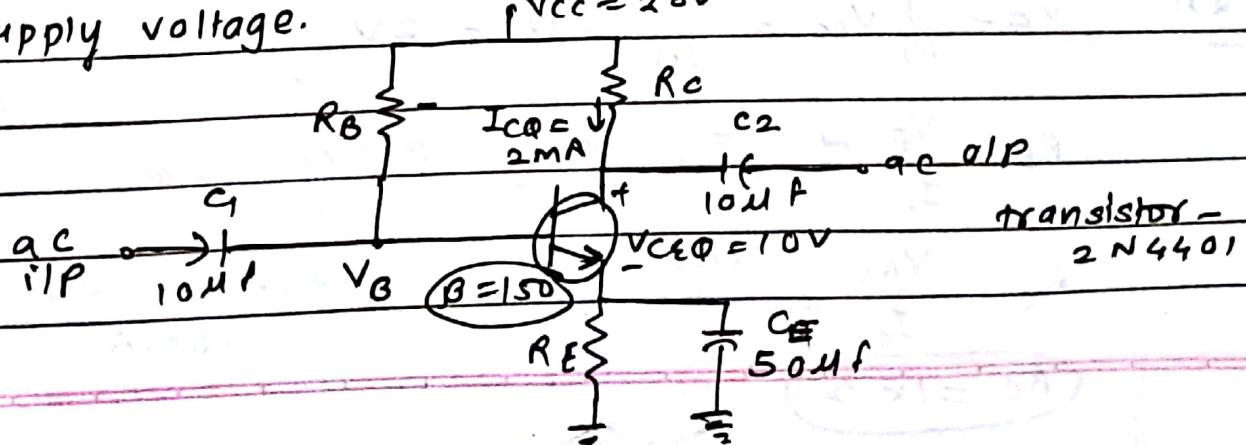
$$= \frac{27.3V}{36.36 \text{ mA}} = 771$$

$$R_B = 638.8 \text{ k}\Omega \quad \text{for standard values,}$$

$$R_C = 2.4 \text{ k}\Omega, R_E = 1 \text{ k}\Omega$$

$$R_B = 620 \text{ k}\Omega$$

Ex19: Determine the resistor values for the network of Fig shown for the indicated operating point & supply voltage.



$$Q1) V_E = \frac{1}{10} V_{CC} = \frac{1}{10} (20V) = 2V$$

$$R_E = \frac{V_E}{I_E} = \frac{2V}{2mA} = 1k\Omega$$

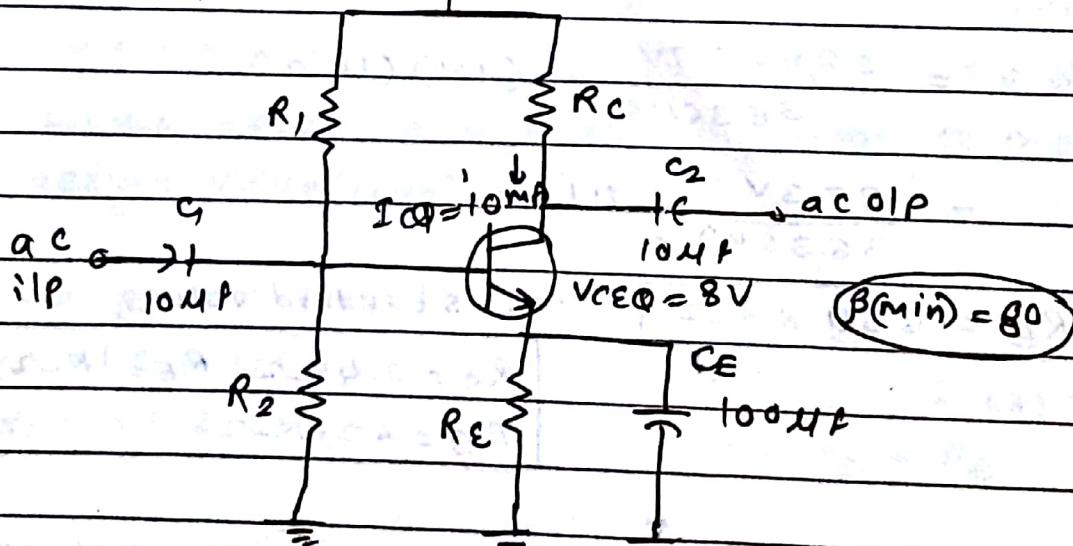
$$R_E = \frac{V_{RE}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20V - 10V - 2V}{2mA} = 8V = 2mA$$

$(R_E = 4k\Omega)$

$$I_B = \frac{I_C}{\beta} = \frac{2mA}{150} = 13.33\mu A$$

$$R_B = \frac{V_{RB}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20V - 0.7V - 2V}{13.33\mu A} = 1.3M\Omega$$

Ex 20) Determine the levels of R_C , R_E , R_1 & R_2 for the network of given figure for the operating point indicated, $V_{CC} = 20V$



current gain stabilized circuit for design considerations

$$Q1) V_E = \frac{1}{10} V_{CC} = \frac{1}{10} (20V) = 2V$$

$$R_E = \frac{V_E}{I_E} \approx \frac{V_E}{I_C} = \frac{2V}{10mA} = 200\Omega$$

$$R_C = \frac{V_{RE}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20V - 8V - 2V}{10mA} = 10V = 10mA$$

$(R_C = 1k\Omega)$

$$V_B = V_{BE} + V_E = 0.7V + 2V = \underline{\underline{2.7V}}$$

For the circuit to operate efficiently, it is assumed that the current through R_1 & R_2 should be approximately equal to & much larger than the base current (at least 10:1).

This fact & the voltage divider equation for the base voltage provide the two relationships necessary to determine the base resistors.

i.e. $R_2 \leq \frac{1}{10} \beta R_E$ & $V_B = \frac{R_2}{R_1 + R_2} V_{CC}$

substitution yields, $R_2 \leq \frac{1}{10} (80)(0.2k\Omega)$

$$V_B = 2.7V = \frac{(1.6k\Omega)(20V)}{R_1 + 1.6k\Omega}$$

$$\& 2.7R_1 + 4.32k\Omega = 32k\Omega$$

$$2.7R_1 = 27.68k\Omega$$

$$R_1 = 10.25k\Omega \quad \text{use } \underline{\underline{10k\Omega}} \text{ (std)}$$

* FOR PNP Transistors -

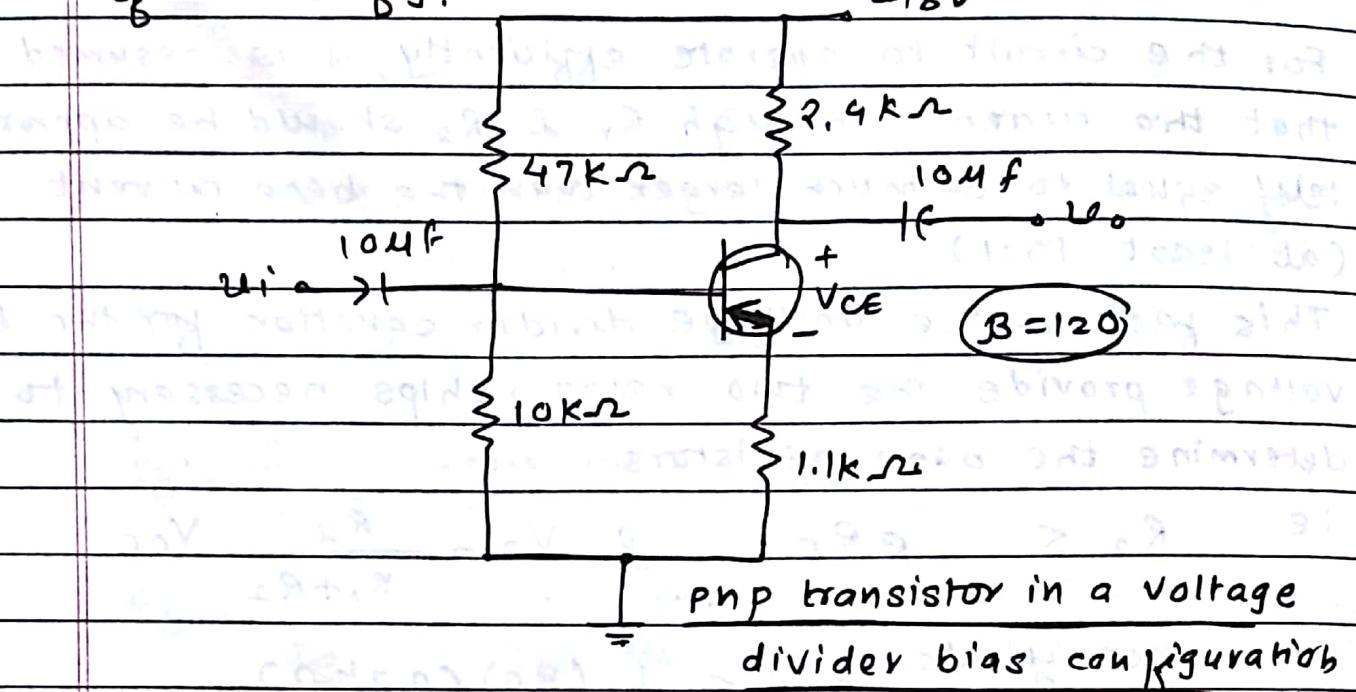
Only difference between the resulting equations for any type of biasing network in which an npn transistor has been replaced by a pnp transistor is the sign associated with particular quantities.

e.g. for emitter bias configuration,

$$I_B = \frac{V_{CC} + V_{BE}}{R_B + (\beta + 1)R_E}$$

$$V_{CE} = -V_{CC} + I_C(R_C + R_E)$$

Ex 21. Determine V_{CE} for the voltage divider bias configuration of shown fig.



Soln Testing the condition $\beta R_E \geq 10R_2$

$$\text{results in } (120)(1.1\text{k}\Omega) \geq 10(47\text{k}\Omega)$$

$$132\text{k}\Omega \geq 100\text{k}\Omega \text{ (satisfied)}$$

solving for V_B ,

$$V_B = \frac{R_2 \cdot V_{CC}}{R_1 + R_2} = \frac{(10\text{k}\Omega)(-18\text{V})}{47\text{k}\Omega + 10\text{k}\Omega} = -3.1\text{V}$$

Applying KVL around BE loop yields-

$$V_B - V_{BE} - V_E = 0$$

$$V_E = V_B - V_{BE}$$

$$= -3.1\text{V} - (-0.7\text{V})$$

$$V_E = -2.4\text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{-2.4\text{V}}{1.1\text{k}\Omega} = 2.24\text{mA}$$

for the collector-emitter loop,

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

$$\text{But } I_E \approx I_C \therefore V_{CE} = -V_{CC} + I_C (R_C + R_E)$$

$$V_{CE} = -18\text{V} + (2.24\text{mA})(2.4\text{k}\Omega + 1.1\text{k}\Omega)$$

$$\therefore V_{CE} = -10.16\text{V}$$

* Bias stabilization -

The stability of a system is a measure of the sensitivity of a network to variations in its parameter.

- In any amplifier employing a transistor the collector current I_C is sensitive to each of the following parameters -

β : increase with increase in temperature

$|V_{BE}|$: decrease about 2.5 mV per degree Celsius ($^{\circ}\text{C}$)
increase in temperature

I_{CO} (reverse saturation current) : doubles in value for every 10°C increase in temperature

Stability factors $S(I_{CO})$, $S(V_{BE})$ & $s(\beta)$ -

A stability factor 's' is defined for each of the parameters affecting bias stability as follows -

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}$$

$$s' = S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

$$s'' = s(\beta) = \frac{\Delta I_C}{\beta}$$

Networks that are quite stable & relatively insensitive to temperature variations have low stability factors.

The higher the stability factor, the more sensitive is the network to variations in that parameter.

* Derivation/Expression for the stability factor 's'

$$S = \frac{\Delta I_C}{\Delta I_{C0}} \quad \text{constant } V_{BE} \text{ & } \beta_{dc}$$

For a CE configuration, we know that

$$\begin{aligned} I_C &= \beta_{dc} I_B + I_{CEO} \\ &= \beta_{dc} I_B + (1 + \beta_{dc}) I_{CBO} \end{aligned}$$

changes in I_C is given by

$$\Delta I_C = \beta_{dc} \Delta I_B + (1 + \beta_{dc}) \Delta I_{CBO}$$

dividing both the sides by ΔI_C ,

$$\frac{\Delta I_C}{\Delta I_C} = \beta_{dc} \left[\frac{\Delta I_B}{\Delta I_C} \right] + (1 + \beta_{dc}) \left[\frac{\Delta I_{CBO}}{\Delta I_C} \right]$$

$$1 - \beta_{dc} \left[\frac{\Delta I_B}{\Delta I_C} \right] = (1 + \beta_{dc}) \left[\frac{\Delta I_{CBO}}{\Delta I_C} \right]$$

$$\therefore \frac{\Delta I_{CBO}}{\Delta I_C} = \frac{1 - \beta_{dc} [\Delta I_B / \Delta I_C]}{(1 + \beta_{dc})}$$

$$\text{But } S = \frac{\Delta I_C}{\Delta I_{CBO}} \quad \therefore S = \frac{(1 + \beta_{dc})}{1 - \beta_{dc} \left[\frac{\Delta I_B}{\Delta I_C} \right]} \quad (1)$$

For Fixed Bias ckt,

$I_B = \frac{V_{cc} - V_{BE}}{R_B}$ But V_{cc} , V_{BE} & R_B all are fixed, so I_B cannot change.

$\therefore \Delta I_B = 0$ put in eqn(1).

$$S = (1 + \beta_{dc}) \quad - \text{for fixed Bias config.}$$

Expression for stability factors' for fixed Bias -

$$S' = \frac{\partial I_C}{\partial V_{BE}}$$

const I_{CO} & β_{DC}

we know for CE,

$$I_C = \beta_{DC} I_B + (1 + \beta_{DC}) I_{CO} \quad \text{--- (1)}$$

We need to put value of I_B ,

which we can get by applying KVL.

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \text{Put in eqn (1)}$$

$$I_C = \beta_{DC} \left[\frac{V_{CC} - V_{BE}}{R_B} \right] + (1 + \beta_{DC}) I_{CO}$$

BUT I_{CO} & I_{CO} are same.

$$\therefore I_C R_B = \beta_{DC} V_{CC} - \beta_{DC} V_{BE} + (1 + \beta_{DC}) I_{CO} R_B$$

Differentiate this eqn w.r.t V_{BE} ,

$$R_B \cdot \frac{\partial I_C}{\partial V_{BE}} = 0 - \beta_{DC} + 0$$

$$R_B \cdot S' = -\beta_{DC}$$

$$S' = \frac{-\beta_{DC}}{R_B}$$

-ve sign indicates that

I_C decreases as temperature

L(2)

increases due to reduction in
 V_{BE} at increased temp.

Relation between S & S' -

$$S = (1 + \beta_{DC})$$

$$\text{from eqn (2)} \quad \beta_{DC} = -S' R_B$$

$$S = 1 - S' R_B$$

or

$$S' = \frac{(1 - S)}{R_B}$$

* Expression for stability factor s'' for a fixed bias

$$s'' = \frac{\partial I_c}{\partial \beta_{dc}} \quad | \quad I_{c0} \text{ & } V_{BE} \text{ constant}$$

$$\text{for CE, } I_c = \beta_{dc} I_B + (1 + \beta_{dc}) I_{cbo}$$

$$= \beta_{dc} I_B + \beta_{dc} I_{cbo} + I_{cbo}$$

Differentiate both side w.r.t β_{dc} ,

$$\frac{\partial I_c}{\partial \beta_{dc}} = I_B + I_{cbo} + 0$$

Neglecting I_{cbo} , we get,

$$s'' = \frac{\partial I_c}{\partial \beta_{dc}} = I_B - \frac{I_c}{\beta_{dc}}$$

$$s'' = \frac{I_c}{\beta_{dc}}$$

out of s , s' & s'' the stability factor s is significantly higher than the remaining two.

$$\therefore S = (1 + \beta_{dc}) \quad \text{for Fixed Bias config.}$$

* Stability Factor S for Emitter Bias configuration -

- Find value of $\Delta I_B / \Delta I_C$ & put in eqn ①

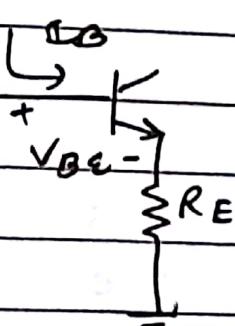
- To obtain the value of $\Delta I_B / \Delta I_C$

V_{CC}

Apply KVL to Base ckt,

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

$$= I_B R_B + V_{BE} + (I_C + I_B) R_E$$



$$I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{(R_B + R_E)}$$

$$I_B = \frac{V_{CC}}{(R_B + R_E)} - \frac{V_{BE}}{(R_B + R_E)} - \frac{I_C R_E}{(R_B + R_E)}$$

But $V_{CC}, V_{BE}, R_B, R_E, \beta_{dc}$ are constant.

Hence differentiation of 1st two terms with respect to I_C will be zero.

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{(R_B + R_E)}$$

$$\frac{\Delta I_B}{\Delta I_C} = \frac{-R_E}{(R_B + R_E)} \quad \text{Put this in eqn ①,}$$

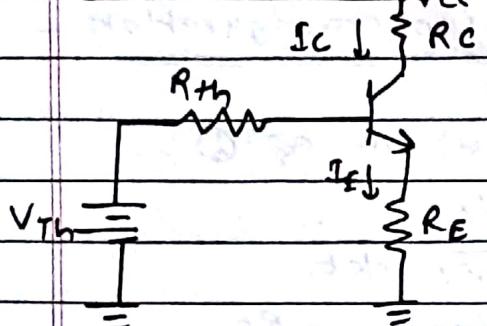
$$S = \frac{(1 + \beta_{dc})}{1 - \beta_{dc} \left[\frac{-R_E}{R_B + R_E} \right]}$$

$$S = \frac{(1 + \beta_{dc})}{1 + \left[\frac{R_E \beta_{dc}}{R_B + R_E} \right]}$$

Here denominator will always > 1 ,
 $\therefore S < (1 + \beta_{dc})$
 Thus Emitter Bias has improved stability.

* Stability Factor for Voltage divider Bias circuit -

To obtain value of $\frac{\Delta I_B}{\Delta I_C}$



Apply KVL,

$$V_{Th} = I_B R_B + V_{BE} + (I_C + I_B) R_E$$

If we consider V_{BE} to be independent of I_C , we can differentiate this eqn w.r.t I_C ,

Thevenin's equivalent circuit
for voltage divider bias

$$\therefore \alpha = R_B \frac{\partial I_B}{\partial I_C} + 0 + R_E + R_E \frac{\partial I_B}{\partial I_C}$$

$$0 = \frac{\partial I_B}{\partial I_C} (R_B + R_E) + R_E$$

$$\frac{\partial I_B}{\partial I_C} = - \frac{R_E}{(R_B + R_E)}$$

$$\frac{\Delta I_B}{\Delta I_C} = - \frac{R_E}{(R_B + R_E)} \quad \text{Put in eqn ①,}$$

$$S = \frac{1 + \beta_{dc}}{1 - \beta_{dc} \left[\frac{-R_E}{R_B + R_E} \right]}$$

$$S = \frac{1 + \beta_{dc}}{1 + \beta_{dc} \left[\frac{R_E}{R_B + R_E} \right]} = \frac{(1 + \beta_{dc})(R_B + R_E)}{R_B + R_E + \beta_{dc} R_E}$$

$$= \frac{(1 + \beta_{dc})(R_B + R_E)}{R_B + (1 + \beta_{dc}) R_E} \quad \text{divide N & D by } R_E$$

$$S = (1 + \beta_{dc}) \frac{1 + (R_B/R_E)}{(1 + \beta_{dc}) + (R_B/R_E)}$$

- The value of s depends on the ratio (R_B/R_E). If (R_B/R_E) is small then the value of $s=1$ & if the ratio $(R_B/R_E) \rightarrow \infty$ then $s \in (1+\beta_{dc})$. Thus self bias ckt is more stable for smaller values of the ratio (R_B/R_E)
- If the ratio (R_B/R_E) is fixed then s increases with increase in the value of β_{dc} . Thus stability decreases with increase in β_{dc} .
- s is independent of β_{dc} for small values of β_{dc}
- Smaller values of R_B give better stabilization.

* stability factor's for collector to Base Bias :-

To obtain $\Delta I_B / \Delta V_{CC}$ -

For collector to base bias, we can write

$$\begin{aligned} V_{CC} &= R_C(I_C + I_B) + I_B R_B + V_{BE} \\ &= I_C R_C + I_B (R_B + R_C) + V_{BE} \end{aligned}$$

V_{BE} & β_{dc} are assumed to be constants.

V_{CC} & V_{BE} do not change.

$$0 = \Delta I_C R_C + \Delta I_B (R_B + R_C)$$

$$-\Delta I_C R_C = \Delta I_B (R_B + R_C)$$

$$\frac{\Delta I_B}{\Delta I_C} = \frac{-R_C}{(R_B + R_C)} \quad \text{put in eqn ①}$$

$$S = \frac{(1 + \beta_{dc})}{1 - \beta_{dc}}$$

$$\left[\frac{-R_C}{R_B + R_C} \right]$$

of S of fixed bias
& collector to base
bias ckt is compared,
 S for collector to base
bias is much less.

$S = \frac{1 + \beta_{dc}}{1 + \beta_{dc}} \left[\frac{R_C}{R_B + R_C} \right]$
--

This indicates 'Q'pt stability is better for collector to Base ckt.

* Thermal Runaway -

The maximum power that a transistor can dissipate without getting damaged depends largely on the maximum temperature that a collector base junction can withstand.

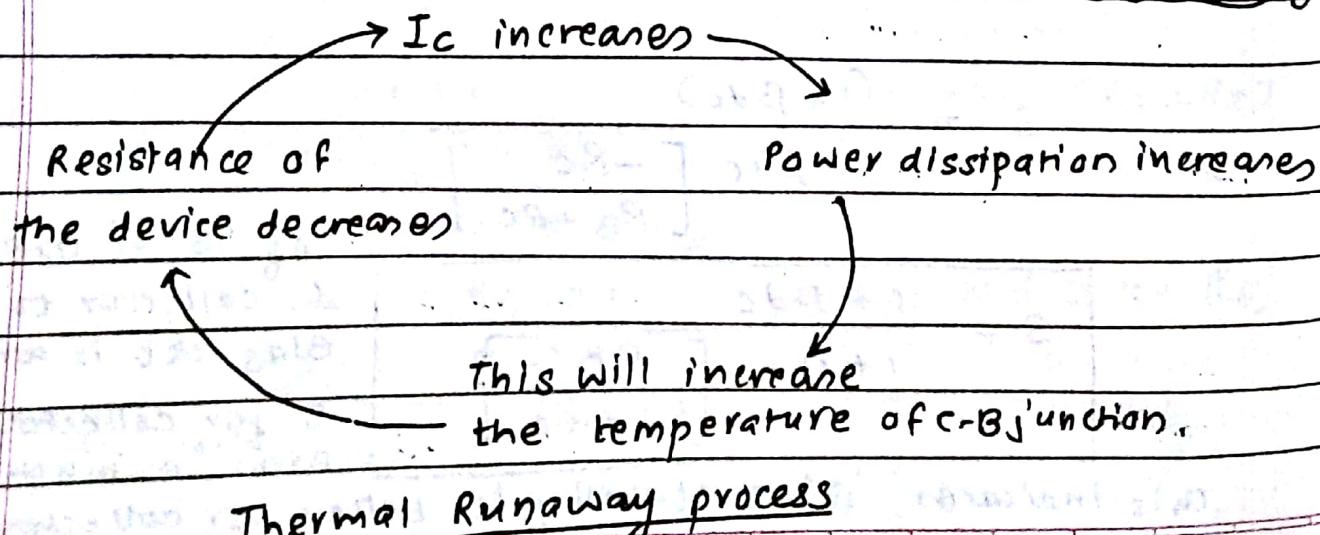
The rise in the collector base junction takes place due to two reasons :-

1. Due to increase in the ambient temperature
2. Due to the internal heating

Out of them the internal heating process is cumulative as explained below :-

1. An increase in collector current I_C increases the power dissipated in the collector base junction of the transistor.
2. This will increase the temperature of C-B junction.
3. As the transistor has a negative temperature coefficient of resistivity, increased junction temperature reduces the resistance.
4. The reduced resistance will increase the collector current further.

This becomes a cumulative process which will finally damage the transistor due to excessive internal heating. This process is known as "Thermal Runaway".



* How to avoid thermal runaway?

- Never exceed the collector current beyond a certain maximum value specified by the manufacturer.
- Never exceed the internal power dissipation above the maximum permissible level/value.
- Use heat sink.

* Bias compensation -

The collector to base bias circuit & voltage divider circuit are examples of feedback amplifiers.

- Due to the negative feedback present in these ckt, the amplification of the AC signal is reduced drastically.
- If this loss of signal cannot be tolerated then the compensation techniques are used to reduce the drift in the operating point.

Very often both stabilization & compensation techniques are used to provide maximum bias & thermal stabilization.

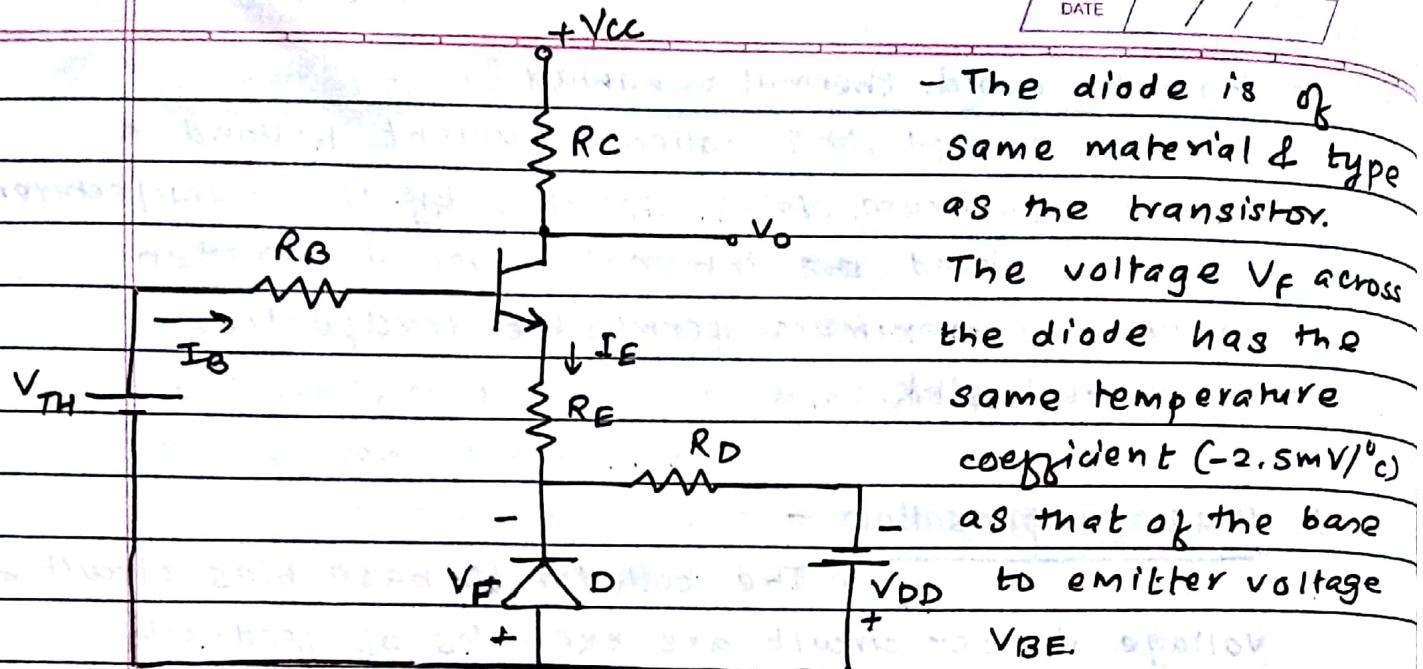
Types of compensation techniques are -

1. Compensation for changes in V_{BE} &
2. compensation for changes in I_{CO} .

* Diode compensation for V_{BE} -

The voltage divider bias circuit with diode compensation is as shown in next fig.

- The additional power supply V_{DD} is connected in order to forward bias diode D.



Diode compensation for V_{BE}

Apply KVL for the base circuit,

$$V_{TH} = I_B R_B + V_{BE} + (I_B + I_c) R_E - V_f \quad \text{--- (1)}$$

$$\text{But } I_c = \beta_{dc} I_B + (1 + \beta_{dc}) I_{CBO} \quad \text{--- (2)}$$

$$\therefore V_{TH} = I_B (R_B + R_E) + V_{BE} + I_c R_E - V_f \quad \text{--- (3)}$$

from eqⁿ (2),

$$I_B = \frac{I_c}{\beta_{dc}} = \frac{(1 + \beta_{dc}) I_{CBO}}{\beta_{dc}} \quad \text{Put this value of } I_B \text{ in eqⁿ (3).}$$

$$\begin{aligned}
 V_{TH} &= \frac{I_c (R_B + R_E)}{\beta_{dc}} - \frac{(1 + \beta_{dc})(R_B + R_E)}{\beta_{dc}} I_{CBO} + V_{BE} + \\
 &\quad I_c R_E - V_f \\
 &= V_{BE} - V_f + \underbrace{R_B + R_E}_{\beta_{dc}} \frac{(1 + \beta_{dc})}{\beta_{dc}} I_c - \frac{(R_B + R_E)}{\beta_{dc}} (1 + \beta_{dc}) I_{CBO}
 \end{aligned}
 \quad \text{--- (4)}$$

These terms are equal & opposite, so they cancel each other.

- The material used for the diode is same as that for the transistor & has same temperature coefficient.

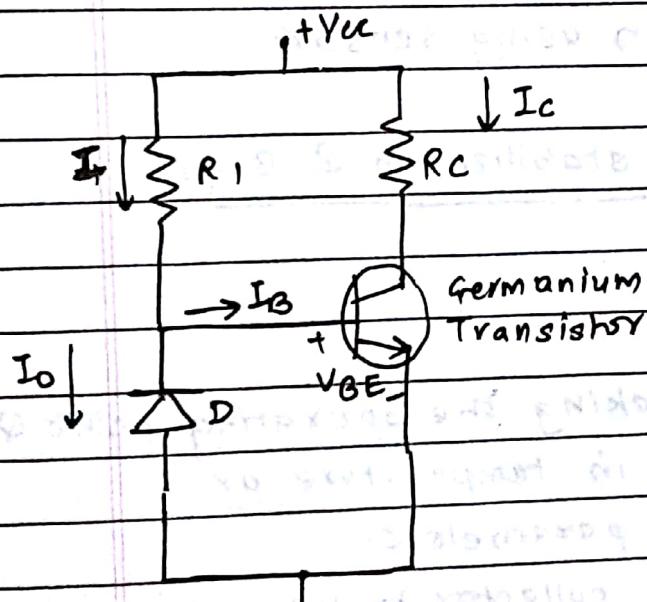
- Hence the change in voltage across the diode (V_F) will be equal to change in V_{EE} due to temperature changes. Hence the first two terms in last eqⁿ ④ cancel each other.

- Thus the change in V_{BE} due to temperature is compensated by change in V_F & the collector current becomes insensitive to variation in V_{BE} .

*2. Diode compensation for I_{CO} -

For the germanium

transistors, changes in I_{CO} due to change in temp is more prominent than changes in V_{BE} due to temperature. The diode compensation circuit shown in next figure offers the stabilization against variation in I_{CO} .



- The diode & the transistor are of same type & material.

- Therefore the reverse saturation current of the diode i.e I_0 will increase with temperature at the same rate as the current I_{CO} .

Diode compensation for I_{CO} from fig,

$$I = \frac{V_{CC} - V_{BE}}{R_1} \approx \frac{V_{CC}}{R_1} \text{ const.}$$

The base current $I_B = I - I_0$

$$\text{We know, } I_C = \beta_{DC} I_B + (1 + \beta_{DC}) I_{CO}$$

$$= \beta_{DC} (I - I_0) + (1 + \beta_{DC}) I_{CO}$$

$$I_C = \beta_{DC} I - \beta_{DC} I_0 + (1 + \beta_{DC}) I_{CO} \quad \text{--- (1)}$$

If the saturation current of the diode (I_0) is equal to the leakage current I_{CO} of the transistor, then the last two terms in above eqⁿ① will get cancelled.

$$I_c = \beta_{DC} I \quad (\because \beta_{DC} T_C \approx (1 + \beta_{DC}) I_{CO})$$

As $I = \text{constant}$, I_c will also remain constant & compensation is provided.

- Looking at the last two terms of eqⁿ①, we conclude that if $\beta_{DC} \gg 1$, if I_0 of D & I_{CO} of the transistor track each other over the desired temperature range then I_c will remain constant. Thus compensation is provided.

NOTE - There are two more ways of Bias compensation

- Bias compensation using Thermistor
- Bias compensation using sensor

* Difference between Bias stabilization & Bias compensation-

Bias stabilization -

- It is a process of making the operating point Q independent of change in temperature or variations of transistor parameters.
- Self Bias, fixed Bias & collector to base bias circuits are the bias stabilization circuits.

Bias compensation -

- The bias stabilizing circuit use a negative feedback. This will reduce the amplification of AC signals drastically.

- If this loss of signal is not to be tolerated then bias compensation techniques are used to reduce the drift in the operating point.

Bias compensation ckt's are -

1. Diode compensation
2. Thermistor compensation.