ARM Processor cores

Prardiva Mangilipally

ARM Ltd

- Founded in November 1990
  - Spun out of Acorn Computers
- Designs the ARM range of RISC processor cores
- Licenses ARM core designs to semiconductor partners who fabricate and sell to their customers.
  - ARM does not fabricate silicon itself
- Also develop technologies to assist with the design-in of the ARM architecture
  - Software tools, boards, debug hardware, application software, bus architectures, peripherals etc

Intoduction

- Leading provider of 32-bit embedded RISC microprocessors, 75% of market
  - High performance
  - Low power consumption
  - Low system cost
- Solutions for
  - Embedded real-time systems for mass storage,
  - automotive, industrial and networking applications
  - Secure applications - smartcards and SIMs
  - Open platforms running complex

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- ARMv1

  First version of ARM processor

  26-bit addressing, no multiply / coprocessor

- ARMv2

  ARM2, First commercial chip

  Included 32-bit result multiply instructions /

  coprocessor support

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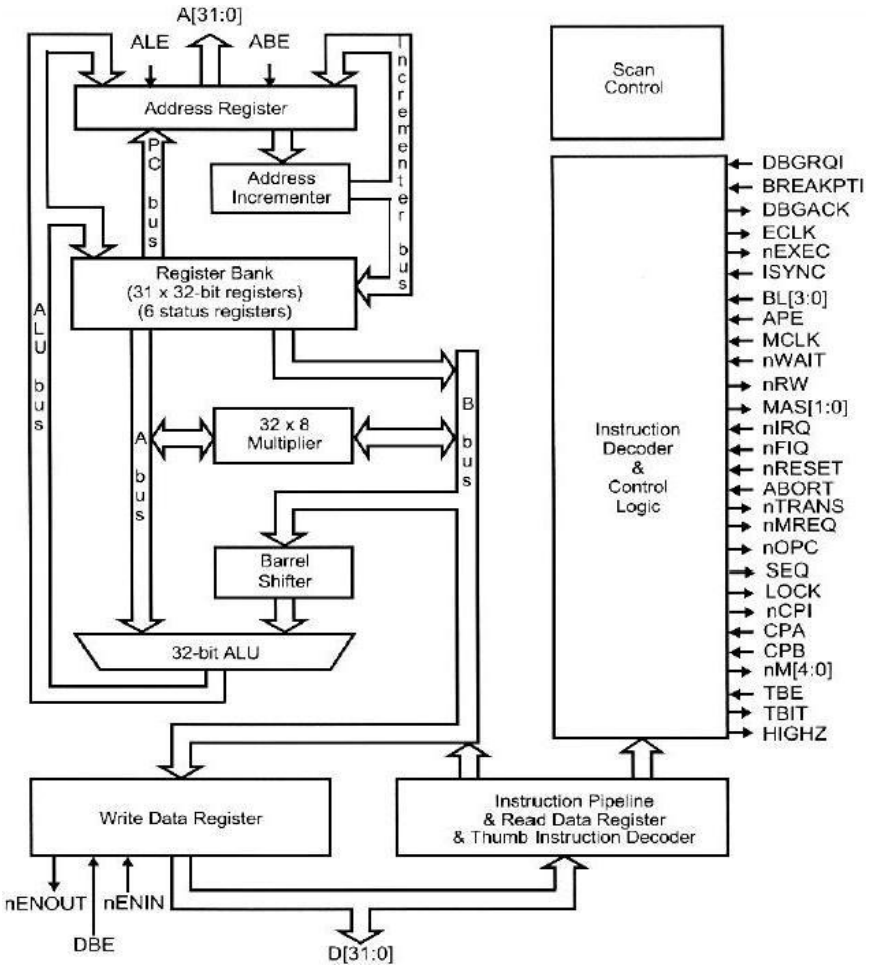
- ARMv2a
  ARM3 chip with on-chip cache
  Added load and store
  cache management

- ARMv3
  ARM6, 32 bit addressing, virtual
  memory support

ARM Processor Core

- Current low-end ARM core for applications like digital mobile phones
- TDMI
  - T: Thumb, 16-bit instruction set
  - D: on-chip Debug support, enabling the processor to halt in response to a debug request
  - M: enhanced Multiplier, yield a full 64-bit result, high performance
  - I: EmbeddedICE hardware
- Von Neumann architecture
- 3-stage pipeline

ARM Core Diagram



The Registers

- ARM has 37 registers all of which are 32-bits long.
  - 1 dedicated program counter
  - 1 dedicated current program status register
  - 5 dedicated saved program status registers
  - 30 general purpose registers
- The current processor mode governs which of several banks is accessible. Each mode can access
  - a particular set of r0-r12 registers
  - a particular r13 (the stack pointer, sp) and r14 (the link register)
  - the program counter, r15 (pc)
  - the current program status register,

DIFFERENT STATES

- When the processor is executing in ARM state:
  - All instructions are 32 bits wide
  - All instructions must be word aligned
- When the processor is executing in Thumb state:
  - All instructions are 16 bits wide
  - All instructions must be halfword aligned
- When the processor is executing in Jazelle state:
  - All instructions are 8 bits wide
  - Processor performs a word access to read 4 instructions at once

Thumb

- Thumb is a 16-bit instruction set
  - Optimised for code density from C code (~65% of ARM code size)
  - Improved performance from narrow memory
  - Subset of the functionality of the ARM instruction set
- execution state - Thumb
  - Switch between ARM and Thumb using BX
  - 32-bit ARM instruction
  - 16-bit Thumb instruction

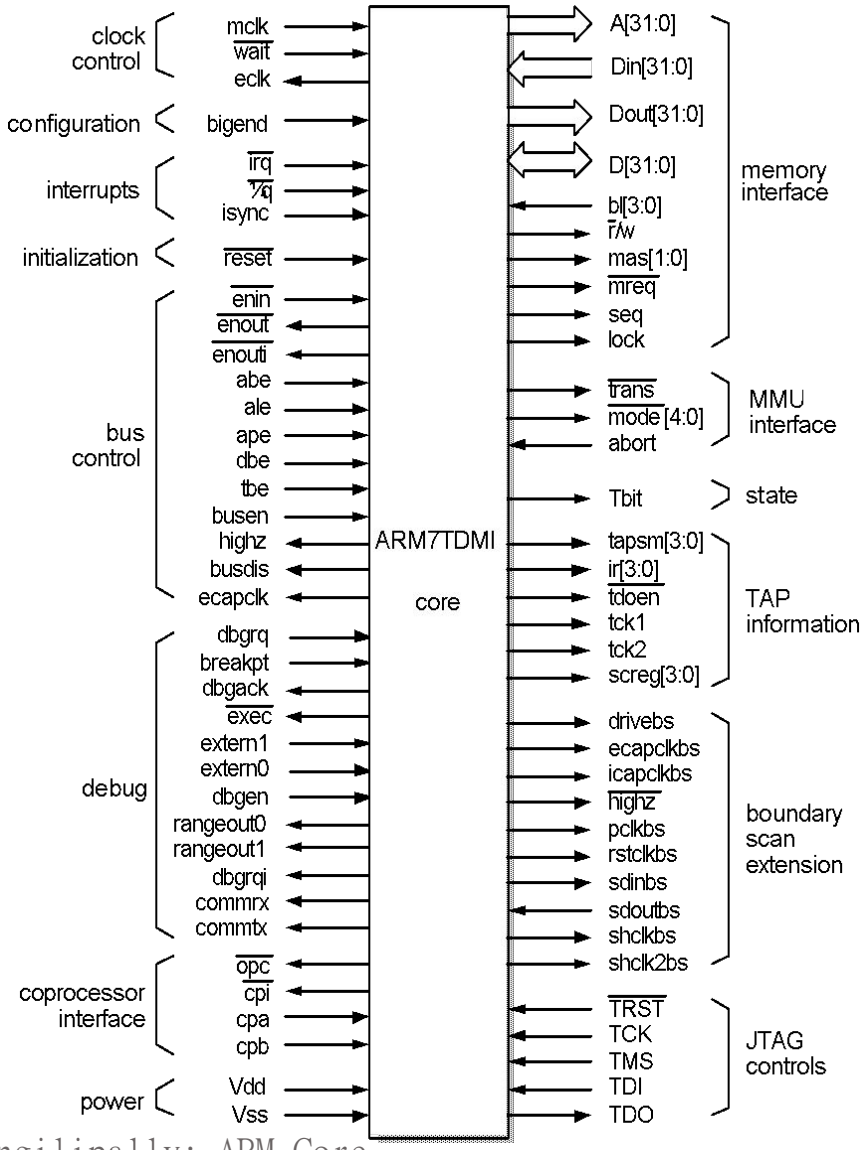
```
ADDS r2,r2,#1
```

```
ADD r2,#1
```

For most instructions generated by compiler:

- Conditional execution is not used
- Source and destination registers identical
- Only Low registers used
- Constants are of limited size
- Inline barrel shifter not used

ARM Interface Signals (1/4)



ARM Interface Signals (2/4)

- Clock control
  - All state change within the processor are controlled by *mclk*, the memory clock
  - Internal clock = *mclk* AND *\wait*
  - *eclk* clock output reflects the clock used by the core
- Memory interface
  - 32-bit address *A[31:0]*, bidirectional data bus *D[31:0]*, separate data out *Dout[31:0]*, data in *Din[31:0]*
  - *seq* indicates that the memory address will be sequential to that used in the previous cycle

$\overline{\text{mreq}}$	seq	Cycle	Use
0	0	N	Non-sequential memory access
0	1	S	Sequential memory access
1	0	I	Internal cycle – bus and memory inactive
1	1	C	Coprocessor register transfer – memory inactive

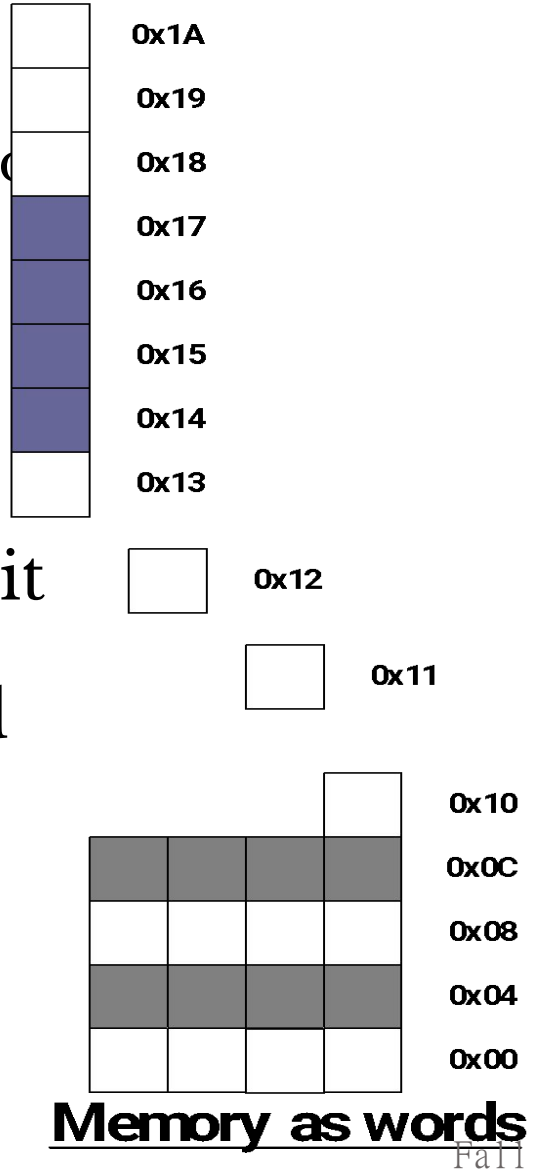
ARM Interface Signals (3/4)

- Interrupt
  - \fiq, fast interrupt request, higher priority
  - \irq, normal interrupt request
  - isync, allow the interrupt synchronizer to be passed
- Initialization
  - \reset, starts the processor from a known state, executing from address 00000000_{16}
- ARM characteristics

Process	0.35 um	**Transistors**	74,209	**MIPS**	60
Metal layers	3	**Core area**	2.1 mm^2	**Power**	87 mW
Vdd	3.3 V	**Clock**	0 to 66 MHz	**MIPS/W**	690

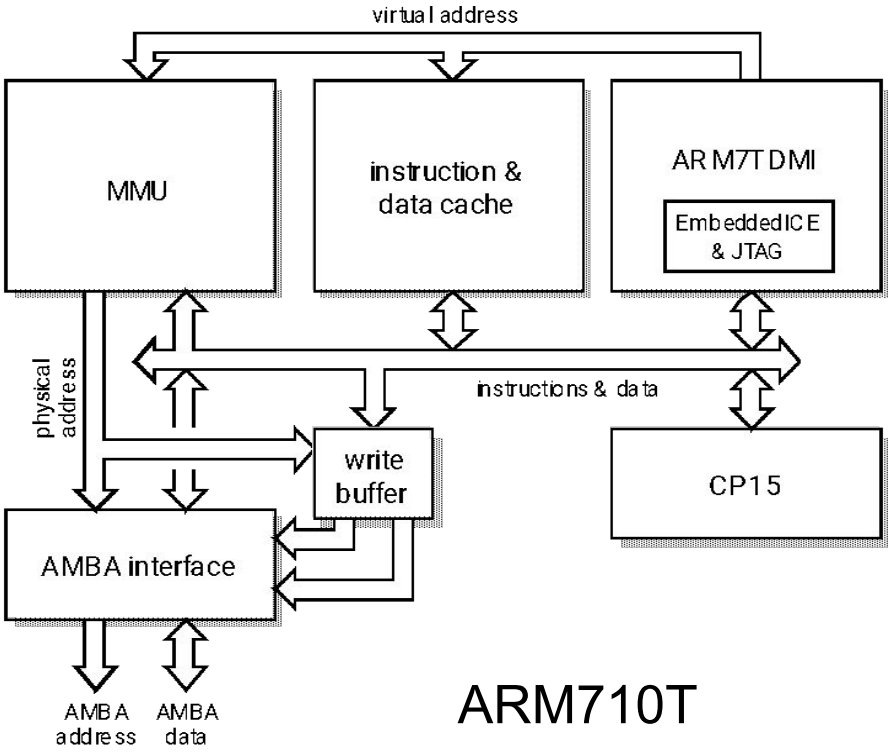
Memory Access

- The ARM is a Von Neumann, load/store architecture, i.e.,
  - Only 32 bit data bus for both inst. And data.
  - Only the load/store inst. (and SWP) access memory.
- Memory is addressed as a 32 bit address space
- Data type can be 8 bit bytes, 16 bit half-words or 32 bit words, and may be seen as a byte line folded into 4-byte words



Processor Core Vs CPU Core

- Processor Core
  - The engine that fetches instructions and execute them
  - E.g.: ARM7TDMI, ARM9TDMI, ARM9E-S
- CPU Core
  - Consists of the ARM processor core and some tightly coupled function blocks
  - Cache and memory management blocks
  - E.g.: ARM710T, ARM720T, ARM74T, ARM920T, ARM922T, ARM940T, ARM946E-S, and ARM966E-S



ARM710T

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Thank you