* Depletion Type MOSFETs :-

The similarities in appearance betn the transfer curve of JFETs & depletion type MOSFETs permit a similar analysis of each in dc domain.

- The primary difference betn the two is the fact that the depletion type MOSFETs permit operating point with positive values of V_{GS} & the level of I_D that exceeds I_{DSS}.
- In fact, for all the config, discussed so far, the analysis is the same if the JFET is replaced by a depletion type MOSFET.
- The only undefined part of the analysis is how to plot the Shockley's eqn for +ve values of V_{GS}.

How far into the region of +ve values of V_{GS} & values of I_D greater than I_{DSS} does the transfer curve have to extend?

- For most situations, this required range will be fairly well defined by MOSFET parameters & the resulting bias line of the N/W.

Biasing for DMOSFET :-

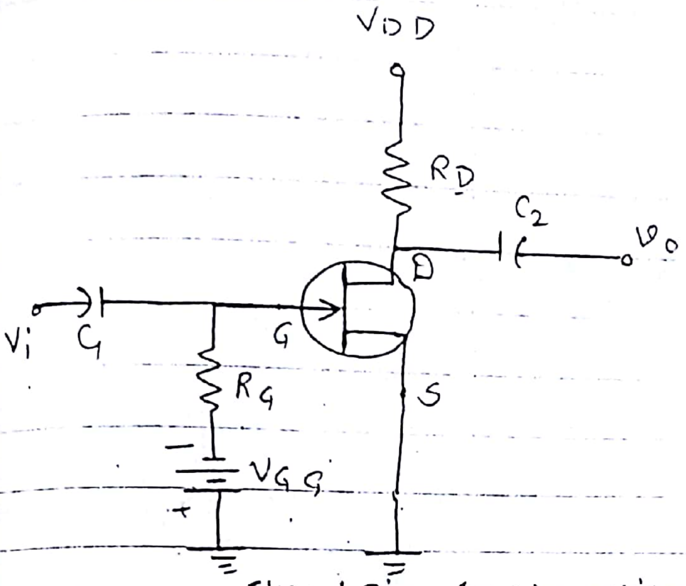
① Fixed Bias ckt : - same as that of JFET

② Voltage divider Bias ckt -

with a example

① Fixed Bias Configuration :-

- It is one of the simplest biasing arrangement, for n-channel JFET.
- It is one of the few FET config that can be solved just as directly using either a mathematical or a graphical approach.



Fixed Bias configuration

ⓐ Mathematical ~~Approach~~ :-

Dc Analysis :-

- C_1, C_2 are open ckt for dc analysis, & s.c for ac analysis
- R_G is present to ensure that V_i appears at the i/p to FET amplifier for ac analysis.

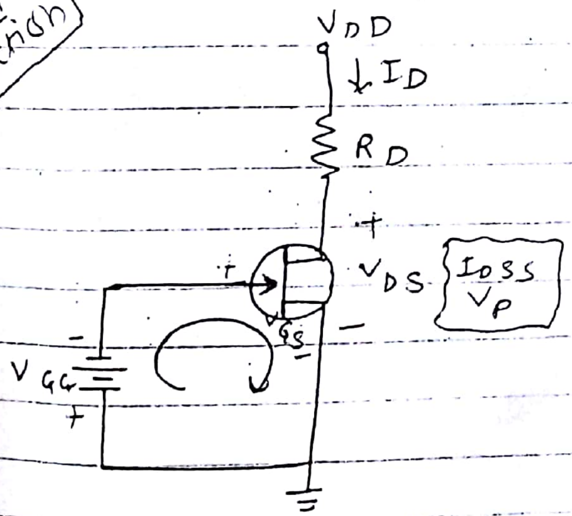
R_G For Dc analysis :-

$$I_G \cong 0 A$$

$$V_{RG} = I_G R_G = 0 \times R_G = 0V$$

- $\therefore V_{RG} \cong 0$ permits replacing R_G by s.c equivalent.

i/p section



Network for dc analysis

- Apply KVL in clockwise direction of the indicated loop,

$$-V_{GG} - V_{GS} = 0$$

$$\therefore \boxed{V_{GS} = -V_{GG}}$$

- Since V_{GG} is a fixed dc supply, the vtg V_{GS} is fixed in magnitude resulting in config - 'Fixed Bias.'

- The resulting level of I_D is controlled by Schockley's Eqn

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

To draw Transfer curve ⇒ $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$-V_{GS}$	I_D (mA)
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0

(b) Graphical Approach

A graphical analysis require a plot of shockley's Eq^n as shown in fig (a)

- choosing $V_{GS} = V_P/2$ will result in $I_D = I_{DSS}/4$ when plotting the eq^n.
- For this analysis 3 pts defined by I_{DSS}, V_P & the intersection just described will be sufficient for plotting the curve.

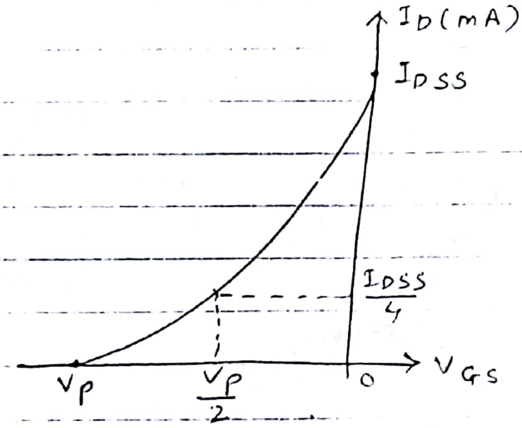


fig (a) plotting shockley's Eq^n

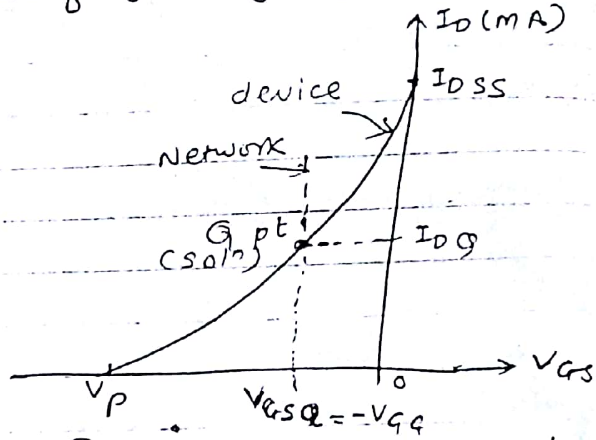
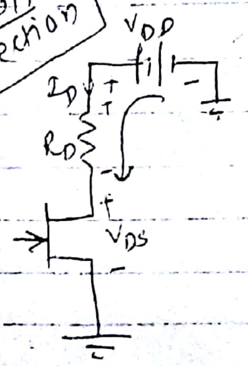


fig (b) finding sol^n for Fixed Bias config.

- The fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$.
- At any pt on the vertical line, the level of V_{GS} is $-V_{GG}$ – the level of I_D must simply be determined by this vertical line.
- The pt where the two curves intersect is the common sol^n to the config i.e quiescent or operating pt.
- The I_{DQ} is determined by drawing a horizontal line from the Q pt to the vertical I_D axis.

O/P section

- The V_{DS} of o/p section by KVL, ⇒ $V_{DD} - I_D R_D - V_{DS} = 0$



$$+V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore \boxed{V_{DS} = V_{DD} - I_D R_D} \qquad \& \qquad V_S = 0V$$

$$V_{DS} = V_D - V_S \qquad \text{ie} \quad V_D = V_{DS} + V_S = V_{DS} + 0V$$

$$\therefore \boxed{V_D = V_{DS}} \qquad \& \quad V_D = V_{DD} - I_D R_D$$

$$\& \quad V_{GS} = V_G - V_S$$

$$V_G = V_{GS} + V_S = V_{GS} + 0V$$

$$\boxed{V_G = V_{GS}}$$

disadvantage: As two power supplies are required it is not preferable.

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EXAMPLE 7.9 Determine the following for the

a. I_{D_Q} and V_{GS_Q}.
b. V_D.

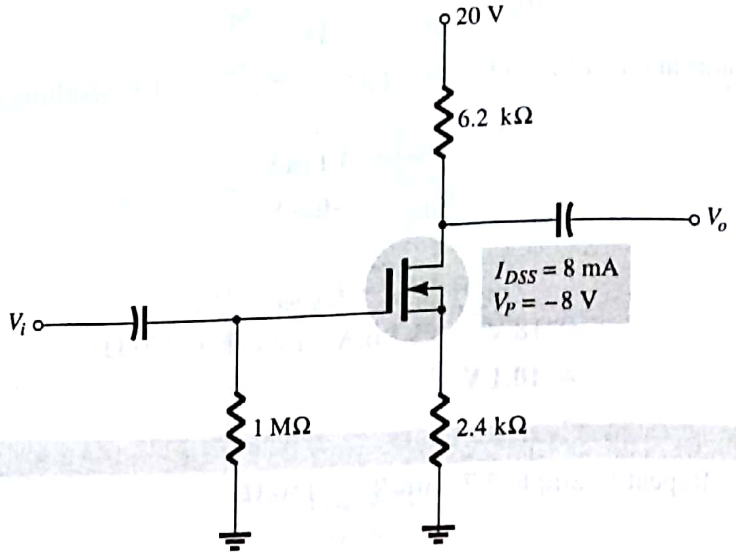


FIG. 7.34
Example 7.9.

Solution:

a. The self-bias configuration results in

$$V_{GS} = -I_D R_S$$

as obtained for the JFET configuration, establishing the fact that V_{GS} must be less than 0 V. There is therefore no requirement to plot the transfer curve for positive values of V_{GS}, although it was done on this occasion to complete the transfer characteristics. A plot point for the transfer characteristics for V_{GS} 6 0 V is

$$I_D = \frac{I_{DSS}}{4} = \frac{8\text{ mA}}{4} = 2\text{ mA}$$

and

$$V_{GS} = \frac{V_P}{2} = \frac{-8\text{ V}}{2} = -4\text{ V}$$

and for V_{GS} 7 0 V, since $V_P = -8$ V, we will choose

$$V_{GS} = +2\text{ V}$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8\text{ mA}\left(1 - \frac{+2\text{ V}}{-8\text{ V}}\right)^2$$
$$= 12.5\text{ mA}$$

The resulting transfer curve appears in Fig. 7.35. For the network bias line, at V_{GS} = 0 V, I_D = 0 mA. Choosing V_{GS} = −6 V gives

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{-6\text{ V}}{2.4\text{ k}\Omega} = 2.5\text{ mA}$$

The resulting Q-point is given by

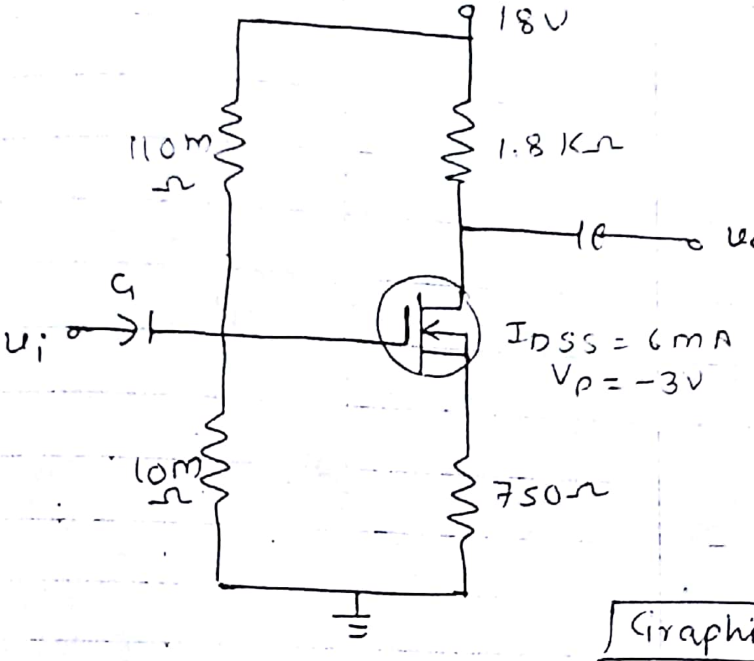
$$I_{D_Q} = \mathbf{1.7\text{ mA}}$$
$$V_{GS_Q} = \mathbf{-4.3\text{ V}}$$

b. $V_D = V_{DD} - I_D R_D$

$= 20\text{ V} - (1.7\text{ mA})(6.2\text{ k}\Omega)$
$= \mathbf{9.46\text{ V}}$

The example to follow employs a design that can also be applied to JFET transistors. At first impression it appears rather simplistic, but in fact it often causes some confusion when first analyzed due to the special point of operation.

(Ex 1.) For the n-channel depletion type MOSFET (DMOSFET) of given fig, determine (a) I_{DQ} & V_{GSQ} (b) V_{DS} (c)



Graphical Approach –

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 = 6mA\left[1-\left(\frac{1V}{-3V}\right)\right]^2 = \underline{\underline{10.67mA}}$$

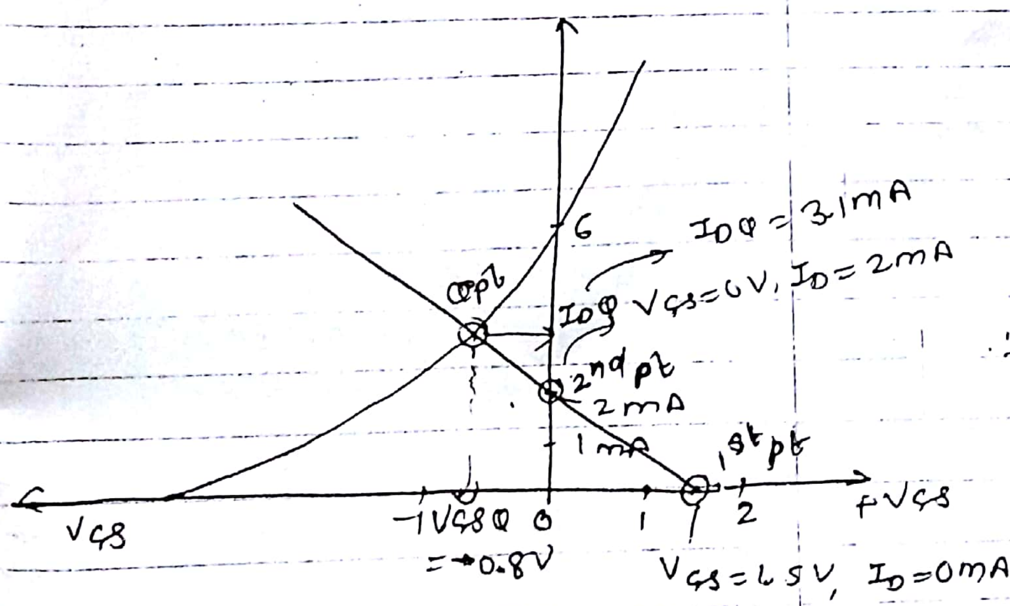
$$V_G = \frac{R_2 \times V_{DD}}{R_1 + R_2} = \underline{\underline{1.5V}}$$

$$V_{GS} = V_G - I_D R_S$$

$$\underbrace{V_{GS} = 1.5V - I_D(750\Omega)}$$

put $I_D = 0mA$, $V_{GS} = 1.5V$ pt ① ($I_D = 0mA$, $V_{GS} = 1.5V$)

$V_{GS} = 0V$, $I_D = V_G/R_S = \frac{1.5V}{750\Omega} = 2mA$ pt ② ($I_D = 2mA$, $V_{GS} = 0V$)



Determining Q pt for given N/W

$\therefore I_{DQ} = 3.1mA$

$V_{GSQ} = -0.8V$

$\therefore V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 18V - [3.1mA(1.8K + 750\Omega)]$

$\boxed{V_{DS} \cong 10.1V}$

$\boxed{I_D^2 + K_1 I_D + K_2 = 0}$

* **Mathematical Approach :-**

① $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$ — ①

$V_G = \frac{R_2 \times V_{DD}}{R_1 + R_2}$

$V_G = \frac{10 \times 18}{(10+110)} = 1.5V$ & $V_{GS} = V_G - I_D R_S$

$V_{GS} = 1.5 - 750 I_D$ — ②

put eqⁿ ② ie value of V_{GS} in eqⁿ ①.

$I_D = I_{DSS}\left[1 - \frac{(1.5 - 750 I_D)}{V_P}\right]^2$

$= 6 \times 10^{-3}\left[1 - \frac{1.5 - 750 I_D}{-3}\right]^2$

$= 6 \times 10^{-3}[1 + 0.5 - 250 I_D]^2$

$= 6 \times 10^{-3}[1.5 - 250 I_D]^2$

$= 6 \times 10^{-3}[2.25 - 750 I_D + 62500 I_D^2]$

$I_D = 0.0135 - 4.5 I_D + 375 I_D^2$

$\therefore$ $\boxed{375 I_D^2 - 5.5 I_D + 0.0135 = 0}$

solve this eqⁿ

$I_D = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$

$= \frac{+5.5 \pm \sqrt{(-5.5)^2 - 4(375 \times 0.0135)}}{2 \times 375}$

$\boxed{I_D = 11.55mA \quad \text{or} \quad I_D = 3.11mA}$

At $I_D = 11.55mA$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 18 - 11.55(1.8 + 0.75)$

$V_{DS} = -11.45V$

-ve V_{DS} is not acceptable as it is impossible practically.

$\therefore$ let us choose $I_{DQ} = 3.11mA$ $\therefore$ $I_{DQ} = 3.11mA$

② $V_{DSQ} \Rightarrow$

$V_{DS} = V_{DD} - I_D(R_S + R_D)$

$= 18 - 3.11(1.8 + 0.75)$

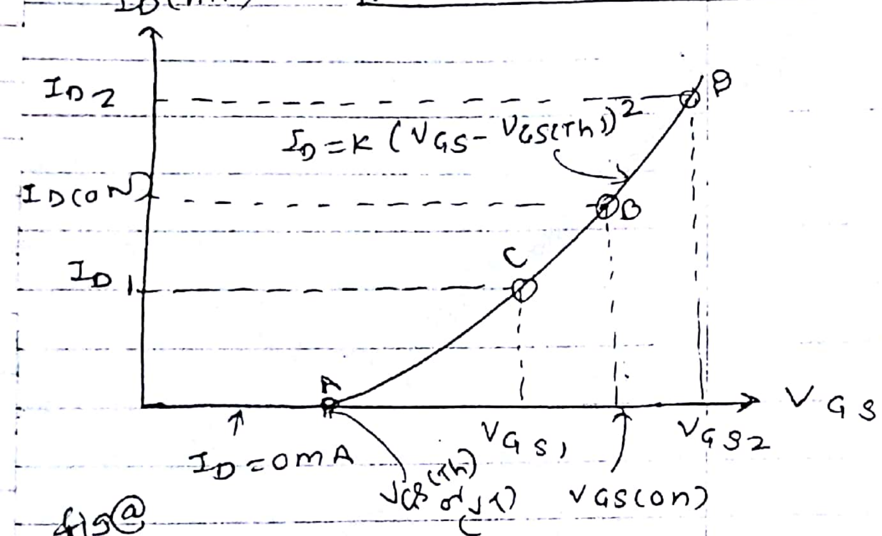
$\boxed{V_{DS} = 10.07V}$

★ Biasing for Enhancement MOSFETs (EMOSFET) :-

- The Transfer characteristics of EMOSFET is quite different from that of JFET & DMOSFET.
- for N-channel EMOSFET, $I_D = 0$ for $V_{GS} < V_{GS(Th)}$ it is shown in transfer curve below.

∴ For $V_{GS} > V_{GS(Th)}$, I_D is defined by

$$\boxed{I_D = k\left(V_{GS} - V_{GS(Th)}\right)^2} \quad \text{——} \ (1)$$



fig@ Transfer char. of n-channel EMOSFET

To complete the curve, the constant k of eqn (1) must be determined from the specification sheet data by substituting in eq (1) & solving for k as follows.

$$I_D = k\left(V_{GS} - V_{GS(Th)}\right)^2$$
$$I_{D(on)} = k\left(V_{GS(on)} - V_{GS(Th)}\right)^2$$

&

$$\boxed{k = \frac{I_{D(ON)}}{\left(V_{GS(ON)} - V_{GS(Th)}\right)^2}}$$

once k is defined other levels of I_D can be determined for chosen values of V_{GS}.

Typically, a pt betn $V_{GS(Th)}$ & $V_{GS(on)}$ & one just greater than $V_{GS(on)}$ will provide a sufficient number of pts to plot eqn (1). (Note I_{D1} & I_{D2} on fig. @)

* Biasing of EMOSFET – (1) Feedback Biasing
(2) Voltage Divider Bias

(1) Feedback Biasing Arrangement –

The resistor R_G brings a suitably large vtg to gate to drive MOSFET 'on'.

$\because$ $I_G = 0mA$ & $V_{RG} = 0V$, the dc equivalent N/W as shown in fig (b)

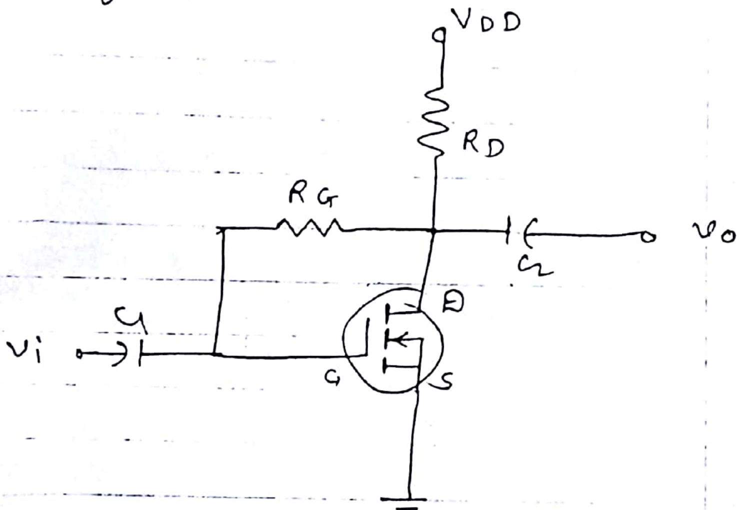


fig (a) feedback biasing N/W

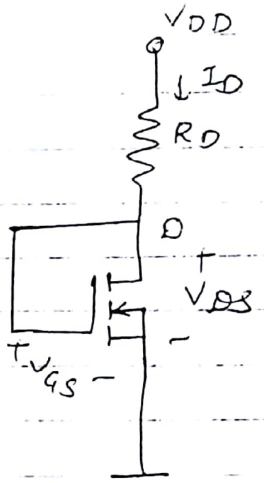


fig (b) DC equivalent

from fig (b), $\boxed{\begin{matrix} V_D = V_G \\ V_{DS} = V_{GS} \end{matrix}}$ —(1)

for o/p ckt, $V_{DS} = V_{DD} - I_D R_D$ put eqn (1)

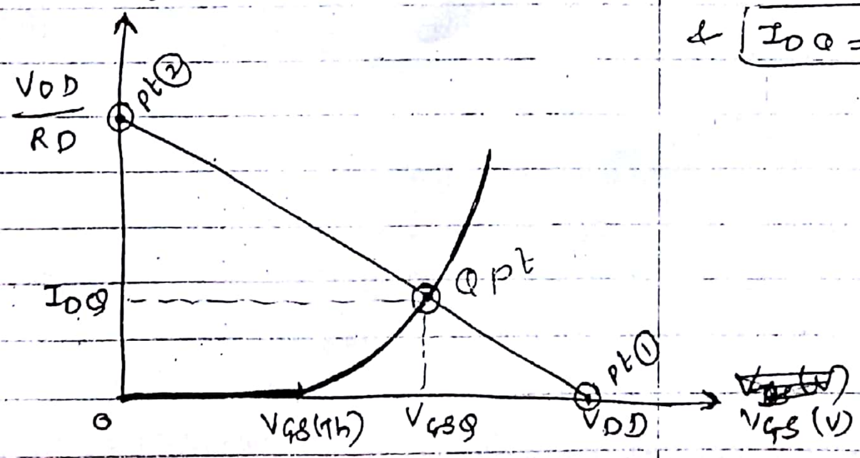
$\therefore \boxed{V_{DS} = V_{DD} - I_D R_D}$ — striaght line

$V_{DS} = V_{GS}$ (2) $\therefore V_{GS} = V_{DD} - I_D R_D$

pt (1) $I_D = 0mA$ in eqn (2) $\therefore$ $\boxed{V_{GS} = V_{DD} \big|_{I_D = 0mA}}$

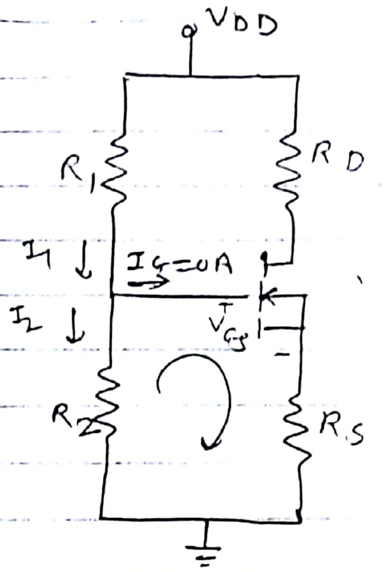
pt (2) $V_{GS} = 0V$, in eqn (2) $\boxed{I_D = \frac{V_{DD}}{R_D} \Big|_{V_{GS} = 0V}}$

& $\boxed{I_{DQ} = k\,[V_{GS} - V_{GS(Th)}]^2}$



Determining Q pt

② Voltage divider Bias Arrangement -



$\because I_G = 0\,mA, \quad I_1 = I_2$

$$\boxed{V_G = \frac{R_2 \, V_{DD}}{R_1 + R_2}}$$

Apply KVL to indicated loop

$V_G - V_{GS} - V_{RS} = 0$

$\boxed{V_{GS} = V_G - I_D R_S}$ — ① $\quad (V_{RS} = I_S R_S = I_D R_S)$

For o/p section

$V_{RS} + V_{DS} + V_{RD} - V_{DD} = 0$

$V_{DS} = V_{DD} - V_{RS} + V_{RD}$

$\boxed{V_{DS} = V_{DD} - I_D (R_S + R_D)}$

Since the characteristics are a plot of I_D vs. V_{GS} & eqn ① relates the same two variables, the two curves can be plotted on the same graph & a soln determined at their intersection.

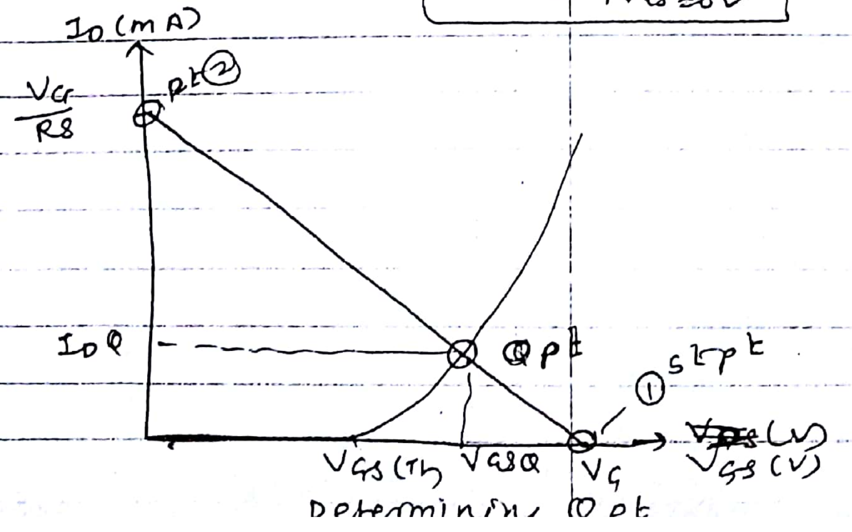
Once I_{DQ} & V_{GSQ} are known, all the remaining quantities of the N/w such as V_{DS}, V_D & V_S can be determined.

& $\boxed{I_{DQ} = k[V_{GS} - V_{GS(Th)}]^2}$

from eqn ①,

pt ① $\quad I_D = 0\,mA, \quad \boxed{V_{GS} = V_G \big|_{I_D = 0\,mA}}$

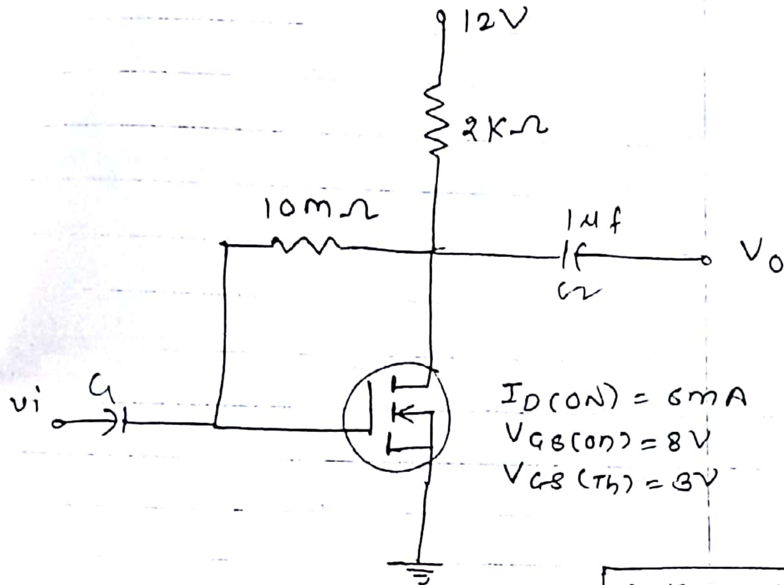
pt ② $\quad V_{GS} = 0 \quad \boxed{I_D = \frac{V_G}{R_S} \Big|_{V_{GS} = 0V}}$



Determining Q pt.

Example ON fb bias EMOSFET

(Ex 1) Determine I_{DQ} & V_{DSQ} for enhancement type MOSFET



$I_{D(ON)} = 6mA$
$V_{GS(on)} = 8V$
$V_{GS(Th)} = 3V$

Mathematical Approach

Soln:- ① $k = \frac{I_{D(on)}}{[V_{GS(on)} - V_{GS(Th)}]^2} = \frac{6\times10^{-3}}{(8-3)^2} = 0.24\times10^{-3}\ A/V^2$

$I_D = k[V_{GS} - V_{GS(Th)}]^2$ — ①

$V_{GS} = V_{DD} - I_D R_D$

$V_{GS} = 12 - I_D R_D$ put in eqn ① & put $V_{GS(Th)} = 3V$ in eqn ①

$I_D = k[12 - I_D R_D - 3]^2$

$= 0.24\times10^{-3}[9 - I_D R_D]^2$

But $R_D = 2K\Omega = 2000\Omega$

$\therefore I_D = 0.24\times10^{-3}[9 - 2000 I_D]^2$

$= 0.24\times10^{-3}[81 - 36\times10^{3} I_D + (4\times10^{6} I_D^2)]$

$I_D = 0.01944 - 8.64\times I_D + 960 I_D^2$

$\therefore \boxed{960 I_D^2 - 9.64 I_D + 0.01944 = 0}$

$I_D = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} = \frac{9.64 \pm \sqrt{(-9.64)^2 - (4\times960\times0.01944)}}{2\times960}$

$\boxed{I_D = 7.24mA \quad \text{or} \quad 2.79mA}$

$V_{DS} = V_{DD} - I_D R_D$

let $I_D = 7.24mA$ $\quad V_{DS} = 12 - (7.24\times2) = -2.48V$

But V_{DS} cannot be −ve hence $I_D \neq 7.24mA$

$\therefore \boxed{I_{DQ} = 2.79mA}$

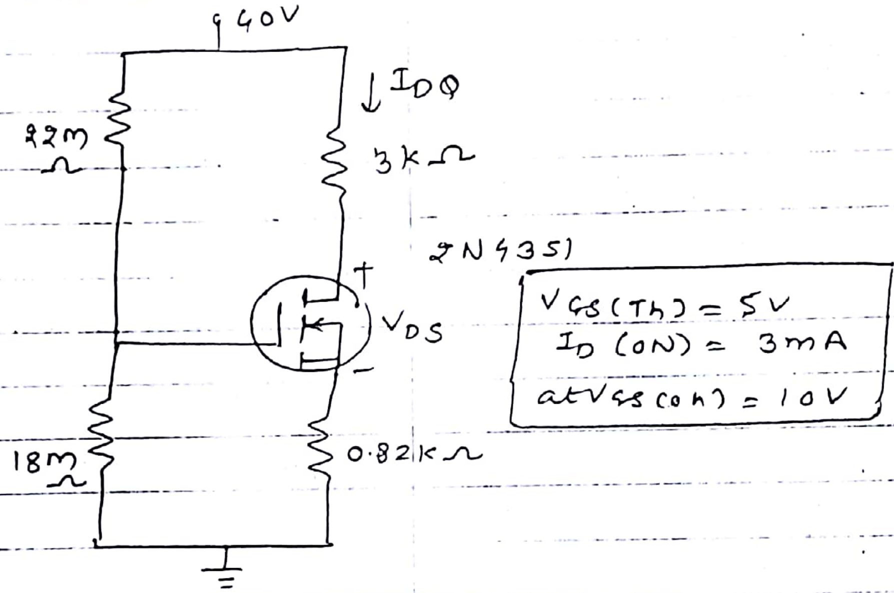
② $V_{DSQ} = V_{DD} - I_{DQ}R_D$

$= 12 - (2.79 \times 2)$

$\boxed{V_{DSQ} = 6.42V}$

$\boxed{\text{for Graphical Approach}}$ - refer Boylested (pg 536)

Ex 2. Determine I_{DQ}, V_{GSQ} & V_{DS} for N/W shown. Eg on V.D EMOS



$\boxed{\text{Mathematical Approach}}$

① $k = \dfrac{I_{D(on)}}{[V_{GS(on)} - V_{GS(Th)}]^2} = \dfrac{3 \times 10^{-3}}{[10-5]^2} = 1.2 \times 10^{-4}$ A/

② $I_{DQ} \Rightarrow$

$I_D = k[V_{GS} - V_{GS(Th)}]^2$

$= 1.2 \times 10^{-4} A/V^2 [V_{GS} - 5]^2$ — ①

$V_G = V_{GS} + V_{RS} = V_{GS} + I_D R_S$

$V_{GS} = V_G - I_D R_S$

$V_{GS} = \dfrac{R_2 . V_{DD}}{R_1 + R_2} - I_D R_S = \dfrac{18 \times 40}{(18+22)} - (820 I_D)$

$V_{GS} = 18 - 820 I_D$ — put in eqⁿ ①

$I_D = 1.2 \times 10^{-4}[18 - 820 I_D - 5]^2$

$= 1.2 \times 10^{-4} [13 - 820 I_D]^2$

$= 1.2 \times 10^{-4} [169 - 21.32 \times 10^3 I_D + 672.4 I_D^2]$

$I_D = 0.02028 - 2.56 I_D + 80.68 I_D^2$

$$\boxed{80.68 I_D^2 - 3.56 I_D + 0.02028 = 0}$$

$$I_D = \frac{3.56 \pm \sqrt{(-3.56)^2 - (4 \times 80.68 \times 0.02028)}}{2 \times 80.68}$$

$$\boxed{I_D = 6.69\,mA \quad or \quad I_D = 37.4\,mA}$$

$I_D = 37.4\,mA \Rightarrow V_{DS} = V_{DD} - I_D(R_S + R_D)$

$= 40 - 37.4\,(0.82 + 3)$

$V_{DS} = -102.87\,V$

$-ve$ V_{DS} is practically not acceptable $\therefore I_D \neq 37.4\,mA$

$\therefore \boxed{I_{DQ} = 6.69\,mA}$

$V_G - I_D R_S$

$V_{GSQ} = 18 - 820 \times 6.69\,mA$

$\boxed{V_{GSQ} = 12.51\,V}$

$V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_S)$

$= 40 - 6.69\,(3 + 0.820)$

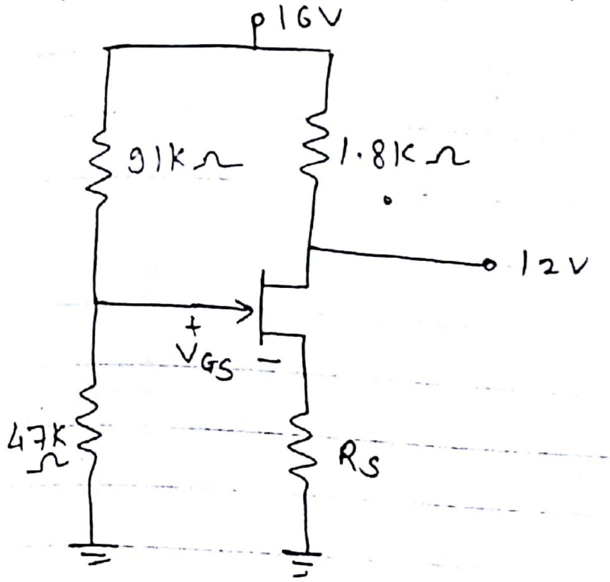
$\boxed{V_{DSQ} = 14.44\,V}$

* **Design** -

It is good design practice for linear amplifiers to choose operating points that do not crowd the saturation level (I_{DSS}) or cut off (V_P) regions.

- Levels of V_{GSQ} close to ($V_P/2$) or levels of I_{DQ} near ($I_{DSS}/2$) are certainly responsible starting points in the design.
- In every design procedure, the maximum levels of I_D & V_{DS} as appearing on the specification sheet must not be exceeded.
- The specific levels of N/W are provided & N/W parameters such as R_D, R_S, V_{DD} & so on must be determined.

Ex 2.) For the voltage divider bias configuration of given fig. if $V_D = 12V$ & $V_{GSQ} = -2V$. Determine value of R_S.



Soln:-

$$V_G = \frac{R_2 . V_{DD}}{R_1 + R_2} = \frac{47k \times 16V}{(47+91k)}$$

$$\boxed{V_G = 5.44V}$$

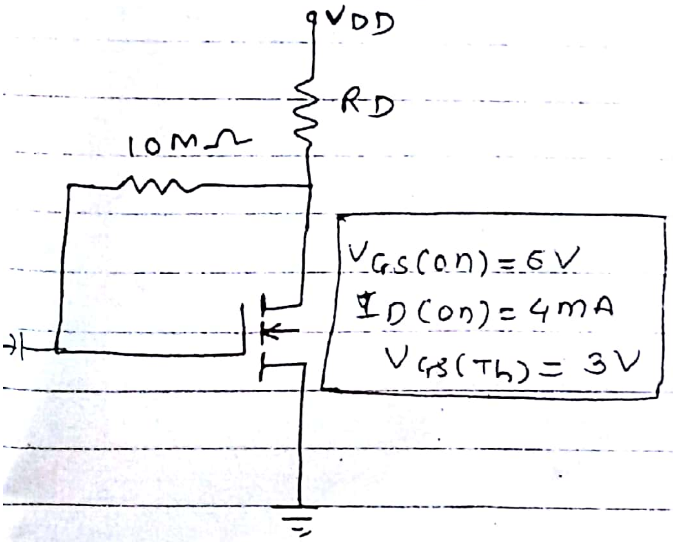
$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{16V - 12V}{1.8k\Omega} = 2.22 \, mA$$

$$V_{GS} = V_G - I_D R_S$$

$$-2V = 5.44V - (2.22mA \times R_S)$$

$$R_S = \frac{7.44V}{2.22mA} = 3.35k\Omega \qquad \therefore \boxed{R_S = 3.3k\Omega \ (std)}$$

3) The levels of V_{DS} & I_D are specified as $V_{DS} = \frac{1}{2} V_{DD}$ & $I_D = I_{D(on)}$ for the N/W of fig. given determine the level of V_{DD} & R_D



given $I_D = I_{D(on)} = 4mA$

$V_{GS} = V_{GS(on)} = 6V$

$$V_{DS} = V_{GS} = \frac{1}{2} V_{DD}$$

$$6V = \frac{1}{2} V_{DD}$$

$$\boxed{V_{DD} = 12V}$$

$$R_D = \frac{V_{RD}}{I_D} = \frac{V_{DD} - V_{DS}}{I_{D(ON)}}$$

$$= \frac{V_{DD} - \frac{1}{2}V_{DD}}{I_{D(ON)}} = \frac{\frac{1}{2}V_{DD}}{I_{D(ON)}} = \frac{6V}{4mA}$$

$$\boxed{R_D = 1.5k\Omega}$$ — std. value