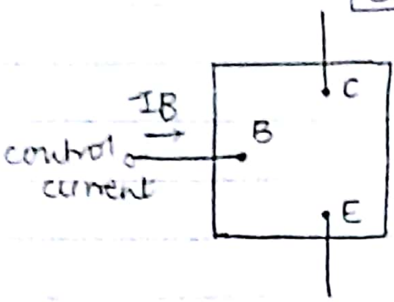
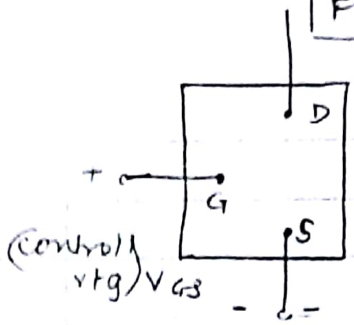
Introduction –

The field effect transistor (FET) is a three-terminal device used for a variety of applications. These applications are very much similar to those of a BJT.

BJT	FET
	
a) current controlled device	b) voltage controlled ampl's
- The current I_C is the direct function of level of I_B.	- I_D current will be a function of voltage V_{GS}.
- Bipolar device - conduction level is a function of two charge carriers electrons & holes.	- Unipolar Device conduction level is function of solely either electrons (n-channel) or hole (p-channel)

Field effect :-

For the FET, an electric field is established by the charges present, which controls the conduction path of the o/p ckt without the need for direct contact betn the controlling & controlled quantities.

Advantages of FET over BJT :-

① FET has high input impedance.
② FETs are more temperature stable than BJTs.
③ FETs are usually smaller than BJTs, making them particularly useful in integrated ckt (IC) chips.

Disadvantage of FET :- It has relatively small gain bandwidth product as compared with that of BJT (conventional)

Scanned by CamScanner

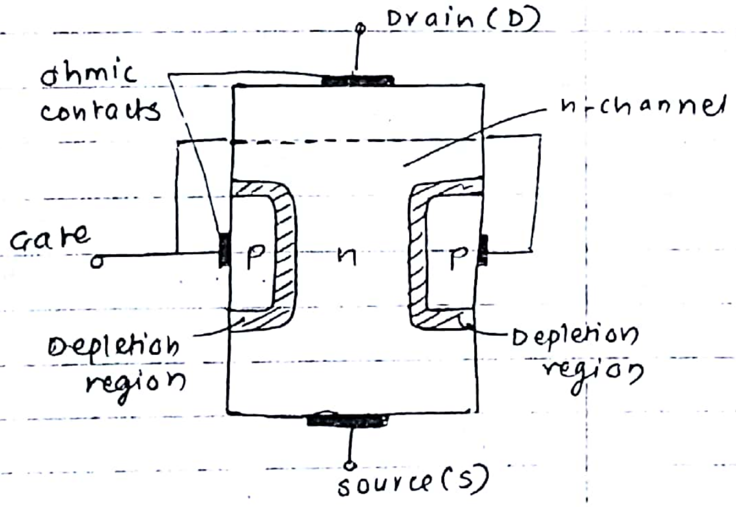
classification of FET :-

- Field Effect Transistor (FETs)
  - JFET
    - n-channel JFET
    - p-channel JFET
  - MOSFET
    - Depletion MOSFET
    - Enhancement MOSFET

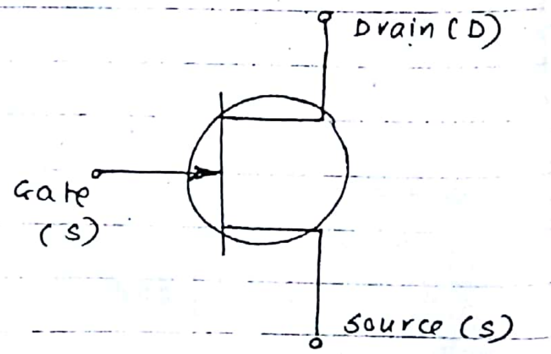
* Construction of JFET :-

n-channel JFET :-

- The major part of the structure is the n-type bar material & ohmic contacts are made to the two ends of bar. These are the terminals named Drain (D) & source (S)
- On both sides of n-type bar, the heavily doped (p^+) regions have been formed by allowing or by diffusion to create a p-n junction. Both these p^+ regions are connected together & via an ohmic contact the gate terminal is brought out.



structure of n channel JFET



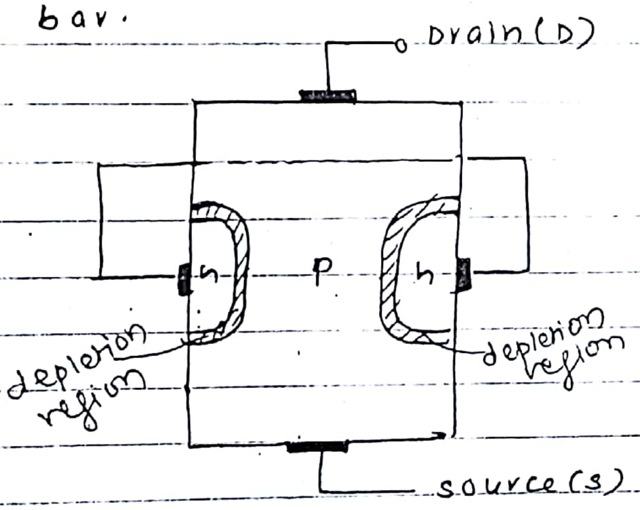
symbol of n-channel JFET

- The supply vtg is connected betn the drain & source terminals of JFET hence current is caused to flow along the length of the n-type bar.
  This current is due to the majority carriers which in this case are electrons.

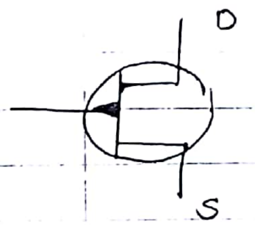
- channel is the n-type material betⁿ two gate regions. The majority carriers (electrons) move through this channel from source to drain. Since the channel is made of n-type material, this FET is called as n-channel FET.
- The channel width reduces with increase in V_{GS}.
- The channel width is constant when a JFET is operated in the saturation region.

* p-channel JFET -

The only difference betⁿ p-channel & n-channel JFET is that a p-type semiconductor bar is being used with two n-type gate regions.
- The p-channel JFET, current flows due to the holes. This is because holes are majority carriers in a p-type semiconductor bar.



Structure of p-channel JFET



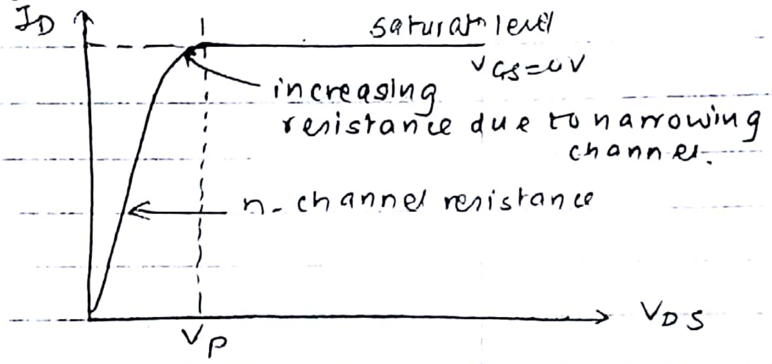
Symbol of p-channel JFET

* Unbiased JFET :-

operation when Gate is open ($V_{GS} = 0V$) -

- A positive supply voltage is (V_{DS}) connected betⁿ drain & source terminals.
- Inside the n-type semiconductor bar, there are a number of electrons available for conduction. Under the influence of V_{DS}; ~~these~~ electrons starts flowing from source to drain.
- This constitute the drain current I_D. These electrons pass through the narrow passage betⁿ two p-type gates. This passage is called as channel.

- In the absence of any applied potential, the JFET has two p-n junctions under no bias condⁿ. This result is a depletion region at each junction.
- As V_{DS} increases & approaches a level as V_P, the depletion region will widen, causing noticeable reduction in channel width.
- The reduced path of conduction causes the resistance to increase & the curve as shown.
- The more horizontal curve, the higher the resistance, approaching infinite ohms in the horizontal region.

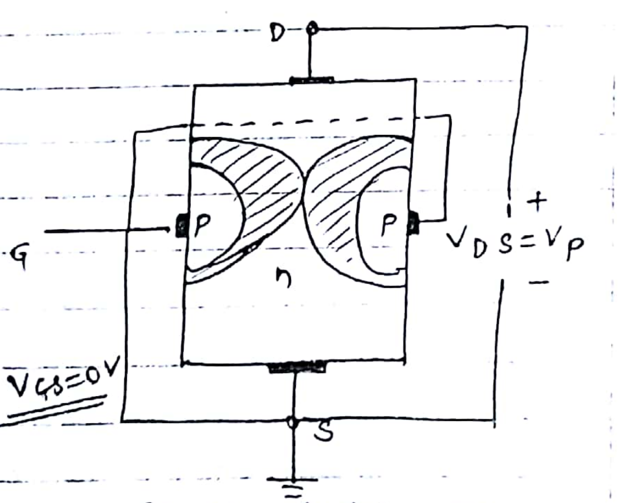


I_D versus V_{DS} for $V_{GS}=0V$

I_{DSS} = drain to source current with a short ckt connection from gate to source.

I_{DSS} is the maximum drain current for a JFET & is defined by the condition $V_{GS}=0V$ & $V_{DS}>|V_P|$

* Pinch-off Condⁿ :-
- If V_{DS} is increased to a level where it appears that the depletion region would touch as shown in fig. a condⁿ referred to as pinch-off



Pinch-off ($V_{GS}=0V$, $V_{DS}=V_P$)

The level of V_{DS} that establishes this condⁿ is referred to as the pinch-off voltage (V_P)

The pinch-off suggests the current I_D is pinched off & drops to 0A.

I_D maintains a saturation level I_{DSS}

Biased JFET (operation of n-channel JFET) :-

The operation of JFET is explained for different values of V_{GS} as follows :-

① $\boxed{V_{GS} = 0}$ -

same as previously explained (for No bias)

② $\boxed{V_{GS} < 0V}$ - (small -ve V_{GS})

Due to reverse voltage applied across the gate source junction, the penetration of depletion region into the n-type material increases further.
This will reduce the channel width. Due to reduced channel width, less number of electrons can pass through to drain from source. Therefore drain current I_D reduces with increases in V_{GS}.

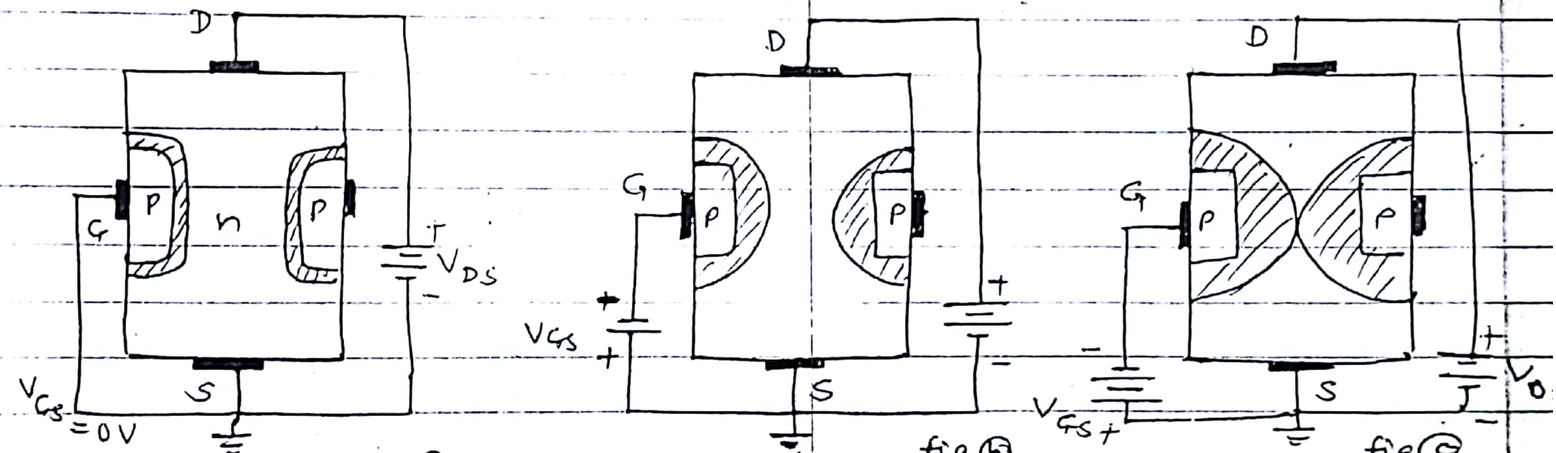


fig ⓐ When $\boxed{V_{GS} = 0}$

fig ⓑ $V_{GS} < 0$ (small -ve vtg)

fig ⓒ $V_{GS} << 0$ (large -ve vtg)

③ $\boxed{V_{GS} << 0V}$ (large value -ve V_{GS})

As the -ve V_{GS} is further increased, the depletion region spread more inside the n-type bar.
- A certain value of -ve V_{GS}, the depletion region touch each other as shown in fig ⓒ
- The channel width is therefore zero & $I_D = 0$. This gate to source vtg at which I_D is cut off is called $V_{GS(off)}$
- Thus with increase in -ve V_{GS}, the channel becomes more & more narrow & I_D reduces.

Thus, for $V_{GS}=0$, the maximum drain current I_{DSS} will flow through JFET. The drain current then reduces with increase in -ve V_{GS}. Hence JFET is a voltage controlled device.

* cut off voltage ($V_{GS(off)}$) :-

The value of V_{GS} that makes the drain current I_D approximately equal to zero is called as cut off vtg ($V_{GS(off)}$)

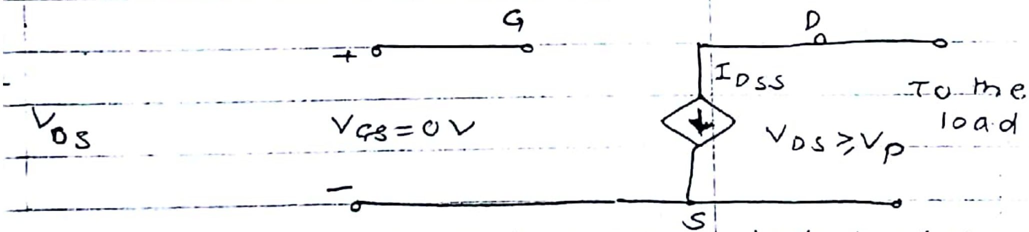
A JFET must be operated betn $V_{GS}=0$ & $V_{GS(off)}$. For this range I_D will change betn I_{DSS} & 0 resp.

④ $\boxed{V_{DS}=V_P}$ — pinch off condn (from previous page)

⑤ $\boxed{V_{DS}\geq V_P}$:-

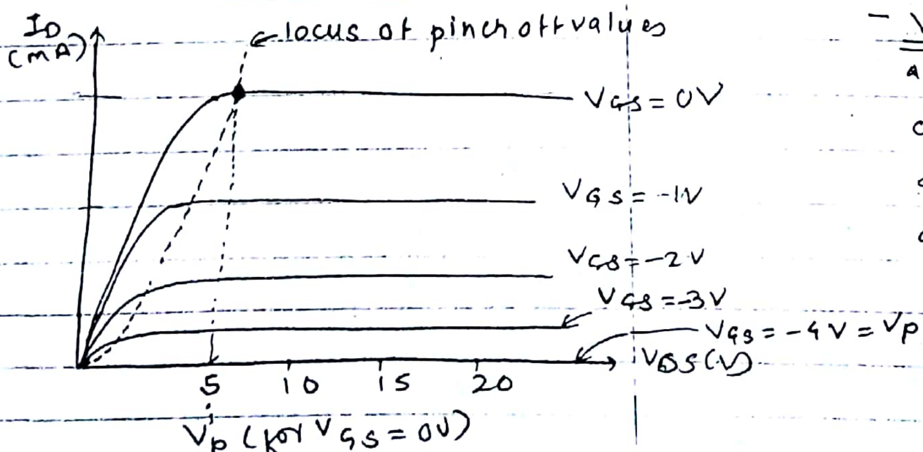
As V_{DS} is increased beyond V_P, the channel narrows down along the length of the depletion region, towards the source.

- But I_D remains constant. Hence for $V_{DS}\geq V_P$, the drain current essentially remains constant.
- Hence for $V_{DS}\geq V_P$, the JFET acts as a constant current source, producing a drain current $I_D = I_{DSS}$ (for $V_{GS}=0V$) as shown in fig.



current source equivalent of JFET for $V_{GS}=0V$, $V_{DS}\geq V_P$

* comparision of pinch off & cut off :-



- V_P is the value of V_{DS} at which the drain current becomes constant & is always measured at $V_{GS}=0V$
- pinch off occurs for V_{DS} values less than V_P when there is change in V_{GS}.

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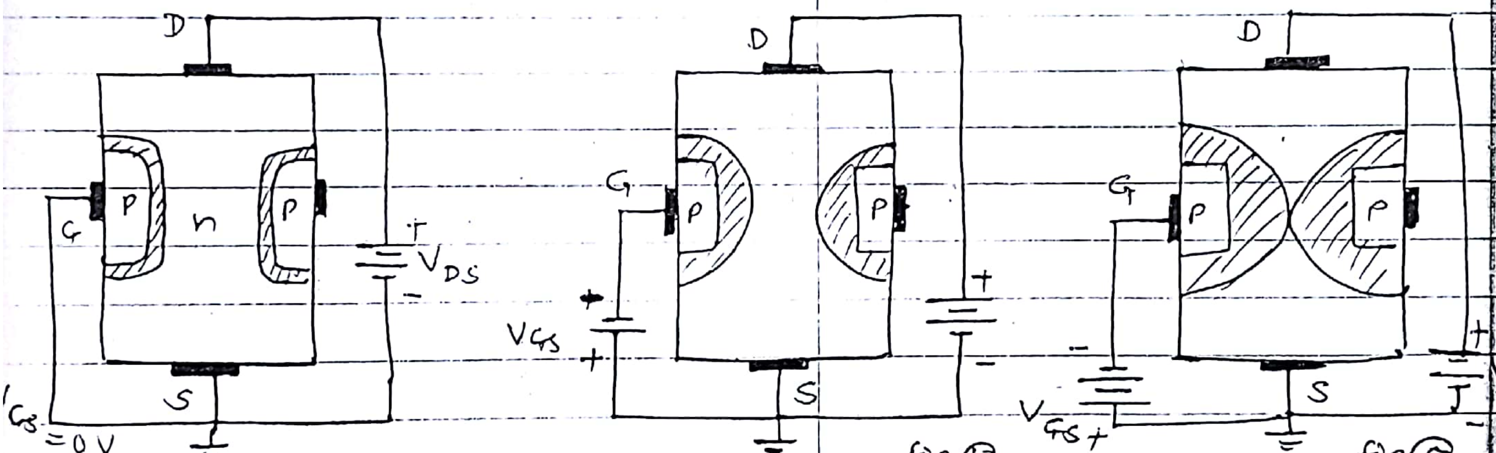

When $V_{GS} = 0$ fig ⓐ

fig ⓑ $V_{GS} < 0$ (small -ve vtg)

fig ⓒ $V_{GS} << 0$ (large -ve vtg)

③ $V_{GS} << 0V$ (large value -ve V_{GS})

As the -ve V_{GS} is further increased, the depletion region spread more inside the n-type bar.

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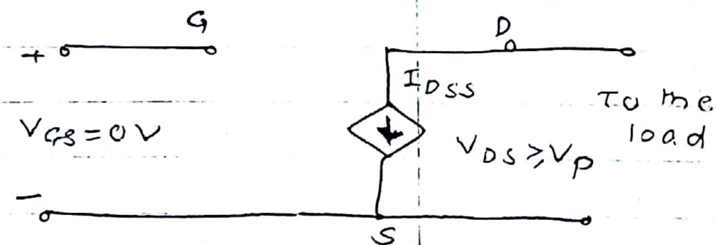

current source equivalent of JFET for $V_{GS}=0V$, $V_{DS}\geq V_P$

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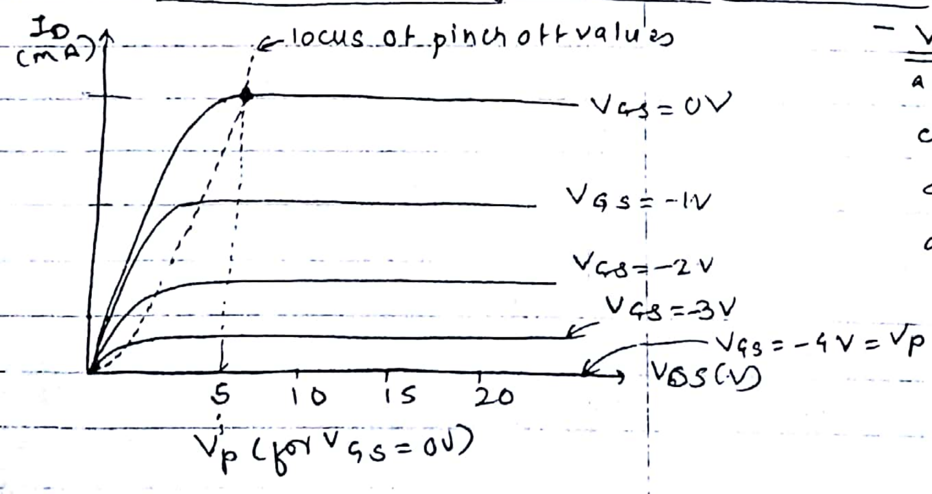
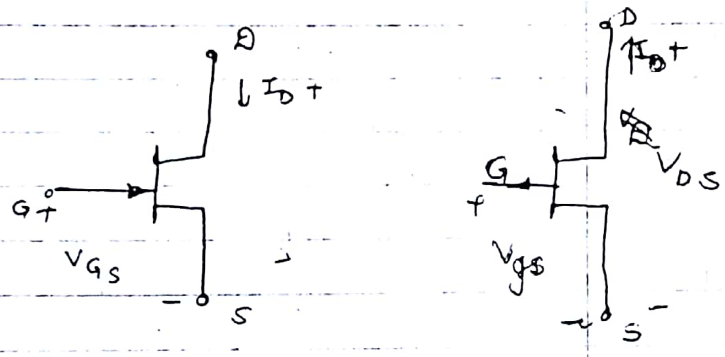


- V_P is the value of V_{DS} at which the drain current becomes constant & is always measured at $V_{GS}=0V$
- pinch off occurs for V_{DS} values less than V_P when there is change in V_{GS}.

$V_p \Rightarrow V_p = V_{DS}$ at $V_{GS} = 0$, $I_D = I_{DSS}$ = constant

$V_{GS(off)} \Rightarrow V_{GS(off)} = V_{GS}$ at $I_D = 0$ mA, $V_{GS} = -V_p$ (for n-channel)
$V_{GS} = +V_p$ (for p-channel)

- so eventhough V_p is constant, the maximum value of V_{DS} at which I_D becomes constant varies with V_{GS}.
- V_p is -ve for n-channel devices & +ve for p channel device.
- At $V_{GS} = V_p = V_{GS(off)}$, the saturation level reduces to 0 mA. That means I_D will remain constant at 0 mA.
- Thus the device will turn off when $V_{GS} = V_p = V_{GS(off)}$.
- $V_{GS(off)}$ is the value of V_{GS} at which the JFET is turned off & I_D reduces to zero.



n-channel   p-channel

* JFET characteristics :-

① Drain characteristics
② Transfer characteristics.

① Drain characteristics :-

It is a plot of drain current I_D versus drain to source vtg V_{DS} at different values of gate to source vtg V_{GS}.

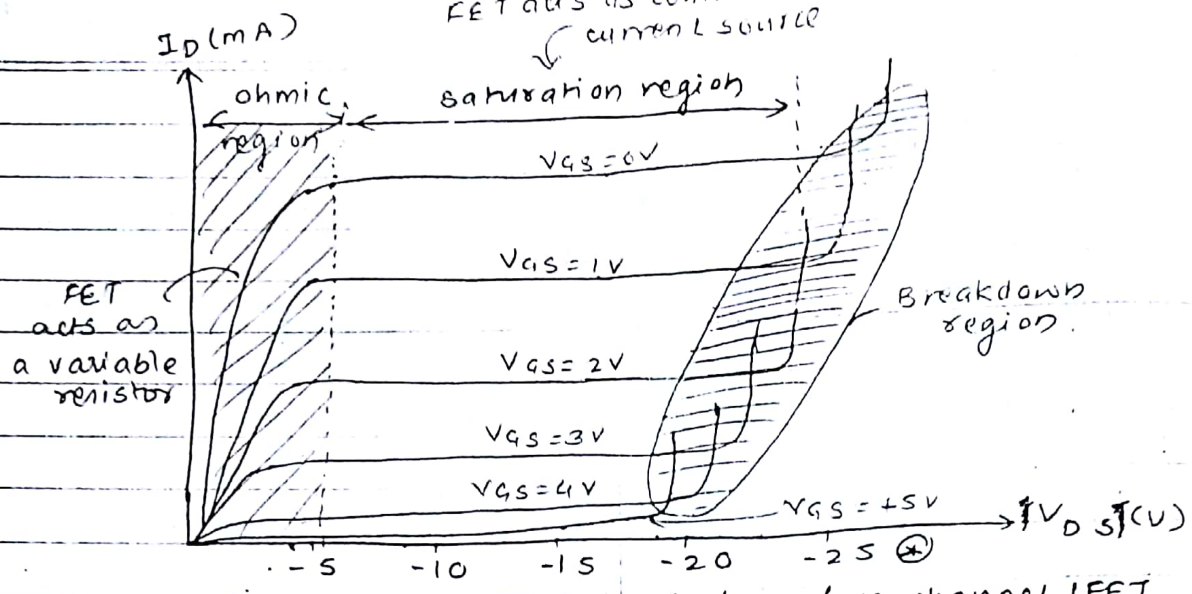
- It is divided into 3 regions

(i) cut off region (ii) Saturation region (iii) ohmic Region

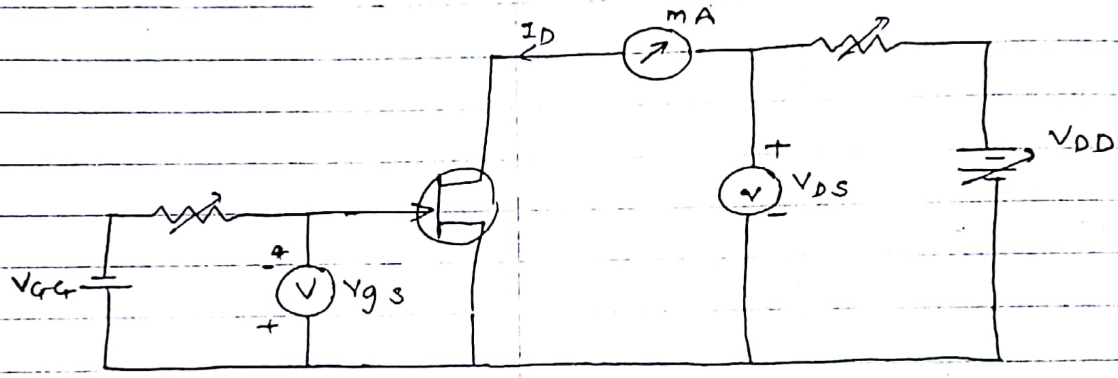
(i) cut off region :-

With increase in -ve V_{GS} vtg, the channel width available for conduction decreases. At certain vtg called '$V_{GS(off)}$' the depletion regions touch each other close to the channel completely. Thus cut off region corresponds to $I_D = 0$ & $V_{GS} > V_{GS(off)}$.

(*) –ve values of V_{DS} on the x axis indicates source is at high potential than drain.



Drain characteristics of n-channel JFET



② Saturation Region :-

It is the region of characteristics where I_D remains fairly constant & does not change with change in V_{DS}.

This 'saturation' is entirely different than 'saturation' in a transistor. In order to use JFET as an amplifier, it is operated in its saturation region.

③ Ohmic region :-

It is the region of characteristics where I_D varies with variation in V_{DS}.

- JFET is said to be operated as a voltage variable resistor in the ohmic region. The resistance offered by JFET decreases with decrease in –ve V_{GS}.
- FET resistance in ohmic region is

$$R_{DS} = \frac{V_P}{I_{DSS}}$$

V_P = pinch off vtg

I_{DSS} = max. drain current

expression for ON resistance ($r_{d(ON)}$) :-

In the ohmic region, the JFET behaves like a variable resistance whose value is decided by V_{GS}.

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$

r_d = ON drain resistance.
r_o = resist with $V_{GS} = 0V$
r_d = resist at particular value of V_{GS}.

④ **Breakdown Region :-**

When a JFET is operating in saturation region, I_D does not change with change in V_{DS} upto a certain level of V_{DS}.

- If V_{DS} is increased further beyond this value, the gate channel junction breaks down due to avalanche effect & the drain current shoots up suddenly as shown in fig.
- This can damage the device. The value of breakdown vtg does not remain constant. It decreases with increase in -ve V_{GS}.
- The operation in the breakdown region should be avoided in order to protect the JFET against damage. This region can be avoided if the level of $V_{DS max}$ is noted on the specification sheet. ⊛

⑤ **Effect of -ve V_{GS} -**

With increase in -ve V_{GS}, the channel width decreases & I_D reduces proportionally, with increase in -ve V_{GS}, the breakdown will take place at the lower values of V_{DS}.

⑥ **Pinch off Vtg :-**

It is the value of V_{DS}, at which drain current reaches its constant saturation value.

- Any further increase in V_{DS} does not have any effect on value of I_D.

⊛ And the design is such that actual level of V_{DS} is less than $V_{DS max}$ for all values of V_{GS}.

② **Transfer characteristics :-**

It is the plot of o/p current I_D Vs the input controlling quantity which is V_{GS} in this case.

Derivation :-

For BJT, o/p current I_C & i/p controlling current I_B are related by beta. ie

$$\boxed{I_C = \beta I_B} \qquad \beta = \text{constant.}$$

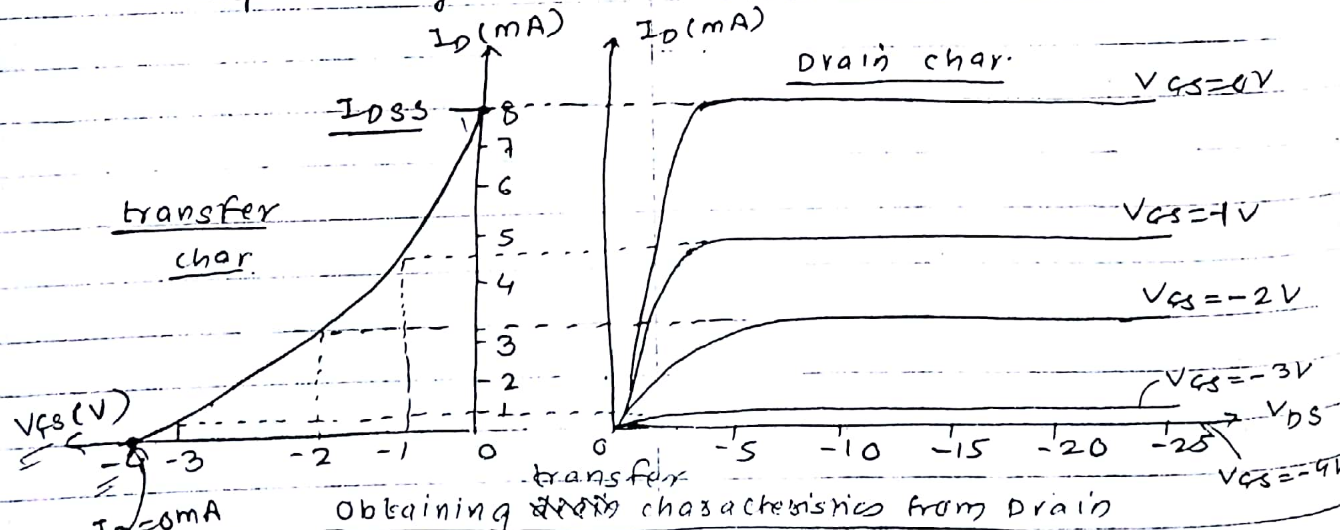
Therefore transfer characteristics of transistor is a straight line indicating a linear relation betn I_C & I_B.

In JFET, relation betn I_D & V_{DS} is not linear. The relationship betn I_D & V_{GS} is defined by Shockley's Equation.

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

where I_{DSS} = Max. drain current } constant
V_P = pinch-off vtg

The relationship betn I_D & V_{GS} is therefore a squared relationship, which produces a curve which is growing exponentially as shown.



Obtaining transfer characteristics from Drain characteristics

- When $V_{GS} = 0$, $I_D = I_{DSS}$ & $V_{GS} = V_P = -4$, $I_D = 0$.

These are the two extreme pts on the characteristics. Transfer characteristics grows exponentially with reduction in −ve V_{GS}.

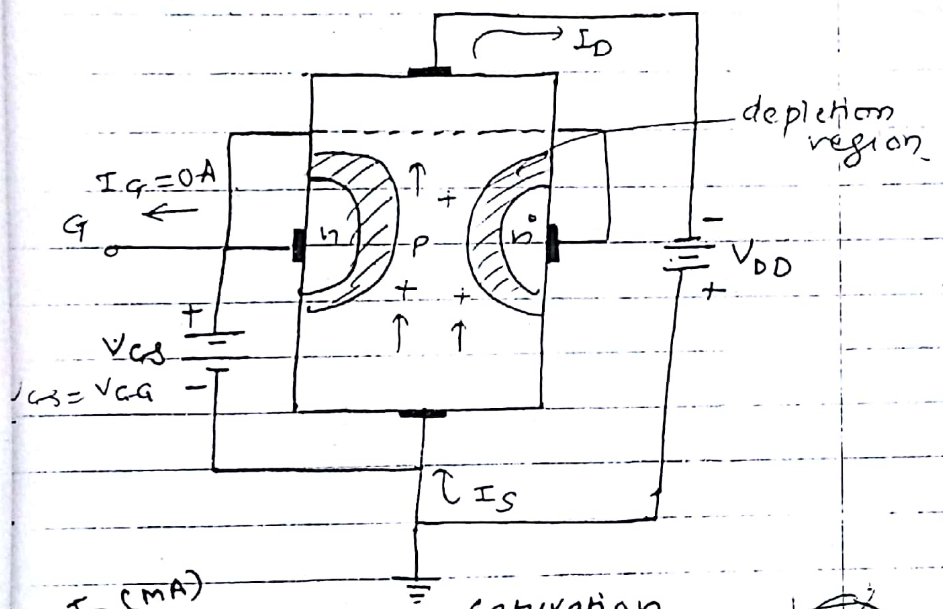
* p-channel JFET, operation -

The construction of p-channel JFET is very similar to that of an n-channel JFET.

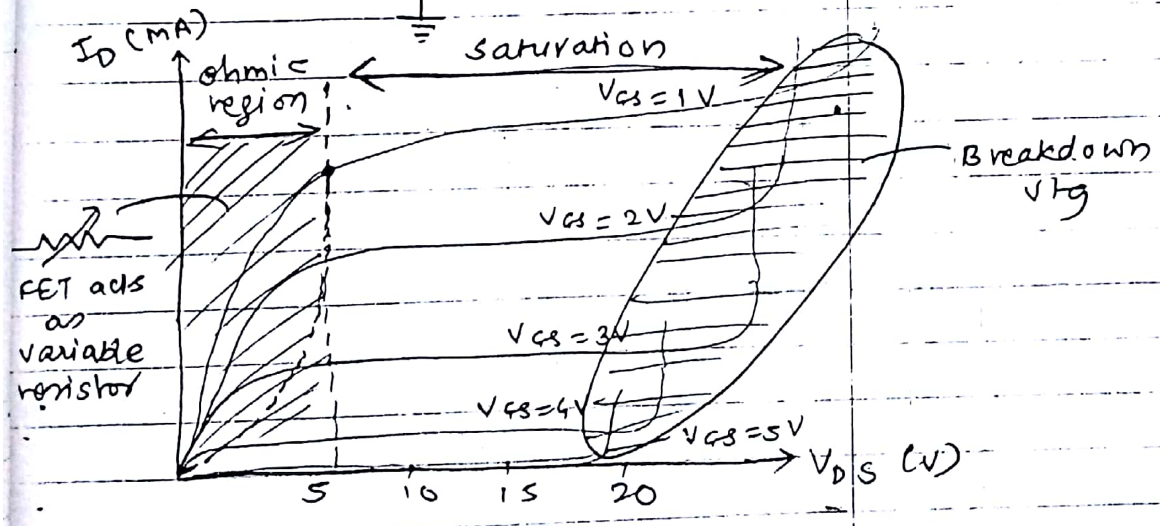
- Only change is that the p-type & n-type materials are reversed.

The defined direction of current are reversed as are the actual polarities for the vtgs V_{GS} & V_{DS}.

For the p-channel device, the channel will be constricted by increasing +ve vtg from gate to source.

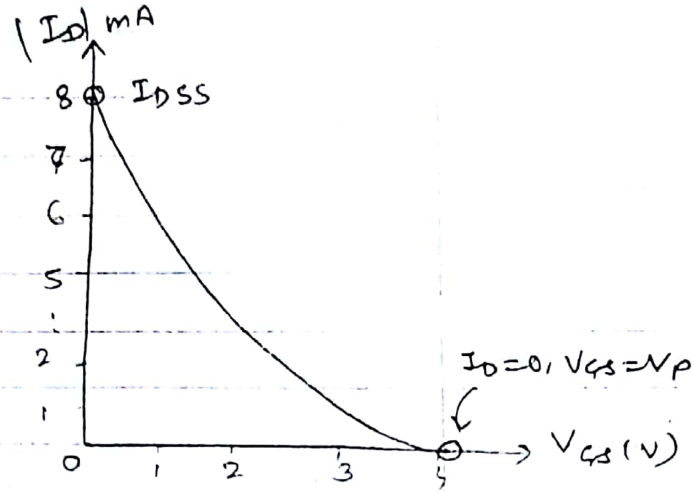


The V_{GS} is +ve & the drain current decreases with increase in V_{GS} due to reduction in the channel width.



Drain characteristics of p-channel JFET

- The shape of drain characteristic is same as that for the n-channel JFET except for the reversal of polarities of V_{DS} & V_{GS}.



Transfer characteristics of p-channel JFET

* Specifications of FET from Data sheets :-

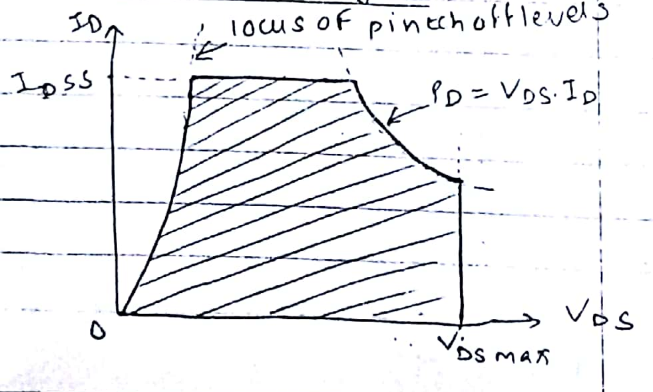
Maximum Ratings :-

Maximum rating list usually appears at the beginning of the specification sheet.

- These include maximum voltage, maximum current levels & maximum power dissipation level of the device eg V_{DSmax} or V_{DGmax}.
- These vtg levels should never be exceeded.
- The term reverse in V_{GSR} defines the maximum vtgs with source positive with respect to the gate before breakdown will occur. It is referred to as BV_{DSS} – the breakdown vtg with drain source shorted ($V_{DS}=0V$) – on some specification sheets.
- Normally $I_G = 0mA$, it forced to accept a gate current, it could withstand 10mA before damage would occur.
- The maximum power the device can dissipate under normal operating cond^ns is defined by

$$\boxed{P_D = V_{DS} \cdot I_D}$$

* Operating Region :-



The specification sheet & the curve defined by the pinch-off levels at each level of V_{GS} define the region of operation for linear amplification on the drain characteristics as shown in fig.

- The ohmic region defines the maximum permissible values of V_{DS} at each level of V_{GS} and $V_{DS\,max}$ specifies the maximum value for this parameter.
- The saturation current I_{DSS} is the maximum drain current & the Maximum power dissipation level defines the curve drawn in the same manner as described for BJT transistors.
- The resulting shaded region is the normal operating region for amplifier design.

Electrical characteristics :-

The electrical characteristics include the values of V_P & I_{DSS}. In case of JFET, $V_P = V_{GS(off)}$.

Maximum Ratings :-

Rating	Symbol	Values	Unit
Drain-source voltage	V_{DS}	25	V_{dc}
Drain-Gate voltage	V_{DG}	25	Vdc
Reverse gate source vtg	V_{GSR}	-25	Vdc
Gate current	I_G	10	mAdc
Total device dissipatn @ $T_A = 25°C$	P_D	310	mW
derate above 25°C		2.82	mW/°C
Junctn Temp range	T_J	125	°C

* **Parameters of JFET** :-

The important parameters of JFET are as follows :-

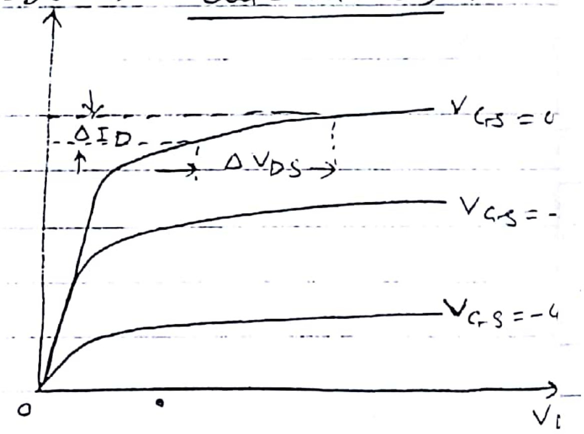
1. Dynamic Drain resistance (r_d)
2. Transconductance (g_m)
3. Amplification factor (μ)
4. Input resistance
5. Input capacitance.

① Dynamic Drain Resistance (r_d) :-

- It is an AC resistance of JFET. It is defined as the ratio of change in the drain to source vtg to the corresponding change in the drain current at a constant value of gate to source vtg.
- It is calculated in the saturation region of FET o/p characteristics.

Calculation :-

$$\boxed{r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{\text{const } V_{GS}}}$$



- It is the reciprocal of slope of the o/p characteristics for a constant value of V_{GS}.
- Slope of the characteristics is very small, & the value of 'r_d' is very large. r_d = 50kΩ to few hundred kΩ

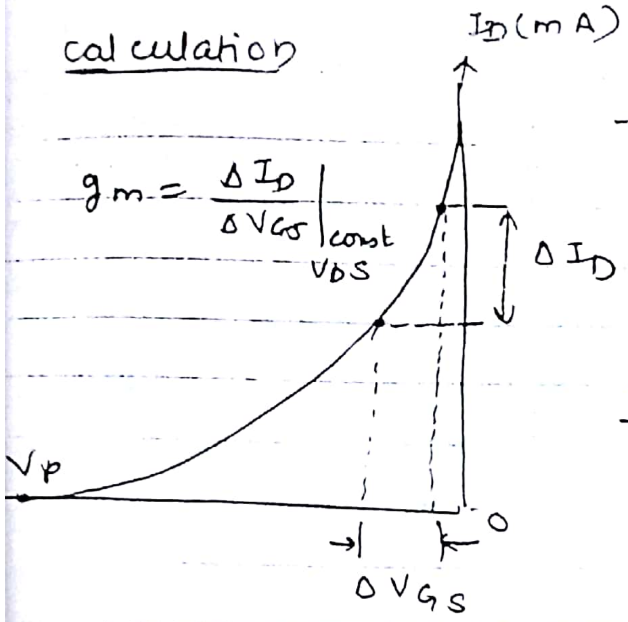
② Transconductance :- (g_m)

It is the ratio of change in drain current to the corresponding change in gate to source vtg at a constant value of drain to source vtg.

$$\boxed{g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{\text{const } V_{DS}}}$$

- g_m can be obtained from the transfer characteristics of JFET.
- It is the slope of transfer characteristics.

calculation



$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{\text{const } V_{DS}}$$

- slope of the transfer characteristics is not constant. It depends on the value of V_{GS}. Therefore g_m has larger values near the top of the transfer characteristics.
- Unit for g_m will be mA/V.

Mathematical expression of g_m :-

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_P}\right] \quad (1)$$ where $g_{mo} = g_m$ at $V_{GS}=0$

we know, $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

$$I_D = I_{DSS}\left[1 - \frac{2V_{GS}}{V_P} + \frac{V_{GS}^2}{V_P^2}\right]$$

differentiating eqn w.r.t. V_{GS}

$$\frac{\partial I_D}{\partial V_{GS}} = \frac{-2 I_{DSS}}{V_P} + \frac{2 I_{DSS} \cdot V_{GS}}{V_P^2}$$

But $\frac{\partial I_D}{\partial V_{GS}} = g_m$

$$\therefore g_m = \frac{-2 I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right] \quad (3)$$

comparing eqn (1) & (3),

$$\boxed{g_{mo} = \frac{-2 I_{DSS}}{V_P}}$$

$$\boxed{g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_P}\right]}$$

③ Amplification Factor (μ) :-

It is defined as the ratio of ch in the drain to source vtg to change in gate to source vtg at a constant I_D.

$$\boxed{\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\bigg|_{I_D \text{ const}}}$$ — unitless

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\boxed{\mu = r_d \times g_m}$$

④ Input Resistance :- (Rin)

JFET operates with reverse biased gate source junction. Therefore its i/p resistance at the gate is very high.

- I/p Resistance is often specified by giving a value of gate reverse current I_{GSS} at a certain V_{GS}.

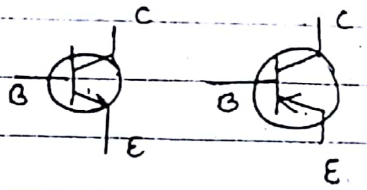
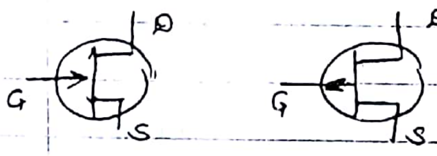
$$\boxed{R_{in} = \frac{V_{GS}}{I_{GSS}}}$$

$R_{in} \propto$ temp

⑤ Input capacitance (Ciss) :-

It is the capacitance of reverse bia gate to source pn juncth.

- The reverse biased pn junction offers a capacitance called junction capacitance or transition capacitance.
- It depends on reverse vtg. It decreases with increase in reverse vtg. (transition capacitance)

BJT	JFET
1) BJT is a current controlled device.	JFET is a voltage controlled device
2) It is a Bipolar device (current flows due to majority & minority carriers)	It is a Unipolar device (current flows due to the majority carriers)
3) Low i/p impedance	High i/p impedance
4) Transfer characteristics is linear	Transfer characteristics is nonlinear
5) Thermal runaway can damage the BJT.	Thermal runaway does not take place
6) BJT has a much higher sensitivity to changes in the applied signal.	JFET is less sensitive to changes in the applied signal.
7)  NPN PNP	 n-channel p-channel
8) AC vtg gain of transistor ampl^r is much higher than that of JFET ampl^r.	AC vtg gain of JFET ampl^r is less than that of BJT ampl^r.
9) Useful regions of operation - saturation & cut off for switching appl^n, active region for amplification.	Useful regions of operation - ohmic & cut off for the switching applications, saturation for amplification
10) Noise generated by BJT is high	Noise generated by JFET is low.
11) BJT is bigger in size than JFET	JFET is smaller in size than BJT.