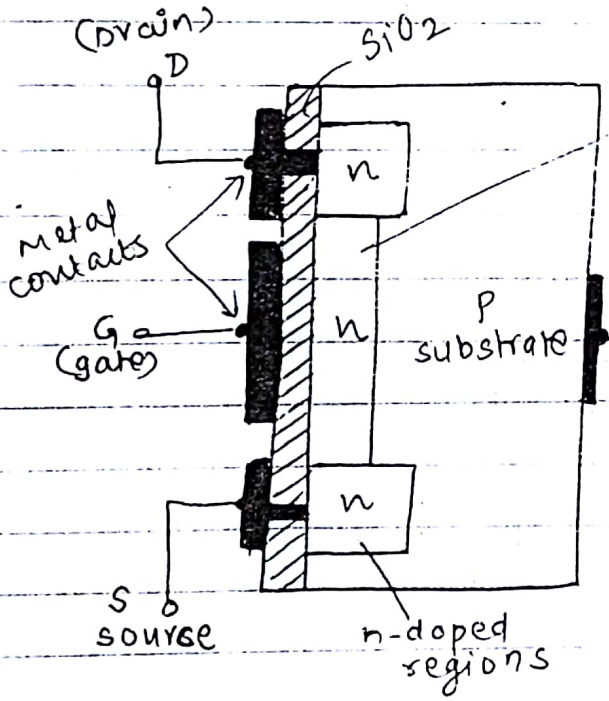
MOSFET :-

- Metal oxide- semiconductor Field Effect Transistor.
  1. Depletion type MOSFET
  2. Enhancement type MOSFET

1. Depletion Type MOSFET :-

Basic construction :-



- A slab of p-type material is formed from a silicon base & is referred to as substrate (s
- It is the foundation on which the device is constructed
- Sometimes, the substrate is internally connected to source terminal.
- Sometimes an additional terminal is taken out & labe as 'SS'.

- The drain & source terminals are connected through metal contacts to n-doped regions linked by n-channel as shown in above fig.
- The gate is also connected to metal contact surface but remains insulated from the n-channel by a very thin silic oxide (SiO2 lay

- SiO_2 is a type of insulator referred to as a dielectric. ('di')
(which sets up opposing electric field within the dielectric when exposed to an externally applied field).
- SiO_2 layer is an insulating layer means that there is no direct electrical connection beth gate terminal & the channel of MOSFET.
- This insulating layer of SiO_2 accounts for the very desirable high i/p impedance of the device.
(i/p resistance of a MOSFET is usually more than that of typical JFET.)
- Because of the very high i/p impedance, the gate current I_G is essentially 0A for dc-biased configurations.

Meaning of MOSFET :-

'Metal' for metallic contacts used for connecting drain, source & gate,
'oxide' for silicon dioxide insulating layer
& 'Semiconductor' for the basic structure on which the n- & p type regions are diffused.

IGFET : Insulated Gate FET (as there is insulating layer beth gate & the channel.)

* n-channel Depletion type MOSFET :-

operation & characteristics :-

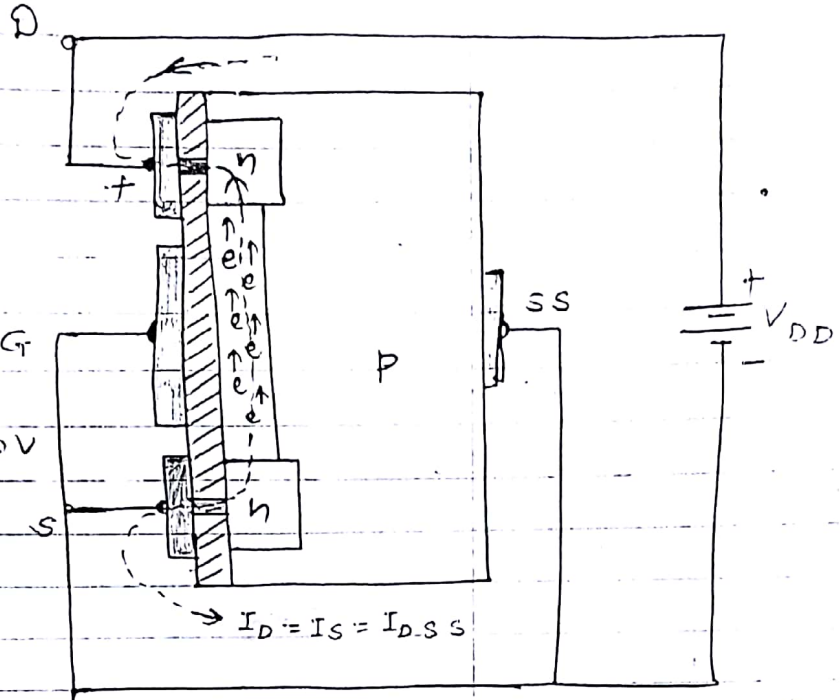


fig ⓐ

n-channel depletion type MOSFET with $V_{GS}=0V$ & applied Vtg V_{DD}

① $V_{GS}=0V$, V_{DS} is applied

When $V_{GS}=0V$ & Vtg V_{DS} is applied across the drain to source terminals. The result is an attraction for the +ve potential at the drain by the free electrons of n-channel & a current similar to that established through the channel of JFET. i.e with $V_{GS}=0V$, $I_D = I_{DSS}$.

② V_{GS} = -ve

The -ve potential at the gate will tend to pressure electrons towards the p type substrate (like charges repel) & attract holes from p type substrate (opposite charges attract) as shown in fig ⓑ

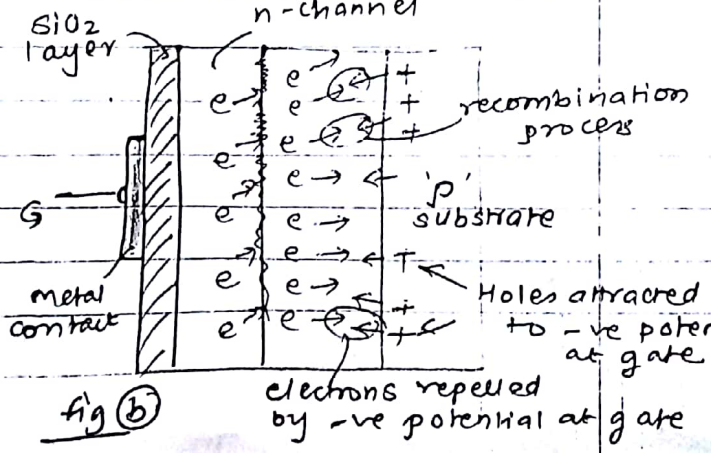
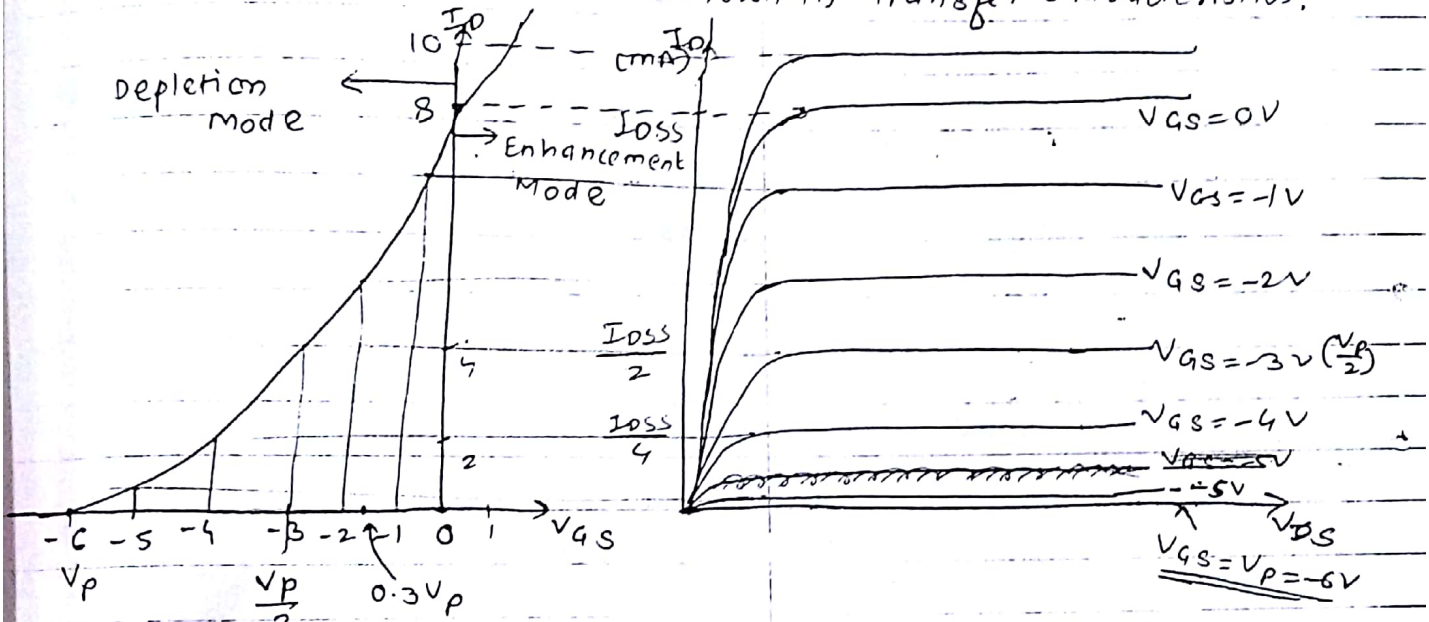


fig ⓑ

- Depending on magnitude of -ve bias established by V_{GS} a level of recombination of both electrons & holes will occur.
- This will reduce the number of free electrons

in the n-channel available for conduction.
- Therefor I_D will decrease with increase in -ve value of V_{GS}. Thus as $-V_{GS}$ increases, I_D decreases for a constant level of V_{DS}.
- The higher the -ve bias, the more recombination & less is the drain current. This is shown in transfer characteristics.



Fig© Drain & Transfer characteristics for n-channel depletion type MOSFET

③ **V_{GS} = +ve**

For +ve values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the p-type substrate due to the reverse leakage current & establish new carriers through the collisions resulting bet accelerating particles.
- As V_{GS} continues to increase in +ve direction, the drain current will increase rapidly (as shown in fig ©).
- Due to the rapid rise, the user must be aware of the maximum drain current rating since it could be exceeded with a +ve V_{GS}.
- The application of +ve V_{GS} has 'enhanced' the level of free carriers in the channel (compared to that encountered with $V_{GS}=0V$). For this reason the region of +ve gate vtg on the drain or transfer characteristics is often referred to as the "enhancement region". With the region bet cut off &

the saturation level of I_{DSS} referred to as "depletion region"

- The transfer characteristics shows that I_D has a nonlinear relation with V_{GS} which is expressed mathematically as

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

* **p-channel Depletion type MOSFET :-** The construction of p-channel depletion type MOSFET is exactly reverse of n-channel MOSFET.

- That is there is now an n-type substrate & p-type channel as shown in fig (d)
- All the voltage polarities & current directions are reversed.
- As V_{GS} also is reversed, the transfer characteristics is the mirror image of the transfer characteristics of n-type depletion MOSFET.

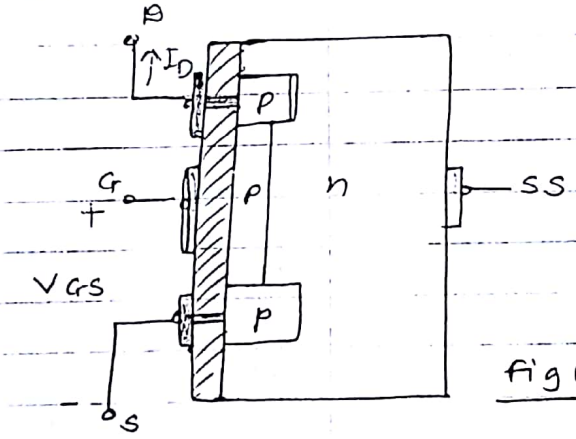
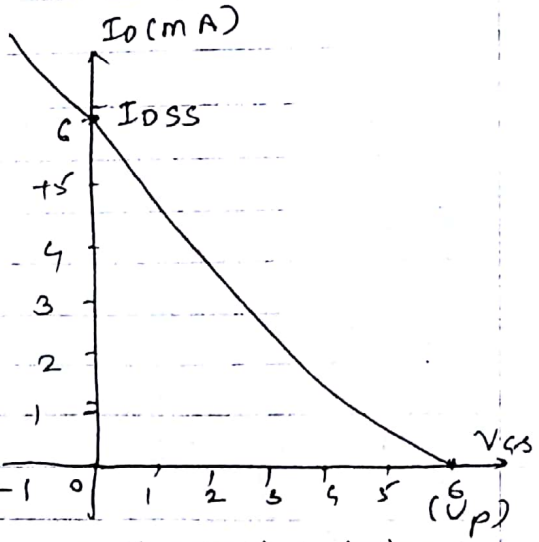
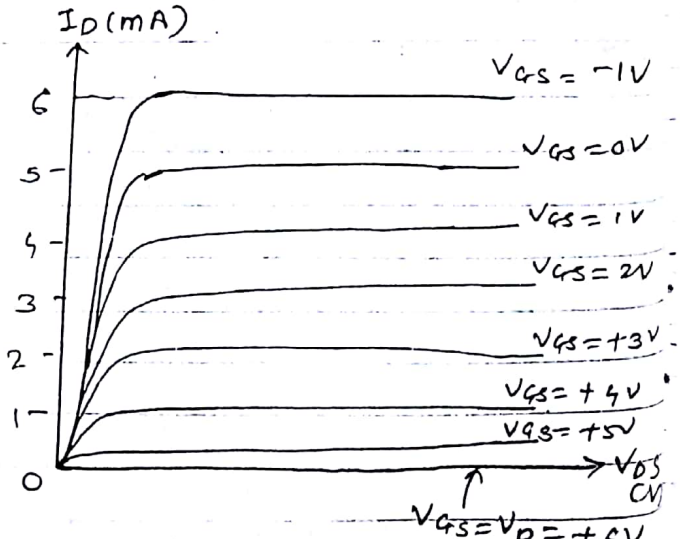


fig (d) construction

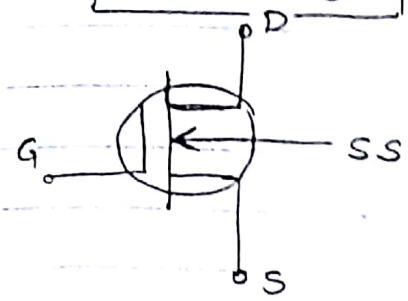




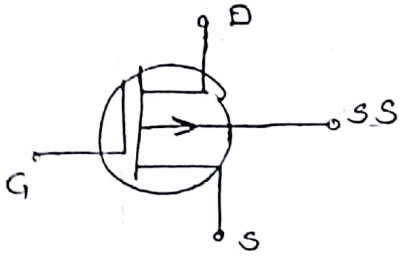
p-channel depletion type MOSFET with $I_{DSS} = 6mA$ & $V_p = 6V$

Symbols :-

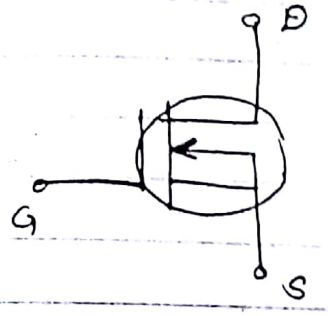
n-channel



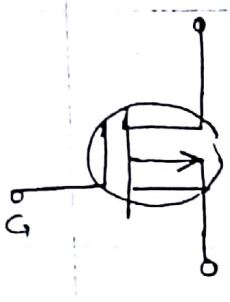
p-channel



n-channel depletion Type



p channel depletion type



n-channel depletion Type

p channel depletion type

* D-MOSFET is called as normally ON MOSFET.

As n-channel D-MOSFET is ON for $V_{GS}=0V$, it turns OFF only when $V_{GS} \leq V_{GS(OFF)}$. is applied.

Hence D-MOSFET is called as normally ON devices.

We have to apply external -ve V_{GS} to turn it OFF.

Without the application

* Enhancement MOSFET :-

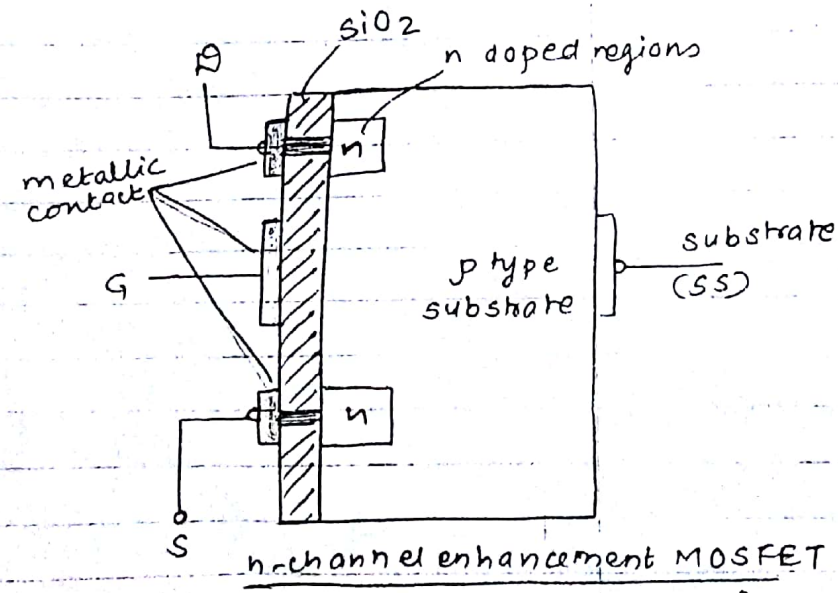
The transfer curve is not defined by Shockley's eqn & the drain current is now cut off until the gate to source voltage reaches a specific magnitude, in case of Enhancement MOSFET.

The current control in an n-channel device is now effected by a positive gate to source Vtg rather than the range of negative Vtg encountered for n-channel JFETs & n-channel depletion type MOSFETs.

n-channel EMOSFET :-

The basic construction of n-channel enhancement type MOSFET is given in fig (a)

- A slab of p-type material is formed from a silicon base & is referred to as substrate. The substrate is sometimes connected to the source (internally), whereas in other cases a fourth lead is made available for external control of its potential level.
- The source & drain terminals are connected through metallic contacts to n-doped regions.
- But a channel bet two n-doped region is absent.
- The SiO_2 layer is present to isolate the gate metalic platform from the region bet D & S, but now it is simply separate from a section of p-type material.



n-channel enhancement MOSFET (NO channel)

The construction of an enhancement type MOSFET is quite similar to the depletion type MOSFET except for the absence of a channel bet D & S terminals.

Operation of n-channel Enhancement MOSFET –

The operation can be explained with two different operating condn.

① $V_{GS} = 0V$ – & V_{DS} +ve

If $V_{GS} = 0V$ & +ve vtg applied both drain & the source of the device, the absence of n-type channel will result in a current of effectively 0A.
(This is quite different from depletion MOSFET & JFET where $I_D = I_{DSS}$ at $V_{GS} = 0$)

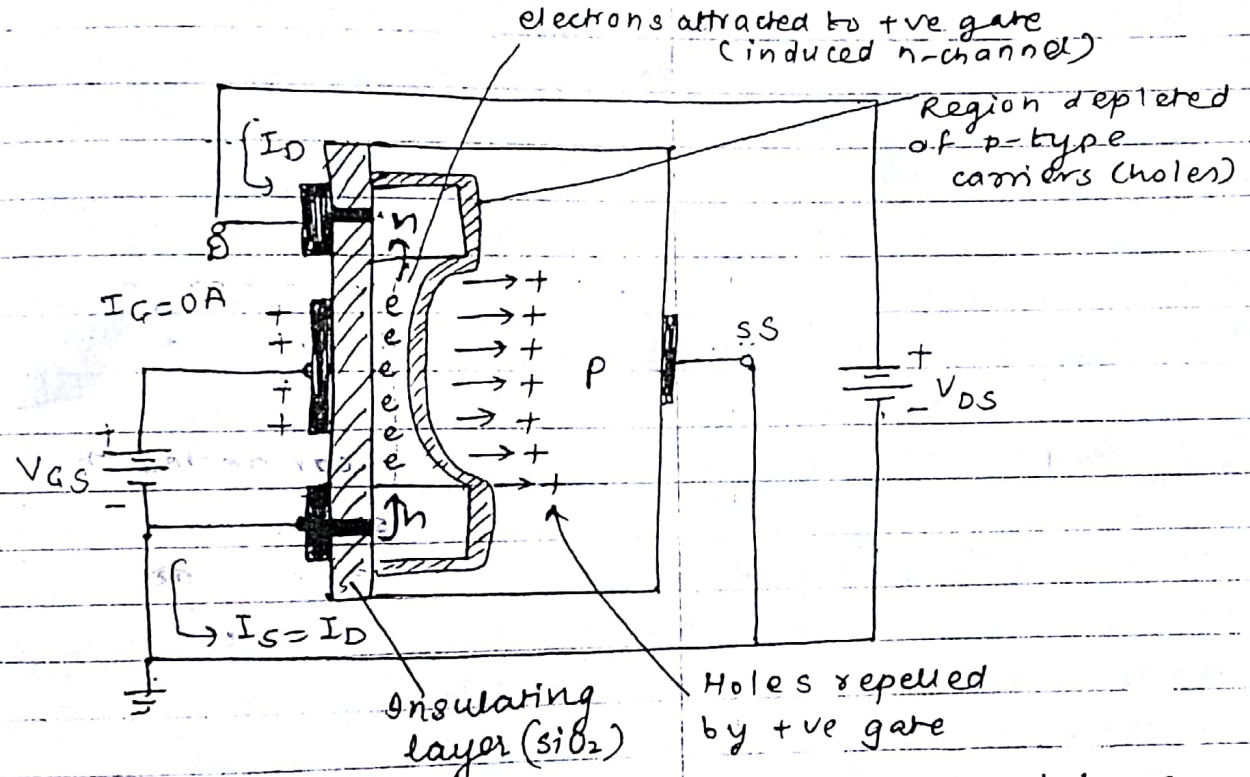


fig ⓑ channel formation in n-channel enhancement type

② V_{GS} is +ve – & V_{DS} +ve

When V_{GS} & V_{DS} are positive (>0) establishing the drain & the gate at a +ve (terminal) potential w.r.t source.

- The +ve potential at the gate will pressure the holes (since like charges repel) in the p substrate along the edge of SiO_2 layer to leave the area & enter deeper regions of the p-substrate as shown in fig ⓑ.
- This result in a formation of depletion region near the SiO_2 insulating layer void of holes.

- And the electrons in the p-substrate (minority carriers of the material) will be attracted to the +ve gate & accumulate in the region near the surface of the SiO_2 layer.
- As V_{GS} is increased, the concentration of electrons near the SiO_2 surface increases until it creates an induced n-channel which connects the n-type doped region.
- The drain current starts flowing through this induced channel. The value of V_{GS} that results in the significant increase in drain current is called 'threshold voltage.' (V_T) or $V_{GS(Th)}$
- Since channel is nonexistent with $V_{GS} = 0V$ & 'enhanced' by the application of +ve V_{GS}, this type of MOSFET is called as Enhancement Type MOSFET.

$V_{GS} > V_T \Rightarrow$

- If V_{GS} is increased beyond the threshold level (V_T), the density of free electrons in the induced channel will increase resulting in increasing level of I_D.

③ V_{GS} = constant V_{DS} = increased :-

due to this, the gate terminal becomes less & less +ve w.r.t drain. So the less number electrons are attracted towards gate terminal & the induced ~~channel~~ channel becomes narrow as shown in fig c).

Eventually, the channel width reduced to a pt of pinch off & the saturation condⁿ will be established, which is same as that in JFET or depletion type MOSFET.

- means, any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D unless breakdown cond. are encountered.

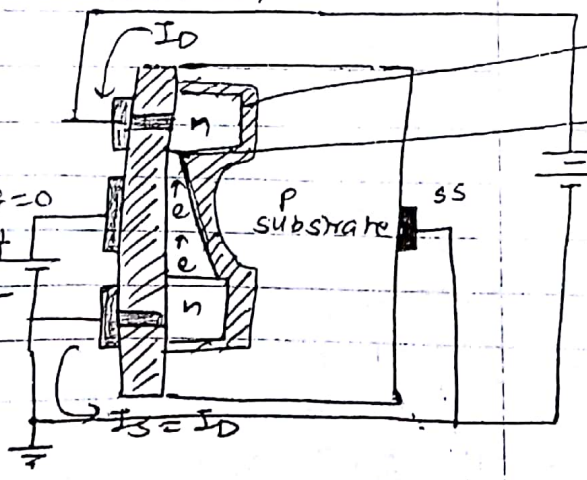


fig c)
effect of change in V_{DS} at fixed V_{GS} on the channel width

* p-channel Enhancement Type MOSFET :-

* construction -

- The construction of a p-channel enhancement type MOSFET is exactly the reverse of n-channel enhancement type MOSFET as shown in fig below.

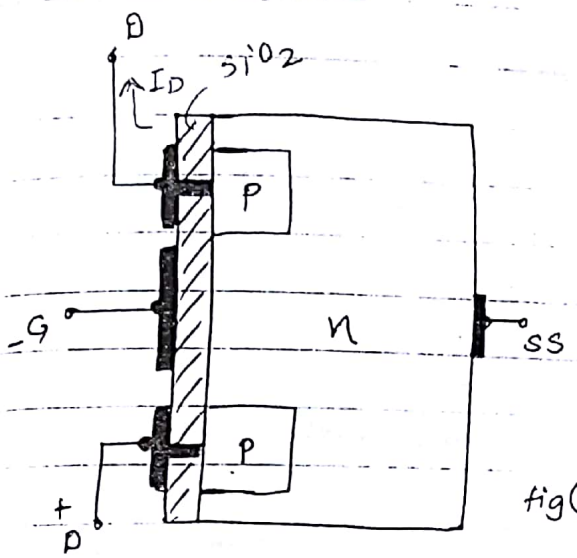


fig ⓐ

- Now, there is an n-type substrate and p-doped regions under the drain & source connections.
- All the voltage polarities & current directions are reversed.

* characteristics -

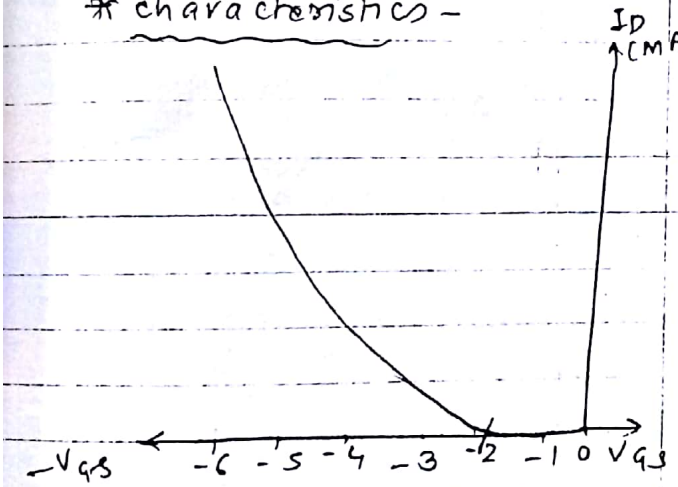


fig ⓑ Transfer characteristics

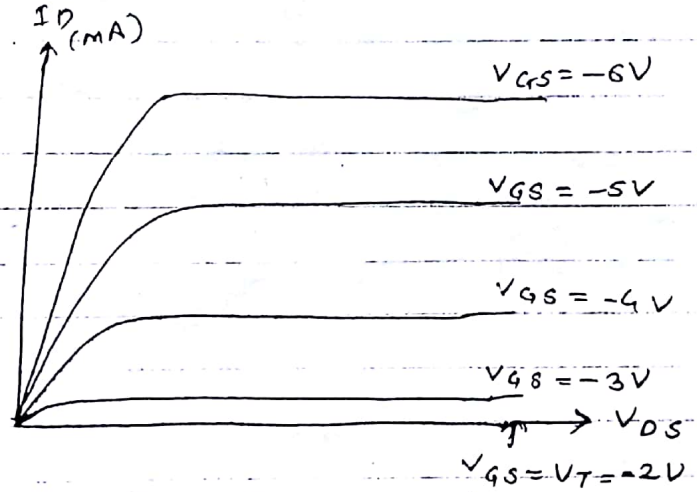


fig ⓒ Drain characteristics

- The drain characteristics will appear as shown in fig ⓒ, with increasing levels of current resulting from increasingly -ve values of V_{GS}.
- The transfer characteristics will be the mirror image (abt I_D axis) of the transfer curve of n-channel enhancement MOSFET, with I_D increasing with increasingly -ve values of V_{GS} beyond V_T.

Characteristics of n-channel Enhancement Type MOSFET :-

- The drain characteristics & transfer characteristics of n-channel enhancement MOSFET is shown in fig © & ⓓ resp.

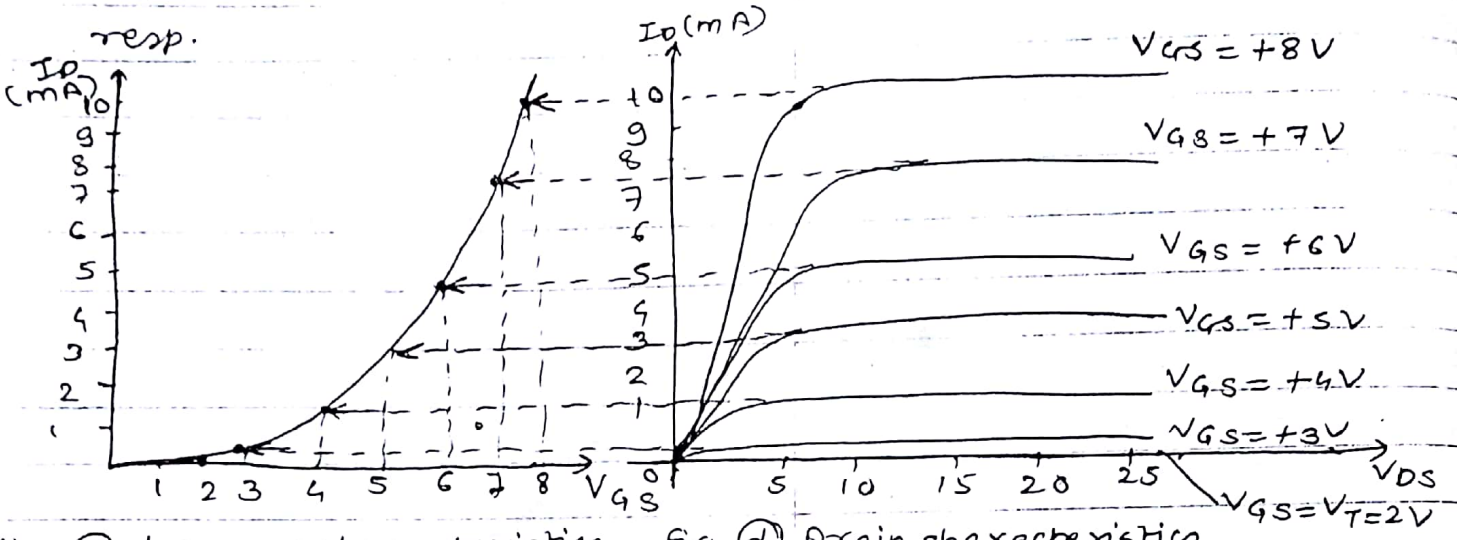


fig © transfer characteristics fig ⓓ Drain characteristics.

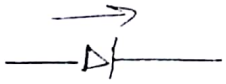
- Drain current is zero for $V_{GS} \leq V_T$.
- The transfer characteristics is shown in fig ©. is very much different from those obtain earlier.
- It is now totally in the +ve V_{GS} region & remains zero till $V_{GS} = V_T$.
- The relation bet^n I_D & V_{GS} is given by the following eqn

$$I_D = K (V_{GS} - V_T)^2$$

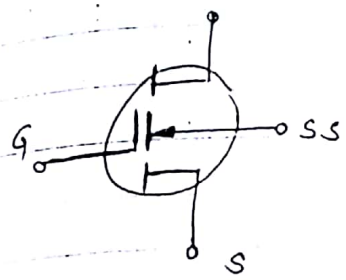
- It is the squared term that results in nonlinear (curved) relationship bet^n I_D & V_{GS}.

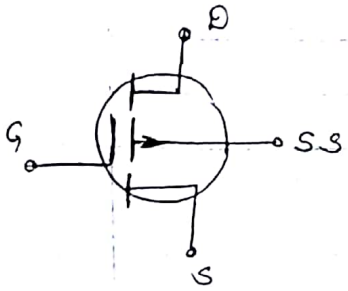
The term K is constant & its value depends on the construction of device

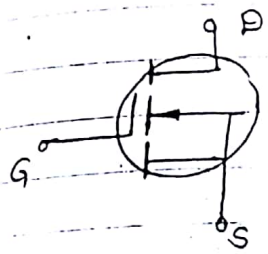
$$\text{where} \quad K = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

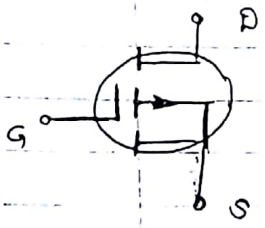


* **symbols** –









n-channel enhancement MOSFET

p-channel enhancement MOSFET

- The dashed line beth D & S is choses to reflect the fact that a channel does not exist beth the two under no-bias condn.
- It is the only difference bet the symbols for the depletion type & enhancement type MOSFETs.