Introduction :-

The Bipolar Junction Transistor (BJT) is an extremely common electronic device to all forms of electronic circuits. It can be used for a number of useful applications such as an amplifier, a switch, a buffer, an oscillator, a nonlinear circuit – so forth.
The BJT is made by P and N type semiconductor material, which should be familiar from the study of diodes. The BJT is a three terminal device (Fig 1).

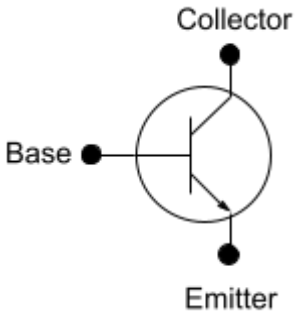
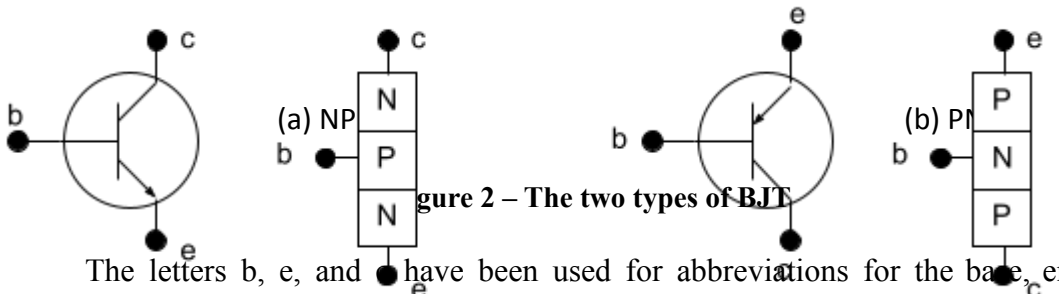


Fig.1.

The three terminals are Base, Collector and Emitter. The emitter terminal always has an arrow. The collector is always on the opposite side of the emitter and the base is the other remaining terminal on the left. Note that this is the conventional schematic diagram of a BJT transistor. Furthermore, there are two types of BJT transistors. They are the NPN type, and the PNP type. Figure 2 illustrates this:



gure 2 – The two types of BJT

The letters b, e, and c have been used for abbreviations for the base, emitter and collector terminals respectively. An NPN transistor is always drawn with the arrow pointing outwards whilst the PNP transistor always has the arrow pointing inwards. And of course, remember that the arrow is always the emitter terminal. So which type is the transistor in Fig 1? – It is NPN. The other diagrams shown in Figure 2 illustrate why the transistors are called either NPN or PNP. It's simply due to the semiconductor material used for each terminal.

Now, lets take a more detailed look:

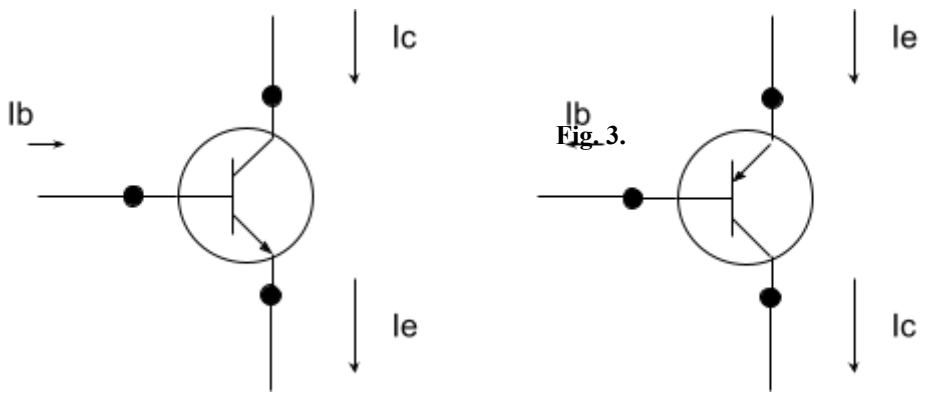
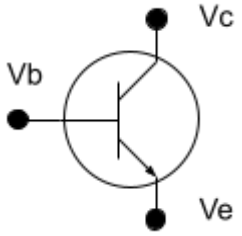


Fig. 3.

The arrows show the direction of DC current flow for both the NPN and PNP cases. In both cases the base current (Ib) is a very small current in the order of microamps whilst the collector current (Ic) and emitter current (Ie) are larger and in the order of milliamps. Note that for the NPN transistor, the base current flows into the transistor but for the PNP transistor, the base current flows out the transistor. Also note Ic and Ie always flow in the same direction and in the direction of the (black) arrow, the same arrow that tells us whether the transistor is PNP or NPN.
Now for the voltages



The voltage at the base is normally written as Vb.
The voltage at the collector is normally written as Vc.
The voltage at the emitter is normally written Ve.

That part was easy, but what about the voltage between the collector and the emitter? Is it written as Vce or Vec? The convention is that the first subscript letter is the voltage that you are measuring and the second subscript letter is the reference. That means, if:

Vc = 6V *(The voltage at the collector is 6 volts)*
Ve = 2V *(The voltage at the emitter is 2 volts)*

Then Vce is 4V because the voltage at the collector is 4V higher than the voltage at the emitter. Also, Vec = -4V because the voltage at the emitter (measuring point) is 4V lower than the voltage at the collector (reference point). This concept is important and If you're a bit lost read it again. The following diagram should summarize. This is the convention used for measuring voltages between terminals of the NPN and PNP transistors. The reason for this is that in these examples the first subscript letter is usually of higher voltage than the second, hence all variables listed below will have positive values.

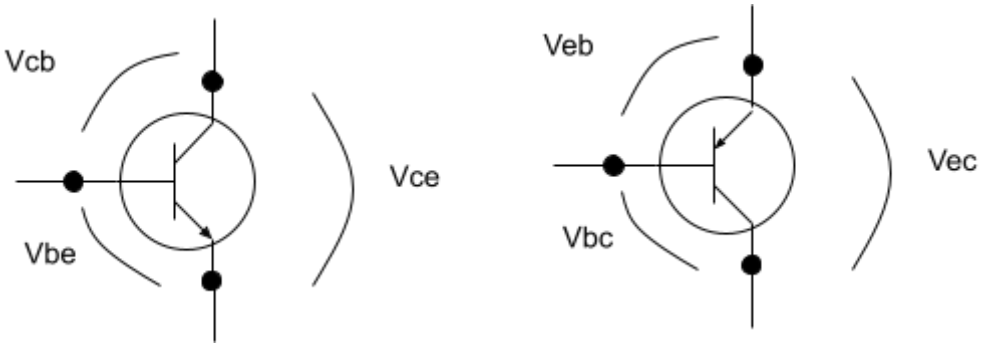


Fig.4

<u>Transistor Working :-</u>

A transistor is basically a Si on Ge crystal containing three separate regions. It can be either NPN or PNP type **Fig.1** The middle region is called the base and the outer two regions are called emitter and the collector. The outer layers although they are of same type but their functions cannot be changed. They have different physical and electrical properties.

In most transistors, emitter is heavily doped. Its job is to emit or inject electrons into the base. These bases are lightly doped and very thin, it passes most of the emitter-injected electrons on to the collector. The doping level of collector is intermediate between the heavy doping of emitter and the light doping of the base.

The collector is so named because it collects electrons from base. The collector is the largest of the three regions; it must dissipate more heat than the emitter or base. The transistor has two junctions. One between emitter and the base and other between the base and the collector. Because of this the transistor is similar to two diodes, one emitter diode and other collector base diode.

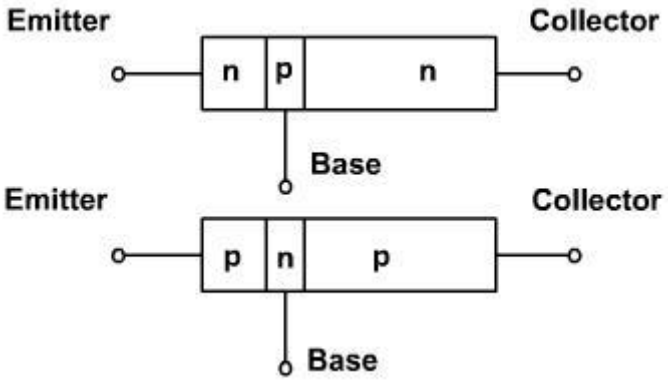


Fig .1

When transistor is made, the diffusion of free electrons across the junction produces two depletion layers. For each of these depletion layers, the barrier potential is 0.7 V for Si transistor and 0.3 V for Ge transistor.

The depletion layers do not have the same width, because different regions have different doping levels. The more heavily doped a region is, the greater the concentration of ions near the junction. This means the depletion layer penetrates more deeply into the base and slightly into emitter. Similarly, it penetration more into collector. The thickness of collector depletion layer is large while the base depletion layer is small as shown in **fig 2**

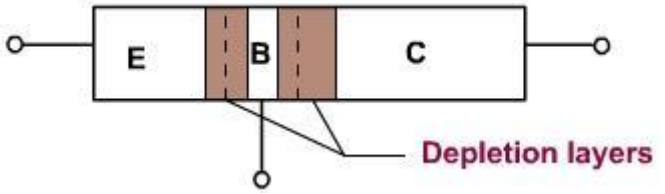


Fig2

If both the junctions are forward biased using two d.c sources, as shown in **Fig3a** free electrons (majority carriers) enter the emitter and collector of the transistor, joins at the base and come out of the base. Because both the diodes are forward biased, the emitter and collector currents are large**.**

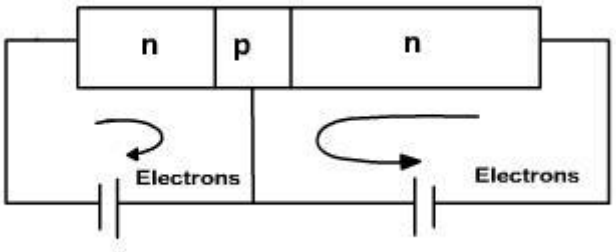


Fig3a

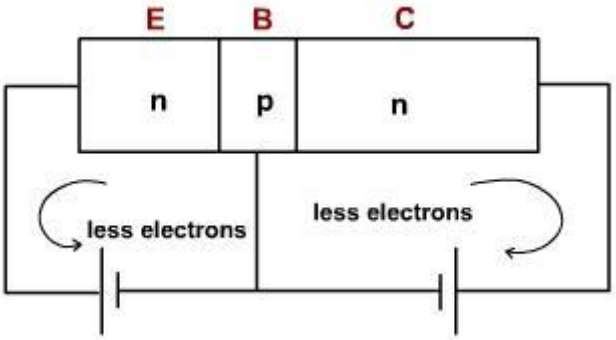


Fig3b

If both the junction are reverse biased as shown in **Fig. 3b**, then small currents flows through both junctions only due to thermally produced minority carriers and surface leakage. Thermally produced carriers are temperature dependent it approximately doubles for every 10 degree celsius rise in ambient temperature. The surface leakage current increases with voltage**.**

When the emitter diode is forward biased and collector diode is reverse biased as shown in **fig. 4** then one expect large emitter current and small collector current but collector current is almost as large as emitter current.

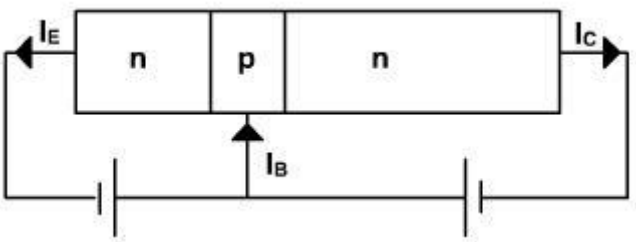


Fig. 4

When emitter diodes forward biased and the applied voltage is more than 0.7 V (barrier potential) then larger number of majority carriers (electrons in n-type) diffuse across the junction.

Once the electrons are injected by the emitter enter into the base, they become minority carriers. These electrons do not have separate identities from those, which are thermally generated, in the base region itself. The base is made very thin and is very lightly doped. Because of this only few electrons traveling from the emitter to base region recombine with holes. This gives rise to recombination current. The rest of the electrons exist for more time. Since the collector diode is reverse biased, (n is connected to positive supply) therefore most of the electrons are pushed into collector layer. These collector elections can then flow into the external collector lead.

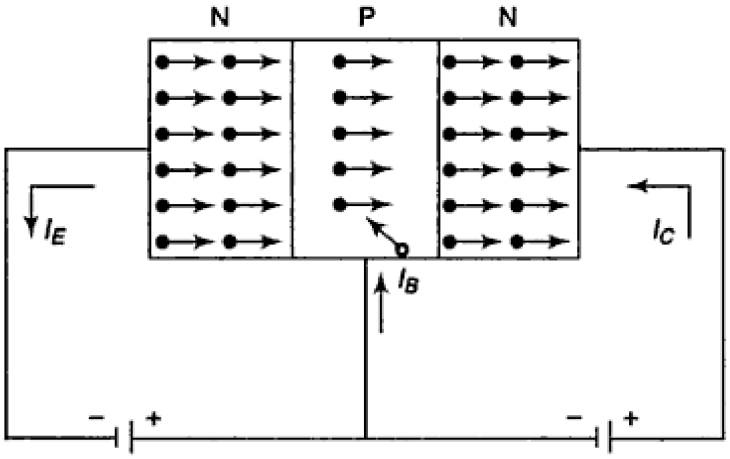


Fig. 6.4 Current in NPN transistor

Thus, there is a steady stream of electrons leaving the negative source terminal and entering the emitter region. The V_{EB} forward bias forces these emitter electrons to enter the base region. The thin and lightly doped base gives almost all those electrons enough lifetime to diffuse into the depletion layer. The depletion layer field pushes a steady stream of electron into the collector region. These electrons leave the collector and flow into the positive terminal of the voltage source. In most transistor, more than 95% of the emitter injected electrons flow to the collector, less than 5% fall into base holes and flow out the external base lead. But the collector current is less than emitter current.

Relation between different currents in a transistor:

The total current flowing into the transistor must be equal to the total current flowing out of it. Hence, the emitter current I_E is equal to the sum of the collector (I_C) and base current (I_B). That is,

$$I_E = I_C + I_B$$

The currents directions are positive directions. The total collector current I_C is made up of two components.

1. The fraction of emitter (electron) current which reaches the collector ($a_{dc}\, I_E$)
2. The normal reverse leakage current I_{CO}

$$\therefore I_C = \alpha_{dc} I_E + I_{co}$$

$$\text{or} \qquad \alpha_{dc} = \frac{I_C - I_{co}}{I_E}$$

a_{dc} is known as large signal current gain or dc alpha. It is always positive. Since collector current is almost equal to the I_E therefore αdc I_E varies from 0.9 to 0.98. Usually, the reverse leakage current is very small compared to the total collector current.

$$\text{Neglecting } I_{co}, \quad \alpha_{dc} = \frac{I_C}{I_E}$$

NOTE

Early effect or base-width modulation As the collector voltage V_{CC} is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base-width on collector-to-emitter voltage is known as the *Early effect*. This decrease in effective base-width has three consequences:

(i) There is less chance for recombination within the base region. Hence, α increases with increasing $|V_{CB}|$.

(ii) The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the emitter junction increases.

(iii) For extremely large voltages, the effective base-width may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is called the *punch through*.

For higher values of V_{CB}, due to Early effect, the value of α increases. For example, α changes, say from 0.98 to 0.985. Hence, there is a very small positive slope in the CB output characteristics and hence the output resistance is not zero.

The Common Base Configuration:

If the base is common to the input and output circuits, it is know as common base configuration as shown in **fig. 1**.

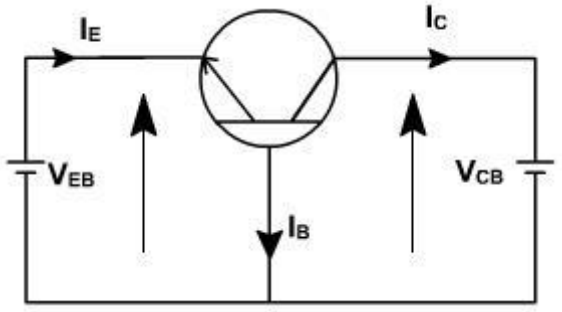


Fig. 1

For a pnp transistor the largest current components are due to holes. Holes flow from emitter to collector and few holes flow down towards ground out of the base terminal. The current directions are shown in **fig. 1**.

$$(I_E = I_C + I_B).$$

For a forward biased junction, V_{EB} is positive and for a reverse biased junction V_{CB} is negative. The complete transistor can be described by the following two relations, which give the input voltage V_{EB} and output current I_C in terms of the output voltage (V_{CB}) and input current I_E.

$$V_{EB} = f_1(V_{CB}, I_E)$$

$$I_C = f_2(V_{CB}, I_E)$$

The output characteristic:

The collector current I_C is completely determined by the input current I_E and the V_{CB} voltage. The relationship is given in **fig. 2.** It is a plot of I_C versus V_{CB}, with emitter current I_E as parameter. The curves are known as the output or collector or static characteristics. The transistor consists of two diodes placed in series back to back (with two cathodes connected together). The complete characteristic can be divided in three regions.

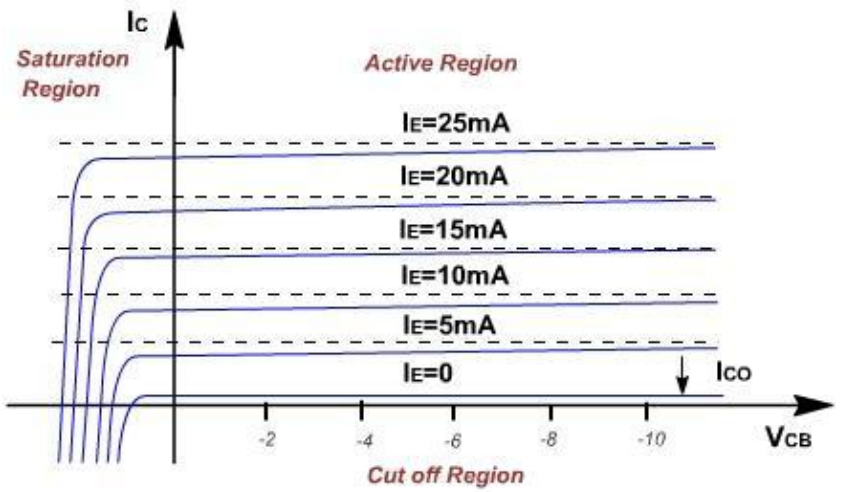


Fig 2

1. **Active region:**

In this region the collector diode is reverse biased and the emitter diode is forward biased. Consider first that the emitter current is zero. Then the collector current is small and equals the reverse saturation current I_{CO} of the collector junction considered as a diode.

If the forward current I_B is increased, then a fraction of I_E ie. $\alpha_{dc}I_E$ will reach the collector. In the active region, the collector current is essentially independent of collector voltage and depends only upon the emitter current. Because α_{dc} is, less than one but almost equal to unity, the magnitude of the collector current is slightly less that of emitter current. The collector current is almost constant and work as a current source.

The collector current slightly increases with voltage. This is due to early effect. At higher voltage collector gathers in a few more electrons. This reduces the base current. The difference is so small, that it is usually neglected. If the collector voltage is increased, then

space charge width increases; this decreased the effective base width. Then there is less chance for recombination within the base region.

2. **Saturation region:**

The region to the left of the ordinate $V_{CB} = 0$, and above the $I_E = 0$, characteristic in which both emitter and collector junction are forward biased, is called saturation region.

When collector diode is forward biased, there is large change in collector current with small changes in collector voltage. A forward bias means, that p is made positive with respect to n, there is a flow of holes from p to n. This changes the collector current direction. If diode is sufficiently forward biased the current changes rapidly. It does not depend upon emitter current.

3. **Cut off region:**

The region below $I_E = 0$ and to the right of V_{CB} for which emitter and collector junctions are both reversed biased is referred to cutoff region. The characteristics $I_E = 0$, is similar to other characteristics but not coincident with horizontal axis. The collector current is same as I_{CO}. I_{CBO} is frequently used for I_{CO}. It means collector to base current with emitter open. This is also temperature dependent.

The Input Characteristic:

In the active region the input diode is forward biased, therefore, input characteristic is simply the forward biased characteristic of the emitter to base diode for various collector voltages. **fig. 3.** Below cut in voltage (0.7 or 0.3) the emitter current is very small. The curve with the collector open represents the forward biased emitter diode. Because of the early effect the emitter current increases for same V_{EB}. (The diode becomes better diode).

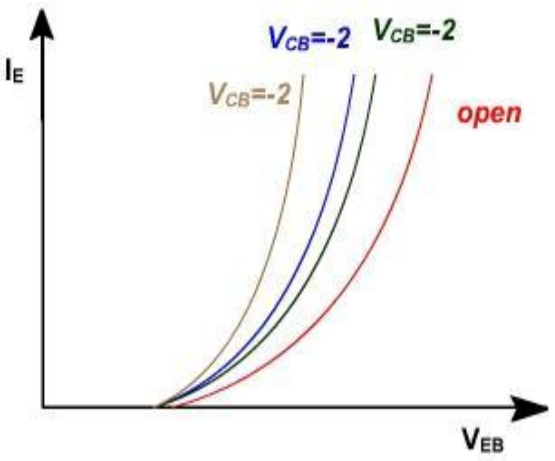


Fig. 3

When the collector is shorted to the base, the emitter current increases for a given V_{EB}since the collector now removes minority carriers from the base, and hence base can attract more holes from the emitter. This mean that the curve V_{CB}= 0, is shifted from the character when V_{CB} = open.

Equivalent circuit of a transistor: (Common Base) :-

In an ideal transistor, α_{dc}= 1. This means all emitter electrons entering the base region go on to the collector. Therefore, collector current equals emitter current. For transistor action, emitter diode acts like a forward bias diode and collector diode acts like a current source. The equivalent circuits of npn and pnp transistors are shown in **fig. 4.** The current source arrow points for conventional current. The current source is controlled by emitter current.

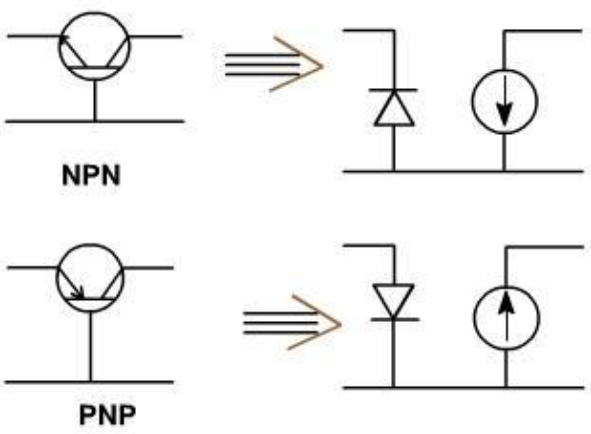


Fig.4

In the dc mode the levels of *IC* and *IE* due to the majority carriers are related by a quantity called *alpha* and defined by the following equation:

Common Emitter Configuration :-

The common emitter configuration of BJT is shown in **fig. 1**.

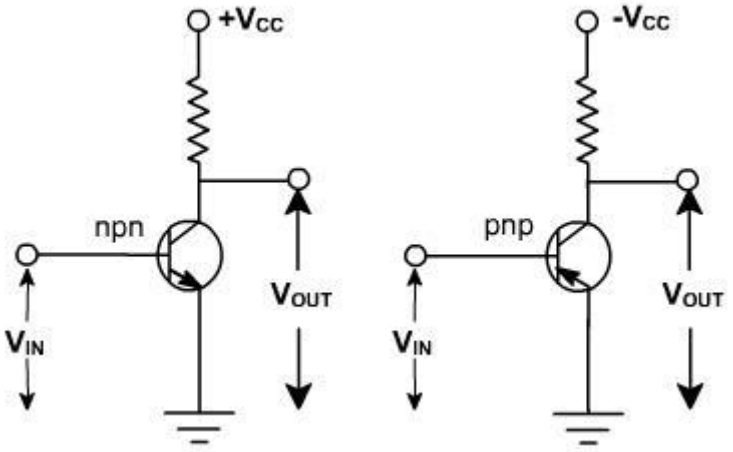


Fig. 1

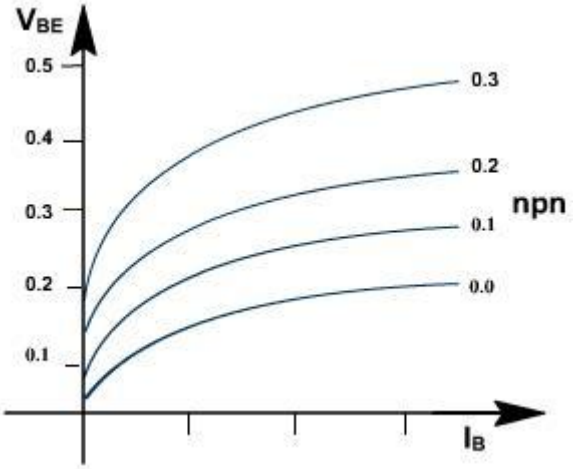
In C.E. configuration the emitter is made common to the input and output. It is also referred to as grounded emitter configuration . It is most commonly used configuration. In this, base current and output voltages are taken as impendent parameters and input voltage and output current as dependent parameters

$$V_{BE} = f_1 (I_B, V_{CE})$$

$$I_C = f_2(I_B, V_{CE})$$

Input Characteristic:

The curve between I_B and V_{BE} for different values of V_{CE} are shown in **fig. 2**. Since the base emitter junction of a transistor is a diode, therefore the characteristic is similar to diode one. With higher values of V_{CE} collector gathers slightly more electrons and therefore base current reduces. Normally this effect is neglected. (Early effect). When collector is shorted with emitter then the input characteristic is the characteristic of a forward biased diode when V_{BE} is zero and I_B is also zero.



Output Characteristic:

The output characteristic is the curve between V_{CE} and I_C for various values of I_B. For fixed value of I_B and is shown in **fig. 3**. For fixed value of I_B, I_C is not varying much dependent on V_{CE} but slopes are greater than CE characteristic. The output characteristics can again be divided into three parts.

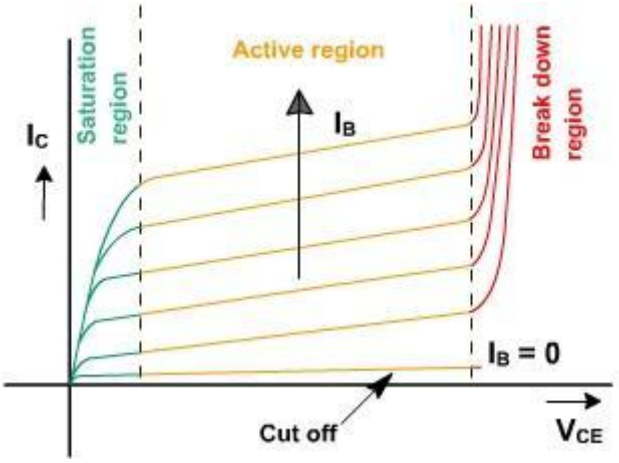


Fig. 3

(1) Active Region:

In this region collector junction is reverse biased and emitter junction is forward biased. It is the area to the right of V_{CE} = 0.5 V and above I_B= 0. In this region transistor

current responds most sensitively to I_B. If transistor is to be used as an amplifier, it must operate in this region.

$$I_E = I_C + I_B$$

Since, $I_C = I_{Co} + \alpha_{dc} I_E$

$$I_C = I_{Co} + \alpha_{dc}(I_C + I_B)$$

or $(1 - \alpha_{dc}) I_C = \alpha_{dc} I_B + I_{CO}$

or $$I_C = \left(\frac{\alpha_{dc}}{1 - \alpha_{dc}}\right) I_B + \left(\frac{1}{1 - \alpha_{dc}}\right) I_{CO}$$

Let, $\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}$

$\therefore I_C = (1 + \beta_{dc}) I_{CO} + \beta_{dc} I_B$

β_{dc} is defined as current gain of the transistor is given by

$$\beta_{dc} = \frac{I_C - I_{CO}}{I_B + I_{CO}}$$

If α_{dc} is truly constant then I_C would be independent of V_{CE}. But because of early effect, α_{dc} increases by 0.1% (0.001) e.g. from 0.995 to 0.996 as V_{CE} increases from a few volts to 10V. Then€β_{dc} increases from 0.995 / (1-0.995) = 200 to 0.996 / (1-0.996) = 250 or about 25%. This shows that small change in α reflects large change in β. Therefore the curves are subjected to large variations for the same type of transistors.

(2) Cut Off:

Cut off in a transistor is given by $I_B = 0$, $I_C = I_{CO}$. A transistor is not at cut off if the base current is simply reduced to zero (open circuited) under this condition,

$$I_C = I_E = I_{CO} / (1 - \alpha_{dc}) = I_{CEO}$$

The actual collector current with base open is designated as I_{CEO}. Since even in the neighborhood of cut off, ✔ ▲$_{dc}$ may be as large as 0.9 for Ge, then I_C=10 I_{CO}(approximately), at zero base current. Accordingly in order to cut off transistor it is not enough to reduce I_B to zero, but it is necessary to reverse bias the emitter junction slightly. It is found that reverse voltage of 0.1 V is sufficient for cut off a transistor. In Si, the ▲ ✔ ▲$_{dc}$ is very nearly equal to zero, therefore, $I_C = I_{CO}$. Hence even with $I_B = 0$, $I_C = I_E = I_{CO}$ so that transistor is very close to cut off.

In summary, cut off means $I_E = 0$, $I_C = I_{CO}$, $I_B = -I_C = -I_{CO}$, and V_{BE} is a reverse voltage whose magnitude is of the order of 0.1 V for Ge and 0 V for Si.

Reverse Collector Saturation Current I_{CBO}:

When in a physical transistor emitter current is reduced to zero, then the collector current is known as I_{CBO} (approximately equal to I_{CO}). Reverse collector saturation current I_{CBO} also varies with temperature, avalanche multiplication and variability from sample to

sample. Consider the circuit shown in **fig. 4**. V_{BB} is the reverse voltage applied to reduce the emitter current to zero.

$I_E = 0, \qquad I_B = -I_{CBO}$

If we require, $V_{BE} = -0.1$ V

Then $-V_{BB} + I_{CBO} R_B < -0.1$ V

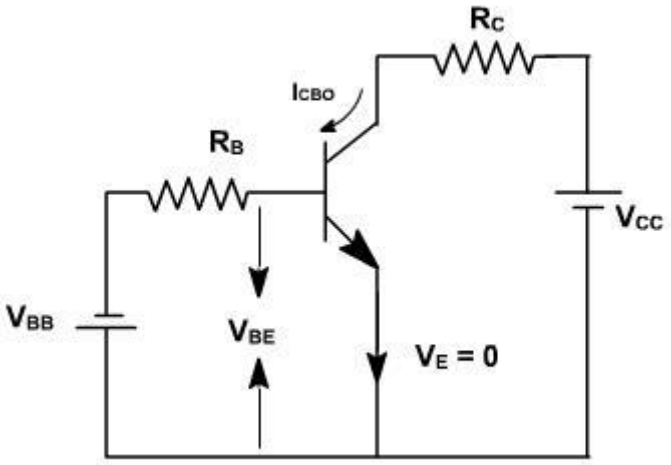


Fig. 4

If $R_B = 100$ K, $I_{CBO} = 100$ m A, Then V_{BB} must be 10.1 Volts. Hence transistor must be capable to withstand this reverse voltage before breakdown voltage exceeds.

(3).Saturation Region:

In this region both the diodes are forward biased by at least cut in voltage. Since the voltage V_{BE} and V_{BC} across a forward is approximately 0.7 V therefore, $V_{CE} = V_{CB} + V_{BE} = -V_{BC} + V_{BE}$ is also few tenths of volts. Hence saturation region is very close to zero voltage axis, where all the current rapidly reduces to zero. In this region the transistor collector current is approximately given by V_{CC} / R_C and independent of base current. Normal transistor action is last and it acts like a small ohmic resistance.

Large Signal Current Gain β_{dc} :-

The ratio I_c / I_B is defined as transfer ratio or large signal current gain β_{dc}

$$\beta_{dc} = \frac{I_C}{I_B}$$

Where I_C is the collector current and I_B is the base current. The β_{dc} is an indication if how well the transistor works. The typical value of β_{dc} varies from 50 to 300.

In terms of h parameters, β_{dc} is known as dc current gain and in designated h_{fE} ($\beta_{dc} = h_{fE}$). Knowing the maximum collector current and β_{dc} the minimum base current can be found which will be needed to saturate the transistor.

$$I_{C(max)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = I_{C(sat)}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}}$$

This expression of β_{dc} is defined neglecting reverse leakage current (I_{CO}). Taking reverse leakage current (I_{CO}) into account, the expression for the β_{dc} can be obtained as follows:

β_{dc} in terms of α_{dc} is given by

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}$$

$$= \frac{\frac{I_C - I_{CO}}{I_E}}{1 - \frac{I_C - I_{CO}}{I_E}} = \frac{I_C - I_{CO}}{I_E - I_C + I_{CO}}$$

$$= \frac{I_C - I_{CO}}{I_B + I_{CO}}$$

Since, $I_{CO} = I_{CBO}$

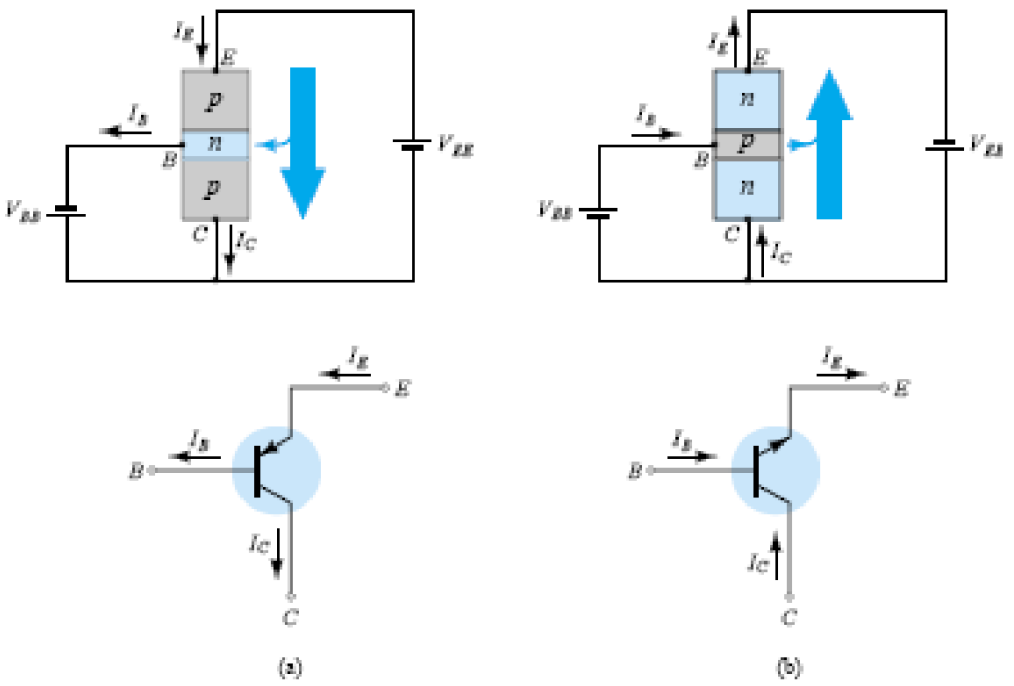
$$\therefore \beta_{dc} = \frac{I_C - I_{CBO}}{I_B + I_{CBO}}$$

Cut off of a transistor means $I_E = 0$, then $I_C = I_{CBO}$ and $I_B = - I_{CBO}$. Therefore, the above expression. β_{dc} gives the collector current increment to the base current change form cut off to I_B and hence it represents the large signal current gain of all common emitter transistor.

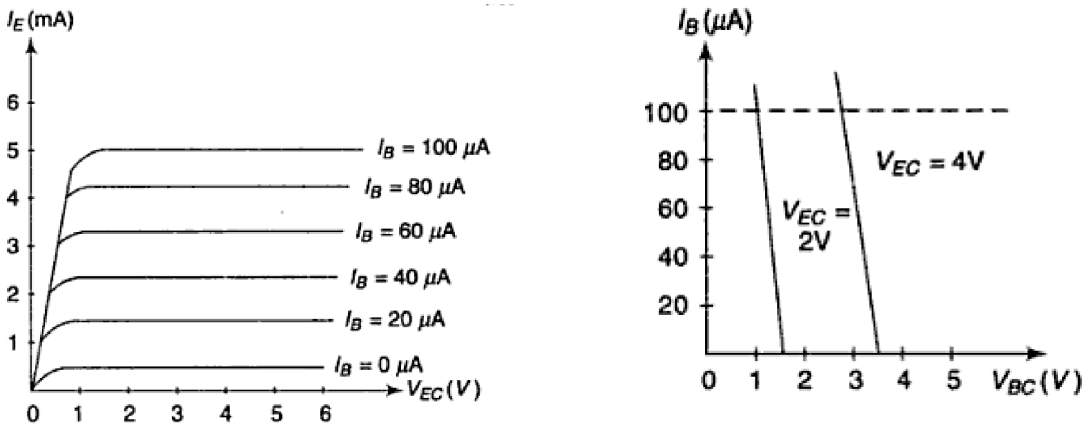
Common Collector Configuration :-

The third and final transistor configuration is the *common-collector configuration,* shown in Fig. 3.20 with the proper current directions and voltage notation. The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common-emitter configurations.

A common-collector circuit configuration is provided in **Fig.** with the load resistor connected from emitter to ground. Note that the collector is tied to ground even though the transistor is connected in a manner similar to the common-emitter configuration.



Fig



CC Output Characteristics

Baising Technique :-

CC Input Characteristics

Fixed Bias :

The fixed-bias circuit of **Fig**.1 provides a relatively straightforward and simple introduction to transistor dc bias analysis. Even though the network employs an *npn* transistor, the equations and calculations apply equally well to a *pnp* transistor configuration merely by changing all current directions and voltage polarities. The current directions of

Fig. 1 are the actual current directions, and the voltages are defined by the standard double-subscript notation. For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an opencircuit equivalent. In addition, the dc supply *VCC* can be separated into two supplies (for analysis purposes only) as shown in **Fig.** to permit a separation of input and output circuits. It also reduces the linkage between the two to the base current *IB*. The separation is certainly valid, as we note in **Fig.2** that *VCC* is connected directly to *RB* and *RC* just as in **Fig.1**

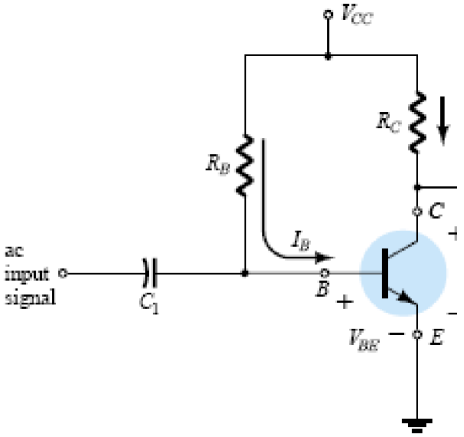


Fig1

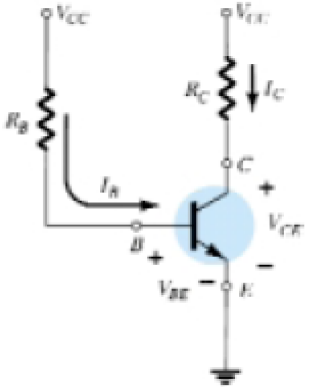


Fig 2

<u>Forward Bias of Base–Emitter</u>

Consider first the base–emitter circuit loop of **Fig. 4.4.** Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Note the polarity of the voltage drop across *RB* as established by the indicated direction of *IB*. Solving the equation for the current *IB* will result in the following:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

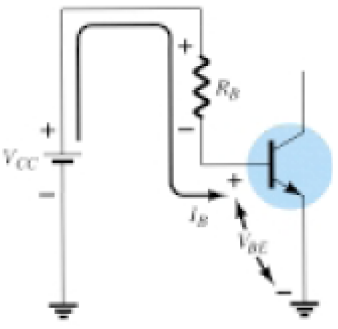


Fig4.4 :- Base Emitter loop

Above equation is certainly not a difficult one to remember if one simply keeps in mind that the base current is the current through *RB* and by Ohm's law that current is the voltage across *RB* divided by the resistance *RB*. The voltage across *RB* is the applied voltage *VCC* at one end less the drop across the base-to-emitter junction (*VBE*).

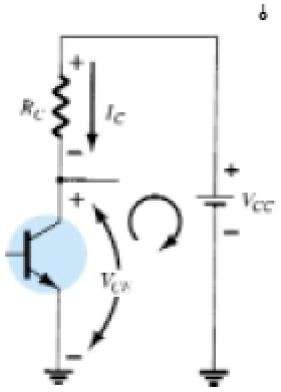
In addition, since the supply voltage *VCC* and the base–emitter voltage *VBE* are constants, the selection of a base resistor, *RB*, sets the level of base current for the operating point.

Collector–Emitter Loop

The collector–emitter section of the network appears in **Fig. 4.5** with the indicated direction of current *IC* and the resulting polarity across *RC*. The magnitude of the collector current is related directly to *IB* through

$$I_C = \beta I_B$$

It is interesting to note that since the base current is controlled by the level of *RB* and *IC* is related to *IB* by a constant _, the magnitude of *IC* is not a function of the resistance *RC*. Change *RC* to any level and it will not affect the level of *IB* or *IC* as long as we remain in the active region of the device. However, as we shall see, the level of *RC* will determine the magnitude of *VCE*, which is an important parameter. Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop of Fig. 4.5 will result in the following:



$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

Fig 4.5 Collector Emitter loop

which states in words that the voltage across the collector–emitter region of a transistor in the fixed-bias configuration is the supply voltage less the drop across *RC*. As a brief review of single- and double-subscript notation recall that

$$V_{CE} = V_C - V_E$$

where *VCE* is the voltage from collector to emitter and *VC* and *VE* are the voltages from collector and emitter to ground respectively. But *in this case,* since *VE* = 0 V, we have

$$V_{CE} = V_C$$

$$V_{BE} = V_B - V_E$$

$$V_{BE} = V_B$$

and V_E = 0 V, then

Biasing Circuit Techniques or Locating the Q - Point:

In order for a transistor to amplify, it has to be properly biased. This means forward biasing the base emitter junction and reverse biasing collector base junction. For linear amplification, the transistor should operate in active region (If I_E increases, I_C increases, V_{CE} decreases proportionally).

The source V_{BB}, through a current limit resistor R_B forward biases the emitter diode and V_{CC} through resistor R_C (load resistance) reverse biases the collector junction as shown in **fig. 1.**

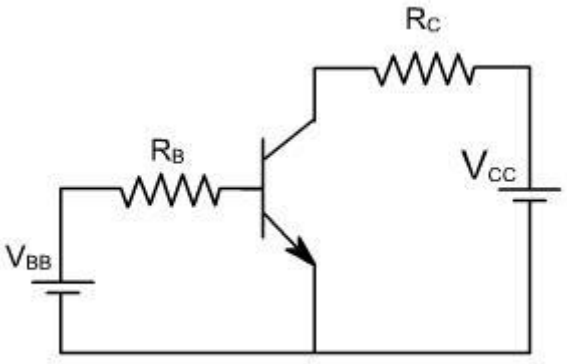


Fig. 1

The dc base current through R_B is given by

$$I_B = (V_{BB} - V_{BE}) / R_B$$

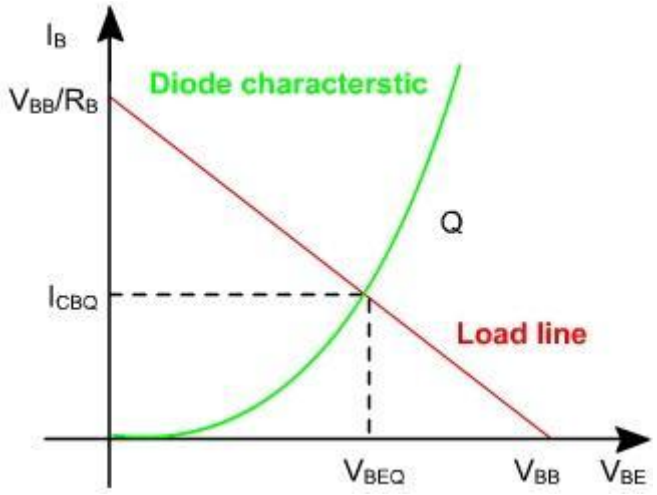
$$\text{or } V_{BE} = V_{BB} - I_B R_B$$

Normally V_{BE} is taken 0.7V or 0.3V. If exact voltage is required, then the input characteristic (I_B vs V_{BE}) of the transistor should be used to solve the above equation. The load line for the input circuit is drawn on input characteristic. The two points of the load line can be obtained as given below

$$\text{For } I_B = 0, \qquad V_{BE} = V_{BB}.$$

$$\text{and For } V_{BE} = 0, I_B = V_{BB}/ R_B.$$

The intersection of this line with input characteristic gives the operating point Q as shown in **fig. 2**. If an ac signal is connected to the base of the transistor, then variation in V_{BE} is about Q - point. This gives variation in I_B and hence I_C.



Biasing Techniques for CE Amplifiers

In the output circuit, the load equation can be written as

$V_{CE} = V_{CC} - I_C R_C$

This equation involves two unknown V_{CE} and I_C and therefore can not be solved. To solve this equation output characteristic ($I_C$vs V_{CE}) is used.

The load equation is the equation of a straight line and given by two points:

$I_C = 0, \quad V_{CE} = V_{CC}$

& $\quad V_{CE} = 0, \quad I_C = V_{CC} / R_C$

The intersection of this line which is also called dc load line and the characteristic gives the operating point Q as shown in **fig. 3**.

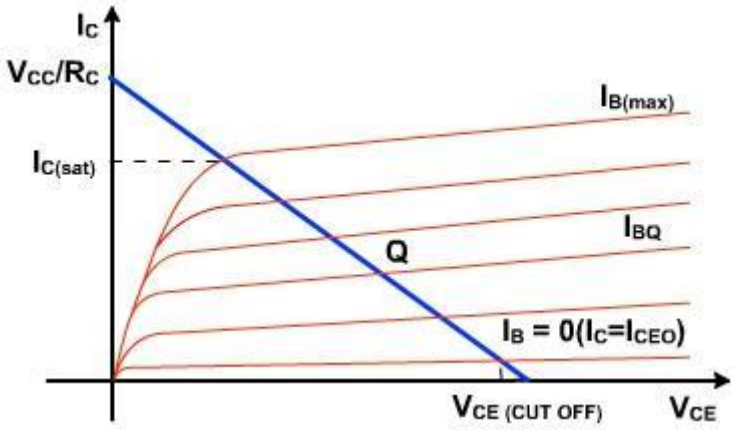


Fig. 3

The point at which the load line intersects with $I_B = 0$ characteristic is known as cut off point. At this point base current is zero and collector current is almost negligibly small. At

cut off the emitter diode comes out of forward bias and normal transistor action is lost. To a close approximation.

$$V_{CE} \text{ (cut off)} \approx V_{CC} \text{ (approximately).}$$

The intersection of the load line and $I_B = I_{B(max)}$ characteristic is known as saturation point . At this point $I_B = I_{B(max)}$, $I_C = I_{C(sat)}$. At this point collector diodes comes out of reverse bias and again transistor action is lost. To a close approximation,

$$I_{C(sat)} \approx V_{CC} / R_C \text{(approximately).}$$

The $I_{B(sat)}$ is the minimum current required to operate the transistor in saturation region. If the I_B is less than $I_{B\,(sat)}$, the transistor will operate in active region. If $I_B > I_{B\,(sat)}$ it always operates in saturation region.

If the transistor operates at saturation or cut off points and no where else then it is operating as a switch is shown in **fig. 4**.

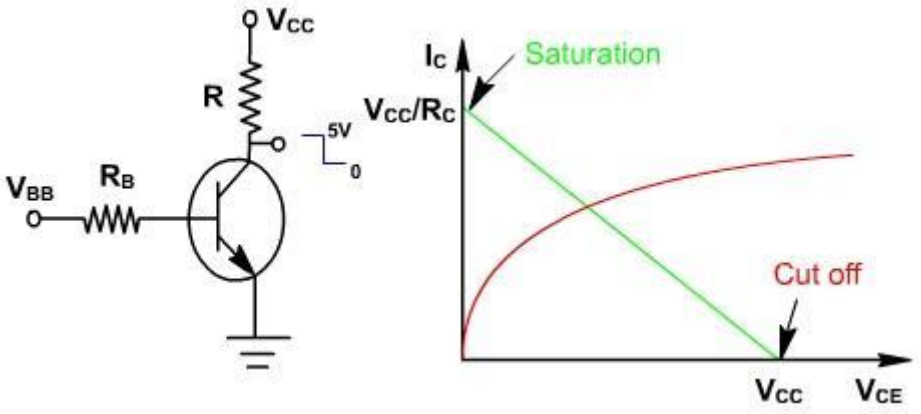


Fig. 4

$$V_{BB} = I_B R_B + V_{BE}$$

$$I_B = (V_{BB} - V_{BE}) / R_B$$

If $I_B > I_{B(sat)}$, then it operates at saturation, If $I_B = 0$, then it operates at cut off.

If a transistor is operating as an amplifier then Q point must be selected carefully. Although we can select the operating point any where in the active region by choosing different values of R_B & $R_C$but the various transistor ratings such as maximum collector dissipation $P_{C(max)}$ maximum collector voltage $V_{C(max)}$ and $I_{C(max)}$ & $V_{BE(max)}$ limit the operating range.

Once the Q point is established an ac input is connected. Due to this the ac source the base current varies. As a result of this collector current and collector voltage also varies and the amplified output is obtained.

If the Q-point is not selected properly then the output waveform will not be exactly the input waveform. i.e. It may be clipped from one side or both sides or it may be distorted one.

Voltage Divider Bias:

If the load resistance R_C is very small, e.g. in a transformer coupled circuit, then there is no improvement in stabilization in the collector to base bias circuit over fixed bias circuit. A circuit which can be used even if there is no dc resistance in series with the collector, is the voltage divider bias or self bias. **fig**.

The current in the resistance R_E in the emitter lead causes a voltage drop which is in the direction to reverse bias the emitter junction. Since this junction must be forward biased, the base voltage is obtained from the supply through R_1, R_2 network. If $R_b = R_1 \| R_2$ equivalent resistance is very – very small, then V_{BE} voltage is independent of I_{CO} and $\partial I_c / \partial I_{co} \to 0$. For best stability R_1 & R_2 must be kept small.

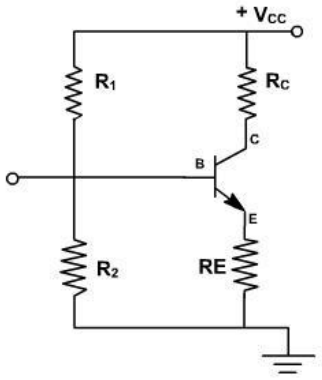


Fig.

If I_C tends to increase, because of I_{CO}, then the current in R_C increases, hence base current is decreased because of more reverse biasing and it reduces I_C .To analysis this circuit, the base circuit is replaced by its thevenin's equivalent as shown in **fig. 4**.

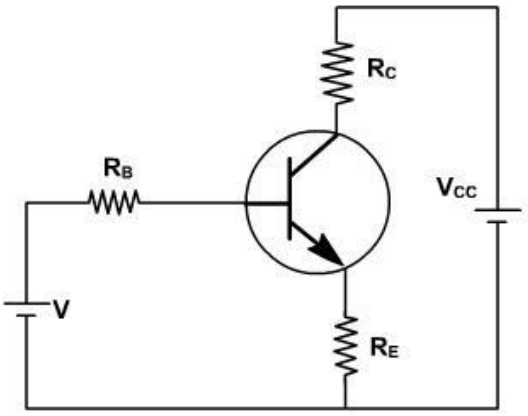


Fig. 4

Thevenin's voltage is

$$V = \frac{R_2}{R_1 + R_2} V_{CC},$$

$$R_b = \frac{R_1 R_2}{R_1 + R_2}$$

R_b is the effective resistance seen back from the base terminal.

$$V = I_B R_b + V_{BE} + (I_B + I_C) R_E$$

If V_{BE} is considered to be independent of I_C, then

In order to avoid the loss of ac signal because of the feedback caused by R_E, this resistance is often by passed by a large capacitance (> 10 μF) so that its reactance at the frequency under consideration is very small.

Small signal low frequency transistor Models:

All the transistor amplifiers are two port networks having two voltages and two currents. The positive directions of voltages and currents are shown in **fig. 1**.

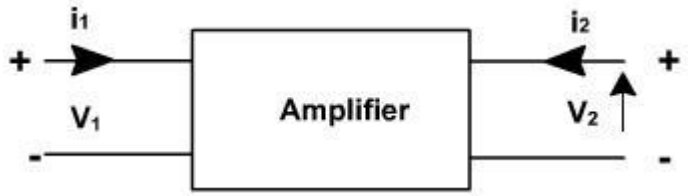


Fig. 1

Out of four quantities two are independent and two are dependent. If the input current i_1 and output voltage v_2 are taken independent then other two quantities i_2 and v_1 can be expressed in terms of i_1 and V_2.

$$v_1 = f_1(i_1, v_2)$$
$$i_2 = f_2(i_1, v_2)$$

The equations can be written as

$$v_1 = h_{11} i_1 + h_{12} v_2$$
$$i_2 = h_{21} i_1 + h_{22} v_2$$

where h_{11}, h_{12}, h_{21} and h_{22} are called h-parameters.

$$h_{11} = \left.\frac{v_1}{i_1}\right|_{v_2 = 0}$$

$h_{11} = h_i$ = input impedance with output short circuit to ac.

$$h_{12} = \left.\frac{v_1}{v_2}\right|_{i_2 = 0}$$

$h_{12}=h_r$ = fraction of output voltage at input with input open circuited or reverse voltage gain with input open circuited to ac (dimensions).

$$h_{21} = \left.\frac{i_2}{i_1}\right|_{v_2 = 0}$$

$h_{21} = h_f$ = negative of current gain with output short circuited to ac.

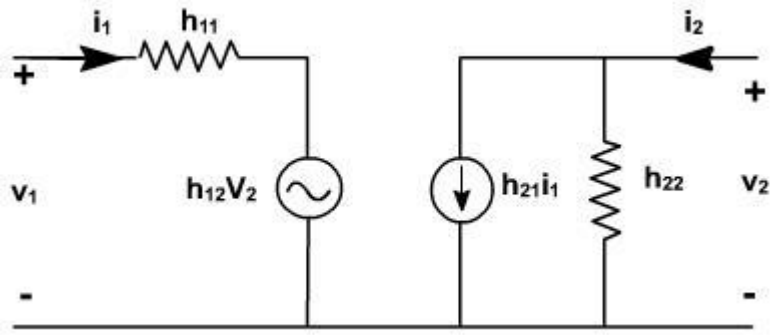
The current entering the load is negative of I_2. This is also known as forward short circuit current gain.

$$h_{22} = \left.\frac{i_2}{i_1}\right|_{i_2 = 0}$$

$h_{22}= h_o$ = output admittance with input open circuited to ac.

If these parameters are specified for a particular configuration, then suffixes e,b or c are also included, e.g. h_{fe} ,h_{ib} are h parameters of common emitter and common collector amplifiers

Using two equations the generalized model of the amplifier can be drawn as shown in **fig. 2**.



h-Parameters

The hybrid model for a transistor amplifier can be derived as follow:

Let us consider CE configuration as show in **fig.** . The variables, i_B, i_C ,v_C, and v_B represent total instantaneous currents and voltages i_B and v_C can be taken as independent variables and v_B, I_C as dependent variables.

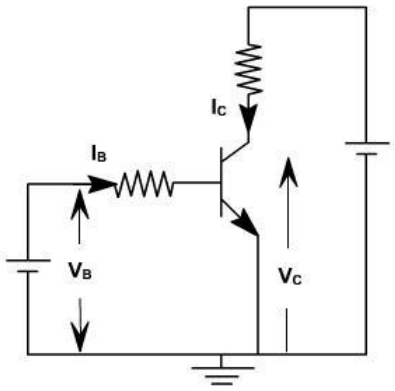


Fig.

$$v_B = f_1 (i_B , v_C)$$
$$I_C = f_2 (i_B , v_C).$$

Using Taylor 's series expression, and neglecting higher order terms we obtain.

$$\Delta v_B = \left.\frac{\partial f_1}{\partial i_B}\right|_{v_C} \Delta i_B + \left.\frac{\partial f_1}{\partial v_C}\right|_{i_B} \Delta v_C$$
$$\Delta i_C = \left.\frac{\partial f_2}{\partial i_B}\right|_{v_C} \Delta i_B + \left.\frac{\partial f_2}{\partial v_C}\right|_{i_B} \Delta v_C$$

The partial derivatives are taken keeping the collector voltage or base current constant. The Δv_B, Δv_C, Δi_B, Δi_C represent the small signal (incremental) base and collector current and voltage and can be represented as v_b ,i_b ,v_C ,i_C.

$$\therefore v_b = h_{ie}\, i_B + h_{re}\, v_C$$
$$i_C = h_{fe}\, i_B + h_{oe}\, v_b$$

where

$$h_{ie} = \left.\frac{\partial f_1}{\partial i_B}\right|_{v_c} = \left.\frac{\partial v_B}{\partial i_B}\right|_{v_c} ; \qquad h_{re} = \left.\frac{\partial f_1}{\partial v_C}\right|_{i_B} = \left.\frac{\partial v_B}{\partial v_C}\right|_{i_B}$$
$$h_{fe} = \left.\frac{\partial f_2}{\partial i_B}\right|_{v_c} = \left.\frac{\partial i_C}{\partial i_B}\right|_{v_c} ; \qquad h_{oe} = \left.\frac{\partial f_2}{\partial v_C}\right|_{i_B} = \left.\frac{\partial v_B}{\partial v_C}\right|_{i_B}$$

The model for CE configuration is shown in **fig. 4**.

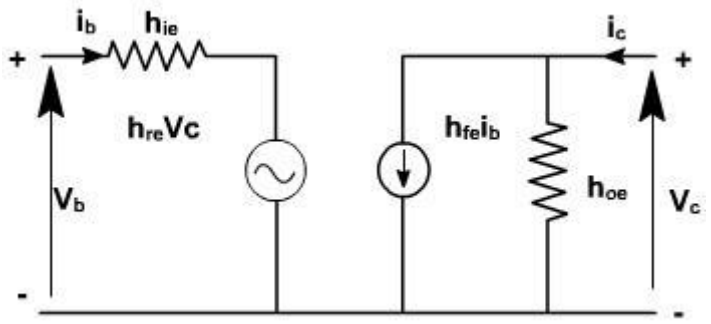


Fig. 4

Graphical Determination of h - parameters:

To determine the four h-parameters of transistor amplifier, input and output characteristic are used. Input characteristic depicts the relationship between input voltage and input current with output voltage as parameter. The output characteristic depicts the relationship between output voltage and output current with input current as parameter. Fig. 5, shows the output characteristics of CE amplifier.

$$h_{fe} = \left.\frac{\partial i_C}{\partial i_B}\right|_{V_C} = \frac{i_{C2} - i_{C1}}{i_{b2} - i_{b1}}$$

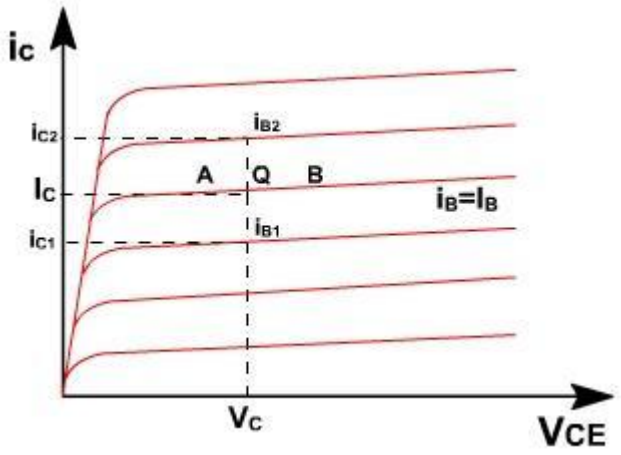


Fig. 5

The current increments are taken around the quiescent point Q which corresponds to iB = IB and to the collector voltage VCE = VC

$$h_{oe} = \left.\frac{\partial i_C}{\partial V_C}\right|_{i_B}$$

The value of hoe at the quiescent operating point is given by the slope of the output characteristic at the operating point (i.e. slope of tangent AB).

$$h_{ie} = \frac{\partial V_B}{\partial i_B} \approx \left.\frac{\Delta V_B}{\Delta i_B}\right|_{V_C}$$

hie is the slope of the appropriate input on fig. 6, at the operating point (slope of tangent EF at Q).

$$h_{re} = \frac{\partial V_B}{\partial V_C} = \left.\frac{\Delta V_B}{\Delta V_C}\right|_{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

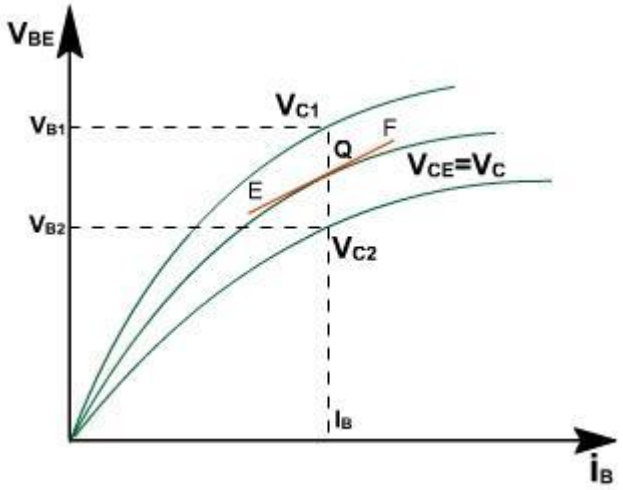


Fig. 6

A vertical line on the input characteristic represents constant base current. The parameter hre can be obtained from the ratio (VB2– V B1) and (VC2– V C1) for at Q.

Analysis of a transistor amplifier using h-parameters:

To form a transistor amplifier it is only necessary to connect an external load and signal source as indicated in fig. 1 and to bias the transistor properly.

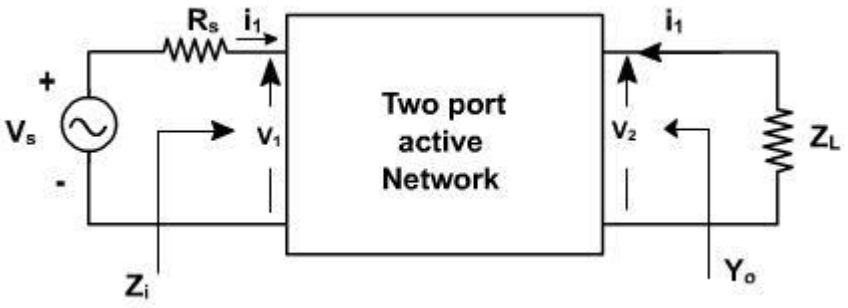


Fig. 1

Consider the two-port network of CE amplifier. R_S is the source resistance and Z_L is the load impedence h-parameters are assumed to be constant over the operating range. The ac equivalent circuit is shown in **fig. 2**. (Phasor notations are used assuming sinusoidal voltage input). The quantities of interest are the current gain, input impedence, voltage gain, and output impedence.

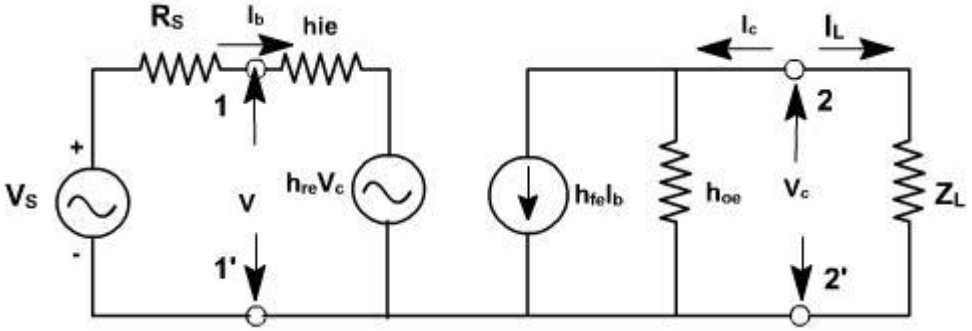


Fig. 2

Current gain: For the transistor amplifier stage, A_i is defined as the ratio of output to input currents.

$$A_i = \frac{I_L}{I_b} = \frac{-I_C}{I_b} \qquad (I_L + I_c = 0. \quad \therefore I_L = -I_c)$$

$$I_C = h_{fe} I_b + h_{oe} V_c$$

$$V_c = I_L Z_L = -I_c Z_L$$

$$\therefore I_c = h_{fe} I_b + h_{oe} (-I_c Z_L)$$

$$\text{or } \frac{I_c}{I_b} = \frac{h_{fe}}{1 + h_{oe} Z_L}$$

$$\therefore A_i = - \frac{h_{fe}}{1 + h_{oe} Z_L}$$

Input Impedence: The impedence looking into the amplifier input terminals (1,1') is the input impedence Z_i

$$Z_i = \frac{V_b}{I_b}$$

$$V_b = h_{ie} I_b + h_{re} V_c$$

$$\frac{V_b}{I_b} = h_{ie} + h_{re} \frac{V_c}{I_b}$$

$$= h_{ie} - \frac{h_{re} I_c Z_L}{I_b}$$

$$\therefore Z_i = h_{ie} + h_{re} A_i Z_L$$

$$= h_{ie} - \frac{h_{re} h_{fe} Z_L}{1 + h_{oe} Z_L}$$

$$\therefore Z_i = h_{ie} - \frac{h_{re} h_{fe}}{Y_L + h_{oe}} \qquad (\text{since } Y_L = \frac{1}{Z_L})$$

Voltage gain: The ratio of output voltage to input voltage gives the gain of the transistors.

$$A_v = \frac{V_C}{V_b} = - \frac{I_C Z_L}{V_b}$$

$$\therefore A_v = \frac{I_B A_i Z_L}{V_b} = \frac{A_i Z_L}{Z_i}$$

Output Admittance: It is defined as

$$Y_0 = \left. \frac{I_c}{V_c} \right|_{V_s} = 0$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

$$\frac{I_c}{V_c} = h_{fe} \frac{I_b}{V_c} + h_{oe}$$

when $V_s = 0$, $R_s . I_b + h_{ie} . I_b + h_{re} V_c = 0$.

$$\frac{I_b}{V_c} = - \frac{h_{re}}{R_s + h_{ie}}$$

$$\therefore Y_0 = h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}}$$

Voltage amplification taking into account source impedance (R_S) is given by

$$A_{VS} = \frac{V_c}{V_s} = \frac{V_c}{V_b} * \frac{V_b}{V_S} \qquad \left(V_b = \frac{V_s}{R_s + Z_i} * Z_i \right)$$

$$= A_V . \frac{Z_i}{Z_i + R_s}$$

$$= \frac{A_i Z_L}{Z_i + R_s}$$

A_v is the voltage gain for an ideal voltage source ($R_v = 0$).
Consider input source to be a current source I_S in parallel with a resistance R_S as shown in **fig. 3**.

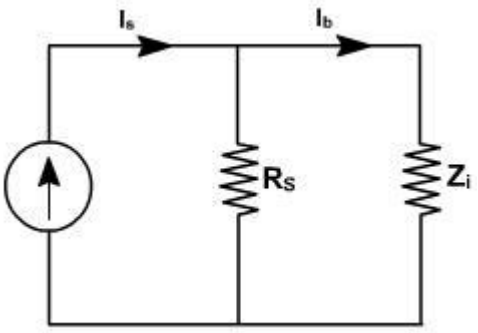


Fig. 3

In this case, overall current gain A_{IS} is defined as

$$A_{I_s} = \frac{I_L}{I_s}$$

$$= -\frac{I_c}{I_s}$$

$$= -\frac{I_c}{I_b} * \frac{I_b}{I_s} \qquad \left(I_b = \frac{I_s * R_s}{R_s + Z_i} \right)$$

$$= A_I * \frac{R_s}{R_s + Z_i}$$

$$\text{If } R_s \to \infty, \quad A_{Is} \to A_I$$