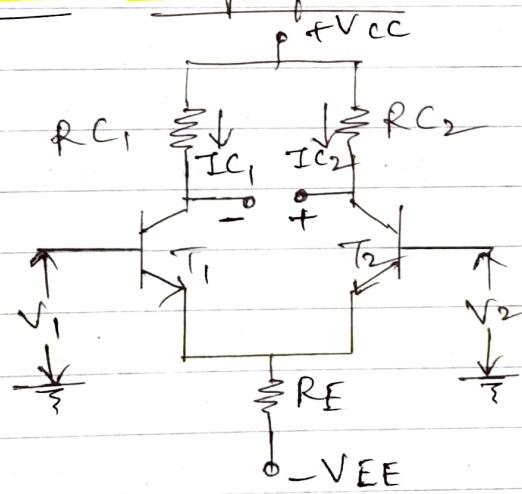


Chapter-1 Introduction to OPAMP

Clinton Jethva

- **OPAMP (Operational Amplifier).**
- An operational amplifier is direct coupled high gain amplifier usually consist of one or more differential amp & usually followed by level translator & o/p stage.
- The o/p stage is generally push-pull complementary symmetry pair. It is available as a single integrated ckt package.
- The OPAMP is versatile device that can be used to ~~not~~ amplify dc as well as ac o/p signals & was originally designed for mathematical operation such as addition, subtraction, multiplication & integration. Thus the name is Operational amp. Also log, antilog, waveform generator.

Differential Amplifier



- In Differential amp, there are two transistors, T_1 & T_2 are exactly identical, collector resistor R_C & R_{C2} are equal. Supply V_{LG} , biasing V_{EE} & Emitter resistance R_E are common for both the transistor.

➤ Case I When $V_1 = V_2 = +2V$

The base of T_1 & T_2 becomes more forward bias, so base \downarrow
amp \rightarrow Amplifier. $V_{LG} \rightarrow$ Voltage, $C/N \rightarrow$ Current

base cln of T_1 & T_2 ↑ses. Also collector cln ↑ses
∴ the vlg at collector of T_1 & T_2 ↓ses by same
amount because $V_1 = V_2$, ∴ olp vlg = 0.

→ Case 2 When $V_1 = +2V$, $V_2 = 0V$.

Then base of T_1 becomes more forward bias
so I_{B1} & I_{C1} ↑ses, ∴ V_{CE1} ↓ses. At the same time there
is no change in collector vlg of T_2 & so V_{CE2} ↑ses.

→ Case 3 When $V_1 = 0V$, $V_2 = +2V$.

Then the base of T_1 becomes less F.B. so I_{B1} &
 I_{C1} is less & ∴ V_{CE1} ↑ses. At the same time, T_2 is
more F.B. because $V_2 = +2V$, ∴ I_{B2} & I_{C2} is ↑ses
& V_{CE2} ↓ses.

& because of that olp vlg is -ve. So when V_2 is
+ve, then V_o is -ve i.e. olp vlg is inverted
hence V_2 is known as inverting terminal.

→ because T_2 is less F.B. so I_{B2} & I_{C2} ↓ses.

As we can see that when V_1 is +ve our olp is
also +ve ∴ V_1 is known as non inverting
terminal.

→ Case 4 When $V_1 = +2V$, $V_2 = -2V$.

Then T_1 becomes more F.B. ∴ I_{B1} & I_{C1} ↑ses &
 V_{CE1} ↓ses. At other side T_2 becomes less F.B.
& so V_{CE2} ↑ses & I_{B2} & I_{C2} ↓ses.

In this amplifier olp will be more when
differential ips are applied i.e. $V_o = A(V_1 - V_2)$

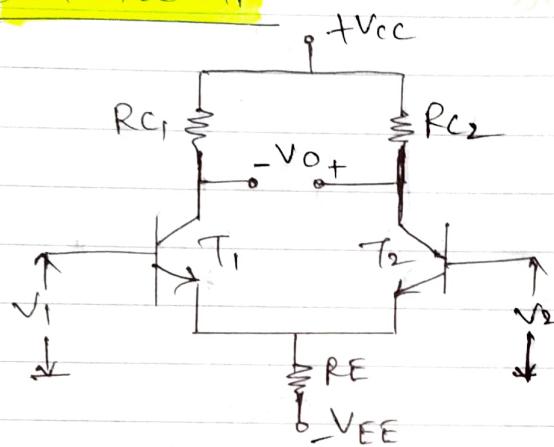
'A' is the gain of amplifier & amplifier is
known as differential amplifier.

\downarrow current ↑ses → increase, ↓ses → decrease.
F.B → forward bias.

→ Types of Differential Amplifier.

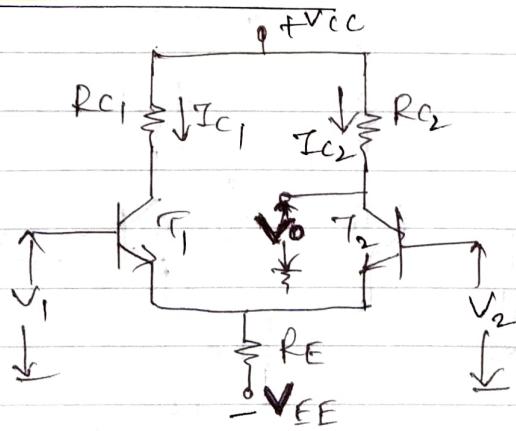
- Dual ilp balance o/p.
- Dual ilp unbalance o/p.
- Single ilp balance o/p.
- Single ilp unbalance o/p.

→ Dual ilp balance o/p.



In this type, ilp slg V_1 & V_2 are applied at the base of T_1 & T_2 & o/p is taken across the collector of both transistor. When we are connecting ilp terminal to the ground o/p is that we are getting is zero. ∴ it is known as balanced amplifier.

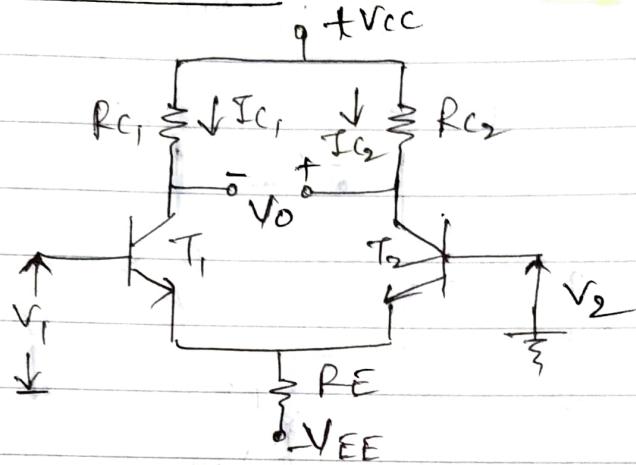
→ Dual ilp unbalance o/p



Here two ilp slgs V_1 & V_2 are applied at the slg → signal

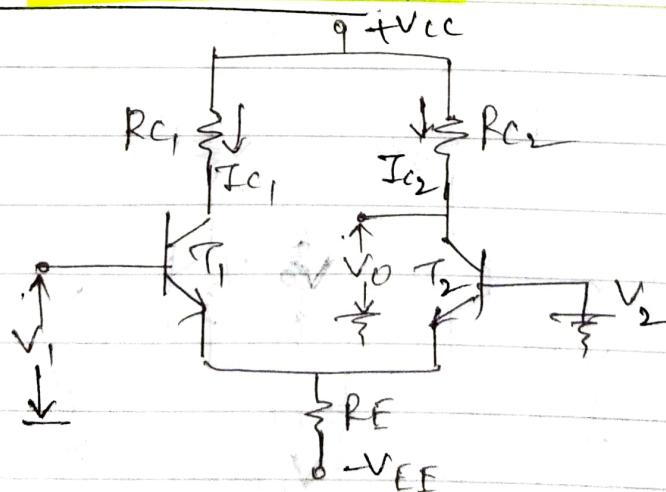
base of T_1 & T_2 , o/p is taken across the collector of T_1 or T_2 with respect to ground. When we are connecting i/p terminals to ground then there will be definite o/p. Hence it is called unbalanced differential amp.

→ Single i/p balance o/p



In this ckt, i/p is applied at the base of any one transistor & the base of other transistor is connected to ground. And the o/p is taken across the collector of both transistors, when i/p terminals are grounded, then o/p is equal to zero. \therefore it is known as balanced amplifier.

→ Single i/p Unbalance o/p



In this, i/p is applied at the base of one transistor & another base is grounded. And

→ Applications of OPAMP

Amplifier, Active filter, Arithmetic ckt's, log & antilog amplifier, comparator, waveform generator, multiplier, Timers, Multivibrator.

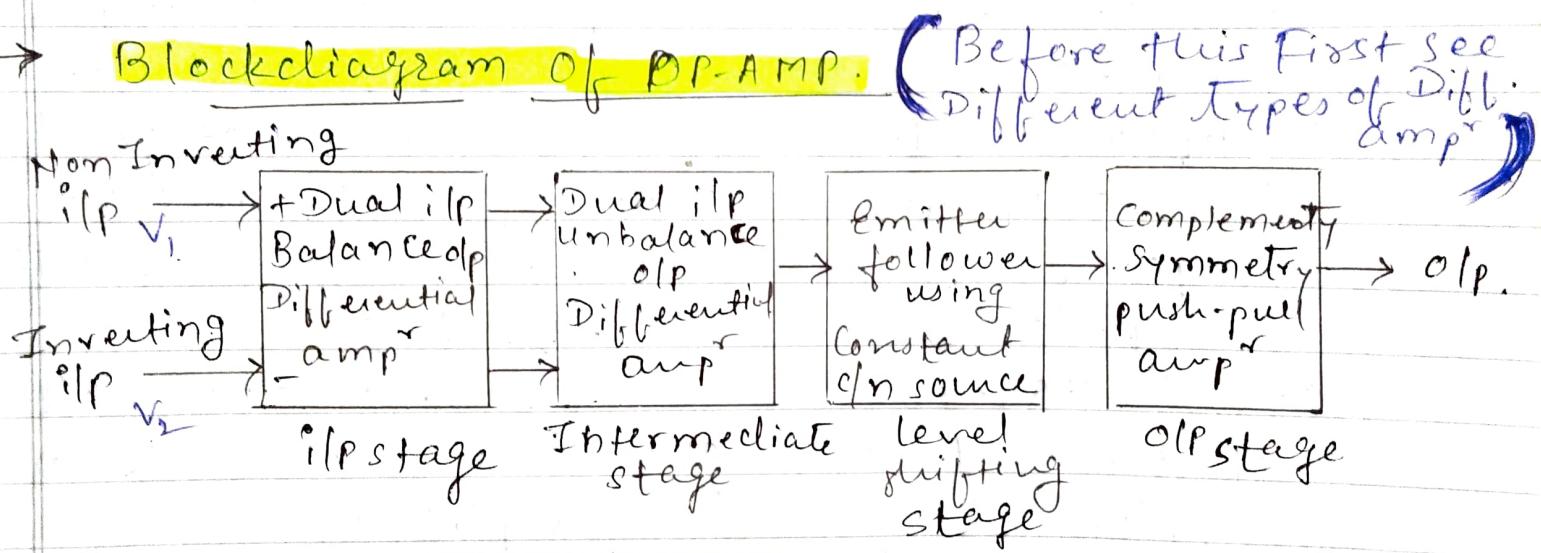
→ What is an OPAMP?

Earlier we have studied amplifier using BJT along with different components, also for high vlg. gain we require more than one amp. At it was too ~~bulky~~ we started amplifiers in IC form.

→ Advantage of OPAMP over Conventional amplifier.

Size is small, Reliability is higher, Cost is less, Easy to replace, Less power consumption.

→ Blockdiagram of OP-AMP.



Ideal Differential amp.

Its function is to amplify difference betⁿ two slgs. Here OLP vlg is directly proportional to the difference of two i/p's. ie. $V_o \propto (V_1 - V_2)$

$$\text{Differential sig. } V_{d1} = V_1 - V_2$$

$$\text{Differential gain } A_{d1} = V_o / V_{d1}$$

vlg → voltage, betⁿ → between, slg → signal.]

Common mode sig. ie. same signal is applied to both the i/p.

$$V_c = V_1 + V_2 / 2 \quad \therefore V_o = A_C \cdot V_c$$

➤ Total voltage of an Differential amp is.

$$V_o = A_D V_d + A_C \cdot V_c$$

For ideal case 'Ad' should be infinite & 'Ac' should be zero. So that o/p vlg is proportional to differential i/p sig.

But practically not possible.

➤ Explanation of Block diagram

- V_1 & V_2 are two i/p vlg applied to first stage. It is Dual i/p balance o/p differential amp. It provides necessary vlg gain & i/p resistance.
- After that it is applied to second stage which is dual i/p unbalance o/p differential amp. & the purpose is to provide additional gain. Then it is applied to level shifting stage.
- This stage shifts the dc level at the o/p of second stage to ground ie. zero volt. Then applied to push-pull amplifier.
- This stage is used to provide necessary power gain & o/p vlg & also provides low resistance.

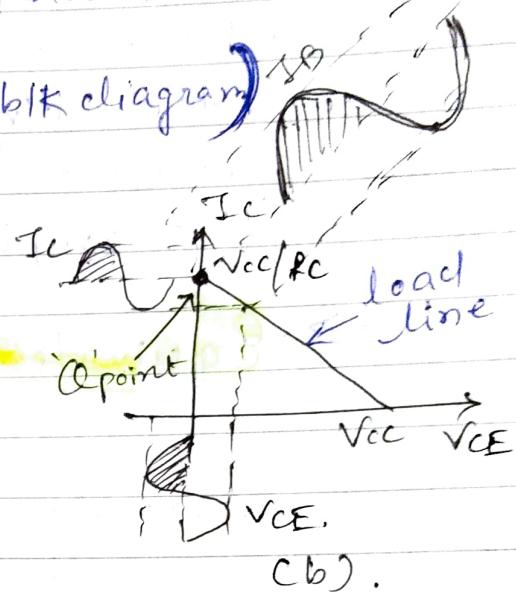
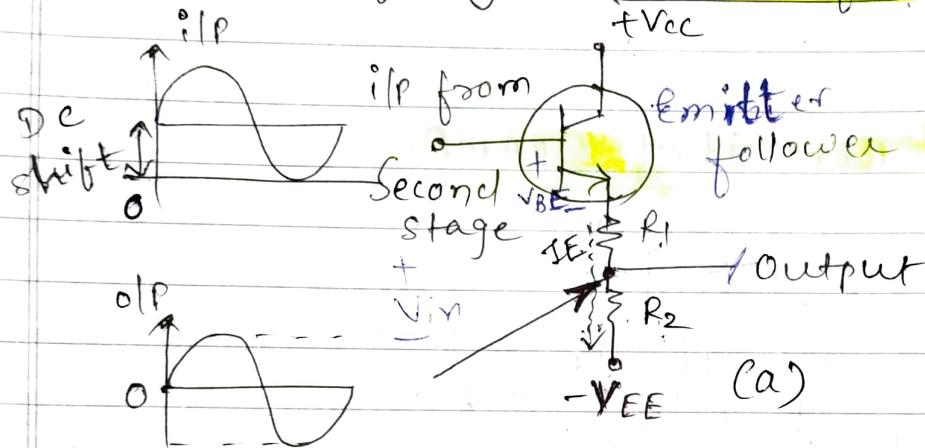
i/p \rightarrow input, o/p \rightarrow output, amp \rightarrow amplifier

\uparrow $S_{es} \rightarrow$ increases, \downarrow $S_{es} \rightarrow$ decreases.

olp is taken across the collector of T_1 or T_2 with respect to ground. When olp terminals are grounded there will be definite olp . Hence it is known as Unbalanced differential amp.

(Continue after the explanation of blk diagram)

level shifting ie. level shifter



- olp of differential amp is given to power amp but because of direct coupling the dc level at the collector of differential amp will reach the base of power amp & due to this power amp is always in Saturation. ie. power amp can't amplify the sig. See in fig. (b).
- Also the high DC level may spoil the transistor in power amplifier.

So to avoid this dc level at the collector of differential amp is shifted to zero volt. & then given to power amplifier.

- As the gain of emitter follower is approx equal to 1, there is no change in signal swing.
- Apply KVL to the base emitter loop,

$$\text{Vin} - \text{VBE} - \text{IE}R_1 - \text{IE}R_2 + \text{VEE} = 0.$$

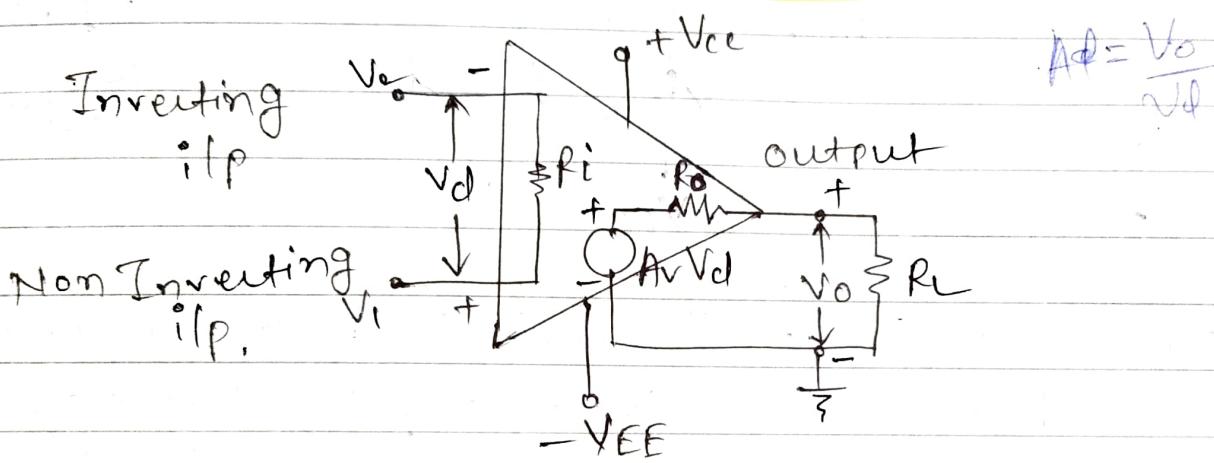
& olp vlg with respect to ground is,

$$\text{Vo} = \text{VEE} - \text{IE}R_2$$

We can adjust the value of R_1, R_2 & I_E to get a '0' dc o/p vlg.

Also we can replace R_2 by a constant c/n source & this c/n can adjust the value of I_E to get zero dc vlg at o/p. & it does not reduce the amplitude.

→ Equivalent Circuit of OPAMP.



$$A_d = \frac{V_o}{V_d}$$

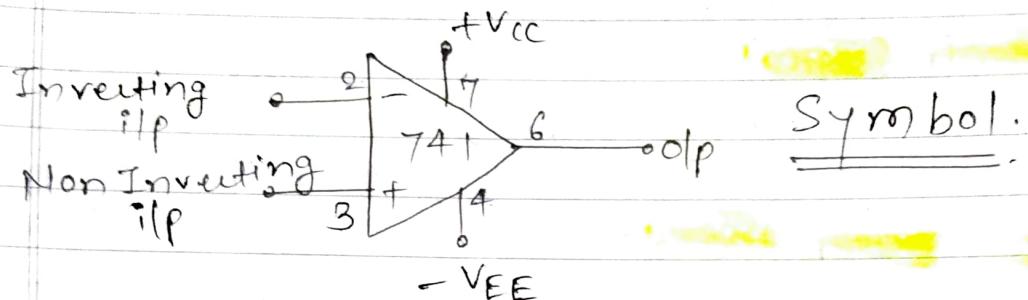
A_v = Voltage gain , V_d = Differential i/p
ie. $(V_1 - V_2)$

R_i = i/p Resistance , R_o = o/p resistance.

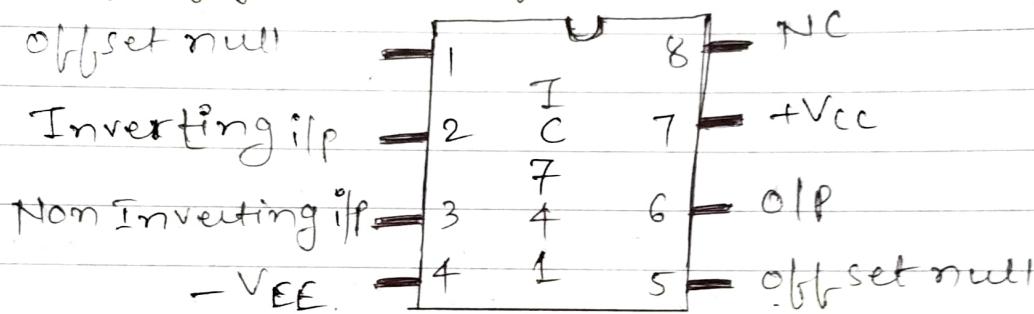
$$V_o = \text{o/p vlg} = A_v V_d \rightarrow \textcircled{A}$$

Here i/p is Double ended & o/p is single ended.
From equation \textcircled{A} it is clear that o/p vlg is directly proportional to difference of the i/p vlg's & not the only one i/p vlg. because $V_d = V_1 - V_2$. Hence OPAMP are also called as Differential amplifiers.

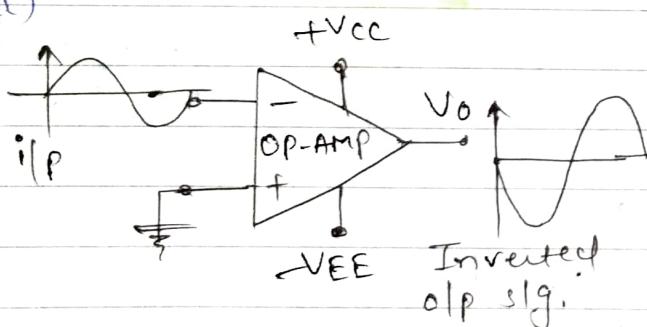
→ OPAMP IC 741



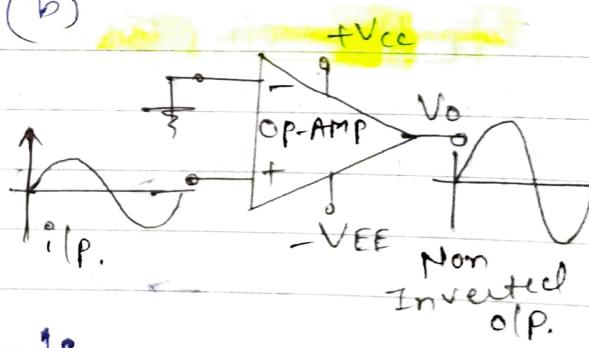
→ PIN configuration of 741



(a)



(b)



i/p & o/p slgs with 180° phase shift when the i/p sig is applied to inverting terminal

i/p & o/p slgs with 0° phase shift when i/p sig is applied to non inverting terminal.

→ OPAMP Parameters

- i) IIP offset voltage (V_{ios}) → It is the voltage that must be applied at the i/p to make o/p vlg zero. Because Ideally if i/p vlg is zero then o/p vlg should be zero but practically it is not zero.

I_{DS} value is nearly about 6mA & it is also temperature dependent.

(ii) I_D offset c/in (I_{DOS}) → It is the algebraic difference bet' the c/ins entering into the +ve & -ve i.e. inverting & non inverting terminal of opamp.

$$I_{DOS} = I_{B1} - I_{B2}$$

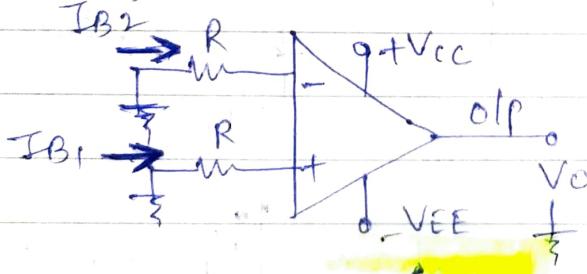
Ideally 'I_{DOS}' should be zero & practically it should be as small as possible.

I_{B1} flows into non inverting input & the I_{B2} flows into Inverting input terminal.

It is not equal because I_{B1} & I_{B2} are different from each other since transistors in OPAMP are not exactly identical. [ie. matched].

Its value is nearly about 200nA.

(iii) I_P Bias c/in (I_B) → It is the average of the c/in entering into the two o/p terminals of OPAMP.



$$I_B = I_{B1} + I_{B2} / 2$$

Ideally ~~not~~ I_{B1} & I_{B2} should be zero but practically 'R_i' is not infinite i.e. it is having some finite value & because of this I_{B1} & I_{B2} exist. Its value is 500nA.

(iv) Differential o/p resistance (R_d) →

It is also called as o/p resistance & it is the equivalent resistance which can be measured at

[bet' → between, c/in → current, +ve → positive, -ve → negative]

either the inverting or non-inverting terminal with the other terminal is connected to ground. It should be as high as possible & its value is $2M\Omega$.

(v) Input Capacitance → (i) It is the equivalent capacitance, measured at either inverting or non-inverting terminal with the other terminal connected to ground. It should be as small as possible & its value is 1.4 pF .

(vi) Input voltage range → When we apply same i/p sig at both the i/p terminal then it is known as common mode sig.

And the i/p vlg range is defined under this condition. For 741 range of i/p vlg is maximum & we can easily apply $+13V$ to $-13V$ without damaging OPAMP.

(vii) Offset voltage Adjustment Range → It is the capability to null the offset voltage.

For this potentiometer of $10k\Omega$ is connected betⁿ offset null pins '1' & '3' & the variable terminal is connected to ~~common~~ -VEE.

By varying potentiometer we can reduce o/p offset voltage. Its range is $\pm 15mV$.

(viii) Common mode Rejection ratio (CMRR) → It is the ratio of differential mode gain to common mode gain. ie. $\text{CMRR} = A_d / A_c$

It shows the capability of OPAMP to reject the common mode sig. It should be as high as possible & its value is 90 dB .

[betⁿ → between, sig → signal]

(ix) Supply voltage Rejection Ratio (SVRR) →

It is the ratio of change in i/p offset vlg (ΔV_{ios}) ~~due to~~ to variation in the supply vlg.

$$SVRR = \frac{\Delta V_{ios}}{\Delta V}$$

ΔV_{ios} → change in i/p offset vlg.

ΔV → change in Supply vlg.

It is measured in mV per volt or in decibels.

It should be as small as possible, ~~FET~~ ^{so as to} ~~possible~~ ^{small}.

(x) Large slg. voltage Gain → It is given as,

$$\text{Voltage Gain} = \frac{\text{O/P voltage}}{\text{Differential i/p vlg.}}$$

$$\text{i.e. } A_v = \frac{V_o}{V_{in}}$$

As ' V_o ' is larger than ' V_d ' thus vlg gain is called large slg vlg gain. $A_v = 2 \times 10^5$

(xi) Supply Voltage → Some OPAMP uses dual power supply & some use single polarity supply vlg.

Dual supply is equal to $\pm 15\text{V}$ & single polarity supply vlg is $+12\text{V}$ ~~or~~ 15V .

(xii) Supply current → I_s is defined as the current drawn by the OPAMP from power supply. Its value is 2 to 3 mA.

(xiii) Output Resistance (R_o) → It is the resistance measured by looking into the o/p terminal of OPAMP, with the i/p ^{source} ~~feedback~~ short ckted. R_o should be as small as possible. Its value for 741 75Ω .

Ckt → circuit

Clinton Jethva

OP voltage swing \rightarrow Maximum +ve or -ve op vlg of OPAMP is called as Saturation vlg.

$$V_{o(max)} = \pm V_{sat}$$

Typically $V_{sat} = 0.9 V_{cc}$, $-V_{sat} = -0.9 V_{cc}$

If the supply vlg $\pm 15V$ then $V_o(max) = \pm 13V$
Output vlg swing is defined as the difference bet' $+V_{sat}$ & $-V_{sat}$. So typically vlg swing is 26V.

Slew rate \rightarrow It is defined as the maximum rate of change of op vlg per unit time & it is expressed in Volts per microsecond.

$$SR \rightarrow \frac{dV_o}{dt} \text{ Volts/microsec.}$$

It decides the capability of OPAMP to change its op rapidly, hence it decides the frequency of operation.

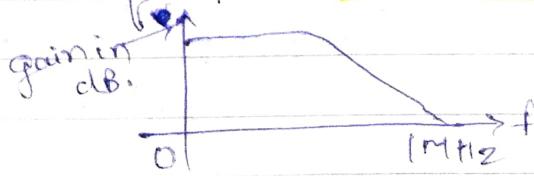
It changes with change in vlg gain \therefore generally specified at unity (1) gain.

It should be as high as possible. Its value is nearly about 0.5V/microsec.

Bandwidth \rightarrow It is the frequency range of an amp over which all the vlg frequencies are amplified equally.

It should be as high as possible & it is nearly about 1MHz.

Gain Bandwidth product \rightarrow GBP product is the Bandwidth of OPAMP when vlg gain is 1.



[\therefore \rightarrow Therefore, bet' \rightarrow between, Amp \rightarrow Amplifier]

(xviii) Opamp short circuit cfn \rightarrow opamp o/p ~~shorted never~~
be short circuited to ground because then
large uncontrolled output cfn would flow
& damage the opamp.

To avoid this, in built short ckt protection ckt
is provided to limit this cfn.

opamp short ckt cfn is the value of ~~the~~ opamp cfn
that is allowed to flow by internal short
ckt protection ckt, if opamp is shorted to ground.
'Isc' Its typical value is 25mA.

→ Ideal OPAMP electrical Characteristic

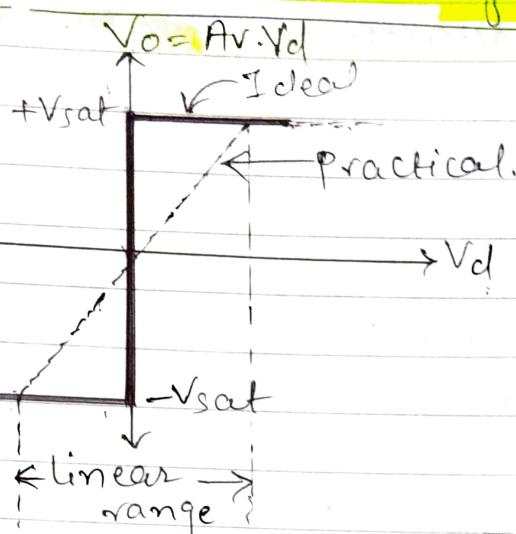
- i) Voltage gain is Infinite ie. $A_v = \infty$
- ii) Infinite i/p resistance ie. $R_i = \infty$
So that I_{B1} & I_{B2} becomes zero.
- iii) o/p resistance is zero, ie. $R_o = 0$.
So that it can drive infinite no. of other devices.
- iv) Zero offset vlg. It means o/p vlg is zero when
input voltage is zero.
- v) Infinite Bandwidth, so that it can amplify
all sig frequencies from the range 0 to ω ~~with~~
equally.
- vi) Infinite CMRR., It means common mode
sig gain is zero.
- vii) Infinite Slew rate, So that opamp vlg changes
occur simultaneously with the i/p vlg changes.
- viii) SVRR is zero, It means opamp vlg does not change
with the variation in supply.

[cfn \rightarrow current, ckt \rightarrow circuit, no.of \rightarrow Number
of]

$$V_o = A_v V_d$$

Clinton Tetiva

→ Voltage Transfer characteristics of OPAMP.



- Voltage transfer curve or characteristics of an OPAMP is graph of its o/p vlg versus i/p vlg \$V_{in}\$. i.e. On x-axis \rightarrow Differential i/p vlg (\$V_d\$) & on y-axis \rightarrow o/p vlg (\$V_o\$).

$$V_o = A_v \cdot V_d$$

- Maximum value of o/p vlg is \$V_{omax} = \pm V_{sat}\$ & \$V_{sat}\$ is called as saturation voltage.
- As the o/p vlg cannot exceed +ve & -ve saturation vlg. & we are keeping gain as constant. i.e. \$A_v\$ The saturation vlg is defined by the o/p vlg swing.
- So the o/p vlg is directly proportional to the i/p difference voltage only until the saturation vlg.
- After reaching at saturation vlg o/p vlg remains constant.

In figure ideal & practical voltage transfer characteristics is shown.

[+ve \rightarrow positive, -ve \rightarrow Negative, vlg \rightarrow voltage]

<u>Characteristics</u>	<u>Value for 741 IC</u>	<u>Ideal Value</u>
R_i	$2M\Omega$	∞
R_o	75Ω	0
A_v	2×10^5	∞
Bandwidth	1MHz	∞
CMRR	90dB	∞
Stew rate	0.5V/msec	∞
I/p offset vlg.	6mV	0
SVRR	150mV/V	0
I/p bias c/n	500nA	0
I/p offset c/n.	200nA	0

⇒ Features of IC741

- ⇒ No external frequency compensation required
- ⇒ Short ckt protection is provided.
- ⇒ Offset null capability.
- ⇒ Large Common mode & differential vlg range.
- ⇒ Low power consumption.

5) Thermal Drift :-

- The values of V_{IB} , I_B & I_{IO} vary with,
 - i> change in temperature
 - ii> change in supply voltages : +V_{CC} & -V_{EE}
 - iii> Time
- most affecting factor is temperature.
- Thermal drift :-

The average rate of change of IIP offset voltage per unit change in temperature is called thermal voltage drift & is denoted by $\Delta V_{IO} / \Delta T$. It is expressed in $\mu V / ^\circ C$.

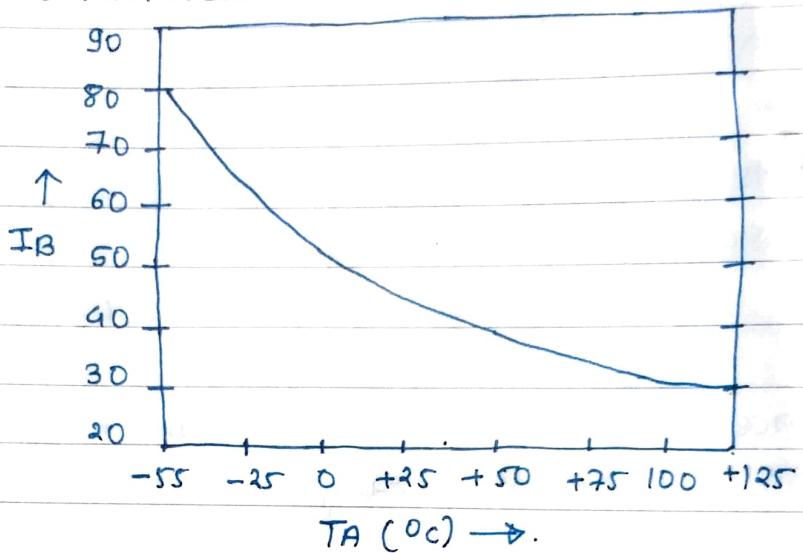
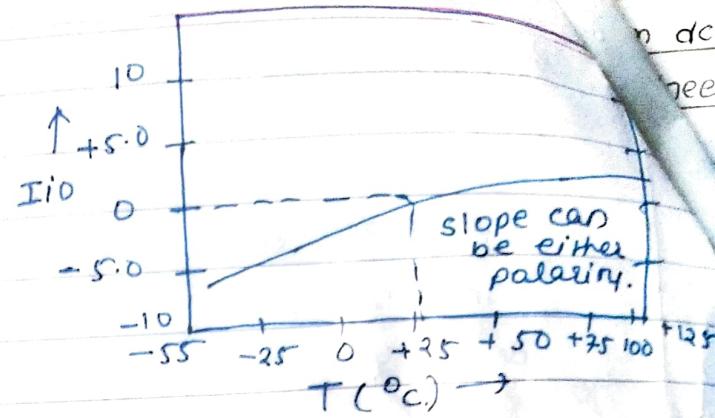
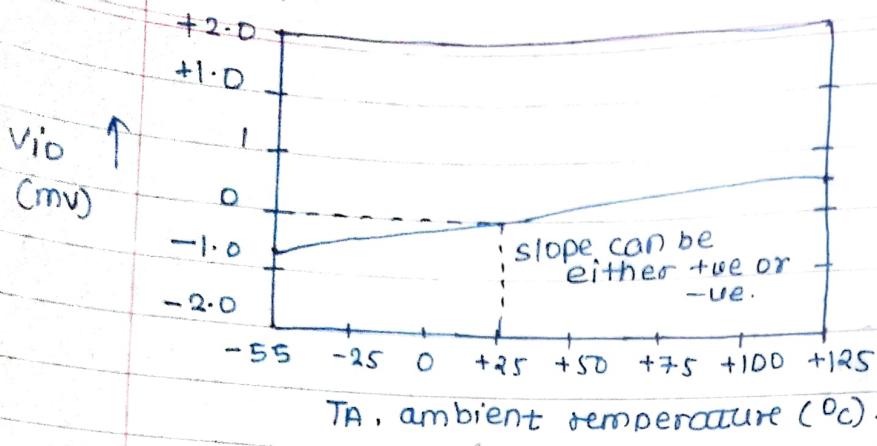
We can also define thermal drift as,

$$\frac{\Delta I_{IO}}{\Delta T} = \text{thermal drift in the IIP offset current } (\mu A / ^\circ C)$$

= thermal current drift.

$$\frac{\Delta I_B}{\Delta T} = \text{thermal drift in the IIP bias current. } (\mu A / ^\circ C).$$

$$\frac{\Delta V_{IO}}{\Delta T} = \text{thermal voltage drift. , } \frac{\Delta \Delta I_{IO}}{\Delta T} = \text{thermal current drift.}$$



* Effect of variation in power supply voltages on offset voltage:-

- most serious variation in values of V_{IO} & I_B & I_{IO} is due to change in temp.
- from graph we can observe that the manufacturer has consider V_{IO} & I_{IO} values 0 at room temp. i.e $25^{\circ}C$.
- To calculate thermal drift we can find ΔT & ΔV_{IO} or ΔI_{IO} , as,

$$\frac{\Delta V_{IO}}{\Delta T} = \text{Thermal vrg. drift} \quad \& \quad \frac{\Delta I_{IO}}{\Delta T} = \text{Thermal current drift.}$$

- But this is time consuming process. so some manufacturers specify No avg. value of the drift in offset vrg. & offset current over an entire operating temp. range instead.
- these values are indicated as absolute values i.e it may be +ve or -ve.

Analysis of differential amp^r using FETs:-

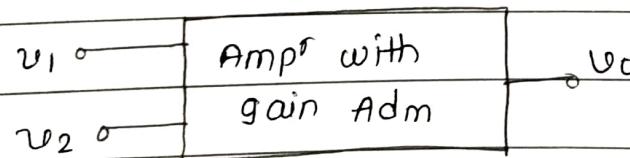
- Amplifies difference betⁿ two signals.
- In many physical measurements, where response from dc to many MHz of freqⁿ is required, which give rise to need of differential amp^r. This forms basic IIP stage of an integrated amp^r.

Properties of differential amp^r :-

1. excellent stability
2. high versatility &
3. high immunity to interference signals.

Advantages of diffⁿ amp^r :-

1. Lower cost.
 2. easier fabrication as IC component & .
 3. Closely matched components.
- Basic Block dia of diffⁿ amp^r :-



$$v_0 = \text{Adm} [v_1 - v_2]$$

If $v_1 = v_2$, $v_0 = 0$ Hence v_0 is obtained when $v_1 \neq v_2$.

The difference mode IIP utg. is defined as,

$$v_{dm} = [v_1 - v_2]$$

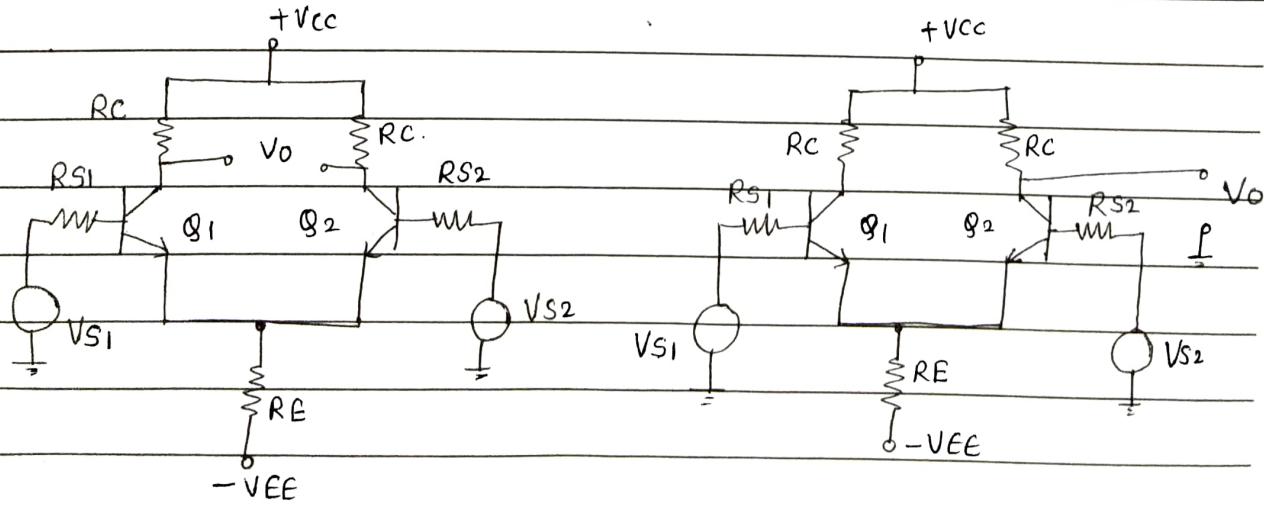
& the common mode input voltage is defined as,

$$v_{cm} = \left[\frac{v_1 + v_2}{2} \right]$$

- In practice, common mode input signal affects the OIP. While designing diffn amp^r, main aim is to minimise the effect of common mode input signal.
- Features of Differential amp^r :-
- High differential gain & low common mode gain.
- High common mode Rejection Ratio (CMRR).
- High IIP impedance
- Low OIP impedance.
- High gain
- Large Bandwidth.

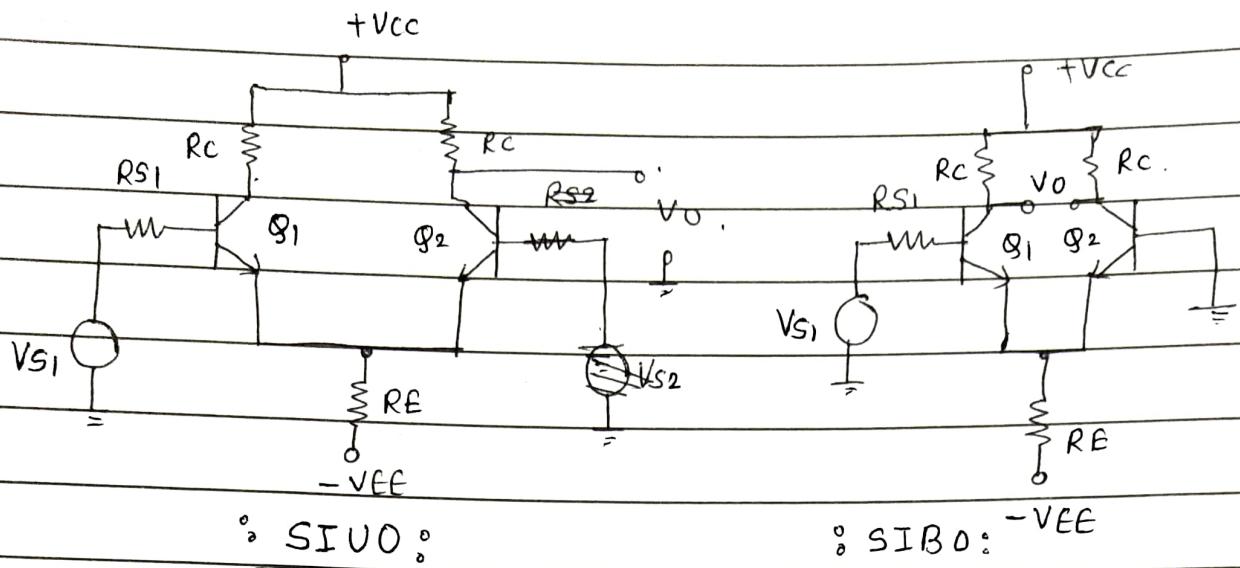
* Differential Amp^r. configurations using BJT:-

- Uses 2 transistors. Depending on connecting IIP to them & the way of measuring OIP, there are 4 config. of a diffn amp^r.
- 1. Dual IIP, balanced OIP diffn amp^r
- 2. Dual IIP, unbalanced OIP diffn amp^r
- 3. Single IIP, balanced OIP diffn amp^r.
- 4. Single IIP, unbalanced OIP diffn amp^r.



: DIBO .

: DIUO :



* Differential Amp^r using BJT:-

Diffⁿ amp^r with resistive loading

-BJT

-JFET

-MOSFET

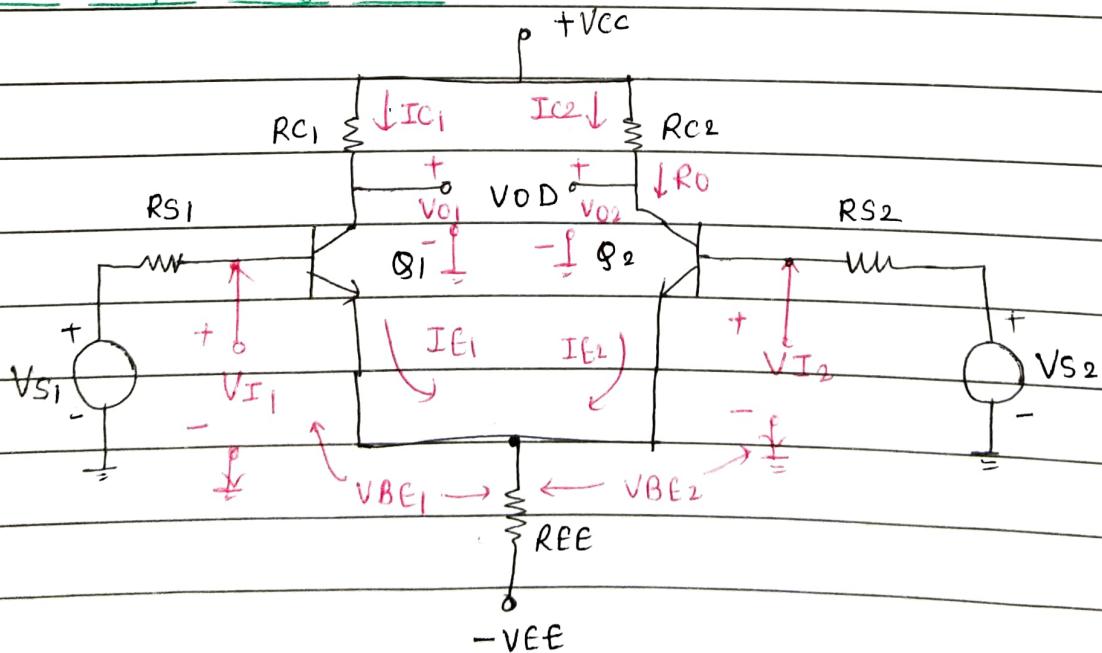
Diffⁿ amp^r with active loading

-BJT

-JFET

-MOSFET.

1. DIFFⁿ amp^r using BJT:-



\therefore Emitter - Coupled Differential amp^r :-

- Emitter coupled or source coupled diffⁿ amp forms the IP stage of most analog ICs. The performance of diffⁿ amp depends on the ideal matching characteristics of the transistor pair Q_1 & Q_2 .

• DC Analysis :-

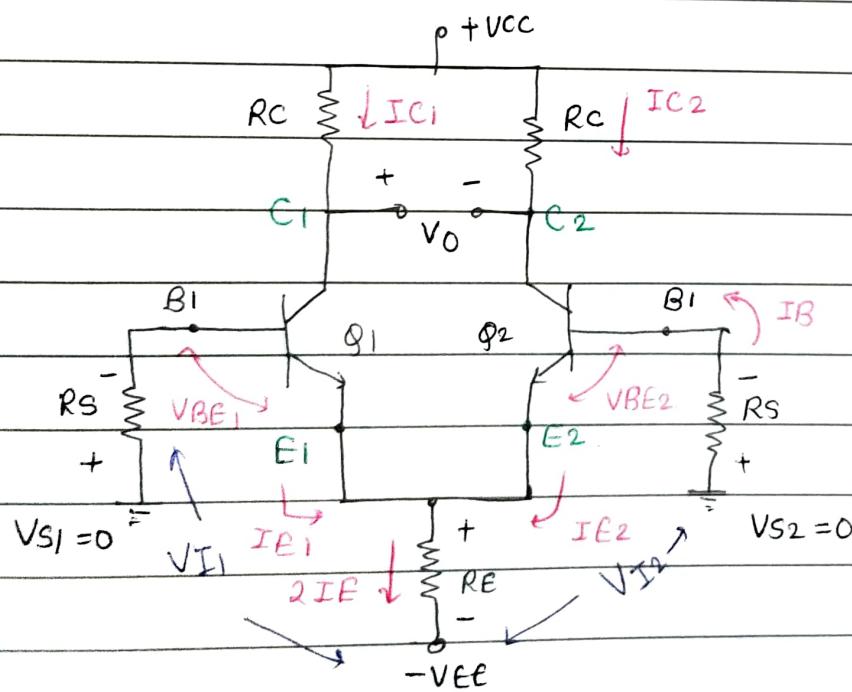
Let Q_1 & Q_2 are ideally matched, & the mismatching effects will be considered later. Also consider $B \gg 1$ so that, [$B = \frac{I_C}{I_B}$ -- current gain]

$$IE_1 \approx IC_1 \text{ & } -IE_2 \approx IC_2$$

$$\therefore V_{I1} = V_{BE1} - V_{BE2} + V_{I2}. \quad \dots \textcircled{1} \quad [V_{I1} - V_{BE1} = V_{I2} - V_{BE2}]$$

In DC analysis, co-ordinates of operating pt are obtained i.e V_{CQ} & V_{CEQ} for both Q_1 & Q_2 .

I) Draw DC equivalent ckt. (make $V_{S1} = V_{S2} = 0$).



For matched or identical transistor pair, we have.

$$R_E = R_{E1} \parallel R_{E2}, \text{ since } R_{E1} = R_{E2}.$$

$$R_{C1} = R_{C2} = R_C$$

$$|V_{CC}| = |V_{EE}|$$

} ... \textcircled{2}

For symmetrical ckt with matched transistors, $|IC_{1Q}| = |IC_{2Q}|$ &

$|V_{CE1Q}| = |V_{CE2Q}|$. Hence we can find operating point.

from fig, Apply KVL to base-emitter loop of Q₁, we get

$$I_B R_S + V_{BE} + 2 I_E R_E = V_{EE}$$

As $\beta = \frac{I_C}{I_B}$ for CE configuration & $I_C \approx I_E$, $\beta = \frac{I_E}{I_B}$

$$\therefore I_B = \frac{I_E}{\beta}$$

$$\therefore I_E R_S + V_{BE} + 2 I_E R_E = V_{EE}$$

$$I_E \left[\frac{R_S}{\beta} + 2 R_E \right] = V_{EE} - V_{BE}$$

$$I_E = \frac{V_{EE} - V_{BE}}{\left[\frac{R_S}{\beta} + 2 R_E \right]}$$

Practically, $\frac{R_S}{\beta} \ll 2 R_E$.

$$\therefore I_E = \frac{V_{EE} - V_{BE}}{2 R_E} \quad \dots \textcircled{3}$$

from above eqⁿ, it can be inferred that,

(i) for a known value of V_{EE}, the I_E of Q₁ & Q₂ are determined by R_E.

(ii) The emitter current, I_E is independent of R_C when I_E >> I_C. Neglecting drop ac & applying KVL to the C-B loop, we get,

$$V_C = V_{CC} - I_C R_C$$

$$\& V_{CE} = V_C - V_E$$

$$= V_{CC} - I_C R_C - V_E$$

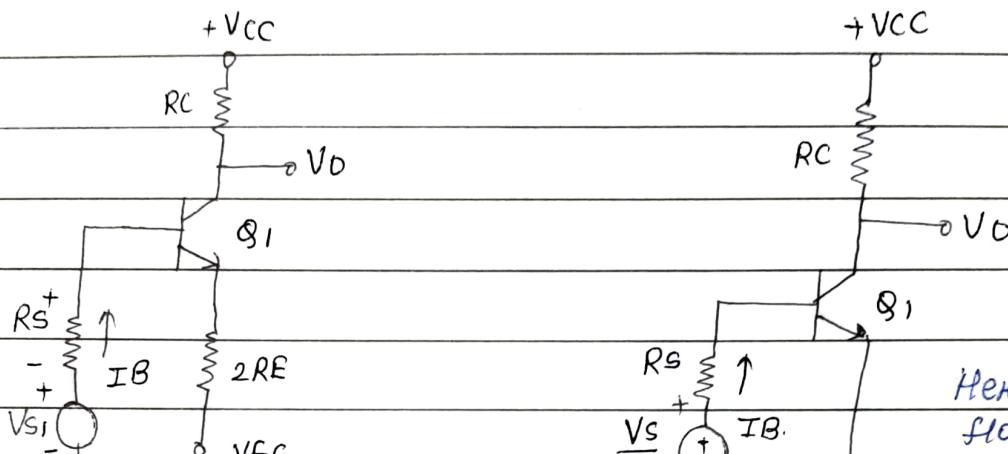
But V_E = -V_{BE} (vtg. at the emitter of Q₁).

$$\text{Thus, } V_{CE} = V_{CC} - I_C R_C + V_{BE}$$

The above eqⁿ gives $V_{CEQ} = V_{CE}$ when $I_E \approx I_C = I_{CQ}$, for the given values of V_{CC} & V_{EE}.

- AC analysis of an emitter-coupled pair:-

The symmetrical ckt. split into two equivalent circuits as shown below for AC analysis.



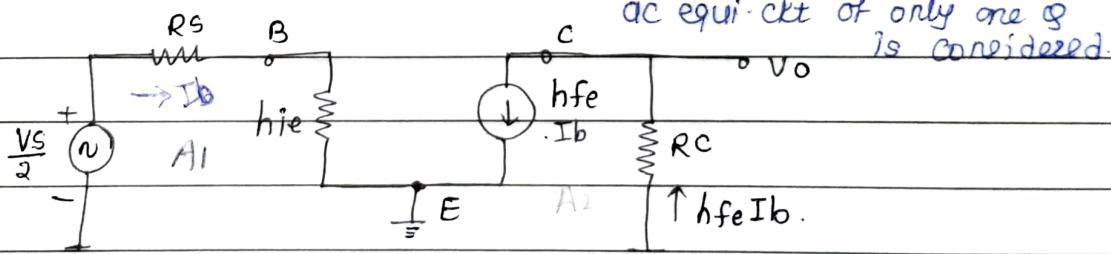
a] for ACM analysis.

b] for Adm analysis.

- Differ mode gain (Adm):-

for analysis, let that two IPs = $V_s/2$ & 180° phase shifted. (b)

[In fig. a. since $I_{E1} = I_{E2}$ & they are out of phase, they cancel each other]. The ac equi. ckt is, As two transistors are matching.



\therefore Approx. hybrid model neglecting hoe :-

Apply KVL to the input loop A1, we get

$$I_b (R_s + h_{ie}) = V_s/2$$

$$\therefore I_b = \frac{V_s}{2(R_s + h_{ie})} \quad \dots \textcircled{1}$$

Apply KVL to A2, V_o is

$$V_o = -h_{fe} \cdot I_b \cdot R_c \quad \text{substitute value of } I_b \text{ from eqn } \textcircled{1}$$

$$\therefore V_o = -h_{fe} \cdot R_c \cdot \frac{V_s}{2(R_s + h_{ie})} \quad \dots \textcircled{2}$$

$$\therefore \frac{V_o}{V_s} = -\frac{h_{fe} \cdot R_c}{2(R_s + h_{ie})}$$

(- sign indicates 180° phase bet'n V_o & V_s)

magnitude of $I_{IP} = V_s/2$ (180°).

$$\therefore V_{id} = \frac{V_s}{2} - \left(-\frac{V_s}{2} \right) = V_s \quad \dots \text{(3)}$$

$$\therefore A_{dm} = \frac{V_o}{V_{id}} = \frac{V_o}{V_s} = -\frac{h_{fe} \cdot R_c}{2(R_s + h_{ie})} \quad \begin{matrix} \text{--- w.r.t ground} \\ (\text{unbalanced}) \end{matrix}$$

where V_s = differential IIP vrg.

$$\text{For balanced oip, } A_{dm} = -\frac{h_{fe} \cdot R_c}{2(R_s + h_{ie})} = -\frac{h_{fe} \cdot R_c}{(R_s + h_{ie})}$$

common mode gain (A_{cm}):-

- For common mode analysis, consider that the IIP signals have same magnitude V_s & are in phase.

$$\therefore V_{ic} = \frac{V_1 + V_2}{2} = \frac{V_s + V_s}{2} = V_s.$$

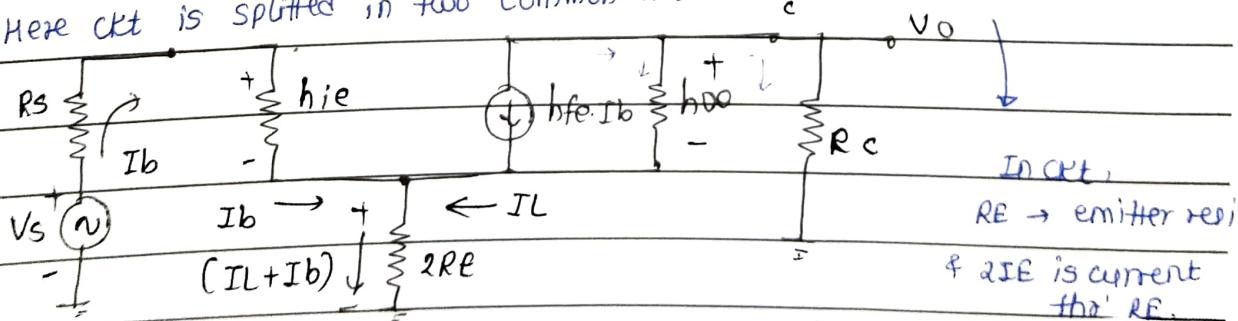
$$\text{we know that } V_o = A_{cm} \cdot V_s \quad \therefore A_{cm} = V_o/V_s.$$

Here consider emitter current for analysis.

- current thr' RE is $\approx I_E$. Emitter resi is assumed to be ~~be~~ $2RE$ & emitter current to be I_E instead of $\approx I_E$ as shown.

The h-model is as below:

Here ckt is splitted in two common mode half ckt's.

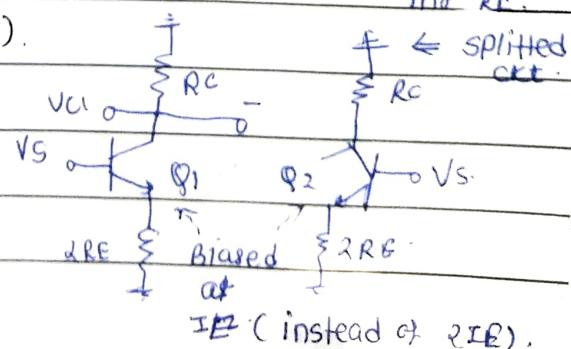


current thr' $R_C = I_L$ (load current).

effective emitter resi = $2RE$

current thr' emitter resi = $I_L + I_B$.

current thr' $h_{oe} = (I_L - h_{fe} \cdot I_B)$



Apply KVL to input side.

$$I_b R_s + I_b h_{ie} + 2R_E (I_L + I_b) = V_S$$

$$\therefore V_S = I_b (R_s + h_{ie} + 2R_E) + I_L (2R_E) \rightarrow A$$

$$\therefore V_O = -I_L R_C \rightarrow B$$

As in dc analysis, let us now apply KVL to o/p loop.

$$I_L R_C + 2R_E (I_L + I_b) + \frac{(I_L - h_{fe} \cdot I_b)}{h_{oe}} = 0$$

$$\text{i.e. } I_L R_C + 2R_E I_L + 2R_E I_b + I_L - \frac{h_{fe} \cdot I_b}{h_{oe}} = 0$$

$$\therefore I_b \left[\frac{2R_E - h_{fe}}{h_{oe}} \right] + I_L \left[R_C + 2R_E + \frac{1}{h_{oe}} \right] = 0$$

$$\text{i.e. } I_L \left[R_C + 2R_E + \frac{1}{h_{oe}} \right] = -I_b \left[\frac{2R_E - h_{fe}}{h_{oe}} \right]$$

$$\text{i.e. } \frac{I_L}{I_b} = \frac{\left[\frac{h_{fe}}{h_{oe}} - 2R_E \right]}{\left[R_C + 2R_E + \frac{1}{h_{oe}} \right]} = \frac{h_{fe} - 2R_E h_{oe}}{1 + h_{oe} (2R_E + R_C)}$$

$$\therefore I_b = I_L \frac{[1 + h_{oe} (2R_E + R_C)]}{h_{fe} - 2R_E h_{oe}}$$

From A \rightarrow i.e. $V_S = I_L [1 + h_{oe} (2R_E + R_C)] (R_s + h_{ie} + 2R_E) + I_L (2R_E)$.

$$\frac{V_S}{I_L} = \frac{[1 + h_{oe} (2R_E + R_C)] [R_s + h_{ie} + 2R_E] + 2R_E}{[h_{fe} - 2R_E h_{oe}]}$$

$$= \frac{[1 + h_{oe} (2R_E + R_C)] (R_s + h_{ie} + 2R_E) + 2R_E (h_{fe} - 2R_E h_{oe})}{[h_{fe} - 2R_E h_{oe}]}$$

Simplify, we get

$$\frac{V_S}{I_L} = h_{oe} \cdot R_C [R_s + h_{ie} + 2R_E] + 2R_E (1 + h_{fe}) + R_s (1 + 2R_E h_{oe}) + h_{ie} (1 + 2R_E h_{oe})$$
$$(h_{fe} - 2R_E h_{oe}).$$

Rearranging terms,

$$\frac{V_S}{I_L} = \frac{h_{oe} \cdot R_C (R_s + R_s + h_{ie}) + 2R_E (1 + h_{fe}) + (R_s + h_{ie}) (1 + 2R_E h_{oe})}{(h_{fe} - 2R_E h_{oe})}$$

Practically $h_{oe} R_C \ll 1$

$$\frac{V_S}{I_L} = \frac{2R_E(1+h_{fe}) + (R_S + h_{ie}) + (1+2R_E h_{oe})}{(h_{fe} - 2R_E h_{oe})}$$

so m(B) $\therefore A_{cm} = \frac{V_O}{V_S} = \frac{-I_L \cdot R_C}{2R_E} = \frac{-(h_{fe} - 2R_E h_{oe}) \cdot R_C}{2R_E(1+h_{fe}) + (R_S + h_{ie}) (1+2R_E h_{oe})}$

$$= \frac{R_C (2R_E h_{oe} - h_{fe})}{2R_E (1+h_{fe}) + (R_S + h_{ie}) (1+2R_E h_{oe})}$$

Generally h_{oe} is neglected in practical terms.

$$\therefore A_{cm} = \frac{-R_C \cdot h_{fe}}{R_S + h_{ie} + 2R_E (1+h_{fe})}$$

same for both balanced & unbalanced OIPs.

• CMRR :-

- Diffⁿ ampr is set to operate in common mode config. (when $U_1 = U_2$)
- To cancel noise signal which appears as a common IIP to IIP terminals.
- Fig. of merit \rightarrow CMRR \rightarrow define ability of diffⁿ amp^r to reject the common-mode input signal.
- This is the ratio of diffⁿ utg. gain to common-mode utg gain A_{cm}

$$CMRR = 20 \log \left| \frac{A_{dm}}{A_{cm}} \right| dB$$

- For ideal diffⁿ ampr, $A_{cm} = 0 \therefore CMRR = \infty$.

Practically, $A_{dm} > A_{cm}$, CMRR is high, though finite.

$$\therefore V_O = A_{dm} \cdot V_{id} + A_{cm} \cdot V_{ic}$$

$$= A_{dm} \cdot V_{id} \left[1 + \frac{A_{cm} V_{ic}}{A_{dm} V_{id}} \right]$$

$$= A_{dm} V_{id} \left[1 + \frac{1}{(A_{dm}/A_{cm})} \frac{V_{ic}}{V_{id}} \right]$$

$$\therefore V_o = \text{Adm. Vid} \left[1 + \frac{1}{\text{CMRR}} \frac{V_{ic}}{\text{Vid}} \right]$$

where CMRR is not expressed in dB. As $\text{CMRR} \rightarrow \infty$
 $V_o = \text{Adm. Vid.}$

Here common mode voltage is nullified to a greater extent.
 for a balanced case, substituting the results of Adm &
 ACM, we get

$$\text{CMRR} = 20 \log_{10} \left| \frac{R_s + h_{ie} + 2RE(1+h_{fe})}{R_s + h_{ie}} \right| \text{dB.}$$

& for an unbalanced OIP,

$$\text{CMRR} = 20 \log_{10} \left| \frac{R_s + h_{ie} + 2RE(1+h_{fe})}{2(R_s + h_{ie})} \right| \text{dB.}$$

• IIP impedance R_i :-

Equivalent resi. existing betw any one of the inputs & the ground, when the other input is grounded.

$$R_i = \frac{V_s}{I_b}$$

for a single IIP, $R_i = R_s + h_{ie}$

for dual IIP circuits, $R_i = 2(R_s + h_{ie})$.

R_i is not depending on whether OIP is balanced or unbalanced.

• OIP impedance R_o :-

equivalent resi existing betw any one of the outputs & ground.

from fig.

$$R_o = R_C$$

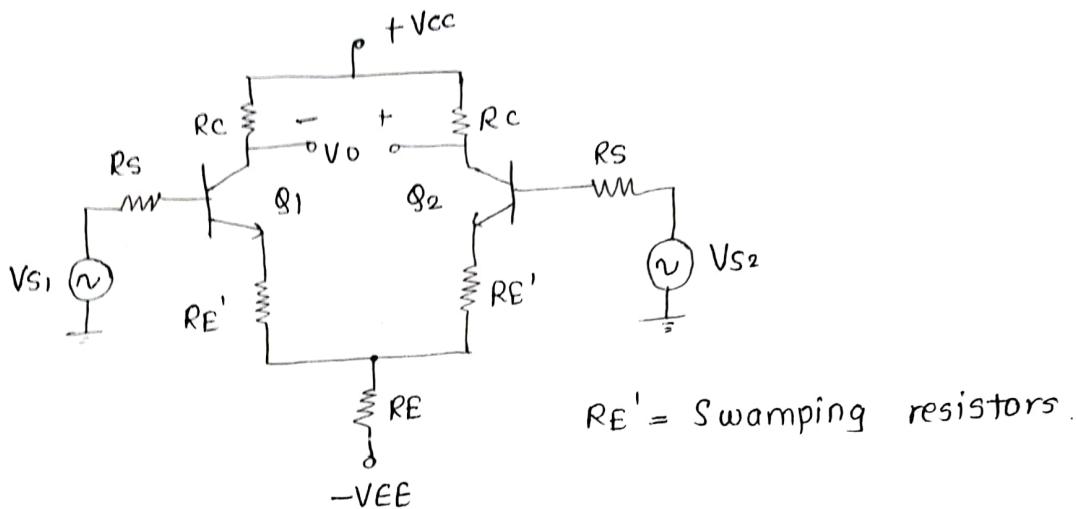
$A_{cm} \downarrow$ as $R_o \downarrow$ $\therefore \text{CMRR} \uparrow$ as $R_o \uparrow$

Effect of swamping Resistor on diff' n amplifier:-

Voltage gain of a differential amp^r is dependent on the values of h-parameter. Hence with change in the values of h-parameters due to factors such as temperature, the vtg. gain will change.

↳ To ↑ dependence of A_v

External resistor R_E' is connected in series with each emitter.



: DIBO Diff' n amp^r with swamping Resistors :

- This resistor is called as swamping resistors as they swamp the effect of change in the h-parameters. They also increase the linearity range of the differential amp^r.

Effects of swamping Resistors :-

1. The Q point gets shifted & needs to be readjusted.
2. The differential gain reduces substantially.
3. There is a considerable ↑ in the IIP resistance.

$$A_d = \frac{R_C}{r_e} \text{ (without } R_E') , \quad A_d = \frac{R_C}{r_e + R_E'} \text{ (with } R_E')$$

$$\rightarrow R_i = 2\beta r_e \text{ (without } R_E') , \quad R_i = 2\beta(r_e + R_E') \text{ (with } R_E')$$

$$\rightarrow I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E + R_E'} \text{ (with } R_E') , \quad I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E} \text{ (without } R_E')$$