* Thermal Considerations & Power Transistor:-

- class C power amplifier should conduct for less than ½ cycle so Q point for transistor is selected below the cut off region.
- To operate the transistor below the cut off region, a voltage $-V_{BB}$ is applied to the base of NPN transistor, which will make BE junction reverse biased up to V_{BB}.
- During +ve half cycle, without V_{BB} BE junction will become forward biased.

  But as we are applied $-V_{BB}$ to base, during +ve half cycle, of I/P signal the base emitter junction will remain reverse biased (off), till V_{BB}.
- Whenever $V_i > V_{BB}$, BE junction will be F.Bed & we are getting +ve pulse at O/P.

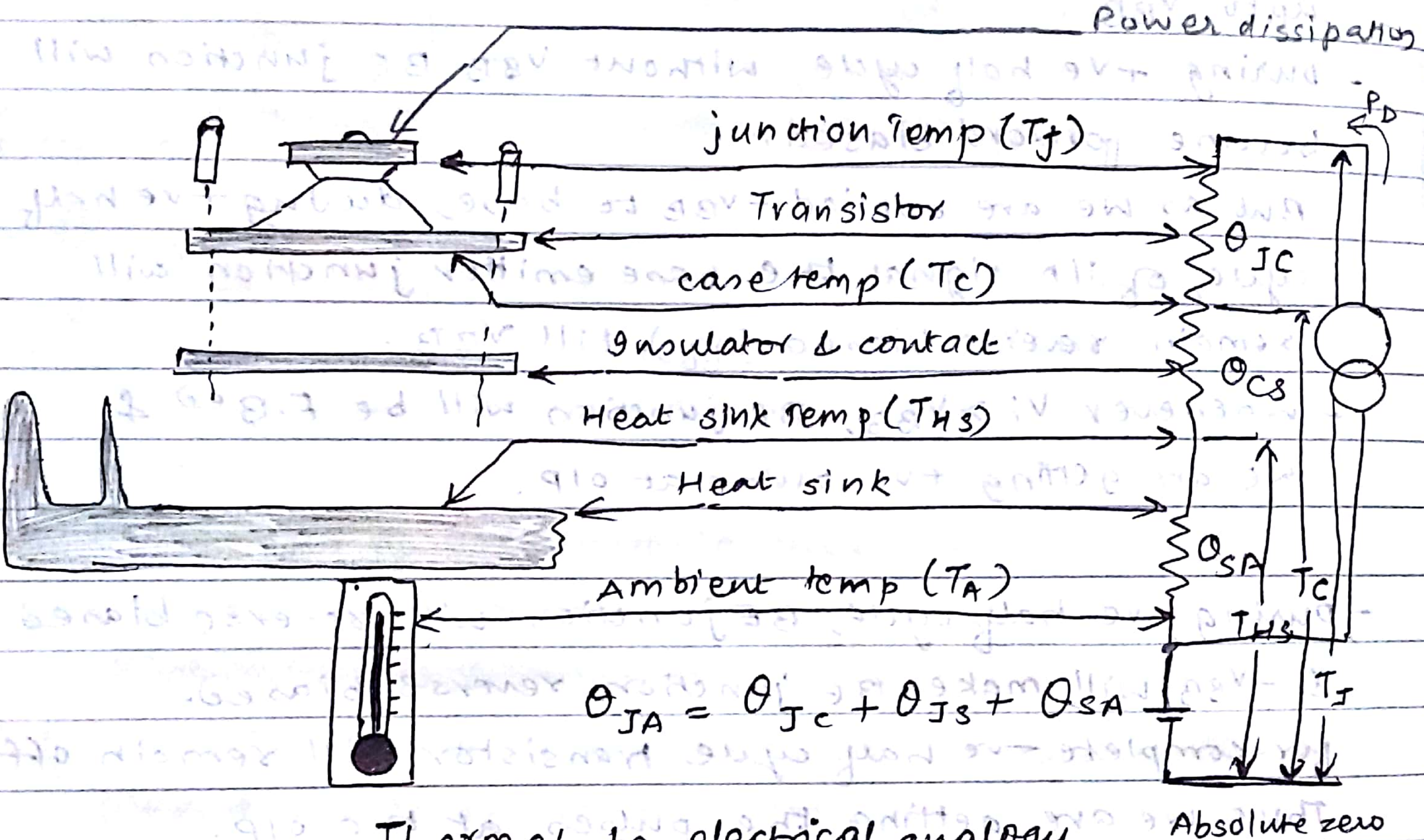
- During -ve half cycle, BE junction will reverse biased & $-V_{BB}$ will make BE junction reverse biased.

  for complete -ve half cycle transistor will remain off.

  Thus we are getting the pulses at the O/P.

  To get complete signal (0 to 360°) at the O/P.
- capacitor is connected in parallel to the primary Thus a tank circuit will be formed.

  Due to charging & discharging of capacitor via a primary winding so we get complete cycle at O/P. (Flywheel effect.)



$$\theta_{JA} = \theta_{JC} + \theta_{JS} + \theta_{SA}$$

Thermal to electrical analogy

* Thermal Considerations & Power Transistor :-

Power dissipated by the device causes an increase in temperature at the junction of device. So the maximum power handled by a particular device & the temperature of the transistor junctions are related.

of the Two types of BJTs,

Silicon (Si) : 150 - 200°c

Germanium (Ge) : 100 - 110°c

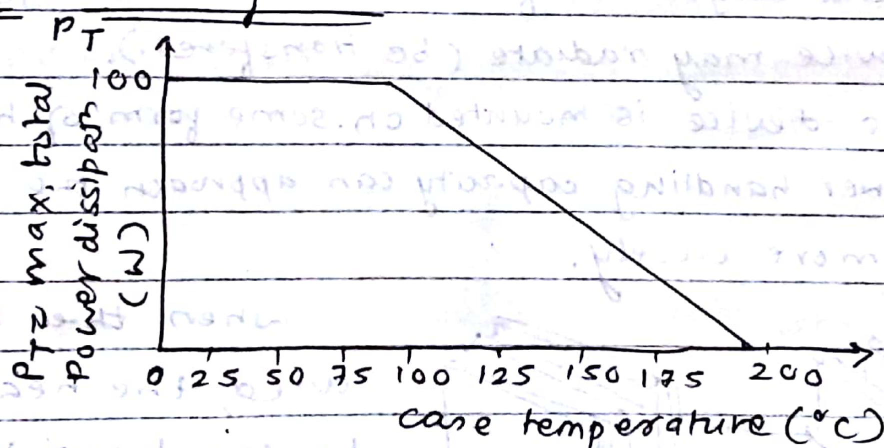
Silicon transistors provide greater maximum temparature ratings.

For many applications, avg power dissipated may be approximated as

$$P_D = V_{CE} I_C$$

This PD is allowed only up to maximum temperature. Above this temp, device PD capacity must be reduced or degrated so that at higher case temp, power handling capacity is reduced to 0W.

Power derating curve :-



typical power derating curve for silicon

The curve shows that the manufacturer will specify an upper temp point, after which a linear derating takes place. for Si, Pmax (handled by device) does not reduce to 0W until case temp is 200°C.

It is necessary to provide a (device) derating curve since it can be listed as 'derating factor' on device specification sheet.

$$P_D(\text{temp}_1) = P_D(\text{temp}_0) - (\text{Temp}_1 - \text{Temp}_0)(\text{derating factor})$$

where Temp0 = temp at which derating should begin

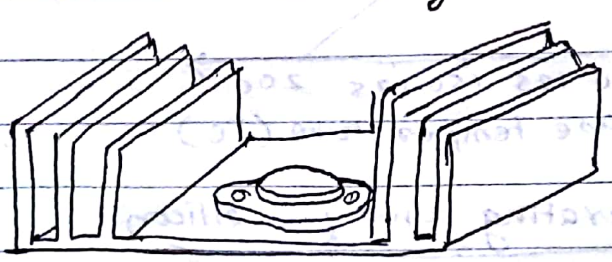
Temp1 = particular temp of interest (above Temp0)

$P_D(\text{temp}_0)$ & $P_D(\text{temp}_1)$ = maximum power dissipation at the temp specified.

Derating factor = is the value given by manufacturer in units of Watts per degree of temp ie W/°C.

* **Heat Sink :-** metal cases or frames and fans to remove the heat generated.

- The greater the power handled by the transistor, higher is the case temperature.
- The limiting factor in power handling by a particular transistor is the temperature of the device's collector junction.
- Power transistors are mounted in large metal cases to provide a large area from which the heat generated by the device may radiate (be transfered.).
- so the device is mounted on some form of heat sink, so that its power handling capacity can approach the rated maximum value more closely.



Typical Heat Sink

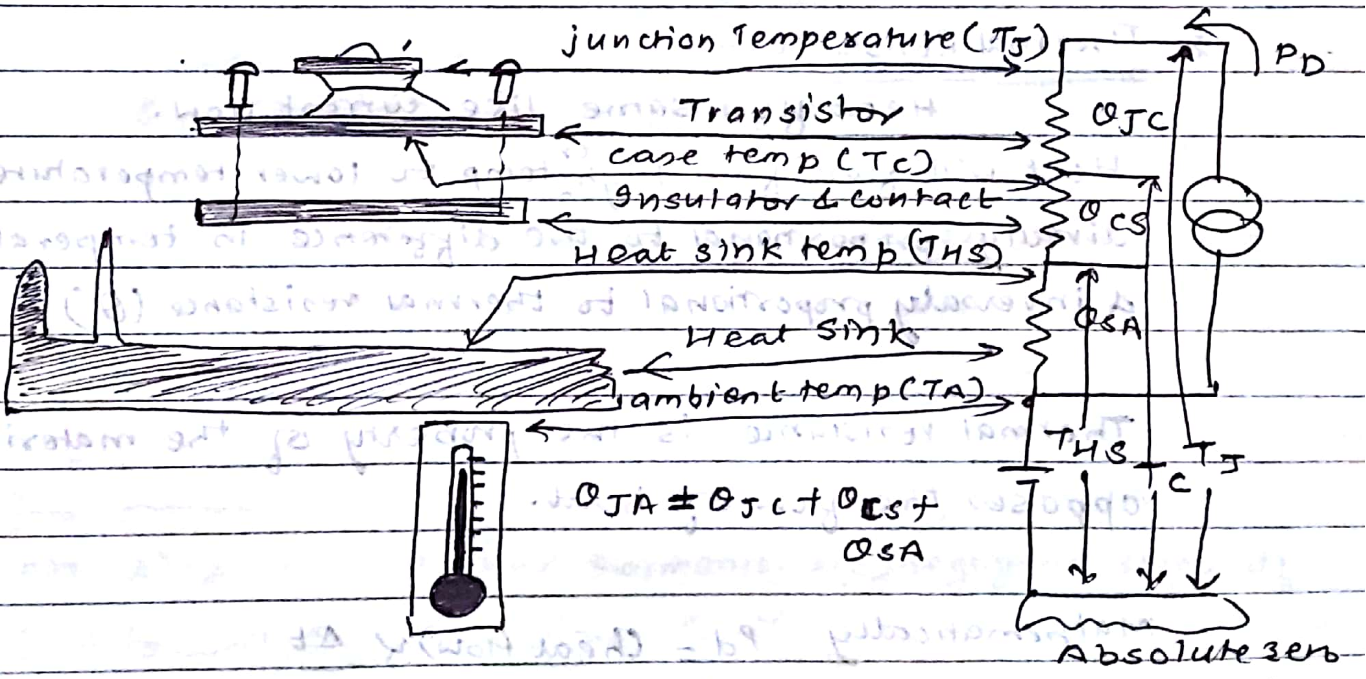
When the heat sink is used, the heat produced by the transistor dissipating power has a larger area from which to radiate (transfer) the heat into the air, thereby holding the case temparature to a much lower value than would result without the heat sink.

Even with an infinite heat sink (which, of course, is not available), for which the case temperature is held at the ambient (air) temperature, the junction will be heated above the case temperature & a maximum power rating must be considered.

* Thermal Analogy of a Power Transistor:-

Thermal to electrical analogy shows how the junction temperature T_J, case temperature T_C & ambient (air) temperature T_A are related by the device heat handling capacity.

- Temperature coefficient usually called thermal Resistance
- Thermal Resistance is used to describe heat effects by an electrical term.



θ_{JA} = total thermal Resistance (junction to ambient)

θ_{JC} = transistor thermal resistance (juncth to case)

θ_{CS} = Insulator " " (case to heatsink)

θ_{SA} = heat sink thermal resist. (heat sink to ambient)

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

analogy can be used in applying kirchoff's law to obtain

$$T_J = P_D \theta_{JA} + T_A$$

This shows that, junction temperature "floats" on the ambient temp & that the higher the ambient temperature, the lower is the allowed value of device power dissipation.

The thermal factor θ provides information abt how much temperature drop (or rise) results for a given amount of power dissipation.

$$T_J - T_C = \theta_{JC} P_D.$$

$$\boxed{P_D = \frac{T_J - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}}$$

* **Thermal Resistance :-**

Heat flow same like current flow.

Heat will flow from Higher temp to lower temperature. It is directly proportional to the difference in temperature (Δt) & inversely proportional to thermal resistance (θ)

Thermal resistance is the property of the material which opposes the flow of heat.

Mathematically $P_d = (\text{heat flow}) \propto \frac{\Delta t}{\theta}$

$$P_d = \frac{T_2 - T_1}{\theta}$$

or Thermal resistance of material is given by,

$$\boxed{\theta = \rho \frac{d}{A}} \quad \text{or} \quad \boxed{\theta = \frac{T_2 - T_1}{P_d}}$$

ρ = Thermal resistivity.
d = thickness of the material
A = Area of crosssection

Ex1) To determine what max dissipation will be allowed for an 80W silicon transistor (rated at 25°C). If derating is required above 25°C by a derating factor of 0.5W/°C. At case temp of 125°C

Soln:-
$Pd(temp_1) = Pd(25°C) = 80W$

Derating factor $= 0.5 W/°C$

$T_2 = 125°C$

$Pd(T_2) = ?$

$Pd(Temp_2) = Pd(Temp_1) - (Temp_2 - Temp_1)(Derating\ f.)$

$$\boxed{Pd(T_2) = 30W}$$

Ex2) A silicon transistor is operated with a heat sink ($\theta_{SA} = 1.5°C/W$). The transistor rated at 150W (25°C) has $\theta_{JC} = 0.5°C/W$ & mounting insulation has $\theta_{CS} = 0.6°C/W$. What max. power can be dissipated if the ambient temp is 40°C & $T_j(max) = 200°C$

Soln:-

$\theta_{SA} = 1.5°C/W$ $\theta_{CS} = 0.6°C/W$

$Pd_{max} = 150W$ $T_A = 40°C$

$Pd(25°C) = 150W$ $T_j = 200°C$

$\theta_{JC} = 0.5°C/W$ $Pd = ?$

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$

$= 0.5 + 0.6 + 1.5$

$\underline{\theta_{JA} = 2.6°C/W}$

$Pd = \frac{T_j - T_A}{\theta_{JA}} = \frac{200-40}{2.6}$

$\underline{Pd = 61.53W}$

Ex3) The principle harmonic in a certain $10V_{(p)}$ 15kHz are 2nd & 4th. All other harmonics are negligibly small if THD is 12% & the amplitude of 2nd harmonics is 0.5V. What is the amplitude of 60kHz harmonics.

Soln:-

$f_1 = 15kHz$ $A(60kHz) = A_4 = ?$

$A_1 = 10V(p)$ $THD = \sqrt{D_2^2 + D_4^2}$

$THD = 12\% = 0.12$

$A_2 = 0.5V$ $D_2 = \frac{A_2}{A_1} = \frac{0.5}{10} = \underline{0.05}$

$0.12 = \sqrt{(0.05)^2 + D_4^2}$ $\therefore \underline{D_4 = 0.109}$