

* Transistor -

It is having two PN junctions, one junction giving low resistance (as forward biased) & other junction offering high resistance because of reverse bias.

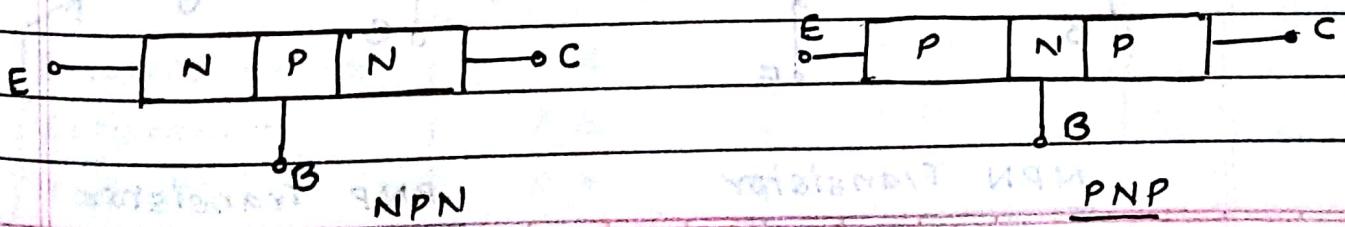
Small signal is introduced in low resistance & output is taken from high resistance. So this system can transfer current signal from low resistance to high resistance. therefore the name is given transistor. ie. Transfer of resistor.

* Bipolar Junction Transistor (BJT) :-

In transistor, the current conduction takes place due to both electrons & holes.

- Electrons have -ve charge & holes have +ve charge. Thus current in transistor flows due to +ve charge as well as -ve charge carriers.
- Therefore transistor is called Bipolar Junction Transistor (BJT).
- It has very important property that it can raise the strength of weak signal, this property is called as amplification.
- BJT consists of two PN junctions, the junctions are formed by sandwiching either 'P' type or 'N' type semiconductor layers between pair of opposite types.

* Two types of BJT -



* Terminals of BJT -

BJT has three regions known as emitter, base & collector.

All these regions are provided with terminals labelled as E, B, C.

• Emitter - It is the region situated in one side of transistor, which supplies charge carriers (ie electrons & holes) to the other two regions. Emitter is heavily doped region.

• Base - It is the middle region that forms two PN junctions in the transistor. It is thin compared to emitter & is lightly doped region.

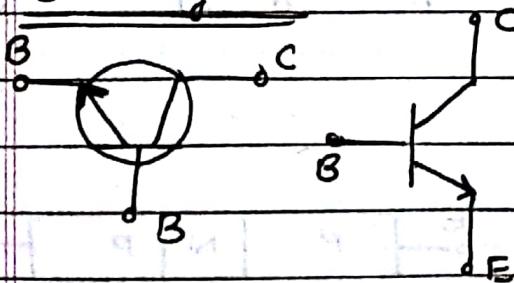
• Collector - It is the region situated in other side of transistor, which collects charge carriers. The collector of transistor is always larger than E & B of transistor. Its doping level is moderate.

- Transistor has two PN junctions J_c & $J_{E,B}$.

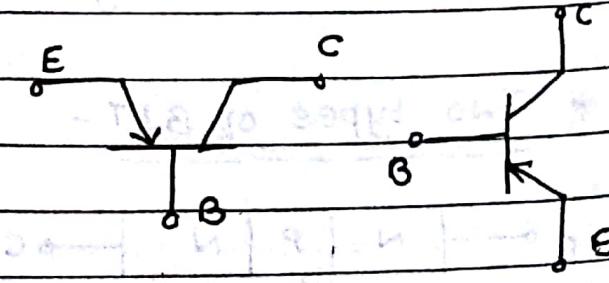
' J_E ' is a junction between emitter & base region & known as emitter base junction.

' J_c ' is a junction between collector & base region & known as collector base junction.

* BJT symbol



NPN Transistor

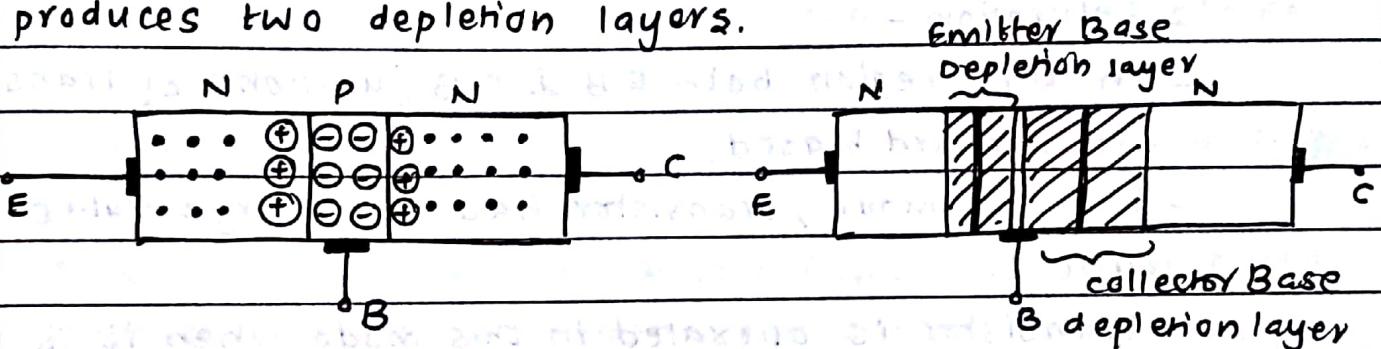


PNP Transistor

- Transistor symbol carries an arrowhead in the emitter pointing from 'P' region towards 'N' region.
- Arrowhead indicates the direction of conventional current flow in transistor.
- Direction of arrowhead at the emitter in NPN & PNP transistor is opposite to each other.

* Unbiased BJT :-

When three terminals are open, that BJT/transistor is called unbiased transistor. Under this condition, the diffusion of free e^- s across the junction produces two depletion layers.



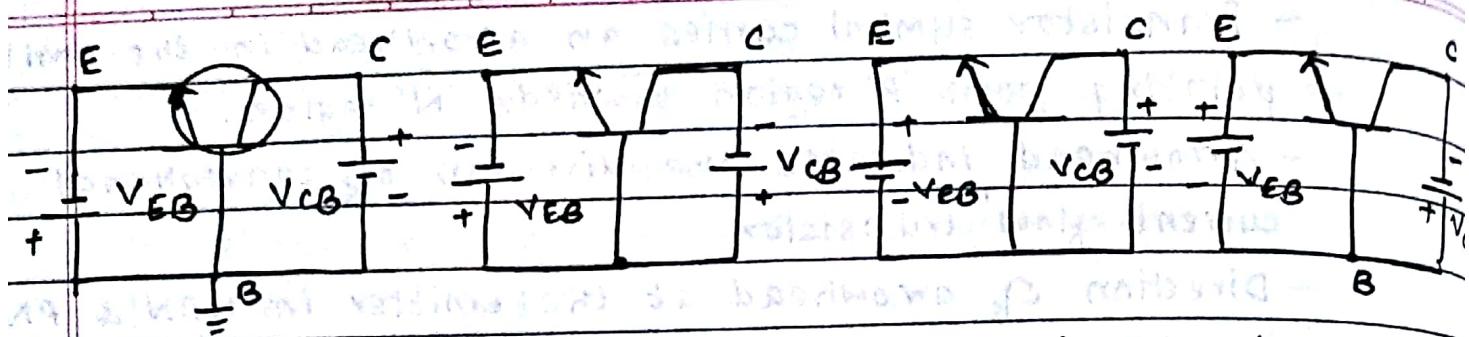
- The potential barrier for each of these layers is at $25^\circ C$, is approx $0.7V$ for 'Si' & $0.3V$ for 'Ge'.
- Three regions have different doping level, therefore width of depletion layer is also different.
- Unbiased transistors never used in actual practice.

* BJT Biasing (Operating Modes) :-

Biasing means applying suitable dc voltage across transistor terminals.

- There are four modes of transistor operation. i.e ways of biasing.

	EB junction	CB junction
Forward Active	F.B.	R.B.
Saturation	F.B.	F.B.
Cut off	R.B.	R.B.
Inverted	R.B.	F.B.



Forward Active Saturation Cut-off Inverted

1. Forward Active -

- In this region, E-B junction of transistor is forward biased & C-B junction is reverse biased.

2. Saturation -

- In this region, both E-B & C-B junctions of transistor are forward biased.

- In this mode, transistor has very large value of current.

- Transistor is operated in this mode, when it is used as closed switch.

3. cut-off -

- In this mode, both E-B & C-B junctions of transistor are reverse biased.

- In this mode, transistor has practically zero current.

- The transistor is operated in this mode, when it is used as open switch.

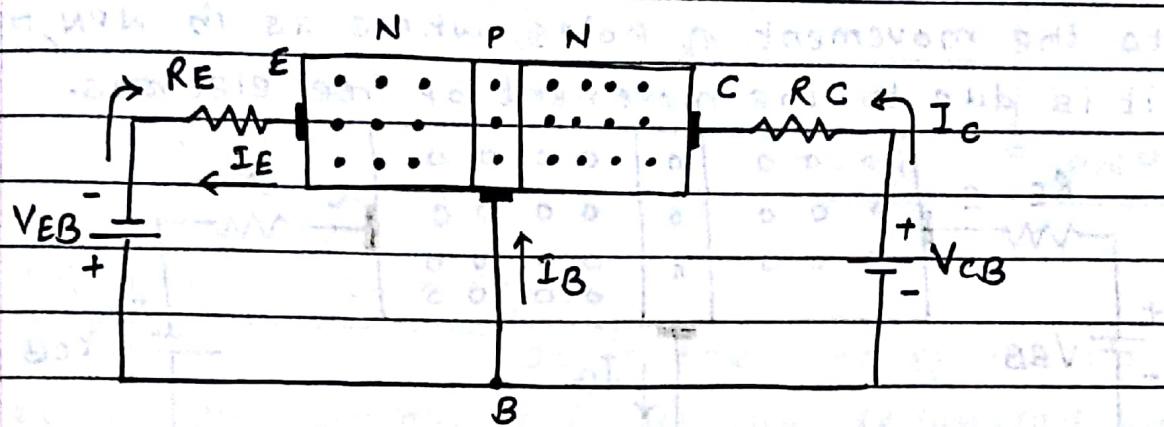
4. Inverted -

- In this mode E-B junction of transistor is reverse biased & C-B junction of transistor is forward biased.

* Operation of NPN Transistor :-

Here NPN transistor is

biased in Forward Active mode. i.e. E-B junction is FBEd & C-B junction R.Bed.

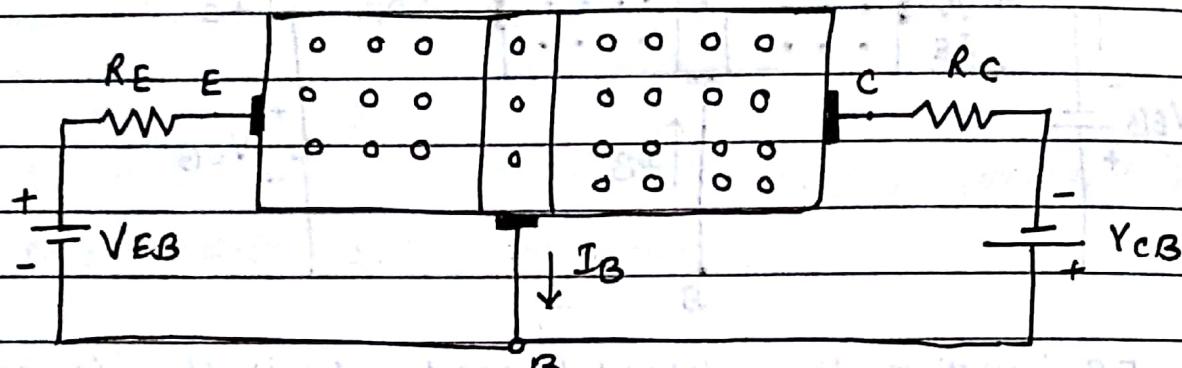


- EB junction is forward biased only if V_{EB} is greater than barrier voltage i.e. 0.7 for Si & 0.3 for Ge.
- Forward Biased EB junction causes free electrons in N type emitter to flow towards the base region.
- This constitutes emitter current (I_E). It may be noted that direction of conventional current is opposite to flow of electrons.
- Therefore electrons after reaching base region tends to combine with holes. This constitute base current (I_B).
- However most of free electrons do not combine with the holes in the base because base width is externally small & electrons do not get sufficient holes for recombination.
- Thus most of the electrons diffuse to the collector region & constitute collector current (I_C).
- However current due to thermally generated carriers, this is an other small component of collector current. This small component of collector current is called reverse saturation current.
- Resistor R_E & R_C are used for limiting the magnitude of current.

* operation of PNP Transistor -

The operation of PNP

Transistor is similar to NPN.
- However, the current within a PNP transistor is due to the movement of holes, whereas in NPN, transistor it is due to the movement of free electrons.



For both NPN & PNP,

$$I_E = I_B + I_C$$

As I_B is very small $\therefore I_E = I_C$

* BJT circuit configurations:-

When transistor is connected

in the circuit, we require four terminals, two for ilp & two for olp. This can be overcome by using one of the three terminals as a common terminal.

① Common Base configuration -

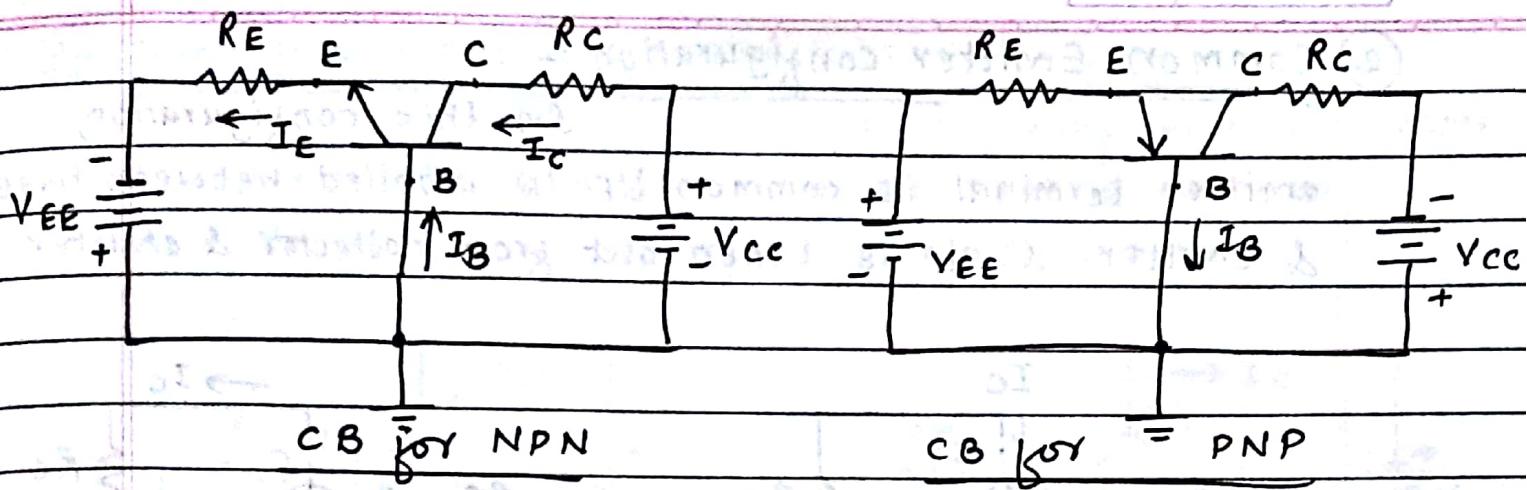
In this configuration,

base is common terminal to both ilp & olp.

The input is applied between emitter & base terminal & olp is taken between collector & base terminal.

- The ratio of transistor olp to ilp is called gain of transistor. Since the ilp & olp current may a.c or d.c

\therefore current gains namely, dc current gain & ac current gain.



DC current Gain (α) -

It is the ratio of collector current to emitter current & is usually designated by ' α ' or α_{dc} or h_{FB}

$$\alpha \text{ or } \alpha_{dc} \text{ or } h_{FB} = \frac{I_C}{I_E}$$

- In transistor, collector current is always less than emitter current. Therefore current gain in CB configuration is always less than unity.

- If $I_C = 9.8\text{mA}$ & $I_E = 10\text{mA}$ then $\alpha = 0.98$
which means that I_C is 98% of I_E .

- The actual value ranges from 0.95 to 0.998

$$I_C = \alpha I_E \quad \& \quad I_E = I_B + I_C \therefore I_B = I_E - I_C$$

$$= I_E - \alpha I_E$$

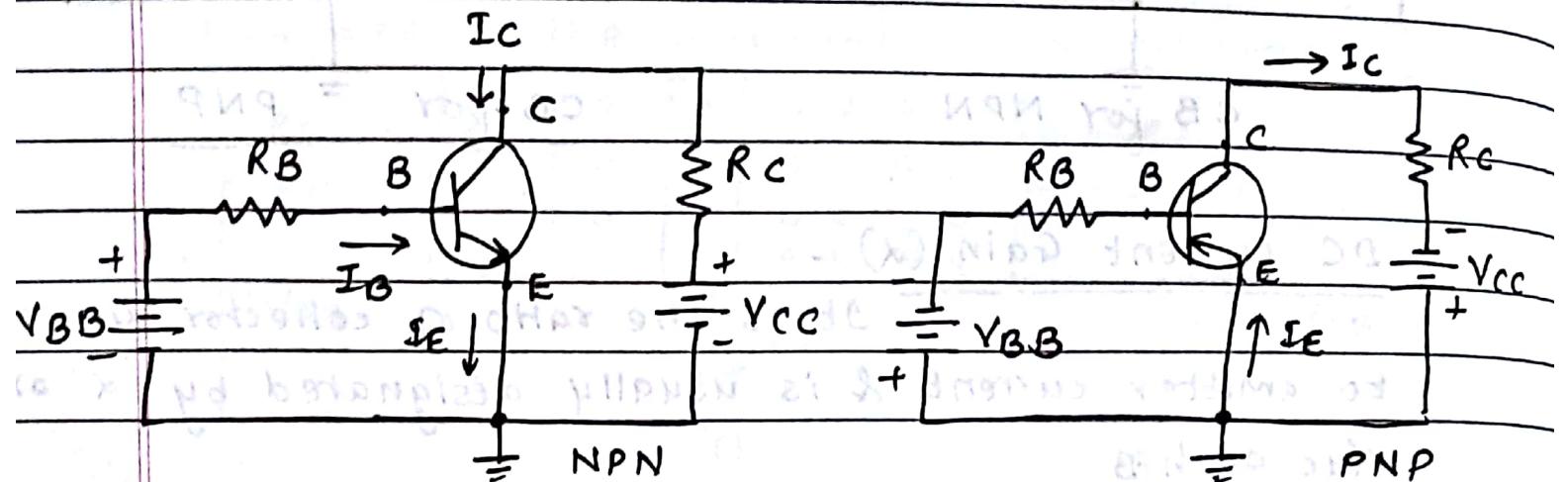
$$I_B = (1 - \alpha) I_E$$

AC current Gain (α_0 or α_{ac}) -

$$\alpha_0 \text{ or } \alpha_{ac} = \frac{\Delta I_C}{\Delta I_E}$$

2. Common Emitter configuration :-

In this configuration, emitter terminal is common. I_{Bp} is applied between base & emitter & o_{lp} is taken out from collector & emitter.



DC current Gain (β) or (β_{dc} or h_{FE})

It is the ratio of collector current to base current & is designated by β , β_{dc} , h_{FE} .

$$\beta \text{ or } \beta_{dc} \text{ or } h_{FE} = \frac{I_C}{I_B}$$

- current I_C of transistor is much larger than I_B

Therefore, value of β is greater than unity.

$$- \text{ If } I_C = 50 \text{ mA}, I_B = 0.5 \text{ mA} \text{ then } \beta = \frac{50}{0.5} = 100$$

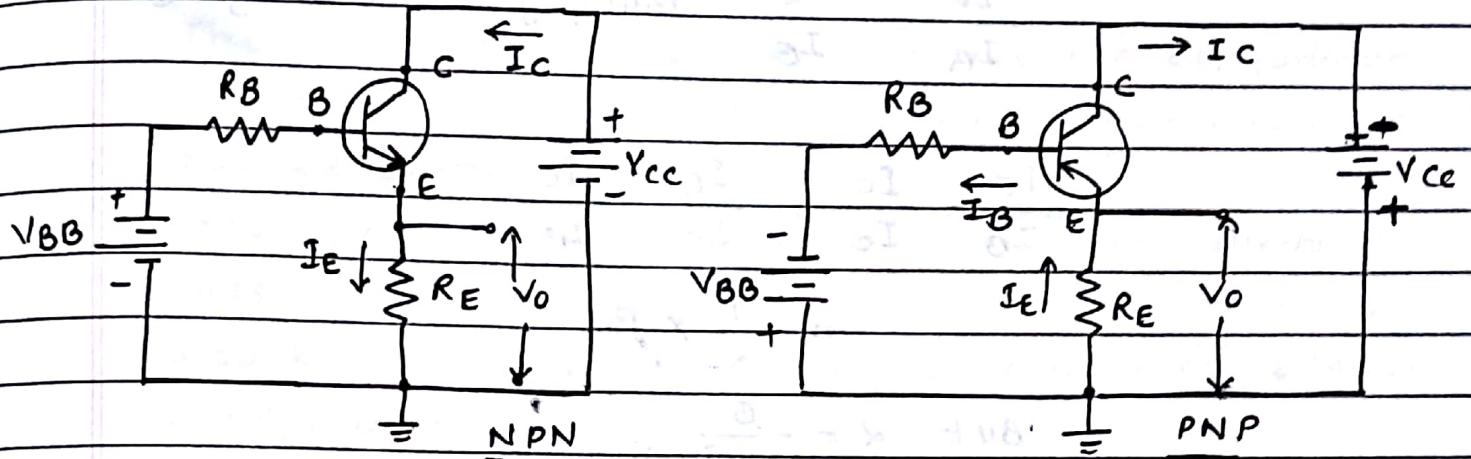
It indicates I_C is 100 times that of I_B .

AC current Gain (β_0 or β_{ac})

$$\beta_0 \text{ or } \beta_{dc} = \frac{\Delta I_C}{\Delta I_B}$$

3. Common collector configuration :-

In this configuration, collector is common. A.P is applied between base & collector. And o.p is taken between emitter & collector.



DC current Gain (γ) -

It is the ratio of I_E to I_B i.e
emitter current to base current.

$$\gamma = \frac{I_E}{I_B}$$

* Relation between α & β -

$$I_E = I_B + I_C$$

divide both side by I_C

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1 \quad \text{But } \frac{I_C}{I_E} = \alpha \quad \frac{I_C}{I_B} = \beta$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1 = \frac{1+\beta}{\beta}$$

$$\alpha = \frac{\beta}{\beta+1}$$

$$\text{or } \beta = \frac{I_C}{I_B} = \frac{\alpha \times I_E}{(1-\alpha)I_E} = \frac{\alpha}{1-\alpha} \therefore \beta = \frac{\alpha}{1-\alpha}$$

* Relation between β & γ :-

we know that,

$$\gamma = \frac{I_E}{I_B}$$

$$\frac{I_E}{I_B} = \frac{I_E}{I_B} \text{ multiply & divide by } I_C$$

$$\frac{I_E}{I_B} \times \frac{I_C}{I_C} = \frac{I_E}{I_C} \times \frac{I_C}{I_B}$$

$$= \frac{1}{\alpha} \times \beta$$

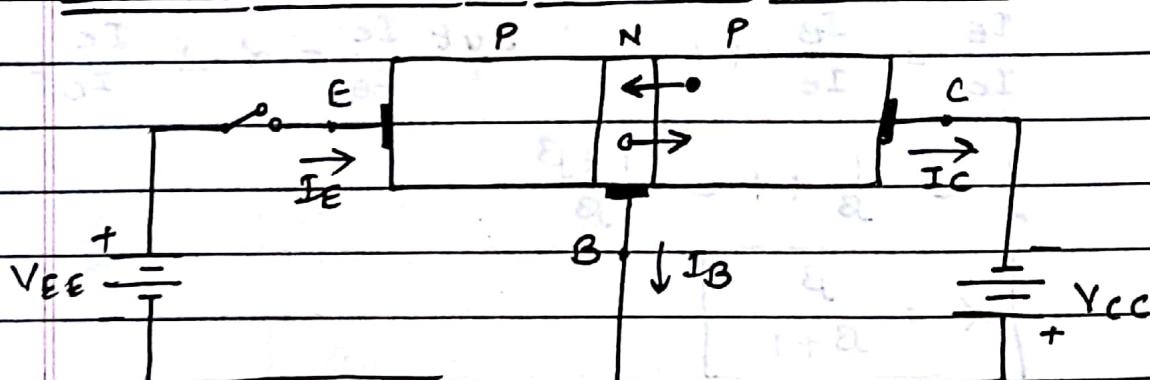
$$\text{But } \alpha = \frac{\beta}{1+\beta}$$

$$\therefore \gamma = \frac{\beta}{\left(\frac{\beta}{1+\beta}\right)} = \frac{\beta}{\beta} \cdot \frac{1+\beta}{\beta} = 1 + \beta \quad \therefore \boxed{\gamma = 1 + \beta}$$

$$\text{Similarly } \beta = \frac{\alpha}{1-\alpha} \quad \gamma = \frac{\alpha}{\alpha(1-\alpha)} = \frac{1}{1-\alpha} \quad \boxed{\gamma = \frac{1}{1-\alpha}}$$

it means for $\gamma = 1 + \beta$, output current gain of CC is $(1 + \beta)$ times that of IP current. gain $\approx \beta$ $\because \beta > 1$

* Leakage current in Common Base BJT -



- let switch 'S' be opened. it disconnects emitter from the base & hence the E-B junction of transistor is open circuited.

- Thus, there is no I_E . So there is no I_B or I_C . However it may noted that CB junction of transistor is reverse biased due to the holes injected from emitter. But this junction is forward biased due to the thermally generated minority carriers.

- The minority carriers diffuse across the CB junction & hence produce a certain value of current known as leakage current.

- This current is called leakage current from collector to base with emitter open & designated by I_{CBO} . It is also known as reverse saturation current or collector cut off current (I_C^0).

- Thus I_{CBO} or I_C^0 is similar to reverse saturation current in PN junction.

- Total collector current

$$I_C = \alpha I_E + I_C^0$$

$$\alpha = (I_C - I_C^0)$$

$$\text{but } I_E = I_B + I_C$$

$$\alpha = \frac{I_C - I_C^0}{(I_B + I_C)}$$

$$I_C = \alpha (I_B + I_C) + I_C^0$$

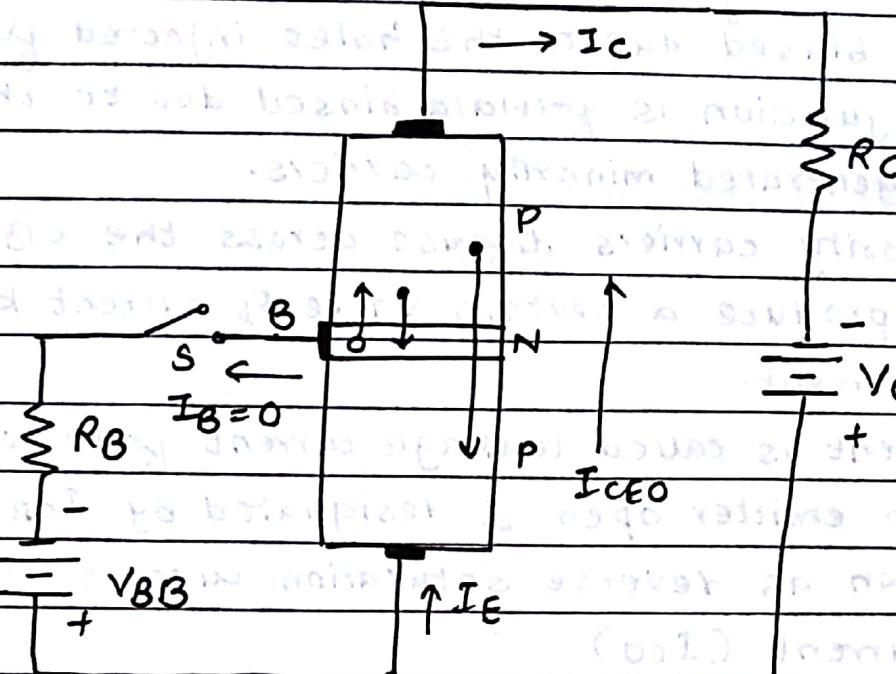
$$= \alpha I_B + \alpha I_C + I_C^0$$

$$(1-\alpha) I_C = \alpha I_B + I_C^0$$

$$I_C = \left(\frac{\alpha}{1-\alpha} \right) I_B + \frac{I_C^0}{1-\alpha}$$

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

* Leakage current in Common Emitter BJT :-



- If switch is open then base is disconnected from the emitter. Hence BE junction of transistor is open & $\therefore I_B$ is zero.

- Under this condition leakage current flows (through) from emitter to collector terminal. The current is designated as I_{CEO} .

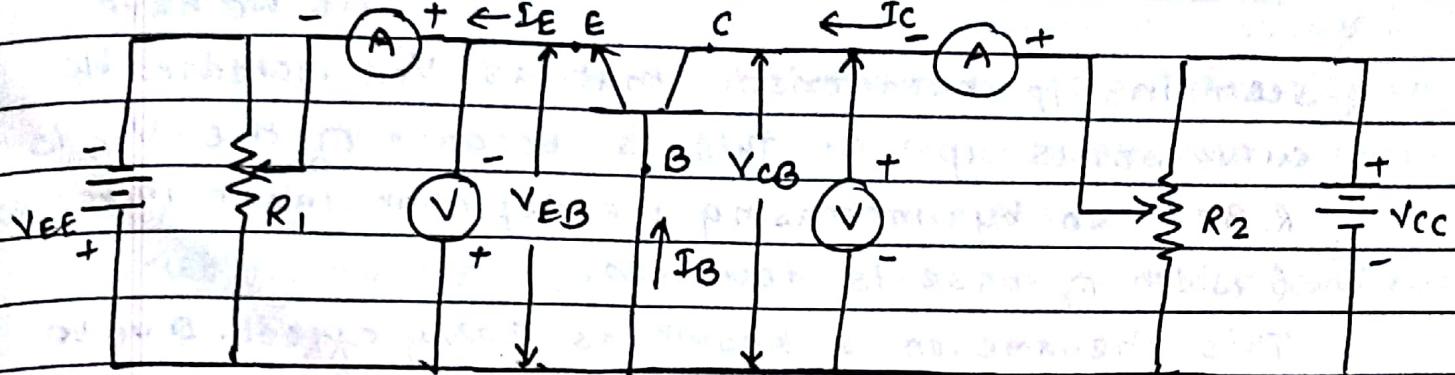
- This leakage is not just due to the thermally generated carriers across the collector base junction but also due to movement of electrons across the base emitter junction.

$$\begin{aligned} \text{Total } I_{CEO} &= I_{CO} + \beta I_{CO} \\ &= (1 + \beta) I_{CO} \end{aligned}$$

$$\begin{aligned} \text{Total } I_C &= \beta I_B + I_{CEO} \\ I_C &= \beta I_B + (1 + \beta) I_{CO} \end{aligned}$$

- This implies that leakage current in CE configuration is β times larger than CB transistor.

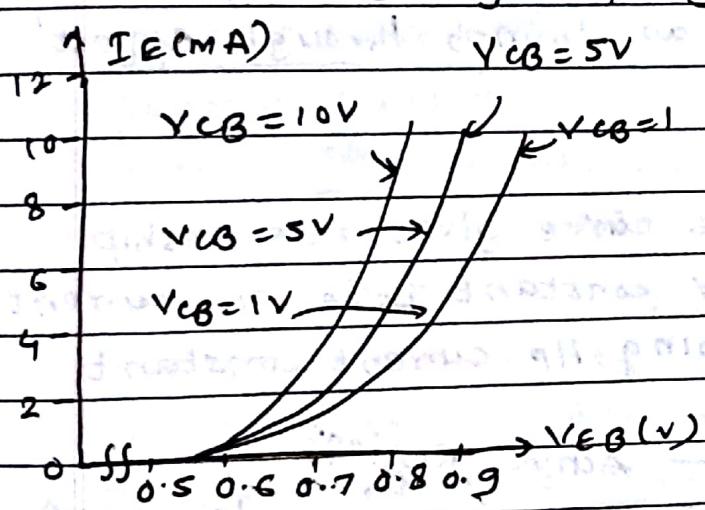
* Characteristics of CB configuration -



Experimental set up for I_P, O_P characteristics

I/P characteristics -

This curve gives relationship between I_E & V_{EB} for constant V_{CB} , which means i/p current & i/p voltage by keeping o/p voltage constant.



- first keep $V_{CB} = 1V$ & by increasing V_{EB} measure corresponding I_E & plot it.
 - same for $V_{CB} 5V$ and $10V$
 - these exist threshold voltage or current called as offset voltage or cut in voltage or knee voltage, below which

I_E is negligible. It is denoted as ' V_k ' for Si, $0.5V$ & for Ge it is $0.1V$

- After this knee voltage, as I_E increases rapidly by increasing small amount value of V_{EB} which means for CB config R_i is small,

$$\text{for DC} \quad R_i = \frac{V_{EB}}{I_E} \quad \text{Typically value } 50\text{--}100 \Omega$$

$$\text{for AC} \quad R_i = \frac{\Delta V_{EB}}{\Delta I_E}$$

-Base width modulation or Early effect -

As we have seen in i/p characteristic that as V_{CB} increases the curve shifts upward. This is because of the V_{CB} is R.Bed, so by increasing the depletion layer increases & width of base is decreases.

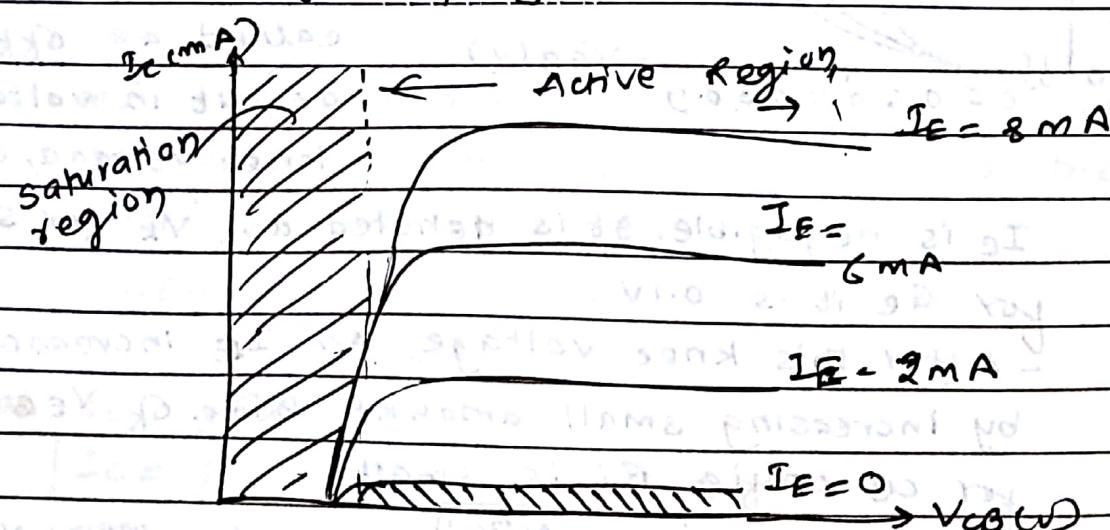
This phenomenon is known as Early effect. Due to ~~part~~ this effect following happens,

⇒ Recombination of electrons with holes in base region reduces hence of increases with increase of V_{CB} .

⇒ For extremely large collector voltage, the effective base width may reduces to zero, causing breakdown of transistor known as 'punch through effect'.

-o/p characteristics -

This curve gives relationship between I_C & V_{CB} for constant I_E i.e. o/p current & o/p voltage by keeping i/p current constant.



Saturation region - It is the region to the left of the dotted line. In this region, V_{CB} is -ve for NPN transistor. It means c-B junction is also forward biased. In this small change in V_{CB}

results in large number of current.

Active Region - It is the region between vertical dotted line & horizontal ~~shaded~~ axis. On this region, BE junction is F.B.E. In this region ~~the~~ BE junction is F.B.E & BC junction is reverse biased.

Cut off Region - It is region along with horizontal axis & shaded lines. It corresponds to $I_{EC} = 0$.

- In cut off region, along with horizontal axis & shaded lines. It is corresponds to $I_{EC} = 0$.
- In cut off region, both junction are reverse biased.
- This is due to the fact that electrons are injected in to base under (condition e^- , e^+) action of F.B.E EBJ.

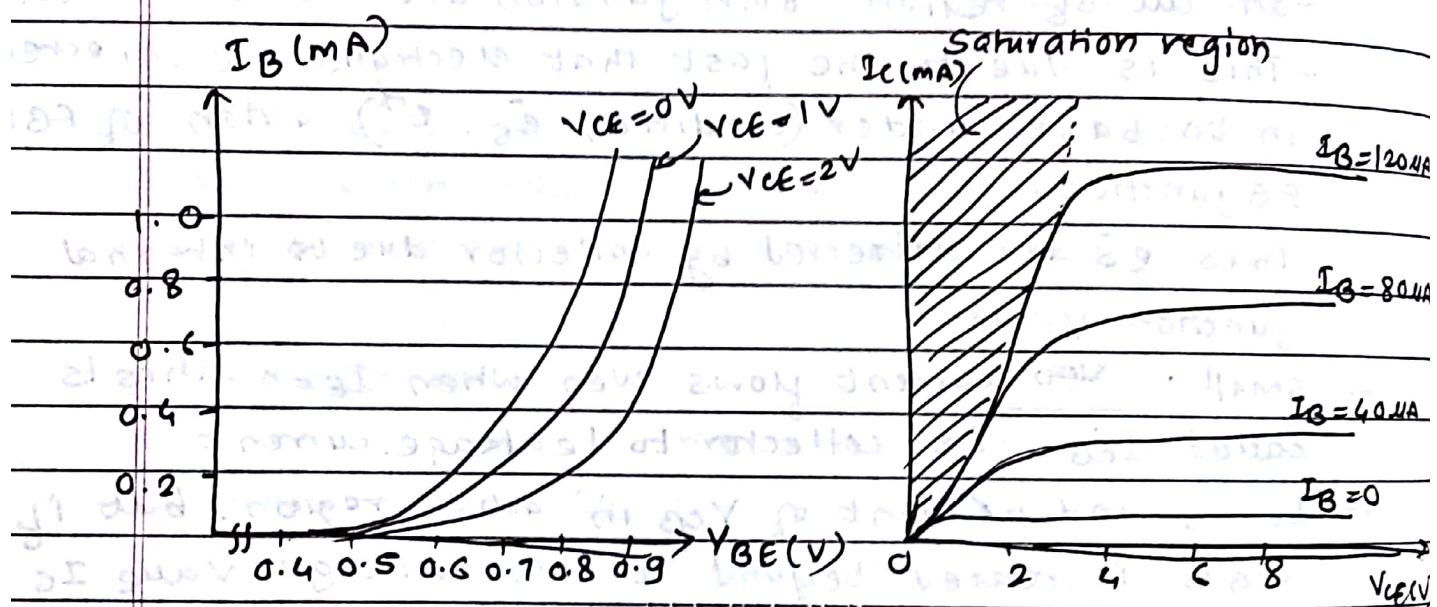
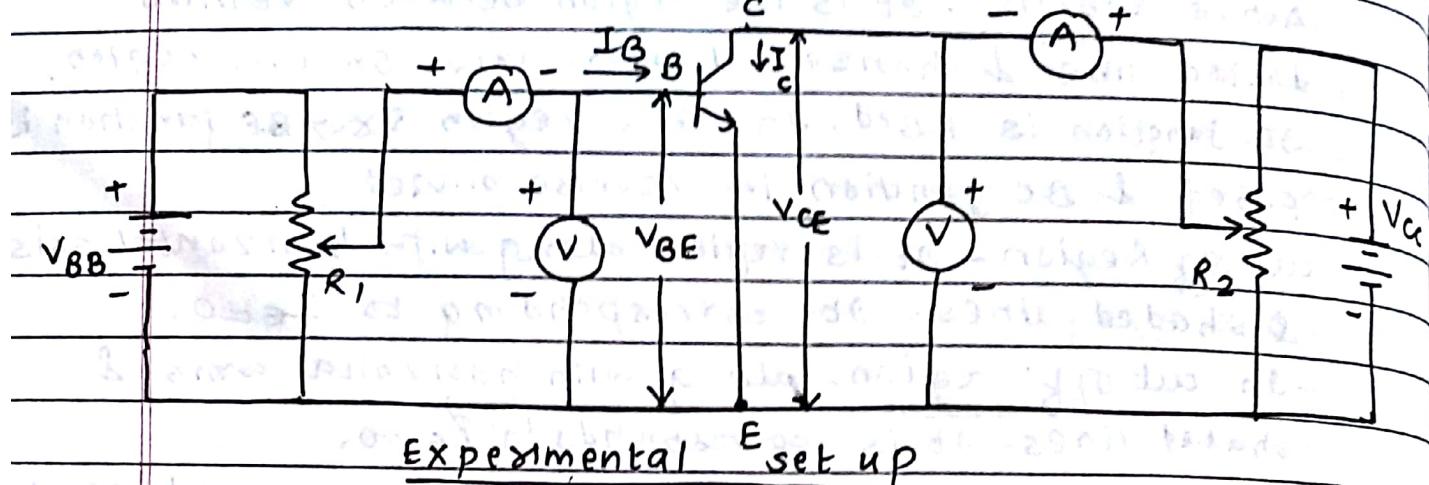
Thus e^- are collected by collector due to internal junction Voltage.

- Small ~~no~~ current flows even when $I_{EC} = 0$. This is called I_{CEO} . i.e collector to leakage current.
- I_C is independent of V_{CB} in active region. but if V_{CB} is increased beyond certain leakage value I_C increases rapidly due to avalanche breakdown and transistor action is lost.

$$\text{OIP resistance (dc)} = R_O = \frac{V_{CB}}{I_C} \quad \text{Typical value} = 500\text{k}\Omega$$

$$R_O \text{ for ACT is } R_O = \frac{\Delta V_{CB}}{\Delta I_C}$$

* Characteristics of Common Emitter Configuration -



I_{BP} characteristics

I_{OP} characteristics

I_{BP} characteristics -

- It is the curve of I_{BP} current & input voltage by keeping O_{LP} voltage current. Here the difference is that by increasing V_{CE}, the curve shifts downward.
- because as V_{CE} increased the depletion width in base region increases & reduces effective base width.

- AC I_{BP} Resistance $R_i = \Delta V_{BE} / \Delta I_B$

- R_i varies with location of operating point.

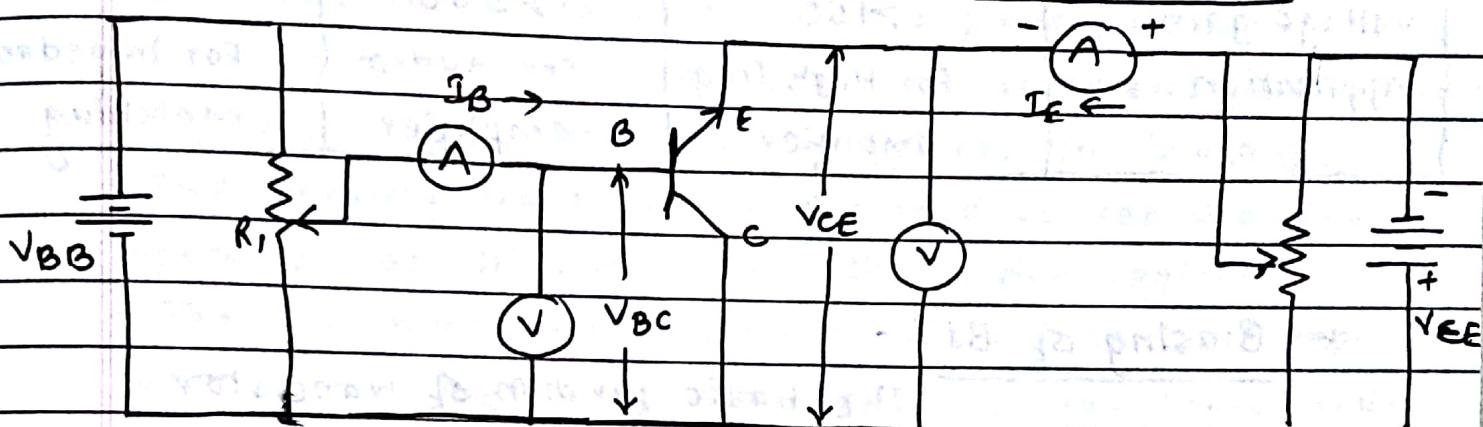
- R_i ranges from 600Ω to 4000Ω

O_{LP} characteristics - I_C reaches to saturation when V_{CE} = 1V. Then there is same phenomenon by early

effect.

- Also $I_B = 0$ but there is I_C , which is leakage current.
- Under this condition transistor is cut off.
- ac o/p Resistance $R_o = \Delta V_{CE} / \Delta I_C$
- o/p ranges from $10k\Omega$ to $50k\Omega$.

* Characteristics of common collector configuration -



Experimental set up

$I_B(MA)$

$V_{CE}=2V$

0.8
0.6
0.4
0.2

$V_{CE}=5V$

0.5 0.6 0.7 0.8

$V_{BC}(V)$

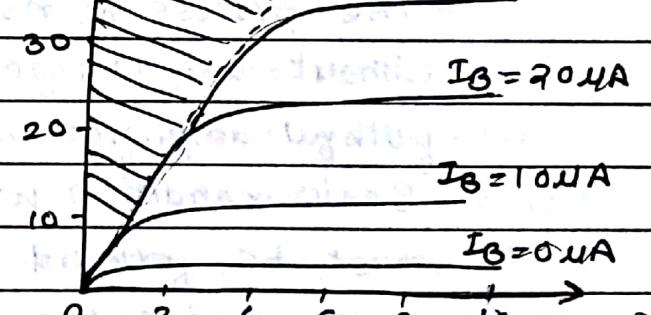
$I_E(MA)$

$I_B=30\mu A$

$I_B=20\mu A$

$I_B=10\mu A$

$I_B=0\mu A$



I/p characteristics

o/p characteristics

I/p Resistance

$$R_i = \frac{V_{BC}}{I_B}$$

o/p Resistance

$$R_o = \frac{V_{CE}}{I_E}$$

R_i is very high about $750k\Omega$ but R_o is low about 50Ω

* Comparison of three configurations of BJT -

Parameters	common Base	common Emitter	common Collector
I/I _P Resistance	Low	Low	High
o/I _P Resistance	High	High	Low
current Gain	< 1	20 to 300	50 to 500
Voltage gain	>150	>500	< 1
Application	For High freq amplifier	For Audio amplifier	For impedance matching

* Biasing of BJT -

The basic function of transistor is to perform amplification. Necessary requirement during amplification is that magnitude of signal should increase & there should be no change in signal shape.

- The process of rising the strength of weak signal without any change in its original shape is known as faithful amplification.
- Basic condition for faithful amplification is BE junction must be forward bias & BC junction must be reverse biased during amplification.

- It is necessary to fulfil this condition & this is done by proper biasing.

The proper flow of zero signal collector current & the maintenance of proper V_{CE} during passage of signal is known as transistor biasing.

- This is achieved with bias battery & associative circuit element. The performance of transistor depends on dc bias condition.

* Operating point -

Biasing means applying

For transistor amplification to dc voltages to establish a fixed level of current & voltage.

- For transistor amplifier the resulting dc current & voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal.

- Because the operating point is a fixed point on the characteristics, it is also called the quiescent point (Q point).

- By definition, quiescent means quiet, still, inactive.

- The biasing circuit can be designed to set the device operation at ' Q ' point within the active region.

- The DC bias should remain constant so that there will be no shifting in operating point but there are certain factors such as temperature variation & unit to unit manufacturing.

Variation of β :-

It is seen that transistor of same type may have different value of several parameter.

- If transistor in given circuit is replaced by another transistor of same type, transistor parameter changes considerably.

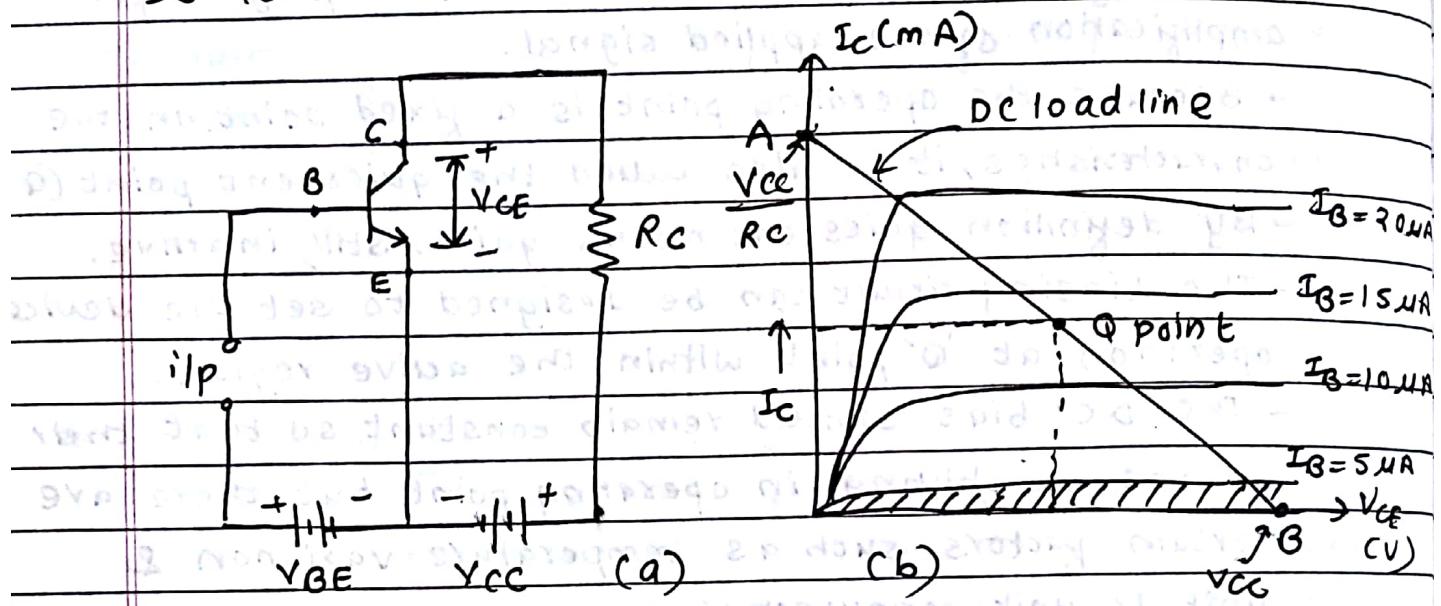
- If β changes, it may shift operating point.

* Load Line -

The straight line drawn on the characteristics of transistor amplifier circuit which gives the value of collector current I_C & collector to emitter voltage V_{CE} corresponding to either DC or AC i/p conditions is called load line.

DC load line -

The straight line drawn on o/p characteristics of transistor amplifier which gives the DC values of collector current I_C & collector to emitter voltage V_{CE} corresponding to zero signal ie DC conditions, is called DC load line.



- consider CE configuration with NPN transistor circuit.

- In this circuit when zero i/p signal is applied, DC conditions remains unchanged.

- o/p characteristics is shown in figure (b).

- The value of V_{CE} at anytime 't' is given by,

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C = \left(\frac{-1}{R_C} \right) V_{CE} + \frac{V_{CC}}{R_C}$$

Comparing this equation with the equation of straight line, $y = mx + c$ $\therefore m = -\frac{1}{R_C}$

- so the slope of this line depends on load resistance.

- To plot load line, we need two end points of straight line. These two points are locations,

case(i) when collector current I_c is zero, then V_{CE} is max & is equal to V_{CC}

$$\therefore V_{CE} = V_{CC} - I_c R_C$$

$$V_{CE(\max)} = V_{CC} \quad \because I_c = 0$$

This gives first point 'B' having co-ordinates $(V_{CC}, 0)$ on the x-axis as shown in figure (b)

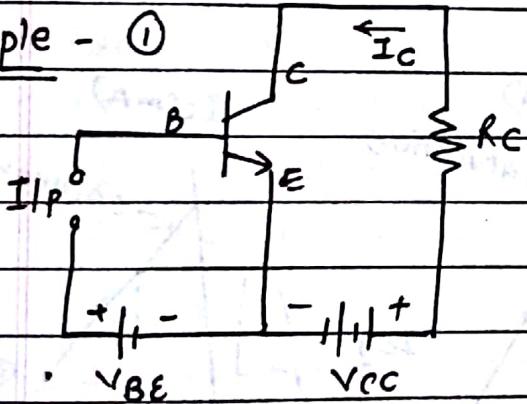
case(ii) When V_{CE} is zero, then collector current is max & is equal to V_{CC}/R_C

$$\therefore V_{CE} = V_{CC} - I_c R_C \text{ but } V_{CE} = 0$$

$$I_{C(\max)} = \frac{V_{CC}}{R_C}$$

This given second point 'A' having co-ordinates $(0, \frac{V_{CC}}{R_C})$ on 'y' axis as shown in fig (b)

Example - ①



For the circuit shown, draw DC load line.

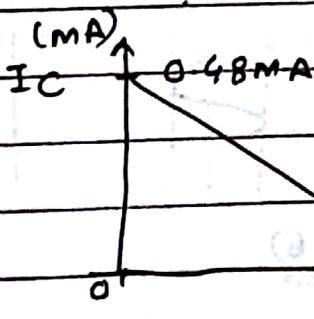
$$2019 - V_{CE} = V_{CC} - I_c R_C$$

case(i) $I_c = 0$

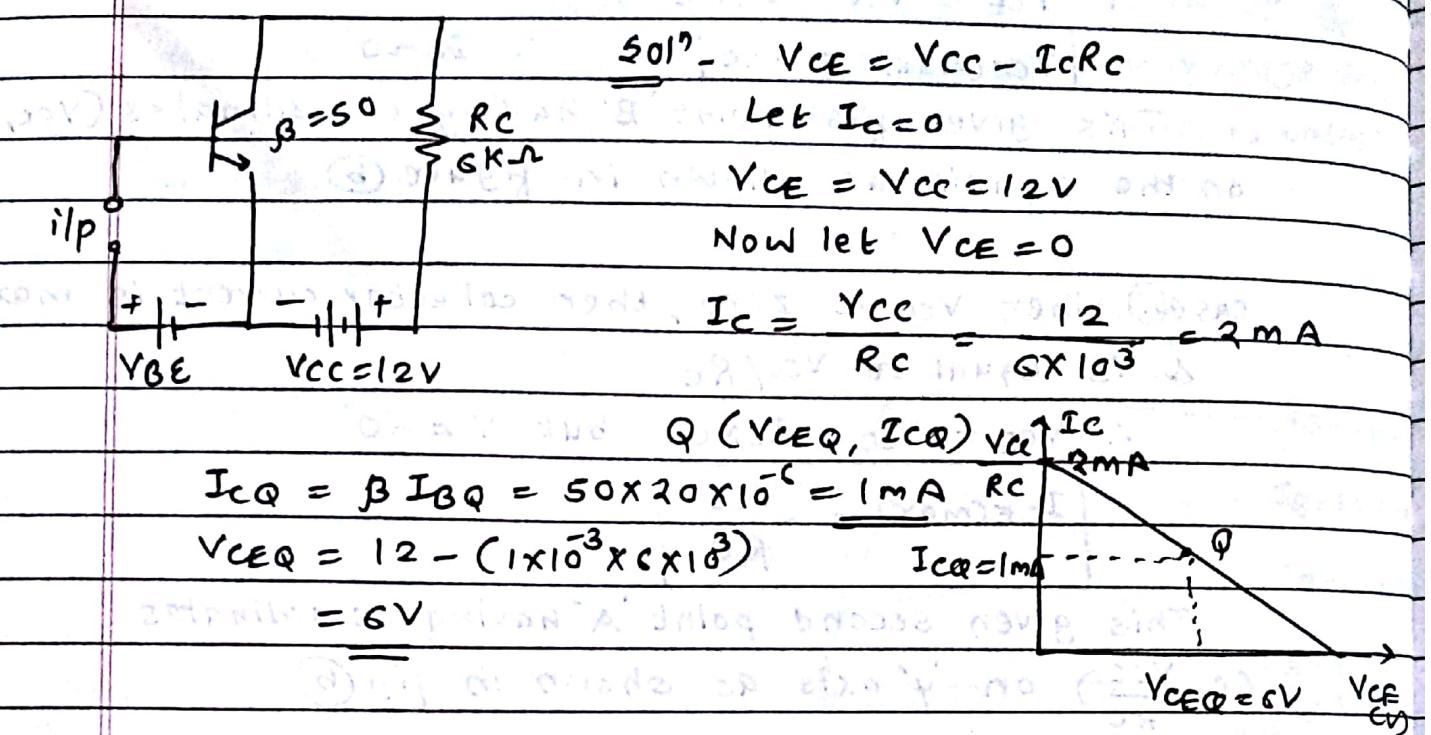
$$V_{CE(\max)} = V_{CC} = 12V$$

case(ii) $V_{CE} = 0$

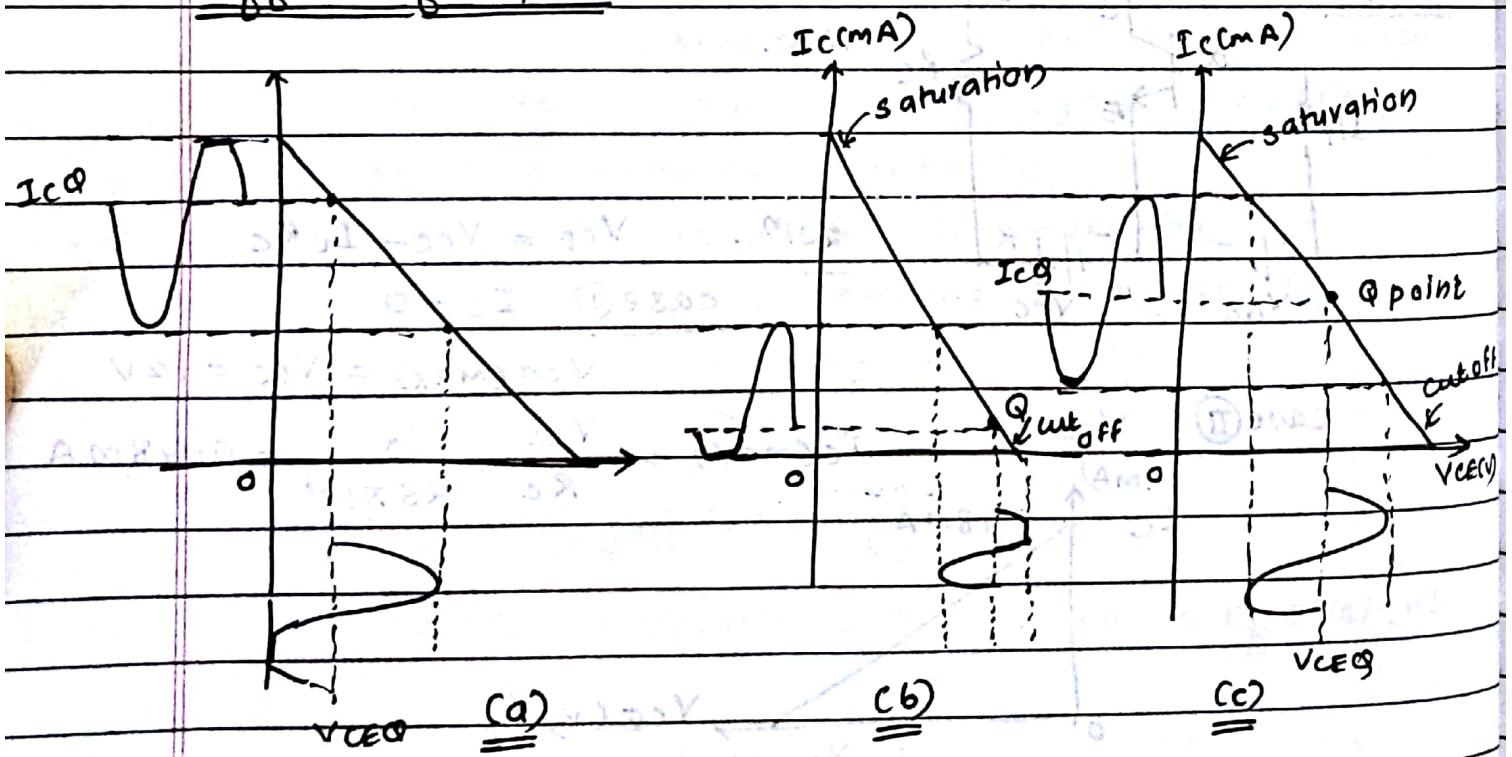
$$I_{C(\max)} = \frac{V_{CC}}{R_C} = \frac{12}{25 \times 10^3} = 0.48mA$$



iii) Draw DC load line, where will be Q point if zero signal
 $I_B = 20\text{mA}$ & $\beta = 50$ ie $I_{BQ} = 20\text{mA}$



* Effect of Q point :-



- It has been observed that under certain condition of QP, the location of Q point on the load line may cause one peak of o/p signal to be clipped.

- If Q point is located near the saturation point as shown in fig @. In this case during -ve half cycle of the i/p, transistor is driven into saturation.

As a result of this, the -ve peak of the i/p signal is clipped at the o/p.

- Consider Q point located near the cut off point as shown in fig (b), the transistor is driven into cut off. therefore, +ve peak of the input signal is clipped at the o/p.

- If Q point is located at the center of the load line as shown in fig (c), we get undistorted signal at the o/p.

* Transistor Biasing Techniques :-

In transistor amplifier circuits, the biasing is done with two power supplies V_{BB} & V_{CC} .

- The V_{BB} is used for biasing of E-B junction & V_{CC} supply for biasing both the junction of transistor.

- Following are the different biasing techniques of BJT.

1. Fixed Bias configuration

2. Emitter Bias configuration

3. collector- feedback configuration

4. Voltage Divider Bias configuration

5. common Base configuration.