2 Diode Applications

CHAPTER OBJECTIVES

- Understand the concept of load-line analysis and how it is applied to diode networks.
- Become familiar with the use of equivalent circuits to analyze series, parallel, and series-parallel diode networks.
- Understand the process of rectification to establish a dc level from a sinusoidal ac input.
- Be able to predict the output response of a clipper and clamper diode configuration.
- Become familiar with the analysis of and the range of applications for Zener diodes.

2.1 INTRODUCTION

The construction, characteristics, and models of semiconductor diodes were introduced in Chapter 1. This chapter will develop a working knowledge of the diode in a variety of configurations using models appropriate for the area of application. By chapter's end, the fundamental behavior pattern of diodes in dc and ac networks should be clearly understood. The concepts learned in this chapter will have significant carryover in the chapters to follow. For instance, diodes are frequently employed in the description of the basic construction of transistors and in the analysis of transistor networks in the dc and ac domains.

This chapter demonstrates an interesting and very useful aspect of the study of a field such as electronic devices and systems:

Once the basic behavior of a device is understood, its function and response in an infinite variety of configurations can be examined.

In other words, now that we have a basic knowledge of the characteristics of a diode along with its response to applied voltages and currents, we can use this knowledge to examine a wide variety of networks. There is no need to reexamine the response of the device for each application.

In general:

The analysis of electronic circuits can follow one of two paths: using the actual characteristics or applying an approximate model for the device.

For the diode the initial discussion will include the actual characteristics to clearly demonstrate how the characteristics of a device and the network parameters interact. Once there is confidence in the results obtained, the approximate piecewise model will be employed to verify the results found using the complete characteristics. It is important that the role and the response of various elements of an electronic system be understood without continually

having to resort to lengthy mathematical procedures. This is usually accomplished through the approximation process, which can develop into an art itself. Although the results obtained using the actual characteristics may be slightly different from those obtained using a series of approximations, keep in mind that the characteristics obtained from a specification sheet may be slightly different from those of the device in actual use. In other words, for example, the characteristics of a 1N4001 semiconductor diode may vary from one element to the next in the same lot. The variation may be slight, but it will often be sufficient to justify the approximations employed in the analysis. Also consider the other elements of the network: Is the resistor labeled 100 Ω exactly 100 Ω? Is the applied voltage exactly 10 V or perhaps 10.08 V? All these tolerances contribute to the general belief that a response determined through an appropriate set of approximations can often be "as accurate" as one that employs the full characteristics. In this book the emphasis is toward developing a working knowledge of a device through the use of appropriate approximations, thereby avoiding an unnecessary level of mathematical complexity. Sufficient detail will normally be provided, however, to permit a detailed mathematical analysis if desired.

2.2 LOAD-LINE ANALYSIS

The circuit of Fig. 2.1 is the simplest of diode configurations. It will be used to describe the analysis of a diode circuit using its actual characteristics. In the next section we will replace the characteristics by an approximate model for the diode and compare solutions. Solving the circuit of Fig. 2.1 is all about finding the current and voltage levels that will satisfy both the characteristics of the diode and the chosen network parameters at the same time.

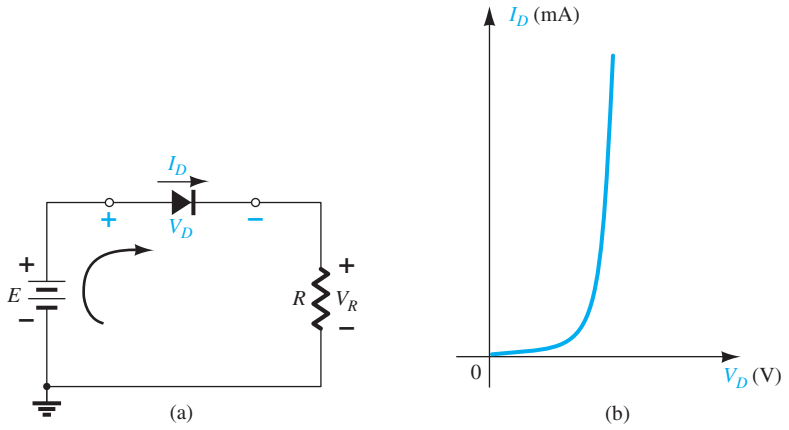


FIG. 2.1
Series diode configuration: (a) circuit; (b) characteristics.

In Fig. 2.2 the diode characteristics are placed on the same set of axes as a straight line defined by the parameters of the network. The straight line is called a *load line* because the intersection on the vertical axis is defined by the applied load *R*. The analysis to follow is therefore called *load-line analysis.* The intersection of the two curves will define the solution for the network and define the current and voltage levels for the network.

Before reviewing the details of drawing the load line on the characteristics, we need to determine the expected response of the simple circuit of Fig. 2.1. Note in Fig. 2.1 that the effect of the "pressure" established by the dc supply is to establish a conventional current in the direction indicated by the clockwise arrow. The fact that the direction of this current has the same direction as the arrow in the diode symbol reveals that the diode is in the "on" state and will conduct a high level of current. The polarity of the applied voltage has resulted in a forward-bias situation. With the current direction established, the polarities for the voltage across the diode and resistor can be superimposed. The polarity of V_D and the direction of I_D clearly reveal that the diode is indeed in the forward-bias state, resulting in a voltage across the diode in the neighborhood of 0.7 V and a current on the order of 10 mA or more.

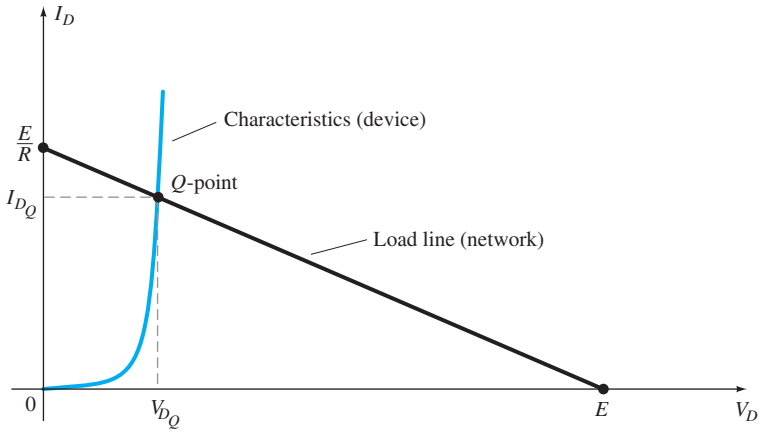


FIG. 2.2
Drawing the load line and finding the point of operation.

The intersections of the load line on the characteristics of Fig. 2.2 can be determined by first applying Kirchhoff's voltage law in the clockwise direction, which results in

$$+E - V_D - V_R = 0$$

or

$$\boxed{E = V_D + I_D R} \tag{2.1}$$

The two variables of Eq. (2.1), V_D and I_D, are the same as the diode axis variables of Fig. 2.2. This similarity permits plotting Eq. (2.1) on the same characteristics of Fig. 2.2.

The intersections of the load line on the characteristics can easily be determined if one simply employs the fact that anywhere on the horizontal axis $I_D = 0$ A and anywhere on the vertical axis $V_D = 0$ V.

If we *set* $V_D = 0$ V in Eq. (2.1) and solve for I_D, we have the magnitude of I_D *on* the vertical axis. Therefore, with $V_D = 0$ V, Eq. (2.1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= 0\,\text{V} + I_D R \end{aligned}$$

and

$$\boxed{I_D = \left.\frac{E}{R}\right|_{V_D = 0\,\text{V}}} \tag{2.2}$$

as shown in Fig. 2.2. If we *set* $I_D = 0$ A in Eq. (2.1) and solve for V_D, we have the magnitude of V_D *on* the horizontal axis. Therefore, with $I_D = 0$ A, Eq. (2.1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= V_D + (0\,\text{A})R \end{aligned}$$

and

$$\boxed{V_D = \left.E\right|_{I_D = 0\,\text{A}}} \tag{2.3}$$

as shown in Fig. 2.2. A straight line drawn between the two points will define the load line as depicted in Fig. 2.2. Change the level of R (the load) and the intersection on the vertical axis will change. The result will be a change in the slope of the load line and a different point of intersection between the load line and the device characteristics.

We now have a load line defined by the network and a characteristic curve defined by the device. The point of intersection between the two is the point of operation for this circuit. By simply drawing a line down to the horizontal axis, we can determine the diode voltage V_{D_Q}, whereas a horizontal line from the point of intersection to the vertical axis will provide the level of I_{D_Q}. The current I_D is actually the current through the entire series configuration of Fig. 2.1a. The point of operation is usually called the *quiescent point* (abbreviated "*Q*-point") to reflect its "still, unmoving" qualities as defined by a dc network.

The solution obtained at the intersection of the two curves is the same as would be obtained by a simultaneous mathematical solution of

$$I_D = \frac{E}{R} - \frac{V_D}{R} \qquad [\text{derived from Eq. (2.1)}]$$

and

$$I_D = I_s(e^{V_D/nV_T} - 1)$$

Since the curve for a diode has nonlinear characteristics, the mathematics involved would require the use of nonlinear techniques that are beyond the needs and scope of this book. The load-line analysis described above provides a solution with a minimum of effort and a "pictorial" description of why the levels of solution for V_{D_Q} and I_{D_Q} were obtained. The next example demonstrates the techniques introduced above and reveals the relative ease with which the load line can be drawn using Eqs. (2.2) and (2.3).

EXAMPLE 2.1 For the series diode configuration of Fig. 2.3a, employing the diode characteristics of Fig. 2.3b, determine:

a. V_{D_Q} and I_{D_Q}.
b. V_R.

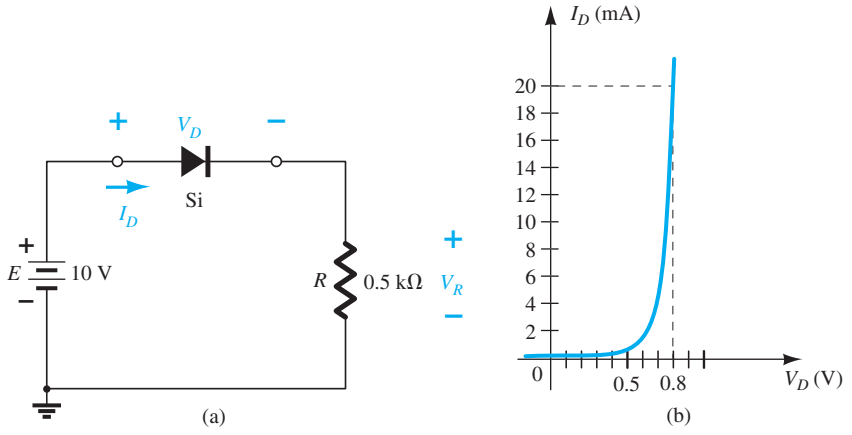


FIG. 2.3
(a) Circuit; (b) characteristics.

Solution:

a. Eq. (2.2): $$I_D = \frac{E}{R}\bigg|_{V_D=0\text{ V}} = \frac{10\text{ V}}{0.5\text{ k}\Omega} = 20\text{ mA}$$

Eq. (2.3): $$V_D = E|_{I_D=0\text{ A}} = 10\text{ V}$$

The resulting load line appears in Fig. 2.4. The intersection between the load line and the characteristic curve defines the Q-point as

$$V_{D_Q} \cong \mathbf{0.78\text{ V}}$$
$$I_{D_Q} \cong \mathbf{18.5\text{ mA}}$$

The level of V_D is certainly an estimate, and the accuracy of I_D is limited by the chosen scale. A higher degree of accuracy would require a plot that would be much larger and perhaps unwieldy.

b. $V_R = E - V_D = 10\text{ V} - 0.78\text{ V} = \mathbf{9.22\text{ V}}$

As noted in the example above,

the load line is determined solely by the applied network, whereas the characteristics are defined by the chosen device.

Changing the model we use for the diode will not disturb the network so the load line to be drawn will be exactly the same as appearing in the example above.

Since the network of Example 2.1 is a dc network the Q-point of Fig.2.4 will remain fixed with $V_{D_Q} = 0.78$ V and $I_{D_Q} = 18.5$ mA. In Chapter 1 a dc resistance was defined at any point on the characteristics by $R_{DC} = V_D/I_D$.

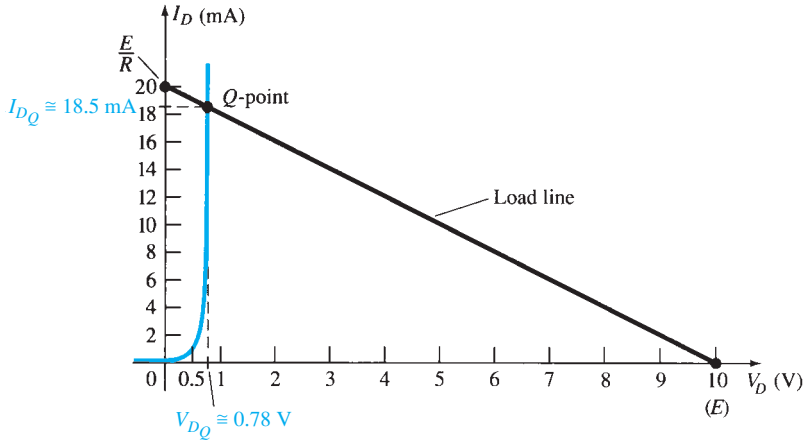


FIG. 2.4
Solution to Example 2.1.

Using the Q-point values, the dc resistance for Example 2.1 is

$$R_D = \frac{V_{D_Q}}{I_{D_Q}} = \frac{0.78\text{ V}}{18.5\text{ mA}} = 42.16\ \Omega$$

An equivalent network (for these operating conditions only) can then be drawn as shown in Fig. 2.5.

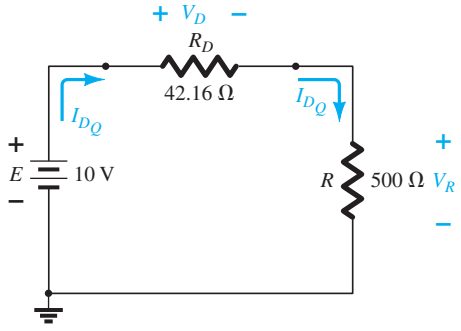


FIG. 2.5
Network quivalent to Fig. 2.4.

The current

$$I_D = \frac{E}{R_D + R} = \frac{10\text{ V}}{42.16\ \Omega + 500\ \Omega} = \frac{10\text{ V}}{542.16\ \Omega} \cong \mathbf{18.5\text{ mA}}$$

and

$$V_R = \frac{RE}{R_D + R} = \frac{(500\ \Omega)(10\text{ V})}{42.16\ \Omega + 500\ \Omega} = \mathbf{9.22\text{ V}}$$

matching the results of Example 2.1.

In essence, therefore, once a dc Q-point has been determined the diode can be replaced by its dc resistance equivalent. This concept of replacing a characteristic by an equivalent model is an important one and will be used when we consider ac inputs and equivalent models for transistors in the chapters to follow. Let us now see what effect different equivalent models for the diode will have on the response in Example 2.1

EXAMPLE 2.2 Repeat Example 2.1 using the approximate equivalent model for the silicon semiconductor diode.

Solution: The load line is redrawn as shown in Fig. 2.6 with the same intersections as defined in Example 2.1. The characteristics of the approximate equivalent circuit for the diode have also been sketched on the same graph. The resulting Q-point is

$$V_{D_Q} = \mathbf{0.7\text{ V}}$$
$$I_{D_Q} = \mathbf{18.5\text{ mA}}$$

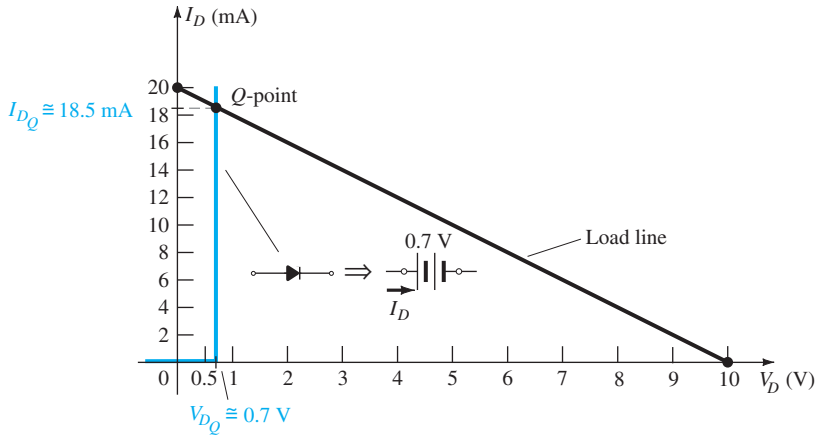


FIG. 2.6
Solution to Example 2.1 using the diode approximate model.

The results obtained in Example 2.2 are quite interesting. The level of I_{D_Q} is exactly the same as obtained in Example 2.1 using a characteristic curve that is a great deal easier to draw than that appearing in Fig. 2.4. The $V_D = 0.7$ V here and the 0.78 V from Example 2.1 are of a different magnitude to the hundredths place, but they are certainly in the same neighborhood if we compare their magnitudes to the magnitudes of the other voltages of the network.

For this situation the dc resistance of the *Q*-point is

$$R_D = \frac{V_{D_Q}}{I_{D_Q}} = \frac{0.7 \text{ V}}{18.5 \text{ mA}} = 37.84\ \Omega$$

which is still relatively close to that obtained for the full characteristics.

In the next example we go a step further and substitute the ideal model. The results will reveal the conditions that must be satisfied to apply the ideal equivalent properly.

EXAMPLE 2.3 Repeat Example 2.1 using the ideal diode model.

Solution: As shown in Fig. 2.7, the load line is the same, but the ideal characteristics now intersect the load line on the vertical axis. The *Q*-point is therefore defined by

$$V_{D_Q} = \mathbf{0\ V}$$
$$I_{D_Q} = \mathbf{20\ mA}$$

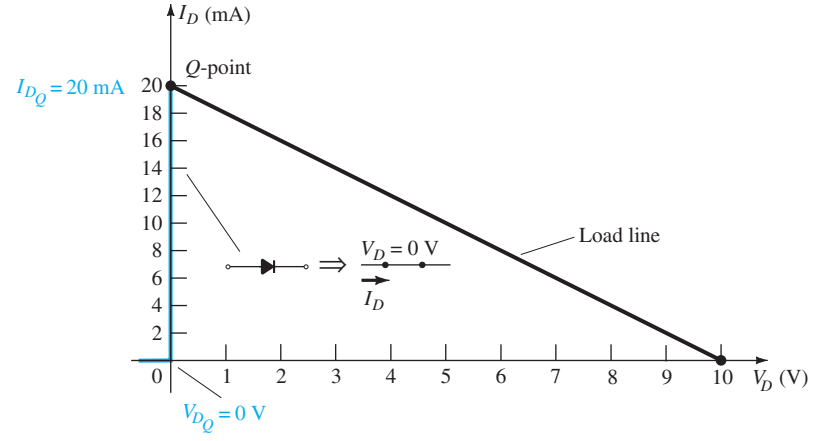


FIG. 2.7
Solution to Example 2.1 using the ideal diode model.

The results are sufficiently different from the solutions of Example 2.1 to cause some concern about their accuracy. Certainly, they do provide some indication of the level of voltage and current to be expected relative to the other voltage levels of the network, but the additional effort of simply including the 0.7-V offset suggests that the approach of Example 2.2 is more appropriate.

Use of the ideal diode model therefore should be reserved for those occasions when the role of a diode is more important than voltage levels that differ by tenths of a volt and in those situations where the applied voltages are considerably larger than the threshold voltage V_K. In the next few sections the approximate model will be employed exclusively since the voltage levels obtained will be sensitive to variations that approach V_K. In later sections the ideal model will be employed more frequently since the applied voltages will frequently be quite a bit larger than V_K and the authors want to ensure that the role of the diode is correctly and clearly understood.

In this case,

$$R_D = \frac{V_{D_Q}}{I_{D_Q}} = \frac{0\text{ V}}{20\text{ mA}} = 0\ \Omega \text{ (or a short-circuit equivalent)}$$

2.3 SERIES DIODE CONFIGURATIONS

In the last section we found that the results obtained using the approximate piecewise-linear equivalent model were quite close, if not equal, to the response obtained using the full characteristics. In fact, if one considers all the variations possible due to tolerances, temperature, and so on, one could certainly consider one solution to be "as accurate" as the other. Since the use of the approximate model normally results in a reduced expenditure of time and effort to obtain the desired results, it is the approach that will be employed in this book unless otherwise specified. Recall the following:

The primary purpose of this text is to develop a general knowledge of the behavior, capabilities, and possible areas of application of a device in a manner that will minimize the need for extensive mathematical developments.

For all the analysis to follow in this chapter it is assumed that

The forward resistance of the diode is usually so small compared to the other series elements of the network that it can be ignored.

This is a valid approximation for the vast majority of applications that employ diodes. Using this fact will result in the approximate equivalents for a silicon diode and an ideal diode that appear in Table 2.1. For the conduction region the only difference between the silicon diode and the ideal diode is the vertical shift in the characteristics, which is accounted for in the equivalent model by a dc supply of 0.7 V opposing the direction of forward current through the device. For voltages less than 0.7 V for a silicon diode and 0 V for the ideal diode the resistance is so high compared to other elements of the network that its equivalent is the open circuit.

For a Ge diode the offset voltage is 0.3 V and for a GaAs diode it is 1.2 V. Otherwise the equivalent networks are the same. For each diode the label Si, Ge, or GaAs will appear along with the diode symbol. For networks with ideal diodes the diode symbol will appear as shown in Table 2.1 without any labels.

The approximate models will now be used to investigate a number of series diode configurations with dc inputs. This will establish a foundation in diode analysis that will carry over into the sections and chapters to follow. The procedure described can, in fact, be applied to networks with any number of diodes in a variety of configurations.

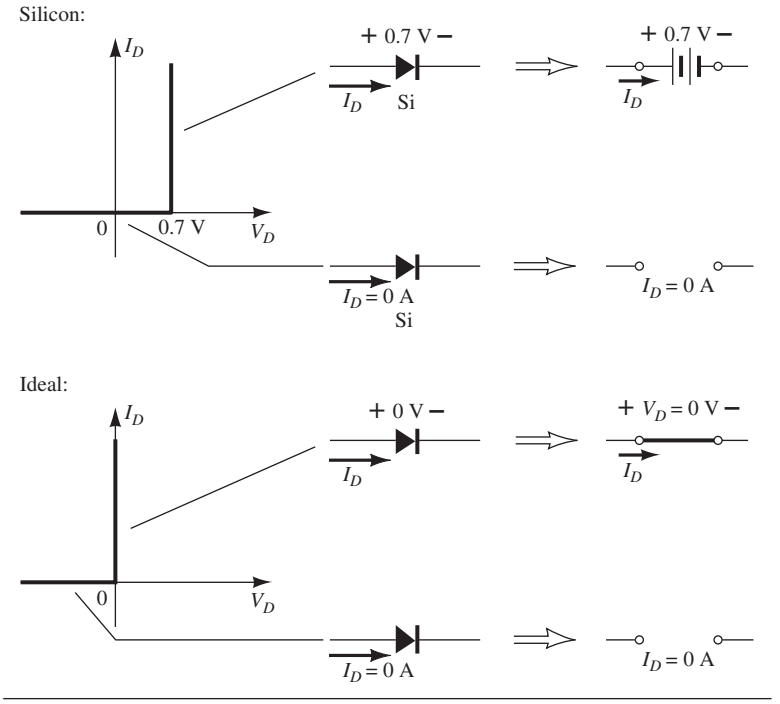
For each configuration the state of each diode must first be determined. Which diodes are "on" and which are "off"? Once determined, the appropriate equivalent can be substituted and the remaining parameters of the network determined.

In general, a diode is in the "on" state if the current established by the applied sources is such that its direction matches that of the arrow in the diode symbol, and $V_D \geq 0.7$ V for silicon, $V_D \geq 0.3$ V for germanium, and $V_D \geq 1.2$ V for gallium arsenide.

For each configuration, *mentally* replace the diodes with resistive elements and note the resulting current direction as established by the applied voltages ("pressure"). If the resulting

TABLE 2.1

Approximate and Ideal Semiconductor Diode Models.



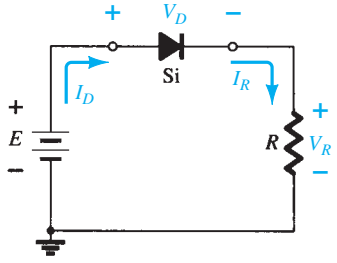


FIG. 2.8

Series diode configuration.

direction is a "match" with the arrow in the diode symbol, conduction through the diode will occur and the device is in the "on" state. The description above is, of course, contingent on the supply having a voltage greater than the "turn-on" voltage (V_K) of each diode.

If a diode is in the "on" state, one can either place a 0.7-V drop across the element or redraw the network with the V_K equivalent circuit as defined in Table 2.1. In time the preference will probably simply be to include the 0.7-V drop across each "on" diode and to draw a diagonal line through each diode in the "off" or open state. Initially, however, the substitution method will be used to ensure that the proper voltage and current levels are determined.

The series circuit of Fig. 2.8 described in some detail in Section 2.2 will be used to demonstrate the approach described in the above paragraphs. The state of the diode is first determined by mentally replacing the diode with a resistive element as shown in Fig. 2.9a. The resulting direction of I is a match with the arrow in the diode symbol, and since $E > V_K$, the diode is in the "on" state. The network is then redrawn as shown in Fig. 2.9b with the appropriate equivalent model for the forward-biased silicon diode. Note for future reference that the polarity of V_D is the same as would result if in fact the diode were a resistive element. The resulting voltage and current levels are the following:

$$V_D = V_K \tag{2.4}$$

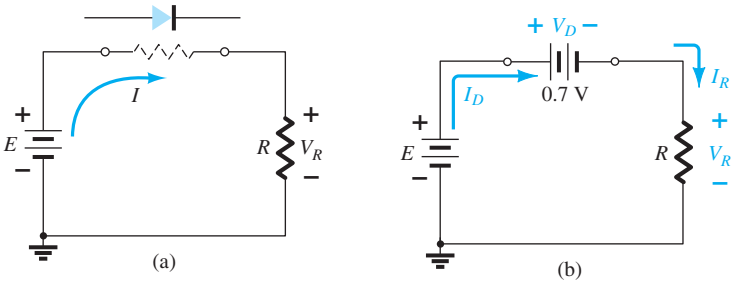


FIG. 2.9

(a) Determining the state of the diode of Fig. 2.8; (b) substituting the equivalent model for the "on" diode of Fig. 2.9a.

$$V_R = E - V_K \tag{2.5}$$

$$I_D = I_R = \frac{V_R}{R} \tag{2.6}$$

In Fig. 2.10 the diode of Fig. 2.7 has been reversed. Mentally replacing the diode with a resistive element as shown in Fig. 2.11 will reveal that the resulting current direction does not match the arrow in the diode symbol. The diode is in the "off" state, resulting in the equivalent circuit of Fig. 2.12. Due to the open circuit, the diode current is 0 A and the voltage across the resistor R is the following:

$$V_R = I_R R = I_D R = (0\text{ A})R = \mathbf{0\text{ V}}$$

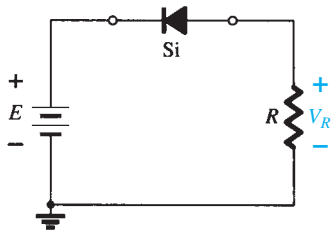


FIG. 2.10
Reversing the diode of Fig. 2.8.

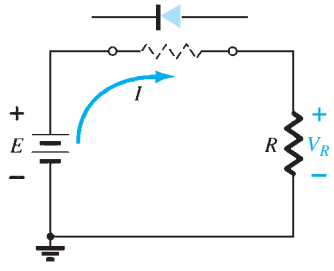


FIG. 2.11
Determining the state of the diode of Fig. 2.10.

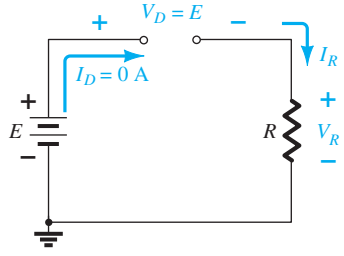


FIG. 2.12
Substituting the equivalent model for the "off" diode of Fig. 2.10.

The fact that $V_R = 0$ V will establish E volts across the open circuit as defined by Kirchhoff's voltage law. Always keep in mind that under any circumstances—dc, ac instantaneous values, pulses, and so on—Kirchhoff's voltage law must be satisfied!

EXAMPLE 2.4 For the series diode configuration of Fig. 2.13, determine V_D, V_R, and I_D.

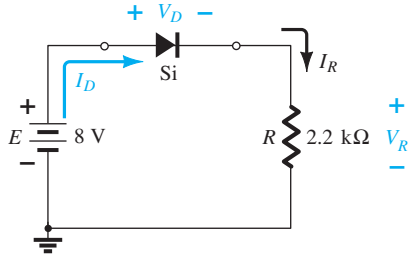


FIG. 2.13
Circuit for Example 2.4.

Solution: Since the applied voltage establishes a current in the clockwise direction to match the arrow of the symbol and the diode is in the "on" state,

$$V_D = \mathbf{0.7\text{ V}}$$

$$V_R = E - V_D = 8\text{ V} - 0.7\text{ V} = \mathbf{7.3\text{ V}}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{7.3\text{ V}}{2.2\text{ k}\Omega} \cong \mathbf{3.32\text{ mA}}$$

EXAMPLE 2.5 Repeat Example 2.4 with the diode reversed.

Solution: Removing the diode, we find that the direction of I is opposite to the arrow in the diode symbol and the diode equivalent is the open circuit no matter which model is employed. The result is the network of Fig. 2.14, where $I_D = \mathbf{0\ A}$ due to the open circuit. Since $V_R = I_R R$, we have $V_R = (0)R = \mathbf{0\ V}$. Applying Kirchhoff's voltage law around the closed loop yields

$$E - V_D - V_R = 0$$

and

$$V_D = E - V_R = E - 0 = E = 8\ \text{V}$$

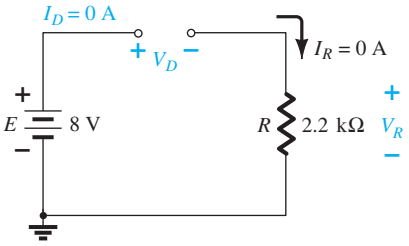


FIG. 2.14
Determining the unknown quantities for Example 2.5.

In particular, note in Example 2.5 the high voltage across the diode even though it is an "off" state. The current is zero, but the voltage is significant. For review purposes, keep the following in mind for the analysis to follow:

An open circuit can have any voltage across its terminals, but the current is always 0 A. A short circuit has a 0-V drop across its terminals, but the current is limited only by the surrounding network.

In the next example the notation of Fig. 2.15 will be employed for the applied voltage. It is a common industry notation and one with which the reader should become very familiar. Such notation and other defined voltage levels are treated further in Chapter 4.

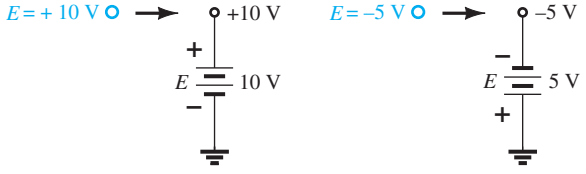


FIG. 2.15
Source notation.

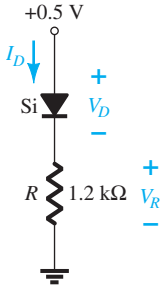


FIG. 2.16
Series diode circuit for Example 2.6.

EXAMPLE 2.6 For the series diode configuration of Fig. 2.16, determine V_D, V_R, and I_D.

Solution: Although the "pressure" establishes a current with the same direction as the arrow symbol, the level of applied voltage is insufficient to turn the silicon diode "on." The point of operation on the characteristics is shown in Fig. 2.17, establishing the open-circuit equivalent as the appropriate approximation, as shown in Fig. 2.18. The resulting voltage and current levels are therefore the following:

$$I_D = \mathbf{0\ A}$$

$$V_R = I_R R = I_D R = (0\ \text{A})\,1.2\ \text{k}\Omega = \mathbf{0\ V}$$

and

$$V_D = E = \mathbf{0.5\ V}$$

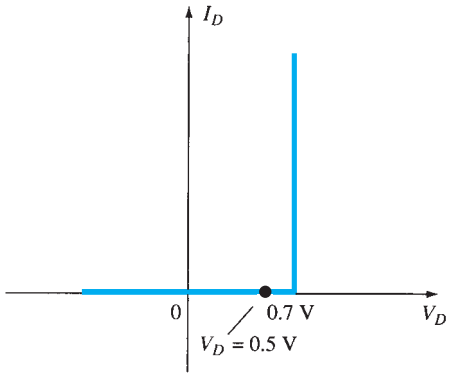


FIG. 2.17
Operating point with E = 0.5 V.

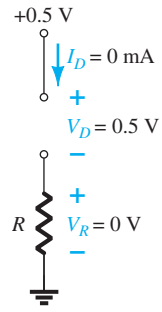


FIG. 2.18
Determining I_D, V_R, and V_D for the circuit of Fig. 2.16.

EXAMPLE 2.7 Determine V_o and I_D for the series circuit of Fig. 2.19.

Solution: An attack similar to that applied in Example 2.4 will reveal that the resulting current has the same direction as the arrowheads of the symbols of both diodes, and the network of Fig. 2.20 results because $E = 12\text{ V} > (0.7\text{ V} + 1.8\text{ V}\ [\text{Table 1.8}]) = 2.5\text{ V}$. Note the redrawn supply of 12 V and the polarity of V_o across the 680-Ω resistor. The resulting voltage is

$$V_o = E - V_{K_1} - V_{K_2} = 12\text{ V} - 2.5\text{ V} = \mathbf{9.5\text{ V}}$$

and

$$I_D = I_R = \frac{V_R}{R} = \frac{V_o}{R} = \frac{9.5\text{ V}}{680\ \Omega} = \mathbf{13.97\text{ mA}}$$

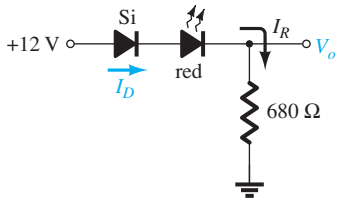


FIG. 2.19
Circuit for Example 2.7.

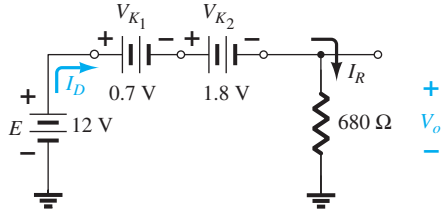


FIG. 2.20
Determining the unknown quantities for Example 2.7.

EXAMPLE 2.8 Determine I_D, V_{D_2}, and V_o for the circuit of Fig. 2.21.

Solution: Removing the diodes and determining the direction of the resulting current I result in the circuit of Fig. 2.22. There is a match in current direction for one silicon diode but not for the other silicon diode. The combination of a short circuit in series with an open circuit always results in an open circuit and $I_D = \mathbf{0\text{ A}}$, as shown in Fig. 2.23.

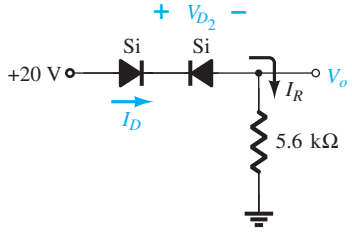


FIG. 2.21
Circuit for Example 2.8.

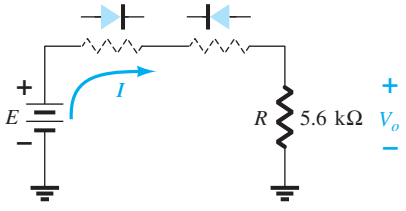


FIG. 2.22
Determining the state of the diodes of Fig. 2.21.

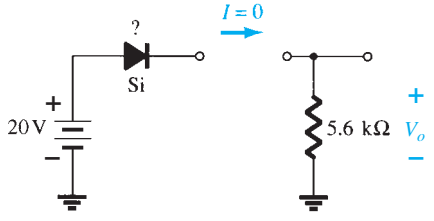


FIG. 2.23
Substituting the equivalent state for the open diode.

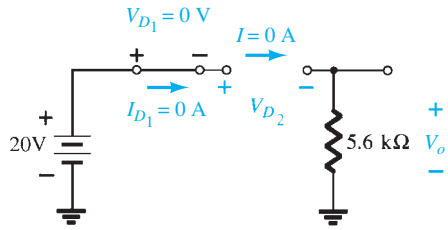


FIG. 2.24
Determining the unknown quantities for the circuit of Example 2.8.

The question remains as to what to substitute for the silicon diode. For the analysis to follow in this and succeeding chapters, simply recall for the actual practical diode that when $I_D = 0$ A, $V_D = 0$ V (and vice versa), as described for the no-bias situation in Chapter 1. The conditions described by $I_D = 0$ A and $V_{D_1} = 0$ V are indicated in Fig. 2.24. We have

$$V_o = I_R R = I_D R = (0\text{ A})R = \mathbf{0\text{ V}}$$

and

$$V_{D_2} = V_{\text{open circuit}} = E = \mathbf{20\text{ V}}$$

Applying Kirchhoff's voltage law in a clockwise direction gives

$$E - V_{D_1} - V_{D_2} - V_o = 0$$

and

$$V_{D_2} = E - V_{D_1} - V_o = 20\text{ V} - 0 - 0$$
$$= \mathbf{20\text{ V}}$$

with

$$V_o = \mathbf{0\text{ V}}$$

EXAMPLE 2.9 Determine I, V_1, V_2, and V_o for the series dc configuration of Fig. 2.25.

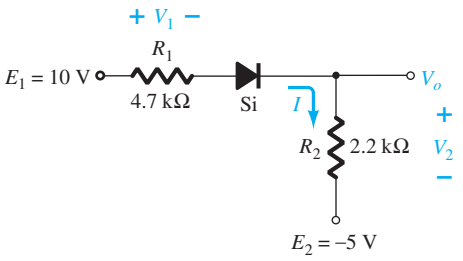


FIG. 2.25
Circuit for Example 2.9.

Solution: The sources are drawn and the current direction indicated as shown in Fig. 2.26. The diode is in the "on" state and the notation appearing in Fig. 2.27 is included to indicate this state. Note that the "on" state is noted simply by the additional $V_D = 0.7$ V on the figure. This eliminates the need to redraw the network and avoids any confusion that may

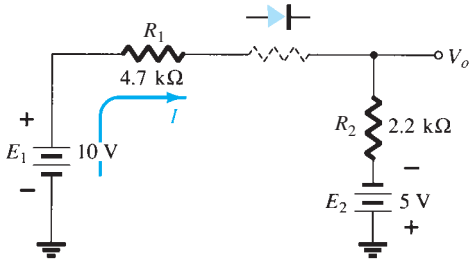


FIG. 2.26
Determining the state of the diode for the network of Fig. 2.25.

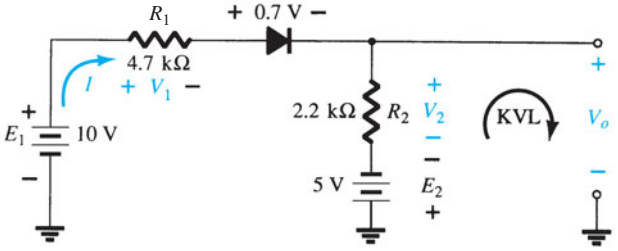


FIG. 2.27
Determining the unknown quantities for the network of Fig. 2.25. KVL, Kirchhoff voltage loop.

result from the appearance of another source. As indicated in the introduction to this section, this is probably the path and notation that one will take when a level of confidence has been established in the analysis of diode configurations. In time the entire analysis will be performed simply by referring to the original network. Recall that a reverse-biased diode can simply be indicated by a line through the device.

The resulting current through the circuit is

$$I = \frac{E_1 + E_2 - V_D}{R_1 + R_2} = \frac{10\text{ V} + 5\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega + 2.2\text{ k}\Omega} = \frac{14.3\text{ V}}{6.9\text{ k}\Omega}$$
$$\cong \mathbf{2.07\text{ mA}}$$

and the voltages are

$$V_1 = IR_1 = (2.07\text{ mA})(4.7\text{ k}\Omega) = \mathbf{9.73\text{ V}}$$
$$V_2 = IR_2 = (2.07\text{ mA})(2.2\text{ k}\Omega) = \mathbf{4.55\text{ V}}$$

Applying Kirchhoff's voltage law to the output section in the clockwise direction results in

$$-E_2 + V_2 - V_o = 0$$

and

$$V_o = V_2 - E_2 = 4.55\text{ V} - 5\text{ V} = \mathbf{-0.45\text{ V}}$$

The minus sign indicates that V_o has a polarity opposite to that appearing in Fig. 2.25.

2.4 PARALLEL AND SERIES–PARALLEL CONFIGURATIONS

The methods applied in Section 2.3 can be extended to the analysis of parallel and series–parallel configurations. For each area of application, simply match the sequential series of steps applied to series diode configurations.

EXAMPLE 2.10 Determine V_o, I_1, I_{D_1}, and I_{D_2} for the parallel diode configuration of Fig. 2.28.

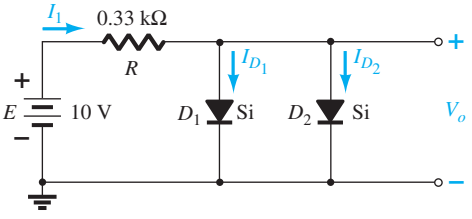


FIG. 2.28
Network for Example 2.10.

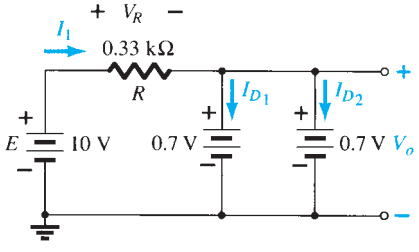


FIG. 2.29
Determining the unknown quantities for the network of Example 2.10.

Solution: For the applied voltage the "pressure" of the source acts to establish a current through each diode in the same direction as shown in Fig. 2.29. Since the resulting current direction matches that of the arrow in each diode symbol and the applied voltage is greater than 0.7 V, both diodes are in the "on" state. The voltage across parallel elements is always the same and

$$V_o = \mathbf{0.7\text{ V}}$$

The current is

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{0.33\text{ k}\Omega} = \mathbf{28.18\text{ mA}}$$

Assuming diodes of similar characteristics, we have

$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\text{ mA}}{2} = \mathbf{14.09\text{ mA}}$$

This example demonstrates one reason for placing diodes in parallel. If the current rating of the diodes of Fig. 2.28 is only 20 mA, a current of 28.18 mA would damage the device if it appeared alone in Fig. 2.28. By placing two in parallel, we limit the current to a safe value of 14.09 mA with the same terminal voltage.

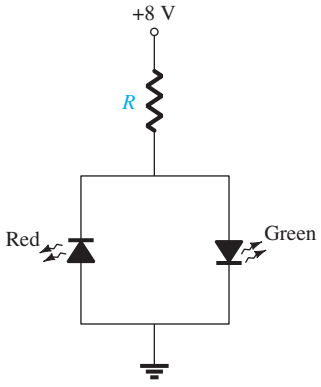


FIG. 2.30
Network for Example 2.11.

EXAMPLE 2.11 In this example there are two LEDs that can be used as a polarity detector. Apply a positive source voltage and a green light results. Negative supplies result in a red light. Packages of such combinations are commercially available.

Find the resistor R to ensure a current of 20 mA through the "on" diode for the configuration of Fig. 2.30. Both diodes have a reverse breakdown voltage of 3 V and an average turn-on voltage of 2 V.

Solution: The application of a positive supply voltage results in a conventional current that matches the arrow of the green diode and turns it on.

The polarity of the voltage across the green diode is such that it reverse biases the red diode by the same amount. The result is the equivalent network of Fig. 2.31.

Applying Ohm's law, we obtain

$$I = 20\text{ mA} = \frac{E - V_{\text{LED}}}{R} = \frac{8\text{ V} - 2\text{ V}}{R}$$

and

$$R = \frac{6\text{ V}}{20\text{ mA}} = \mathbf{300\ \Omega}$$

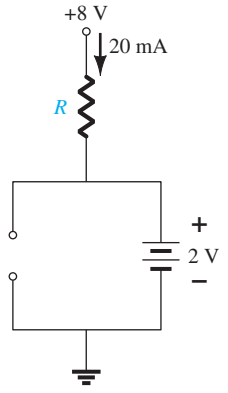


FIG. 2.31
Operating conditions for the network of Fig. 2.30.

Note that the reverse breakdown voltage across the red diode is 2 V, which is fine for an LED with a reverse breakdown voltage of 3 V.

However, if the green diode were to be replaced by a blue diode, problems would develop, as shown in Fig. 2.32. Recall that the forward bias required to turn on a blue diode is about 5 V. The result would appear to require a smaller resistor R to establish the current of 20 mA. However, note that the reverse bias voltage of the red LED is 5 V, but the reverse breakdown voltage of the diode is only 3 V. The result is the voltage across the red LED would lock in at 3 V as shown in Fig. 2.33. The voltage across R would be 5 V and the current limited to 20 mA with a 250 Ω resistor but neither LED would be on.

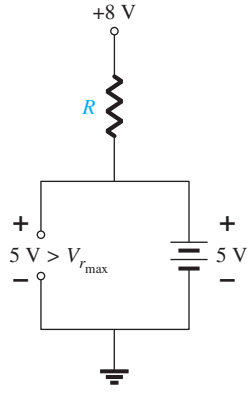


FIG. 2.32
Network of Fig. 2.31 with a blue diode.

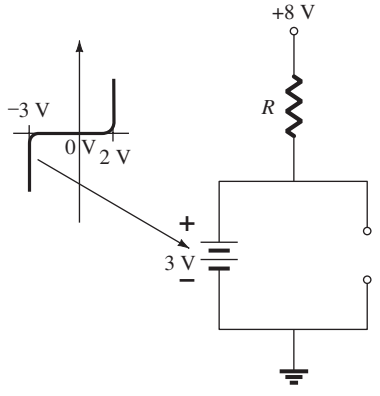


FIG. 2.33
Demonstrating damage to the red LED if the reverse breakdown voltage is exceeded.

A simple solution to the above is to add the appropriate resistance level in series with each diode to establish the desired 20 mA and to include another diode to add to the reverse-bias total reverse breakdown voltage rating, as shown in Fig. 2.34. When the blue LED is on, the diode in series with the blue LED will also be on, causing a total voltage drop of 5.7 V across the two series diodes and a voltage of 2.3 V across the resistor R_1, establishing a high emission current of 19.17 mA. At the same time the red LED diode and

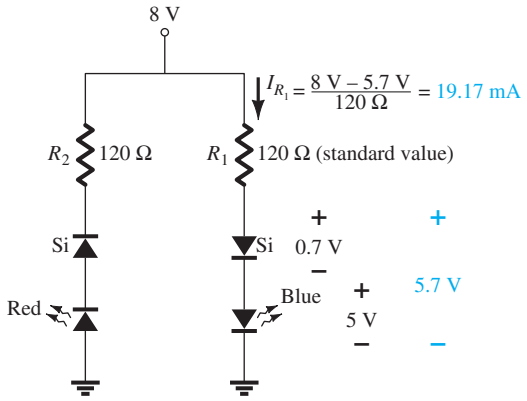


FIG. 2.34
Protective measure for the red LED of Fig. 2.33.

its series diode will also be reverse biased, but now the standard diode with a reverse breakdown voltage of 20 V will prevent the full reverse-bias voltage of 8 V from appearing across the red LED. When forward biased, the resistor R_2 will establish a current of 19.63 mA to ensure a high level of intensity for the red LED.

EXAMPLE 2.12 Determine the voltage V_o for the network of Fig. 2.35.

Solution: Initially, it might appear that the applied voltage will turn both diodes "on" because the applied voltage ("pressure") is trying to establish a conventional current through each diode that would suggest the "on" state. However, if both were on, there would be more than one voltage across the parallel diodes, violating one of the basic rules of network analysis: The voltage must be the same across parallel elements.

The resulting action can best be explained by remembering that there is a period of build-up of the supply voltage from 0 V to 12 V even though it may take milliseconds or microseconds. At the instant the increasing supply voltage reaches 0.7 V the silicon diode will turn "on" and maintain the level of 0.7 V since the characteristic is vertical at this voltage—the current of the silicon diode will simply rise to the defined level. The result is that the voltage across the green LED will never rise above 0.7 V and will remain in the equivalent open-circuit state as shown in Fig. 2.36.

The result is

$$V_o = 12\text{ V} - 0.7\text{ V} = \mathbf{11.3\text{ V}}$$

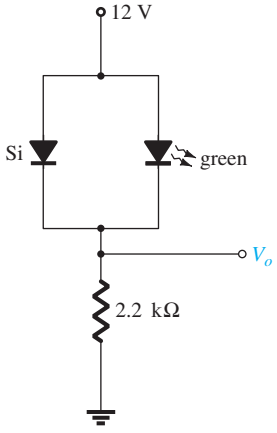


FIG. 2.35
Network for Example 2.12.

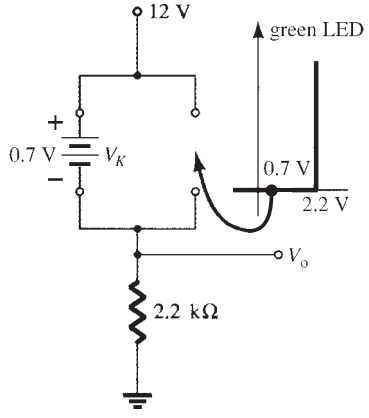


FIG. 2.36
Determining V_o for the network of Fig. 2.35.

EXAMPLE 2.13 Determine the currents I_1, I_2, and I_{D_2} for the network of Fig. 2.37.

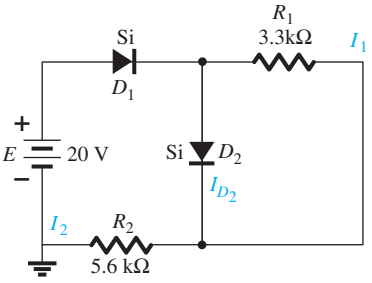


FIG. 2.37
Network for Example 2.13.

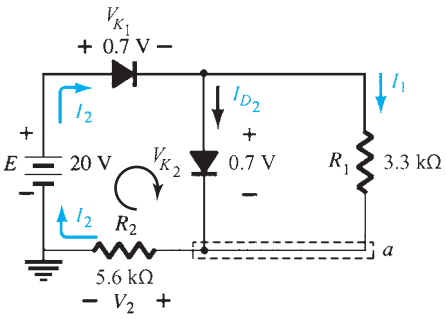


FIG. 2.38
Determining the unknown quantities for Example 2.13.

Solution: The applied voltage (pressure) is such as to turn both diodes on, as indicated by the resulting current directions in the network of Fig. 2.38. Note the use of the abbreviated notation for "on" diodes and that the solution is obtained through an application of techniques applied to dc series–parallel networks. We have

$$I_1 = \frac{V_{K_2}}{R_1} = \frac{0.7\text{ V}}{3.3\text{ k}\Omega} = \mathbf{0.212\text{ mA}}$$

Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction yields

$$-V_2 + E - V_{K_1} - V_{K_2} = 0$$

and

$$V_2 = E - V_{K_1} - V_{K_2} = 20\text{ V} - 0.7\text{ V} - 0.7\text{ V} = \mathbf{18.6\text{ V}}$$

with

$$I_2 = \frac{V_2}{R_2} = \frac{18.6\text{ V}}{5.6\text{ k}\Omega} = \mathbf{3.32\text{ mA}}$$

At the bottom node a,

$$I_{D_2} + I_1 = I_2$$

and

$$I_{D_2} = I_2 - I_1 = 3.32\text{ mA} - 0.212\text{ mA} \cong \mathbf{3.11\text{ mA}}$$

2.5 AND/OR GATES

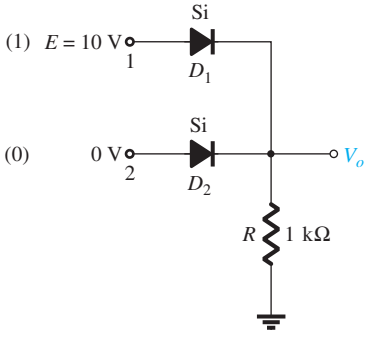


FIG. 2.39
Positive logic OR gate.

The tools of analysis are now at our disposal, and the opportunity to investigate a computer configuration is one that will demonstrate the range of applications of this relatively simple device. Our analysis will be limited to determining the voltage levels and will not include a detailed discussion of Boolean algebra or positive and negative logic.

The network to be analyzed in Example 2.14 is an OR gate for positive logic. That is, the 10-V level of Fig. 2.39 is assigned a "1" for Boolean algebra and the 0-V input is assigned a "0." An OR gate is such that the output voltage level will be a 1 if either *or* both inputs is a 1. The output is a 0 if both inputs are at the 0 level.

The analysis of AND/OR gates is made easier by using the approximate equivalent for a diode rather than the ideal because we can stipulate that the voltage across the diode must be 0.7 V positive for the silicon diode to switch to the "on" state.

In general, the best approach is simply to establish a "gut" feeling for the state of the diodes by noting the direction and the "pressure" established by the applied potentials. The analysis will then verify or negate your initial assumptions.

EXAMPLE 2.14 Determine V_o for the network of Fig. 2.39.

Solution: First note that there is only one applied potential; 10 V at terminal 1. Terminal 2 with a 0-V input is essentially at ground potential, as shown in the redrawn network of

Fig. 2.40. Figure 2.40 "suggests" that D_1 is probably in the "on" state due to the applied 10 V, whereas D_2 with its "positive" side at 0 V is probably "off." Assuming these states will result in the configuration of Fig. 2.41.

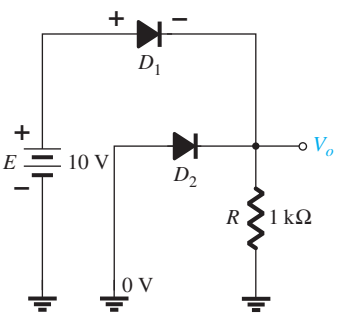


FIG. 2.40
Redrawn network of Fig. 2.39.

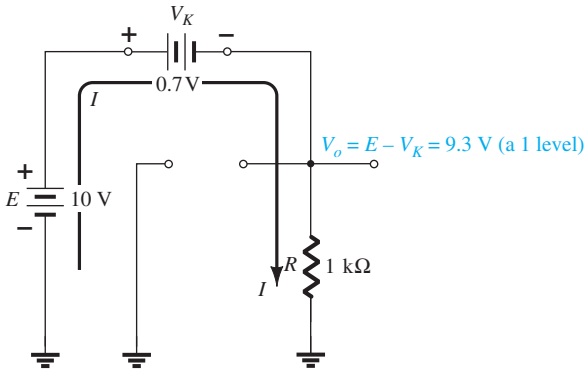


FIG. 2.41
Assumed diode states for Fig. 2.40.

The next step is simply to check that there is no contradiction in our assumptions. That is, note that the polarity across D_1 is such as to turn it on and the polarity across D_2 is such as to turn it off. For D_1 the "on" state establishes V_o at $V_o = E - V_D = 10\text{ V} - 0.7\text{ V} = \mathbf{9.3\text{ V}}$. With 9.3 V at the cathode (−) side of D_2 and 0 V at the anode (+) side, D_2 is definitely in the "off" state. The current direction and the resulting continuous path for conduction further confirm our assumption that D_1 is conducting. Our assumptions seem confirmed by the resulting voltages and current, and our initial analysis can be assumed to be correct. The output voltage level is not 10 V as defined for an input of 1, but the 9.3 V is sufficiently large to be considered a 1 level. The output is therefore at a 1 level with only one input, which suggests that the gate is an OR gate. An analysis of the same network with two 10-V inputs will result in both diodes being in the "on" state and an output of 9.3 V. A 0-V input at both inputs will not provide the 0.7 V required to turn the diodes on, and the output will be a 0 due to the 0-V output level. For the network of Fig. 2.41 the current level is determined by

$$I = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\text{ mA}}$$

EXAMPLE 2.15 Determine the output level for the positive logic AND gate of Fig. 2.42. An AND gate is one where a 1 output is only obtained when a 1 input appears at each and every input.

Solution: Note in this case that an independent source appears in the grounded leg of the network. For reasons soon to become obvious, it is chosen at the same level as the input logic level. The network is redrawn in Fig. 2.43 with our initial assumptions regarding the state of the diodes. With 10 V at the cathode side of D_1 it is assumed that D_1 is in the "off" state even though there is a 10-V source connected to the anode of D_1 through the resistor.

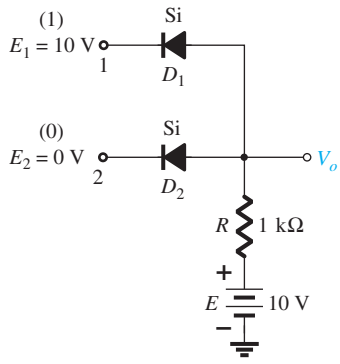


FIG. 2.42
Positive logic AND gate.

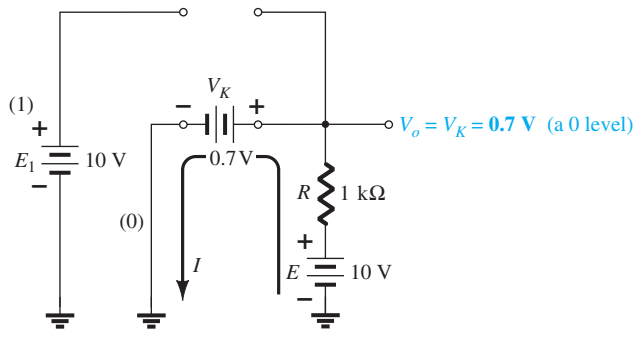


FIG. 2.43
Substituting the assumed states for the diodes of Fig. 2.42.

However, recall that we mentioned in the introduction to this section that the use of the approximate model will be an aid to the analysis. For D_1, where will the 0.7 V come from if the input and source voltages are at the same level and creating opposing "pressures"? D_2 is assumed to be in the "on" state due to the low voltage at the cathode side and the availability of the 10-V source through the 1-kΩ resistor.

For the network of Fig. 2.43 the voltage at V_o is 0.7 V due to the forward-biased diode D_2. With 0.7 V at the anode of D_1 and 10 V at the cathode, D_1 is definitely in the "off" state. The current I will have the direction indicated in Fig. 2.43 and a magnitude equal to

$$I = \frac{E - V_K}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\text{ mA}}$$

The state of the diodes is therefore confirmed and our earlier analysis was correct. Although not 0 V as earlier defined for the 0 level, the output voltage is sufficiently small to be considered a 0 level. For the AND gate, therefore, a single input will result in a 0-level output. The remaining states of the diodes for the possibilities of two inputs and no inputs will be examined in the problems at the end of the chapter.

2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

The diode analysis will now be expanded to include time-varying functions such as the sinusoidal waveform and the square wave. There is no question that the degree of difficulty will increase, but once a few fundamental maneuvers are understood, the analysis will be fairly direct and follow a common thread.

The simplest of networks to examine with a time-varying signal appears in Fig. 2.44. For the moment we will use the ideal model (note the absence of the Si, Ge, or GaAs label) to ensure that the approach is not clouded by additional mathematical complexity.

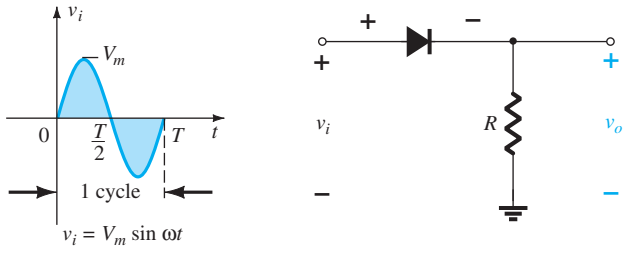


FIG. 2.44
Half-wave rectifier.

Over one full cycle, defined by the period T of Fig. 2.44, the average value (the algebraic sum of the areas above and below the axis) is zero. The circuit of Fig. 2.44, called a *half-wave rectifier*, will generate a waveform v_o that will have an average value of particular use in the ac-to-dc conversion process. When employed in the rectification process, a diode is typically referred to as a *rectifier*. Its power and current ratings are typically much higher than those of diodes employed in other applications, such as computers and communication systems.

During the interval $t = 0 \rightarrow T/2$ in Fig. 2.44 the polarity of the applied voltage v_i is such as to establish "pressure" in the direction indicated and turn on the diode with the polarity appearing above the diode. Substituting the short-circuit equivalence for the ideal diode will result in the equivalent circuit of Fig. 2.45, where it is fairly obvious that the output signal is an exact replica of the applied signal. The two terminals defining the output voltage are connected directly to the applied signal via the short-circuit equivalence of the diode.

For the period $T/2 \rightarrow T$, the polarity of the input v_i is as shown in Fig. 2.46, and the resulting polarity across the ideal diode produces an "off" state with an open-circuit equivalent. The result is the absence of a path for charge to flow, and $v_o = iR = (0)R = 0$ V for the period $T/2 \rightarrow T$. The input v_i and the output v_o are sketched together in Fig. 2.47 for comparison purposes. The output signal v_o now has a net positive area above the axis over

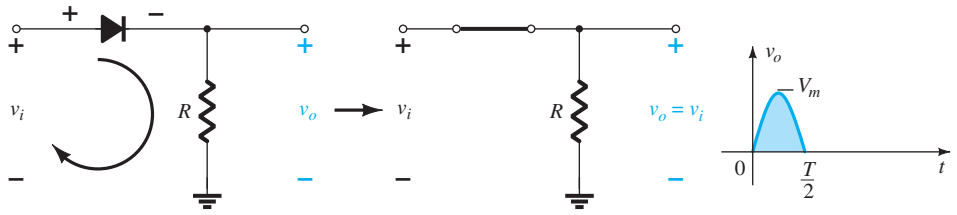


FIG. 2.45
Conduction region ($0 \rightarrow T/2$).

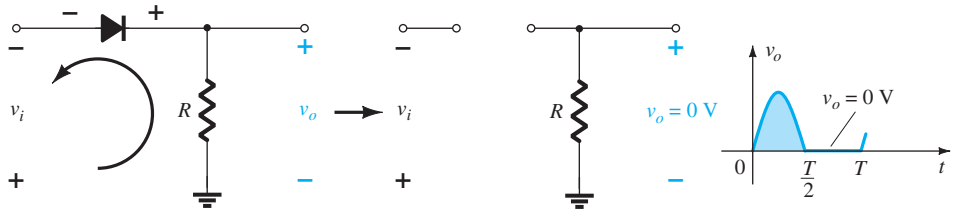


FIG. 2.46
Nonconduction region ($T/2 \rightarrow T$).

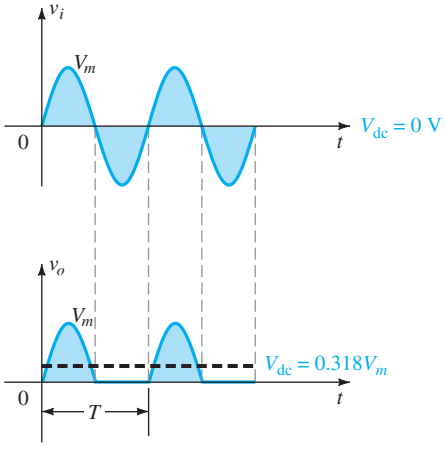


FIG. 2.47
Half-wave rectified signal.

a full period and an average value determined by

$$V_{dc} = 0.318\,V_m \quad \text{half-wave} \tag{2.7}$$

The process of removing one-half the input signal to establish a dc level is called *half-wave rectification*.

The effect of using a silicon diode with $V_K = 0.7$ V is demonstrated in Fig. 2.48 for the forward-bias region. The applied signal must now be at least 0.7 V before the diode can turn "on." For levels of v_i less than 0.7 V, the diode is still in an open-circuit state and $v_o = 0$ V, as shown in the same figure. When conducting, the difference between v_o and v_i is a fixed

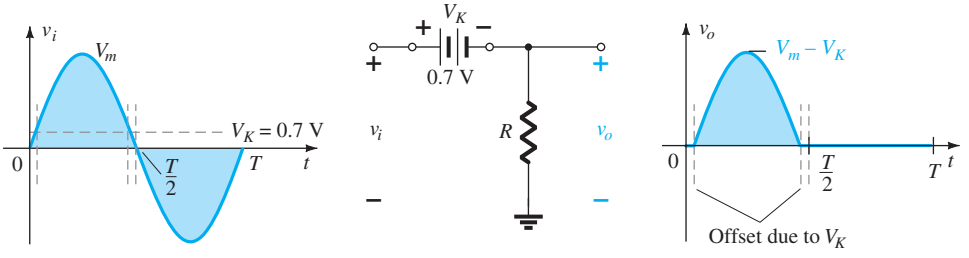


FIG. 2.48
Effect of V_K on half-wave rectified signal.

level of $V_K = 0.7$ V and $v_o = v_i - V_K$, as shown in the figure. The net effect is a reduction in area above the axis, which reduces the resulting dc voltage level. For situations where $V_m \gg V_K$, the following equation can be applied to determine the average value with a relatively high level of accuracy.

$$V_{dc} \cong 0.318(V_m - V_K) \tag{2.8}$$

In fact, if V_m is sufficiently greater than V_K, Eq. (2.7) is often applied as a first approximation for V_{dc}.

EXAMPLE 2.16

a. Sketch the output v_o and determine the dc level of the output for the network of Fig. 2.49.
b. Repeat part (a) if the ideal diode is replaced by a silicon diode.
c. Repeat parts (a) and (b) if V_m is increased to 200 V, and compare solutions using Eqs. (2.7) and (2.8).

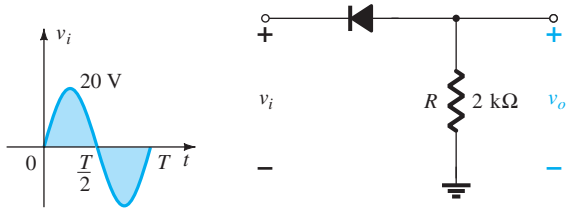


FIG. 2.49
Network for Example 2.16.

Solution:

a. In this situation the diode will conduct during the negative part of the input as shown in Fig. 2.50, and v_o will appear as shown in the same figure. For the full period, the dc level is

$$V_{dc} = -0.318V_m = -0.318(20\text{ V}) = \mathbf{-6.36\text{ V}}$$

The negative sign indicates that the polarity of the output is opposite to the defined polarity of Fig. 2.49.

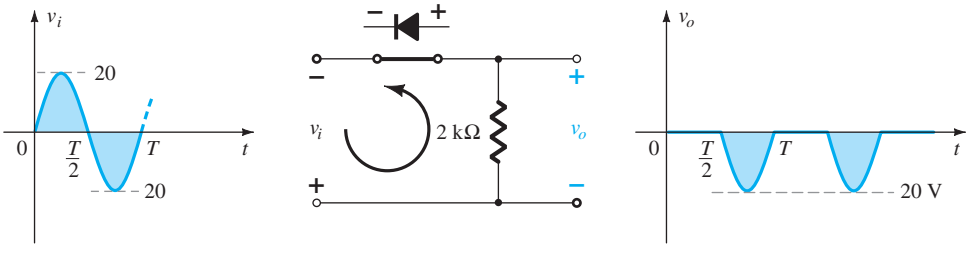


FIG. 2.50
Resulting v_o for the circuit of Example 2.16.

b. For a silicon diode, the output has the appearance of Fig. 2.51, and

$$V_{dc} \cong -0.318(V_m - 0.7\text{ V}) = -0.318(19.3\text{ V}) \cong \mathbf{-6.14\text{ V}}$$

The resulting drop in dc level is 0.22 V, or about 3.5%.

c. Eq. (2.7): $V_{dc} = -0.318\,V_m = -0.318(200\text{ V}) = \mathbf{-63.6\text{ V}}$

Eq. (2.8): $V_{dc} = -0.318(V_m - V_K) = -0.318(200\text{ V} - 0.7\text{ V})$

$= -(0.318)(199.3\text{ V}) = \mathbf{-63.38\text{ V}}$

which is a difference that can certainly be ignored for most applications. For part (c) the offset and drop in amplitude due to V_K would not be discernible on a typical oscilloscope if the full pattern is displayed.

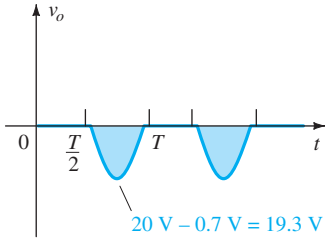


FIG. 2.51
Effect of V_K on output of Fig. 2.50.

PIV (PRV)

The peak inverse voltage (PIV) [or PRV (peak reverse voltage)] rating of the diode is of primary importance in the design of rectification systems. Recall that it is the voltage rating that must not be exceeded in the reverse-bias region or the diode will enter the Zener avalanche region. The required PIV rating for the half-wave rectifier can be determined from Fig. 2.52, which displays the reverse-biased diode of Fig. 2.44 with maximum applied voltage. Applying Kirchhoff's voltage law, it is fairly obvious that the PIV rating of the diode must equal or exceed the peak value of the applied voltage. Therefore,

$$\text{PIV rating} \geqq V_m \quad \text{half-wave rectifier} \tag{2.9}$$

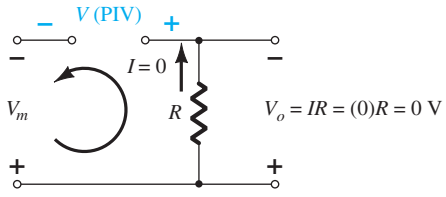
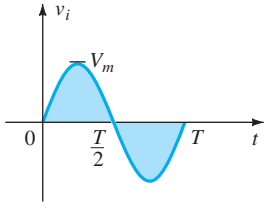


FIG. 2.52
Determining the required PIV rating for the half-wave rectifier.

2.7 FULL-WAVE RECTIFICATION

Bridge Network

The dc level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification*. The most familiar network for performing such a function appears in Fig. 2.53 with its four diodes in a *bridge* configuration. During the period $t = 0$ to $T/2$ the polarity of the input is as shown in Fig. 2.54. The resulting polarities across the ideal diodes are also shown in Fig. 2.54 to reveal that D_2 and D_3 are conducting, whereas D_1 and D_4 are in the "off" state. The net result is the configuration of Fig. 2.55, with its indicated current and polarity across R. Since the diodes are ideal, the load voltage is $v_o = v_i$, as shown in the same figure.



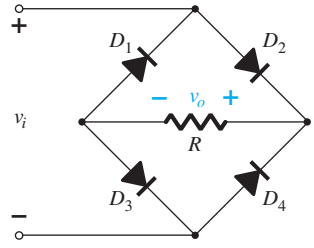


FIG. 2.53
Full-wave bridge rectifier.

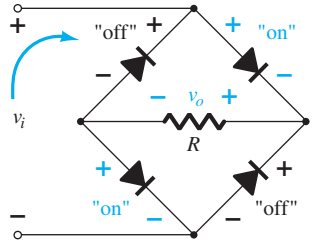
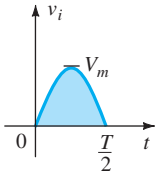
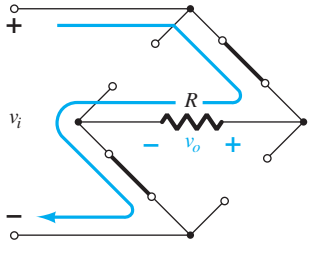


FIG. 2.54
Network of Fig. 2.53 for the period $0 \rightarrow T/2$ of the input voltage v_i.





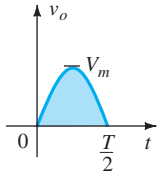


FIG. 2.55
Conduction path for the positive region of v_i.

For the negative region of the input the conducting diodes are D_1 and D_4, resulting in the configuration of Fig. 2.56. The important result is that the polarity across the load resistor R is the same as in Fig. 2.54, establishing a second positive pulse, as shown in Fig. 2.56. Over one full cycle the input and output voltages will appear as shown in Fig. 2.57.

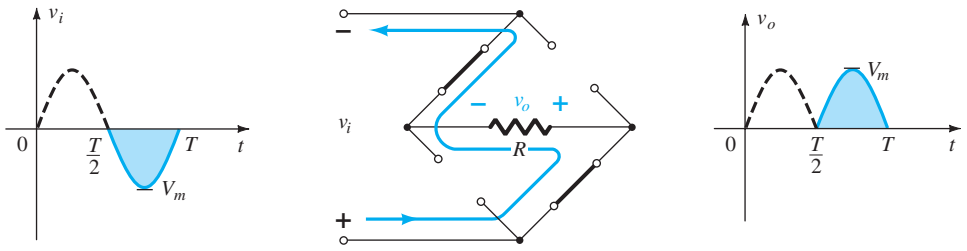


FIG. 2.56
Conduction path for the negative region of v_i.

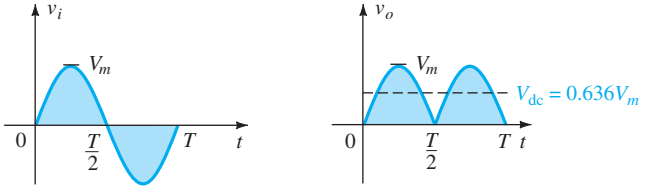


FIG. 2.57
Input and output waveforms for a full-wave rectifier.

Since the area above the axis for one full cycle is now twice that obtained for a half-wave system, the dc level has also been doubled and

$$V_{dc} = 2[\text{Eq. (2.7)}] = 2(0.318V_m)$$

or

$$\boxed{V_{dc} = 0.636\,V_m} \quad \text{full-wave} \tag{2.10}$$

If silicon rather than ideal diodes are employed as shown in Fig. 2.58, the application of Kirchhoff's voltage law around the conduction path results in

$$v_i - V_K - v_o - V_K = 0$$

and

$$v_o = v_i - 2V_K$$

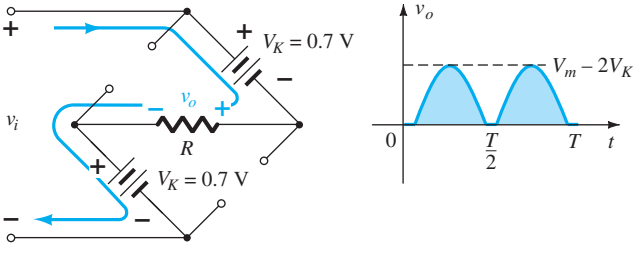


FIG. 2.58
Determining $V_{o_{max}}$ for silicon diodes in the bridge configuration.

The peak value of the output voltage v_o is therefore

$$V_{o_{max}} = V_m - 2V_K$$

For situations where $V_m \gg 2V_K$, the following equation can be applied for the average value with a relatively high level of accuracy:

$$\boxed{V_{dc} \cong 0.636(V_m - 2V_K)} \tag{2.11}$$

Then again, if V_m is sufficiently greater than $2V_K$, then Eq. (2.10) is often applied as a first approximation for V_{dc}.

PIV The required PIV of each diode (ideal) can be determined from Fig. 2.59 obtained at the peak of the positive region of the input signal. For the indicated loop the maximum voltage across R is V_m and the PIV rating is defined by

$$\text{PIV} \geqq V_m \quad \text{full-wave bridge rectifier} \tag{2.12}$$

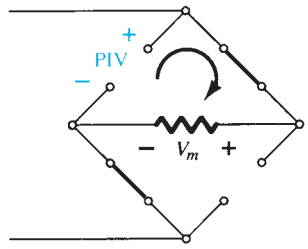


FIG. 2.59
Determining the required PIV for the bridge configuration.

Center-Tapped Transformer

A second popular full-wave rectifier appears in Fig. 2.60 with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer. During the positive portion of v_i applied to the primary of the transformer, the network will appear as shown in Fig. 2.61 with a positive pulse across each section of the secondary coil. D_1 assumes the short-circuit equivalent and D_2 the open-circuit equivalent, as determined by the secondary voltages and the resulting current directions. The output voltage appears as shown in Fig. 2.61.

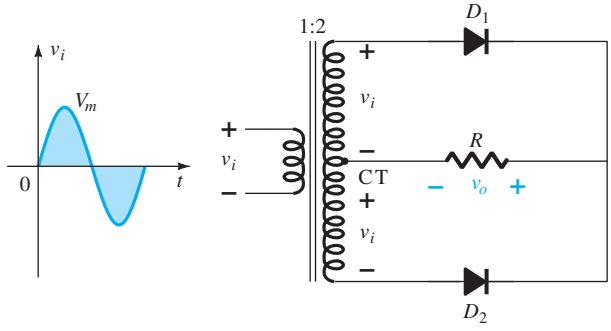


FIG. 2.60
Center-tapped transformer full-wave rectifier.

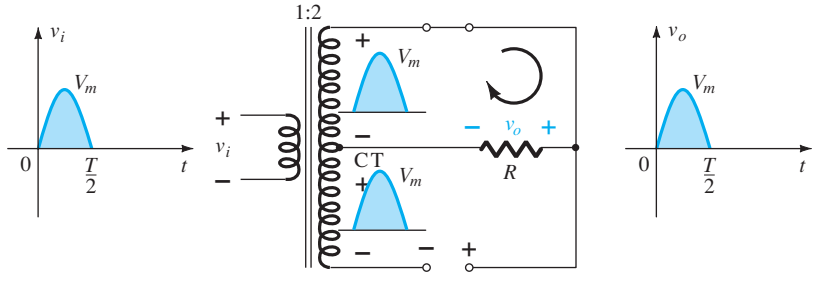


FIG. 2.61
Network conditions for the positive region of v_i.

During the negative portion of the input the network appears as shown in Fig. 2.62, reversing the roles of the diodes but maintaining the same polarity for the voltage across the load resistor R. The net effect is the same output as that appearing in Fig. 2.57 with the same dc levels.

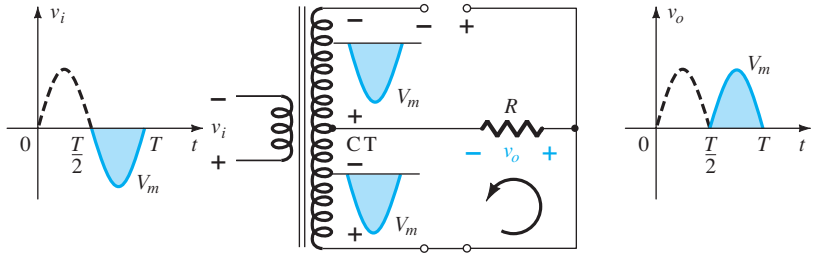


FIG. 2.62
Network conditions for the negative region of v_i.

PIV The network of Fig. 2.63 will help us determine the net PIV for each diode for this full-wave rectifier. Inserting the maximum voltage for the secondary voltage and V_m as established by the adjoining loop results in

$$\text{PIV} = V_{\text{secondary}} + V_R$$
$$= V_m + V_m$$

and

$$\boxed{\text{PIV} \geqq 2V_m} \quad \text{CT transformer, full-wave rectifier} \tag{2.13}$$

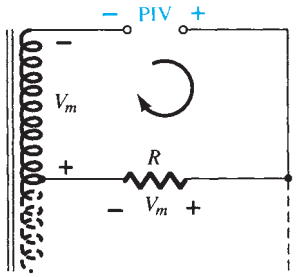


FIG. 2.63
Determining the PIV level for the diodes of the CT transformer full-wave rectifier.

EXAMPLE 2.17 Determine the output waveform for the network of Fig. 2.64 and calculate the output dc level and the required PIV of each diode.

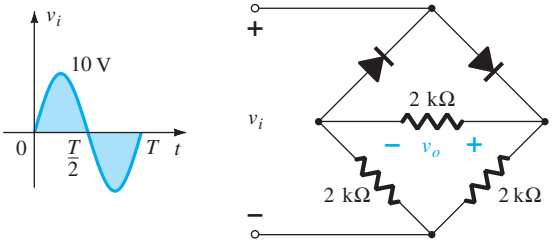


FIG. 2.64
Bridge network for Example 2.17.

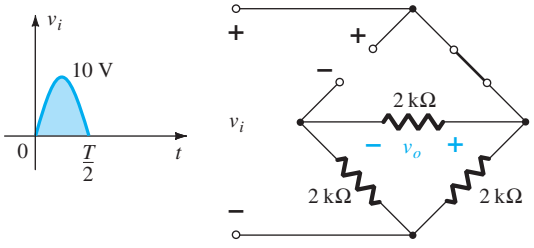


FIG. 2.65
Network of Fig. 2.64 for the positive region of v_i.

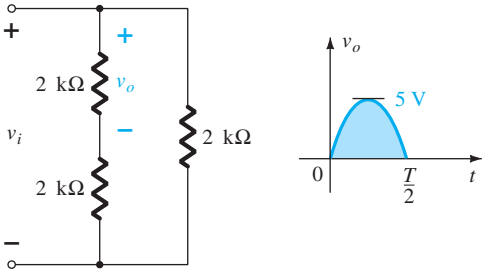


FIG. 2.66
Redrawn network of Fig. 2.65.

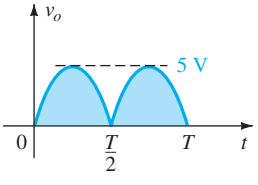


FIG. 2.67
Resulting output for Example 2.17.

Solution: The network appears as shown in Fig. 2.65 for the positive region of the input voltage. Redrawing the network results in the configuration of Fig. 2.66, where $v_o = \frac{1}{2}v_i$ or $V_{o_{\max}} = \frac{1}{2}V_{i_{\max}} = \frac{1}{2}(10\text{ V}) = 5\text{ V}$, as shown in Fig. 2.66. For the negative part of the input, the roles of the diodes are interchanged and v_o appears as shown in Fig. 2.67.

The effect of removing two diodes from the bridge configuration is therefore to reduce the available dc level to the following:

$$V_{\text{dc}} = 0.636(5\text{ V}) = \mathbf{3.18\text{ V}}$$

or that available from a half-wave rectifier with the same input. However, the PIV as determined from Fig. 2.59 is equal to the maximum voltage across R, which is 5 V, or half of that required for a half-wave rectifier with the same input.

2.8 CLIPPERS

The previous section on rectification gives clear evidence that diodes can be used to change the appearance of an applied waveform. This section on clippers and the next on clampers will expand on the wave-shaping abilities of diodes.

Clippers are networks that employ diodes to "clip" away a portion of an input signal without distorting the remaining part of the applied waveform.

The half-wave rectifier of Section 2.6 is an example of the simplest form of diode clipper—one resistor and a diode. Depending on the orientation of the diode, the positive or negative region of the applied signal is "clipped" off.

There are two general categories of clippers: *series* and *parallel.* The series configuration is defined as one where the diode is in series with the load, whereas the parallel variety has the diode in a branch parallel to the load.

Series

The response of the series configuration of Fig. 2.68a to a variety of alternating waveforms is provided in Fig. 2.68b. Although first introduced as a half-wave rectifier (for sinusoidal waveforms), there are no boundaries on the type of signals that can be applied to a clipper.

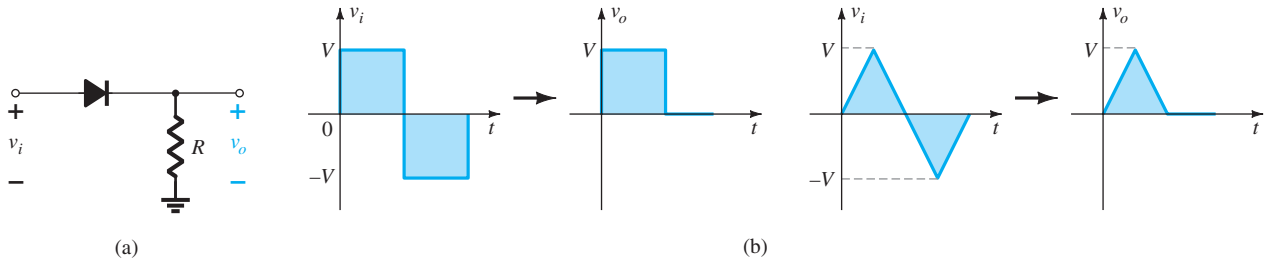


FIG. 2.68
Series clipper.

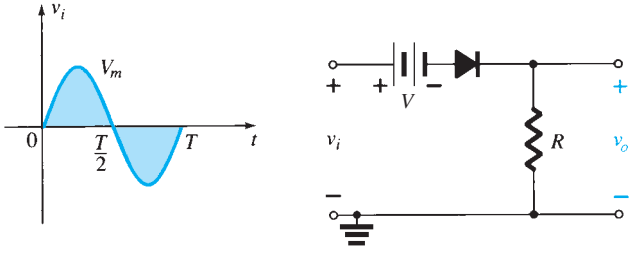


FIG. 2.69
Series clipper with a dc supply.

The addition of a dc supply to the network as shown in Fig. 2.69 can have a pronounced effect on the analysis of the series clipper configuration. The response is not as obvious because the dc supply can aid or work against the source voltage, and the dc supply can be in the leg between the supply and output or in the branch parallel to the output.

There is no general procedure for analyzing networks such as the type in Fig. 2.69, but there are some things one can do to give the analysis some direction.

First and most important:

1. **Take careful note of where the output voltage is defined.**

In Fig. 2.69 it is directly across the resistor *R*. In some cases it may be across a combination of series elements.

Next:

2. **Try to develop an overall sense of the response by simply noting the "pressure" established by each supply and the effect it will have on the conventional current direction through the diode.**

In Fig. 2.69, for instance, any positive voltage of the supply will try to turn the diode on by establishing a conventional current through the diode that matches the arrow in the diode symbol. However, the added dc supply *V* will oppose that applied voltage and try to keep the diode in the "off" state. The result is that any supply voltage greater than *V* volts will turn the diode on and conduction can be established through the load resistor. Keep in mind that we are dealing with an ideal diode for the moment, so the turn-on voltage is simply 0 V. In general, therefore, for the network of Fig. 2.69 we can conclude that the

diode will be on for any voltage v_i that is greater than V volts and off for any lesser voltage. For the "off" condition, the output would be 0 V due to the lack of current, and for the "on" condition it would simply be $v_o = v_i - V$ as determined by Kirchhoff's voltage law.

3. Determine the applied voltage (transition voltage) that will result in a change of state for the diode from the "off" to the "on" state.

This step will help to define a region of the applied voltage when the diode is on and when it is off. On the characteristics of an ideal diode this will occur when $V_D = 0$ V and $I_D = 0$ mA. For the approximate equivalent this is determined by finding the applied voltage when the diode has a drop of 0.7 V across it (for silicon) and $I_D = 0$ mA.

This exercise was applied to the network of Fig. 2.69 as shown in Fig. 2.70. Note the substitution of the short-circuit equivalent for the diode and the fact that the voltage across the resistor is 0 V because the diode current is 0 mA. The result is $v_i - V = 0$, and so

$$v_i = V \tag{2.14}$$

is the transition voltage.

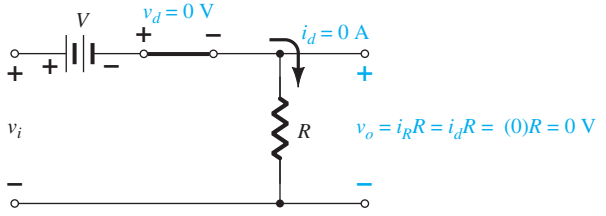


FIG. 2.70
Determining the transition level for the circuit of Fig. 2.69.

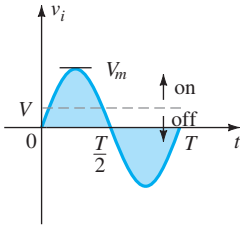


FIG. 2.71
Using the transition voltage to define the "on" and "off" regions.

This permits drawing a line on the sinusoidal supply voltage as shown in Fig. 2.71 to define the regions where the diode is on and off.

For the "on" region, as shown in Fig. 2.72, the diode is replaced by a short-circuit equivalent, and the output voltage is defined by

$$v_o = v_i - V \tag{2.15}$$

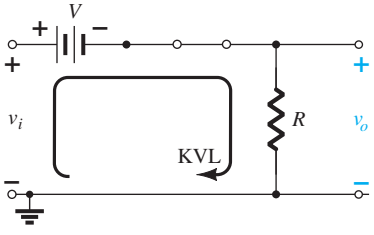


FIG. 2.72
Determining v_o for the diode in the "on" state.

For the "off" region, the diode is an open circuit, $I_D = 0$ mA, and the output voltage is

$$v_o = 0 \text{ V}$$

4. It is often helpful to draw the output waveform directly below the applied voltage using the same scales for the horizontal axis and the vertical axis.

Using this last piece of information, we can establish the 0-V level on the plot of Fig. 2.73 for the region indicated. For the "on" condition, Eq. (2.15) can be used to find the output voltage when the applied voltage has its peak value:

$$v_{o_{\text{peak}}} = V_m - V$$

and this can be added to the plot of Fig. 2.73. It is then simple to fill in the missing section of the output curve.

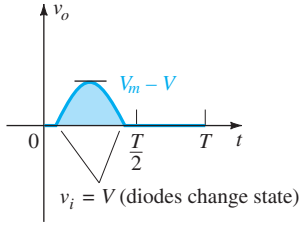


FIG. 2.73
Sketching the waveform of v_o using the results obtained for v_o above and below the transition level.

EXAMPLE 2.18 Determine the output waveform for the sinusoidal input of Fig. 2.74.

Solution:

Step 1: The output is again directly across the resistor *R*.

Step 2: The positive region of v_i and the dc supply are both applying "pressure" to turn the diode on. The result is that we can safely assume the diode is in the "on" state for the entire range of positive voltages for v_i. Once the supply goes negative, it would have to exceed the dc supply voltage of 5 V before it could turn the diode off.

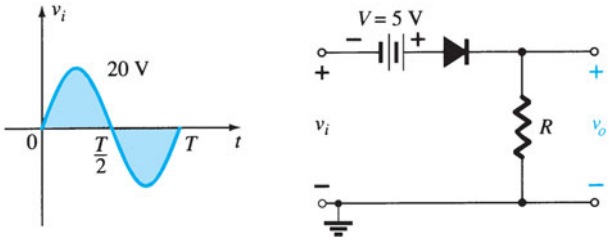


FIG. 2.74
Series clipper for Example 2.18.

Step 3: The transition model is substituted in Fig. 2.75, and we find that the transition from one state to the other will occur when

$$v_i + 5\text{ V} = 0\text{ V}$$

or

$$v_i = -5\text{ V}$$

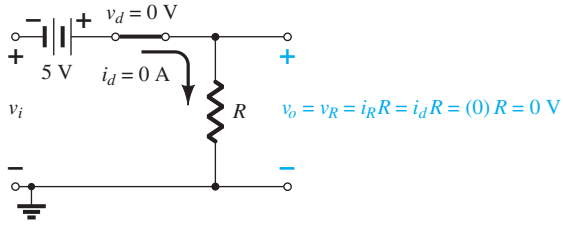


FIG. 2.75
Determining the transition level for the clipper of Fig. 2.74.

Step 4: In Fig. 2.76 a horizontal line is drawn through the applied voltage at the transition level. For voltages less than −5 V the diode is in the open-circuit state and the output is 0 V, as shown in the sketch of v_o. Using Fig. 2.76, we find that for conditions when the diode is on and the diode current is established the output voltage will be the following, as determined using Kirchhoff's voltage law:

$$v_o = v_i + 5\text{ V}$$

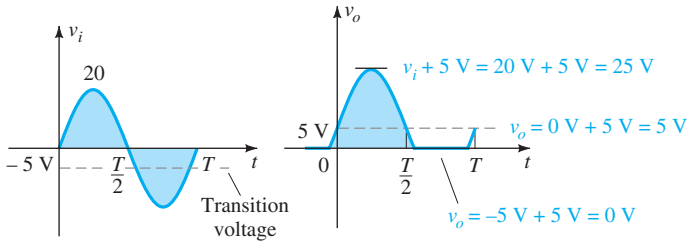


FIG. 2.76
Sketching v_o for Example 2.18.

The analysis of clipper networks with square-wave inputs is actually easier than with sinusoidal inputs because only two levels have to be considered. In other words, the network can be analyzed as if it had two dc level inputs with the resulting v_o plotted in the proper time frame. The next example demonstrates the procedure.

EXAMPLE 2.19 Find the output voltage for the network examined in Example 2.18 if the applied signal is the square wave of Fig. 2.77.

Solution: For $v_i = 20\text{ V}\ (0 \rightarrow T/2)$ the network of Fig. 2.78 results. The diode is in the short-circuit state, and $v_o = 20\text{ V} + 5\text{ V} = 25\text{ V}$. For $v_i = -10\text{ V}$ the network of Fig. 2.79

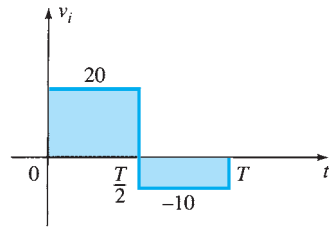


FIG. 2.77
Applied signal for Example 2.19.

results, placing the diode in the "off" state, and $v_o = i_R R = (0)R = 0$ V. The resulting output voltage appears in Fig. 2.80.

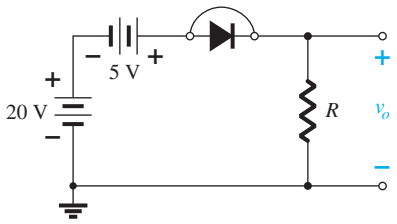


FIG. 2.78
v_o at $v_i = +20$ V.

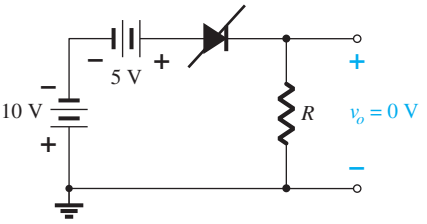


FIG. 2.79
v_o at $v_i = -10$ V.

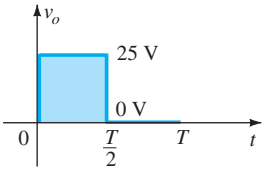


FIG. 2.80
Sketching v_o for Example 2.19.

Note in Example 2.19 that the clipper not only clipped off 5 V from the total swing, but also raised the dc level of the signal by 5 V.

Parallel

The network of Fig. 2.81 is the simplest of parallel diode configurations with the output for the same inputs of Fig. 2.68. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next example.

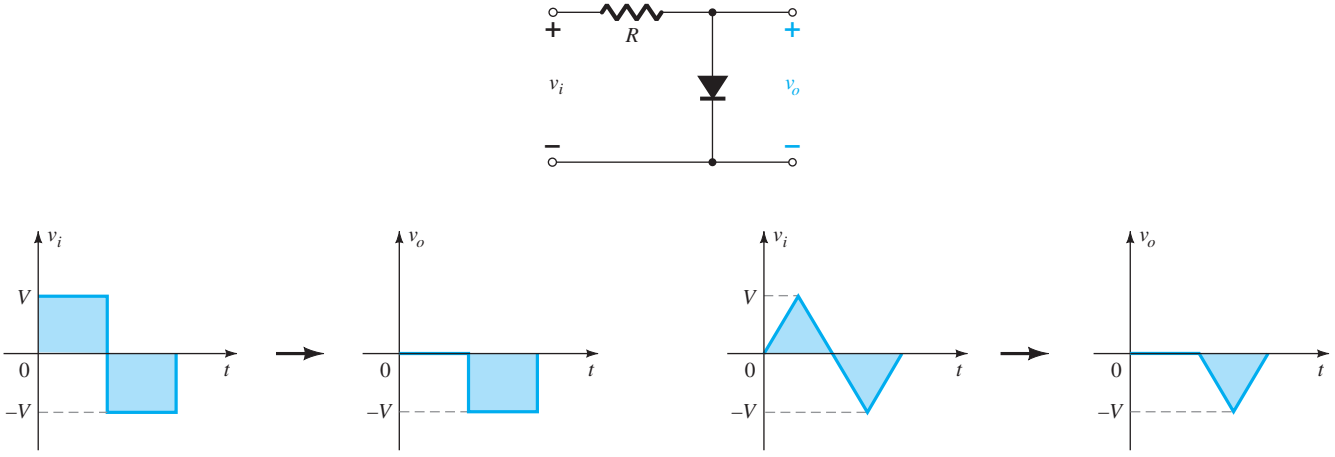


FIG. 2.81
Response to a parallel clipper.

EXAMPLE 2.20 Determine v_o for the network of Fig. 2.82.

Solution:

Step 1: In this example the output is defined across the series combination of the 4-V supply and the diode, not across the resistor *R*.

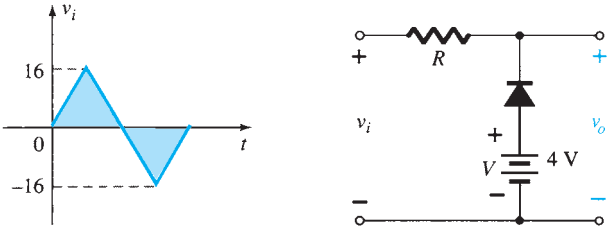


FIG. 2.82
Example 2.20.

Step 2: The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "on" state for a good portion of the negative region of the input signal. In fact, it is interesting to note that since the output is directly across the series combination, when the diode is in its short-circuit state the output voltage will be directly across the 4-V dc supply, requiring that the output be fixed at 4 V. In other words, when the diode is on the output will be 4 V. Other than that, when the diode is an open circuit, the current through the series network will be 0 mA and the voltage drop across the resistor will be 0 V. That will result in $v_o = v_i$ whenever the diode is off.

Step 3: The transition level of the input voltage can be found from Fig. 2.83 by substituting the short-circuit equivalent and remembering the diode current is 0 mA at the instant of transition. The result is a change in state when

$$v_i = 4 \text{ V}$$

Step 4: In Fig. 2.84 the transition level is drawn along with $v_o = 4$ V when the diode is on. For $v_i \geq 4$ V, $v_o = 4$ V, and the waveform is simply repeated on the output plot.

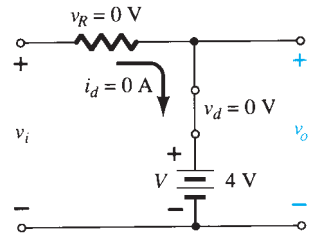


FIG. 2.83
Determining the transition level for Example 2.20.

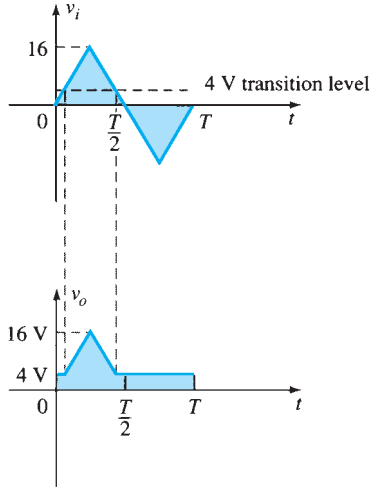


FIG. 2.84
Sketching v_o for Example 2.20.

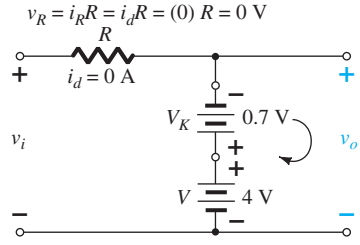


FIG. 2.85
Determining the transition level for the network of Fig. 2.82.

To examine the effects of the knee voltage V_K of a silicon diode on the output response, the next example will specify a silicon diode rather than the ideal diode equivalent.

EXAMPLE 2.21 Repeat Example 2.20 using a silicon diode with $V_K = 0.7$ V.

Solution: The transition voltage can first be determined by applying the condition $i_d = 0$ A at $v_d = V_D = 0.7$ V and obtaining the network of Fig. 2.85. Applying Kirchhoff's voltage law around the output loop in the clockwise direction, we find that

$$v_i + V_K - V = 0$$

and

$$v_i = V - V_K = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3\ V}$$

For input voltages greater than 3.3 V, the diode will be an open circuit and $v_o = v_i$. For input voltages less than 3.3 V, the diode will be in the "on" state and the network of Fig. 2.86 results, where

$$v_o = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3\ V}$$

The resulting output waveform appears in Fig. 2.87. Note that the only effect of V_K was to drop the transition level to 3.3 from 4 V.

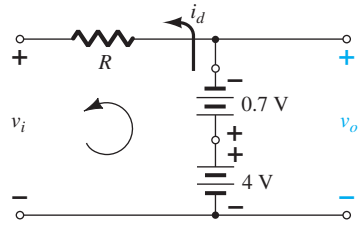


FIG. 2.86
Determining v_o for the diode of Fig. 2.82 in the "on" state.

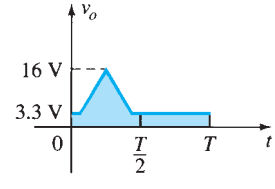
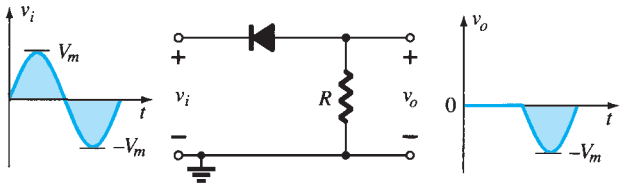


FIG. 2.87
Sketching v_o for Example 2.21.

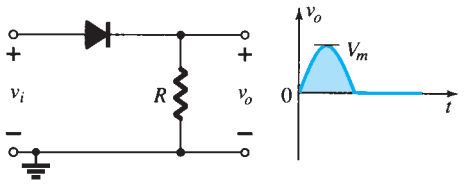
There is no question that including the effects of V_K will complicate the analysis somewhat, but once the analysis is understood with the ideal diode, the procedure, including the effects of V_K, will not be that difficult.

Simple Series Clippers (Ideal Diodes)

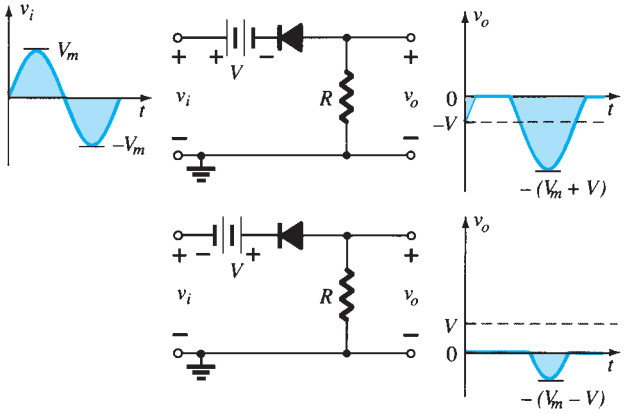
POSITIVE

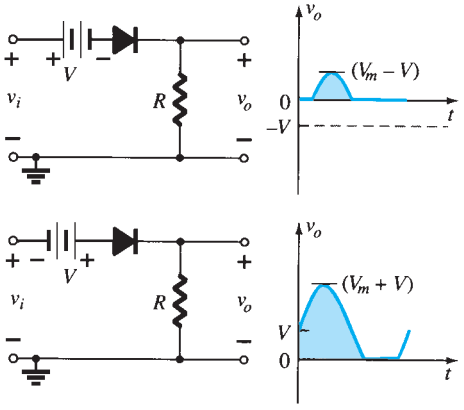


NEGATIVE

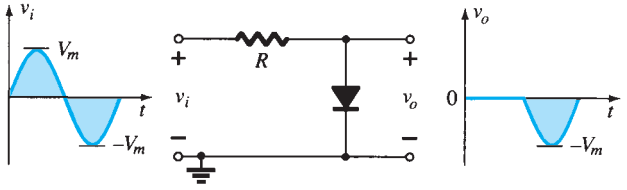


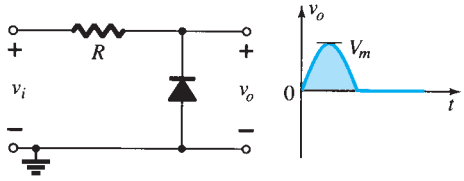
Biased Series Clippers (Ideal Diodes)



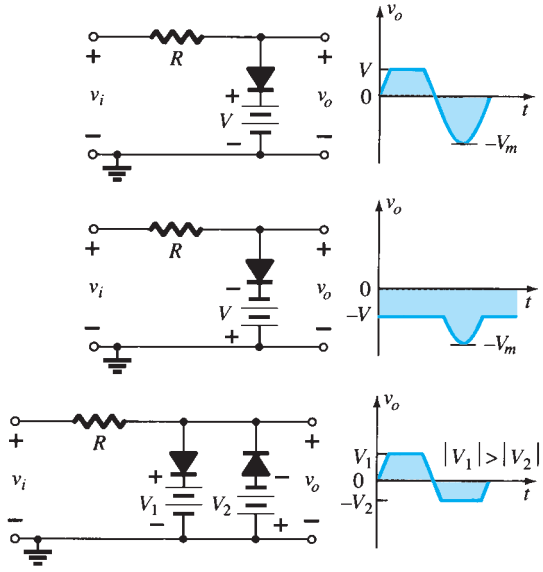


Simple Parallel Clippers (Ideal Diodes)





Biased Parallel Clippers (Ideal Diodes)



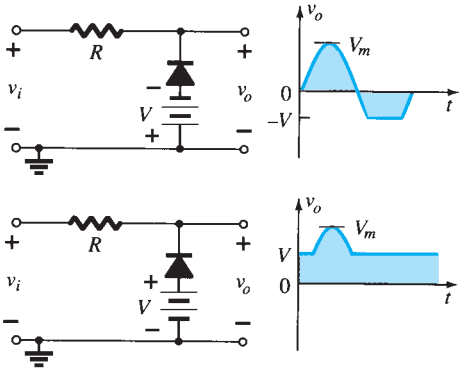


FIG. 2.88
Clipping circuits.

Summary

A variety of series and parallel clippers with the resulting output for the sinusoidal input are provided in Fig. 2.88. In particular, note the response of the last configuration, with its ability to clip off a positive and a negative section as determined by the magnitude of the dc supplies.

2.9 CLAMPERS

The previous section investigated a number of diode configurations that clipped off a portion of the applied signal without changing the remaining part of the waveform. This section will examine a variety of diode configurations that shift the applied signal to a different level.

A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.

Additional shifts can also be obtained by introducing a dc supply to the basic structure. The chosen resistor and capacitor of the network must be chosen such that the time constant determined by $\tau = RC$ is sufficiently large to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting. Throughout the analysis we assume that for all practical purposes the capacitor fully charges or discharges in five time constants.

The simplest of clamper networks is provided in Fig. 2.89. It is important to note that the capacitor is connected directly between input and output signals and the resistor and the diode are connected in parallel with the output signal.

Clamping networks have a capacitor connected directly from input to output with a resistive element in parallel with the output signal. The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.

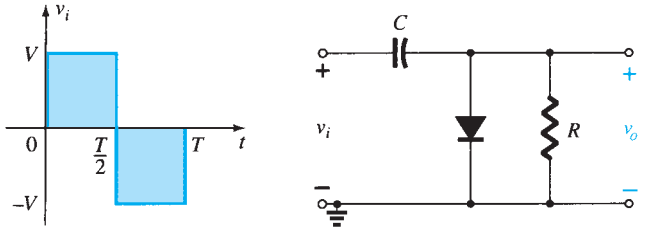


FIG. 2.89
Clamper.

There is a sequence of steps that can be applied to help make the analysis straightforward. It is not the only approach to examining clampers, but it does offer an option if difficulties surface.

Step 1: Start the analysis by examining the response of the portion of the input signal that will forward bias the diode.

Step 2: During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the surrounding network.

For the network of Fig. 2.89 the diode will be forward biased for the positive portion of the applied signal. For the interval 0 to $T/2$ the network will appear as shown in Fig. 2.90. The short-circuit equivalent for the diode will result in $v_o = 0$ V for this time interval, as shown in the sketch of v_o in Fig. 2.92. During this same interval of time, the time constant determined by $\tau = RC$ is very small because the resistor R has been effectively "shorted out" by the conducting diode and the only resistance present is the inherent (contact, wire) resistance of the network. The result is that the capacitor will quickly charge to the peak value of V volts as shown in Fig. 2.90 with the polarity indicated.

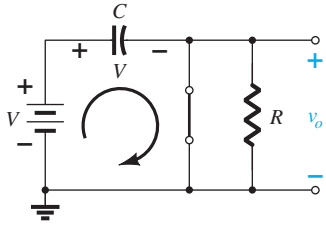


FIG. 2.90
Diode "on" and the capacitor charging to V volts.

Step 3: Assume that during the period when the diode is in the "off" state the capacitor holds on to its established voltage level.

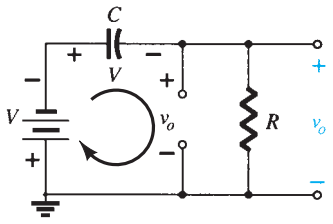


FIG. 2.91
Determining v_o with the diode "off."

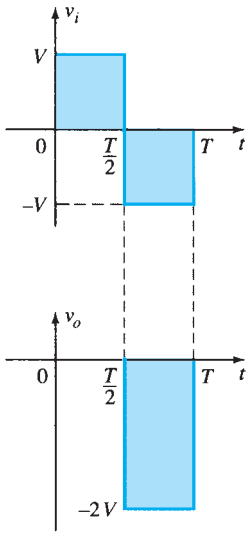


FIG. 2.92
Sketching v_o for the network of Fig. 2.91.

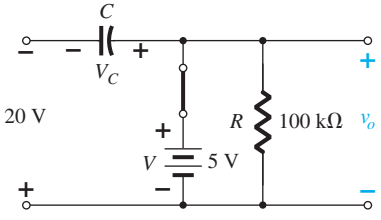


FIG. 2.94
Determining v_o and V_C with the diode in the "on" state.

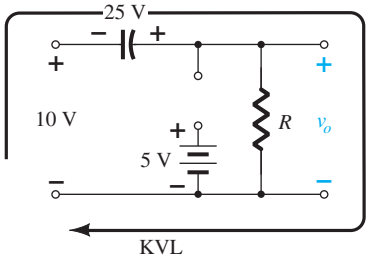


FIG. 2.95
Determining v_o with the diode in the "off" state.

Step 4: Throughout the analysis, maintain a continual awareness of the location and defined polarity for v_o to ensure that the proper levels are obtained.

When the input switches to the $-V$ state, the network will appear as shown in Fig. 2.91, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both "pressuring" current through the diode from cathode to anode. Now that R is back in the network the time constant determined by the RC product is sufficiently large to establish a discharge period 5τ, much greater than the period $T/2 \rightarrow T$, and it can be assumed on an approximate basis that the capacitor holds onto all its charge and, therefore, voltage (since $V = Q/C$) during this period.

Since v_o is in parallel with the diode and resistor, it can also be drawn in the alternative position shown in Fig. 2.91. Applying Kirchhoff's voltage law around the input loop results in

$$-V - V - v_o = 0$$

and

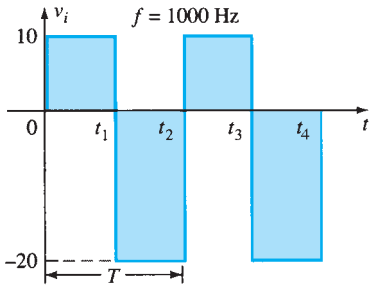
$$v_o = -2V$$

The negative sign results from the fact that the polarity of $2V$ is opposite to the polarity defined for v_o. The resulting output waveform appears in Fig. 2.92 with the input signal. The output signal is clamped to 0 V for the interval 0 to $T/2$ but maintains the same total swing ($2V$) as the input.

Step 5: Check that the total swing of the output matches that of the input.

This is a property that applies for all clamping networks, giving an excellent check on the results obtained.

EXAMPLE 2.22 Determine v_o for the network of Fig. 2.93 for the input indicated.



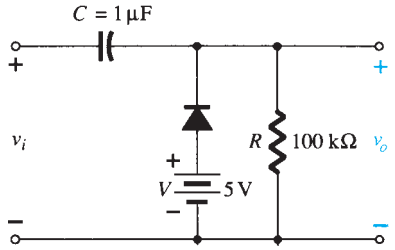


FIG. 2.93
Applied signal and network for Example 2.22.

Solution: Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an interval of 0.5 ms between levels. The analysis will begin with the period $t_1 \rightarrow t_2$ of the input signal since the diode is in its short-circuit state. For this interval the network will appear as shown in Fig. 2.94. The output is across R, but it is also directly across the 5-V battery if one follows the direct connection between the defined terminals for v_o and the battery terminals. The result is $v_o = 5$ V for this interval. Applying Kirchhoff's voltage law around the input loop results in

$$-20\text{ V} + V_C - 5\text{ V} = 0$$

and

$$V_C = 25\text{ V}$$

The capacitor will therefore charge up to 25 V. In this case the resistor R is not shorted out by the diode, but a Thévenin equivalent circuit of that portion of the network that includes the battery and the resistor will result in $R_{Th} = 0\ \Omega$ with $E_{Th} = V = 5$ V. For the period $t_2 \rightarrow t_3$ the network will appear as shown in Fig. 2.95.

The open-circuit equivalent for the diode removes the 5-V battery from having any effect on v_o, and applying Kirchhoff's voltage law around the outside loop of the network results in

$$+10\text{ V} + 25\text{ V} - v_o = 0$$

and

$$v_o = 35\text{ V}$$

The time constant of the discharging network of Fig. 2.95 is determined by the product RC and has the magnitude

$$\tau = RC = (100\,\text{k}\Omega)(0.1\,\mu\text{F}) = 0.01\text{ s} = 10\text{ ms}$$

The total discharge time is therefore $5\tau = 5(10\text{ ms}) = 50\text{ ms}$.

Since the interval $t_2 \rightarrow t_3$ will only last for 0.5 ms, it is certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signal. The resulting output appears in Fig. 2.96 with the input signal. Note that the output swing of 30 V matches the input swing as noted in step 5.

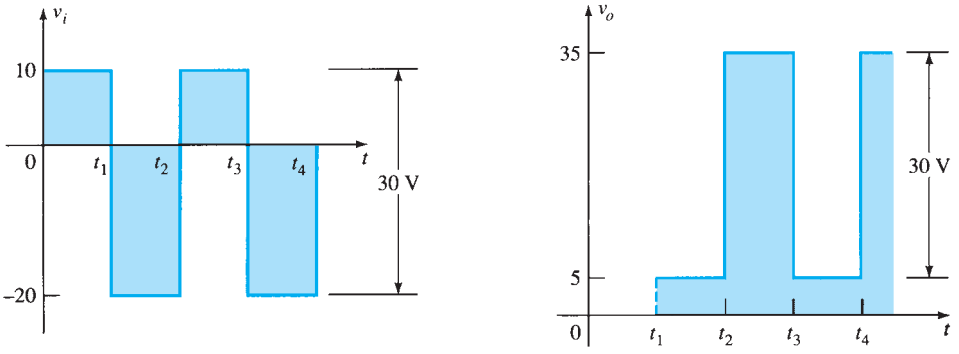


FIG. 2.96
v_i and v_o for the clamper of Fig. 2.93.

EXAMPLE 2.23 Repeat Example 2.22 using a silicon diode with $V_K = 0.7$ V.

Solution: For the short-circuit state the network now takes on the appearance of Fig. 2.97, and v_o can be determined by Kirchhoff's voltage law in the output section:

$$+5\text{ V} - 0.7\text{ V} - v_o = 0$$

and

$$v_o = 5\text{ V} - 0.7\text{ V} = 4.3\text{ V}$$

For the input section Kirchhoff's voltage law results in

$$-20\text{ V} + V_C + 0.7\text{ V} - 5\text{ V} = 0$$

and

$$V_C = 25\text{ V} - 0.7\text{ V} = 24.3\text{ V}$$

For the period $t_2 \rightarrow t_3$ the network will now appear as in Fig. 2.98, with the only change being the voltage across the capacitor. Applying Kirchhoff's voltage law yields

$$+10\text{ V} + 24.3\text{ V} - v_o = 0$$

and

$$v_o = 34.3\text{ V}$$

The resulting output appears in Fig. 2.99, verifying the statement that the input and output swings are the same.

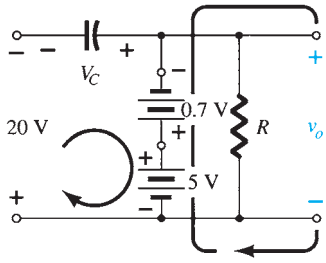


FIG. 2.97
Determining v_o and V_C with the diode in the "on" state.

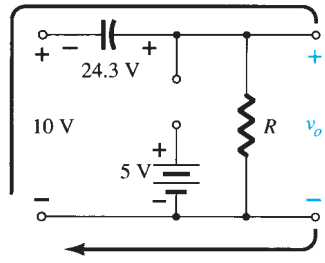


FIG. 2.98
Determining v_o with the diode in the open state.

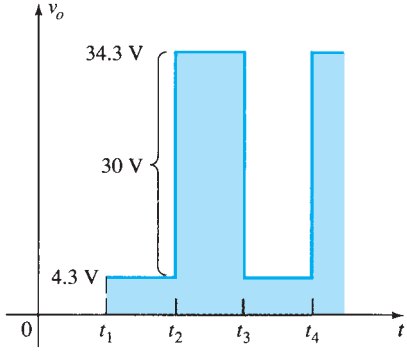


FIG. 2.99
Sketching v_o for the clamper of Fig. 2.93 with a silicon diode.

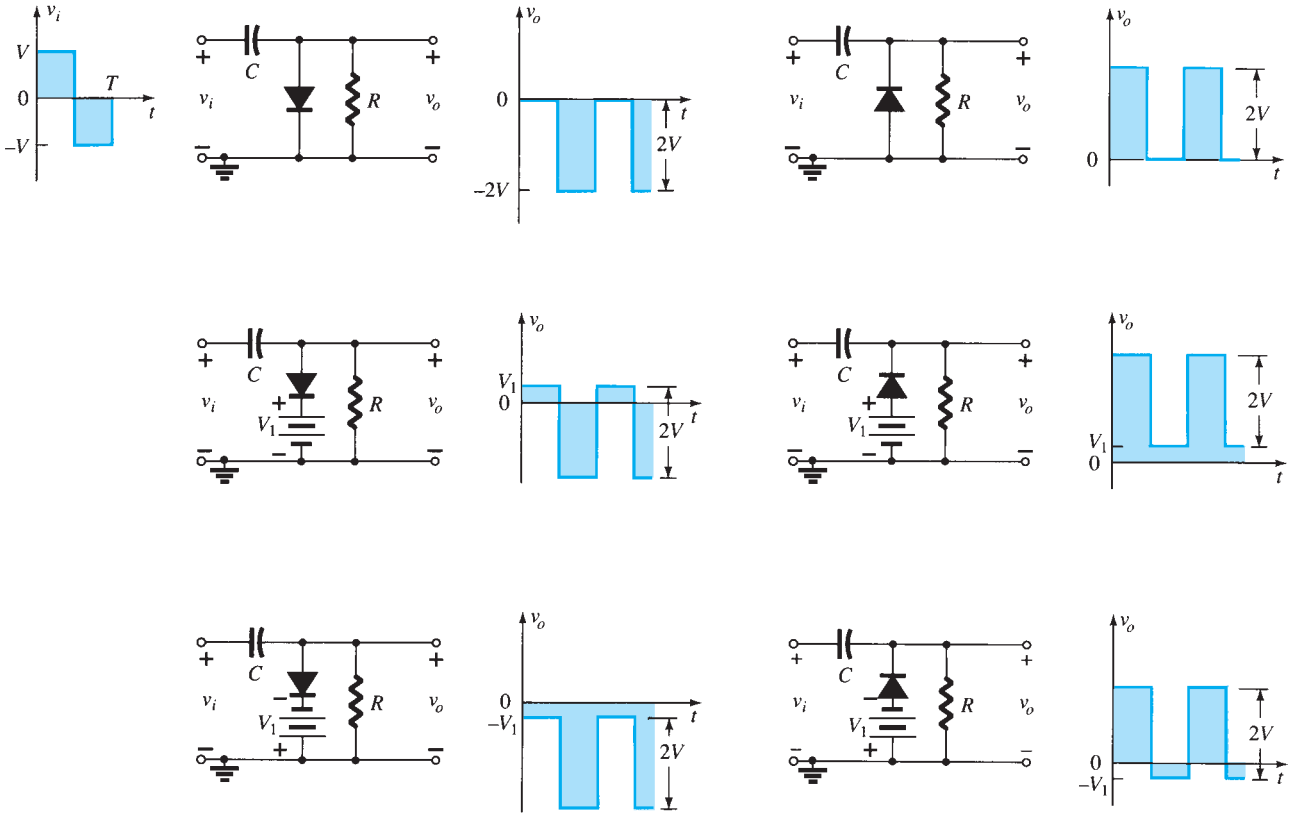


FIG. 2.100
Clamping circuits with ideal diodes ($5\tau = 5RC \gg T/2$).

A number of clamping circuits and their effect on the input signal are shown in Fig. 2.100. Although all the waveforms appearing in Fig. 2.100 are square waves, clamping networks work equally well for sinusoidal signals. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response as shown in Fig. 2.101 for a network appearing in the bottom right of Fig. 2.100.

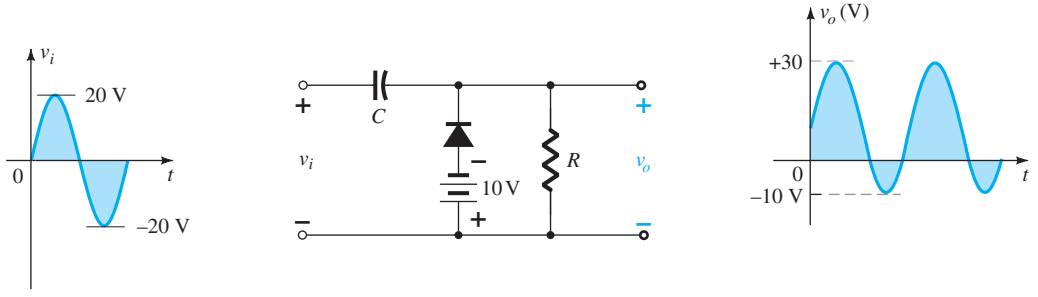


FIG. 2.101
Clamping network with a sinusoidal input.

2.10 NETWORKS WITH A DC AND AC SOURCE

The analysis thus far has been limited to circuits with a single dc, ac, or square wave input. This section will expand that analysis to include both an ac and a dc source in the same configuration. In Fig. 2.102 the simplest of two-source networks has been constructed.

For such a system it is especially important that the Superposition Theorem can be applied. That is,

The response of any network with both an ac and a dc source can be found by finding the response to each source independently and then combining the results.

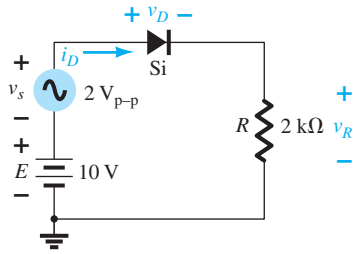


FIG. 2.102
Network with a dc and ac supply.

DC Source

The network is redrawn as shown in Fig. 2.103 for the dc source. Note that the ac source was removed by simply replacing it with a short-circuit equivalent to the condition $v_s = 0$ V.

Using the approximate equivalent circuit for the diode, the output voltage is

$$V_R = E - V_D = 10\text{ V} - 0.7\text{ V} = 9.3\text{ V}$$

and the currents are

$$I_D = I_R = \frac{9.3\text{ V}}{2\text{ k}\Omega} = 4.65\text{ mA}$$

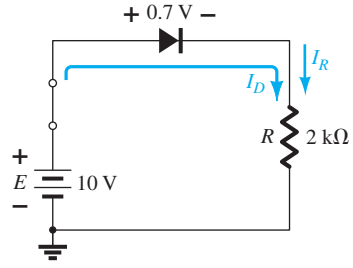


FIG. 2.103
Applying superposition to determine effects of the dc source.

AC Source

The dc source is also replaced by a short-circuit equivalent, as shown in Fig. 2.104. The diode will be replaced by the ac resistance, as determined by Eq. 1.5 in Chapter 1—the current in the equation being the quiescent or dc value. For this case,

$$r_d = \frac{26\text{ mV}}{I_D} = \frac{26\text{ mV}}{4.65\text{ mA}} = 5.59\ \Omega$$

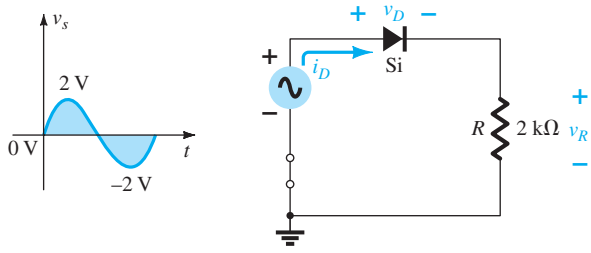


FIG. 2.104
Determing the response of v_R to the applied ac source.

Replacing the diode by this resistance will result in the circuit of Fig. 2.105. For the peak value of the applied voltage, the peak values of v_R and v_D will be

$$v_{R_{peak}} = \frac{2\text{ k}\Omega\ (2\text{ V})}{2\text{ k}\Omega + 5.59\ \Omega} \cong 1.99\text{ V}$$

and

$$v_{D_{peak}} = v_{s_{peak}} - v_{R_{peak}} = 2\text{ V} - 1.99\text{ V} = 0.01\text{ V} = 10\text{ mV}$$

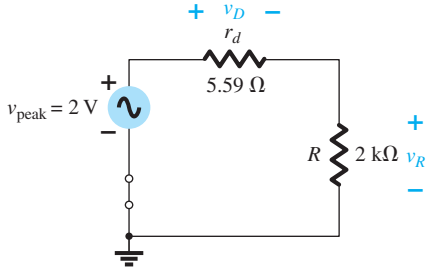


FIG. 2.105
Replacing the diode of Fig. 2.104 by its equivalent ac resistance.

Combining the results of the dc and ac analysis will result in the waveforms of Fig. 2.106 for v_R and v_D.

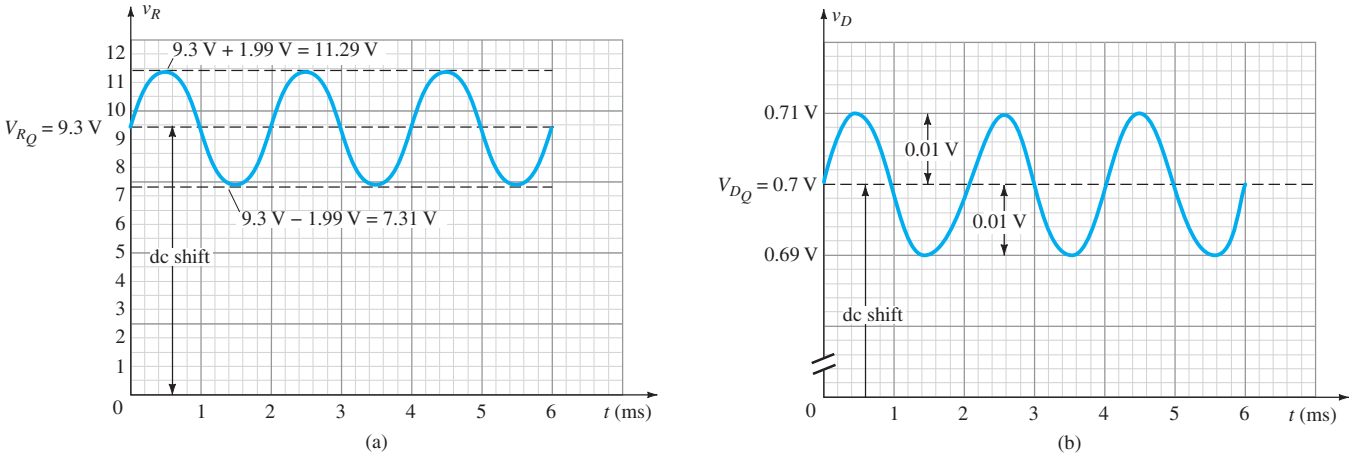


FIG. 2.106

(a) v_R and (b) v_D for the network of Fig. 2.102.

Note that the diode has an important impact on the resulting output voltage v_R but very little impact on the ac swing.

For comparison purposes the same system will now be analyzed using the actual characteristics and a load-line analysis. In Fig. 2.107 the dc load line has been drawn as described in Section 2.2. The resulting dc current is now slightly less due to a voltage drop across the diode that is slightly more than the approximate value of 0.7 V. For the peak value of the input voltage the load line will have intersections of $E = 12$ V and $I = \frac{E}{R} = \frac{12\text{ V}}{2\text{ k}\Omega} = 6$ mA. For the negative peak the intersections are at 8 V and 4 mA. Take particular note of the region of the diode characteristics traversed by the ac swing. It defines the region for which the diode resistance was determined in the analysis above. In this case, however, the quiescent value of dc current is ≅4.6 mA so the new ac resistance is

$$r_d = \frac{26\text{ mV}}{4.6\text{ mA}} = 5.65\ \Omega$$

which is very close to the above value.

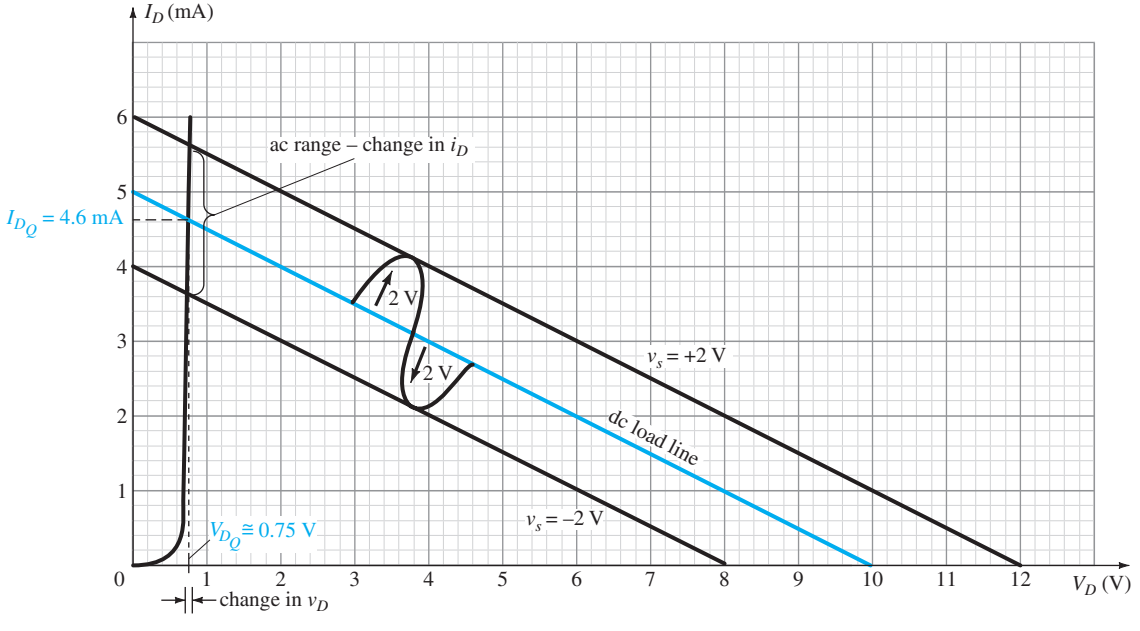


FIG. 2.107

Shifting load line due to v_s source.

In any event, it is now clear that the change in diode voltage for this region is very small, resulting in minimum impact on the output voltage. In general, the diode had a strong impact on the dc level of the output voltage but very little impact on the ac swing of the output. The diode was clearly close to ideal for the ac voltage and 0.7 V off for the dc level. This is all due primarily to the almost vertical rise of the diode once conduction is fully established through the diode. In most cases, diodes in the "on" state that are in series with loads will have some effect on the dc level but very little effect on the ac swing if the diode is fully conducting for the full cycle.

For the future, when dealing with diodes and an ac signal the dc level through the diode is first determined and the ac resistance level determined by Eq. 1.3. This ac resistance can then be substituted in place of the diode for the required analysis.

2.11 ZENER DIODES

The analysis of networks employing Zener diodes is quite similar to the analysis of semiconductor diodes in previous sections. First the state of the diode must be determined, followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network. Figure 2.108 reviews the approximate equivalent circuits for each region of a Zener diode assuming the straight-line approximations at each break point. Note that the forward-bias region is included because occasionally an application will skip into this region also.

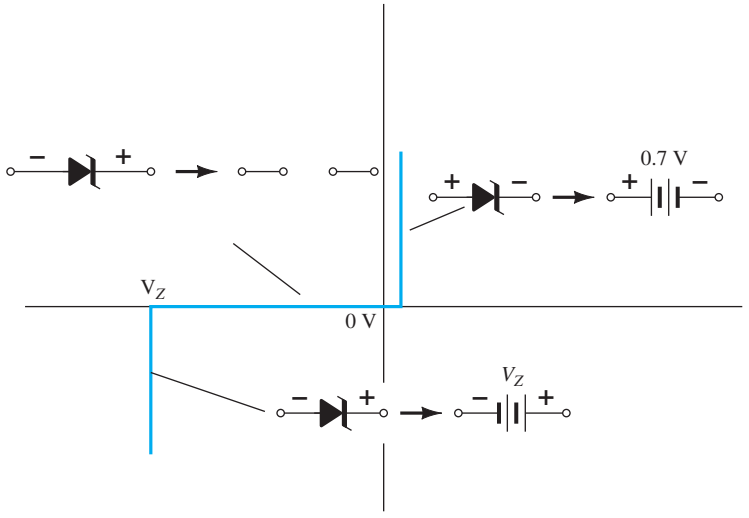


FIG. 2.108
Approximate equivalent circuits for the Zener diode in the three possible regions of application.

The first two examples will demonstrate how a Zener diode can be used to establish reference voltage levels and act as a protection device. The use of a Zener diode as a *regulator* will then be described in detail because it is one of its major areas of application. A regulator is a combination of elements designed to ensure that the output voltage of a supply remains fairly constant.

EXAMPLE 2.24 Determine the reference voltages provided by the network of Fig. 2.109, which uses a white LED to indicate that the power is on. What is the level of current through the LED and the power delivered by the supply? How does the power absorbed by the LED compare to that of the 6-V Zener diode?

Solution: First we have to check that there is sufficient applied voltage to turn on all the series diode elements. The white LED will have a drop of about 4 V across it, the 6-V and 3.3-V Zener diodes have a total of 9.3 V, and the forward-biased silicon diode has 0.7 V, for a total of 14 V. The applied 40 V is then sufficient to turn on all the elements and, one hopes, establish a proper operating current.

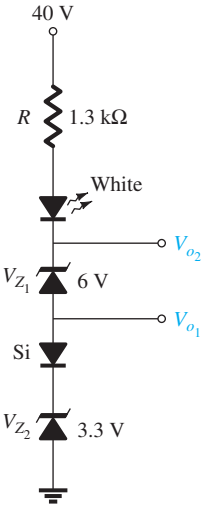


FIG. 2.109
Reference setting circuit for Example 2.24.

Note that the silicon diode was used to create a reference voltage of 4 V because

$$V_{o_1} = V_{Z_2} + V_K = 3.3\text{ V} + 0.7\text{ V} = \mathbf{4.0\text{ V}}$$

Combining the voltage of the 6-V Zener diode with the 4 V results in

$$V_{o_2} = V_{o_1} + V_{Z_1} = 4\text{ V} + 6\text{ V} = \mathbf{10\text{ V}}$$

Finally, the 4 V across the white LED will leave a voltage of 40 V – 14 V = 26 V across the resistor, and

$$I_R = I_{\text{LED}} = \frac{V_R}{R} = \frac{40\text{ V} - V_{o_2} - V_{\text{LED}}}{1.3\text{ k}\Omega} = \frac{40\text{ V} - 10\text{ V} - 4\text{ V}}{1.3\text{ k}\Omega} = \frac{26\text{ V}}{1.3\text{ k}\Omega} = \mathbf{20\text{ mA}}$$

which should establish the proper brightness for the LED.

The power delivered by the supply is simply the product of the supply voltage and current drain as follows:

$$P_s = EI_s = EI_R = (40\text{ V})(20\text{ mA}) = \mathbf{800\text{ mW}}$$

The power absorbed by the LED is

$$P_{\text{LED}} = V_{\text{LED}}I_{\text{LED}} = (4\text{ V})(20\text{ mA}) = \mathbf{80\text{ mW}}$$

and the power absorbed by the 6-V Zener diode is

$$P_Z = V_Z I_Z = (6\text{ V})(20\text{ mA}) = \mathbf{120\text{ mW}}$$

The power absorbed by the Zener diode exceeds that of the LED by 40 mW.

EXAMPLE 2.25 The network of Fig. 2.110 is designed to limit the voltage to 20 V during the positive portion of the applied voltage and to 0 V for a negative excursion of the applied voltage. Check its operation and plot the waveform of the voltage across the system for the applied signal. Assume the system has a very high input resistance so it will not affect the behavior of the network.

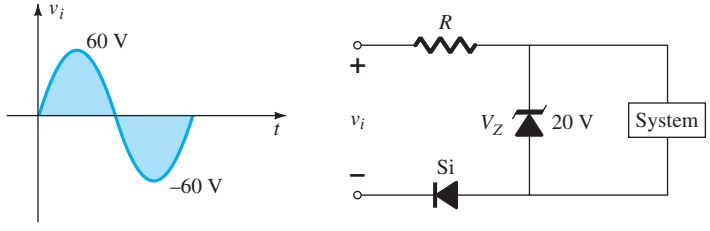


FIG. 2.110
Controlling network for Example 2.25.

Solution: For positive applied voltages less than the Zener potential of 20 V the Zener diode will be in its approximate open-circuit state, and the input signal will simply distribute itself across the elements, with the majority going to the system because it has such a high resistance level.

Once the voltage across the Zener diode reaches 20 V the Zener diode will turn on as shown in Fig. 2.111a and the voltage across the system will lock in at 20 V. Further increases in the applied voltage will simply appear across the series resistor with the voltage across the system and the forward-biased diode remaining fixed at 20 V and 0.7 V, respectively. The voltage across the system is fixed at 20 V, as shown in Fig. 2.111a, because the 0.7 V of the diode is not between the defined output terminals. The system is therefore safe from any further increases in applied voltage.

For the negative region of the applied signal the silicon diode is reverse biased and presents an open circuit to the series combination of elements. The result is that the full negatively applied signal will appear across the open-circuited diode and the negative voltage across the system locked in at 0 V, as shown in Fig. 2.111b.

The voltage across the system will therefore appear as shown in Fig. 2.111c.

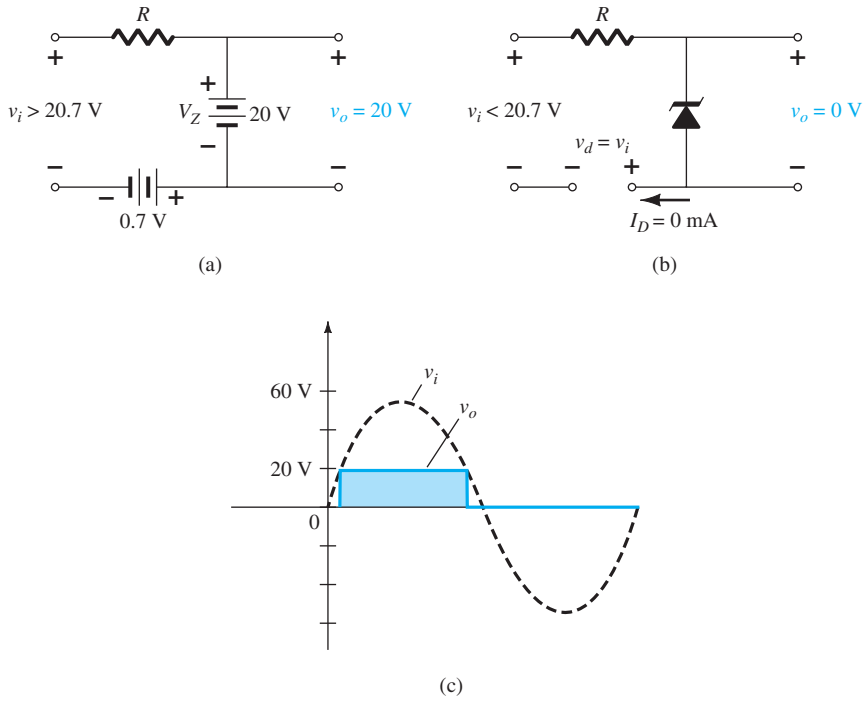


FIG. 2.111
Response of the network of Fig. 2.110 to the application of a 60-V sinusoidal signal.

The use of the Zener diode as a regulator is so common that three conditions surrounding the analysis of the basic Zener regulator are considered. The analysis provides an excellent opportunity to become better acquainted with the response of the Zener diode to different operating conditions. The basic configuration appears in Fig. 2.112. The analysis is first for fixed quantities, followed by a fixed supply voltage and a variable load, and finally a fixed load and a variable supply.

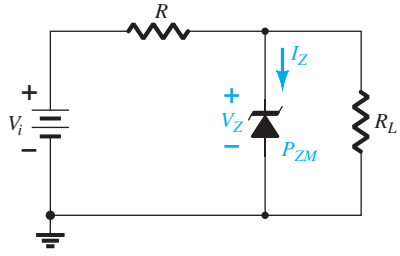


FIG. 2.112
Basic Zener regulator.

V_i and R Fixed

The simplest of Zener diode regulator networks appears in Fig. 2.112. The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.

1. ***Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.***

Applying step 1 to the network of Fig. 2.112 results in the network of Fig. 2.113, where an application of the voltage divider rule results in

$$V = V_L = \frac{R_L V_i}{R + R_L} \tag{2.16}$$

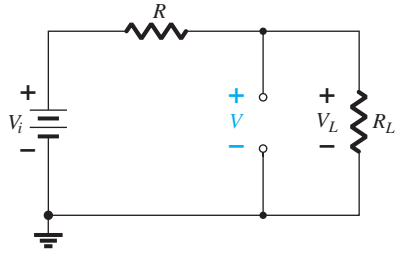


FIG. 2.113
Determining the state of the Zener diode.

If $V \geq V_Z$, the Zener diode is on, and the appropriate equivalent model can be substituted. If $V < V_Z$, the diode is off, and the open-circuit equivalence is substituted.

2. ***Substitute the appropriate equivalent circuit and solve for the desired unknowns.***

For the network of Fig. 2.112, the "on" state will result in the equivalent network of Fig. 2.114. Since voltages across parallel elements must be the same, we find that

$$V_L = V_Z \tag{2.17}$$

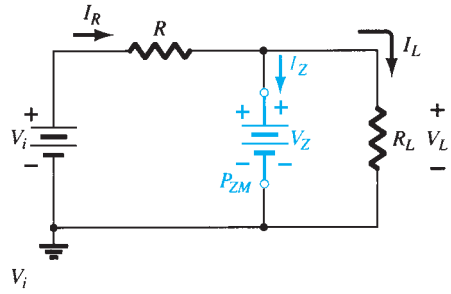


FIG. 2.114
Substituting the Zener equivalent for the "on" situation.

The Zener diode current must be determined by an application of Kirchhoff's current law. That is,

$$I_R = I_Z + I_L$$

and

$$\boxed{I_Z = I_R - I_L} \tag{2.18}$$

where

$$I_L = \frac{V_L}{R_L} \quad \text{and} \quad I_R = \frac{V_R}{R} = \frac{V_i - V_L}{R}$$

The power dissipated by the Zener diode is determined by

$$\boxed{P_Z = V_Z I_Z} \tag{2.19}$$

that must be less than the P_{ZM} specified for the device.

Before continuing, it is particularly important to realize that the first step was employed only to determine the *state of the Zener diode.* If the Zener diode is in the "on" state, the voltage across the diode is not V volts. When the system is turned on, the Zener diode will turn on as soon as the voltage across the Zener diode is V_Z volts. It will then "lock in" at this level and never reach the higher level of V volts.

EXAMPLE 2.26

a. For the Zener diode network of Fig. 2.115, determine V_L, V_R, I_Z, and P_Z.
b. Repeat part (a) with $R_L = 3\ \text{k}\Omega$.

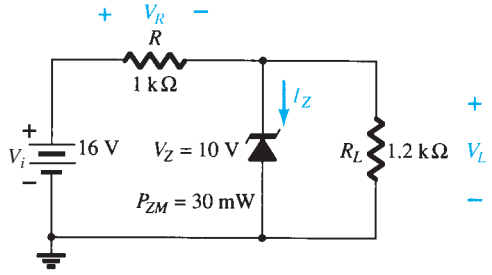


FIG. 2.115
Zener diode regulator for Example 2.26.

Solution:

a. Following the suggested procedure, we redraw the network as shown in Fig. 2.116.
Applying Eq. (2.16) gives

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 1.2\ \text{k}\Omega} = 8.73\ \text{V}$$

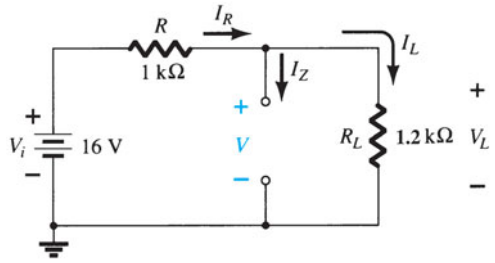


FIG. 2.116
Determining V for the regulator of Fig. 2.115.

Since $V = 8.73$ V is less than $V_Z = 10$ V, the diode is in the "off" state, as shown on the characteristics of Fig. 2.117. Substituting the open-circuit equivalent results in the same network as in Fig. 2.116, where we find that

$$V_L = V = \mathbf{8.73\ V}$$
$$V_R = V_i - V_L = 16\ \text{V} - 8.73\ \text{V} = \mathbf{7.27\ V}$$
$$I_Z = \mathbf{0\ A}$$

and
$$P_Z = V_Z I_Z = V_Z(0\ \text{A}) = \mathbf{0\ W}$$

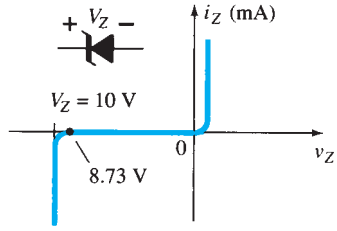


FIG. 2.117
Resulting operating point for the network of Fig. 2.115.

b. Applying Eq. (2.16) results in

$$V = \frac{R_L V_i}{R + R_L} = \frac{3\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 3\ \text{k}\Omega} = 12\ \text{V}$$

Since $V = 12$ V is greater than $V_Z = 10$ V, the diode is in the "on" state and the network of Fig. 2.118 results. Applying Eq. (2.17) yields

$$V_L = V_Z = \mathbf{10\ V}$$

and
$$V_R = V_i - V_L = 16\ \text{V} - 10\ \text{V} = \mathbf{6\ V}$$

with
$$I_L = \frac{V_L}{R_L} = \frac{10\ \text{V}}{3\ \text{k}\Omega} = 3.33\ \text{mA}$$

and
$$I_R = \frac{V_R}{R} = \frac{6\ \text{V}}{1\ \text{k}\Omega} = 6\ \text{mA}$$

so that
$$I_Z = I_R - I_L\ [\text{Eq. (2.18)}]$$
$$= 6\ \text{mA} - 3.33\ \text{mA}$$
$$= \mathbf{2.67\ mA}$$

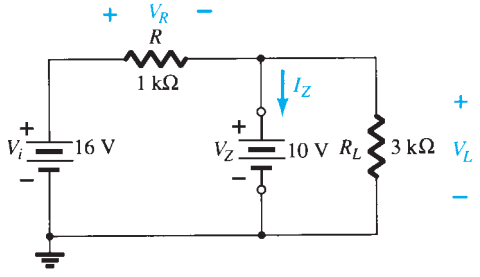


FIG. 2.118
Network of Fig. 2.115 in the "on" state.

The power dissipated is

$$P_Z = V_Z I_Z = (10\ \text{V})(2.67\ \text{mA}) = \mathbf{26.7\ mW}$$

which is less than the specified $P_{ZM} = 30$ mW.

Fixed V_i, Variable R_L

Due to the offset voltage V_Z, there is a specific range of resistor values (and therefore load current) that will ensure that the Zener is in the "on" state. Too small a load resistance R_L will result in a voltage V_L across the load resistor less than V_Z, and the Zener device will be in the "off" state.

To determine the minimum load resistance of Fig. 2.112 that will turn the Zener diode on, simply calculate the value of R_L that will result in a load voltage $V_L = V_Z$. That is,

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

Solving for R_L, we have

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} \tag{2.20}$$

Any load resistance value greater than the R_L obtained from Eq. (2.20) will ensure that the Zener diode is in the "on" state and the diode can be replaced by its V_Z source equivalent.

The condition defined by Eq. (2.20) establishes the minimum R_L, but in turn specifies the maximum I_L as

$$I_{L_{\max}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{\min}}} \tag{2.21}$$

Once the diode is in the "on" state, the voltage across R remains fixed at

$$V_R = V_i - V_Z \tag{2.22}$$

and I_R remains fixed at

$$I_R = \frac{V_R}{R} \tag{2.23}$$

The Zener current

$$I_Z = I_R - I_L \tag{2.24}$$

resulting in a minimum I_Z when I_L is a maximum and a maximum I_Z when I_L is a minimum value, since I_R is constant.

Since I_Z is limited to I_{ZM} as provided on the data sheet, it does affect the range of R_L and therefore I_L. Substituting I_{ZM} for I_Z establishes the minimum I_L as

$$I_{L_{\min}} = I_R - I_{ZM} \tag{2.25}$$

and the maximum load resistance as

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}} \tag{2.26}$$

EXAMPLE 2.27

a. For the network of Fig. 2.119, determine the range of R_L and I_L that will result in V_{RL} being maintained at 10 V.
b. Determine the maximum wattage rating of the diode.

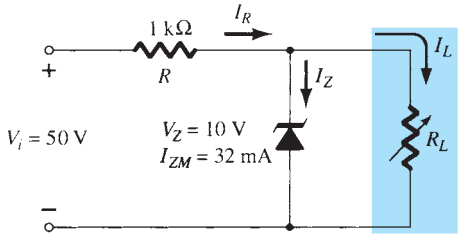


FIG. 2.119
Voltage regulator for Example 2.27.

Solution:

a. To determine the value of R_L that will turn the Zener diode on, apply Eq. (2.20):

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} = \frac{(1\text{ k}\Omega)(10\text{ V})}{50\text{ V} - 10\text{ V}} = \frac{10\text{ k}\Omega}{40} = \mathbf{250\ \Omega}$$

The voltage across the resistor R is then determined by Eq. (2.22):

$$V_R = V_i - V_Z = 50\text{ V} - 10\text{ V} = \mathbf{40\ V}$$

and Eq. (2.23) provides the magnitude of I_R:

$$I_R = \frac{V_R}{R} = \frac{40\text{ V}}{1\text{ k}\Omega} = \mathbf{40\ mA}$$

The minimum level of I_L is then determined by Eq. (2.25):

$$I_{L_{\min}} = I_R - I_{ZM} = 40\text{ mA} - 32\text{ mA} = \mathbf{8\ mA}$$

with Eq. (2.26) determining the maximum value of R_L:

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}} = \frac{10\text{ V}}{8\text{ mA}} = \mathbf{1.25\ k\Omega}$$

A plot of V_L versus R_L appears in Fig. 2.120a and for V_L versus I_L in Fig. 2.120b.

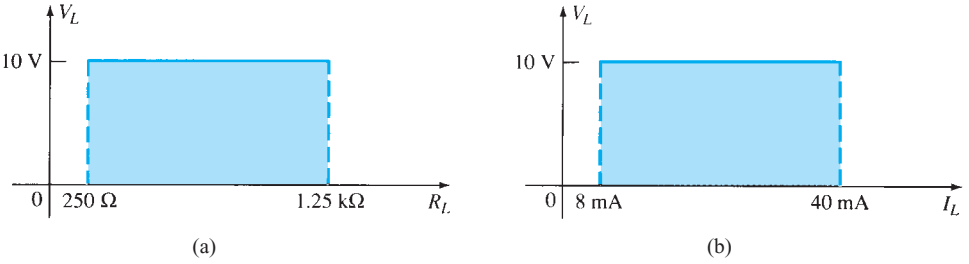


FIG. 2.120
V_L versus R_L and I_L for the regulator of Fig. 2.119.

b. $P_{\max} = V_Z I_{ZM}$
$= (10\text{ V})(32\text{ mA}) = \mathbf{320\ mW}$

Fixed R_L, Variable V_i

For fixed values of R_L in Fig. 2.112, the voltage V_i must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage $V_i = V_{i_{\min}}$ is determined by

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

and

$$\boxed{V_{i_{\min}} = \frac{(R_L + R)V_Z}{R_L}} \qquad \textbf{(2.27)}$$

The maximum value of V_i is limited by the maximum Zener current I_{ZM}. Since $I_{ZM} = I_R - I_L$,

$$\boxed{I_{R_{\max}} = I_{ZM} + I_L} \qquad \textbf{(2.28)}$$

Since I_L is fixed at V_Z/R_L and I_{ZM} is the maximum value of I_Z, the maximum V_i is defined by

$$V_{i_{\max}} = V_{R_{\max}} + V_Z$$

$$\boxed{V_{i_{\max}} = I_{R_{\max}} R + V_Z} \qquad \textbf{(2.29)}$$

EXAMPLE 2.28 Determine the range of values of V_i that will maintain the Zener diode of Fig. 2.121 in the "on" state.

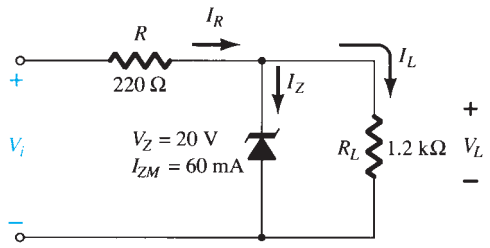


FIG. 2.121
Regulator for Example 2.28.

Solution:

Eq. (2.27):
$$V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L} = \frac{(1200\ \Omega + 220\ \Omega)(20\ \text{V})}{1200\ \Omega} = \mathbf{23.67\ V}$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20\ \text{V}}{1.2\ \text{k}\Omega} = 16.67\ \text{mA}$$

Eq. (2.28):
$$I_{R_{max}} = I_{ZM} + I_L = 60\ \text{mA} + 16.67\ \text{mA}$$
$$= 76.67\ \text{mA}$$

Eq. (2.29):
$$V_{i_{max}} = I_{R_{max}}R + V_Z$$
$$= (76.67\ \text{mA})(0.22\ \text{k}\Omega) + 20\ \text{V}$$
$$= 16.87\ \text{V} + 20\ \text{V}$$
$$= \mathbf{36.87\ V}$$

A plot of V_L versus V_i is provided in Fig. 2.122.

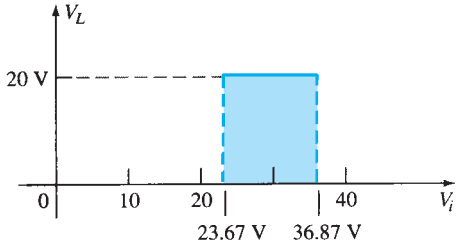


FIG. 2.122
V_L versus V_i for the regulator of Fig. 2.121.

The results of Example 2.28 reveal that for the network of Fig. 2.121 with a fixed R_L, the output voltage will remain fixed at 20 V for a range of input voltage that extends from 23.67 V to 36.87 V.

2.12 VOLTAGE-MULTIPLIER CIRCUITS

Voltage-multiplier circuits are employed to maintain a relatively low transformer peak voltage while stepping up the peak output voltage to two, three, four, or more times the peak rectified voltage.

Voltage Doubler

The network of Fig. 2.123 is a half-wave voltage doubler. During the positive voltage half-cycle across the transformer, secondary diode D_1 conducts (and diode D_2 is cut off), charging capacitor C_1 up to the peak rectified voltage (V_m). Diode D_1 is ideally a short during this half-cycle, and the input voltage charges capacitor C_1 to V_m with the polarity shown in Fig. 2.124a. During the negative half-cycle of the secondary voltage, diode D_1 is cut off and diode D_2 conducts charging capacitor C_2. Since diode D_2 acts as a short during the negative half-cycle (and diode D_1 is open), we can sum the voltages around the outside loop (see Fig. 2.124b):

$$-V_m - V_{C_1} + V_{C_2} = 0$$
$$-V_m - V_m + V_{C_2} = 0$$

from which we obtain

$$V_{C_2} = 2V_m$$

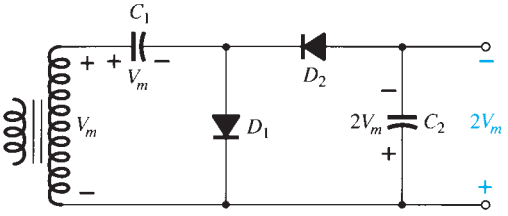


FIG. 2.123
Half-wave voltage doubler.

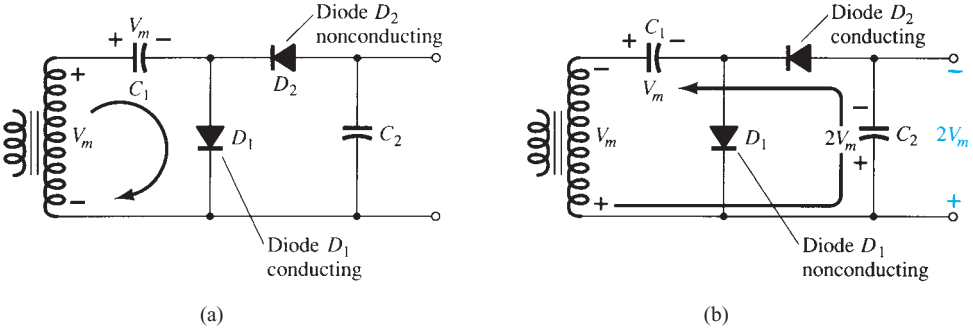


FIG. 2.124
Double operation, showing each half-cycle of operation: (a) positive half-cycle; (b) negative half-cycle.

On the next positive half-cycle, diode D_2 is nonconducting and capacitor C_2 will discharge through the load. If no load is connected across capacitor C_2, both capacitors stay charged—C_1 to V_m and C_2 to $2V_m$. If, as would be expected, there is a load connected to the output of the voltage doubler, the voltage across capacitor C_2 drops during the positive half-cycle (at the input) and the capacitor is recharged up to $2V_m$ during the negative half-cycle. The output waveform across capacitor C_2 is that of a half-wave signal filtered by a capacitor filter. The peak inverse voltage across each diode is $2V_m$.

Another doubler circuit is the full-wave doubler of Fig. 2.125. During the positive half-cycle of transformer secondary voltage (see Fig. 2.126a) diode D_1 conducts, charging capacitor C_1 to a peak voltage V_m. Diode D_2 is nonconducting at this time.

During the negative half-cycle (see Fig. 2.126b) diode D_2 conducts, charging capacitor C_2, while diode D_1 is nonconducting. If no load current is drawn from the circuit, the voltage across capacitors C_1 and C_2 is $2V_m$. If load current is drawn from the circuit, the voltage across capacitors C_1 and C_2 is the same as that across a capacitor fed by a full-wave rectifier circuit. One difference is that the effective capacitance is that of C_1 and C_2 in series, which is less than the capacitance of either C_1 or C_2 alone. The lower capacitor value will provide poorer filtering action than the single-capacitor filter circuit.

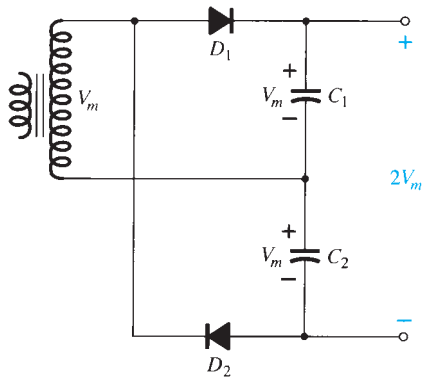


FIG. 2.125
Full-wave voltage doubler.

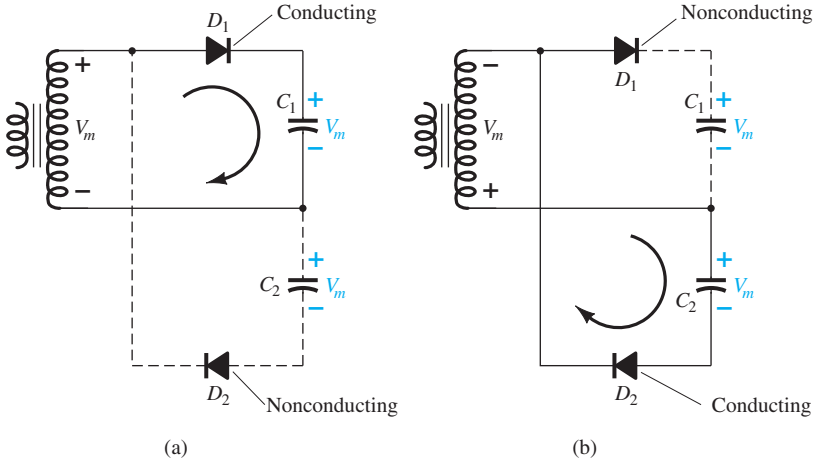


FIG. 2.126
Alternate half-cycles of operation for full-wave voltage doubler.

The peak inverse voltage across each diode is $2V_m$, as it is for the filter capacitor circuit. In summary, the half-wave or full-wave voltage-doubler circuits provide twice the peak voltage of the transformer secondary while requiring no center-tapped transformer and only $2V_m$ PIV rating for the diodes.

Voltage Tripler and Quadrupler

Figure 2.127 shows an extension of the half-wave voltage doubler, which develops three and four times the peak input voltage. It should be obvious from the pattern of the circuit

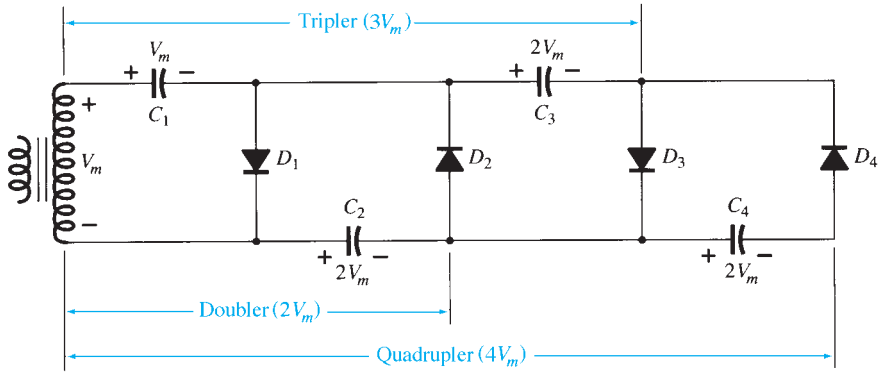


FIG. 2.127
Voltage tripler and quadrupler.

connection how additional diodes and capacitors may be connected so that the output voltage may also be five, six, seven, and so on, times the basic peak voltage (V_m).

In operation, capacitor C_1 charges through diode D_1 to a peak voltage V_m during the positive half-cycle of the transformer secondary voltage. Capacitor C_2 charges to twice the peak voltage, $2V_m$, developed by the sum of the voltages across capacitor C_1 and the transformer during the negative half-cycle of the transformer secondary voltage.

During the positive half-cycle, diode D_3 conducts and the voltage across capacitor C_2 charges capacitor C_3 to the same $2V_m$ peak voltage. On the negative half-cycle, diodes D_2 and D_4 conduct with capacitor C_3, charging C_4 to $2V_m$.

The voltage across capacitor C_2 is $2V_m$, across C_1 and C_3 it is $3V_m$, and across C_2 and C_4 it is $4V_m$. If additional sections of diode and capacitor are used, each capacitor will be charged to $2V_m$. Measuring from the top of the transformer winding (Fig. 2.127) will provide odd multiples of V_m at the output, whereas measuring the output voltage from the bottom of the transformer will provide even multiples of the peak voltage V_m.

The transformer rating is only V_m, maximum, and each diode in the circuit must be rated at $2V_m$ PIV. If the load is small and the capacitors have little leakage, extremely high dc voltages may be developed by this type of circuit, using many sections to step up the dc voltage.

2.13 PRACTICAL APPLICATIONS

The range of practical applications for diodes is so broad that it would be virtually impossible to consider all the options in one section. However, to develop some sense for the use of the device in everyday networks, a number of common areas of application are introduced below. In particular, note that the use of diodes extends well beyond the important switching characteristic that was introduced earlier in this chapter.

Rectification

Battery chargers are a common household piece of equipment used to charge everything from small flashlight batteries to heavy-duty, marine, lead-acid batteries. Since all are plugged into a 120-V ac outlet such as found in the home, the basic construction of each is quite similar. In every charging system a *transformer* must be included to cut the ac voltage to a level appropriate for the dc level to be established. A *diode* (also called *rectifier*) arrangement must be included to convert the ac voltage, which varies with time, to a fixed dc level such as described in this chapter. Some dc chargers also include a *regulator* to provide an improved dc level (one that varies less with time or load). Since the car battery charger is one of the most common, it will be described in the next few paragraphs.

The outside appearance and the internal construction of a Sears 6/2 AMP Manual Battery Charger are provided in Fig. 2.128. Note in Fig. 2.128b that the transformer (as in most chargers) takes up most of the internal space. The additional air space and the holes in the casing are there to ensure an outlet for the heat that develops due to the resulting current levels.

The schematic of Fig. 2.129 includes all the basic components of the charger. Note first that the 120 V from the outlet are applied directly across the primary of the transformer. The charging rate of 6 A or 2 A is determined by the switch, which simply controls how many windings of the primary will be in the circuit for the chosen charging rate. If the battery is charging at the 2-A level, the full primary will be in the circuit, and the ratio of the turns in the primary to the turns in the secondary will be a maximum. If it is charging at the 6-A level, fewer turns of the primary are in the circuit, and the ratio drops. When you study transformers, you will find that the voltage at the primary and secondary is directly related to the *turns ratio*. If the ratio from primary to secondary drops, then the voltage drops also. The reverse effect occurs if the turns on the secondary exceed those on the primary.

The general appearance of the waveforms appears in Fig. 2.129 for the 6-A charging level. Note that so far, the ac voltage has the same wave shape across the primary and the secondary. The only difference is in the peak value of the waveforms. Now the diodes take

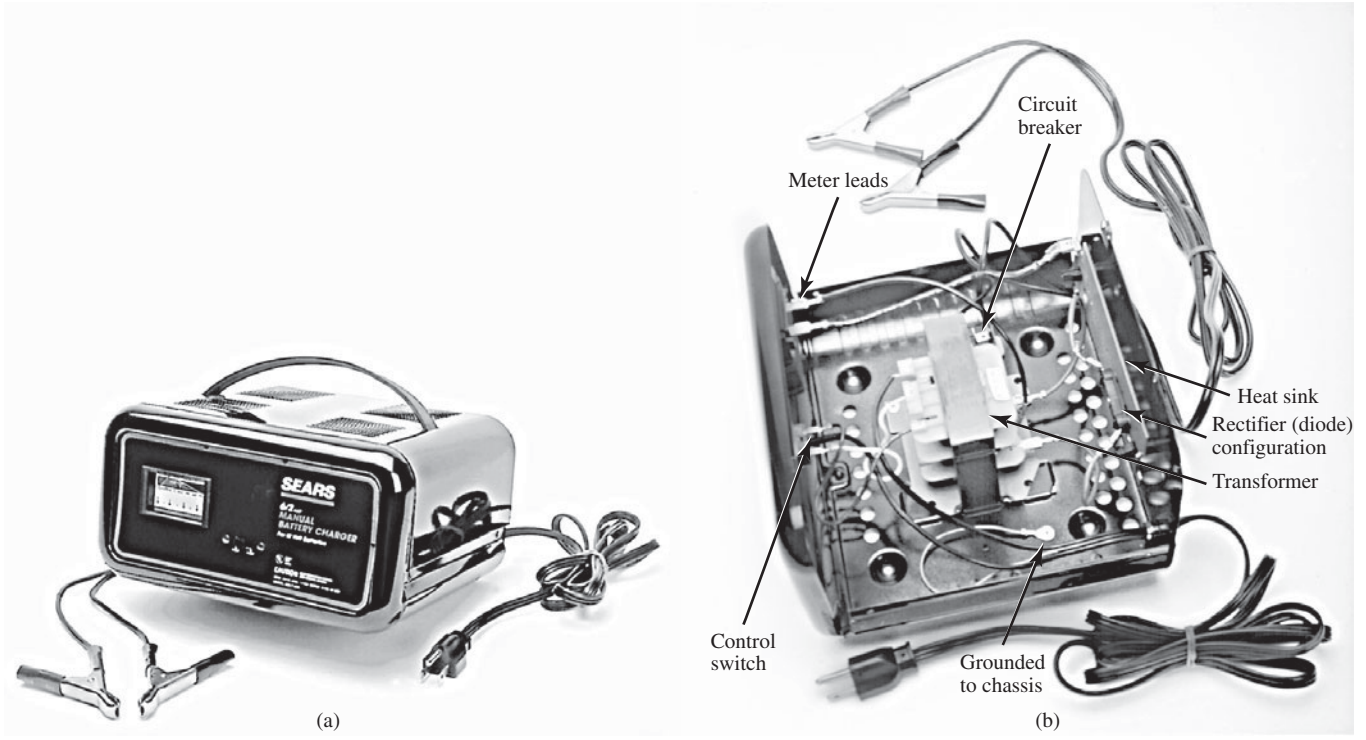


FIG. 2.128

Battery charger: (a) external appearance; (b) internal construction.

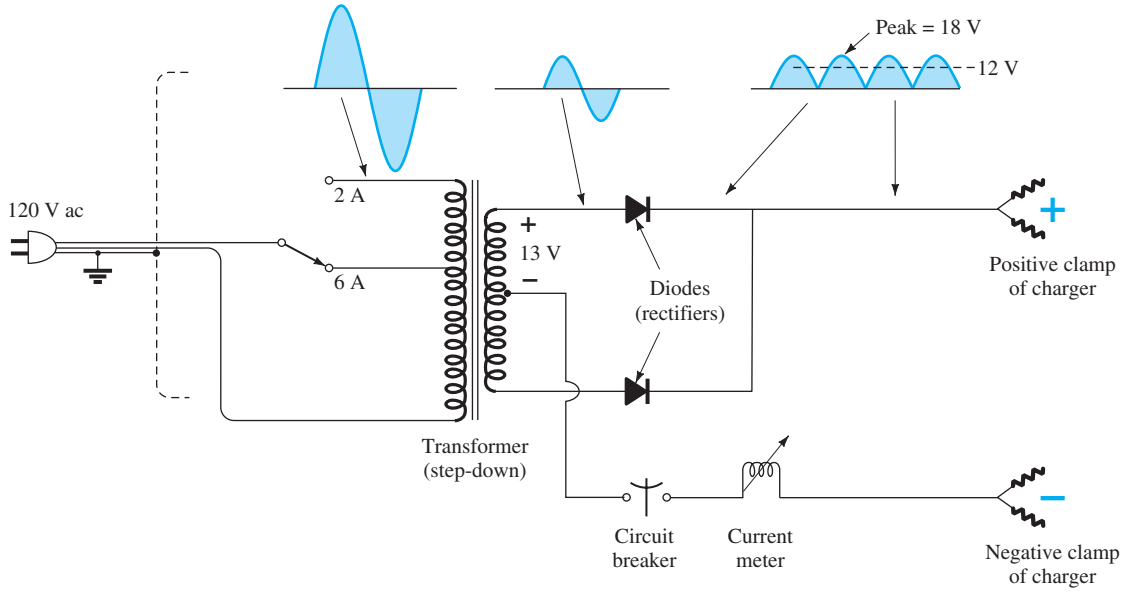


FIG. 2.129

Electrical schematic for the battery charger of Fig. 2.128.

over and convert the ac waveform, which has zero average value (the waveform above equals the waveform below), to one that has an average value (all above the axis) as shown in the same figure. For the moment simply recognize that diodes are semiconductor electronic devices that permit only conventional current to flow through them in the direction indicated by the arrow in the symbol. Even though the waveform resulting from the diode action has a pulsing appearance with a peak value of about 18 V, it will charge the 12-V battery whenever its voltage is greater than that of the battery, as shown by the shaded area.

Below the 12-V level the battery cannot discharge back into the charging network because the diodes permit current flow in only one direction.

In particular, note in Fig. 2.128b the large plate that carries the current from the rectifier (diode) configuration to the positive terminal of the battery. Its primary purpose is to provide a *heat sink* (a place for the heat to be distributed to the surrounding air) for the diode configuration. Otherwise the diodes would eventually melt down and self-destruct due to the resulting current levels. Each component of Fig. 2.129 has been carefully labeled in Fig. 2.128b for reference.

When current is first applied to a battery at the 6-A charge rate, the current demand, as indicated by the meter on the face of the instrument, may rise to 7 A or almost 8 A. However, the level of current will decrease as the battery charges until it drops to a level of 2 A or 3 A. For units such as this that do not have an automatic shutoff, it is important to disconnect the charger when the current drops to the fully charged level; otherwise, the battery will become overcharged and may be damaged. A battery that is at its 50% level can take as long as 10 hours to charge, so one should not expect it to be a 10-minute operation. In addition, if a battery is in very bad shape, with a lower than normal voltage, the initial charging current may be too high for the design. To protect against such situations, the circuit breaker will open and stop the charging process. Because of the high current levels, it is important that the directions provided with the charger be carefully read and applied.

In an effort to compare the theoretical world with the real world, a load (in the form of a headlight) was applied to the charger to permit a viewing of the actual output waveform. It is important to note and remember that **a diode with zero current through it will not display its rectifying capabilities**. In other words, the output from the charger of Fig. 2.129 will not be a rectified signal unless a load is applied to the system to draw current through the diode. Recall from the diode characteristics that when $I_D = 0$ A, $V_D = 0$ V.

By applying the headlamp as a load, however, sufficient current is drawn through the diode for it to behave like a switch and convert the ac waveform to a pulsating one as shown in Fig. 2.130 for the 6-A setting. First note that the waveform is slightly distorted by the nonlinear characteristics of the transformer and the nonlinear characteristics of the diode at low currents. The waveform, however, is certainly close to what is expected when we compare it to the theoretical patterns of Fig. 2.129. The peak value is determined from the vertical sensitivity as

$$V_{peak} = (3.3 \text{ divisions})(5 \text{ V/division}) = 16.5 \text{ V vs. the 18 V of Fig. 1.129}$$

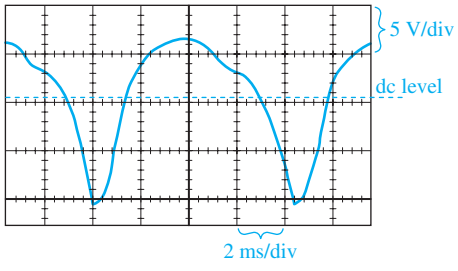


FIG. 2.130
Pulsating response of the charger of Fig. 2.129 to the application of a headlamp as a load.

with a dc level of

$$V_{dc} = 0.636V_{peak} = 0.636(16.5 \text{ V}) = 10.49 \text{ V}$$

A dc meter connected across the load registered 10.41 V, which is very close to the theoretical average (dc) level of 10.49 V.

One may wonder how a charger having a dc level of 10.49 V can charge a 12-V battery to a typical level of 14 V. It is simply a matter of realizing that (as shown in Fig. 2.130) for a good deal of each pulse, the voltage across the battery will be greater than 12 V and the battery will be charging—a process referred to as **trickle charging**. In other words, charging does not occur during the entire cycle, but only when the charging voltage is more than the voltage of the battery.

Protective Configurations

Diodes are used in a variety of ways to protect elements and systems from excessive voltages or currents, polarity reversals, arcing, and shorting, to name a few. In Fig. 2.131a, the switch on a simple *RL* circuit has been closed, and the current will rise to a level determined by the applied voltage and series resistor *R* as shown on the plot. Problems arise when the switch is quickly opened as in Fig. 2.131b to essentially tell the circuit that the current must drop to zero almost instantaneously. You will remember from your basic circuits courses, however, that the inductor will not permit an instantaneous change in current through the coil. A conflict results, which will establish arcing across the contacts of the switch as the coil tries to find a path for discharge. Recall also that the voltage across an inductor is directly related to the rate of change in current through the coil ($v_L = L\,di_L/dt$). When the switch is opened, it is trying to dictate that the current change almost instantaneously, causing a very high voltage to develop across the coil that will then appear across the contacts to establish this arcing current. Levels in the thousands of volts will develop across the contacts, which will soon, if not immediately, damage the contacts and thereby the switch. The effect is referred to as an "inductive kick." Note also that the polarity of the voltage across the coil during the "build-up" phase is opposite to that during the "release" phase. This is due to the fact that the current must maintain the same direction before and after the switch is opened. During the "build-up" phase, the coil appears as a load, whereas during the release phase, it has the characteristics of a source. In general, therefore, always keep in mind that

Trying to change the current through an inductive element too quickly may result in an inductive kick that could damage surrounding elements or the system itself.

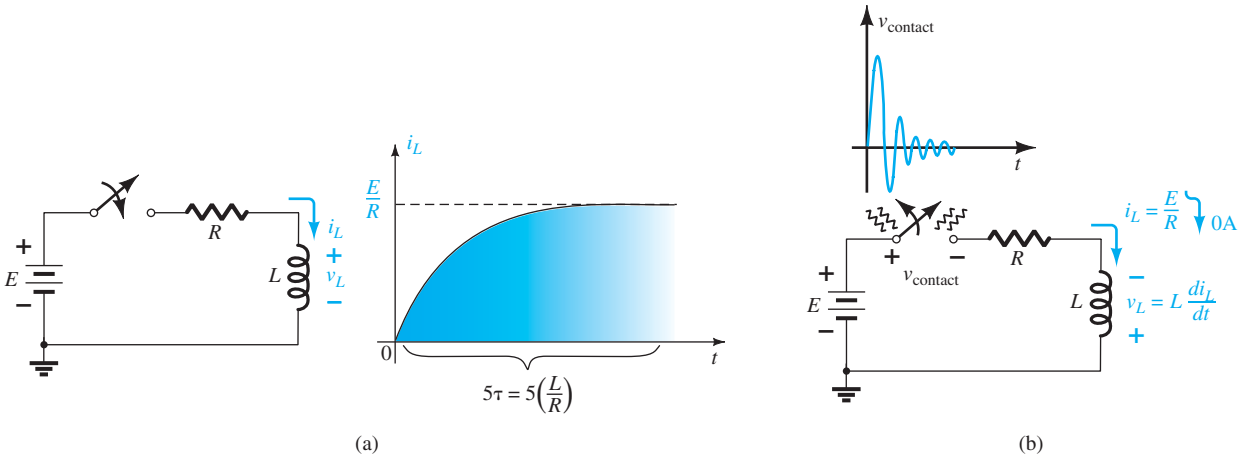


FIG. 2.131

(a) Transient phase of a simple RL circuit; (b) arcing that results across a switch when opened in series with an RL circuit.

In Fig. 2.132a the simple network above may be controlling the action of a relay. When the switch is closed, the coil will be energized, and steady-state current levels will be established. However, when the switch is opened to deenergize the network, we have the problem introduced above because the electromagnet controlling the relay action will appear as a coil to the energizing network. One of the cheapest but most effective ways to protect the switching system is to place a capacitor (called a "snubber") across the terminals of the coil as shown in Fig. 2.132b. When the switch is opened, the capacitor will initially appear as a short to the coil and will provide a current path that will bypass the dc supply and switch. The capacitor has the characteristics of a short (very low resistance) because of the high-frequency characteristics of the surge voltage, as shown in Fig. 2.131b. Recall that the reactance of a capacitor is determined by $X_C = 1/2\pi fC$, so the higher the frequency, the less is the resistance. Normally, because of the high surge voltages and relatively low cost, ceramic capacitors of about 0.01 μF are used. You don't want to use large capacitors because the voltage across the capacitor will build up too slowly and will essentially slow down the

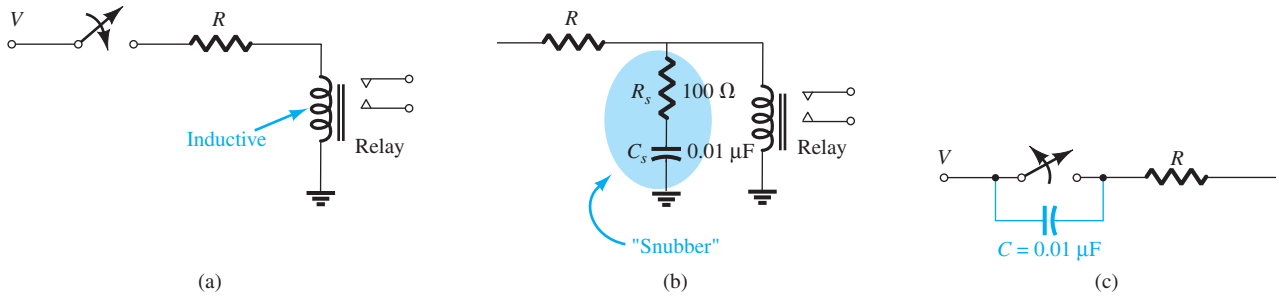


FIG. 2.132

(a) Inductive characteristics of a relay; (b) snubber protection for the configuration of part (a); (c) capacitive protection for a switch.

performance of the system. The resistor of 100 Ω in series with the capacitor is introduced solely to limit the surge current that will result when a change in state is called for. Often, the resistor does not appear because of the internal resistance of the coil as established by many turns of fine wire. On occasion, you may find the capacitor across the switch as shown in Fig. 2.132c. In this case, the shorting characteristics of the capacitor at high frequencies will bypass the contacts with the switch and extend its life. Recall that the voltage across a capacitor cannot change instantaneously. In general, therefore,

Capacitors in parallel with inductive elements or across switches are often there to act as protective elements, not as typical network capacitive elements.

Finally, the diode is often used as a protective device for situations such as above. In Fig. 2.133, a diode has been placed in parallel with the inductive element of the relay configuration. When the switch is opened or the voltage source quickly disengaged, the polarity of the voltage across the coil is such as to turn the diode on and conduct in the direction indicated. The inductor now has a conduction path through the diode rather than through the supply and switch, thereby saving both. Since the current established through the coil must now switch directly to the diode, the diode must be able to carry **the same level of current** that was passing through the coil before the switch was opened. The rate at which the current collapses will be controlled by the resistance of the coil and the diode. It can be reduced by placing an additional resistor in series with the diode. The advantage of the diode configuration over that of the snubber is that the diode reaction and behavior are not frequency dependent. However, the protection offered by the diode will not work if the applied voltage is an alternating one such as ac or a square wave since the diode will conduct for one of the applied polarities. For such alternating systems, the "snubber" arrangement would be the best option.

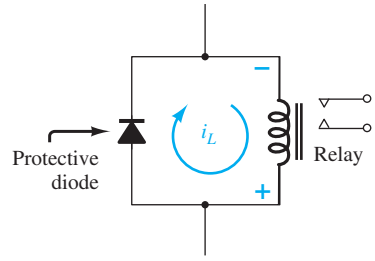


FIG. 2.133

Diode protection for an RL circuit.

In the next chapter we will find that the base-to-emitter junction of a transistor is forward-biased. That is, the voltage V_{BE} of Fig. 2.134a will be about 0.7 V positive. To prevent a situation where the emitter terminal would be made more positive than the base terminal by a voltage that could damage the transistor, the diode shown in Fig. 2.134a is added. The diode will prevent the reverse-bias voltage V_{EB} from exceeding 0.7 V. On

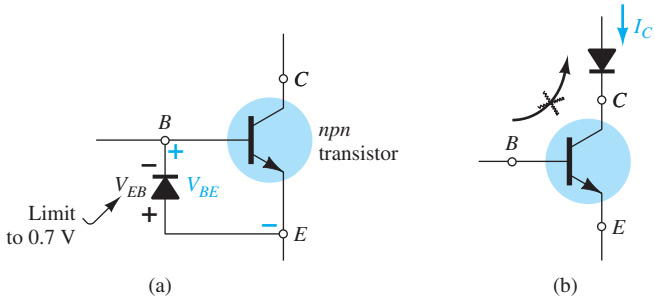


FIG. 2.134

(a) Diode protection to limit the emitter-to-base voltage of a transistor; (b) diode protection to prevent a reversal in collector current.

occasion, you may also find a diode in series with the collector terminal of a transistor as shown in Fig. 2.134b. Normal transistor action requires that the collector be more positive than the base or emitter terminal to establish a collector current in the direction shown. However, if a situation arises where the emitter or base terminal is at a higher potential than the collector terminal, the diode will prevent conduction in the opposite direction. In general, therefore,

Diodes are often used to prevent the voltage between two points from exceeding 0.7 V or to prevent conduction in a particular direction.

As shown in Fig. 2.135, diodes are often used at the input terminals of systems such as op-amps to limit the swing of the applied voltage. For the 400-mV level the signal will pass undisturbed to the input terminals of the op-amp. However, if the voltage jumps to a level of 1 V, the top and bottom peaks will be clipped off before appearing at the input terminals of the op-amp. Any clipped-off voltage will appear across the series resistor R_1.

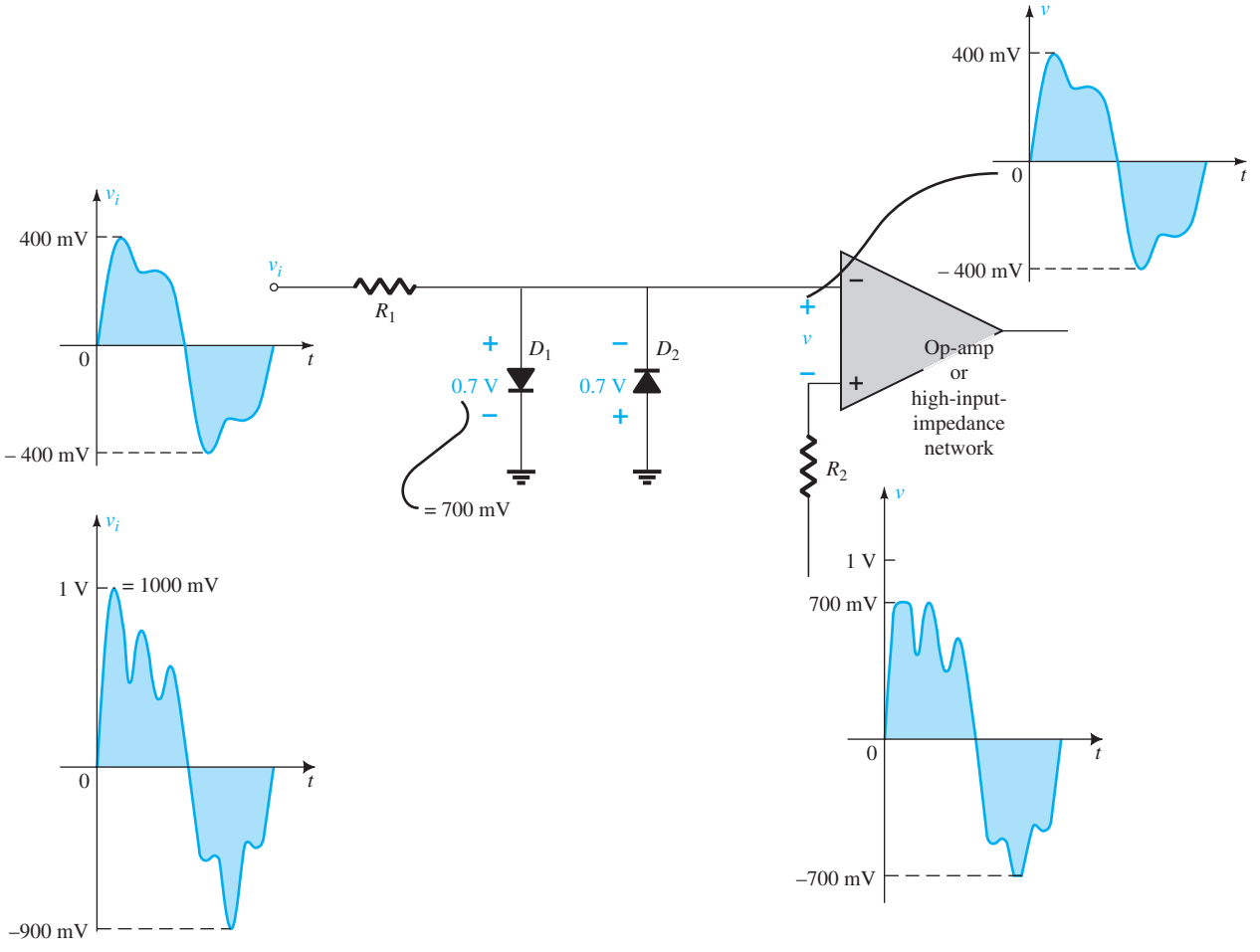


FIG. 2.135

Diode control of the input swing to an op-amp or a high-input-impedance network.

The controlling diodes of Fig. 2.135 may also be drawn as shown in Fig. 2.136 to control the signal appearing at the input terminals of the op-amp. In this example, the diodes are acting more like shaping elements than as limiters as in Fig. 2.135. However, the point is that

The placement of elements may change, but their function may still be the same. Do not expect every network to appear exactly as you studied it for the first time.

In general, therefore, don't always assume that diodes are used simply as switches. There is a wide variety of uses for diodes as protective and limiting devices.

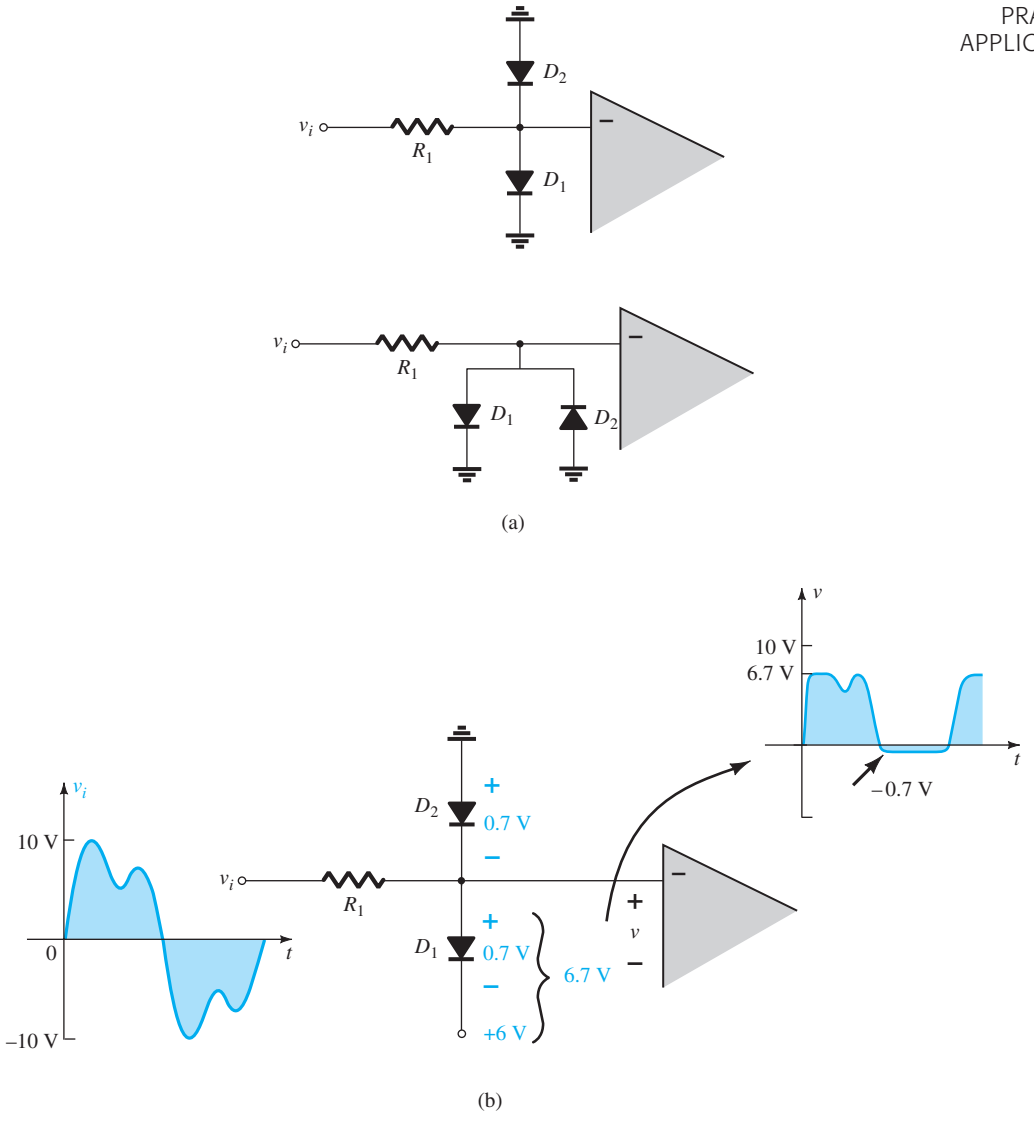


FIG. 2.136

(a) Alternate appearances for the network of Fig. 2.135; (b) establishing random levels of control with separate dc supplies.

Polarity Insurance

There are numerous systems that are very sensitive to the polarity of the applied voltage. For instance, in Fig. 2.137a, assume for the moment that there is a very expensive piece of equipment that would be damaged by an incorrectly applied bias. In Fig. 2.137b the correct applied bias is shown on the left. As a result, the diode is reverse-biased, but the system works just fine—the diode has no effect. However, if the wrong polarity is applied as

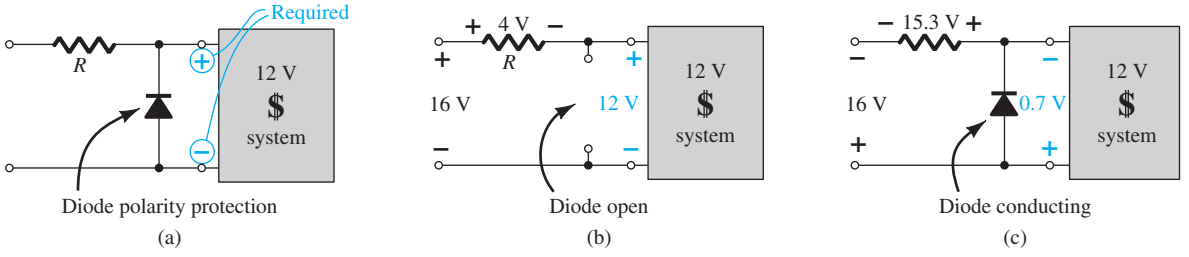


FIG. 2.137

(a) Polarity protection for an expensive, sensitive piece of equipment; (b) correctly applied polarity; (c) application of the wrong polarity.

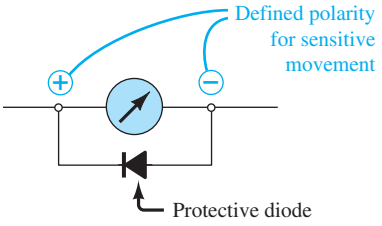


FIG. 2.138
Protection for a sensitive meter movement.

shown in Fig. 2.137c, the diode will conduct and ensure that no more than 0.7 V will appear across the terminals of the system, protecting it from excessive voltages of the wrong polarity. For either polarity, the difference between the applied voltage and the load or diode voltage will appear across the series source or network resistance.

In Fig. 2.138 a sensitive measuring movement cannot withstand voltages greater than 1 V of the wrong polarity. With this simple design the sensitive movement is protected from voltages of the wrong polarity of more than 0.7 V.

Controlled Battery-Powered Backup

In numerous situations a system should have a backup power source to ensure that the system will still be operational in case of a loss of power. This is especially true of security systems and lighting systems that must turn on during a power failure. It is also important when a system such as a computer or a radio is disconnected from its ac-to-dc power conversion source to a portable mode for traveling. In Fig. 2.139 the 12-V car radio operating off the 12-V dc power source has a 9-V battery backup system in a small compartment in the back of the radio ready to take over the role of saving the clock mode and the channels stored in memory when the radio is removed from the car. With the full 12 V available from the car, D_1 is conducting, and the voltage at the radio is about 11.3 V. D_2 is reverse-biased (an open circuit), and the reserve 9-V battery inside the radio is disengaged. However, when the radio is removed from the car, D_1 will no longer be conducting because the 12-V source is no longer available to forward-bias the diode. However, D_2 will be forward-biased by the 9-V battery, and the radio will continue to receive about 8.3 V to maintain the memory that has been set for components such as the clock and the channel selections.

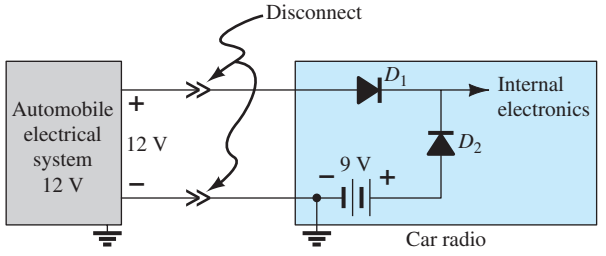


FIG. 2.139
Backup system designed to prevent the loss of memory in a car radio when the radio is removed from the car.

Polarity Detector

Through the use of LEDs of different colors, the simple network of Fig. 2.140 can be used to check the polarity at any point in a dc network. When the polarity is as indicated for the applied 6 V, the top terminal is positive, D_1 will conduct along with LED1, and a green light will result. Both D_2 and LED2 will be back-biased for the above polarity. However, if the polarity at the input is reversed, D_2 and LED2 will conduct, and a red light will appear, defining the top lead as the lead at the negative potential. It would appear that the

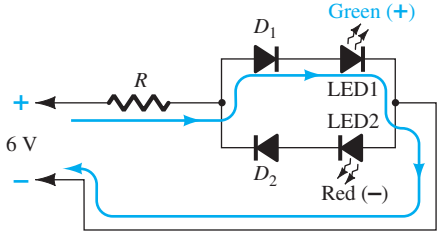


FIG. 2.140
Polarity detector using diodes and LEDs.

network would work without diodes D_1 and D_2. However, in general, LEDs do not like to be reverse-biased because of sensitivity built in during the doping process. Diodes D_1 and D_2 offer a series open-circuit condition that provides some protection to the LEDs. In the forward-bias state, the additional diodes D_1 and D_2 reduce the voltage across the LEDs to more common operating levels.

Displays

Some of the primary concerns of using electric light bulbs in exit signs are their limited lifetime (requiring frequent replacement); their sensitivity to heat, fire, and so on; their durability factor when catastrophic accidents occur; and their high voltage and power requirements. For this reason LEDs are often used to provide the longer life span, higher durability levels, and lower demand voltage and power levels (especially when the reserve dc battery system has to take over).

In Fig. 2.141 a control network determines when the EXIT light should be on. When it is on, all the LEDs in series will be on, and the EXIT sign will be fully lit. Obviously, if one of the LEDs should burn out and open up, the entire section will turn off. However, this situation can be improved by simply placing parallel LEDs between every two points. Lose one, and you will still have the other parallel path. Parallel diodes will, of course, reduce the current through each LED, but two at a lower level of current can have a luminescence similar to one at twice the current. Even though the applied voltage is ac, which means that the diodes will turn on and off as the 60-Hz voltage swings positive and negative, the persistence of the LEDs will provide a steady light for the sign.

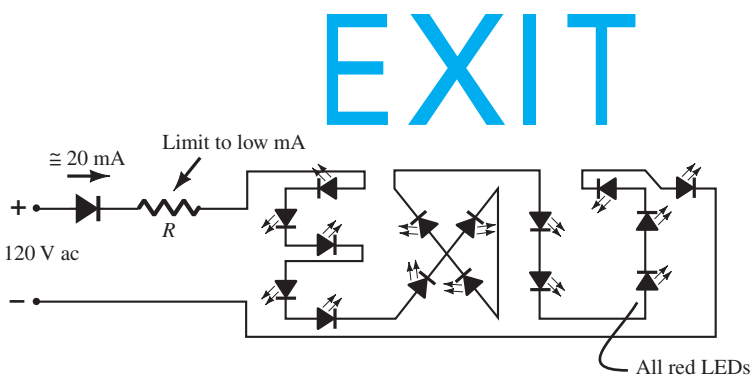


FIG. 2.141
EXIT sign using LEDs.

Setting Voltage Reference Levels

Diodes and Zeners can be used to set reference levels as shown in Fig. 2.142. The network, through the use of two diodes and one Zener diode, is providing three different voltage levels.

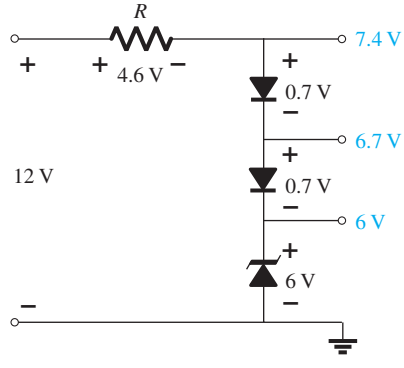


FIG. 2.142
Providing different reference levels using diodes.

Establishing a Voltage Level Insensitive to the Load Current

As an example that clearly demonstrates the difference between a resistor and a diode in a voltage-divider network, consider the situation of Fig. 2.143a, where a load requires about 6 V to operate properly but a 9-V battery is all that is available. For the moment let us assume that operating conditions are such that the load has an internal resistance of 1 kΩ. Using the voltage-divider rule, we can easily determine that the series resistor should be 470 Ω (commercially available value) as shown in Fig. 2.143b. The result is a voltage across the load of 6.1 V, an acceptable situation for most 6-V loads. However, if the operating conditions of the load change and the load now has an internal resistance of only 600 Ω, the load voltage will drop to about 4.9 V, and the system will not operate correctly. This sensitivity to the load resistance can be eliminated by connecting four diodes in series with the load as shown in Fig. 2.143c. When all four diodes conduct, the load voltage will be

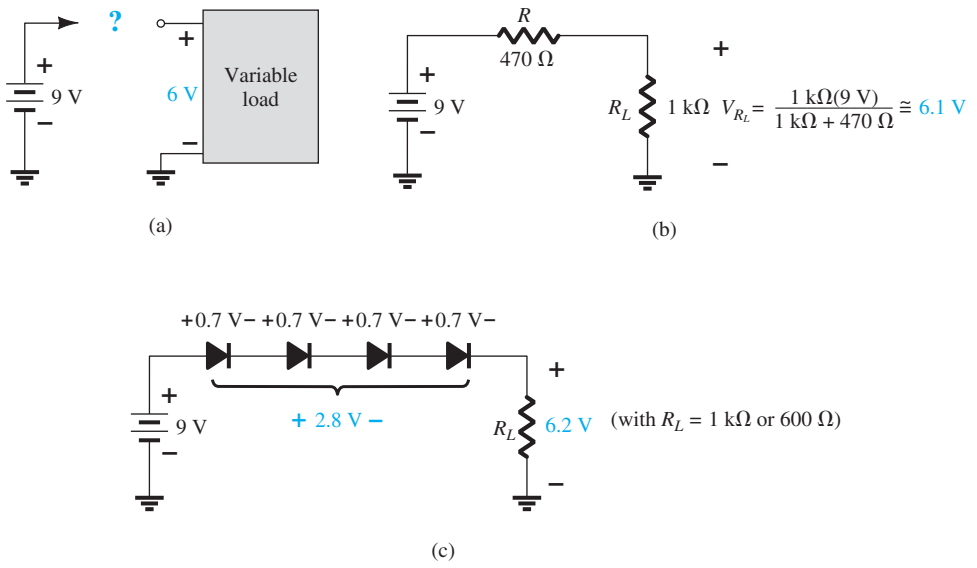


FIG. 2.143

(a) How to drive a 6-V load with a 9-V supply (b) using a fixed resistor value. (c) Using a series combination of diodes.

about 6.2 V, irrespective of the load impedance (within device limits, of course)—the sensitivity to the changing load characteristics has been removed.

AC Regulator and Square-Wave Generator

Two back-to-back Zeners can also be used as an ac regulator as shown in Fig. 2.144a. For the sinusoidal signal v_i the circuit will appear as shown in Fig. 2.144b at the instant $v_i = 10$ V. The region of operation for each diode is indicated in the adjoining figure. Note that Z_1 is in a low-impedance region, whereas the impedance of Z_2 is quite large, corresponding to the open-circuit representation. The result is that $v_o = v_i$ when $v_i = 10$ V. The input and the output will continue to duplicate each other until v_i reaches 20 V. Then Z_2 will "turn on" (as a Zener diode), whereas Z_1 will be in a region of conduction with a resistance level sufficiently small compared to the series 5-kΩ resistor to be considered a

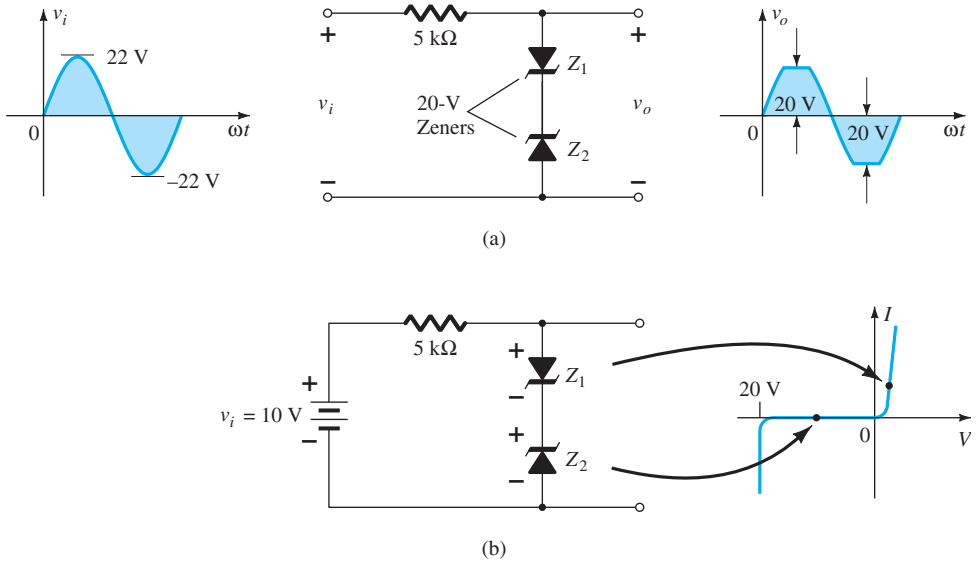


FIG. 2.144

Sinusoidal ac regulation: (a) 40-V peak-to-peak sinusoidal ac regulator; (b) circuit operation at $v_i = 10$ V.

short circuit. The resulting output for the full range of v_i is provided in Fig. 2.144a. Note that the waveform is not purely sinusoidal, but its root mean square (rms) value is lower than that associated with a full 22-V peak signal. The network is effectively limiting the rms value of the available voltage. The network of Fig. 2.144b can be extended to that of a simple square-wave generator (due to the clipping action) if the signal v_i is increased to perhaps a 50-V peak with 10-V Zeners as shown in Fig. 2.145 with the resulting output waveform.

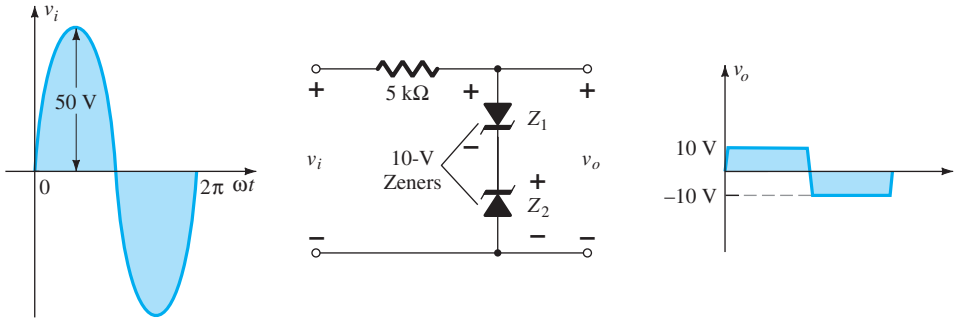


FIG. 2.145
Simple square-wave generator.

2.14 SUMMARY

Important Conclusions and Concepts

1. The characteristics of a diode are **unaltered** by the network in which it is employed. The network simply determines the point of operation of the device.
2. The operating point of a network is determined by the **intersection** of the network equation and an equation defining the characteristics of the device.
3. For most applications, the characteristics of a diode can be defined simply by the **threshold voltage in the forward-bias region** and an open circuit for applied voltages less than the threshold value.
4. To determine the state of a diode, simply **think of it initially as a resistor**, and find the polarity of the voltage across it and the direction of conventional current through it. If the voltage across it has a forward-bias polarity and the **current has a direction that matches the arrow in the symbol**, the diode is conducting.
5. To determine the state of diodes used in a logic gate, first make an **educated guess** about the state of the diodes, and then **test your assumptions**. If your estimate is incorrect, refine your guess and try again until the analysis verifies the conclusions.
6. Rectification is a process whereby an applied waveform of **zero average value** is changed to one that **has a dc level**. For applied signals of more than a few volts, the ideal diode approximations can normally be applied.
7. It is very important that the PIV rating of a diode be checked when choosing a diode for a particular application. Simply determine the **maximum voltage** across the diode under **reverse-bias conditions**, and compare it to the nameplate rating. For the typical half-wave and full-wave bridge rectifiers, it is the peak value of the applied signal. For the CT transformer full-wave rectifier, it is twice the peak value (which can get quite high).
8. Clippers are networks that "**clip**" away part of the applied signal either to create a specific type of signal or to limit the voltage that can be applied to a network.
9. Clampers are networks that "**clamp**" the input signal to a different dc level. In any event, the peak-to-peak swing of the applied signal will remain the same.
10. Zener diodes are diodes that make effective use of the **Zener breakdown potential** of an ordinary *p–n* junction characteristic to provide a device of wide importance and application. For Zener conduction, the direction of conventional flow is **opposite to the arrow in the symbol**. The polarity under conduction is also **opposite to that of the conventional diode**.

11. To determine the state of a Zener diode in a dc network, simply remove the Zener from the network, and determine the **open-circuit voltage** between the two points where the Zener diode was originally connected. If it is **more than the Zener potential** and has the correct polarity, the Zener diode is in the "on" state.
12. A half-wave or full-wave voltage doubler employs two capacitors; a tripler, three capacitors; and a quadrupler, four capacitors. In fact, for each, the number of diodes equals the number of capacitors.

Equations

Approximate:

Silicon: $V_K = 0.7\text{ V}$; I_D is determined by network.

Germanium: $V_K = 0.3\text{ V}$; I_D is determined by network.

Gallium arsenide: $V_K = 1.2\text{ V}$; I_D is determined by network.

Ideal:

$V_K = 0\text{ V}$; I_D is determined by network.

For conduction:

$$V_D \geq V_K$$

Half-wave rectifier:

$$V_{\text{dc}} = 0.318V_m$$

Full-wave rectifier:

$$V_{\text{dc}} = 0.636V_m$$

2.15 COMPUTER ANALYSIS

Cadence OrCAD

Series Diode Configuration In the previous chapter the OrCAD 16.3 folder was established as the location for our projects. This section will define the name of our project, set up the software for the analysis to be performed, describe how to build a simple circuit, and, finally, perform the analysis. The coverage will be quite extensive since this will be the first true exposure to the mechanics associated with using the software package. In the chapters to follow you will find the analysis can be performed quite rapidly to obtain results that confirm the long-hand solutions.

Our first project can now be initiated by double-clicking on the **OrCAD Capture CIS Demo** icon on the screen, or you can use the sequence **Start–All Programs–Cadence–OrCAD 16.3 Demo**. The resulting screen has only a few active keys on the top toolbar. The first at the top left is the **Create document** key (or you can use the sequence **File-New-Project**). Selecting the key will result in a **New Project** dialog box, in which the **Name** of the project must be entered. For our purposes we will choose **OrCAD 2-1** as shown in the heading of Fig. 2.146, and select **Analog or Mixed A/D** (to be used for all the analyses of this text). Note at the bottom of the dialog box that the **Location** appears as **C:\OrCAD 16.3** as set earlier. Click **OK**, and another dialog box will appear titled **Create PSpice Project**. Select **Create a blank project** (again, for all the analyses to be performed in this text). Click **OK**, and additional keys will be turned on along with additional toolbars. A **Project Manager Window** will appear with **OrCAD 2-1** as its heading. The new project listing will appear with an icon and an associated + sign in a small square. Clicking on the + sign will take the listing a step further to **SCHEMATIC1**. Click + again (to the left of SCHEMATIC1), and **PAGE1** will appear; clicking on a − sign will reverse the process. Double-clicking on **PAGE1** will create a working window titled **SCHEMATIC1: PAGE1**, revealing that a project can have more than one schematic file and more than one associated page. The width and the height of the window can be adjusted by grabbing an edge to obtain a double-headed arrow and dragging the border to the desired location. Either window on the screen can be moved by clicking on the top heading to make it dark blue and then dragging it to any location.

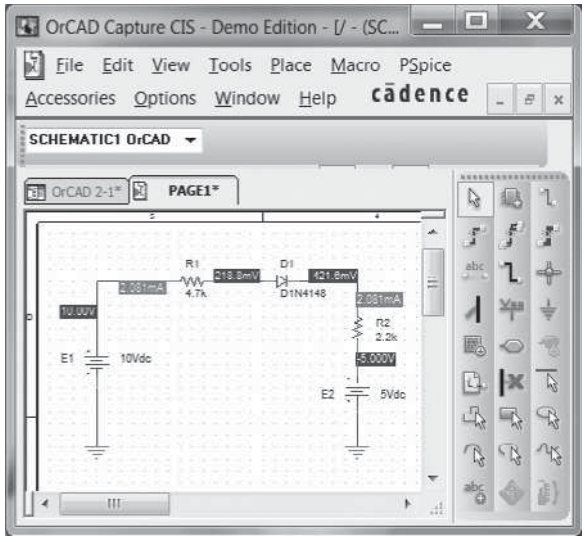


FIG. 2.146
Cadence OrCAD analysis of a series diode configuration.

Now we are ready to build the simple circuit of Fig. 2.146. Select the **Place part** key (the top key on the far right vertical toolbar that looks like an integrated circuit with a positive sign in the bottom right corner) to obtain the **Place Part** dialog box. Since this is the first circuit to be constructed, we must ensure that the parts appear in the list of active libraries. Go to **Libraries** and select the **Add Library** key (looks like a dashed rectangular box with a yellow star in the top left corner). The result is a **Browse File** in which **analog.olb** can be selected, followed by **Open** to place it in the active list of **Libraries**. Repeat the process to add the **eval.olb** and **source.olb** libraries. All three libraries will be required to build the networks appearing in this text. However, it is important to realize that:

Once the library files have been selected, they will appear in the active listing for each new project without having to add them each time—a step, such as the Folder step above, that does not have to be repeated with each similar project.

Click the small x in the top right corner of the dialog box to remove the **Place Part** dialog box. We can now place components on the screen. For the dc voltage source, first select the **Place Part** key and then select **SOURCE** in the library listing. Under **Part List**, a list of available sources will appear; select **VDC** for this project. Once **VDC** has been selected, its symbol, label, and value will appear on the picture window at the bottom left of the dialog box. Click the **Place Part** key on the top of the dialog box, and the **VDC** source will follow the cursor across the screen. Move it to a convenient location, left-click the mouse, and it will be set in place as shown in Fig. 2.146.

Since a second source is present in Fig. 2.146, move the cursor to the general area of the second source and click it in place. Since this is the last source to appear in the network, execute a right click of the mouse and select **End Mode**. Choosing this option will end the procedure, leaving the last source in a red dashed box. The fact that it is red indicates that it is still in the active mode and can be operated on. One more click of the mouse, and the second source will be in place and the red active status removed. The second source can be rotated 180° to match Fig. 2.146 by first clicking the source to make it red (active) to obtain a long list of options and select **Rotate**. Since each rotation only turns it 90° counterclockwise, two rotations will be required. The rotations can also be accomplished using the sequence **Ctrl-R**.

One of the most important steps in the procedure is to ensure that a 0-V ground potential is defined for the network so that voltages at any point in the network have a reference point. *The result is a requirement that every network must have a ground defined.* For our purposes, the **0/SOURCE** option will be our choice when the **GND** key is selected. It is obtained by selecting the ground symbol in the middle of the far right toolbar to obtain the **Place Ground** dialog box. Scroll down until **0/SOURCE** is selected and click **OK**. The result is a ground that can be placed anywhere on the screen. As with the voltage source,

multiple grounds can be added by simply going from one point to another. The process is ended with a right click and the **End Mode** option.

The next step will be to place the resistors of the network of Fig. 2.146. This is accomplished by selecting the **Place Part** key again and then selecting the **ANALOG** library. Scrolling the options, note that **R** will appear and should be selected. Click the **Place Part** key, and the resistor will appear next to the cursor on the screen. Move it to the desired location and click it in place. The second resistor can be placed by simply moving to the general area of its location in Fig. 2.146 and clicking it in place. Since there are only two resistors, the process can be ended by making a right click of the mouse and selecting **End Mode**. The second resistor will have to be rotated to the vertical position using the same procedure described for the second voltage source.

The last element to be placed is the diode. Selecting the **Place Part** keypad will again result in the **Place Part** dialog box, in which the **EVAL** library is chosen from the **Libraries** listing. Then type **D** under **Part** heading and select **D14148** under **Part List** followed by the **Place Part** command to place on the screen in the same manner described for the source and resistors.

Now that all the components are on the screen you may want to move them to positions corresponding directly with Fig. 2.146. This is accomplished by simply clicking on the element and holding the left-click down as you move the element.

All the required elements are on the screen, but they need to be connected. This is accomplished by selecting the **Place wire** key, which looks like a step, near the top of the toolbar to the left of the toolbar with the **Place Part** key. The result is a crosshair with a center that should be placed at the point to be connected. Place the crosshair at the top of the voltage source, and left-click it once to connect it to that point. Then draw a line to the end of the next element, and click the mouse again when the crosshair is at the correct point. A red line will result with a square at each end to confirm that the connection has been made. Then move the crosshair to the other elements, and build the circuit. Once everything is connected, a right click will provide the **End Mode** option. Don't forget to connect the source to ground as shown in Fig. 2.146.

Now we have all the elements in place, but their labels and values are wrong. To change any parameter, simply double-click on the parameter (the label or the value) to obtain the **Display Properties** dialog box. Type in the correct label or value, click **OK**, and the quantity is changed on the screen. The labels and values can be moved by simply clicking on the center of the parameter until it is closely surrounded by the four small squares and then dragging it to the new location. Another left click, and it is deposited in its new location.

Finally, we can initiate the analysis process, called **Simulation**, by selecting the **New Simulation Profile** key near the top left of the display—it resembles a data page with a star in the top right corner. A **New Simulation** dialog box will result that first asks for the **Name** of the simulation. **OrCAD 2-1** is entered, and **none** is left in the **Inherit From** request. Then select **Create**, and a **Simulation Setting** dialog box will appear in which **Analysis-Analysis Type-Bias Point** is sequentially selected. Click **OK**, and select the **Run** key (which looks like an isolated arrowhead in a green background) or choose **PSpice-Run** from the menu bar. An **Output Window** will result that appears to be somewhat inactive. It will not be used in the current analysis, so close (X) the window, and the circuit of Fig. 2.146 will appear with the voltage and current levels of the network. The voltage, current, or power levels can be removed (or replaced) from the display by simply selecting the **V**, **I**, or **W** in the third toolbar from the top. Individual values can be removed by simply selecting the value and pressing the **Delete** key. Resulting values can be moved by simply left-clicking the value and dragging it to the desired location.

The results of Fig. 2.146 show that the current through the series configuration is 2.081 mA through each element, compared to the 2.072 mA of Example 2.9. The voltage across the diode is 218.8 mV $-$ ($-$421.6 mV) $\cong$ 0.64 V, compared to the 0.7 V applied in the long-hand solution of Example 2.9. The voltage across R_1 is 10 V $-$ 218.8 mV $\cong$ 9.78 V, compared to 9.74 V in the long-hand solution. The voltage across the resistor R_2 is 5 V $-$ 421.6 mV $\cong$ 4.58 V, compared to 4.56 V in Example 2.9.

To understand the differences between the two solutions, one must be aware that the diode has internal characteristics that affect its behavior such as the reverse saturation current and its resistance levels at different current levels. Those characteristics can be viewed through the sequence **Edit-PSpice Model** resulting in the **PSpice Model Editor Demo** dialog box.

You will find that the default value of the reverse saturation current is 2.682 nA—a quantity that can have an important effect on the characteristics of the device. If we choose I_s = 3.5E-15A (a value determined by trial and error) and delete the other parameters for the device, a new simulation of the network will result in the response of Fig. 2.147. Now the current through the circuit is 2.072 mA, which is an exact match with the result of Example 2.9. The voltage across the diode is 260.2 mV + 440.9 mV ≅ 0.701 V, or essentially 0.7 V, and the voltage across each resistor is exactly as obtained in the long-hand solution. In other words, by choosing this value of reverse saturation current, we created a diode with characteristics that permitted the approximation that $V_D = 0.7$ V when in the "on" state.

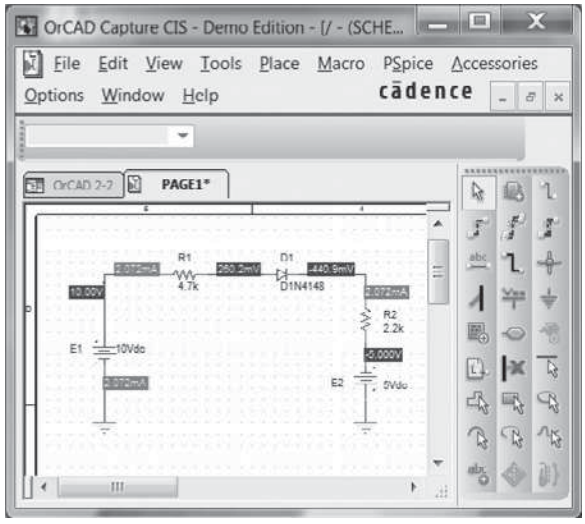


FIG. 2.147

The circuit of Fig. 2.146 reexamined with I_s set at 3.5E-15A.

The results can also be viewed in tabulated form by selecting **PSpice** at the head of the screen followed by **View Output File**. The result is the listing of Fig. 2.148 (modified to conserve space), which includes the **CIRCUIT DESCRIPTION** with all the components of the network, the **Diode MODEL PARAMETERS** with the chosen **Is** value, and the **INITIAL TRANSIENT SOLUTION** with the dc voltage levels, current levels, and total power dissipation.

The analysis is now complete for the diode circuit of interest. Granted, there was a wealth of information provided to establish and investigate this rather simple network. However, the vast majority of this material will not be repeated in the PSpice examples to follow, which will have a dramatic effect on the length of the descriptions. For practice purposes, it is suggested that other examples in this chapter be checked using PSpice and that the exercises at the end of the chapter be investigated to develop confidence in applying the software package.

Diode Characteristics The characteristics of the D1N4148 diode used in the above analysis will now be obtained using a few maneuvers somewhat more sophisticated than those employed in the first example. The process begins by first building the network of Fig. 2.149 using the procedures just described. Note in particular that the source is labeled **E** and set at **0V** (its initial value). Next the **New Simulation Profile** icon is selected from the toolbar to obtain the **New Simulation** dialog box. For the **Name**, Fig. 2-150 is entered since it is the location of the graph to be obtained. **Create** is then selected and the **Simulation Settings** dialog box will appear. Under **Analysis Type**, **DC Sweep** is chosen because we want to sweep through a range of values for the source voltage. When **DC Sweep** is selected a list of options will simultaneously appear in the right-hand region of the dialog box, requiring that some choices be made. Since we plan to sweep through a range of voltages, the **Sweep variable** is a **Voltage source**. Its name must be entered as **E** as appearing in Fig. 2.149. The sweep will be **Linear** (equal space between data points) with a **Start value** of 0 V, **End Value** of 10 V, and an **Increment** of 0.01 V. After making all the entries, click **OK** and the

```
****     CIRCUIT DESCRIPTION

******************************************************************************

*Analysis directives:
.TRAN  0 1000ns 0
.PROBE V(alias(*)) I(alias(*))
 W(alias(*)) D(alias(*)) NOISE(alias(*))
.INC "..\SCHEMATIC1.net"

**** INCLUDING SCHEMATIC1.net ****
* source ORCAD2-2
V_E1        N00103 0 10Vdc
V_E2        0 N00099 5Vdc
R_R1        N00103 N00204  4.7k TC=0,0
R_R2        N00099 N00185  2.2k TC=0,0
D_D1        N00204 N00185 D1N4148

****     Diode MODEL PARAMETERS
******************************************************************************

           D1N4148
       IS  2.000000E-15

****    INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

******************************************************************************
NODE     VOLTAGE
(N00099)  -5.0000
(N00103)  10.0000
(N00185)  -.4455
(N00204)  .2700


VOLTAGE SOURCE CURRENTS

 NAME        CURRENT
  V_E1       -2.070E-03
  V_E2       -2.070E-03

TOTAL POWER DISSIPATION  3.11E–02  WATTS
```

FIG. 2.148

Output file for PSpice Windows analysis of the circuit of Fig. 2.147.

RUN PSpice option can be selected. The analysis will be performed with the source voltage changing from 0 V to 10 V in 1000 steps (as resulting from the division of 10 V/0.01 V). The result, however, is simply a graph with a horizontal scale from 0 V to 10 V.

Since the plot we want is of I_D versus V_D, we must change the horizontal (x-axis) to V_D. This is accomplished by selecting **Plot** and then **Axis Settings**. An **Axis Settings** dialog box will appear, in which choices have to be made. If **Axis Variables** is selected, an **X-Axis**

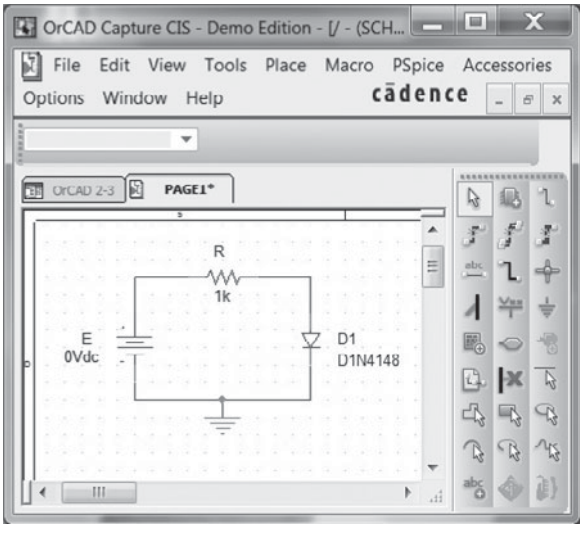


FIG. 2.149

Network for obtaining the characteristics of the D1N4148 diode.

Variable dialog box will appear with a list of variables that can be chosen for the *x*-axis. **V1(D1)** will be selected since it represents the voltage across the diode. If we then select **OK**, the **Axis Settings** dialog box will return, where **User Defined** is selected under the **Data Range** heading. **User Defined** is chosen because it will allow us to limit the graph to a range of 0 V to 1 V since the "on" voltage of the diode should be around 0.7 V. After entering the 0–1 V range, selecting **OK** will result in a graph with **V1(D1)** as the *x* variable with a range of 0 V to 1 V. The horizontal axis now seems to be set for the desired plot.

We must now turn our attention to the vertical axis, which should be the diode current. Choosing **Trace** followed by **Add Trace** will result in an **Add Trace** dialog box in which **I(D1)** will appear as one of the possibilities. Selecting **I(D1)** will also cause it to appear as the **Trace Expression** at the bottom of the dialog box. Selecting **OK** will then result in the diode characteristics of Fig. 2.150, clearly showing a steep rise around 0.7 V.

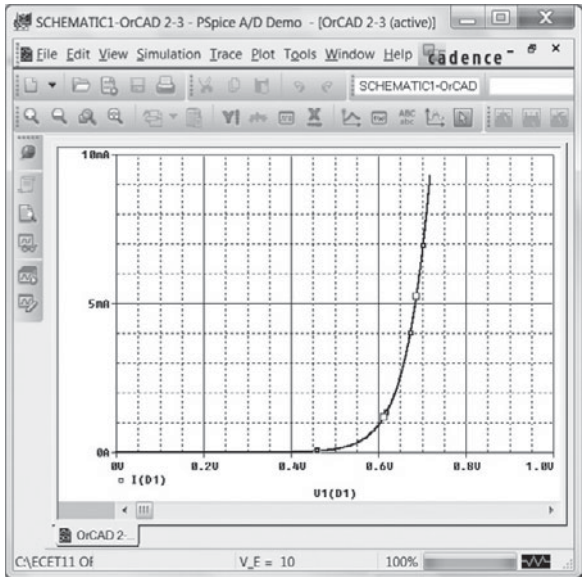


FIG. 2.150
Characteristics of the D1N4148 diode.

If we turn back to the **PSpice Model Editor** for the diode and change I_s to 3.5E-15A as in the previous example, the curve will shift to the right. Similar procedures will be used to obtain the characteristic curves for a variety of elements to be introduced in later chapters.

Multisim

Fortunately, there are a number of similarities between Cadence OrCAD and Multisim. Then again, there are a number of differences also, but the saving point is that once you become proficient in the use of one software package, the other will be much easier to learn. For those users familiar with the earlier versions of Multisim, you will find that the new version has a minimum of changes, permitting an easy transition to the new procedures.

Once the Multisim icon is chosen, a screen will appear with a vast array of toolbars. The content of each and the name of each can be found through the sequence **View-toolbars**. The result is a long vertical list of available toolbars. The content and location of each can be found by simply selecting or deleting a toolbar and noting the effect on the full screen. For our purposes the **Standard, View, Main, Components, Simulation Switch, Simulation and Instruments** will be used.

When using Multisim you have a choice between using "virtual" or "real" components. Virtual components are those that can be given any value when you build the network. The term *real* comes from the fact that the resulting list is a list of standard component values that can be purchased from a supplier. Finding a component is initiated by first selecting the second keypad (from the left) on the component toolbar that looks like a resistor. As you approach the key, the label **Place Basic** will appear. Once it is chosen, the **Select a**

Component dialog box will appear that contains a subset titled **Family**. Third down on that list is a **RATED_VIRTUAL** option with a resistor symbol. When this is selected a list of components including **RESISTOR_RATED, CAPACITOR_RATED, INDUCTOR_RATED**, and a variety of others will appear. If **RESISTOR-RATED** is selected, a resistor symbol will appear under the Symbol heading. Note that the resistor docs not have a specific value. If we now select **OK** and place it on the screen in much the same way we did for the OrCAD introduction, you will find that the value was automatically labeled **R1** with a value of 1 kΩ. In order to place another resistor the same sequence must be followed, but this time the resistor will automatically be called **R2** but with the same value of 1 kΩ. This labeling process will continue in the same manner with the same 1-kΩ value for as many resistors as you place. As was done with OrCAD, the resistor labels and values can be changed quite easily. Of course, if the chosen resistor is a standard value then it can be found directly under the **RESISTOR** listing of "real" components.

We are now ready to build the diode network of Example 2.13 so we can compare results. The diodes chosen will be commercially available under the "real" listing. In this case two **1N4009** diodes were found by first selecting the keypad **Place Diode** to the right of the **Place Basic** keypad to obtain the **Select a Component** dialog box. Then the sequence **Family-DIODE-1N4009–OK** will result in a diode on the screen labeled **D1** with **1N4009** below the symbol, as shown in Fig. 2.151. Next we can place the resistors on the screen by going to the **RESISTOR** option and typing in the value of one of the resistors, in this case, the 3.3-kΩ resistor in the area provided at the top of the resistor listing. This certainly removes the need to scroll through the list looking for a particular resistor. Once found and placed, it will appear as **R1** with a value of 3.3 kΩ. The same procedure will result in a second resistor called **R2** with a value of 5.6 kΩ. In each case the elements are initially placed closest to where they will end up. The dc voltage source is found by going to the **Place Source** keypad, which is the first keypad in the **Component** toolbar. Under Family, **POWER SOURCES** is selected, followed by **DC_POWER**. Click **OK** and a voltage source will appear on the screen with the label **V1** at a level of **12 V**. The last circuit element to be set on the screen is the ground, which is accomplished by going back to the **Place Source** option and, after selecting **POWER SOURCES**, choosing "ground" under the **Component** listing. Click **OK** and the ground can be placed anywhere on the screen.

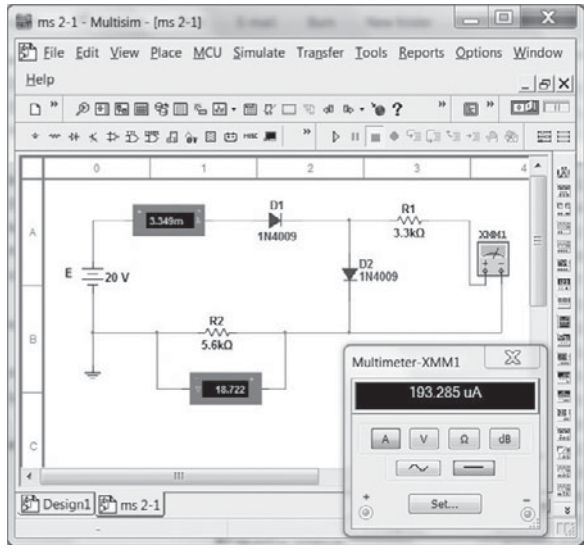


FIG. 2.151
Verifying the results of Example 2.13 using Multisim.

Now that all the components are on the screen, they must be placed and labeled properly. For each component, simply selecting the device will create a blue dashed box around it to indicate it is in the active mode. When clicked to establish this condition, it can be moved to any location on the screen. To rotate an element, establish the active mode and apply **Crtl-R** to rotate it 90 degrees. Each application of this process will rotate it an additional 90 degrees. Changing a label simply requires double-clicking the label of interest to create

a small blue box around it and produce a dialog box for the change. For the source, a dialog box labeled **DC_POWER** will result, in which the heading **Label** is selected and the **refDEs** retyped as **E**. Click **OK** and the label **E** will appear. The same procedure can change the value to 20 V, although in this case the **Value** heading is chosen and the units are chosen using the scroll at the right of the entered value.

The next step is to determine what quantities are to be measured and how to measure them. For this network a multimeter will be used to measure the current through the resistor **R1**. The multimeter is found at the top of the **Instrument** toolbar. After selection it can be placed on the screen in the same manner as the other elements. Double-clicking the meter will then result in the **Multimeter-XXM1** dialog box, in which **A** is selected to set the multimeter as an ammeter. In addition, the **DC** box (a straight line) must be selected because we are dealing with dc voltages. The current through the diode **D1** and the voltage across the resistor **R2** will be found using **Indicators**, which are found as the tenth option to the right on the **Component** toolbar. The software symbol looks like an LED with a red dashed figure eight inside. Click on this option and a **Select a Component** dialog box will appear. Under **Family**, select **AMMETER** and then take note of the **Component** listing and the four options for the orientation of the indicator. For our analysis the **AMMETER_H** will be chosen since the plus sign or entering point for the current is on the left for the diode **D1**. Click **OK** and the indicator can be placed to the left of the diode **D1**. For the voltage across the resistor **R2**, the option **VOLTMETER_HR** is chosen so the polarity matches that across the resistor.

Finally, all the components and meters must be connected. This is accomplished by simply placing the cursor at the end of an element until a small circle and a set of crosshairs appear to designate the starting point. Once these are in place, click the location and an **x** will appear at the terminal. Then move to the end of the other element and left-click the mouse again—a red connecting wire will automatically appear with the most direct route between the two elements. The process is called **Automatic Wiring**.

Now that all the components are in place it is time to initiate the analysis of the circuit, an operation that can be performed in one of three ways. One option is to select **Simulate** at the head of the screen followed by **Run**. The next is the green arrow in the **Simulation** toolbar. The last is to simply toggle the switch at the head of the screen to the **1** position. In each case a solution appears in the indicators after a few seconds that seems to flicker over time. This flickering simply indicates the software package is repeating the analysis over time. To accept the solution and stop the continuing simulation, either toggle the switch to the **0** position or select the lightning bolt keypad again.

The current through the diode is 3.349 mA, which compares well with the 3.32 mA in Example 2.13. The voltage across the resistor R_2 is 18.722 V, which is close to the 18.6 V of the same example. After the simulation, the multimeter can be displayed as shown in Fig. 2.151 by double-clicking on the meter symbol. By clicking anywhere on the meter, the top portion is dark blue, and the meter can be moved to any location by simply clicking on the blue region and dragging it to the desired location. The current of 193.285 μA is very close to the 212 μA of Example 2.13. The differences are primarily due to the fact that each diode voltage is assumed to be 0.7 V, whereas in fact it is different for each diode of Fig. 2.151 since the current through each is different. In all, however, the Multisim solution is a very close match with the approximate solution of Example 2.13.

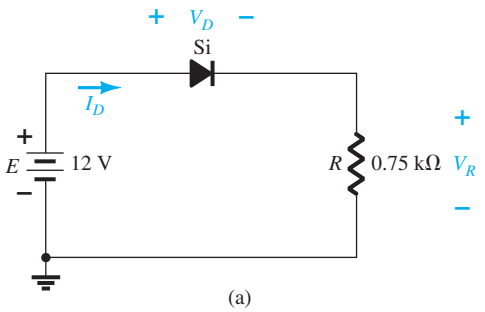
PROBLEMS

**Note:* Asterisks indicate more difficult problems.

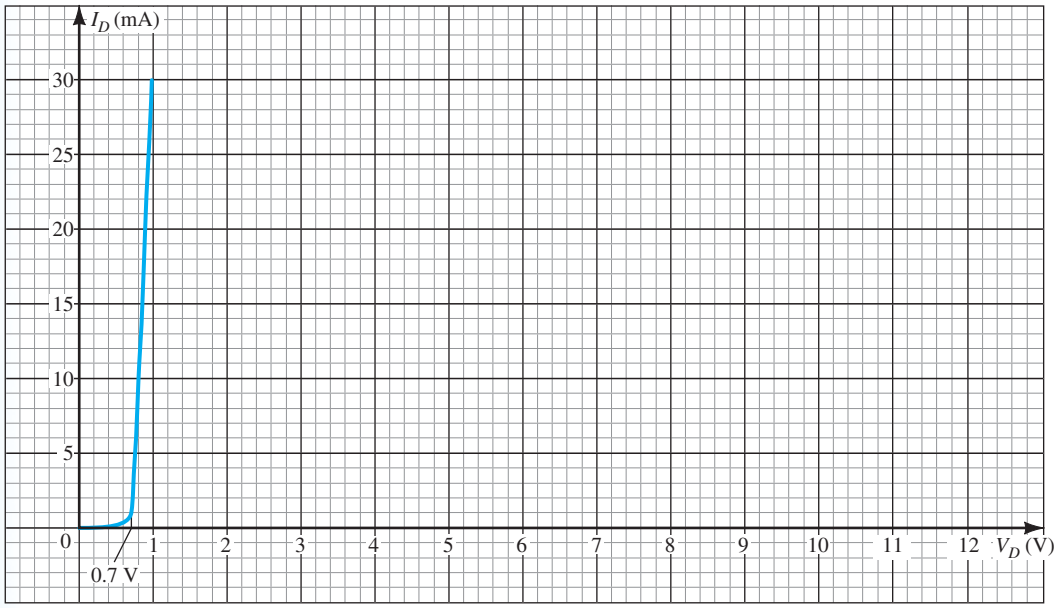
2.2 Load-Line Analysis

1. **a.** Using the characteristics of Fig. 2.152b, determine I_D, V_D, and V_R for the circuit of Fig. 2.152a.
   b. Repeat part (a) using the approximate model for the diode, and compare results.
   c. Repeat part (a) using the ideal model for the diode, and compare results.
2. **a.** Using the characteristics of Fig. 2.152b, determine I_D and V_D for the circuit of Fig. 2.153.
   b. Repeat part (a) with $R = 0.47\ \text{k}\Omega$.
   c. Repeat part (a) with $R = 0.68\ \text{k}\Omega$.
   d. Is the level of V_D relatively close to 0.7 V in each case?

How do the resulting levels of I_D compare? Comment accordingly.



(a)



(b)

FIG. 2.152
Problems 1 and 2.

3. Determine the value of R for the circuit of Fig. 2.153 that will result in a diode current of 10 mA if $E = 7$ V. Use the characteristics of Fig. 2.152b for the diode.

4. **a.** Using the approximate characteristics for the Si diode, determine V_D, I_D, and V_R for the circuit of Fig. 2.154.
b. Perform the same analysis as part (a) using the ideal model for the diode.
c. Do the results obtained in parts (a) and (b) suggest that the ideal model can provide a good approximation for the actual response under some conditions?

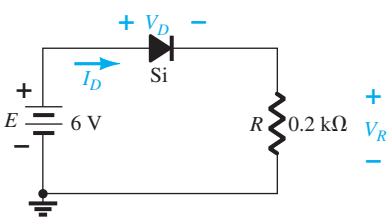


FIG. 2.153
Problems 2 and 3.

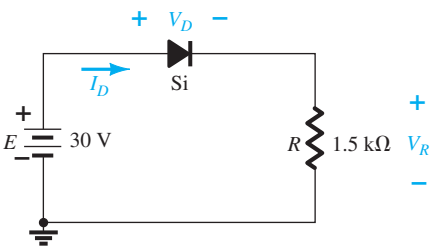


FIG. 2.154
Problem 4.

5. Determine the current I for each of the configurations of Fig. 2.155 using the approximate equivalent model for the diode.

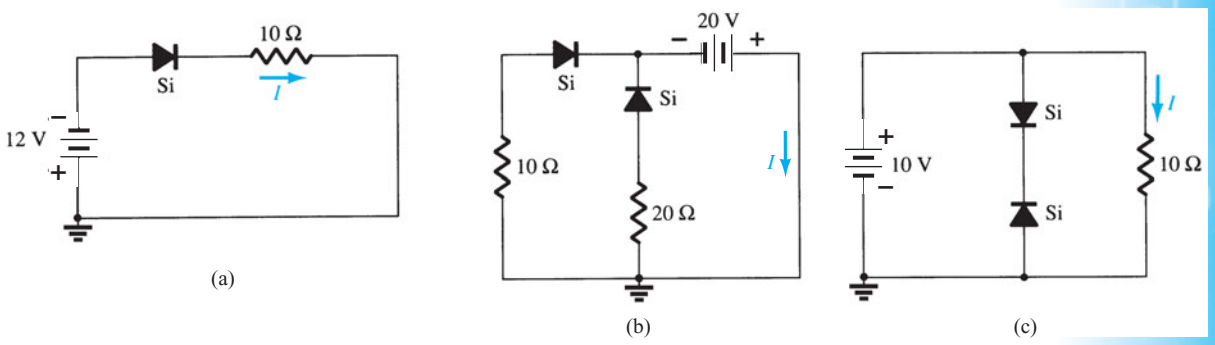


FIG. 2.155
Problem 5.

6. Determine V_o and I_D for the networks of Fig. 2.156.

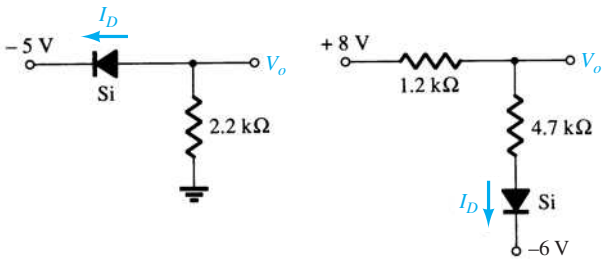


FIG. 2.156
Problems 6 and 49.

***7.** Determine the level of V_o for each network of Fig. 2.157.

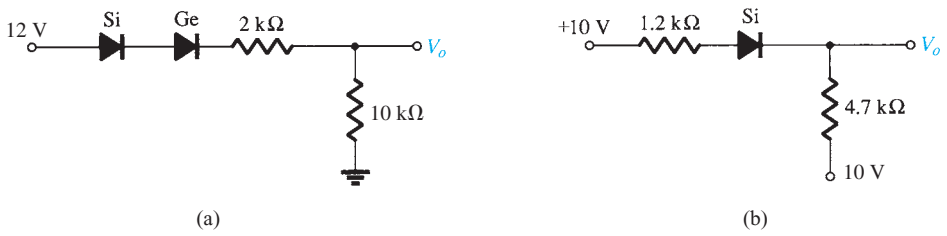


FIG. 2.157
Problem 7.

***8.** Determine V_o and I_D for the networks of Fig. 2.158.

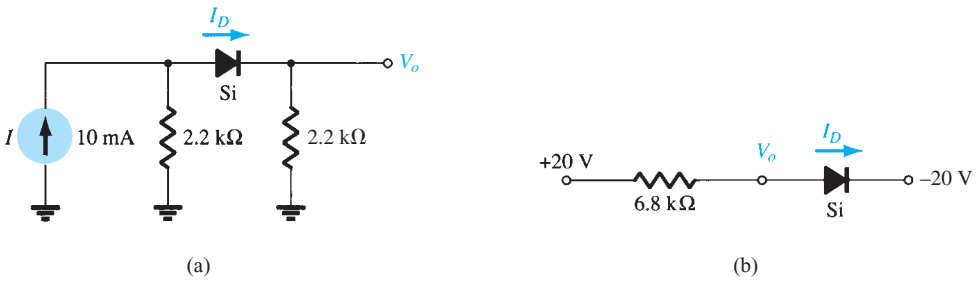


FIG. 2.158
Problem 8.

*9. Determine V_{o_1} and V_{o_2} for the networks of Fig. 2.159.

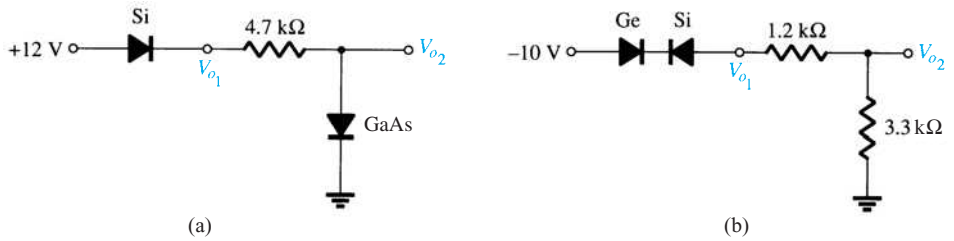


FIG. 2.159
Problem 9.

2.4 Parallel and Series–Parallel Configurations

10. Determine V_o and I_D for the networks of Fig. 2.160.

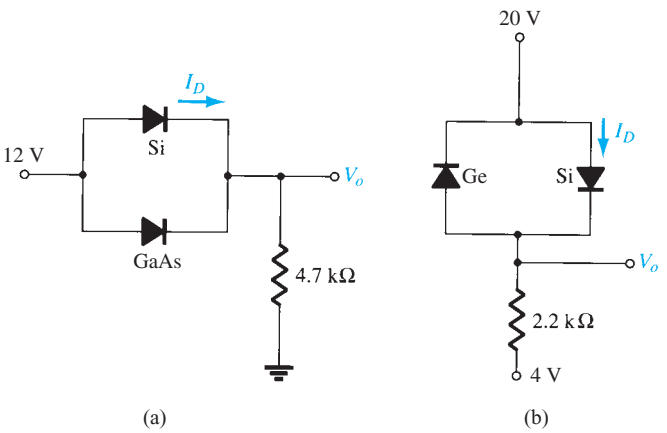


FIG. 2.160
Problems 10 and 50.

*11. Determine V_o and I for the networks of Fig. 2.161.

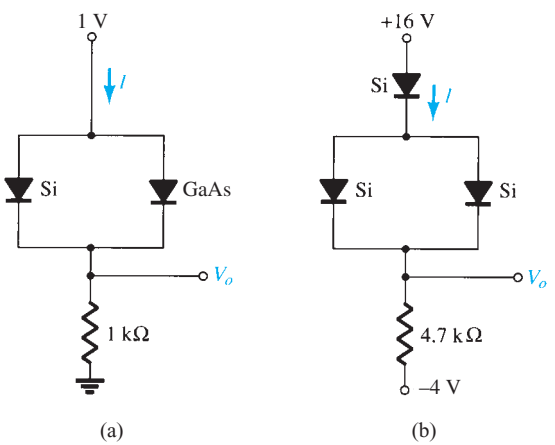


FIG. 2.161
Problem 11.

12. Determine V_{o_1}, V_{o_2}, and I for the network of Fig. 2.162.

*13. Determine V_o and I_D for the network of Fig. 2.163.

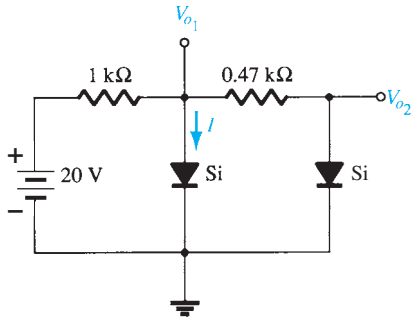


FIG. 2.162
Problem 12.

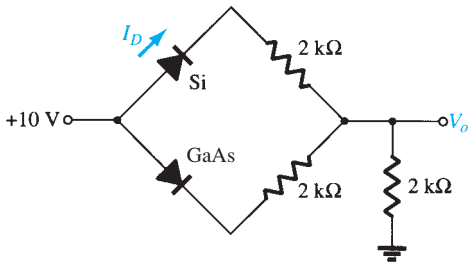


FIG. 2.163
Problems 13 and 51.

2.5 AND/OR Gates

14. Determine V_o for the network of Fig. 2.39 with 0 V on both inputs.

15. Determine V_o for the network of Fig. 2.39 with 10 V on both inputs.

16. Determine V_o for the network of Fig. 2.42 with 0 V on both inputs.

17. Determine V_o for the network of Fig. 2.42 with 10 V on both inputs.

18. Determine V_o for the negative logic OR gate of Fig. 2.164.

19. Determine V_o for the negative logic AND gate of Fig. 2.165.

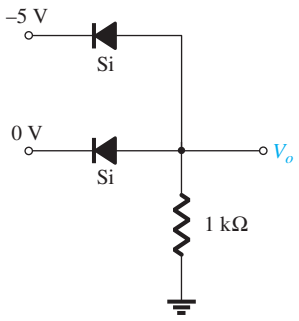


FIG. 2.164
Problem 18.

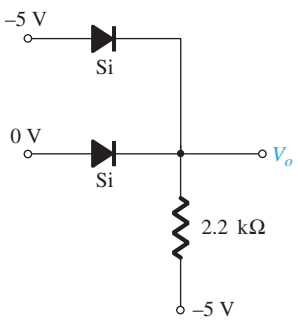


FIG. 2.165
Problem 19.

20. Determine the level of V_o for the gate of Fig. 2.166.

21. Determine V_o for the configuration of Fig. 2.167.

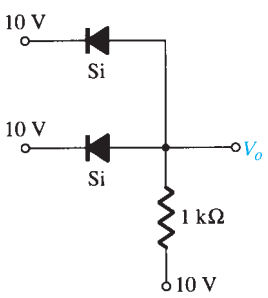


FIG. 2.166
Problem 20.

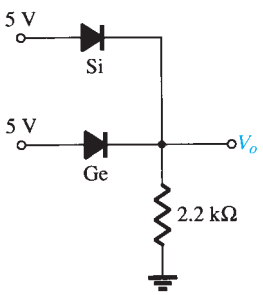


FIG. 2.167
Problem 21.

2.6 Sinusoidal Inputs; Half-Wave Rectification

22. Assuming an ideal diode, sketch v_i, v_d, and i_d for the half-wave rectifier of Fig. 2.168. The input is a sinusoidal waveform with a frequency of 60 Hz. Determine the profit value of v_i from the given dc level.

23. Repeat Problem 22 with a silicon diode ($V_K = 0.7$ V).

24. Repeat Problem 22 with a 10 kΩ load applied as shown in Fig. 2.169. Sketch v_L and i_L.

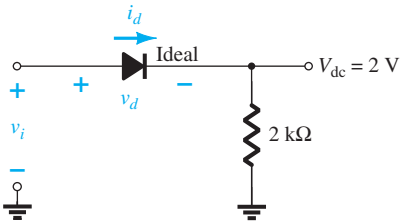


FIG. 2.168
Problems 22 through 24.

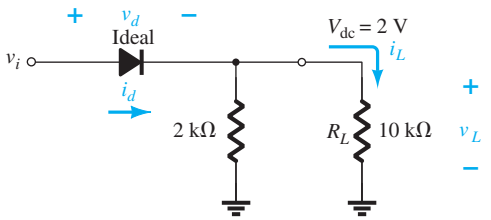


FIG. 2.169
Problem 24.

25. For the network of Fig. 2.170, sketch v_o and determine V_{dc}.

***26.** For the network of Fig. 2.171, sketch v_o and i_R.

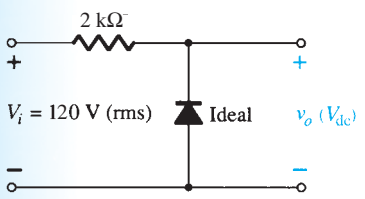


FIG. 2.170
Problem 25.

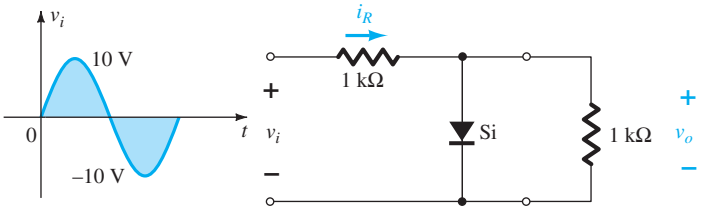


FIG. 2.171
Problem 26.

***27.** **a.** Given $P_{max} = 14$ mW for each diode at Fig. 2.172, determine the maximum current rating of each diode (using the approximate equivalent model).
b. Determine I_{max} for the parallel diodes.
c. Determine the current through each diode at $V_{i_{max}}$ using the results of part (b).
d. If only one diode were present, which would be the expected result?

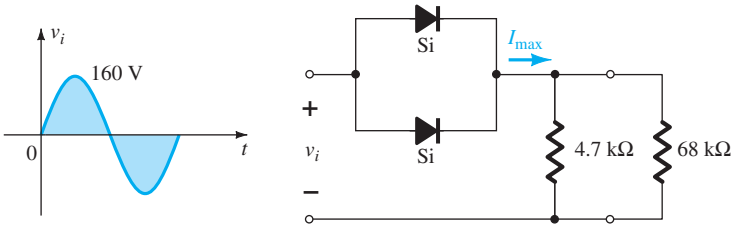


FIG. 2.172
Problem 27.

2.7 Full-Wave Rectification

28. A full-wave bridge rectifier with a 120-V rms sinusoidal input has a load resistor of 1 kΩ.
a. If silicon diodes are employed, what is the dc voltage available at the load?
b. Determine the required PIV rating of each diode.
c. Find the maximum current through each diode during conduction.
d. What is the required power rating of each diode?

29. Determine v_o and the required PIV rating of each diode for the configuration of Fig. 2.173. In addition, determine the maximum current through each diode.

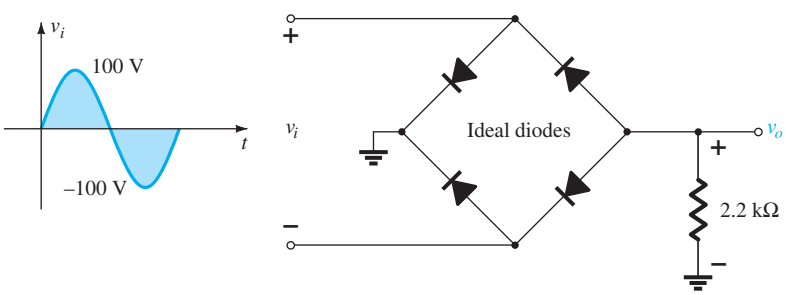


FIG. 2.173
Problem 29.

*30. Sketch v_o for the network of Fig. 2.174 and determine the dc voltage available.

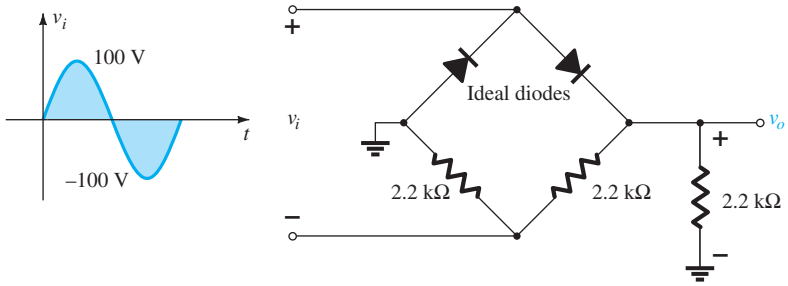


FIG. 2.174
Problem 30.

*31. Sketch v_o for the network of Fig. 2.175 and determine the dc voltage available.

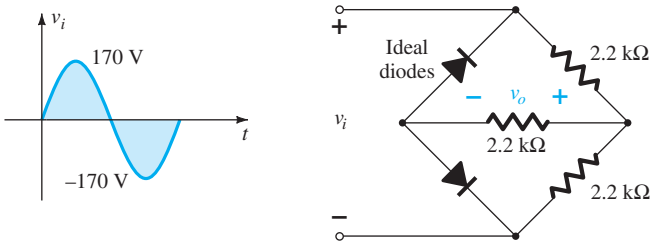


FIG. 2.175
Problem 31.

2.8 Clippers

32. Determine v_o for each network of Fig. 2.176 for the input shown.

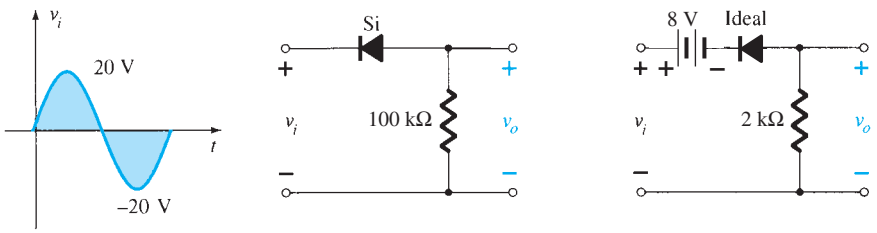


FIG. 2.176
Problem 32.

33. Determine v_o for each network of Fig. 2.177 for the input shown.

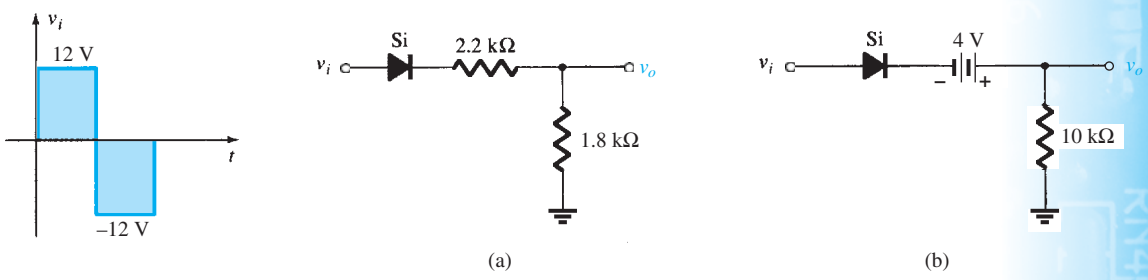


FIG. 2.177
Problem 33.

*34. Determine v_o for each network of Fig. 2.178 for the input shown.

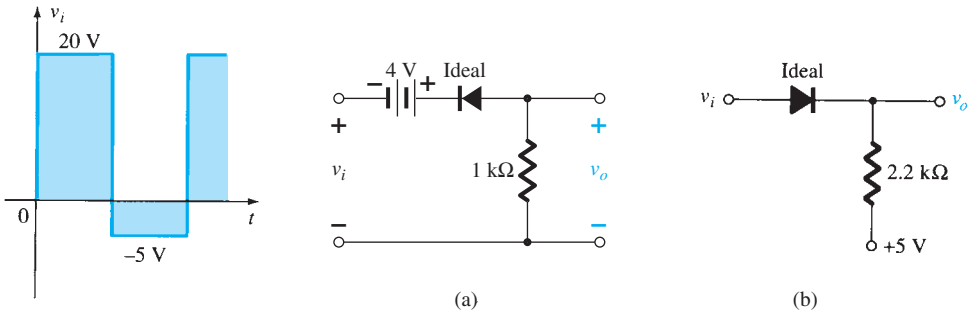


FIG. 2.178
Problem 34.

*35. Determine v_o for each network of Fig. 2.179 for the input shown.

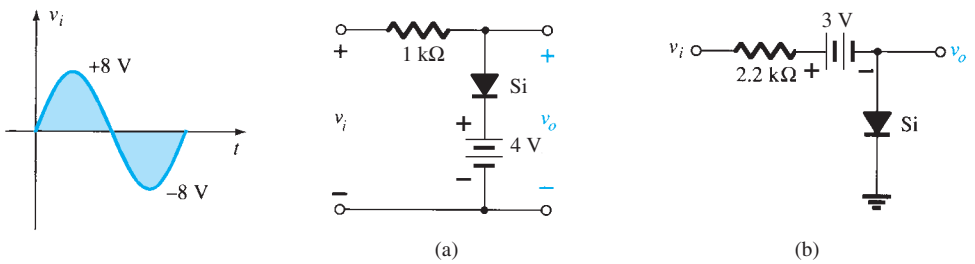


FIG. 2.179
Problem 35.

36. Sketch i_R and v_o for the network of Fig. 2.180 for the input shown.

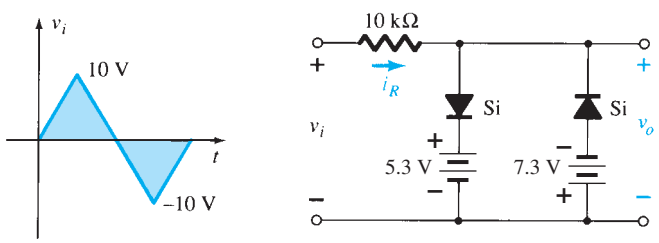


FIG. 2.180
Problem 36.

2.9 Clampers

37. Sketch v_o for each network of Fig. 2.181 for the input shown.

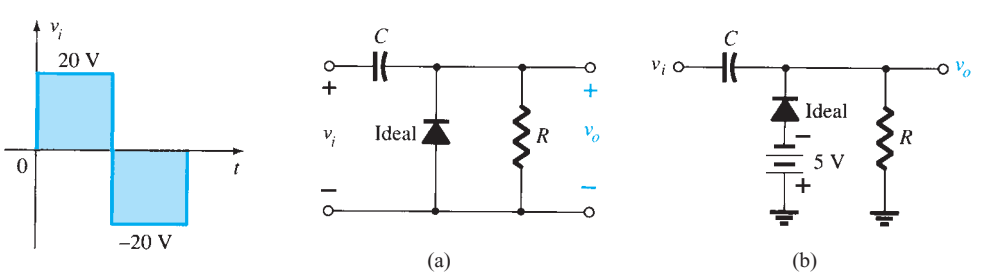


FIG. 2.181
Problem 37.

38. Sketch v_o for each network of Fig. 2.182 for the input shown.

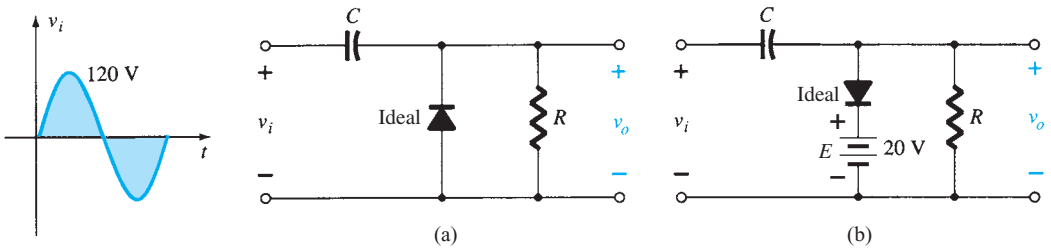


FIG. 2.182
Problem 38.

***39.** For the network of Fig. 2.183:

a. Calculate 5τ.

b. Compare 5τ to half the period of the applied signal.

c. Sketch v_o.

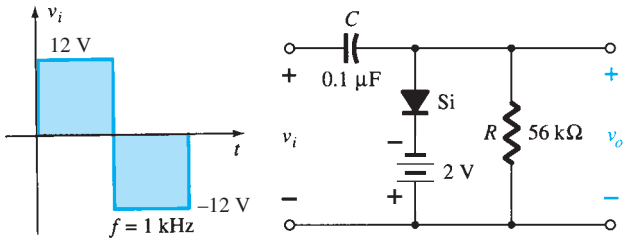


FIG. 2.183
Problem 39.

***40.** Design a clamper to perform the function indicated in Fig. 2.184.

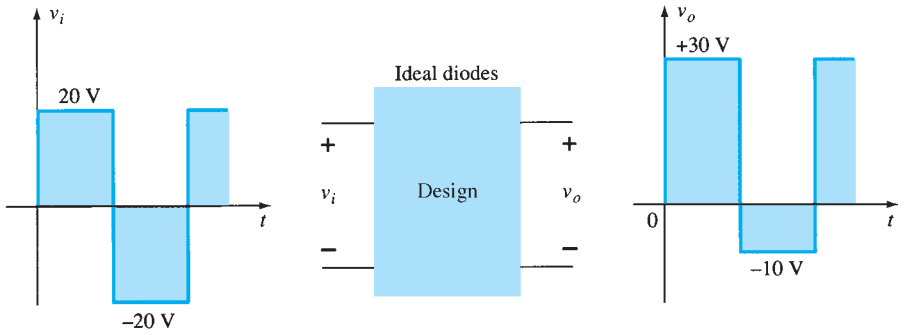


FIG. 2.184
Problem 40.

***41.** Design a clamper to perform the function indicated in Fig. 2.185.

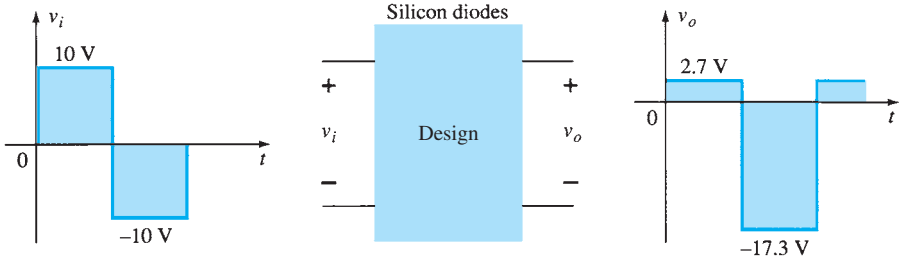


FIG. 2.185
Problem 41.

2.10 Zener Diodes

*42. **a.** Determine V_L, I_L, I_Z, and I_R for the network of Fig. 2.186 if $R_L = 180\ \Omega$.
b. Repeat part (a) if $R_L = 470\ \Omega$.
c. Determine the value of R_L that will establish maximum power conditions for the Zener diode.
d. Determine the minimum value of R_L to ensure that the Zener diode is in the "on" state.

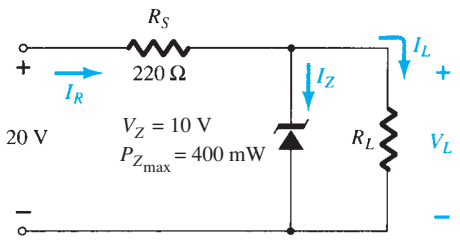


FIG. 2.186
Problem 42.

*43. **a.** Design the network of Fig. 2.187 to maintain V_L at 12 V for a load variation (I_L) from 0 mA to 200 mA. That is, determine R_S and V_Z.
b. Determine $P_{Z\ max}$ for the Zener diode of part (a).

*44. For the network of Fig. 2.188, determine the range of V_i that will maintain V_L at 8 V and not exceed the maximum power rating of the Zener diode.

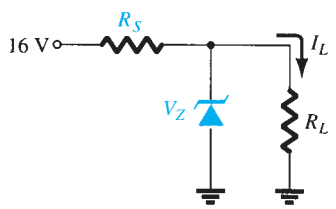


FIG. 2.187
Problem 43.

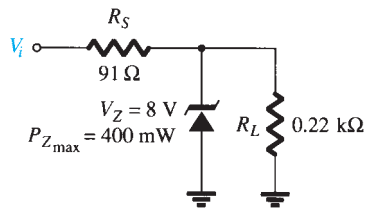


FIG. 2.188
Problems 44 and 52.

45. Design a voltage regulator that will maintain an output voltage of 20 V across a 1-kΩ load with an input that will vary between 30 V and 50 V. That is, determine the proper value of R_S and the maximum current I_{ZM}.

46. Sketch the output of the network of Fig. 2.145 if the input is a 50-V square wave. Repeat for a 5-V square wave.

2.11 Voltage-Multiplier Circuits

47. Determine the voltage available from the voltage doubler of Fig. 2.123 if the secondary voltage of the transformer is 120 V (rms).

48. Determine the required PIV ratings of the diodes of Fig. 2.123 in terms of the peak secondary voltage V_m.

2.14 Computer Analysis

49. Perform an analysis of the network of Fig. 2.156b using PSpice Windows.

50. Perform an analysis of the network of Fig. 2.161b using PSpice Windows.

51. Perform an analysis of the network of Fig. 2.162 using PSpice Windows.

52. Perform a general analysis of the Zener network of Fig. 2.188 using PSpice Windows.

53. Repeat Problem 49 using Multisim.

54. Repeat Problem 50 using Multisim.

55. Repeat Problem 51 using Multisim.

56. Repeat Problem 52 using Multisim.