6 Field-Effect Transistors

CHAPTER OBJECTIVES

- Become familiar with the construction and operating characteristics of Junction Field Effect (JFET), Metal-Oxide Semiconductor FET (MOSFET), and Metal-Semiconductor FET (MESFET) transistors.
- Be able to sketch the transfer characteristics from the drain characteristics of a JFET, MOSFET, and MESFET transistor.
- Understand the vast amount of information provided on the specification sheet for each type of FET.
- Be aware of the differences between the dc analysis of the various types of FETs.

6.1 INTRODUCTION

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor described in Chapters 3 through 5. Although there are important differences between the two types of devices, there are also many similarities, which will be pointed out in the sections to follow.

The primary difference between the two types of transistors is the fact that:

The BJT transistor is a current-controlled device as depicted in Fig. 6.1a, whereas the JFET transistor is a voltage-controlled device as shown in Fig. 6.1b.

In other words, the current I_C in Fig. 6.1a is a direct function of the level of I_B. For the FET the current I_D will be a function of the voltage V_{GS} applied to the input circuit as shown in Fig. 6.1b. In each case the current of the output circuit is controlled by a parameter of the input circuit—in one case a current level and in the other an applied voltage.

Just as there are *npn* and *pnp* bipolar transistors, there are *n-channel* and *p-channel* field-effect transistors. However, it is important to keep in mind that the BJT transistor is a *bipolar* device—the prefix *bi* indicates that the conduction level is a function of two charge carriers, electrons and holes. The FET is a *unipolar* device depending solely on either electron (*n*-channel) or hole (*p*-channel) conduction.

The term *field effect* in the name deserves some explanation. We are all familiar with the ability of a permanent magnet to draw metal filings to itself without the need for actual contact. The magnetic field of the permanent magnet envelopes the filings and attracts them to the magnet along the shortest path provided by the magnetic flux lines. For the FET an *electric field* is established by the charges present, which controls the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

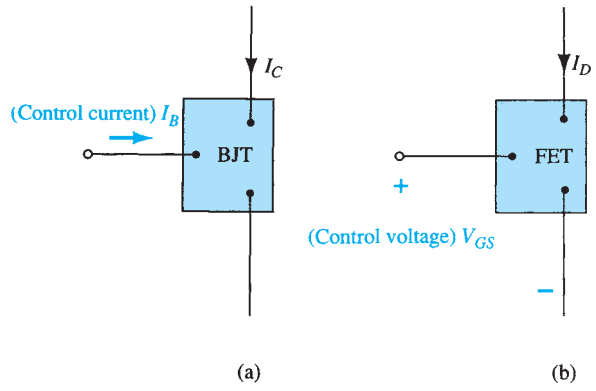


FIG. 6.1
(a) Current-controlled and (b) voltage-controlled amplifiers.

There is a natural tendency when introducing a device with a range of applications similar to one already introduced to compare some of the general characteristics of one to those of the other:

One of the most important characteristics of the FET is its high input impedance.

At a level of 1 MΩ to several hundred megohms it far exceeds the typical input resistance levels of the BJT transistor configurations—a very important characteristic in the design of linear ac amplifier systems. On the other hand, the BJT transistor has a much higher sensitivity to changes in the applied signal. In other words, the variation in output current is typically a great deal more for BJTs than for FETs for the same change in the applied voltage.

For this reason:

Typical ac voltage gains for BJT amplifiers are a great deal more than for FETs.

However,

FETs are more temperature stable than BJTs, and FETs are usually smaller than BJTs, making them particularly useful in integrated-circuit (IC) chips.

The construction characteristics of some FETs, however, can make them more sensitive to handling than BJTs.

Three types of FETs are introduced in this chapter: the *junction field-effect transistor* (JFET), *the metal–oxide–semiconductor field-effect transistor* (MOSFET), and the *metal–semiconductor field-effect transistor* (MESFET). The MOSFET category is further broken down into *depletion* and *enhancement* types, which are both described. The MOSFET transistor has become one of the most important devices used in the design and construction of integrated circuits for digital computers. Its thermal stability and other general characteristics make it extremely popular in computer circuit design. However, as a discrete element in a typical top-hat container, it must be handled with care (to be discussed in a later section). The MESFET is a more recent development and takes full advantage of the high-speed characteristics of GaAs as the base semiconductor material. Although currently the more expensive option, the cost issue is often outweighed by the need for higher speeds in RF and computer designs.

Once the FET construction and characteristics have been introduced, the biasing arrangements will be covered in Chapter 7. The analysis performed in Chapter 4 using BJT transistors will prove helpful in the derivation of the important equations and understanding the results obtained for FET circuits.

Ian Munro Ross and G. C. Dacey (Fig. 6.2) were instrumental in the early stages of development of the field-effect transistor. Take particular note of the equipment used in 1955 for their research.

Drs. Ian Munro Ross (front) and G. C. Dacey jointly developed an experimental procedure for measuring the characteristics of a field-effect transistor in 1955.

Dr. Ross Born: Southport, England; PhD, Gonville and Caius College, Cambridge University; President Emeritus, AT&T Bell Labs; Fellow, IEEE; Member, the National Science Board; Chairman, National Advisory Committee on Semiconductors

Dr. Dacey Born: Chicago, Illinois; PhD, California Institute of Technology; Director of Solid-State Electronics Research, Bell Labs; Vice President, Research, Sandia Corporation; Member IRE, Tau Beta Pi, Eta Kappa Nu

FIG. 6.2
Early development of the field-effect transistor.
(Courtesy of AT&T Archives and History Center.)

6.2 CONSTRUCTION AND CHARACTERISTICS OF JFETs

As indicated earlier, the JFET is a three-terminal device with one terminal capable of controlling the current between the other two. In our discussion of the BJT transistor the *npn* transistor was employed through the major part of the analysis and design sections, with a

section devoted to the effect of using a *pnp* transistor. For the JFET transistor the *n*-channel device will be the prominent device, with paragraphs and sections devoted to the effect of using a *p*-channel JFET.

The basic construction of the *n*-channel JFET is shown in Fig. 6.3. Note that the major part of the structure is the *n*-type material, which forms the channel between the embedded layers of *p*-type material. The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the *drain (D)*, whereas the lower end of the same material is connected through an ohmic contact to a terminal referred to as the *source (S)*. The two *p*-type materials are connected together and to the *gate (G)* terminal. In essence, therefore, the drain and the source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material. In the absence of any applied potentials the JFET has two *p–n* junctions under no-bias conditions. The result is a depletion region at each junction, as shown in Fig. 6.3, that resembles the same region of a diode under no-bias conditions. Recall also that a depletion region is void of free carriers and is therefore unable to support conduction.

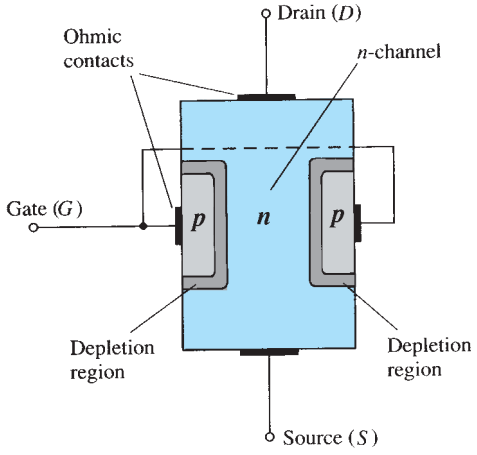


FIG. 6.3
Junction field-effect transistor (JFET).

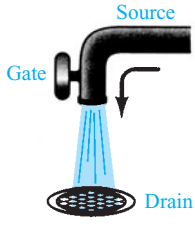


FIG. 6.4
Water analogy for the JFET control mechanism.

Analogies are seldom perfect and at times can be misleading, but the water analogy of Fig. 6.4 does provide a sense for the JFET control at the gate terminal and the appropriateness of the terminology applied to the terminals of the device. The source of water pressure can be likened to the applied voltage from drain to source, which establishes a flow of water (electrons) from the spigot (source). The "gate," through an applied signal (potential), controls the flow of water (charge) to the "drain." The drain and source terminals are at opposite ends of the *n*-channel as introduced in Fig. 6.3 because the terminology is defined for electron flow.

$V_{GS} = 0$ V, V_{DS} Some Positive Value

In Fig. 6.5, a positive voltage V_{DS} is applied across the channel and the gate is connected directly to the source to establish the condition $V_{GS} = 0$ V. The result is a gate and a source terminal at the same potential and a depletion region in the low end of each *p*-material similar to the distribution of the no-bias conditions of Fig. 6.3. The instant the voltage V_{DD} ($=V_{DS}$) is applied, the electrons are drawn to the drain terminal, establishing the conventional current I_D with the defined direction of Fig. 6.5. The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D = I_S$). Under the conditions in Fig. 6.5, the flow of charge is relatively uninhibited and is limited solely by the resistance of the *n*-channel between drain and source.

It is important to note that the depletion region is wider near the top of both *p*-type materials. The reason for the change in width of the region is best described through the help of Fig. 6.6. Assuming a uniform resistance in the *n*-channel, we can break down

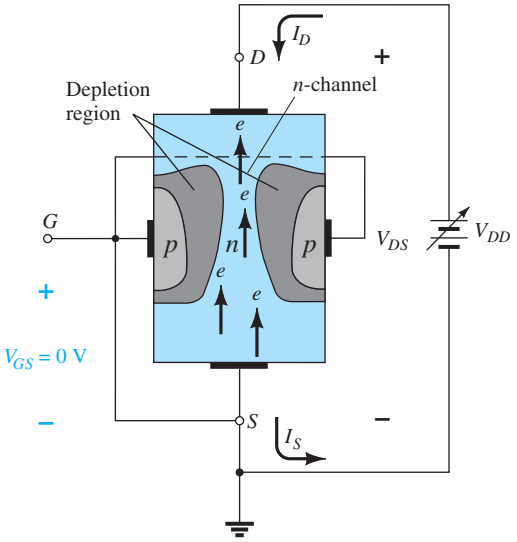


FIG. 6.5
JFET at $V_{GS} = 0$ V and $V_{DS} > 0$ V.

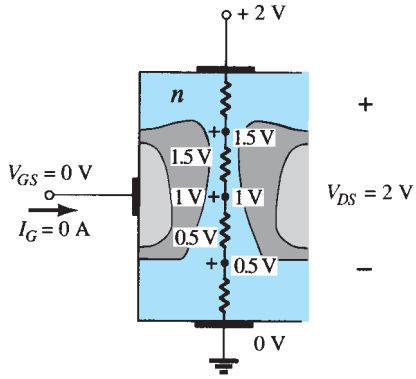


FIG. 6.6
Varying reverse-bias potentials across the p–n junction of an n-channel JFET.

the resistance of the channel into the divisions appearing in Fig. 6.6. The current I_D will establish the voltage levels through the channel as indicated on the same figure. The result is that the upper region of the *p*-type material will be reverse-biased by about 1.5 V, with the lower region only reverse-biased by 0.5 V. Recall from the discussion of the diode operation that the greater the applied reverse bias, the wider is the depletion region—hence the distribution of the depletion region as shown in Fig. 6.6. The fact that the *p–n* junction is reverse-biased for the length of the channel results in a gate current of zero amperes, as shown in the same figure. The fact that $I_G = 0$ A is an important characteristic of the JFET.

As the voltage V_{DS} is increased from 0 V to a few volts, the current will increase as determined by Ohm's law and the plot of I_D versus V_{DS} will appear as shown in Fig. 6.7. The relative straightness of the plot reveals that for the region of low values of V_{DS}, the resistance is essentially constant. As V_{DS} increases and approaches a level referred to as V_P in Fig. 6.7, the depletion regions of Fig. 6.5 will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the curve in the graph of Fig. 6.7 to occur. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region. If V_{DS} is increased to a level where it appears that the two depletion regions would

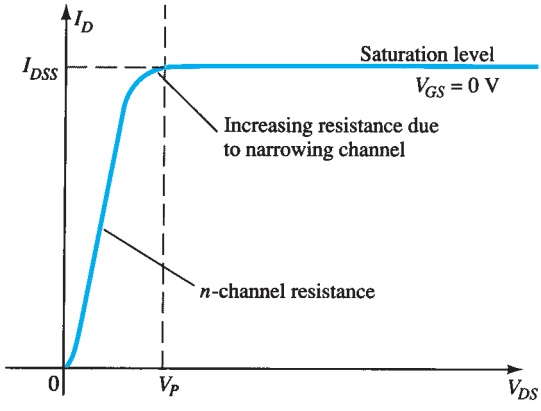


FIG. 6.7
I_D versus V_{DS} for $V_{GS} = 0$ V.

"touch" as shown in Fig. 6.8, a condition referred to as *pinch-off* will result. The level of V_{DS} that establishes this condition is referred to as the *pinch-off voltage* and is denoted by V_P, as shown in Fig. 6.7. In actuality, the term *pinch-off* is a misnomer in that it suggests the current I_D is pinched off and drops to 0 A. As shown in Fig. 6.7, however, this is hardly the case— I_D maintains a saturation level defined as I_{DSS} in Fig. 6.7. In reality a very small channel still exists, with a current of very high density. The fact that I_D does not drop off at pinch-off and maintains the saturation level indicated in Fig. 6.7 is verified by the following fact: The absence of a drain current would remove the possibility of different potential levels through the *n*-channel material to establish the varying levels of reverse bias along the *p*–*n* junction. The result would be a loss of the depletion region distribution that caused pinch-off in the first place.

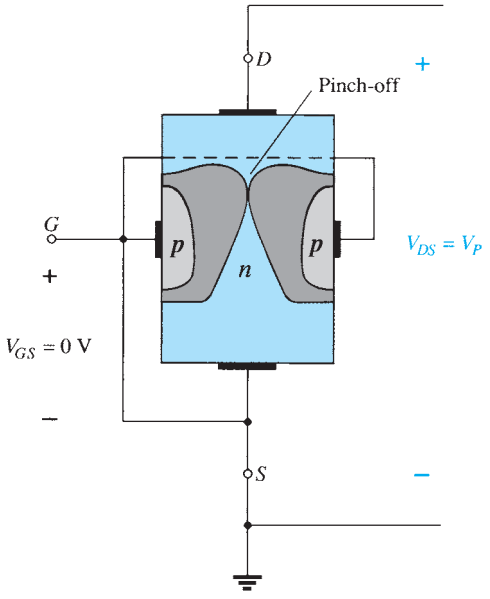


FIG. 6.8
Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).

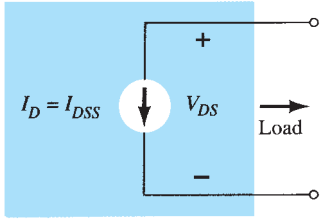


FIG. 6.9
Current source equivalent for $V_{GS} = 0$ V, $V_{DS} > V_P$.

As V_{DS} is increased beyond V_P, the region of close encounter between the two depletion regions increases in length along the channel, but the level of I_D remains essentially the same. In essence, therefore, once $V_{DS} > V_P$ the JFET has the characteristics of a current source. As shown in Fig. 6.9, the current is fixed at $I_D = I_{DSS}$, but the voltage V_{DS} (for levels $> V_P$) is determined by the applied load.

The choice of notation I_{DSS} is derived from the fact that it is the *d*rain-to-*s*ource current with a *s*hort-circuit connection from gate to source. As we continue to investigate the characteristics of the device we will find that:

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$ V and $V_{DS} > |V_P|$.

Note in Fig. 6.7 that $V_{GS} = 0$ V for the entire length of the curve. The next few paragraphs will describe how the characteristics of Fig. 6.7 are affected by changes in the level of V_{GS}.

$V_{GS} < 0$ V

The voltage from gate to source, denoted V_{GS}, is the controlling voltage of the JFET. Just as various curves for I_C versus V_{CE} were established for different levels of I_B for the BJT transistor, curves of I_D versus V_{DS} for various levels of V_{GS} can be developed for the JFET. For the *n*-channel device the controlling voltage V_{GS} is made more and more negative from its $V_{GS} = 0$ V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source.

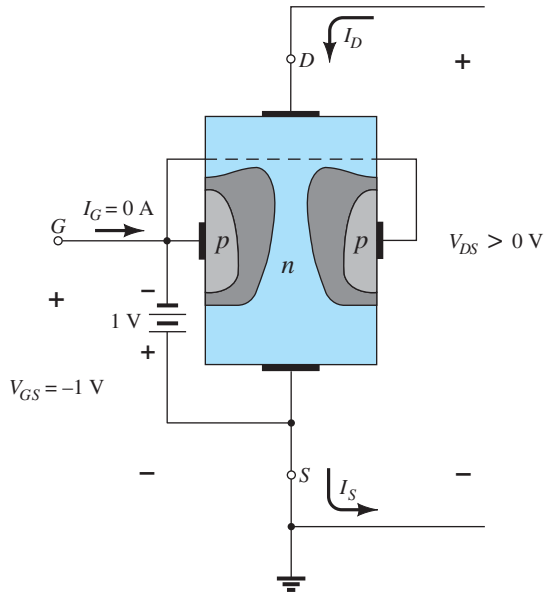


FIG. 6.10
Application of a negative voltage to the gate of a JFET.

In Fig. 6.10 a negative voltage of −1 V is applied between the gate and source terminals for a low level of V_{DS}. The effect of the applied negative-bias V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0$ V, but at lower levels of V_{DS}. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS}, as shown in Fig. 6.11 for $V_{GS} = -1$ V. The resulting saturation level for I_D has been reduced and in fact will continue to decrease as V_{GS} is made more and more negative. Note also in Fig. 6.11 how the pinch-off voltage continues to drop in a parabolic manner as V_{GS} becomes more and more negative. Eventually, V_{GS} when $V_{GS} = -V_P$ will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been "turned off." In summary:

The level of V_{GS} that results in $I_D = 0$ mA is defined by $V_{GS} = V_P$, with V_P being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

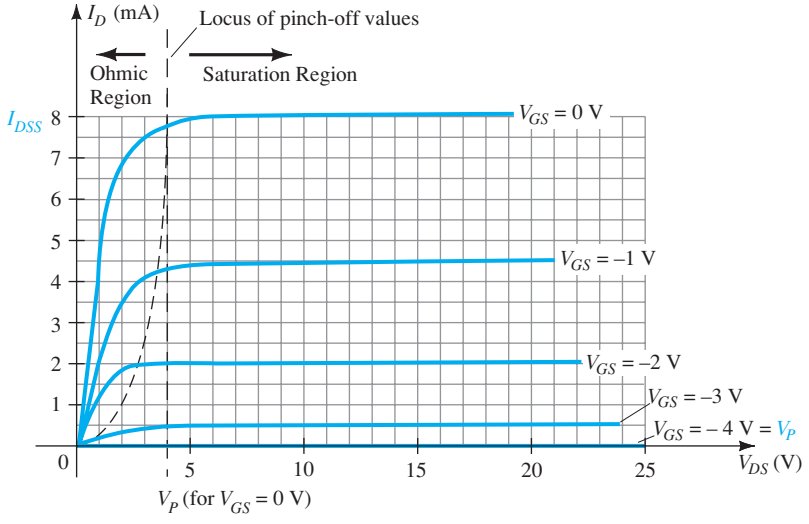


FIG. 6.11
n-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.

On most specification sheets the pinch-off voltage is specified as $V_{GS(off)}$ rather than V_P. A specification sheet will be reviewed later in the chapter when the majority of the controlling elements have been introduced. The region to the right of the pinch-off locus of Fig. 6.11 is the region typically employed in linear amplifiers (amplifiers with minimum distortion of the applied signal) and is commonly referred to as the *constant-current, saturation,* or *linear amplification region.*

Voltage-Controlled Resistor

The region to the left of the pinch-off locus of Fig. 6.11 is referred to as the *ohmic* or *voltage-controlled resistance region.* In this region the JFET can actually be employed as a variable resistor (possibly for an automatic gain control system) whose resistance is controlled by the applied gate-to-source voltage. Note in Fig. 6.11 that the slope of each curve and therefore the resistance of the device between drain and source for $V_{DS} < V_P$ are a function of the applied voltage V_{GS}. As V_{GS} becomes more and more negative, the slope of each curve becomes more and more horizontal, corresponding to an increasing resistance level. The following equation provides a good first approximation to the resistance level in terms of the applied voltage V_{GS}:

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2} \tag{6.1}$$

where r_o is the resistance with $V_{GS} = 0$ V and r_d is the resistance at a particular level of V_{GS}.

For an *n*-channel JFET with $r_o = 10\,\text{k}\Omega$ ($V_{GS} = 0$ V, $V_P = -6$ V), Eq. (6.1) results in 40 kΩ at $V_{GS} = -3$ V.

p-Channel Devices

The *p*-channel JFET is constructed in exactly the same manner as the *n*-channel device of Fig. 6.3 but with a reversal of the *p*- and *n*-type materials as shown in Fig. 6.12. The defined current directions are reversed, as are the actual polarities for the voltages V_{GS} and V_{DS}. For the *p*-channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for V_{DS} will result in negative voltages for V_{DS} on the characteristics of Fig. 6.13, which has an I_{DSS} of 6 mA and a pinch-off voltage of $V_{GS} = +6$ V. Do not let the minus signs for V_{DS} confuse you. They simply indicate that the source is at a higher potential than the drain.

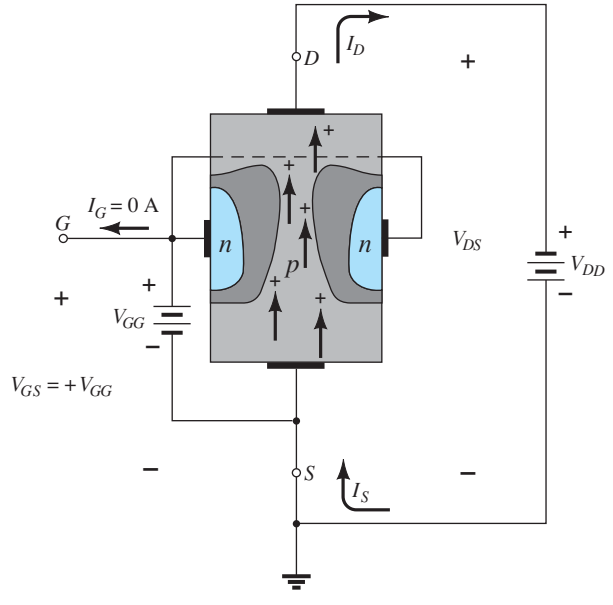


FIG. 6.12
p-Channel JFET.

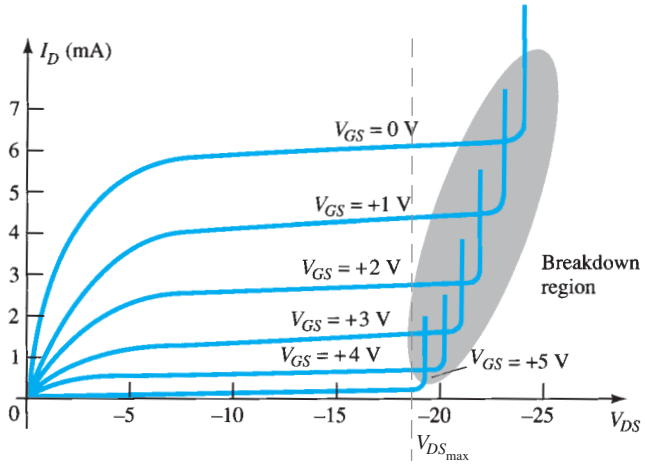


FIG. 6.13
p-Channel JFET characteristics with $I_{DSS} = 6$ mA and $V_P = +6$ V.

Note at high levels of V_{DS} that the curves suddenly rise to levels that seem unbounded. The vertical rise is an indication that breakdown has occurred and the current through the channel (in the same direction as normally encountered) is now limited solely by the external circuit. Although not appearing in Fig. 6.11 for the *n*-channel device, they do occur for the *n*-channel device if sufficient voltage is applied. This region can be avoided if the level of $V_{DS_{max}}$ is noted on the specification sheet and the design is such that the actual level of V_{DS} is less than this value for *all* values of V_{GS}.

Symbols

The graphic symbols for the *n*-channel and *p*-channel JFETs are provided in Fig. 6.14. Note that the arrow is pointing in for the *n*-channel device of Fig. 6.14a to represent the direction in which I_G would flow if the *p*–*n* junction were forward-biased. For the *p*-channel device (Fig. 6.14b) the only difference in the symbol is the direction of the arrow in the symbol.

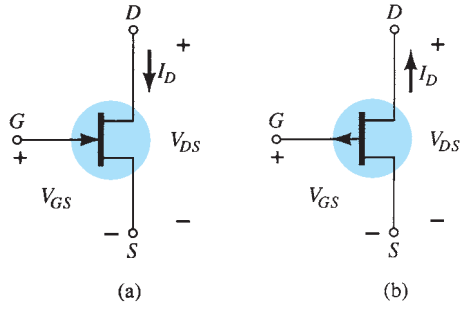


FIG. 6.14
JFET symbols: (a) n-channel; (b) p-channel.

Summary

A number of important parameters and relationships were introduced in this section. A few that will surface frequently in the analysis to follow in this chapter and the next for *n*-channel JFETs include the following:

The maximum current is defined as I_{DSS} and occurs when $V_{GS} = 0$ V and $V_{DS} \geq |V_P|$, as shown in Fig. 6.15a.

For gate-to-source voltages V_{GS} is less than (more negative than) the pinch-off level, the drain current is 0 A ($I_D = 0$ A), as in Fig. 6.15b.

For all levels of V_{GS} between 0 V and the pinch-off level, the current I_D will range between I_{DSS} and 0 A, respectively, as in Fig. 6.15c.

A similar list can be developed for p-channel JFETs.

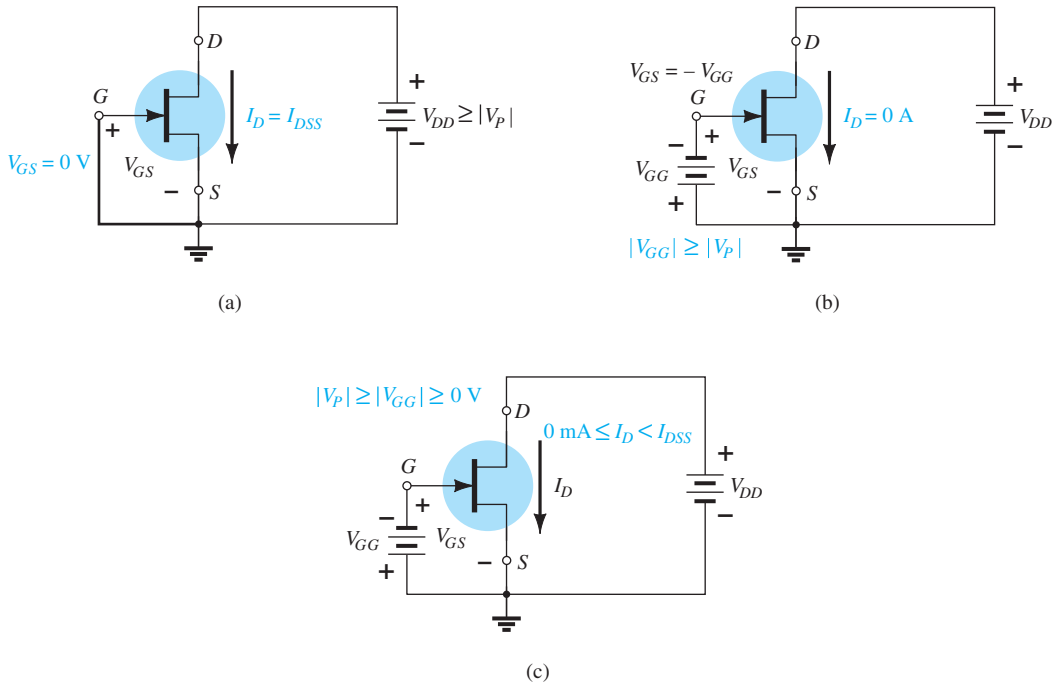


FIG. 6.15

(a) $V_{GS} = 0$ V, $I_D = I_{DSS}$; (b) cutoff ($I_D = 0$ A) V_{GS} less than the pinch-off level; (c) I_D is between 0 A and I_{DSS} for $V_{GS} \leq 0$ V and greater than the pinch-off level.

6.3 TRANSFER CHARACTERISTICS

Derivation

For the BJT transistor the output current I_C and the input controlling current I_B are related by beta, which was considered constant for the analysis to be performed. In equation form,

$$I_C = f(I_B) = \beta I_B \qquad \text{(6.2)}$$

(control variable: I_B; constant: β)

In Eq. (6.2) a linear relationship exists between I_C and I_B. Double the level of I_B and I_C will increase by a factor of two also.

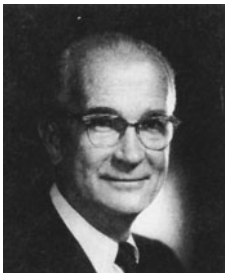
Unfortunately, this linear relationship does not exist between the output and input quantities of a JFET. The relationship between I_D and V_{GS} is defined by *Shockley's equation* (see Fig. 6.16):

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad \text{(6.3)}$$

(control variable: V_{GS}; constants: I_{DSS}, V_P)

The squared term in the equation results in a nonlinear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitude of V_{GS}.

For the dc analysis to be performed in Chapter 7, a graphical rather than a mathematical approach will in general be more direct and easier to apply. The graphical approach, however, will require a plot of Eq. (6.3) to represent the device and a plot of the network equation relating the same variables. The solution is defined by the point of intersection of the two curves. It is important to keep in mind when applying the graphical approach that the device characteristics will be *unaffected* by the network in which the device is employed.



William Bradford Shockley (1910–1989), co-inventor of the first transistor and formulator of the "field-effect" theory employed in the development of the transistor and the FET.

Shockley Born: London, England; PhD, Harvard, 1936; Head, Transistor Physics Department, Bell Laboratories; President, Shockley Transistor Corp.; Poniatoff Professor of Engineering Science, Stanford University; Nobel Prize in physics in 1956 with Walter Brattain and John Bardeen

FIG. 6.16

Dr. William Bradford Shockley. (Courtesy of AT&T Archives and History Center.)

The network equation may change along with the intersection between the two curves, but the transfer curve defined by Eq. (6.3) is unaffected. In general, therefore:

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

The transfer curve can be obtained using Shockley's equation or from the output characteristics of Fig. 6.11. In Fig. 6.17 two graphs are provided, with the vertical scaling in milliamperes for each graph. One is a plot of I_D versus V_{DS}, whereas the other is I_D versus V_{GS}. Using the drain characteristics on the right of the "y" axis, we can draw a horizontal line from the saturation region of the curve denoted $V_{GS} = 0$ V to the I_D axis. The resulting current level for both graphs is I_{DSS}. The point of intersection on the I_D versus V_{GS} curve will be as shown since the vertical axis is defined as $V_{GS} = 0$ V.

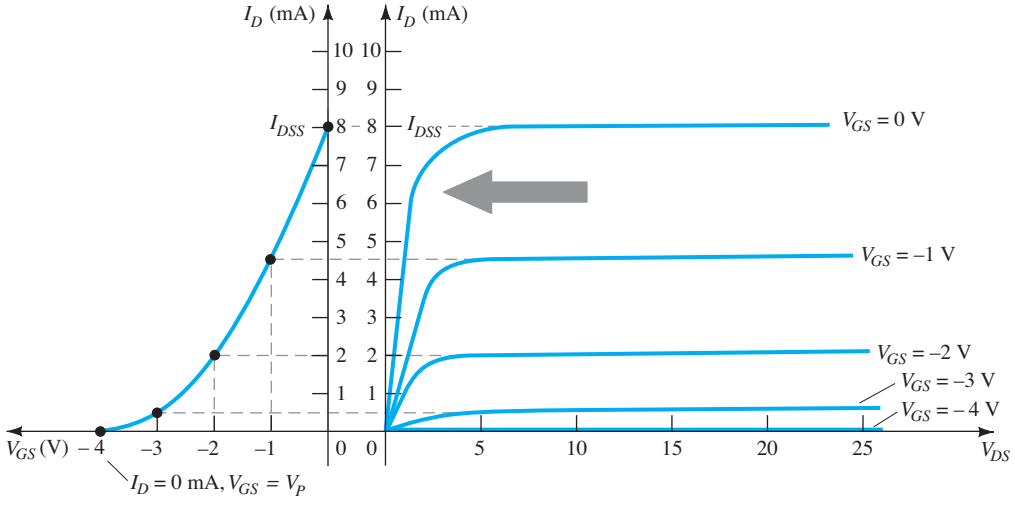


FIG. 6.17
Obtaining the transfer curve from the drain characteristics.

In review:

$$\boxed{\text{When } V_{GS} = 0 \text{ V}, \quad I_D = I_{DSS}} \tag{6.4}$$

When $V_{GS} = V_P = -4$ V, the drain current is 0 mA, defining another point on the transfer curve. That is:

$$\boxed{\text{When } V_{GS} = V_P, \quad I_D = 0 \text{ mA}} \tag{6.5}$$

Before continuing, it is important to realize that the drain characteristics relate one output (or drain) quantity to another output (or drain) quantity—both axes are defined by variables in the same region of the device characteristics. The transfer characteristics are a plot of an output (or drain) current versus an input-controlling quantity. There is therefore a direct "transfer" from input to output variables when employing the curve to the left of Fig. 6.17. If the relationship were linear, the plot of I_D versus V_{GS} would result in a straight line between I_{DSS} and V_P. However, a parabolic curve will result because the vertical spacing between steps of V_{GS} on the drain characteristics of Fig. 6.17 decreases noticeably as V_{GS} becomes more and more negative. Compare the spacing between $V_{GS} = 0$ V and $V_{GS} = -1$ V to that between $V_{GS} = -3$ V and pinch-off. The change in V_{GS} is the same, but the resulting change in I_D is quite different.

If a horizontal line is drawn from the $V_{GS} = -1$ V curve to the I_D axis and then extended to the other axis, another point on the transfer curve can be located. Note that $V_{GS} = -1$ V on the bottom axis of the transfer curve with $I_D = 4.5$ mA. Note in the definition of I_D at $V_{GS} = 0$ V and -1 V that the saturation levels of I_D are employed and the ohmic region ignored. Continuing with $V_{GS} = -2$ V and -3 V, we can complete the transfer curve. It is

the transfer curve of I_D versus V_{GS} that will receive extended use in the analysis of Chapter 7 and not the drain characteristics of Fig. 6.17. The next few paragraphs will introduce a quick, efficient method of plotting I_D versus V_{GS} given only the levels of I_{DSS} and V_P and Shockley's equation.

Applying Shockley's Equation

The transfer curve of Fig. 6.17 can also be obtained directly from Shockley's equation (6.3) given simply the values of I_{DSS} and V_P. The levels of I_{DSS} and V_P define the limits of the curve on both axes and leave only the necessity of finding a few intermediate plot points. The validity of Eq. (6.3) as a source of the transfer curve of Fig. 6.17 is best demonstrated by examining a few specific levels of one variable and finding the resulting level of the other as follows:

Substituting $V_{GS} = 0$ V gives

$$\text{Eq. (6.3):} \quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= I_{DSS}\left(1 - \frac{0}{V_P}\right)^2 = I_{DSS}(1 - 0)^2$$

and

$$\boxed{I_D = I_{DSS}\,|_{V_{GS}=0\text{ V}}} \tag{6.6}$$

Substituting $V_{GS} = V_P$ yields

$$I_D = I_{DSS}\left(1 - \frac{V_P}{V_P}\right)^2$$
$$= I_{DSS}(1 - 1)^2 = I_{DSS}(0)$$

$$\boxed{I_D = 0\text{ A}\,|_{V_{GS}=V_P}} \tag{6.7}$$

For the drain characteristics of Fig. 6.17, if we substitute $V_{GS} = -1$ V,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= 8\text{ mA}\left(1 - \frac{-1\text{ V}}{-4\text{ V}}\right)^2 = 8\text{ mA}\left(1 - \frac{1}{4}\right)^2 = 8\text{ mA}\,(0.75)^2$$
$$= 8\text{ mA}\,(0.5625)$$
$$= \mathbf{4.5\text{ mA}}$$

as shown in Fig. 6.17. Note the care taken with the negative signs for V_{GS} and V_P in the calculations above. The loss of one sign would result in a totally erroneous result.

It should be obvious from the above that given I_{DSS} and V_P (as is normally provided on specification sheets), the level of I_D can be found for any level of V_{GS}. Conversely, by using basic algebra we can obtain [from Eq. (6.3)] an equation for the resulting level of V_{GS} for a given level of I_D. The derivation is quite straightforward and results in

$$\boxed{V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)} \tag{6.8}$$

Let us test Eq. (6.8) by finding the level of V_{GS} that will result in a drain current of 4.5 mA for the device with the characteristics of Fig. 6.17. We find

$$V_{GS} = -4\text{ V}\left(1 - \sqrt{\frac{4.5\text{ mA}}{8\text{ mA}}}\right)$$
$$= -4\text{ V}(1 - \sqrt{0.5625}) = -4\text{ V}(1 - 0.75)$$
$$= -4\text{ V}(0.25)$$
$$= \mathbf{-1\text{ V}}$$

as substituted in the above calculation and verified by Fig. 6.17.

Shorthand Method

Since the transfer curve must be plotted so frequently, it would be quite advantageous to have a shorthand method for plotting the curve in the quickest, most efficient manner while maintaining an acceptable degree of accuracy. The format of Eq. (6.3) is such that specific levels of V_{GS} will result in levels of I_D that can be memorized to provide the plot points needed to sketch the transfer curve. If we specify V_{GS} to be one-half the pinch-off value V_P, the resulting level of I_D will be the following, as determined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= I_{DSS}\left(\frac{1 - V_P/2}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{1}{2}\right)^2 = I_{DSS}(0.5)^2$$
$$= I_{DSS}(0.25)$$

and

$$\boxed{I_D = \frac{I_{DSS}}{4}\Big|_{V_{GS} = V_P/2}} \tag{6.9}$$

Now it is important to realize that Eq. (6.9) is not for a particular level of V_P. It is a general equation for any level of V_P as long as $V_{GS} = V_P/2$. The result specifies that the drain current will always be one-fourth the saturation level I_{DSS} as long as the gate-to-source voltage is one-half the pinch-off value. Note the level of I_D for $V_{GS} = V_P/2 = -4\text{ V}/2 = -2\text{ V}$ in Fig. 6.17.

If we choose $I_D = I_{DSS}/2$ and substitute into Eq. (6.8), we find that

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$
$$= V_P\left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right) = V_P(1 - \sqrt{0.5}) = V_P(0.293)$$

and

$$\boxed{V_{GS} \cong 0.3V_P\big|_{I_D = I_{DSS}/2}} \tag{6.10}$$

Additional points can be determined, but the transfer curve can be sketched to a satisfactory level of accuracy simply using the four plot points defined above and reviewed in Table 6.1. In fact, in the analysis of Chapter 7, a maximum of four plot points are used to sketch the transfer curves. On most occasions using just the plot point defined by $V_{GS} = V_P/2$ and the axis intersections at I_{DSS} and V_P will provide a curve accurate enough for most calculations.

TABLE 6.1
V_{GS} versus I_D Using Shockley's Equation

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0 mA

EXAMPLE 6.1 Sketch the transfer curve defined by $I_{DSS} = 12\text{ mA}$ and $V_P = -6\text{ V}$.

Solution: Two plot points are defined by

$$I_{DSS} = \mathbf{12\text{ mA}} \quad \text{and} \quad V_{GS} = \mathbf{0\text{ V}}$$

and

$$I_D = \mathbf{0\text{ mA}} \quad \text{and} \quad V_{GS} = \boldsymbol{V_P}$$

At $V_{GS} = V_P/2 = -6\text{ V}/2 = \mathbf{-3\text{ V}}$ the drain current is determined by $I_D = I_{DSS}/4 = 12\text{ mA}/4 = \mathbf{3\text{ mA}}$. At $I_D = I_{DSS}/2 = 12\text{ mA}/2 = \mathbf{6\text{ mA}}$ the gate-to-source voltage is determined by $V_{GS} \cong 0.3V_P = 0.3(-6\text{ V}) = \mathbf{-1.8\text{ V}}$. All four plot points are well defined on Fig. 6.18 with the complete transfer curve.

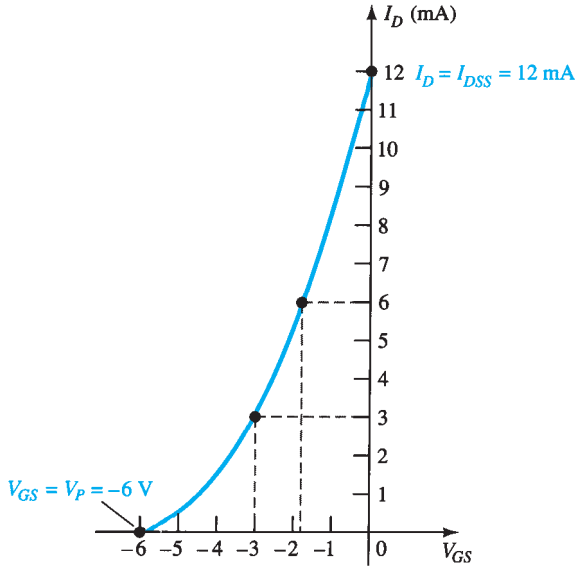


FIG. 6.18
Transfer curve for Example 6.1.

For *p*-channel devices Shockley's equation (6.3) can still be applied exactly as it appears. In this case, both V_P and V_{GS} will be positive and the curve will be the mirror image of the transfer curve obtained with an *n*-channel and the same limiting values.

EXAMPLE 6.2 Sketch the transfer curve for a *p*-channel device with $I_{DSS} = 4$ mA and $V_P = 3$ V.

Solution: At $V_{GS} = V_P/2 = 3\text{ V}/2 = \mathbf{1.5\ V}$, $I_D = I_{DSS}/4 = 4\text{ mA}/4 = \mathbf{1\ mA}$. At $I_D = I_{DSS}/2 = 4\text{ mA}/2 = \mathbf{2\ mA}$, $V_{GS} = 0.3V_P = 0.3(3\text{ V}) = \mathbf{0.9\ V}$. Both plot points appear in Fig. 6.19 along with the points defined by I_{DSS} and V_P.

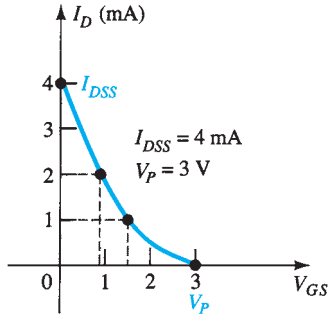


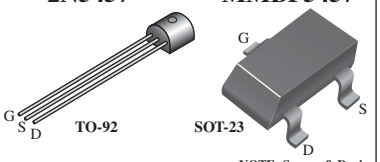
FIG. 6.19
Transfer curve for the p-channel device of Example 6.2.

6.4 SPECIFICATION SHEETS (JFETs)

As with any electronic device it is important to be able to understand the data provided on a specification sheet. Often times the notation used is different than we normally apply so a measure of translation may have to be applied. In general, however, the headings for the data are uniform and include **Maximum Ratings, Thermal Characteristics, Electrical Characteristics**, and sets of **Typical Characteristics**. In Fig. 6.20 the specification sheets for a Fairchild Semiconductor 2N5457 *n*-channel JFET appears with two types of packaging techniques. The TO-92 package is for a higher power device than the surface mount SOT-23 unit.

FAIRCHILD
SEMICONDUCTOR TM

2N5457 **MMBF5457**



NOTE: Source & Drain are interchangeable

N-Channel General Purpose Amplifier
This device is a low-level audio amplifier and switching transistor, and can be used for analog switching applications.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	25	V
V_{DG}	Drain-Gate Voltage	25	V
V_{GS}	Gate-Source Voltage	–25	V
I_{GF}	Forward Gate Current	10	mA
T_j, T_{stg}	Operating and Storage Junction Temperature Range	–55 to +150	°C

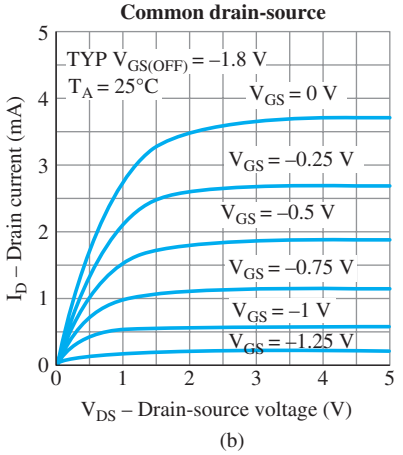
THERMAL CHARACTERISTICS

Symbol	Characteristic	Max		Units
		2N5457	*MMBF5457	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	125		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	357	556	°C/W

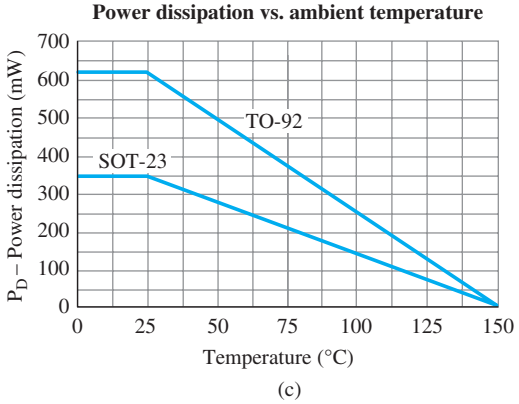
ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	I_G = 10 μA, V_{DS} = 0		–25			V
I_{GSS}	Gate Reverse Current	V_{GS} = –15 V, V_{DS} = 0 V_{GS} = –15 V, V_{DS} = 0, T_A = 100°C				–1.0 –200	nA nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15 V, I_D = 10 nA	5457	–0.5		–6.0	V
V_{GS}	Gate-Source Voltage	V_{DS} = 15 V, I_D = 100 μA	5457		–2.5		V
ON CHARACTERISTICS							
I_{DSS}	Zero-Gate Voltage Drain Current	V_{DS} = 15 V, V_{GS} = 0	5457	1.0	3.0	5.0	mA
SMALL SIGNAL CHARACTERISTICS							
g_{fs}	Forward Transfer Conductance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz	5457	1000		5000	μmhos
g_{os}	Output Conductance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz			10	50	μmhos
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz			4.5	7.0	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz			1.5	3.0	pF
NF	Noise Figure	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz, R_G = 1.0 megohm, BW = 1.0 Hz				3.0	dB

(a)

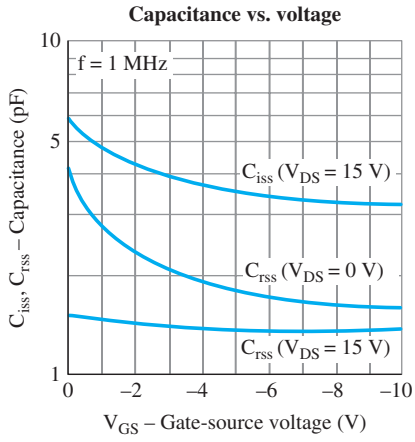


(b)

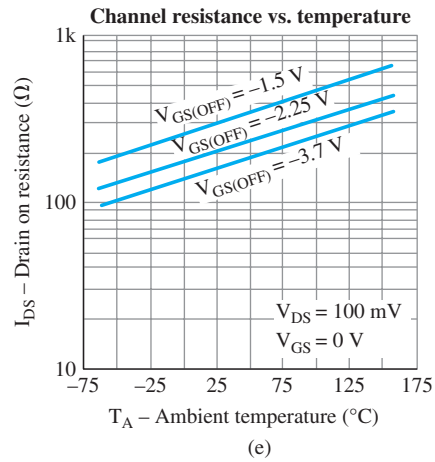


(c)

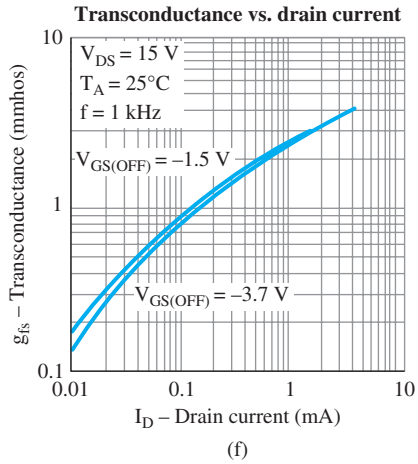
FIG. 6.20
n-channel 2N5457 JFET Characteristic k.



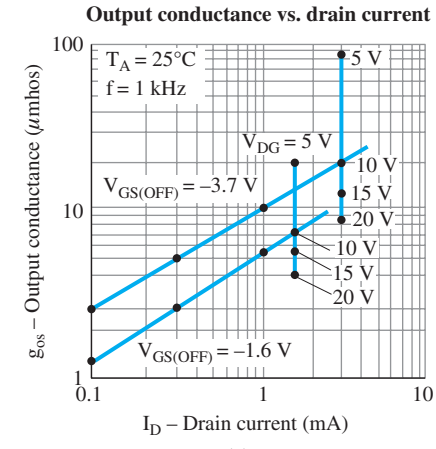
(d)



(e)



(f)



(g)

FIG. 6.20
Continued

Maximum Ratings

The maximum rating list usually appears at the beginning of the specification sheet, with the maximum voltages between specific terminals, maximum current levels, and the maximum power dissipation level of the device. The specified maximum levels for V_{DS}, V_{DG} and V_{GS} must not be exceeded at any point in the design operation of the device. Any good design will try to avoid these levels by a good margin of safety. Although normally designed to operate with $I_G = 0$ mA, if *forced* to accept a gate current, it could withstand 10 mA (I_{GF}) before damage would occur.

Thermal Characteristics

The total device dissipation at 25°C (room temperature) is the maximum power the device can dissipate under normal operating conditions and is defined by

$$P_D = V_{DS} I_D \tag{6.11}$$

Note the similarity in format with the maximum power dissipation equation for the BJT transistor.

The derating factor is discussed in detail in Chapter 3, but for the moment recognize that the 5 mW/°C rating reveals that the dissipation rating *decreases* by 5 mW for each *increase* in temperature of 1°C above 25°C.

Electrical Characteristics

The electrical characteristics include the level of V_P in the "off" characteristics and I_{DSS} in the "on" characteristics. In this case $V_P = V_{GS(\text{off})}$ has a range from −0.5 V to −6.0 V and I_{DSS} from 1 mA to 5 mA. The fact that both will vary from device to device with the same nameplate identification must be considered in the design process. The small-signal characteristics will become important when we examine ac networks in Chapter 8.

Typical Characteristics

The Typical Characteristics listing will include a variety of curves demonstrating how important parameters vary with voltage, current, temperature, and frequency.

First note in Fig. 6.20a that the plot includes the negative region of V_{GS} on the normally positive side of the horizontal axis. Notice also that the plot is for a pinch-off voltage of −2.6 V, which is about halfway between the range of possible pinch-off voltages. If this is the only plot provided it acts like an average value between limits. The Common-Drain characteristics are provided in Fig. 6.20b for a pinch-off voltage of −1.8 V. Note how the drain current drops to 0 ampere when this pinch-off voltage is applied. Also note that the I_{DSS} level is only about 3.75 mA for this pinch-off voltage, whereas it was about 9.5 mA for a pinch-off of −2.6 V in Fig. 6.20a. The Power Dissipation versus Ambient temperature is plotted in Fig. 6.20c, clearly showing the dramatic drop in power handling capability with temperature. At the boiling point of water (100°C) it is only 250 mW compared with 650 mW at room temperature. Capacitive effects in Fig. 6.20d will become very important at high frequencies because of the resulting reactance and the effect on speed of operation. It is interesting to note that the more negative the gate-to-source voltage, the less the capacitive effects at a frequency of 1 MHz. The Channel Resistance plot of Fig. 6.20e demonstrates how the channel resistance changes with temperature at various levels of $V_{GS(\text{OFF})}$. At first glance the change may not appear that dramatic, but take note of the fact that the vertical axis is a log scale extending from 10 Ω to 1 kΩ. The plots of Transconductance (Fig. 6.20f) and Output Conductance (Fig. 6.20g) will become important when we consider JFET ac networks. They define the two parameters of the ac equivalent circuit. Each is certainly affected by the level of drain current with lesser sensitivity to the pinch-off voltage.

Operating Region

The specification sheet and the curve defined by the pinch-off levels at each level of V_{GS} define the region of operation for linear amplification on the drain characteristics as shown in Fig. 6.21. The ohmic region defines the minimum permissible values of V_{DS} at each level of V_{GS}, and $V_{DS_{\text{max}}}$ specifies the maximum value for this parameter. The saturation

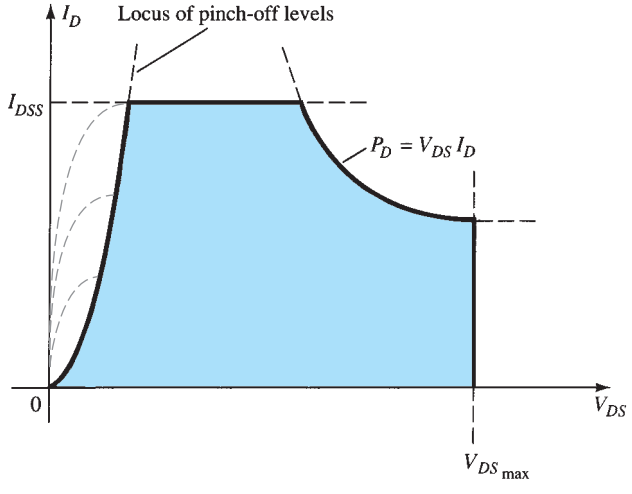


FIG. 6.21
Normal operating region for linear amplifier design.

current I_{DSS} is the maximum drain current, and the maximum power dissipation level defines the curve drawn in the same manner as described for BJT transistors. The resulting shaded region is the normal operating region for amplifier design.

6.5 INSTRUMENTATION

Recall from Chapter 3 that hand-held instruments are available to measure the level of β_{dc} for the BJT transistor. Similar instrumentation is not available to measure the levels of I_{DSS} and V_P. However, the curve tracer introduced for the BJT transistor can also display the drain characteristics of the JFET transistor through a proper setting of the various controls. The vertical scale (in milliamperes) and the horizontal scale (in volts) have been set to provide a full display of the characteristics, as shown in Fig. 6.22. For the JFET of Fig. 6.22, each vertical division (in centimeters) reflects a 1-mA change in I_D, whereas each horizontal division has a value of 1 V. The step voltage is 500 mV/step (0.5 V/step), revealing that the top curve is defined by $V_{GS} = 0$ V and the next curve down is -0.5 V for the *n*-channel device. Using the same step voltage, we see the next curve is -1 V, then -1.5 V, and finally -2 V. By drawing a line from the top curve over to the I_D axis, we can estimate the level of I_{DSS} to be about 9 mA. The level of V_P can be estimated by noting the V_{GS} value of the bottom curve and taking into account the shrinking distance between curves as V_{GS} becomes more and more negative. In this case, V_P is certainly more negative than -2 V, and perhaps V_P is close to -2.5 V. However, keep in mind that the V_{GS} curves contract very quickly as they approach the cutoff condition, and perhaps $V_P = -3$ V is a better choice. It should also be noted that the step control is set for a five-step display, limiting the displayed curves to $V_{GS} = 0, -0.5, -1, -1.5$, and -2 V. If the step control had been increased to 10, the voltage per step could be reduced to 250 mV $= 0.25$ V and the curve for $V_{GS} = -2.25$ V would have been included as well as an additional curve between each step of Fig. 6.22. The $V_{GS} = -2.25$ V curve would reveal how quickly the curves are closing in on each other for the same step voltage. Fortunately, the level of V_P can be estimated to a reasonable degree of accuracy simply by applying a condition appearing

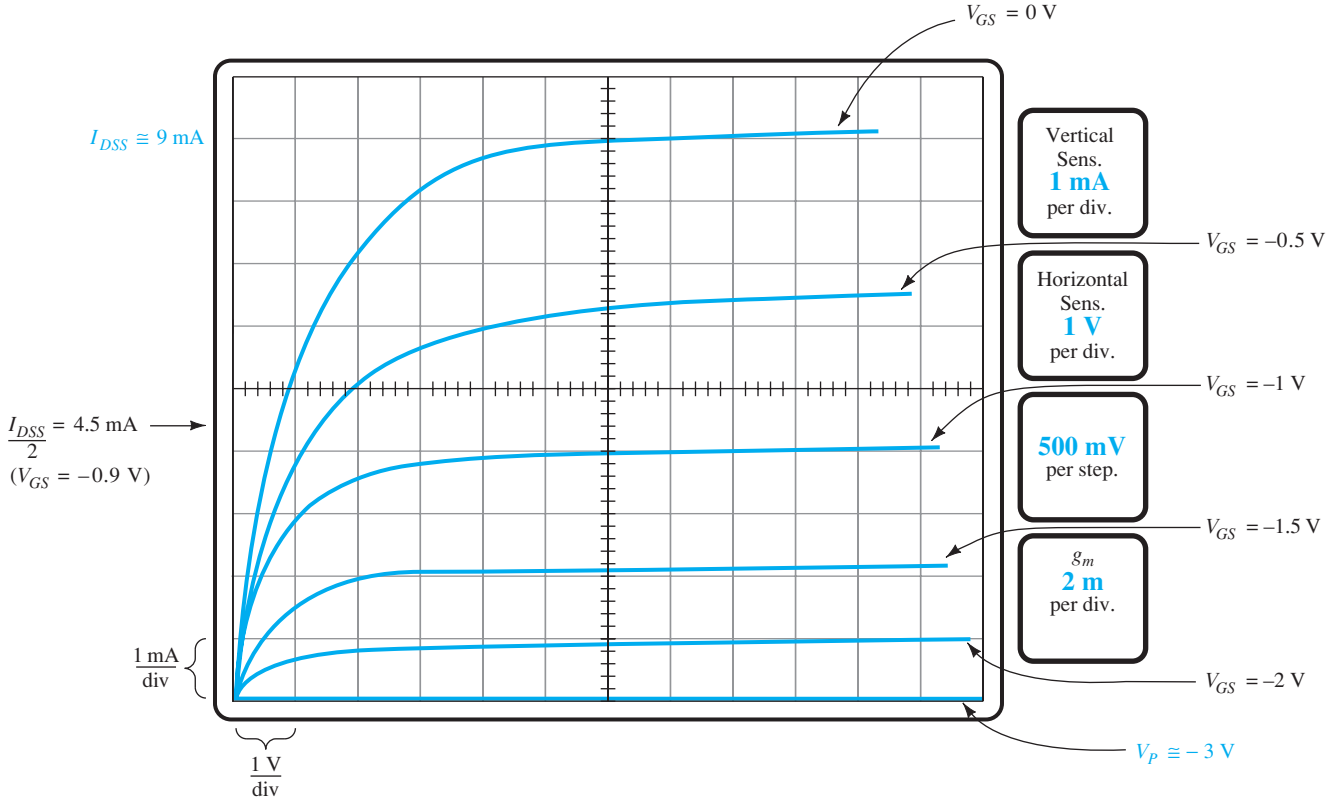


FIG. 6.22

Drain characteristics for a 2N4416 JFET transistor as displayed on a curve tracer.

in Table 6.1. That is, when $I_D = I_{DSS}/2$, then $V_{GS} = 0.3V_P$. For the characteristics of Fig. 6.22, $I_D = I_{DSS}/2 = 9\text{ mA}/2 = 4.5\text{ mA}$, and, as visible from Fig. 6.22, the corresponding level of V_{GS} is about -0.9 V. Using this information, we find that $V_P = V_{GS}/0.3 = -0.9\text{ V}/0.3 = -3\text{ V}$, which will be our choice for this device. Using this value, we find that at $V_{GS} = -2\text{ V}$,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= 9\text{ mA}\left(1 - \frac{-2\text{ V}}{-3\text{ V}}\right)^2$$
$$\cong 1\text{ mA}$$

as supported by Fig. 6.22.

At $V_{GS} = -2.5\text{ V}$, Shockley's equation results in $I_D = 0.25\text{ mA}$, with $V_P = -3\text{ V}$, clearly revealing how quickly the curves contract near V_P. The importance of the parameter g_m and how it is determined from the characteristics of Fig. 6.22 are described in Chapter 8 when small-signal ac conditions are examined.

6.6 IMPORTANT RELATIONSHIPS

A number of important equations and operating characteristics for the JFET have been introduced that are of particular importance for the analysis of dc and ac configurations that will follow. To isolate and emphasize their importance, they are repeated in Table 6.2 next to corresponding equations for the BJT transistor. The JFET equations are defined for the configuration of Fig. 6.23a, whereas the BJT equations relate to Fig. 6.23b.

TABLE 6.2

JFET		*BJT*
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0\text{ A}$	$\Leftrightarrow$	$V_{BE} \cong 0.7\text{ V}$

(6.12)

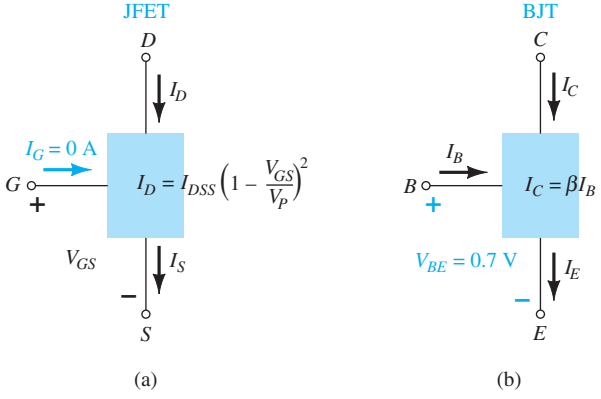


FIG. 6.23
(a) JFET versus (b) BJT.

A clear understanding of the effect of each of the equations above is sufficient background to approach the most complex of dc configurations. Recall that $V_{BE} = 0.7\text{ V}$ was often the key to initiating an analysis of a BJT configuration. Similarly, the condition $I_G = 0\text{ A}$ is often the starting point for the analysis of a JFET configuration. For the BJT configuration, I_B is normally the first parameter to be determined. For the JFET, it is normally V_{GS}. The number of similarities between the analysis of BJT and JFET dc configurations will become quite apparent in Chapter 7.

6.7 DEPLETION-TYPE MOSFET

As noted in the introduction, there are three types of FETs: JFETs, MOSFETs, and MESFETs. MOSFETs are further broken down into *depletion type* and *enhancement type*. The terms *depletion* and *enhancement* define their basic mode of operation; the name MOSFET stands for *m*etal–*o*xide–*s*emiconductor *f*ield-*e*ffect *t*ransistor. Since there are differences in the characteristics and operation of different types of MOSFET, they are covered in separate sections. In this section we examine the depletion-type MOSFET, which has characteristics similar to those of a JFET between cutoff and saturation at I_{DSS}, and also has the added feature of characteristics that extend into the region of opposite polarity for V_{GS}.

Basic Construction

The basic construction of the *n*-channel depletion-type MOSFET is provided in Fig. 6.24. A slab of *p*-type material is formed from a silicon base and is referred to as the *substrate*. It is the foundation on which the device is constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labeled *SS*, resulting in a four-terminal device, such as that in Fig. 6.24. The source and drain terminals are connected through metallic contacts to *n*-doped regions linked by an *n*-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the *n*-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a type of insulator referred to as a *dielectric*, which sets up opposing (as indicated by the prefix *di-*) electric fields within the dielectric when exposed to an externally applied field. The fact that the SiO_2 layer is an insulating layer means that:

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

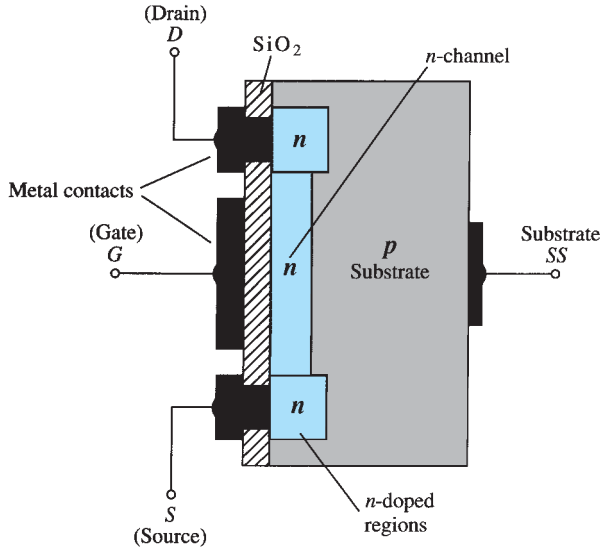


FIG. 6.24
n-Channel depletion-type MOSFET.

In addition:

It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

In fact, the input resistance of a MOSFET is usually more than that of a typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications. Because of the very high input impedance, the gate current I_G is essentially 0 A for dc-biased configurations.

The reason for the label metal–oxide–semiconductor FET is now fairly obvious: *metal* for the drain, source, and gate connections; *oxide* for the silicon dioxide insulating layer; and

semiconductor for the basic structure on which the *n*- and *p*-type regions are diffused. The insulating layer between the gate and the channel has resulted in another name for the device: *insulated-gate FET*, or *IGFET*, although this label is used less and less in the literature.

Basic Operation and Characteristics

In Fig. 6.25 the gate-to-source voltage is set to 0 V by the direct connection from one terminal to the other, and a voltage V_{DD} is applied across the drain-to-source terminals. The result is an attraction of the free electrons of the *n*-channel for the positive voltage at the drain. The result is a current similar to that flowing in the channel of the JFET. In fact, the resulting current with $V_{GS} = 0$ V continues to be labeled I_{DSS}, as shown in Fig. 6.26.

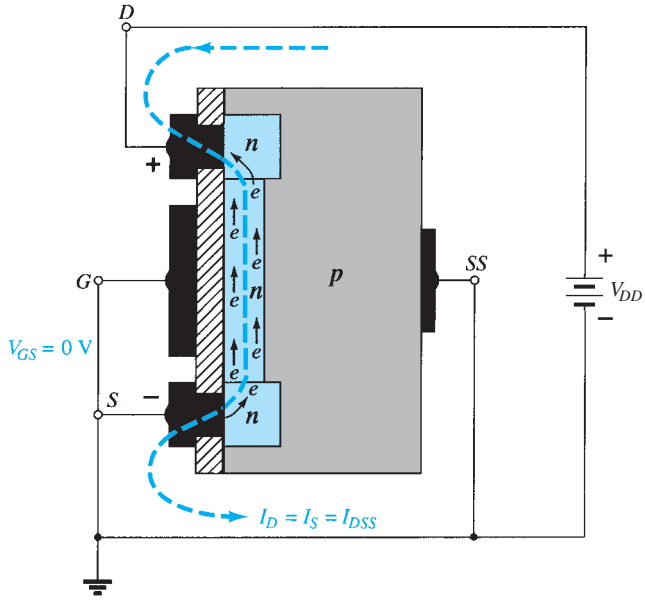


FIG. 6.25
n-Channel depletion-type MOSFET with $V_{GS} = 0$ V and applied voltage V_{DD}.

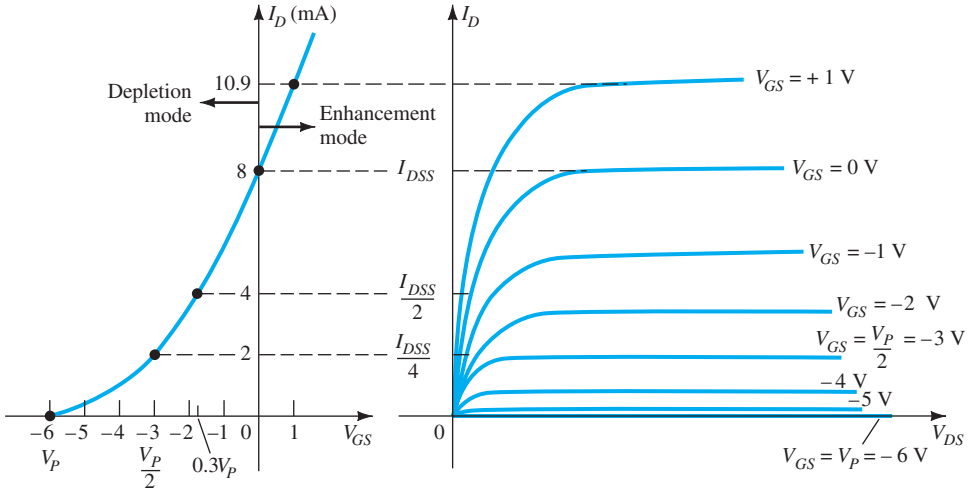


FIG. 6.26
Drain and transfer characteristics for an n-channel depletion-type MOSFET.

In Fig. 6.27, V_{GS} is set at a negative voltage such as −1 V. The negative potential at the gate will tend to pressure electrons toward the *p*-type substrate (like charges repel) and attract holes from the *p*-type substrate (opposite charges attract) as shown in Fig. 6.27. Depending on the

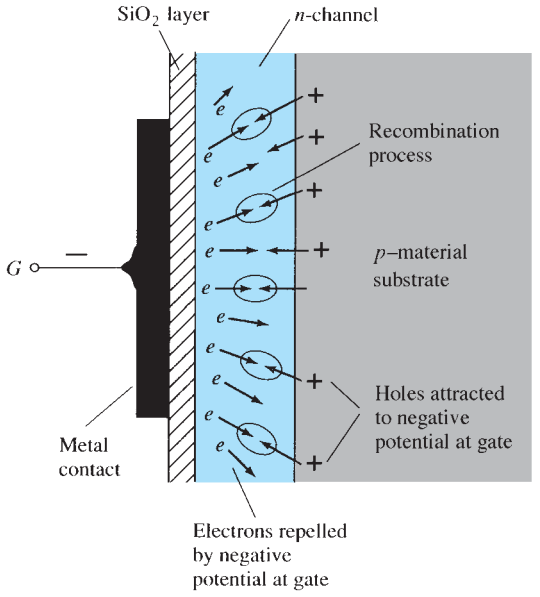


FIG. 6.27
Reduction in free carriers in a channel due to a negative potential at the gate terminal.

magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the *n*-channel available for conduction. The more negative the bias, the higher is the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}, as shown in Fig. 6.26 for $V_{GS} = -1$ V, -2 V, and so on, to the pinch-off level of -6 V. The resulting levels of drain current and the plotting of the transfer curve proceed exactly as described for the JFET.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the *p*-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 6.26 reveals that the drain current will increase at a rapid rate for the reasons listed above. The vertical spacing between the $V_{GS} = 0$ V and $V_{GS} = +1$ V curves of Fig. 6.26 is a clear indication of how much the current has increased for the 1-V change in V_{GS}. Due to the rapid rise, the user must be aware of the maximum drain current rating since it could be exceeded with a positive gate voltage. That is, for the device of Fig. 6.26, the application of a voltage $V_{GS} = +4$ V would result in a drain current of 22.2 mA, which could possibly exceed the maximum rating (current or power) for the device. As revealed above, the application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with $V_{GS} = 0$ V. For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region*, with the region between cutoff and the saturation level of I_{DSS} referred to as the *depletion region.*

It is particularly interesting and helpful that Shockley's equation will continue to be applicable for the depletion-type MOSFET characteristics in both the depletion and enhancement regions. For both regions, it is simply necessary that the proper sign be included with V_{GS} in the equation and the sign be carefully monitored in the mathematical operations.

EXAMPLE 6.3 Sketch the transfer characteristics for an *n*-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

Solution:

$$\text{At } V_{GS} = 0 \text{ V}, \quad I_D = I_{DSS} = 10 \text{ mA}$$

$$V_{GS} = V_P = -4 \text{ V}, \quad I_D = 0 \text{ mA}$$

$$V_{GS} = \frac{V_P}{2} = \frac{-4 \text{ V}}{2} = -2 \text{ V}, \quad I_D = \frac{I_{DSS}}{4} = \frac{10 \text{ mA}}{4} = 2.5 \text{ mA}$$

and at $I_D = \dfrac{I_{DSS}}{2}$,

$$V_{GS} = 0.3V_P = 0.3(-4\text{ V}) = -1.2\text{ V}$$

all of which appear in Fig. 6.28.

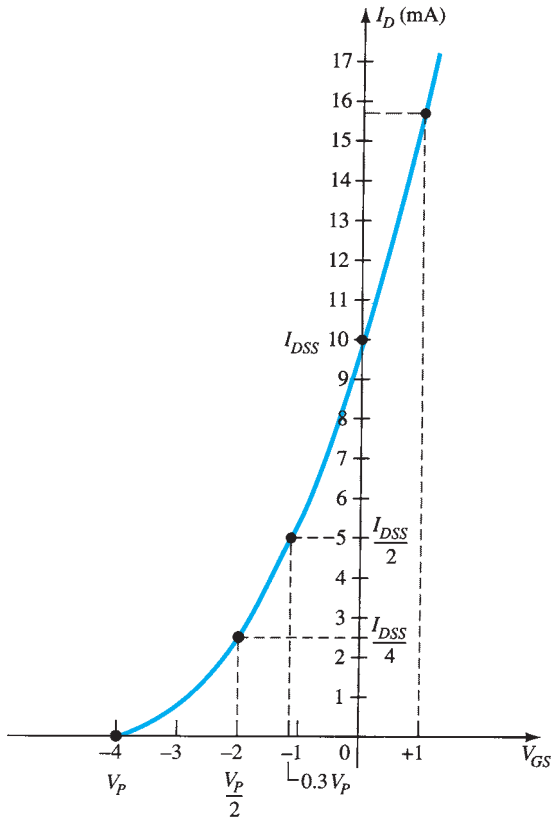


FIG. 6.28

Transfer characteristics for an n-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

Before plotting the positive region of V_{GS}, keep in mind that I_D increases very rapidly with increasing positive values of V_{GS}. In other words, be conservative with the choice of values to be substituted into Shockley's equation. In this case, we try +1 V as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= (10\text{ mA})\left(1 - \frac{+1\text{ V}}{-4\text{ V}}\right)^2 = (10\text{ mA})\,(1 + 0.25)^2 = (10\text{ mA})\,(1.5625)$$

$$\cong 15.63\text{ mA}$$

which is sufficiently high to finish the plot.

p-Channel Depletion-Type MOSFET

The construction of a *p*-channel depletion-type MOSFET is exactly the reverse of that appearing in Fig. 6.24. That is, there is now an *n*-type substrate and a *p*-type channel, as shown in Fig. 6.29a. The terminals remain as identified, but all the voltage polarities and the current directions are reversed, as shown in the same figure. The drain characteristics would appear exactly as in Fig. 6.26, but with V_{DS} having negative values, I_D having positive values as indicated (since the defined direction is now reversed), and V_{GS} having the opposite polarities as shown in Fig. 6.29c. The reversal in V_{GS} will result in a mirror image (about the I_D axis) for the transfer characteristics as shown in Fig. 6.29b. In other words,

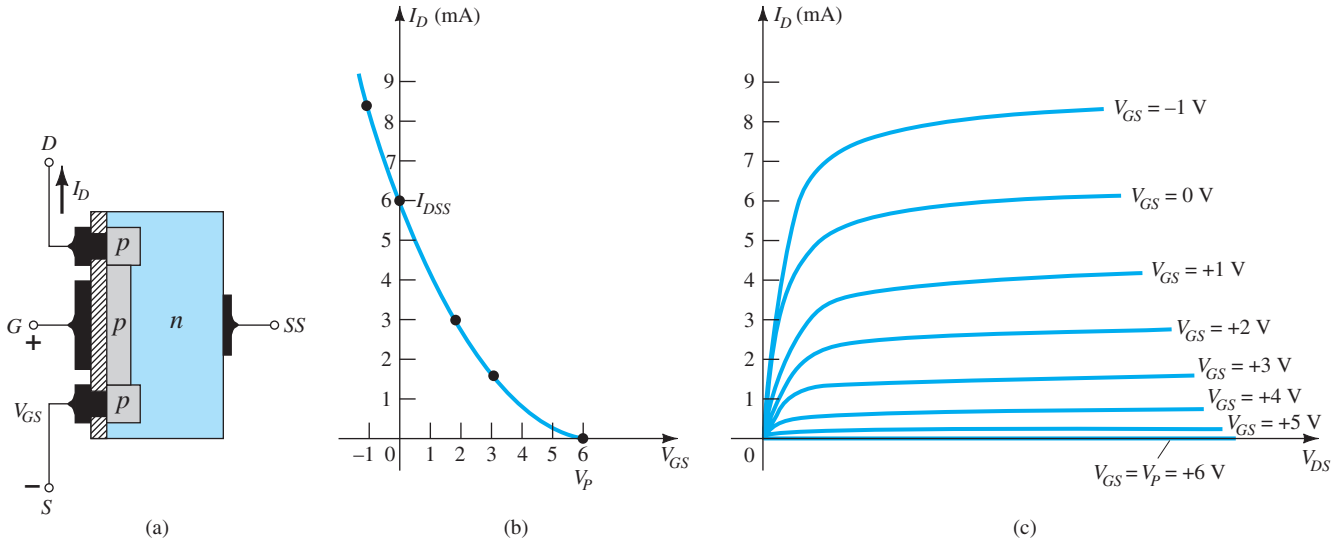


FIG. 6.29

p-Channel depletion-type MOSFET with $I_{DSS} = 6$ mA and $V_P = +6$ V.

the drain current will increase from cutoff at $V_{GS} = V_P$ in the positive V_{GS} region to I_{DSS} and then continue to increase for increasingly negative values of V_{GS}. Shockley's equation is still applicable and requires simply placing the correct sign for both V_{GS} and V_P in the equation.

Symbols, Specification Sheets, and Case Construction

The graphic symbols for an *n*- and *p*-channel depletion-type MOSFET are provided in Fig. 6.30. Note how the symbols chosen try to reflect the actual construction of the device. The lack of a direct connection (due to the gate insulation) between the gate and the channel is represented by a space between the gate and the other terminals of the symbol. The vertical line representing the channel is connected between the drain and the source and is "supported" by the substrate. Two symbols are provided for each type of channel to reflect the fact that in some cases the substrate is externally available, whereas in others it is not. For most of the analysis to follow in Chapter 7, the substrate and the source will be connected and the lower symbols will be employed.

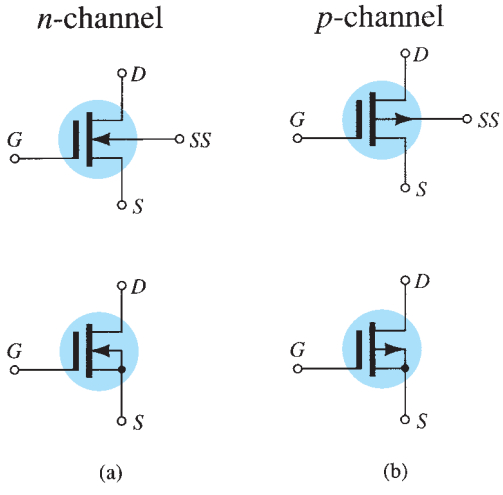


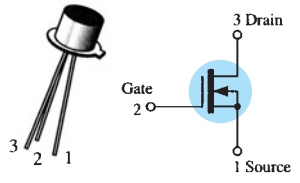
FIG. 6.30

Graphic symbols for: (a) n-channel depletion-type MOSFETs and (b) p-channel depletion-type MOSFETs.

The device appearing in Fig. 6.31 has three terminals, with the terminal identification appearing in the same figure. The specification sheet for a depletion-type MOSFET is similar to that of a JFET. The levels of V_P and I_{DSS} are provided along with a list of maximum values and typical "on" and "off" characteristics. In addition, however, since I_D can extend beyond the I_{DSS} level, another point is normally provided that reflects a typical value of I_D for some positive voltage (for an *n*-channel device). For the unit of Fig. 6.31, I_D is specified as $I_{D(on)} = 9$ mA dc, with $V_{DS} = 10$ V and $V_{GS} = 3.5$ V.

2N3797

MOSFET
LOW–POWER AUDIO



N-CHANNEL – DEPLETION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage 2N3797	V_{DS}	20	Vdc
Gate–Source Voltage	V_{GS}	±10	Vdc
Drain Current	I_D	20	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	200 1.14	mW mW/°C
Junction Temperature Range	T_J	+175	°C
Storage Channel Temperature Range	T_{stg}	–65 to +200	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain Source Breakdown Voltage ($V_{GS} = -7.0$ V, $I_D = 5.0$ μA)	2N3797	$V_{(BR)DSX}$	20	25	–	Vdc
Gate Reverse Current (1) ($V_{GS} = -10$ V, $V_{DS} = 0$) ($V_{GS} = -10$ V, $V_{DS} = 0$, $T_A = 150°C$)		I_{GSS}	– –	– –	1.0 200	pAdc
Gate Source Cutoff Voltage ($I_D = 2.0$ μA, $V_{DS} = 10$ V)	2N3797	$V_{GS(off)}$	–	–5.0	–7.0	Vdc
Drain-Gate Reverse Current (1) ($V_{DG} = 10$ V, $I_S = 0$)		I_{DGO}	–	–	1.0	pAdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current ($V_{DS} = 10$ V, $V_{GS} = 0$)	2N3797	I_{DSS}	2.0	2.9	6.0	mAdc
On-State Drain Current ($V_{DS} = 10$ V, $V_{GS} = +3.5$ V)	2N3797	$I_{D(on)}$	9.0	14	18	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 kHz)	2N3797	$\lvert y_{fs} \rvert$	1500	2300	3000	μmhos
($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz)	2N3797		1500	–	–	
Output Admittance ($I_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 kHz)	2N3797	$\lvert y_{os} \rvert$	–	27	60	μmhos
Input Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz)	2N3797	C_{iss}	–	6.0	8.0	pF
Reverse Transfer Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz)		C_{rss}	–	0.5	0.8	pF
FUNCTIONAL CHARACTERISTICS						
Noise Figure ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 kHz, $R_S = 3$ megohms)		NF	–	3.8	–	dB

(1) This value of current includes both the FET leakage current as well as the leakage current associated with the test socket and fixture when measured under best attainable conditions.

FIG. 6.31
2N3797 Motorola n-channel depletion-type MOSFET.

6.8 ENHANCEMENT-TYPE MOSFET

Although there are some similarities in construction and mode of operation between depletion-type and enhancement-type MOSFETs, the characteristics of the enhancement-type MOSFET are quite different from anything obtained thus far. The transfer curve is not defined by Shockley's equation, and the drain current is now cut off until the gate-to-source voltage reaches a specific magnitude. In particular, current control in an *n*-channel device is now effected by a positive gate-to-source voltage rather than the range of negative voltages encountered for *n*-channel JFETs and *n*-channel depletion-type MOSFETs.

Basic Construction

The basic construction of the *n*-channel enhancement-type MOSFET is provided in Fig. 6.32. A slab of *p*-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, whereas in other cases a fourth lead (labeled SS) is made available for external control of its potential level. The source and drain terminals are again connected through metallic contacts to *n*-doped regions, but note in Fig. 6.32 the absence of a channel between the two *n*-doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs—the absence of a channel as a constructed component of the device. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the *p*-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

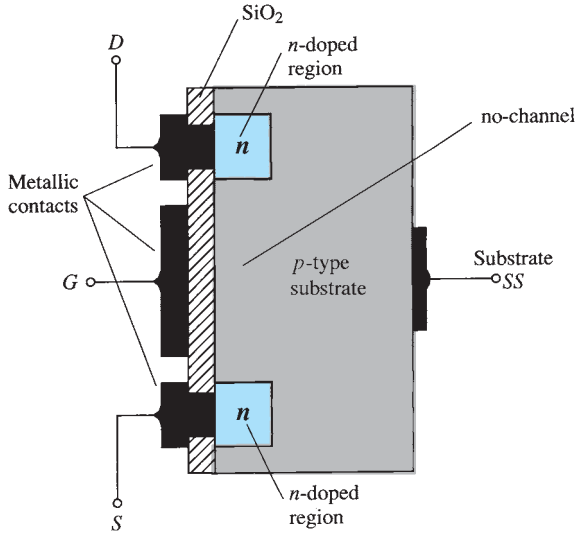


FIG. 6.32
n-Channel enhancement-type MOSFET.

Basic Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and the source of the device of Fig. 6.32, the absence of an *n*-channel (with its generous number of free carriers) will result in a current of effectively 0 A—quite different from the depletion-type MOSFET and JFET, where $I_D = I_{DSS}$. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and the source (due to the *n*-doped regions) if a path fails to exist between the two. With V_{DS} some positive voltage, V_{GS} at 0 V, and terminal *SS* directly connected to the source, there are in fact two reverse-biased *p*–*n* junctions between the *n*-doped regions and the *p*-substrate to oppose any significant flow between drain and source.

In Fig. 6.33, both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and the gate at a positive potential with respect to the source.

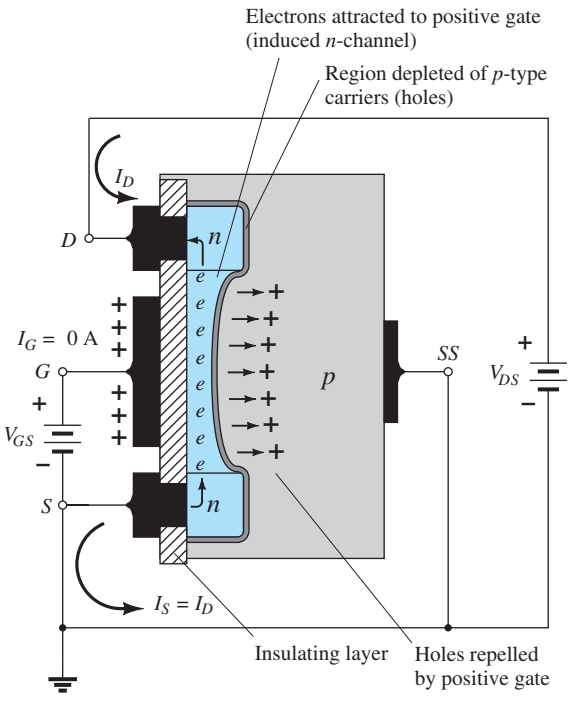


FIG. 6.33
Channel formation in the n-channel enhancement-type MOSFET.

The positive potential at the gate will pressure the holes (since like charges repel) in the *p*-substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the *p*-substrate, as shown in the figure. The result is a depletion region near the SiO_2 insulating layer void of holes. However, the electrons in the *p*-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases until eventually the induced *n*-type region can support a measurable flow between drain and source. The level of V_{GS} that results in the significant increase in drain current is called the *threshold voltage* and is given the symbol V_T. On specification sheets it is referred to as $V_{GS(Th)}$, although V_T is less unwieldy and will be used in the analysis to follow. Since the channel is nonexistent with $V_{GS} = 0$ V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an *enhancement-type MOSFET*. Both depletion- and enhancement-type MOSFETs have enhancement-type regions, but the label was applied to the latter since it is its only mode of operation.

As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V_{GS} constant and increase the level of V_{DS}, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 6.34. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 6.34, we find that

$$\boxed{V_{DG} = V_{DS} - V_{GS}} \qquad \textbf{(6.13)}$$

If V_{GS} is held fixed at some value such as 8 V and V_{DS} is increased from 2 V to 5 V, the voltage V_{DG} [by Eq. (6.13)] will increase from −6 V to −3 V and the gate will become less and less positive with respect to the drain. This reduction in gate-to-drain voltage will in turn reduce the attractive forces for free carriers (electrons) in this region of the induced channel, causing a reduction in the effective channel width. Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established as described

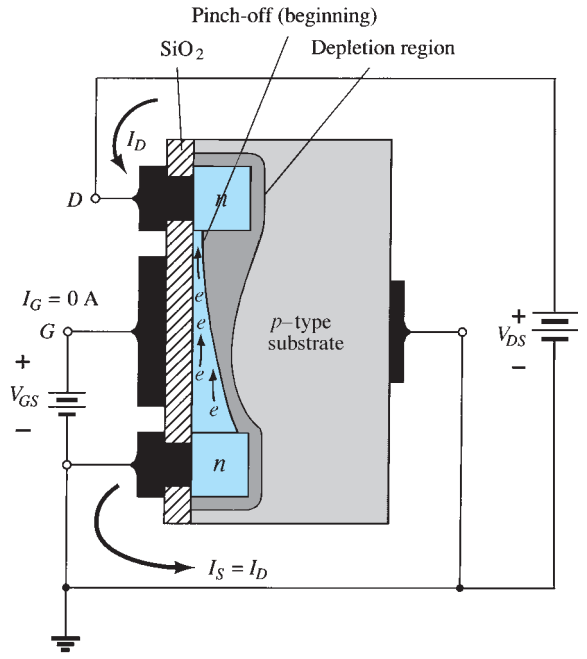


FIG. 6.34
Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}.

earlier for the JFET and depletion-type MOSFET. In other words, any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D until breakdown conditions are encountered.

The drain characteristics of Fig. 6.35 reveal that for the device of Fig. 6.34 with $V_{GS} = 8$ V, saturation occurs at a level of $V_{DS} = 6$ V. In fact, the saturation level for V_{DS} is related to the level of applied V_{GS} by

$$V_{DS_{sat}} = V_{GS} - V_T \tag{6.14}$$

Obviously, therefore, for a fixed value of V_T, the higher the level of V_{GS}, the greater is the saturation level for V_{DS}, as shown in Fig. 6.34 by the locus of saturation levels.

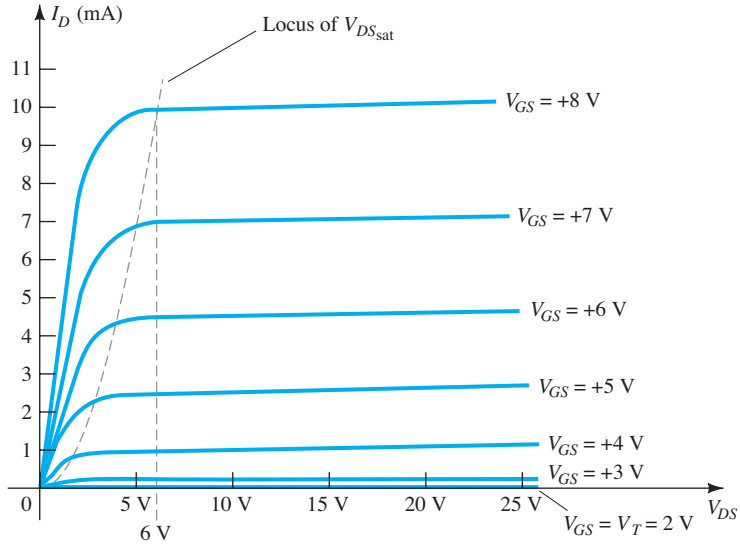


FIG. 6.35
Drain characteristics of an n-channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.278 \times 10^{-3}$ A/V^2.

For the characteristics of Fig. 6.34, the level of V_T is 2 V, as revealed by the fact that the drain current has dropped to 0 mA. In general, therefore:

For values of V_{GS} less than the threshold level, the drain current of an enhancement-type MOSFET is 0 mA.

Figure 6.35 clearly reveals that as the level of V_{GS} increases from V_T to 8 V, the resulting saturation level for I_D also increases from a level of 0 mA to 10 mA. In addition, it is quite noticeable that the spacing between the levels of V_{GS} increases as the magnitude of V_{GS} increases, resulting in ever-increasing increments in drain current.

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2 \tag{6.15}$$

Again, it is the squared term that results in the nonlinear (curved) relationship between I_D and V_{GS}. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation [derived from Eq. (6.15)], where $I_{D(on)}$ and $V_{GS(on)}$ are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} \tag{6.16}$$

Substituting $I_{D(on)} = 10$ mA when $V_{GS(on)} = 8$ V from the characteristics of Fig. 6.35 yields

$$k = \frac{10\text{ mA}}{(8\text{ V} - 2\text{ V})^2} = \frac{10\text{ mA}}{(6\text{ V})^2} = \frac{10\text{ mA}}{36\text{ V}^2}$$
$$= \mathbf{0.278 \times 10^{-3}\ A/V^2}$$

and a general equation for I_D for the characteristics of Fig. 6.35 results in

$$I_D = 0.278 \times 10^{-3}(V_{GS} - 2\text{ V})^2$$

Substituting $V_{GS} = 4$ V, we find that

$$I_D = 0.278 \times 10^{-3}(4\text{ V} - 2\text{ V})^2 = 0.278 \times 10^{-3}(2)^2$$
$$= 0.278 \times 10^{-3}(4) = \mathbf{1.11\ mA}$$

as verified by Fig. 6.35. At $V_{GS} = V_T$, the squared term is 0, and $I_D = 0$ mA.

For the dc analysis of enhancement-type MOSFETs to appear in Chapter 7, the transfer characteristics will again be the characteristics to be employed in the graphical solution. In Fig. 6.36, the drain and transfer characteristics have been set side by side to describe the

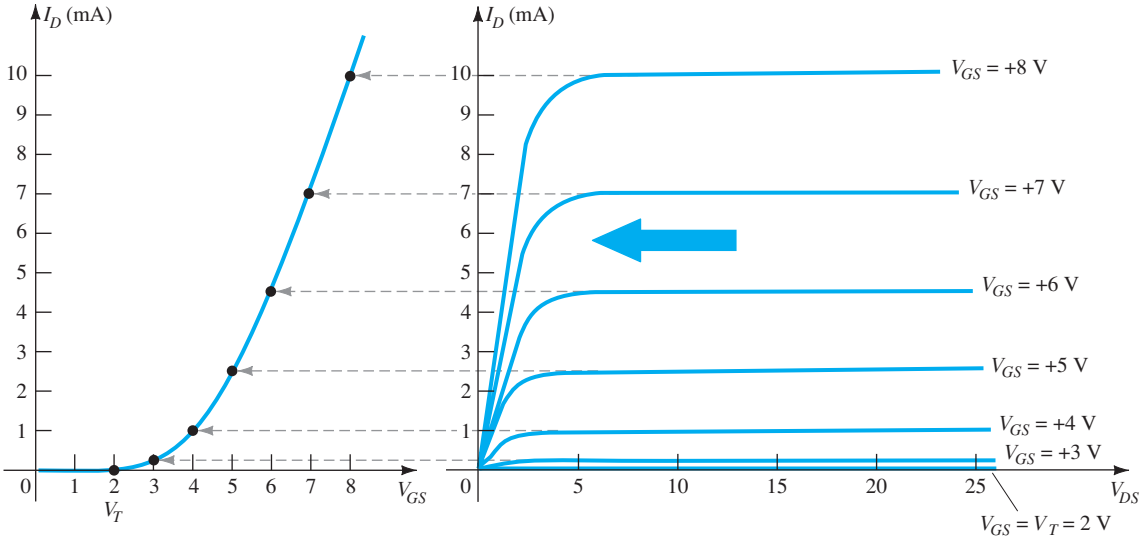


FIG. 6.36

Sketching the transfer characteristics for an n-channel enhancement-type MOSFET from the drain characteristics.

transfer process from one to the other. Essentially, it proceeds as introduced earlier for the JFET and depletion-type MOSFETs. In this case, however, it must be remembered that the drain current is 0 mA for $V_{GS} \leq V_T$. As V_{GS} is increased beyond V_T, the drain current I_D will begin to flow at an increasing rate in accordance with Eq. (6.15). Note that in defining the points on the transfer characteristics from the drain characteristics, only the saturation levels are employed, thereby limiting the region of operation to levels of V_{DS} greater than the saturation levels as defined by Eq. (6.14).

The transfer curve of Fig. 6.36 is certainly quite different from those obtained earlier. For an *n*-channel (induced) device, it is now totally in the positive V_{GS} region and does not rise until $V_{GS} = V_T$. The question now surfaces as to how to plot the transfer characteristics given the levels of k and V_T as included below for a particular MOSFET:

$$I_D = 0.5 \times 10^{-3}(V_{GS} - 4\text{ V})^2$$

First, a horizontal line is drawn at $I_D = 0$ mA from $V_{GS} = 0$ V to $V_{GS} = 4$ V as shown in Fig. 6.37a. Next, a level of V_{GS} greater than V_T such as 5 V is chosen and substituted into Eq. (6.15) to determine the resulting level of I_D as follows:

$$\begin{aligned} I_D &= 0.5 \times 10^{-3}(V_{GS} - 4\text{ V})^2 \\ &= 0.5 \times 10^{-3}(5\text{ V} - 4\text{ V})^2 = 0.5 \times 10^{-3}(1)^2 \\ &= \mathbf{0.5\text{ mA}} \end{aligned}$$

and a point on the plot is obtained as shown in Fig. 6.37b. Finally, additional levels of V_{GS} are chosen and the resulting levels of I_D obtained. In particular, at $V_{GS} = 6$, 7, and 8 V, the level of I_D is 2, 4.5, and 8 mA, respectively, as shown on the resulting plot of Fig. 6.37c.

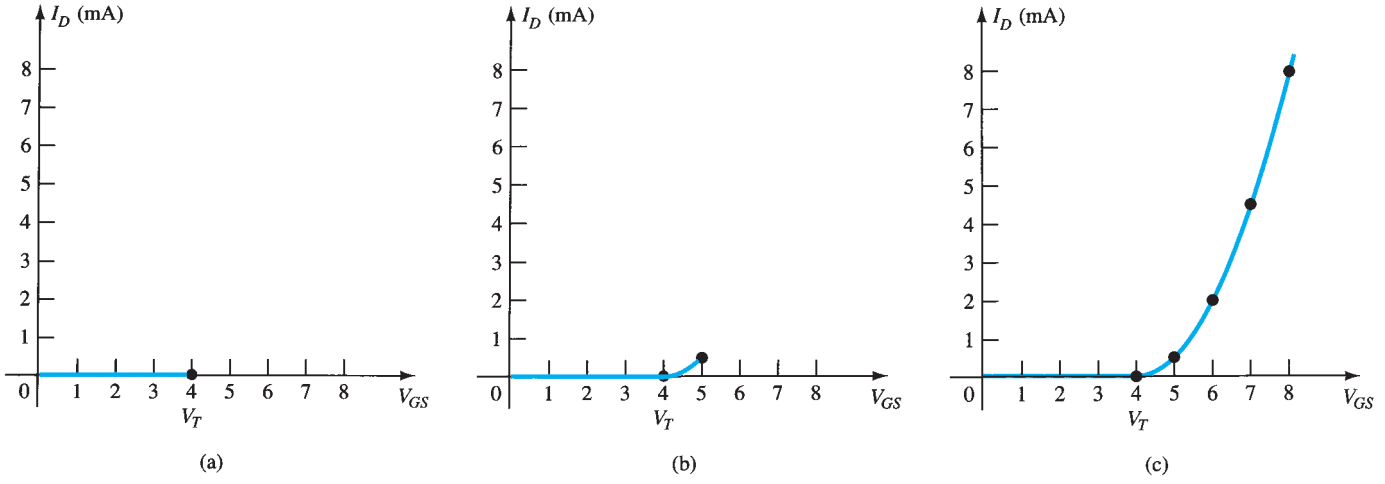


FIG. 6.37

Plotting the transfer characteristics of an n-channel enhancement-type MOSFET with $k = 0.5 \times 10^{-3}$ A/V^2 and $V_T = 4$ V.

p-Channel Enhancement-Type MOSFETs

The construction of a *p*-channel enhancement-type MOSFET is exactly the reverse of that appearing in Fig. 6.32, as shown in Fig. 6.38a. That is, there is now an *n*-type substrate and *p*-doped regions under the drain and source connections. The terminals remain as identified, but all the voltage polarities and the current directions are reversed. The drain characteristics will appear as shown in Fig. 6.38c, with increasing levels of current resulting from increasingly negative values of V_{GS}. The transfer characteristics of Fig. 6.38b will be the mirror image (about the I_D axis) of the transfer curve of Fig. 6.36, with I_D increasing with increasingly negative values of V_{GS} beyond V_T, as shown in Fig. 6.38c. Equations (6.13) through (6.16) are equally applicable to *p*-channel devices.

Symbols, Specification Sheets, and Case Construction

The graphic symbols for the *n*- and *p*-channel enhancement-type MOSFETs are provided as Fig. 6.39. Again note how the symbols try to reflect the actual construction of

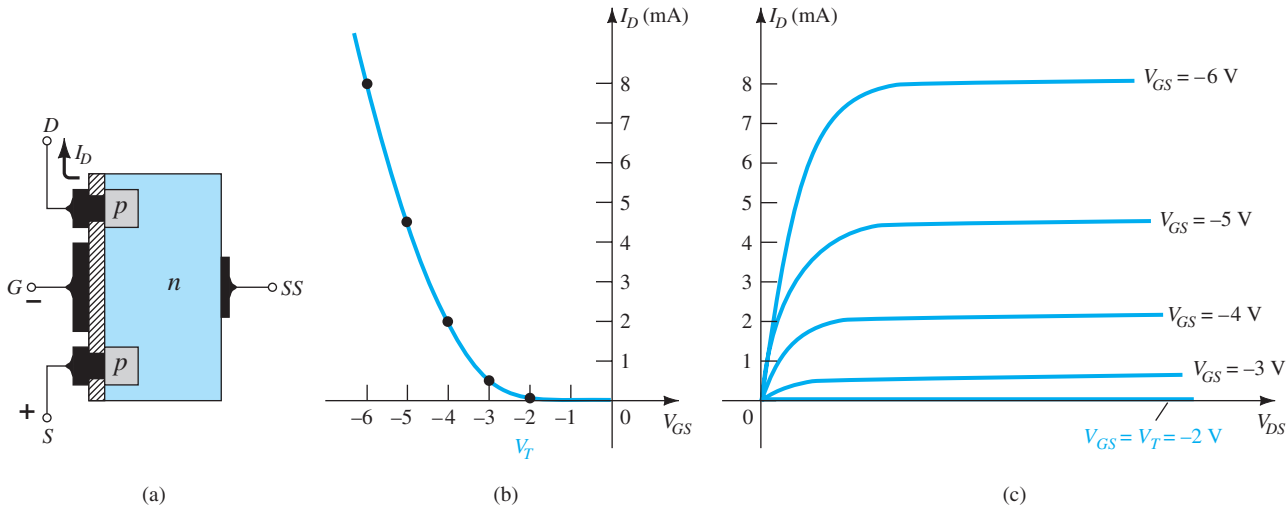


FIG. 6.38
p-Channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.5 \times 10^{-3}$ A/V^2.

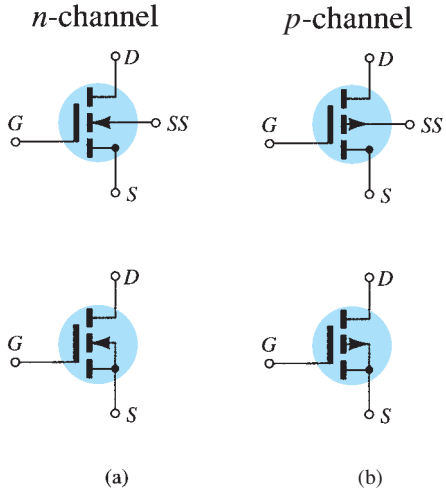


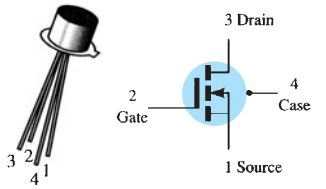
FIG. 6.39
Symbols for: (a) n-channel enhancement-type MOSFETs and (b) p-channel enhancement-type MOSFETs.

the device. The dashed line between drain and source is chosen to reflect the fact that a channel does not exist between the two under no-bias conditions. It is, in fact, the only difference between the symbols for the depletion-type and enhancement-type MOSFETs.

The specification sheet for a Motorola *n*-channel enhancement-type MOSFET is provided as Fig. 6.40. The case construction and the terminal identification are provided next to the maximum ratings, which now include a maximum drain current of 30 mA dc. The specification sheet provides the level of I_{DSS} under "off" conditions, which is now simply 10 nA dc (at $V_{DS} = 10$ V and $V_{GS} = 0$ V), compared to the milliampere range for the JFET and the depletion-type MOSFET. The threshold voltage is specified as $V_{GS(\text{Th})}$ and has a range of 1 to 5 V dc, depending on the device employed. Rather than provide a range of k in Eq. (6.15), a typical level of $I_{D(\text{on})}$ (3 mA in this case) is specified at a particular level of $V_{GS(\text{on})}$ (10 V for the specified I_D level). In other words, when $V_{GS} = 10$ V, $I_D = 3$ mA. The given levels of $V_{GS(\text{Th})}$, $I_{D(\text{on})}$, and $V_{GS(\text{on})}$ permit a determination of k from Eq. (6.16) and a writing of the general equation for the transfer characteristics. The handling requirements of MOSFETs are reviewed in Section 6.9.

2N4351

MOSFET SWITCHING



N-CHANNEL – ENHANCEMENT

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	30	Vdc
Gate–Source Voltage*	V_{GS}	30	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	300 1.7	mW mW/°C
Junction Temperature Range	T_J	175	°C
Storage Temperature Range	T_{stg}	–65 to +175	°C

* Transient potentials of ± 75 Volt will not cause gate-oxide failure.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($I_D = 10\ \mu A$, $V_{GS} = 0$)	$V_{(BR)DSX}$	25	–	Vdc
Zero-Gate-Voltage Drain Current ($V_{DS} = 10$ V, $V_{GS} = 0$) $T_A = 25°C$ $T_A = 150°C$	I_{DSS}	– –	10 10	nAdc μAdc
Gate Reverse Current ($V_{GS} = \pm 15$ Vdc, $V_{DS} = 0$)	I_{GSS}	–	± 10	pAdc
ON CHARACTERISTICS				
Gate Threshold Voltage ($V_{DS} = 10$ V, $I_D = 10\mu A$)	$V_{GS(Th)}$	1.0	5	Vdc
Drain-Source On-Voltage ($I_D = 2.0$ mA, $V_{GS} = 10$V)	$V_{DS(on)}$	–	1.0	V
On-State Drain Current ($V_{GS} = 10$ V, $V_{DS} = 10$ V)	$I_{D(on)}$	3.0	–	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance ($V_{DS} = 10$ V, $I_D = 2.0$ mA, f = 1.0 kHz)	$\lvert y_{fs} \rvert$	1000	–	μmho
Input Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 140 kHz)	C_{iss}	–	5.0	pF
Reverse Transfer Capacitance ($V_{DS} = 0$, $V_{GS} = 0$, f = 140 kHz)	C_{rss}	–	1.3	pF
Drain-Substrate Capacitance ($V_{D(SUB)} = 10$ V, f = 140 kHz)	$C_{d(sub)}$	–	5.0	pF
Drain-Source Resistance ($V_{GS} = 10$ V, $I_D = 0$, f = 1.0 kHz)	$r_{ds(on)}$	–	300	ohms
SWITCHING CHARACTERISTICS				
Turn-On Delay (Fig. 5)	t_{d1}	–	45	ns
Rise Time (Fig. 6)	t_r	–	65	ns
Turn-Off Delay (Fig. 7)	t_{d2}	–	60	ns
Fall Time (Fig. 8)	t_f	–	100	ns

($I_D = 2.0$ mAdc, $V_{DS} = 10$ Vdc, ($V_{GS} = 10$ Vdc) (See Figure 9; Times Circuit Determined))

FIG. 6.40

2N4351 Motorola n-channel enhancement-type MOSFET.

EXAMPLE 6.4 Using the data provided on the specification sheet of Fig. 6.40 and an average threshold voltage of $V_{GS(Th)} = 3$ V, determine:

a. The resulting value of k for the MOSFET.
b. The transfer characteristics.

Solution:

a. Eq. (6.16): $$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$

$$= \frac{3\text{ mA}}{(10\text{ V} - 3\text{ V})^2} = \frac{3\text{ mA}}{(7\text{ V})^2} = \frac{3 \times 10^{-3}}{49}\text{A/V}^2$$

$$= \mathbf{0.061 \times 10^{-3}\ A/V^2}$$

b. Eq. (6.15): $I_D = k(V_{GS} - V_T)^2$

$= 0.061 \times 10^{-3}(V_{GS} - 3\text{ V})^2$

For $V_{GS} = 5$ V,

$$I_D = 0.061 \times 10^{-3}(5\text{ V} - 3\text{ V})^2 = 0.061 \times 10^{-3}(2)^2$$
$$= 0.061 \times 10^{-3}(4) = 0.244\text{ mA}$$

For $V_{GS} = 8, 10, 12$, and 14 V, I_D will be 1.525, 3 (as defined), 4.94, and 7.38 mA, respectively. The transfer characteristics are sketched in Fig. 6.41.

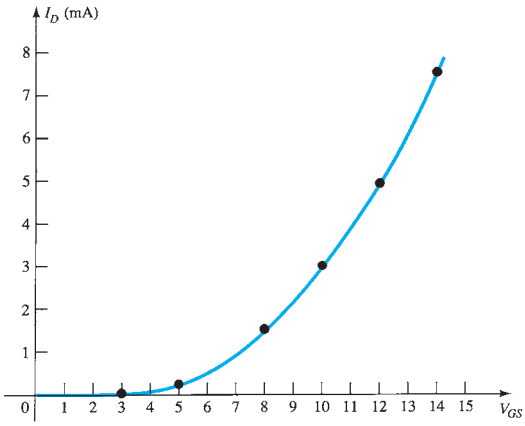


FIG. 6.41
Solution to Example 6.4.

6.9 MOSFET HANDLING

The thin SiO_2 layer between the gate and the channel of MOSFETs has the positive effect of providing a high-input-impedance characteristic for the device, but because of its extremely thin layer, it introduces a concern for its handling that was not present for the BJT or JFET transistors. There is often sufficient accumulation of static charge (picked up from the surroundings) to establish a potential difference across the thin layer that can break down the layer and establish conduction through it. It is therefore imperative to leave the shorting (or conduction) shipping foil (or ring) connecting the leads of the device together until the device is to be inserted in the system. The shorting ring prevents the possibility of applying a potential across any two terminals of the device. With the ring, the potential difference between any two terminals is maintained at 0 V. At the very least always touch ground to permit discharge of the accumulated static charge before handling the device, and always pick up the transistor by the casing.

There are often transients (sharp changes in voltage or current) in a network when elements are removed or inserted if the power is on. The transient levels can often be more than the device can handle, and therefore the power should always be off when network changes are made.

The maximum gate-to-source voltage is normally provided in the list of maximum ratings of the device. One method of ensuring that this voltage is not exceeded (perhaps by transient effects) for either polarity is to introduce two Zener diodes, as shown in Fig. 6.42. The Zeners are back to back to ensure protection for either polarity. If both are 30-V Zeners and a positive transient of 40 V appears, the lower Zener will "fire" at 30 V and the upper will turn on with a 0-V drop (ideally—for the positive "on" region of a semiconductor diode) across the other diode. The result is a maximum of 30 V for the gate-to-source voltage. One disadvantage introduced by the Zener protection is that the off resistance of a Zener diode is less than the input impedance established by the SiO_2 layer. The result is a reduction in input resistance, but even so, it is still high enough for most applications. So many of the discrete devices now have the Zener protection that some of the concerns listed above are not as troublesome. However, it is still best to be somewhat cautious when handling discrete MOSFET devices.

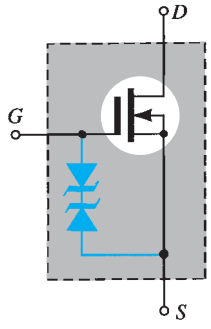


FIG. 6.42
Zener-protected MOSFET.

6.10 VMOS AND UMOS POWER MOSFETs

One of the disadvantages of the typical planar MOSFET is the reduced power handling (typically less than 1 W) and current levels compared with the broad range of bipolar transistors. However, through a vertical design such as shown for the VMOS MOSFET in Fig. 6.43a and the UMOS MOSFET in Fig. 6.43b, power and current levels have been increased along with higher switching speeds and reduced operating dissipation. All the elements of the planar MOSFET are present in the VMOS or UMOS MOSFETs—the metallic surface connection to the terminals of the device, the SiO_2 layer between the gate, and the *p*-type region between the drain and the source for the growth of the induced *n*-channel (enhancement-mode operation). The term *vertical* is due primarily to the fact that the channel is now formed in the *vertical* direction resulting in a vertical current direction rather than the horizontal direction for the planar device. However, the channel of Fig. 6.43a also has the appearance of a "V" cut in the semiconductor base, which often stands out as the reason for the name for the device. The construction of Fig. 6.43a is somewhat simplistic in nature, leaving out some of the transition levels of doping, but it does permit a description of the most important facets of its operation.

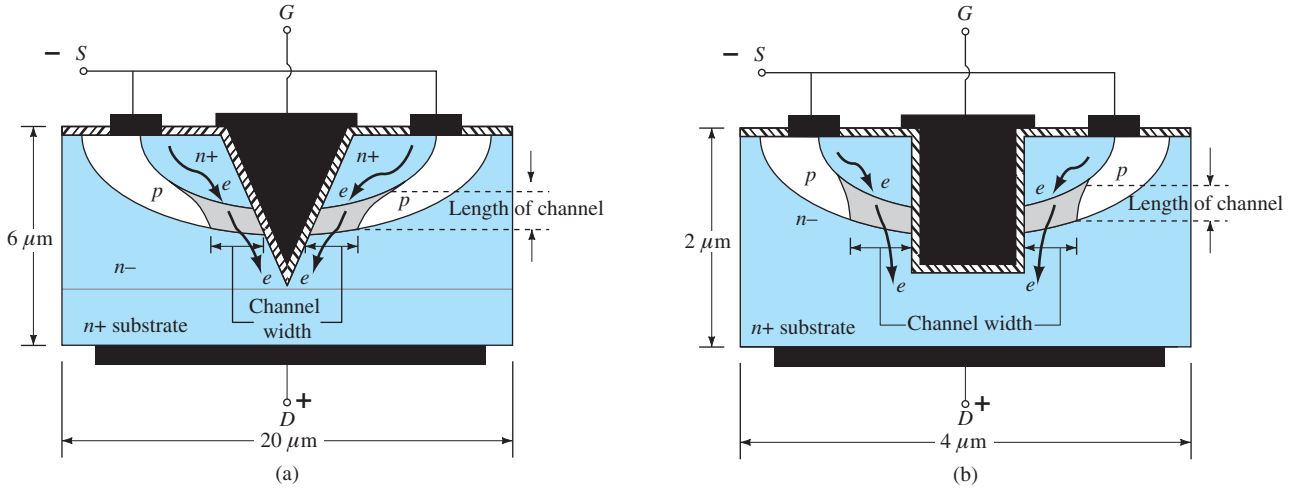


FIG. 6.43
(a) VMOS MOSFET; (b) UMOS MOSFET.

The application of a positive voltage to the drain and a negative voltage to the source with the gate at 0 V or some typical positive "on" level as shown in Fig. 6.43a results in the induced *n*-channel in the narrow *p*-type region of the device. The length of the channel is now defined by the vertical height of the *p*-region, which can be made significantly less than that of a channel using planar construction. On a horizontal plane the length of the channel is limited to 1 μm to 2 μm (1 μm = 10^{-6} m). Diffusion layers (such as the *p*-region of Fig. 6.43) can be controlled to small fractions of a micrometer. Since decreasing channel lengths result in reduced resistance levels, the power dissipation level of the device (power lost in the form of heat) at operating current levels will be reduced. In addition, the contact area between the channel and the n^+ region is greatly increased by the vertical mode construction, contributing to a further decrease in the resistance level and an increased area for current between the doping layers. There is also the existence of two conduction paths between drain and source, as shown in Fig. 6.43, to further contribute to a higher current rating. The net result is a device with drain currents that can reach the ampere levels with power levels exceeding 10 W.

The VMOS MOSFET was the first in line of vertical MOSFETs designed primarily to be used as power switches to control the operation of power supplies, low-voltage motor controllers, DC- to DC-convertors, flat-panel displays, and a host of applications in today's automobiles. Fundamentally, a good power switch should work at relatively low voltages (less than 200 V), has excellent high-speed characteristics, and low levels of "on" resistance to ensure minimum power losses during operation. Over time, a variety of other vertical designs began to surface to improve on the "V" construction of Fig. 6.43a. The delicate

etching required to establish the V groove resulted in difficulties establishing a consistent threshold voltage, and the sharp tip at the end of the channel created high electric fields, which affected the breakdown voltage of the MOSFET. The breakdown voltage is important because it is directly related to the "on" resistance. Increase the breakdown voltage and the "on" resistance begins to increase.

One improvement over the "V" design is the "U" groove or channel as appearing in Fig. 6.43b. The operation of this UMOS MOSFET (also called Trench MOSFET) is very similar to that of the VMOS MOSFET but with improved characteristics. First the fabrication process is preferred because the trench-etching process developed for memory cells in DRAMs can be utilized. The result is reduced widths in the neighborhood of 2–10 μm compared with the VMOS construction with widths in the 20–30 μm range. The channel width itself may be only 1 μm with a height of 2 μm. The "on" resistance is less using the trench approach because the channel length is decreased and the width of the current path is increased near the bottom of the trench. However, due to the large surface area required for the heavy current flow, there are capacitive effects that must be considered at frequencies beyond 100 kHz. The three that have to be considered are C_{GS}, C_{GD}, and C_{DS} (respectively referred to as C_{iss}, C_{rss}, and C_{oss} on specification sheets). For the UMOS MOSFET the gate-to-source capacitance at the input is the largest and typically thousands of pF.

The Toshiba line of UMOS-V MOSFETs has a drain current running from 11 A to 45 A with "on" resistances as low as 3.1–11.5 mΩ at 10 V. The maximum drain-to-source voltage for the units is 30 V, and the gate-to-source capacitance ranges from 1400 pF to 4600 pF. They are primarily used in flat-panel displays, desktop and mobile computers, and other portable electronic devices.

In general, therefore

Power MOSFETs have reduced "on" resistance levels and higher current and power ratings than planar MOSFETs.

An additional important characteristic of the vertical construction is:

Power MOSFETs have a positive temperature coefficient, which combats the possibility of thermal runaway.

If the temperature of a device should increase due to the surrounding medium or currents of the device, the resistance levels will increase, causing a reduction in drain current rather than an increase as encountered for a conventional device. Negative temperature coefficients result in decreased levels of resistance with increases in temperature, which fuel the growing current levels and result in further temperature instability and thermal runaway.

Another positive characteristic of the vertical configuration is:

The reduced charge storage levels result in faster switching times for vertical construction compared to those for conventional planar construction.

In fact, VMOS and UMOS devices typically have switching times less than one-half that encountered for the typical BJT transistor.

6.11 CMOS

A very effective logic circuit can be established by constructing a *p*-channel and an *n*-channel MOSFET on the same substrate as shown in Fig. 6.44. Note the induced *p*-channel on the left and the induced *n*-channel on the right for the *p*- and *n*-channel devices, respectively. The configuration is referred to as a *complementary MOSFET* arrangement (CMOS); it has extensive applications in computer logic design. The relatively high input impedance, fast switching speeds, and lower operating power levels of the CMOS configuration have resulted in a whole new discipline referred to as *CMOS logic design.*

One very effective use of the complementary arrangement is as an inverter, as shown in Fig. 6.45. As introduced for switching transistors, an inverter is a logic element that "inverts" the applied signal. That is, if the logic levels of operation are 0 V (0-state) and 5 V (1-state), an input level of 0 V will result in an output level of 5 V, and vice versa. Note in Fig. 6.45 that both gates are connected to the applied signal and both drain to the output V_o. The source of the *p*-channel MOSFET (Q_2) is connected directly to the applied voltage V_{SS}, whereas the source of the *n*-channel MOSFET (Q_1) is connected to ground. For the logic levels defined above, the application of 5 V at the input should result in approximately 0 V

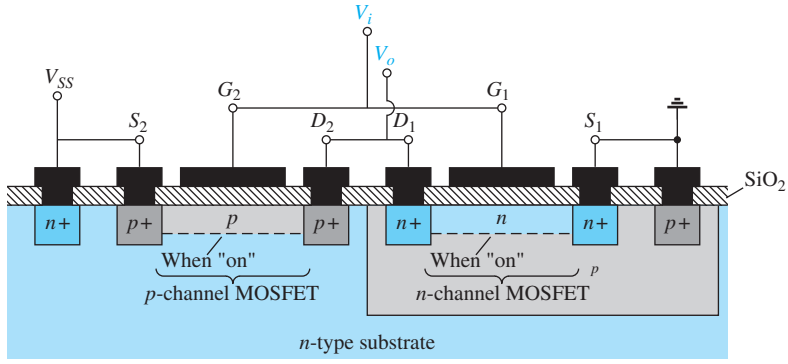


FIG. 6.44
CMOS with the connections indicated in Fig. 6.45.

at the output. With 5 V at V_i (with respect to ground), $V_{GS_1} = V_i$, and Q_1 is "on," resulting in a relatively low resistance between drain and source as shown in Fig. 6.46. Since V_i and V_{SS} are at 5 V, $V_{GS_2} = 0$ V, which is less than the required V_T for the device, resulting in an "off" state. The resulting resistance level between drain and source is quite high for Q_2, as shown in Fig. 6.46. A simple application of the voltage-divider rule will reveal that V_o is very close to 0 V, or the 0-state, establishing the desired inversion process. For an applied voltage V_i of 0 V (0-state), $V_{GS_1} = 0$ V, and Q_1 will be "off" with $V_{SS_2} = -5$ V, turning on the *p*-channel MOSFET. The result is that Q_2 will present a small resistance level, Q_1 a high resistance, and $V_o = V_{SS} = 5$ V (the 1-state). Since the drain current that flows for either case is limited by the "off" transistor to the leakage value, the power dissipated by the device in either state is very low. Additional comment on the application of CMOS logic is presented in Chapter 13.

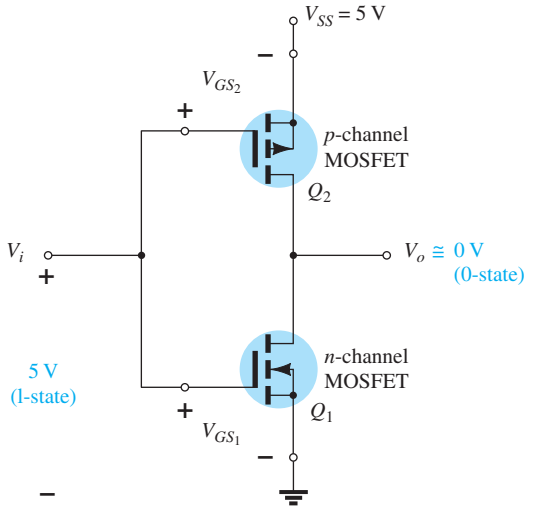


FIG. 6.45
CMOS inverter.

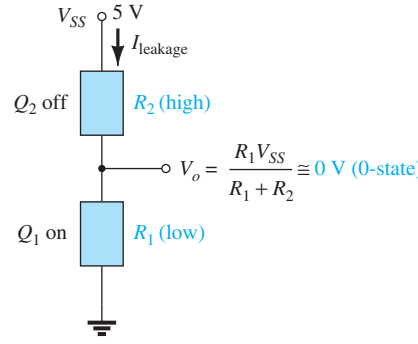


FIG. 6.46
Relative resistance levels for $V_i = 5$ V (1-state).

6.12 MESFETs

As noted in earlier discussions, the use of GaAs in the construction of semiconductor devices has been around for quite a few decades. Unfortunately, however, the manufacturing costs, lower resulting density in ICs, and production problems have kept it from prominence in the industry until the last few years. The need for high-speed devices and improved production methods in recent years have established a strong demand for large-scale integrated circuits using GaAs.

Although the Si MOSFETs just described can be made using GaAs instead, it is a more difficult manufacturing process due to diffusion problems. However, the production of FETs using a Schottky barrier (discussed in detail in Chapter 16) at the gate can be done quite efficiently:

Schottky barriers are barriers established by depositing a metal such as tungsten on an n-type channel.

The use of a Schottky barrier at the gate is the major difference from the depletion- and enhancement-type MOSFETs, which employ an insulating barrier between the metal contact and the *n*-type channel. The absence of an insulating layer reduces the distance between the metal contact surface of the gate and the semiconductor layer, resulting in a lower level of stray capacitance between the two surfaces (recall the effect of distance between the plates of a capacitor and its terminal capacitance). The result of the lower capacitance level is a reduced sensitivity to high frequencies (forming a shorting effect), which further supports the high mobility of carriers in the GaAs material.

The presence of a metal–semiconductor junction is the reason such FETs are called *metal–semiconductor field-effect transistors* (MESFETs). The basic construction of a MESFET is provided in Fig. 6.47. Note in Fig. 6.47 that the gate terminal is connected directly to a metallic conductor lying directly against the *n*-channel between the source and drain terminals. The only difference from the depletion-type MOSFET construction is the absence of the insulator at the gate. When a negative voltage is applied to the gate, it will attract free negative carriers (electrons) in the channel to the metal surface, reducing the number of carriers in the channel. The result is a reduced drain current, as shown in Fig. 6.48, for increasing values of negative voltage at the gate terminal. For positive voltages at the gate, additional electrons will be attracted into the channel and the current will rise as shown by the drain characteristics of Fig. 6.48. The fact that the drain and transfer characteristics of the depletion-type MESFET are so similar to those of the depletion-type MOSFET results in analysis techniques similar to those applied to depletion-type MOSFETs. The defined polarities and current directions for the MESFET are provided in Fig. 6.49 along with the symbol for the device.

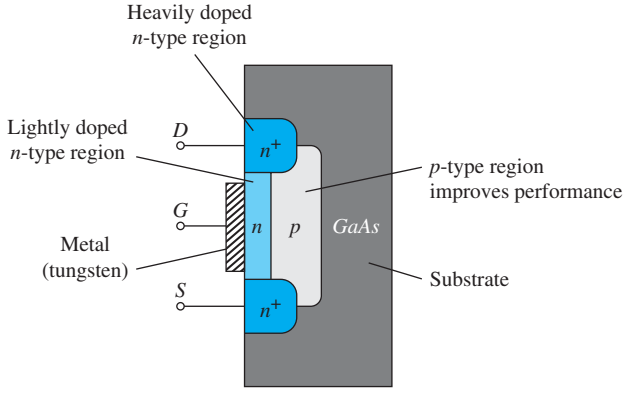


FIG. 6.47
Basic construction of an n-channel MESFET.

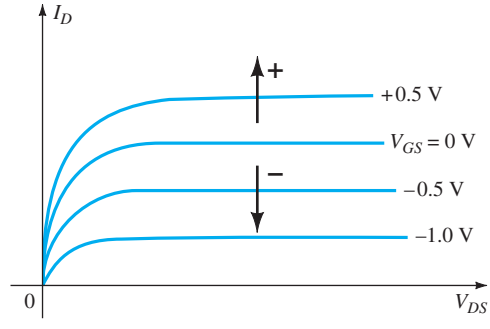


FIG. 6.48
Characteristics of an n-channel MESFET.

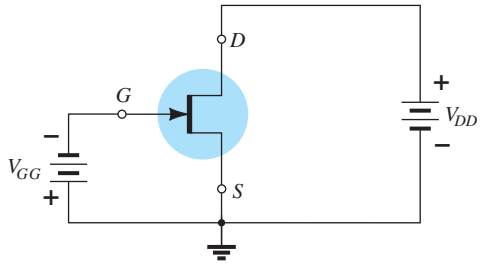


FIG. 6.49
Symbol and basic biasing arrangement for an n-channel MESFET.

There are also enhancement-type MESFETs with a construction the same as in Fig. 6.47 but without the initial channel, as shown in Fig. 6.50 along with its graphic symbol. The response and characteristics are essentially the same as for the enhancement-type MOSFET. However, due to the Schottky barrier at the gate, the positive threshold voltage is limited to 0 V to about 0.4 V because the "turn-on" voltage for a Schottky barrier diode is about 0.7 V. Again, the analysis techniques applied to enhancement-type MESFETs are similar to those employed for enhancement-type MOSFETs.

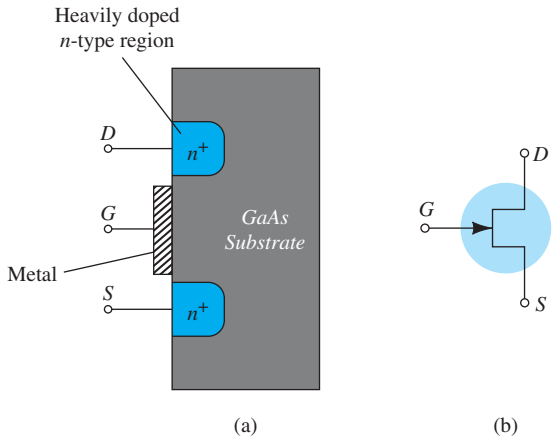


FIG. 6.50
Enhancement-type MESFET: (a) construction; (b) symbol.

It is important to realize, however, that the channel must be an *n*-type material in a MESFET. The mobility of holes in GaAs is relatively low compared to that of the negatively charged carriers, losing the advantage of using GaAs for high-speed applications. The result is:

Depletion-type and enhancement-type MESFETs are made with an n-channel between the drain and the source, and therefore only n-type MESFETs are commercially available.

For both types of MESFETs the channel length (identified in Figs. 6.47 and 6.50) should be made as short as possible for high-speed applications. The length is typically between 0.1 μm and 1 μm.

6.13 SUMMARY TABLE

Since the transfer curves and some important characteristics vary from one type of FET to another, Table 6.3 was developed to clearly display the differences from one device to the next. A clear understanding of all the curves and parameters of the table will provide a sufficient background for the dc and ac analyses to follow. Take a moment to ensure that each curve is recognizable and its derivation understood, and then establish a basis for comparison of the levels of the important parameters of R_i and C_i for each device.

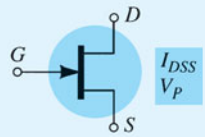
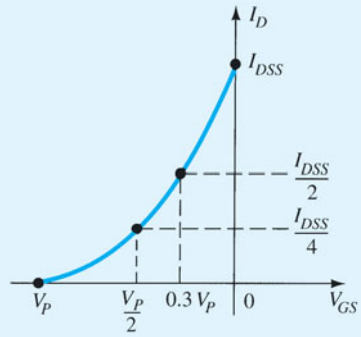
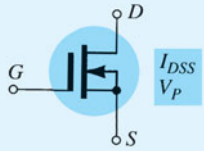
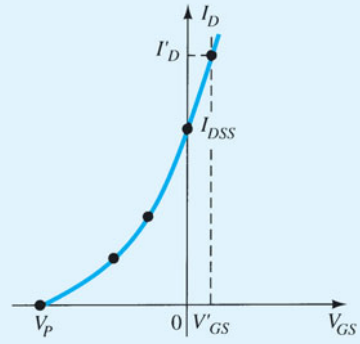
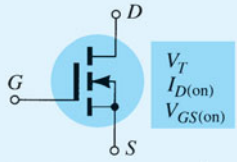
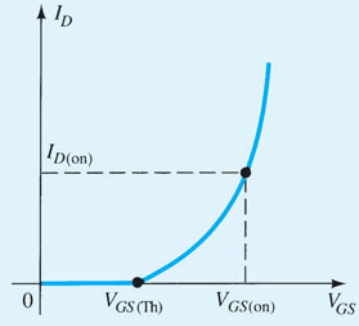
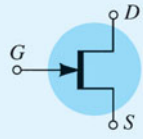
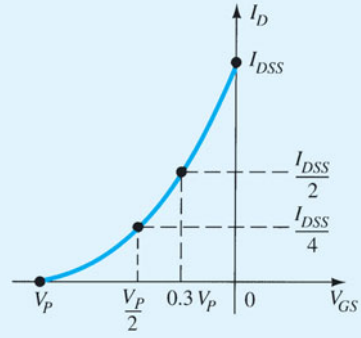
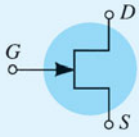
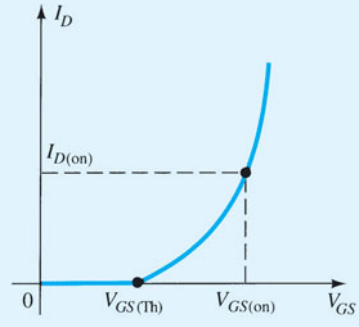
6.14 SUMMARY

Important Conclusions and Concepts

1. A **current-controlled device** is one in which a current defines the operating conditions of the device, whereas a **voltage-controlled device** is one in which a particular voltage defines the operating conditions.
2. The JFET can actually be used as a **voltage-controlled resistor** because of a unique sensitivity of the drain-to-source impedance to the gate-to-source voltage.
3. The **maximum current** for any JFET is labeled I_{DSS} and occurs when $V_{GS} = 0$ V.
4. The **minimum current** for a JFET occurs at pinch-off defined by $V_{GS} = V_P$.
5. The relationship between the drain current and the gate-to-source voltage of a JFET is a **nonlinear one** defined by Shockley's equation. As the current level approaches I_{DSS}, the sensitivity of I_D to changes in V_{GS} increases significantly.

TABLE 6.3

Field Effect Transistors

Type	Symbol and Basic Relationships	Transfer Curve	Input Resistance and Capacitance
JFET (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 100\text{ M}\Omega$ C_i: (1 – 10) pF
MOSFET depletion type (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 10^{10}\ \Omega$ C_i: (1 – 10) pF
MOSFET enhancement type (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = k\,(V_{GS} - V_{GS\,(Th)})^2$ $k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS\,(Th)})^2}$		$R_i > 10^{10}\ \Omega$ C_i: (1 – 10) pF
MESFET depletion type (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ $I_G = 0\text{ A}, I_D = I_S$		$R_i > 10^{12}\ \Omega$ C_i: (1 – 5) pF
MESFET enhancement type (*n*-channel)	 $I_D = k\,(V_{GS} - V_{GS\,(Th)})^2$ $k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS\,(Th)})^2}$		$R_i > 10^{12}\ \Omega$ C_i: (1 – 5) pF

6. The transfer characteristics (I_D versus V_{GS}) are characteristics **of the device itself** and are not sensitive to the network in which the JFET is employed.
7. When $V_{GS} = V_P/2$, $I_D = I_{DSS}/4$; and at a point where $I_D = I_{DSS}/2$, $V_{GS} \cong 0.3$ V.
8. Maximum operating conditions are determined by the **product** of the drain-to-source voltage and the drain current.
9. MOSFETs are available in one of two types: **depletion and enhancement**.
10. The depletion-type MOSFET has the same transfer characteristics as a JFET for drain currents up to the I_{DSS} level. At this point the characteristics of a depletion-type MOSFET **continue to levels above** I_{DSS}, whereas those of the JFET will end.
11. The arrow in the symbol of *n*-channel JFETs or MOSFETs will **always point in to the center of the symbol**, whereas those of a *p*-channel device will always point out of the center of the symbol.
12. The transfer characteristics of an enhancement-type MOSFET are **not defined by Shockley's equation** but rather by a nonlinear equation controlled by the gate-to-source voltage, the threshold voltage, and a constant k defined by the device employed. The resulting plot of I_D versus V_{GS} **rises exponentially with incrseasing values of** V_{GS}.
13. Always handle MOSFETs with **additional care** due to the static electricity that exists in places we might least suspect. Do not remove any shorting mechanism between the leads of the device until it is installed.
14. A CMOS (complementary MOSFET) device employs a unique **combination of a *p*-channel and an *n*-channel MOSFET** with a single set of external leads. It has the advantages of a very high input impedance, fast switching speeds, and low operating power levels, all of which make it very useful in logic circuits.
15. A depletion-type MESFET includes a metal–semiconductor junction, resulting in characteristics that **match those of an *n*-channel depletion-type JFET**. Enhancement-type MESFETs have the same characteristics as enhancement-type MOSFETs. The result of this similarity is that the **same type of dc and ac analysis techniques can be applied to MESFETs as was applied to JFETs**.

Equations

JFET:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}|_{V_{GS}=0\ V}, \quad I_D = 0\ \text{mA}|_{V_{GS}=V_P}, \quad I_D = \left.\frac{I_{DSS}}{4}\right|_{V_{GS}=V_P/2}, \quad V_{GS} \cong 0.3V_P|_{I_D=I_{DSS}/2}$$

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$P_D = V_{DS}I_D$$

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$

MOSFET (enhancement):

$$I_D = k(V_{GS} - V_T)^2$$

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_T)^2}$$

6.15 COMPUTER ANALYSIS

PSpice Windows

The characteristics of an *n*-channel JFET can be displayed using the same procedure employed for the transistor in Section 3.13. The series of curves across the characteristics plotted against various values of voltage requires a nested sweep within the sweep for the drain-to-source voltage. The required configuration of Fig. 6.51 is constructed using procedures described in the previous chapters. In particular, note the complete absence of resistors since the input impedance is assumed to be infinite, resulting in a gate current of 0 A.

The JFET is found under **Part** in the **Place Part** dialog box. It can be called up by simply typing in **JFET** in the provided space under the **Part** heading. Once in place, a single click on the symbol followed by **Edit-PSpice Model** will result in the **PSpice Model Editor Demo** dialog box. Note that **Beta** is equal to 1.304 mA/V^2 and **Vto** is −3 V. For the junction field effect transistor **Beta** is defined by

$$\text{Beta} = \frac{I_{DSS}}{V_P{}^2} \quad (\text{A/V}^2) \tag{6.17}$$

The parameter **Vto** defines $V_{GS} = V_P = -3$ V as the pinch-off voltage. Using Eq. (6.17), one can solve for I_{DSS} and find that it is about 11.37 mA. Once the plots are obtained one can check whether both of these parameters are accurately defined by the characteristics. With the network established, select a **New Simulation** to obtain the **New Simulation** dialog box. Using **OrCAD 6-1** as the name followed by **Create** results in the **Simulation Settings** dialog box, in which **DC Sweep** is selected under the **Analysis type** heading. The **Sweep variable** is set as a **Voltage source** with the **Name VDD**. The **Start Value** is 0 V, the **End Value** is 10 V, and the **Increment** is 0.01 V. Now select **Secondary Sweep** and apply the **Name VGG** with a **Start Value** of 0 V, an **End Value** of −5 V, and an **Increment** of −1 V. Finally, the **Secondary Sweep** must be enabled by ensuring the check appears in the box to the left of the listing, followed by an **OK** to leave the dialog box. A **Simulation**, and the **SCHEMATIC** screen will appear with a horizontal axis labeled **VDD** extending from 0 V to 10 V. Continue with the sequence **Trace-Add Trace** to obtain the **Add Traces** dialog box, and select **ID(J1)** to obtain the characteristics of Fig. 6.52. Note in particular that I_{DSS} is very close to 11.7 mA as predicted based on the value of Beta. Also note that cutoff does occur at $V_{GS} = V_P = -3$ V.

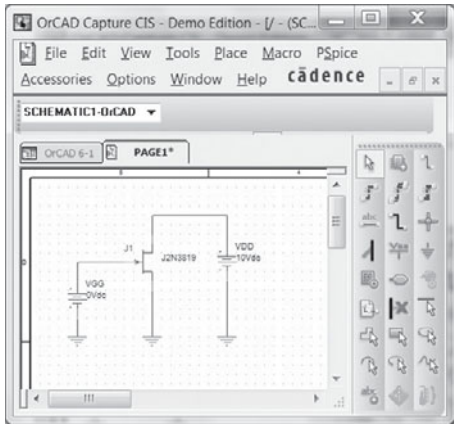


FIG. 6.51
Network used to obtain the characteristics of the n-channel J2N3819 JFET.

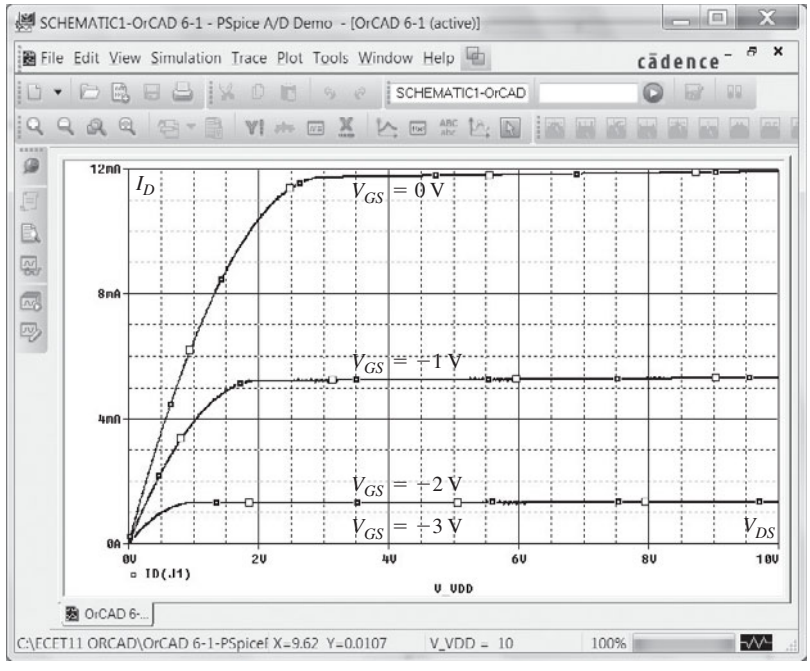


FIG. 6.52
Drain characteristics for the n-channel J2N3819 JFET of Fig. 6.51.

The transfer characteristics can be obtained by setting up a **New Simulation** that has a single sweep since there is only one curve to plot. Once **DC Sweep** is again selected, the **Name** is **VGG** with a **Start Value** of −3 V, an **End Value** of 0 V, and an **Increment** of 0.01 V. Since there is no need for a secondary nested sweep, select **OK**, and the simulation is performed. When the graph appears, select **Trace-Add Trace-ID(J1)** to obtain the transfer characteristics of Fig. 6.53. Note how the axis is set with the −3 V to the far left and the 0 V to the far right. Again, I_{DSS} is very close to the predicted 11.7 mA and $V_P = -3$ V.

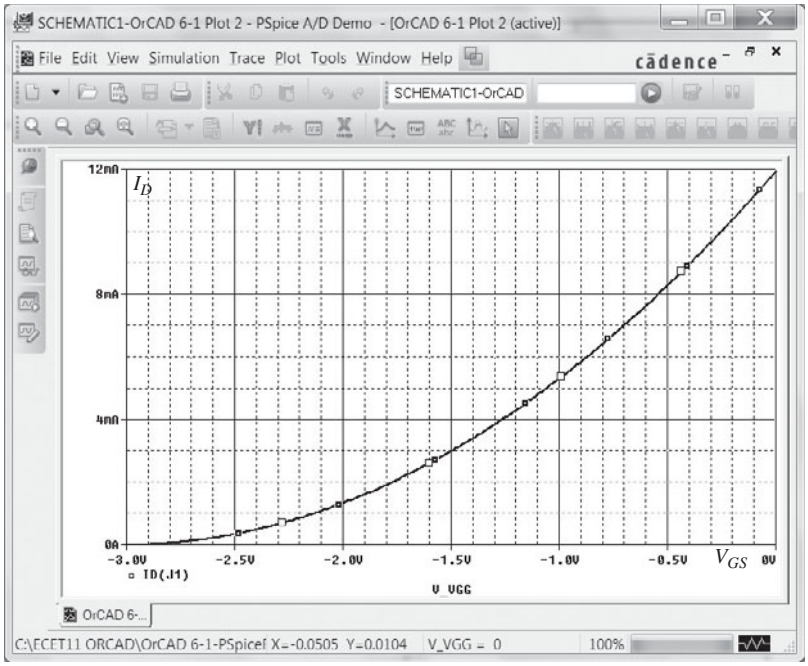


FIG. 6.53
Transfer characteristics for the n-channel J2N3819 JFET of Fig. 6.51.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

6.2 Construction and Characteristics of JFETs

1. **a.** Draw the basic construction of a *p*-channel JFET.
   b. Apply the proper biasing between drain and source and sketch the depletion region for $V_{GS} = 0$ V.
2. Using the characteristics of Fig. 6.11, determine I_D for the following levels of V_{GS} (with $V_{DS} > V_P$):
   a. $V_{GS} = 0$ V.
   b. $V_{GS} = -1$ V.
   c. $V_{GS} = -1.5$ V.
   d. $V_{GS} = -1.8$ V.
   e. $V_{GS} = -4$ V.
   f. $V_{GS} = -6$ V.
3. Using the results of problem 2 plot the transfer characteristics of I_D vs. V_{GS}.
4. **a.** Determine V_{DS} for $V_{GS} = 0$ V and $I_D = 6$ mA using the characteristics of Fig. 6.11.
   b. Using the results of part (a), calculate the resistance of the JFET for the region $I_D = 0$ to 6 mA for $V_{GS} = 0$ V.
   c. Determine V_{DS} for $V_{GS} = -1$ V and $I_D = 3$ mA.
   d. Using the results of part (c), calculate the resistance of the JFET for the region $I_D = 0$ to 3 mA for $V_{GS} = -1$ V.
   e. Determine V_{DS} for $V_{GS} = -2$ V and $I_D = 1.5$ mA.
   f. Using the results of part (e), calculate the resistance of the JFET for the region $I_D = 0$ to 1.5 mA for $V_{GS} = -2$ V.
   g. Defining the result of part (b) as r_o, determine the resistance for $V_{GS} = -1$ V using Eq. (6.1) and compare with the results of part (d).
   h. Repeat part (g) for $V_{GS} = -2$ V using the same equation, and compare the results with part (f).
   i. Based on the results of parts (g) and (h), does Eq. (6.1) appear to be a valid approximation?
5. Using the characteristics of Fig. 6.11:
   a. Determine the difference in drain current (for $V_{DS} > V_P$) between $V_{GS} = 0$ V and $V_{GS} = -1$ V.
   b. Repeat part (a) between $V_{GS} = -1$ and -2 V.
   c. Repeat part (a) between $V_{GS} = -2$ and -3 V.
   d. Repeat part (a) between $V_{GS} = -3$ and -4 V.
   e. Is there a marked change in the difference in current levels as V_{GS} becomes increasingly negative?

f. Is the relationship between the change in V_{GS} and the resulting change in I_D linear or nonlinear? Explain.

6. What are the major differences between the collector characteristics of a BJT transistor and the drain characteristics of a JFET transistor? Compare the units of each axis and the controlling variable. How does I_C react to increasing levels of I_B versus changes in I_D to increasingly negative values of V_{GS}? How does the spacing between steps of I_B compare to the spacing between steps of V_{GS}? Compare $V_{C_{sat}}$ to V_P in defining the nonlinear region at low levels of output voltage.

7. a. Describe in your own words why I_G is effectively 0 A for a JFET transistor.
b. Why is the input impedance to a JFET so high?
c. Why is the terminology *field effect* appropriate for this important three-terminal device?

8. Given $I_{DSS} = 12$ mA and $|V_P| = 6$ V, sketch a probable distribution of characteristic curves for the JFET (similar to Fig. 6.11).

9. In general, comment on the polarity of the various voltages and direction of the currents for an *n*-channel JFET versus a *p*-channel JFET.

6.3 Transfer Characteristics

10. Given the characteristics of Fig. 6.54:
a. Sketch the transfer characteristics directly from the drain characteristics.
b. Using Fig. 6.54 to establish the values of I_{DSS} and V_P, sketch the transfer characteristics using Shockley's equation.
c. Compare the characteristics of parts (a) and (b). Are there any major differences?

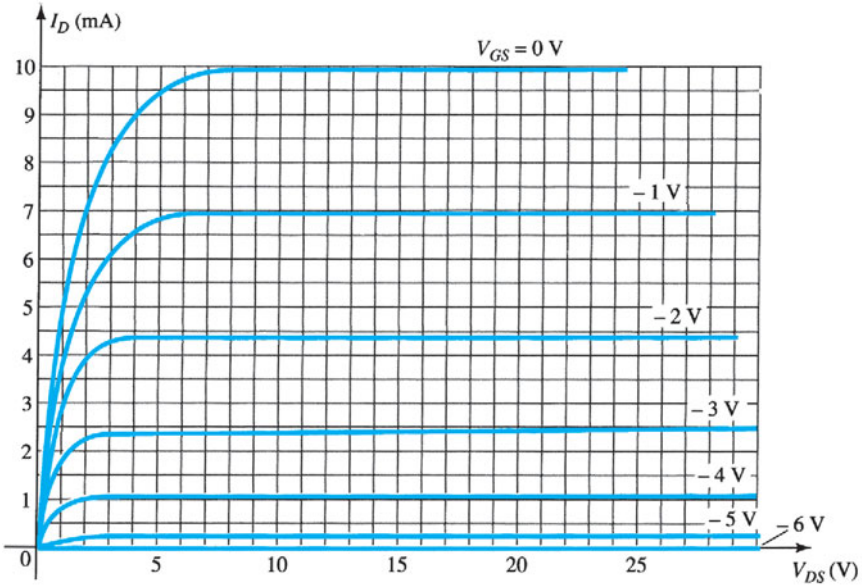


FIG. 6.54
Problems 10 and 20.

11. a. Given $I_{DSS} = 12$ mA and $V_P = -4$ V, sketch the transfer characteristics for the JFET transistor.
b. Sketch the drain characteristics for the device of part (a).

12. Given $I_{DSS} = 9$ mA and $V_P = -4$ V, determine I_D when:
a. $V_{GS} = 0$ V.
b. $V_{GS} = -2$ V.
c. $V_{GS} = -4$ V.
d. $V_{GS} = -6$ V.

13. Given $I_{DSS} = 16$ mA and $V_P = -5$ V, sketch the transfer characteristics using the data points of Table 6.1. Determine the value of I_D at $V_{GS} = -3$ V from the curve, and compare it to the value determined using Shockley's equation. Repeat the above for $V_{GS} = -1$ V.

14. For a particular JFET if $I_D = 4$ mA when $V_{GS} = -3$ V, determine V_P if $I_{DSS} = 12$ mA.

15. Given $I_{DSS} = 6$ mA and $V_P = -4.5$ V:
a. Determine I_D at $V_{GS} = -2$ and -3.6 V.
b. Determine V_{GS} at $I_D = 3$ and 5.5 mA.

16. Given a *Q*-point of $I_{D_Q} = 3$ mA and $V_{GS} = -3$ V, determine I_{DSS} if $V_P = -6$ V.

17. A p-channel JFET has device parameters of $I_{DSS} = 7.5$ mA and $V_P = 4$ V. Sketch the transfer characteristics.

6.4 Specification Sheets (JFETs)

18. Define the region of operation for the 2N5457 JFET of Fig. 6.20 using the range of I_{DSS} and V_P provided. That is, sketch the transfer curve defined by the maximum I_{DSS} and V_P and the transfer curve for the minimum I_{DSS} and V_P. Then, shade in the resulting area between the two curves.
19. For the 2N5457 JFET of Fig. 6.20, what is the power rating at a typical operating temperature of 45°C using the 5.0 mW/°C derating factor.
20. Define the region of operation for the JFET of Fig. 6.54 if $V_{DS_{max}} = 30$ V and $P_{D_{max}} = 100$ mW.

6.5 Instrumentation

21. Using the characteristics of Fig. 6.22, determine I_D at $V_{GS} = -0.7$ V and $V_{DS} = 10$ V.
22. Referring to Fig. 6.22, is the locus of pinch-off values defined by the region of $V_{DS} < |V_P| = 3$ V?
23. Determine V_P for the characteristics of Fig. 6.22 using I_{DSS} and I_D at some value of V_{GS}. That is, simply substitute into Shockley's equation and solve for V_P. Compare the result to the assumed value of -3 V from the characteristics.
24. Using $I_{DSS} = 9$ mA and $V_P = -3$ V for the characteristics of Fig. 6.22, calculate I_D at $V_{GS} = -1$ V using Shockley's equation and compare to the level in Fig. 6.22.
25. **a.** Calculate the resistance associated with the JFET of Fig. 6.22 for $V_{GS} = 0$ V from $I_D = 0$ mA to 4 mA.
    b. Repeat part (a) for $V_{GS} = -0.5$ V from $I_D = 0$ to 3 mA.
    c. Assigning the label r_o to the result of part (a) and r_d to that of part (b), use Eq. (6.1) to determine r_d and compare to the result of part (b).

6.7 Depletion-Type MOSFET

26. **a.** Sketch the basic construction of a p-channel depletion-type MOSFET.
    b. Apply the proper drain-to-source voltage and sketch the flow of electrons for $V_{GS} = 0$ V.
27. In what ways is the construction of a depletion-type MOSFET similar to that of a JFET? In what ways is it different?
28. Explain in your own words why the application of a positive voltage to the gate of an n-channel depletion-type MOSFET will result in a drain current exceeding I_{DSS}.
29. Given a depletion-type MOSFET with $I_{DSS} = 6$ mA and $V_P = -3$ V, determine the drain current at $V_{GS} = -1, 0, 1$, and 2 V. Compare the difference in current levels between -1 V and 0 V with the difference between 1 V and 2 V. In the positive V_{GS} region, does the drain current increase at a significantly higher rate than for negative values? Does the I_D curve become more and more vertical with increasing positive values of V_{GS}? Is there a linear or a nonlinear relationship between I_D and V_{GS}? Explain.
30. Sketch the transfer and drain characteristics of an n-channel depletion-type MOSFET with $I_{DSS} = 12$ mA and $V_P = -8$ V for a range of $V_{GS} = -V_P$ to $V_{GS} = 1$ V.
31. Given $I_D = 14$ mA and $V_{GS} = 1$ V, determine V_P if $I_{DSS} = 9.5$ mA for a depletion-type MOSFET.
32. Given $I_D = 4$ mA at $V_{GS} = -2$ V, determine I_{DSS} if $V_P = -5$ V.
33. Using an average value of 2.9 mA for the I_{DSS} of the 2N3797 MOSFET of Fig. 6.31, determine the level of V_{GS} that will result in a maximum drain current of 20 mA if $V_P = -5$ V.
34. If the drain current for the 2N3797 MOSFET of Fig. 6.31 is 8 mA, what is the maximum permissible value of V_{DS} utilizing the maximum power rating?

6.8 Enhancement-Type MOSFET

35. **a.** What is the significant difference between the construction of an enhancement-type MOSFET and a depletion-type MOSFET?
    b. Sketch a p-channel enhancement-type MOSFET with the proper biasing applied ($V_{DS} > 0$ V, $V_{GS} > V_T$) and indicate the channel, the direction of electron flow, and the resulting depletion region.
    c. In your own words, briefly describe the basic operation of an enhancement-type MOSFET.
36. **a.** Sketch the transfer and drain characteristics of an n-channel enhancement-type MOSFET if $V_T = 3.5$ V and $k = 0.4 \times 10^{-3}$ A/V^2.
    b. Repeat part (a) for the transfer characteristics if V_T is maintained at 3.5 V but k is increased by 100% to 0.8×10^{-3} A/V^2.

37. **a.** Given $V_{GS(Th)} = 4$ V and $I_{D(on)} = 4$ mA at $V_{GS(on)} = 6$ V, determine k and write the general expression for I_D in the format of Eq. (6.15).
b. Sketch the transfer characteristics for the device of part (a).
c. Determine I_D for the device of part (a) at $V_{GS} = 2, 5$, and 10 V.

38. Given the transfer characteristics of Fig. 6.55, determine V_T and k and write the general equation for I_D.

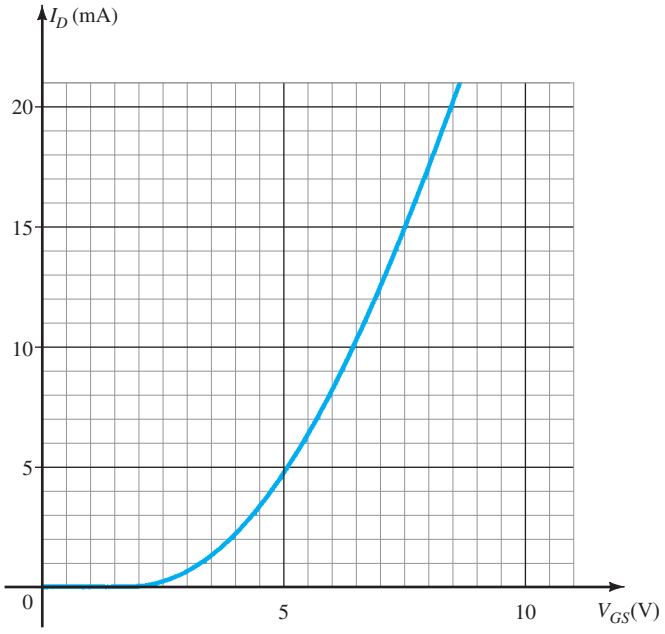


FIG. 6.55
Problem 38.

39. Given $k = 0.4 \times 10^{-3}$ A/V^2 and $I_{D(on)} = 3$ mA with $V_{GS(on)} = 4$ V, determine V_T.

40. The maximum drain current for the 2N4351 n-channel enhancement-type MOSFET is 30 mA. Determine V_{GS} at this current level if $k = 0.06 \times 10^{-3}$ A/V^2 and V_T is the maximum value.

41. Does the current of an enhancement-type MOSFET increase at about the same rate as a depletion-type MOSFET for the conduction region? Carefully review the general format of the equations, and if your mathematics background includes differential calculus, calculate dI_D/dV_{GS} and compare its magnitude.

42. Sketch the transfer characteristics of a p-channel enhancement-type MOSFET if $V_T = -5$ V and $k = 0.45 \times 10^{-3}$ A/V^2.

43. Sketch the curve of $I_D = 0.5 \times 10^{-3}(V_{GS}^2)$ and $I_D = 0.5 \times 10^{-3}(V_{GS} - 4)^2$ for V_{GS} from 0 V to 10 V. Does $V_T = 4$ V have a significant effect on the level of I_D for this region?

6.10 VMOS and UMOS Power MOSFETs

44. **a.** Describe in your own words why the VMOS FET can withstand a higher current and power rating than devices constructed with standard techniques.
b. Why do VMOS FETs have reduced channel resistance levels?
c. Why is a positive temperature coefficient desirable?

45. What are the relative advantages of the UMOS technology over the VMOS technology?

6.11 CMOS

***46.** **a.** Describe in your own words the operation of the network of Fig. 6.45 with $V_i = 0$ V.
b. If the "on" MOSFET of Fig. 6.45 (with $V_i = 0$ V) has a drain current of 4 mA with $V_{DS} = 0.1$ V, what is the approximate resistance level of the device? If $I_D = 0.5\ \mu$A for the "off" transistor, what is the approximate resistance of the device? Do the resulting resistance levels suggest that the desired output voltage level will result?

47. Research CMOS logic at your local or college library, and describe the range of applications and basic advantages of the approach.