California State University, Sacramento
EEE/CPE 64, Section 05, Introduction to Logic Design, Spring 2022

Laboratory Manual

Contact Information:
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Class Day/Time: Thursdays 18:00-20:40
Classroom: Riverside Hall 3005

Parts List: (Mfg. brands and part numbers may be different than the parts in the kit)

SKU	Mfg	MfgNo	Description
2238397	Jameco Benchpro	DT-182	DMM,3.5 MINI MANUAL RANGE METER,0.2-500VDC,.002-10A,200-2Moh
2309167	Jameco Benchpro	GPL-105	PLIER,NEEDLE NOSE, 5.75",2"SMOOTH OVAL JAWS
2127718	Jameco Valuepro	WJW-70B-5	WIRE JUMPER KIT 22AWG,70PCS, 14 LENGTHS,10 COLORS,5 EA LEN
2157693	Goldtool	BB-801	BREADBOARD,3.25"x2.125",400PNT LOW COST ALTERNATIVE TO 20601
2157706	Goldtool	BB-102	BREADBOARD,6.5"x2.125",830PNT LOW COST ALTERNATIVE TO 20723
690865	Jameco Valuepro	CF1/4W102JRC	RES,CF,1K OHM,1/4 WATT,5%, (10 BAG)
690742	Jameco Valuepro	CF1/4W331JRC	RES,CF,330 OHM,1/4 WATT,5%, (10 BAG)
690785	Jameco Valuepro	CF1/4W471JRC	RES,CF,470 OHM,1/4 WATT,5%, (10 BAG)
691585	Jameco Valuepro	CF1/4W105JRC	RES,CF,1.0M OHM,1/4 WATT,5%, (10 BAG)
333973	Jameco Valuepro	UT1871-81-M1-R	LED,RED,643NM,T-1 3/4, 75MCD,2.2V,V/A25,(10)
34761	Jameco Valuepro	LG3330	LED,GRN,GRN DIF,T1-3/4, 565nm,1.7Vf,30mcd V/A36(10)
2192384	Jameco Valuepro	3450XBB-4	SWITCH,SLIDE,SPDT,ON-ON,PCB 125VAC@0.3A,L/S 3MM, 3-PIN
12634	Major Brands	CD4011B	IC,CD4011,DIP-14, QUAD 2-INPUT NAND GATE
13354	Major Brands	CD4081B	IC,CD4081B,QUAD 2-INPUT AND GATE,DIP-14(MC14081BCP)
12562	Major Brands	CD4001B	IC,CD4001B,QUAD 2-INPUT NOR GATE(MC14001BCP)DIP-14
47466	Major Brands	74LS32	IC,74LS32N,DIP-14, QUAD 2-INPUT POS. OR GATE
48961	Major Brands	74S86	IC,74S86N,QUAD 2-INPUT EXCLUS.OR GATE SCHOTTKY,14-DIP
46316	Major Brands	74LS04	IC,74LS04N,DIP-14,HEX INVERTER
12677	Major Brands	CD4013B	IC,CD4013,DIP-14, DUAL D-TYPE FLIP-FLOP
46922	Major Brands	74LS173	IC,74LS173N,DIP-16,4BIT D-TYPE REGISTER W/3-STATE OUTPUT
64696	Major Brands	74S194	IC,74S194,4-BIT BI-DIRECTIONAL SHIFT REGISTER,16-DIP
119011	Jameco Valuepro	01-805-R	SWITCH,PB,TACT,SPST,OFF-(ON) 15VDC/20MA
2157853	DFRobot	DFR0140	BREADBOARD POWER SUPPLY,5/3.3V 6-12VIN,5/3.3VOUT,500mA MAX
2230045	Phihong	PSC12R-090	PWR SPLY,SW,WALL,INTERCHAN,9VDC/1.11A,2.1X5.5mm,V CEC
229155	Phihong	RPA	CLIP,WALL TRANS,USA VERSION(1)

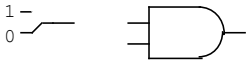
Lab Schedule:

Lab	Date	Day	Time	Lab Topic	Points Towards Grade
0	January 27, 2022	Thr	18:00-20:40	No lab assignment submission. Obtain part kits and install LogicWorks.	
1	February 3, 2022	Thr	18:00-20:40	Introduction	1
2	February 10, 2022	Thr	18:00-20:40	Understanding breadboard and parallel and series resistors	2
3	February 17, 2022	Thr	18:00-20:40	Logic Gates	2
4	February 24, 2022	Thr	18:00-20:40	Breadboard Template	2
5	March 3, 2022	Thr	18:00-20:40	Breadboard with gates	2
6	March 10, 2022	Thr	18:00-20:40	DeMorgan's Law	2
7	March 17, 2022	Thr	18:00-20:40	Breadboard DeMorgan's Law	2
	March 24, 2022	Thr		Spring Recess	
	March 31, 2022	Thr		Cesar Chavez Birthday Observed (Holiday, Campus Closed)	
8	April 7, 2022	Thr	18:00-20:40	Karnaugh Map Calculation	2
9	April 14, 2022	Thr	18:00-20:40	Breadboard Karnaugh Map	2
10	April 21, 2022	Thr	18:00-20:40	NOR SR Latch	2
11	April 28, 2022	Thr	18:00-20:40	Controlled-SR Latch	2
12	May 5, 2022	Thr	18:00-20:40	Understanding Registers - 1	2
13	May 12, 2022	Thr	18:00-20:40	Understanding Registers - 2	2

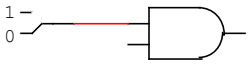
Lab 1: Introduction

We will be using LogicWorks logic circuit design and simulation software during the lab assignments. Please refer to the EEE 64-05 Canvas course page about how to access LogicWorks and video tutorials.

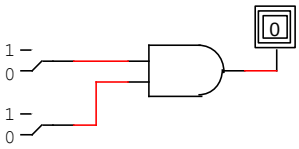
1. Create a new LogicWorks circuit (.cc file). You should see an empty workbook. Make sure the Parts Palette window is open (*View-> Parts Palette* checked).
2. Search for the 'and' keyword in the parts palette *Filter* box. Select **and_2**. Click on the picture of the gate and drag it to the workbook.
3. Search for the 'binary' keyword in the parts palette *Filter* box. Select **Binary Switch**. Click on the picture of the binary switch and drag it onto the workbook. Place the binary switch on the input (left) side of the AND gate. An example is shown below:



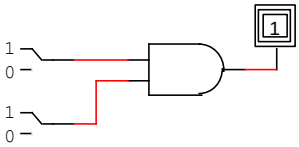
4. Click on the output terminal of the switch and drag the pointer to make a connection to one of the input terminals of the gate. An example is shown below:



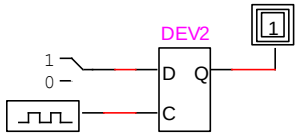
5. Connect another binary switch to the other input of the AND gate.
6. Search for the 'binary' keyword in the parts palette *Filter* box. Select **Binary Probe**. Click on the picture of the binary probe and drag it onto the workbook. Place the binary probe on the output (right) side of the AND gate. Click on the AND gate output terminal and drag the pointer to make a connection to the binary probe input terminal. An example is shown below:



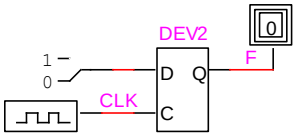
7. Click on the binary switches so that both of the switches apply logic 1. An example is shown below:



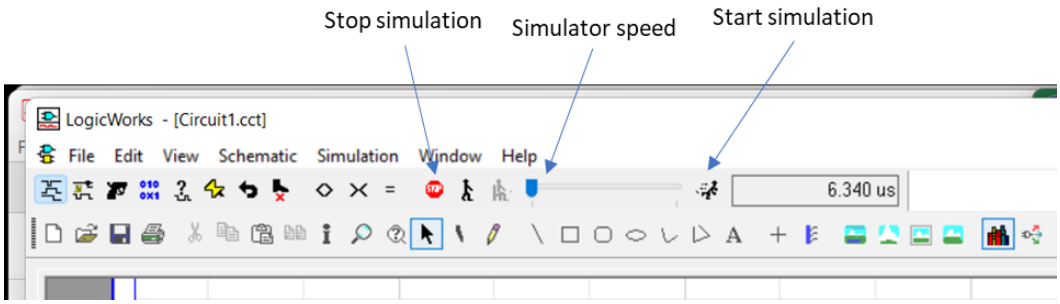
8. Submit the picture of your screenshot as part of your lab assignment. (0.5 points)
9. Search for the 'D flip flop' keyword in the parts palette *Filter* box (you will learn about D flip flops later in the semester.) Select **D Flip Flop wo/RSQ/**. Drag this component onto the workbook.
10. Connect a binary switch to the 'D' input and a binary probe to the Q output terminals.
11. Search for the 'clock' keyword in the parts palette *Filter* box. Click on **Clock**. Drag the picture of the clock onto the workbook and connect it to the C input terminal (if the clock starts running, click on the STOP sign on the menu bar.) An example is shown below:



12. Right click on the connection between the Q terminal and the binary probe and select 'Name' from the pop-up menu. Name it '**F**'. Right click on the connection between the clock symbol and the C input and name it 'CLK'. An example is shown below:



13. Start the simulation by selecting Run form the Simulation menu as follows: *Simulation-> Run* checked. At this time, your binary switch, and the binary probe, should respond when you change the logic level at the switch.
14. Open the Timing Window, if it is not already open, as follows: *Window -> Timing Window*. You should see CLK and F signals in the window. You can slow down the simulation by dragging the slider on the menu bar. See picture below.



15. Submit the picture of your screenshot as part of your lab assignment. Make sure the timing window shows in your screenshot. (0.5 points)

Lab 2: Understanding breadboard and parallel and series resistors

1. Thoroughly evaluate and understand the design and construction of your breadboard. You may find the following link useful: https://www.sciencebuddies.org/science-fair-projects/references/how-to-use-a-breadboard
2. Read the color code on a resistor from each group and determine its value. You can search 'resistor color code chart' on the internet to find the resistor color code charts (Video on resistors and reading the color code: http://www.youtube.com/watch?v=HrZZMhWZiFk&feature=fvwrel).
   Carefully measure the resistance values of the 100Ω, 220Ω, 330Ω, and 1KΩ resistors using the multimeter.
   (Video on how to use a Digital Multimeter: http://www.youtube.com/watch?v=bF3OyQ3HwfU&feature=related)
   Include a table in your lab report that shows the value you read using the color code chart and the value you measured using the multimeter. (0.2 points)
3. Use your breadboard to place two of your resistors in series. Select the resistors from the 100Ω, 220Ω, 330Ω, and 1KΩ resistors. Include the schematic of your circuit and a picture of your breadboard with the two series resistors in your lab report. Measure the combined resistance of the two resistors and report the value within your lab report. (Video on Series and parallel resistors: http://www.youtube.com/watch?v=9O8Di5gugiA). Include in your lab report a comparison of your measured results to the results that you might have expected by calculations. (0.6 points)
4. Use your breadboard to place three of your resistors in parallel. Include the schematic of your circuit and a picture of your breadboard with the three parallel resistors in your lab report. Measure the combined resistance of the three parallel resistors and report the value within your lab report. Include in your lab report a comparison of your measured results to the results that you might have expected by calculations. (0.6 points).
5. Use your breadboard to place two of your resistors in parallel with one resistor in series. Measure the combined resistance of two parallel resistors in series with a single resistor. Include the schematic of your circuit and a picture of your breadboard in your lab report. Include in your lab report a comparison of your measured results to the results that you might have expected by calculations. (0.6 points)

Lab 2: Logic Gates

1. Using online resources obtain the spec sheet for the following logic gates contained within your kit: 74LS08, 74LS32, 74LS86

2. Use your LogicWorks to design and simulate the four circuits displayed below.
   a. The first circuit will have two output LEDs; A and B as shown in the picture below.
   Note: the switches are *SPST* switch in LogicWorks parts palette.
   Note: LogicWorks does not define resistor values. Write the resistor values next to the resistors by using the Text (***A***) tool in the menu bar.
   We will refer to this circuit as our "Simulated Template Circuit". (0.5 points)

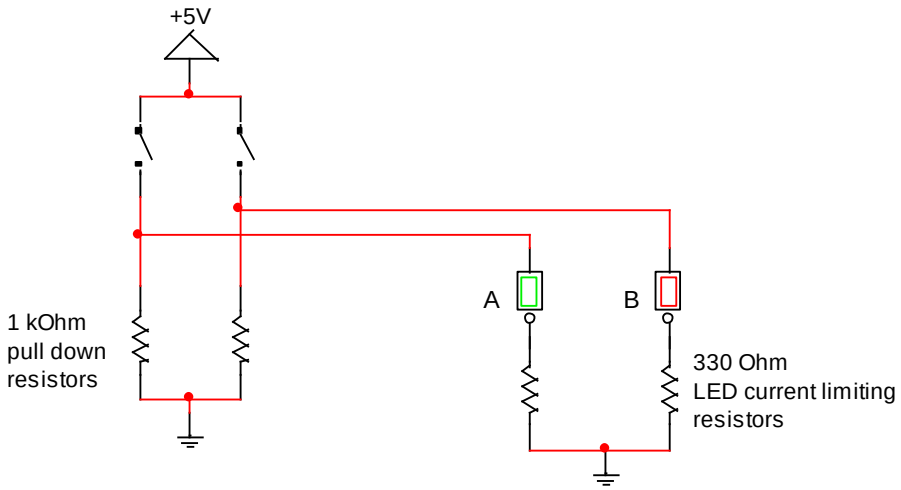


Figure: LogicWorks schematic

   b. The second circuit will have three LEDs. Two of the LEDs will be connected to the two inputs of an AND gate. The third LED will be connected to the output of the AND gate. (See Figures below) (0.5 points)

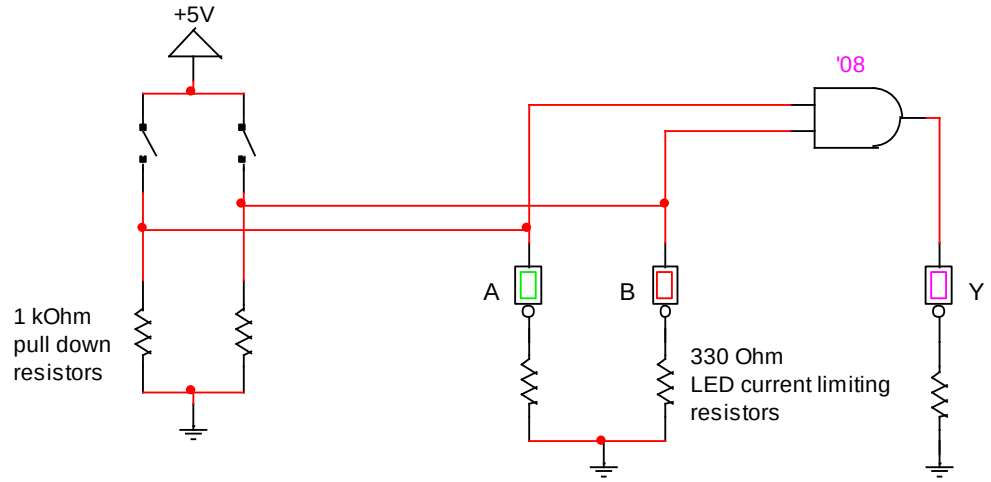


Figure: LogicWorks schematic

c. The third circuit will have three LEDs. Two of the LEDs will be connected to the two inputs of an OR gate. The third LED will be connected to the output of the OR gate. (0.5 points)
d. The fourth circuit have three LEDs. Two of the LEDs will be connected to the two inputs of an XOR gate. The third LED will be connected to the output of the XOR gate. (0.5 points)

3. Simulate each of your circuits using the switches and verify that your circuits behave in a manner that is consistent with the truth table that corresponds to each of the logic gates. Submit the screenshots of your circuits that correspond to the following table with your lab report.

A	B	Y
0	0	
0	1	
1	0	
1	1	

Lab 4: Breadboard Template

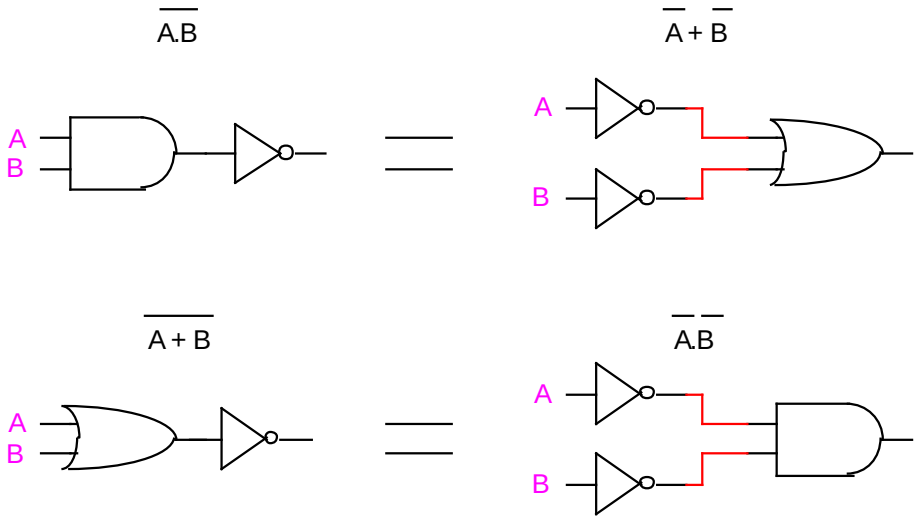
1. Using your breadboard and the parts in your lab kit, physically construct the first of the four circuits that you simulated in the previous lab session (Lab 3).
2. Describe in your lab report any differences that you may observe between your simulated circuit and your breadboard physically constructed circuit.
   Note: Talk to your lab instructor about any significant differences that you observe. Significant differences may be the result of breadboard wiring errors. You will not be able to complete your next lab assignments until you fix those wiring errors.
3. After correcting any breadboard wiring errors put the breadboard aside without removing any of the wires, resistors or LEDs. We will refer to this circuit as our "Breadboard Template Circuit". You will use this circuit as a template for additional circuits that you'll be constructing over the next few weeks.
4. Submit a picture of your breadboard with your lab report. (2 points)

Lab 5: Breadboard with gates

1. Using your Breadboard Template Circuit and the parts in your lab kit, physically construct each of the remaining three circuits that you simulated during the Lab 3 session.
2. Submit a picture of your breadboard with your lab report. Describe in your lab report any differences that you may observe between your simulated circuit and your breadboard physically constructed circuit. (2 points)

Lab 6: DeMorgan's Law

Using the simulation software with your "Simulated Template Circuit" from Lab 3 in combination with NOT gates, AND gates and OR gates, build circuits that demonstrate (with simulated results) the validity of the following two equations known as DeMorgan's Law:



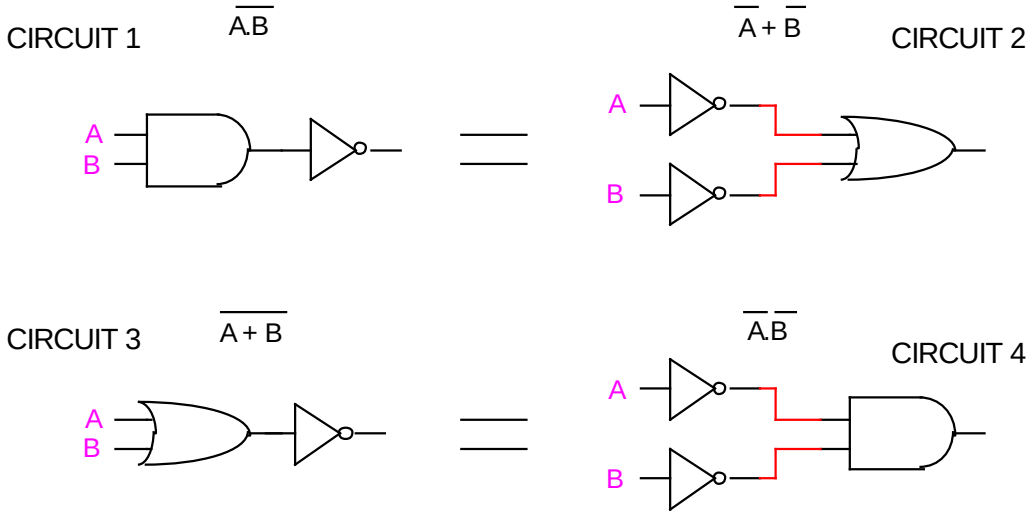
1. Create a truth table for each circuit by simulating your circuit in LogicWorks (use binary switches for each input to construct the truth table.) Submit the screenshot of the schematic and the truth table of each circuit in your lab report. (1 point; 0.5 point for each set of circuits and their truth table)
2. Prove that DeMorgan's Law applies to more than two variables (general DeMorgan's Law) by implementing the following:

   $$(A \cdot B \cdot C)' = A' + B' + C'$$
   $$(A + B + C)' = A' \cdot B' \cdot C'$$

   Design the circuits and create the truth tables to prove general DeMorgan's Law (1 point)

Lab 7: Breadboard DeMorgan's Law

Using your breadboard in combination with NOT gates, AND gates and OR gates from your lab kit, build circuits that demonstrate the validity of the following two equations known as De Morgan's Law. Do not submit a lab report if your circuit is not working. Discuss with your instructor troubleshooting steps.



You will be building each of the four circuits above. Use the breadboard template circuit with LEDs. Take a picture of your breadboard showing the respective LEDs lit up according to the following (you can designate one of the switches as A and the other as B):

1) Circuit 1:

A	ON
B	OFF

Submit a picture of your breadboard circuit in your lab report. (0.5 points)

2) Circuit 2:

A	ON
B	OFF

Submit a picture of your breadboard circuit in your lab report. (0.5 points)

3) Circuit 3:

A	OFF
B	OFF

Submit a picture of your breadboard circuit in your lab report. (0.5 points)

4) Circuit 4:

A	OFF
B	OFF

Submit a picture of your breadboard circuit in your lab report. (0.5 points)

Lab 8: Karnaugh Map Calculation

Design a logic system that has four (a,b,c,d) inputs and one (f/LED) output. "f/LED" will be High/turn-on when at least 2 inputs next to each other are High (set to "1").
Example: these (abcd) inputs: 1110, 0110, .. will set "f" High. While 1001, 1010, .. will set "f" Low.
a) Obtain your solution (equation) using K-maps. Clearly show how you obtained the equation for ***f*** by showing the clusters that you used on your K-map.
b) Create schematics from your K-maps. Make sure you identify the logic gates with part numbers.

Your lab report submission should include the following:

- K-map showing the clusters. (0.6 points)
- The equation for ***f*** that you derived from your K-map. (0.6 points)
- The logic circuit to implement the equation. Make sure all gates are identified by part numbers. (0.8 points)

Hints:

1. Create the truth table for f with inputs a, b, c, d, first. Then create the K-map. Remember that each square in the K-map corresponds to a truth table row.
2. Remember that clusters of ***m*** squares, eliminates ***n*** variables where $2^n = m$. Try to form clusters as large as possible to eliminate as many variables as possible.

Lab 9: Breadboard Karnaugh Map

Construct (using your breadboard, wires, LED and gates), test and verify the circuit that was designed during Lab 7. Do not forget to use the pull-down resistors at the input of the logic gates.

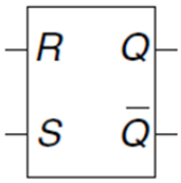
Test the input conditions given below and include in your lab report pictures of your circuit that confirm that the circuit is behaving in a manner that meets all of the Lab 8 requirements. Make sure you mark your pictures by the number of the conditions below.

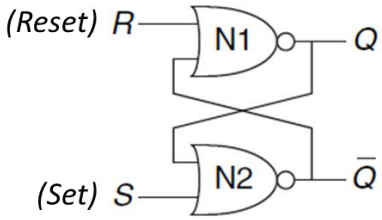
1) a=1, b=0, c=1, d=0
2) a=0, b=0, c=1, d=1
3) a=1, b=1, c=1, d=0

(2 points)

Lab 10: NOR SR Latch

Using your Breadboard Template Circuit and NOR GATES from your lab kit construct an SR Latch. Place an LED at each input (S and R) and an LED at the output (Q).





S	R	Q	$\bar{Q}$
0	0	Q_{prev}	$\bar{Q}_{prev}$
0	1	0	1
1	0	1	0
1	1	0	0

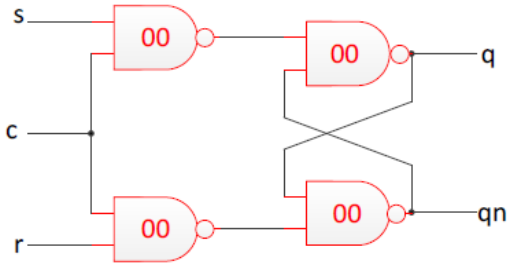
Test the following sequence and take pictures after each step. Submit the pictures with your lab report. Make sure to identify which picture belongs to which step.
Step 0: S=0; R=1
Step 1: S= 1; R= 0
Step 2: S=0; R=0
Step 3: S=0; R=1

In your lab report submit pictures of your circuit that shows the state of the LEDs clearly after each step. (2 points)

Lab 11: Controlled SR-Latch

Using your Breadboard Template Circuit and NAND GATES from your lab kit construct a controlled SR-Latch. Place an LED at each input (s, c, and r) and an LED at the output (q).
Test the following sequence and take pictures after each step. Submit the pictures with your lab report. Make sure to identify which picture belongs to which step.
Step 0: s= 1; r= 0; c= 1
Step 1: s= 1; r= 0; c= 0
Step 2: s= 0; r= 1; c= 0
Step 3: s= 0; r= 1; c= 1

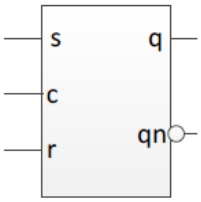
Controlled-SR latch



Truth Table

s	r	c	q	z (qn)
0	0	1	q	qn (last state)
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1 (not allowed)
x	x	0	q	qn (last state)

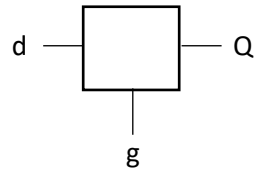
Symbol



In your lab report submit pictures of your circuit that shows the state of the LEDs clearly after each step. (2 points)

Lab 12: Understanding Registers – 1

Consider the black box circuit and the corresponding excitation table shown below:



Excitation Table

Present State	Input	Input	Next State
Q	**d**	**g**	**Q^+**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

a) Draw the state diagram for this circuit. Assume Q = 0 is S0 and Q = 1 is S1.
b) Derive the equation for Q^+.
c) Simplify the equation using Karnaugh Maps.
d) Design the logic circuit inside the box.

Submit the state diagram, the equation, and the screen shot of the schematic of the circuit with your lab report.
(2 points)

Lab 13: Understanding Registers – 2

Implement the circuit you designed in Lab 12 on your breadboard using the SN74LS74 IC and other necessary logic gates and LEDs. Verify its operation following the steps below. When implementing Step 1, set the d input first, then set the g input. Take a picture of your circuit for each step.

Step	d	g	State of output LED
1	1	1	
2	1	0	
3	0	0	
4	0	1	

Submit the completed table and pictures of your circuit for each step with your lab report.

(2 points)