CPE166 Final Exam - Part 1

Started: Dec 14 at 9:36am

Quiz Instructions

Each question in part 1 has only one correct answer.

The CPE 166 final exam has both part 1 and part 2.

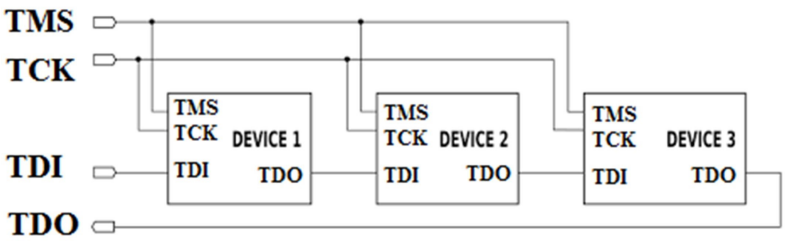
The questions in Part 1 are in the multiple choice format. Once you're done, you'll need to work on the Part 2 questions.

On the Canvas website, click "Assignments" to find the CPE166 Final Exam - Part 2.

You'll need to upload a solution file for the part 2 questions.

Question 1 — 3 pts

The diagram below shows parallel JTAG boundary scan. Is this statement true or false?



- ○ True
- ◉ False

Question 2 — 3 pts

Consider the binary message 111101, and a generating polynomial $P(x)= x^3 + x + 1$. Then for error correction and detection, the CRC bits attached at the end of the above 6-bit message should be 101.

_____ True

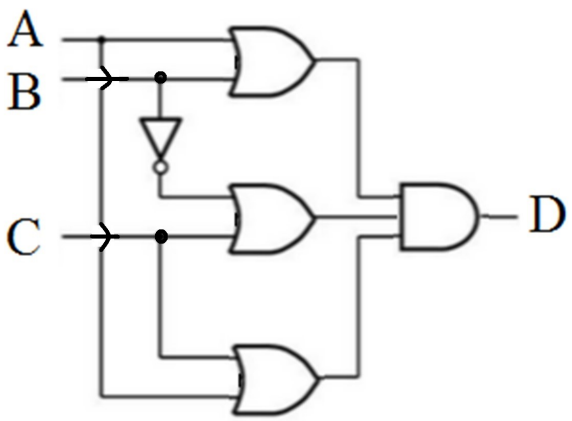
_____ False

- ○ True
- ◉ False

Question 3

3 pts

The circuit below has static-0 hazard.



- ○ True
- ◉ False

Question 4

3 pts

Reducing setup time of D Flip-Flop can be used to minimize the effect of the metastability problem.

- ◉ True
- ○ False

Question 5

3 pts

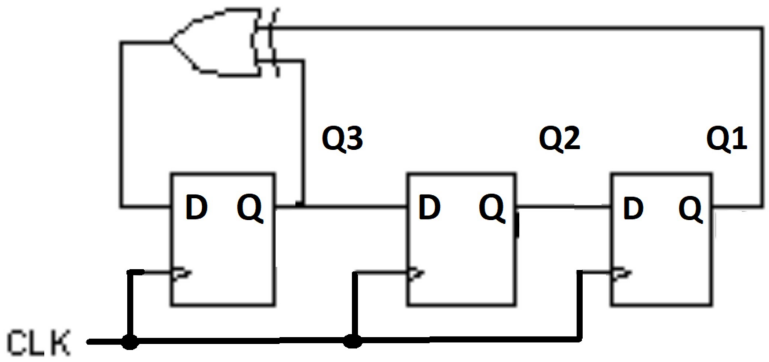
Xilinx CLB is used to implement the input and output functions of an FPGA device.

- ○ True
- ◉ False

Question 6

3 pts

In the follower linear feedback shift register circuit, suppose the currently binary values stored by three registers are Q3Q2Q1 = “001”.



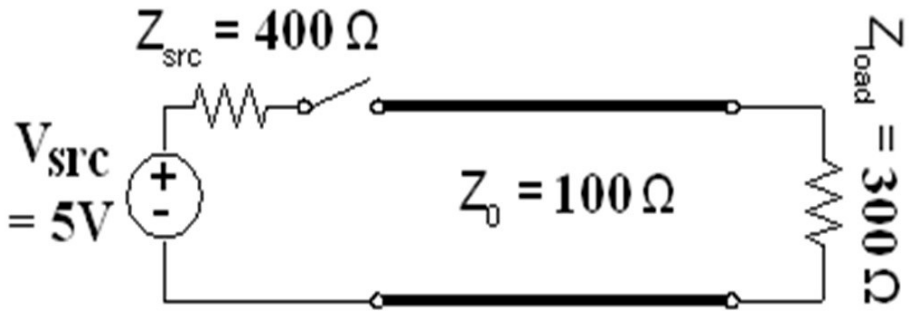
One clock cycle later, Q3Q2Q1 will be _____ 100

_____

Question 7

3 pts

The transmission line circuit is shown below.



Calculate reflection coefficient at the load ρload. Your answer: ___

(300-100)/(300+100) _____

Calculate the load voltage after the first reflection. Your answer: ___

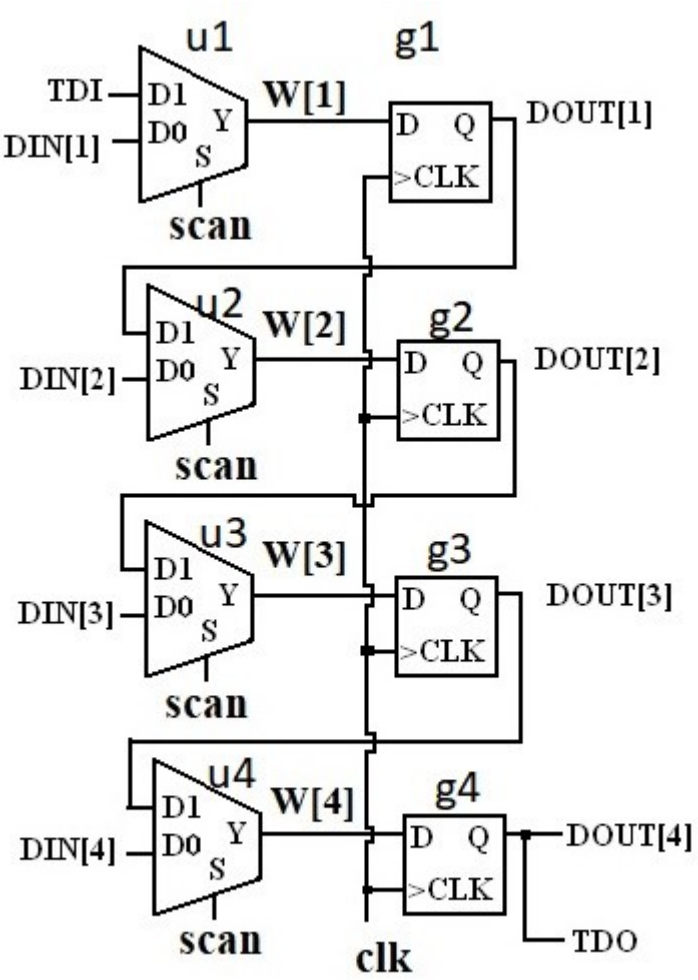
1.5 V _____

Calculate the steady state load voltage. Your answer: ____

(15/7) V _____

Question 8 24 pts

Use hierarchical design strategy to implement the circuit shown below in **Verilog**. When scan is true, the system should shift the testing data TDI through all scannable registers and move out through signal TDO. When scan is false, the system should work in the normal mode.



module mux (D1, D0, S, Y);

input D1, D0, S;

output Y;

assign Y = S? D1 : D0 ;

endmodule

module dff (CLK, D, Q);

input CLK, D;

output Q;

reg Q;

always@(posedge CLK)

Q <= D ;

endmodule

module top(TDI, DIN, SCAN, DOUT, TDO);

input TDI, SCAN ;

input [4:1] DIN ;

output TDO ;

output [4:1] DOUT ;

wire [4:1] W ;

mux u1 (TDI, DIN[1], SCAN, W[1]);

mux u2 (DOUT[1], DIN[2], SCAN, W[2]);

mux u3 (DOUT[2], DIN[3], SCAN, W[3]);

mux u4 (DOUT[3], DIN[4], SCAN, W[4]);

dff g1 (CLK, W[1], DOUT[1]);

dff g2 (CLK, W[2], DOUT[2]);

dff g3 (CLK, W[3], DOUT[3]);

dff g4 (CLK, W[4], DOUT[4]);

assign TDO = DOUT[4] ;

endmodule

Saving... Submit Quiz