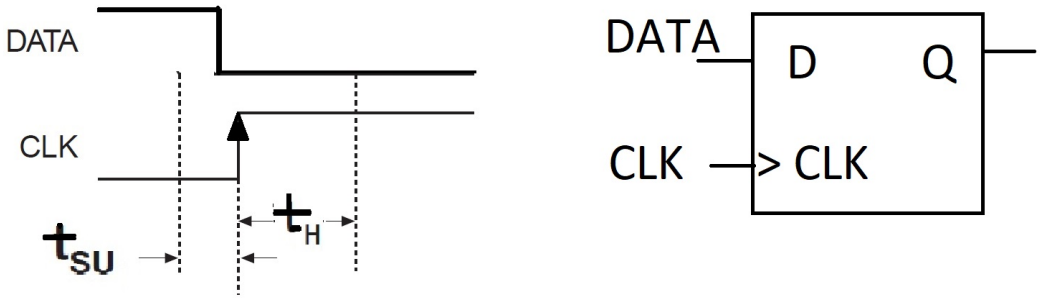
CPE 166 Midterm 2 - Part 1

Started: Nov 16 at 8:49am

Quiz Instructions

Question 1 — 2 pts

Would the following data waveform cause metastability problem? t_{su} and t_h are setup time and hold time for the D flipflop.



- (●) Yes
- ( ) No

Question 2 — 2 pts

In order to reduce metastability in a system, we can reduce the clock frequency.

- (●) True
- ( ) False

Question 3 — 2 pts

s(7 downto 0) <= “0000” & s(7 downto 4); is an logical left shifter which shifts left by 4 bits.

- ○ True
- ◉ False
- ○

Question 4 — 2 pts

The even parity bit for the binary message “1011” is:

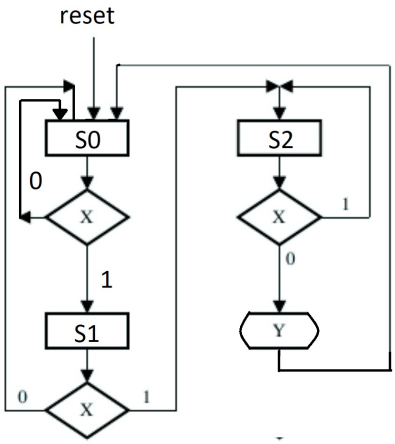
A). 1

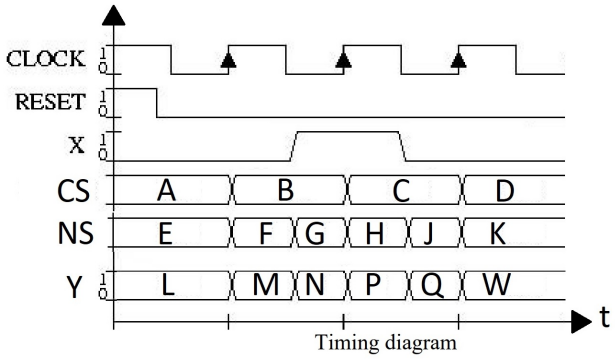
B). 0

- ◉ A
- ○ B

Question 5 — 16 pts

The ASM chart and the simulation waveform are shown below. CS is the current state signal which is updated at the rising edge of the clock, NS is the next state signal, RESET is asynchronous.





For the above waveform, select the correct values below:

A = ____ S0 ____ , B= ____

S0 ____

C = ____ S1 ____ , D= ____

S0 ____

E = '____ S0 ____ , F= ___

S0 ____

G = ____ S1 ____ , H= ____

S2 ____

J= ____ S0 ____ , K= ___

S0 ____

L = ____ 0 ____ , M= ____

0 ____

N = ____ 0 ____ , P= ___

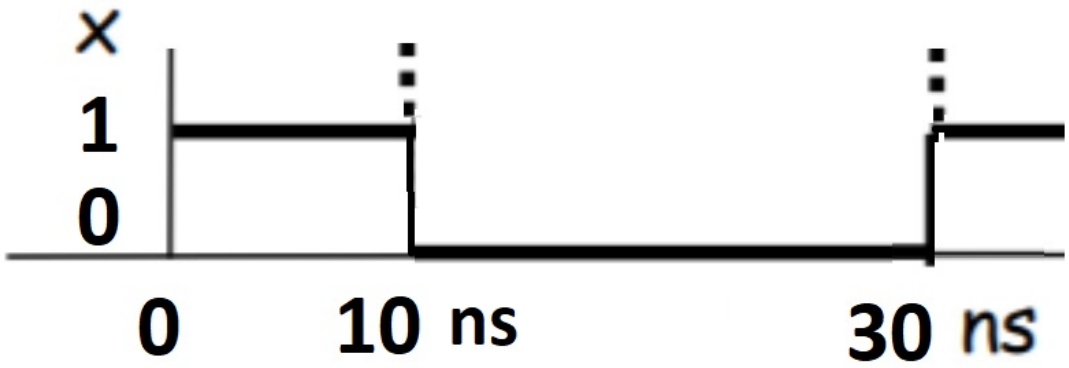
0 ____

Q = ____ 0 ____ , W= ____

0 ____

Question 6 — 5 pts

Generate the following waveform for signal x by using VHDL.



x <= _ '1' _ , _ '0' _ after _

10 _ ns, _ '1' _ after _

30 _ ns;

Quiz saved at 8:51am

Submit Quiz