CPE166 Midterm1 - Part 2 - 2nd

Started: Oct 28 at 9:36am

Quiz Instructions

Students can take the "CPE166 Midterm1 - Part 2 - 2nd" test this Friday 10/28/2022 from 9:00am to 9:50am with a maximum score of 27.
If your previous part 2 test score is above 27, you don't have to take this test on this Friday.
You can study VHDL lecture notes and work on the lab project assignments.

The highest score for "CPE166 Midterm 1 - Part 2" and "CPE166 Midterm1 - Part 2 - 2nd" will be considered as the Part 2 score.

Question 1 — 10 pts

Implement the clock division hardware design in Verilog.
The input clock is clkin and the output clock is clkout.
The frequency of clkout is equal to the frequency of clkin divided by 20.
Each blank below only has one correct answer.

```
module clkdiv (clkin, clkout);

input      clkin;

output   clkout;

___ reg ____ clkout;

___ [2:0] ____ cnt;

always  @ ( __ posedge clkin ____  )

begin

   if ( cnt ==  ___ 19 _____ )

   begin

      cnt  <=  0;
```

```
    clkout   <=  1;
  end
___ [else if] _____( cnt < 9 )
  begin
    cnt <= ___ [cnt + 1] ___;
    clkout <=  1;
  end
else
  begin
    cnt <= ___ [cnt + 1] ___;
    clkout  <= __ [0] ___;
  end
___ [end] _____
___ [endmodule] _____
```

Question 2

17 pts

Design a single Mealy finite state machine to recognize the sequence 110.

```
module fsm ( reset, clk, a, y);
input reset, clk;
input a;        // “a” represents the incoming data
output y;      // “y” is a mealy output for detecting the correct sequence
__ [reg] __ y;
```

__ [1:0] __ cs, ns; //cs: current state, ns: next state

parameter s0 = 2'b00, s1=2'b01, s2=2'b10;

always @ (___ posedge clk or posedge reset ___)

begin

if(reset) ___ cs <= s0 __;

else ___ cs <= ns ___ ;

end

always@(___ cs or a ___)

begin

case@(cs)

s0: if(a) ns = ___ s1 ___;

else ns = ___ s0 ___;

s1: if(a) ns = ___ s2 __;

else ns = ___ s0 __;

s2: if(a) ns =____ s2 __;

else ns = ___ s0 __;

default : ns = s0;

endcase

end

always @ (___ cs or a __)

begin

case(cs)

s0: y = ___ 0 __ ;

s1: y = ___ 0 __ ;

```
s2:     if(a)   y = ___ 0 __;
            else   y = ___ 1 __;
 default:     y = 0;
endcase
end
endmodule
```

Saving...

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