



Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs)

Perry L Heedley, Ph.D.

© 2014*

* Most figures and examples are from the course textbook “Microelectronic Circuits” by Adel S. Sedra and Kenneth C. Smith, 6th Edition, © 2010 by Oxford University Press, Inc.

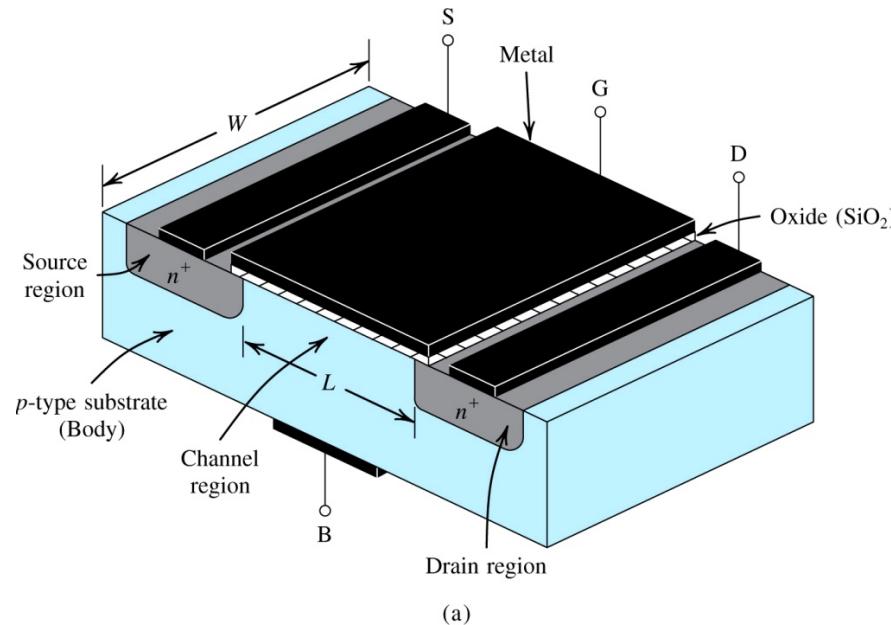


Outline

- NMOS and PMOS FET device structures & symbols
- Regions of Operation
 - Cutoff, Triode, Saturation, Sub-Threshold
- Large-signal MOSFET I-V equations
- Key second-order effects
 - Channel-length modulation, Body effect
- Additional important 2nd and 3rd order effects
 - Leakage currents, DIBL, velocity saturation, mobility degradation, breakdown & punch-through, temperature effects
- DC biasing of MOSFETs
- Small-signal MOSFET models
- Using MOSFETs as voltage amplifiers
- Summary of key concepts

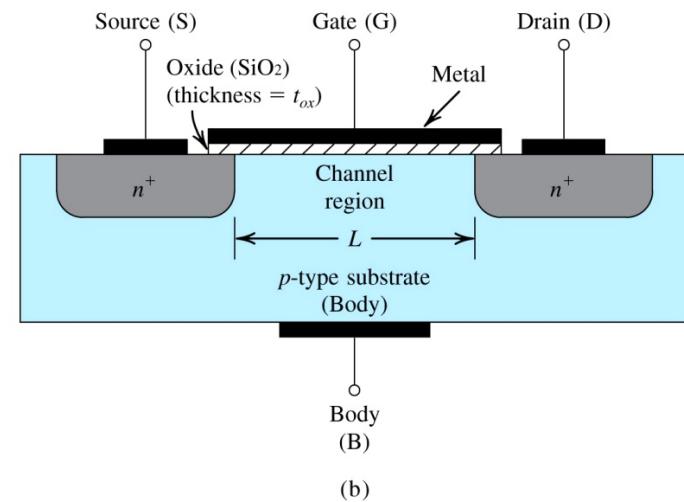


MOSFET device structure



(a)

Cross section view :

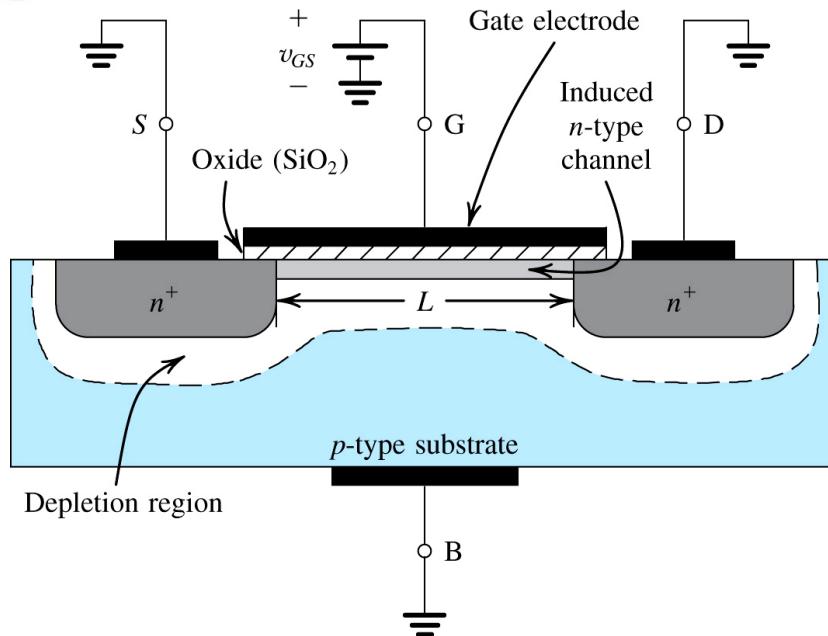


(b)

- **Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs)** control current flow using electric fields
- MOSFETs consist of the **Source** of charge carriers, the **Drain** where the charge carriers leave the device, and the **Gate** which controls the flow of current
- Key design parameters are the gate's **Width** and **Length**



NMOS FET devices



- With $V_{GS} = 0$ the FET is off, since the two PN junctions are reverse (or zero) biased
- With $V_{GS} \geq V_t = \text{Threshold Voltage}$, a channel between the source & drain is formed

- With $V_{GS} \geq V_t$ the MOS gate forms a parallel-plate capacitor between the gate and the channel with :

$$C_{OX} = \frac{\epsilon_{OX}}{t_{OX}} \quad \text{and} \quad C_{GATE} = C_{OX} WL$$

where :

$$\epsilon_{OX} = 3.9 \epsilon_0 \text{ for } SiO_2$$

$$\epsilon_0 = 8.854 \times 10^{-14} F/cm$$

t_{OX} = the gate oxide thickness

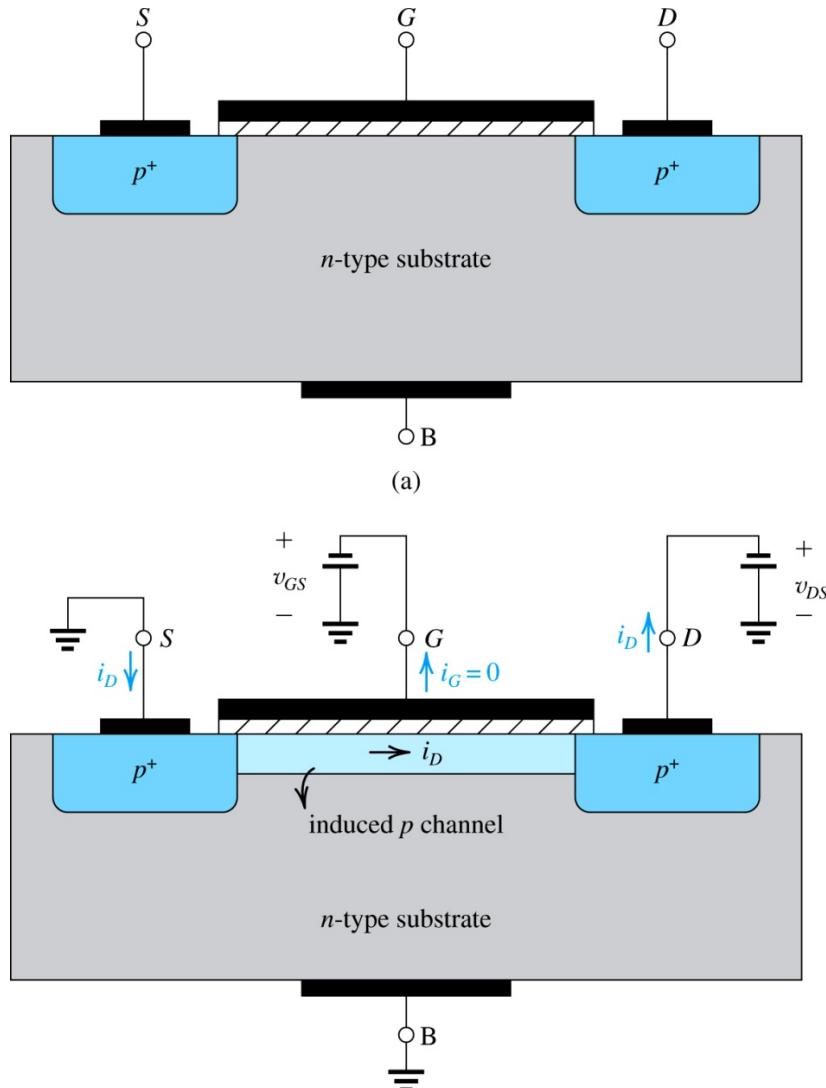
WL = the area of the gate

$$\text{and } |Q| = C_{GATE} (V_{GS} - V_t) = C_{GATE} V_{OV}$$

with V_{OV} = the **overdrive voltage**



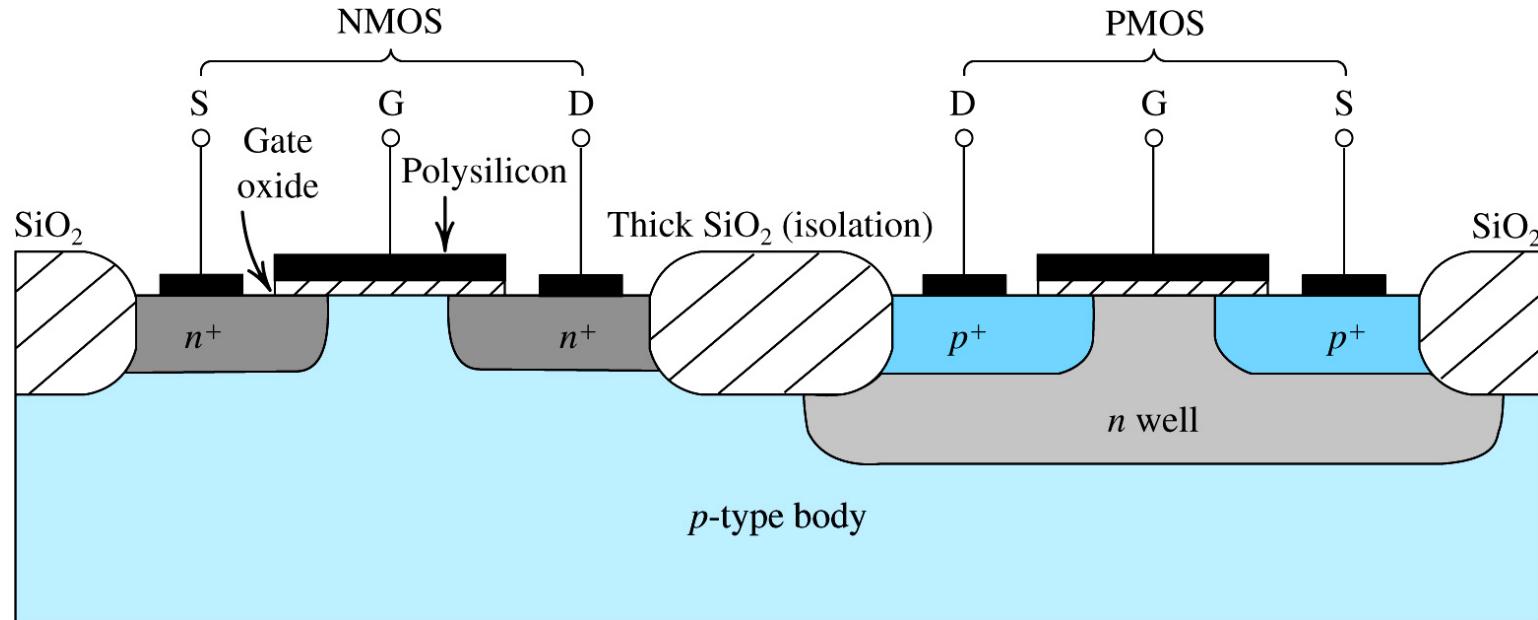
PMOS FET devices



- NMOS FETs use N+ doped source & drain diffusions in a P-type substrate
- PMOS FETs use P+ doped source & drain diffusions in a N-type substrate
- Both NMOS & PMOS FETs operate the same way, but both the doping types and the voltages and currents are reversed :
 - V_t is positive for NMOS FETs
 - V_t is negative for PMOS FETs(but need $|V_{GS}| > |V_t|$ for both!)



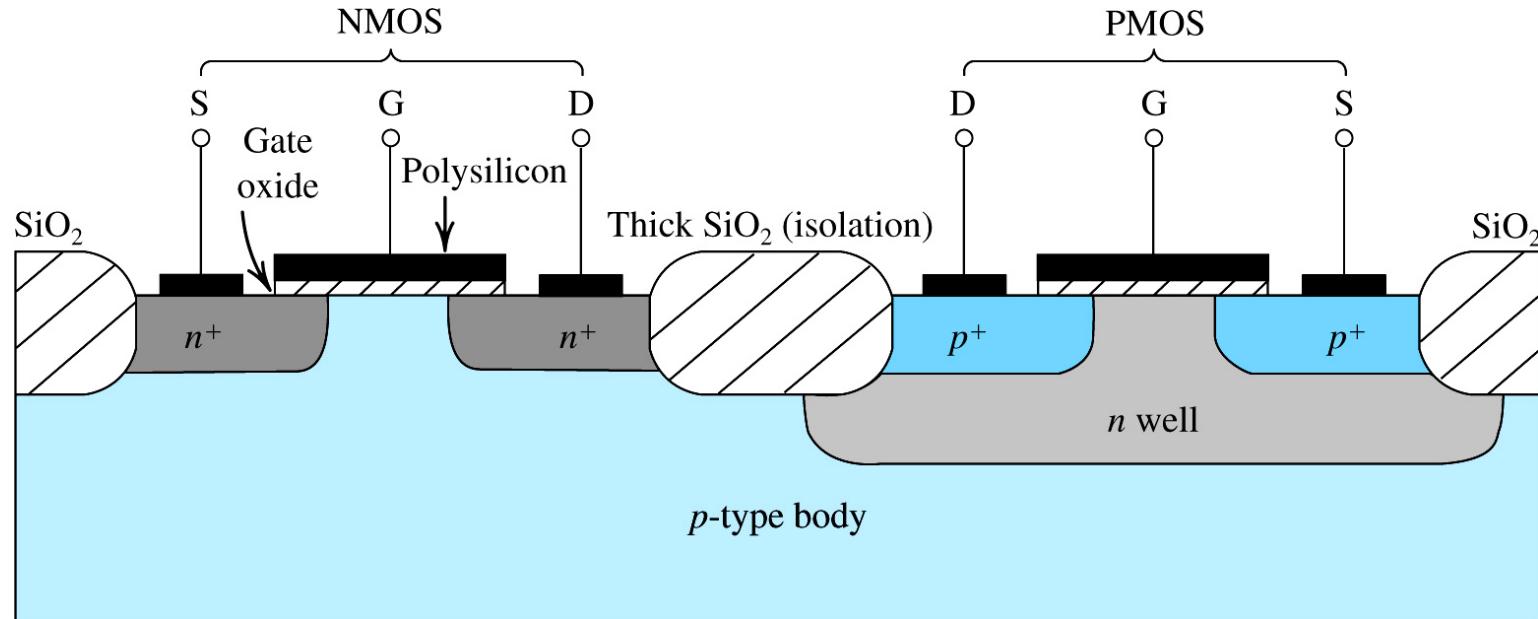
CMOS FET devices



- **Complementary Metal Oxide Semiconductor (CMOS)** technology combines both NMOS and PMOS FETs on a single integrated circuit (called an “IC”, “chip” or “die”)
- Modern CMOS processes use a *P*-type silicon substrate, with PMOS FETs built in **N-wells** (islands of *n*-type Si)



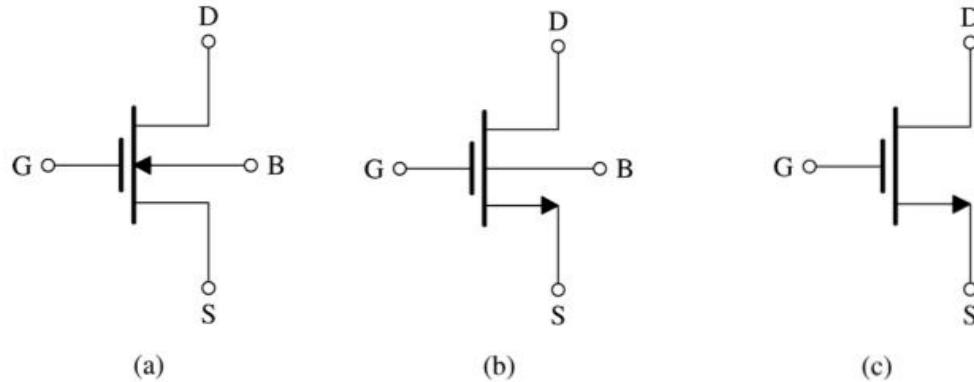
CMOS FET devices



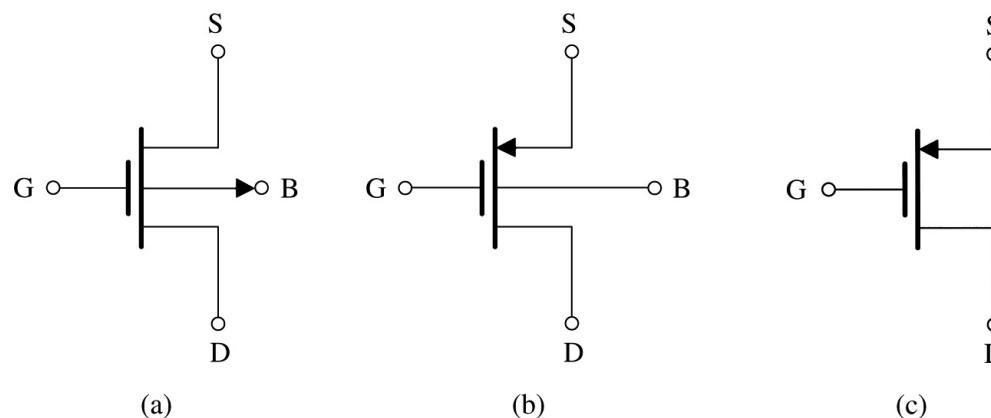
- The FETs are really the devices being intentionally built, the PN junction diodes are just **parasitic devices**
 - Parasitic devices are not desired, but are present anyway
- CMOS designers must keep all the PN junctions turned off !
 - Connect P-substrate to the lowest potential on the IC (usually ground)
 - Connect N-wells to the highest potential on the IC (typically called V_{DD})



MOSFET device schematic symbols



Commonly used NMOS FET symbols



Commonly used PMOS FET symbols

- The (c) symbols are preferred by many analog designers, since :
 - The connections for the “body” or “bulk” are well known and typically all the same
 - Why let schematics get cluttered and hard to read with all the extra wires?
 - The arrows show the current flow direction
 - Similar to BJT symbol



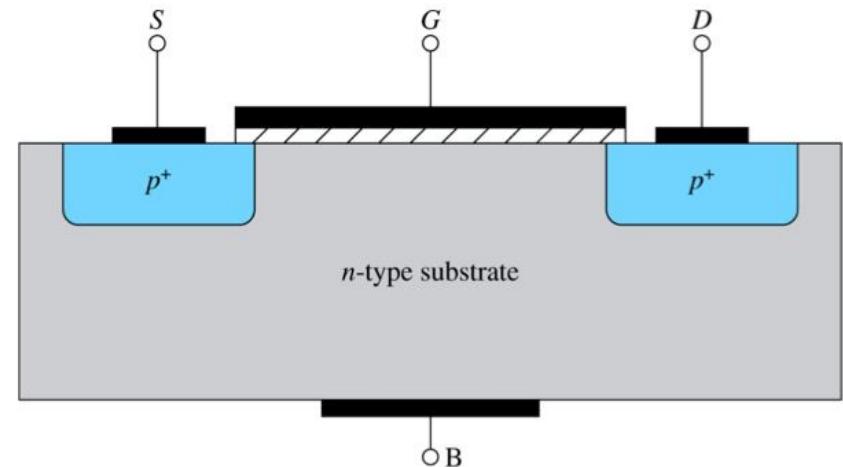
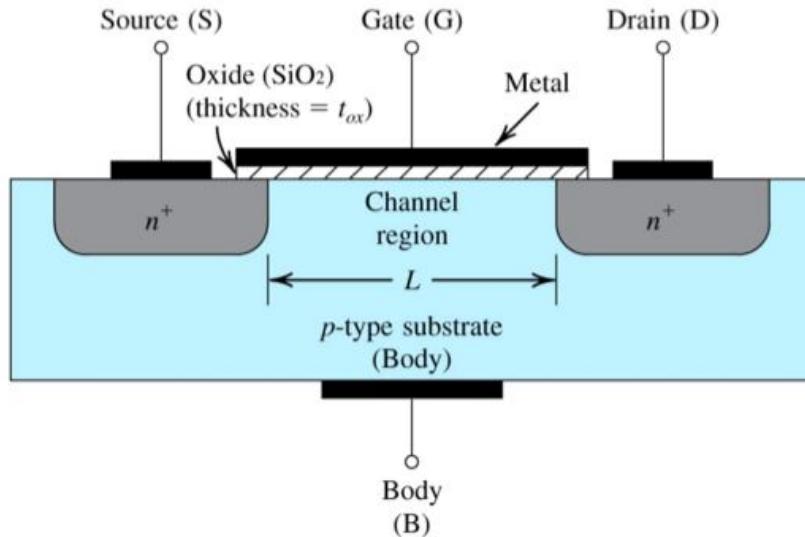
Regions of Operation

- **Cutoff** is when $|V_{GS}| < |V_t|$ so the FET is turned off and no channel exists. This means that zero current flows between drain and source. (For $|V_{GS}|$ slightly $< |V_t|$ the FET is in **sub-threshold** and small currents do flow.)
- **Triode** is when $|V_{GS}| \geq |V_t|$ so the FET is turned on and a channel is formed between the drain and the source, and $|V_{DS}| < |V_{DS-sat}|$, where V_{DS-sat} is the minimum V_{DS} required in order for the device to be in saturation.
- **Saturation** is when $|V_{GS}| \geq |V_t|$ so the FET is turned on and a channel is formed between the drain and the source, and $|V_{DS}| \geq |V_{DS-sat}|$, where V_{DS-sat} is the minimum V_{DS} required in order for the device to be in saturation.

A simple approximation for $V_{DS-sat} = V_{GS} - V_t = V_{ov}$



Cutoff Region

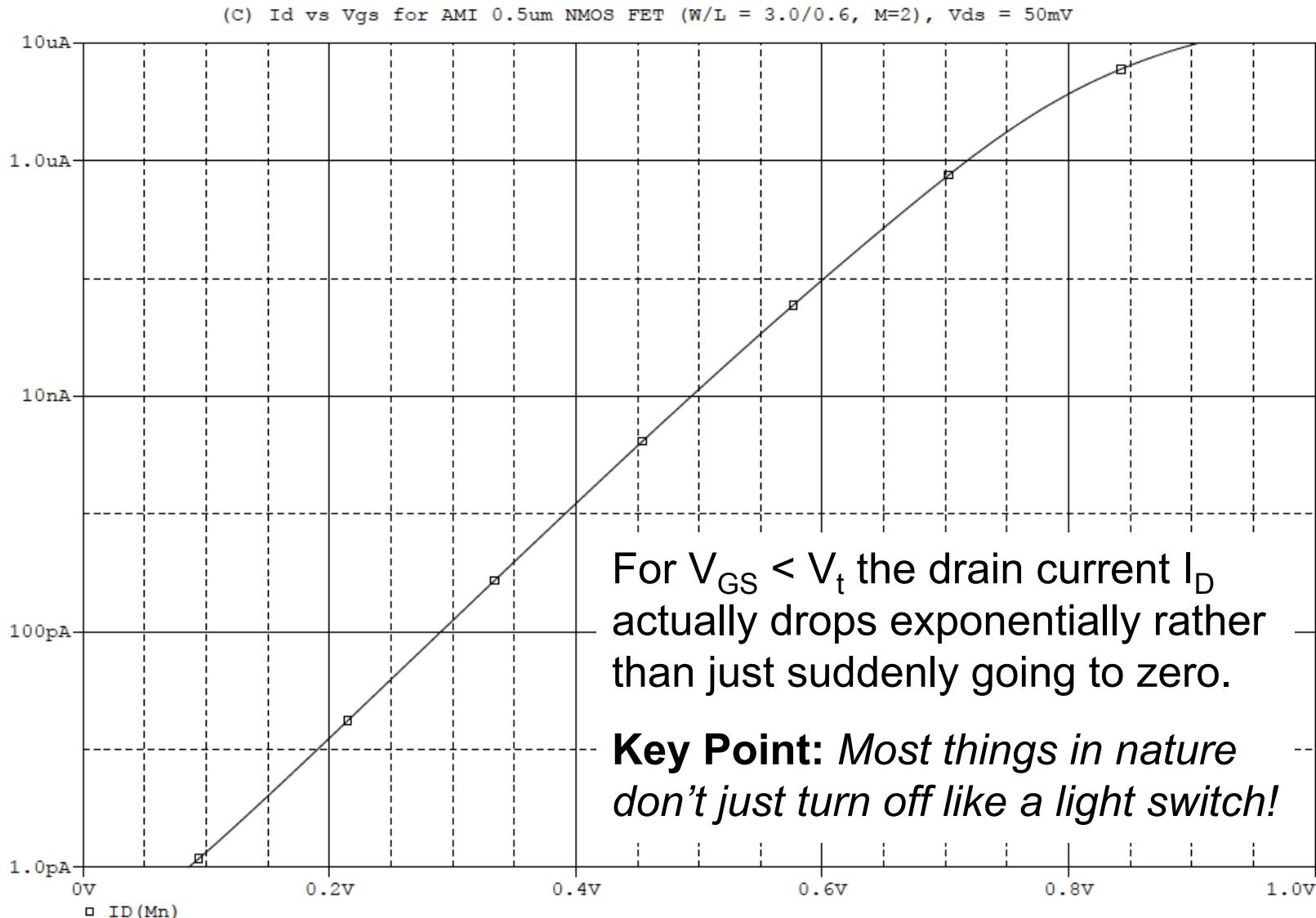


- With $V_{GS} < V_t$ the FET is off and no channel exists between drain and source
 - For an NMOS FET to be on, V_{GS} must be more positive than the positive threshold, V_t
 - The PN junctions are reverse biased, so no current can flow

- With $|V_{GS}| < |V_t|$ the FET is off and no channel exists between drain and source
 - For a PMOS FET to be on, V_{GS} must be more negative than the negative threshold, V_t
 - The PN junctions are reverse biased, so no current can flow

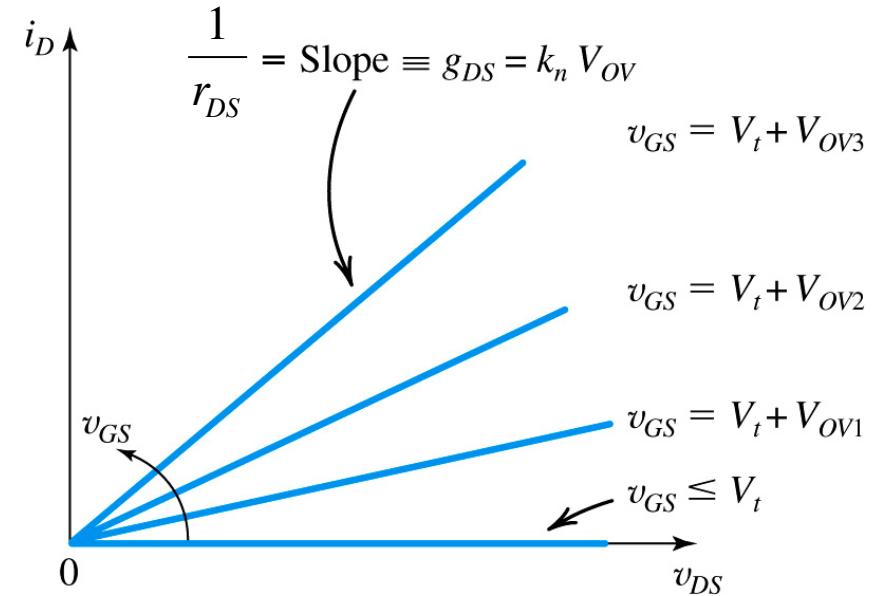
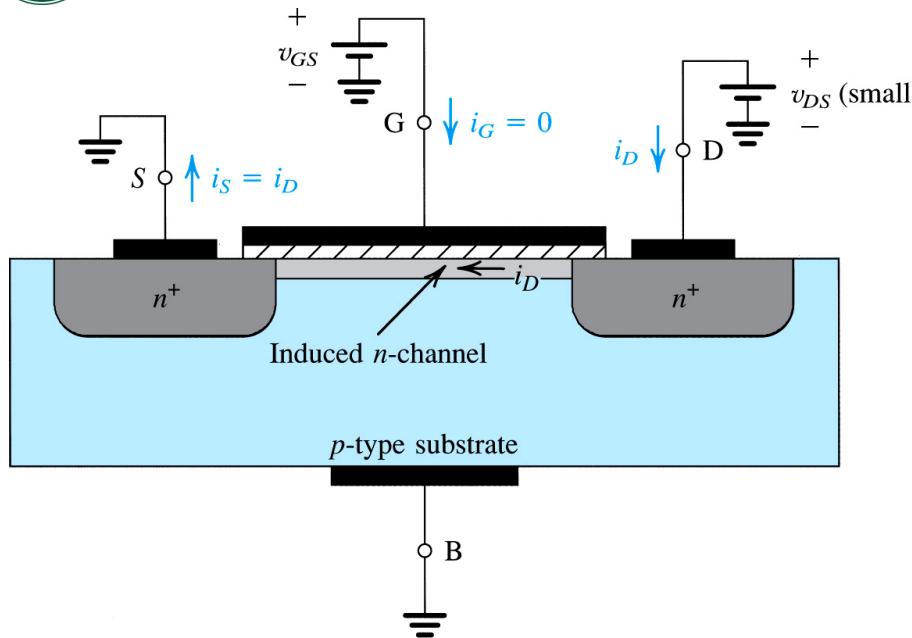


Sub-Threshold operation





Triode Region

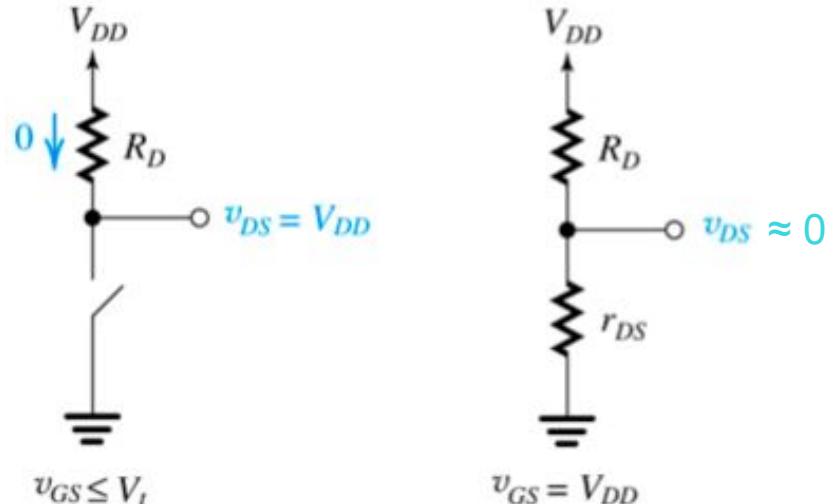
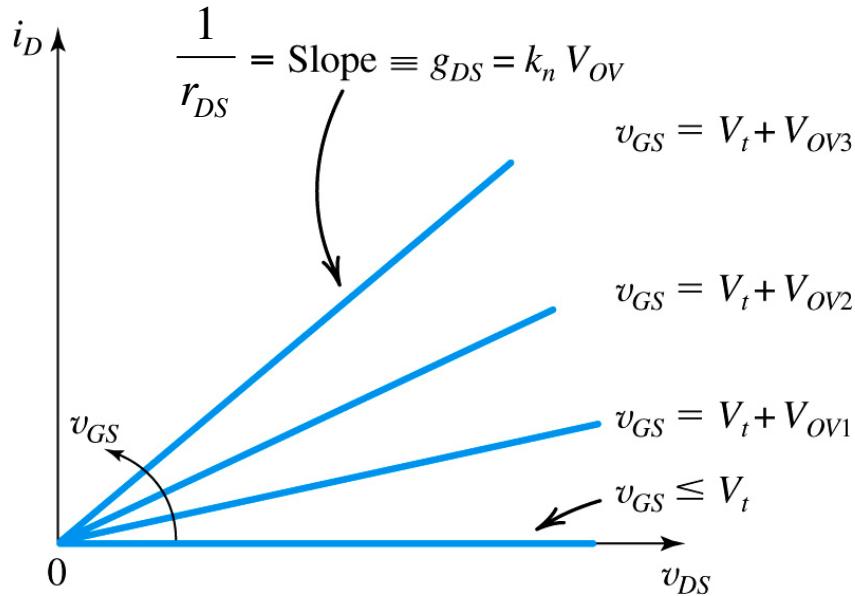


- Since $V_{GS} \geq V_t$ a channel is formed connecting the drain and the source
- The channel looks like a resistor, so $V_{DS} > 0 \rightarrow I_D > 0$

- For small values of V_{DS} the I_D vs V_{DS} curve is linear, and looks just like a resistor
- r_{DS} , the drain-to-source resistance decreases as V_{GS} is increased



Triode MOSFETs as switches



$$r_{DS} = \frac{1}{k_n V_{OV}} = \frac{1}{k'_n (W/L)(V_{GS} - V_t)}$$

where :

$$k_n = \left(\frac{W}{L}\right) k'_n = \text{device transconductance}$$

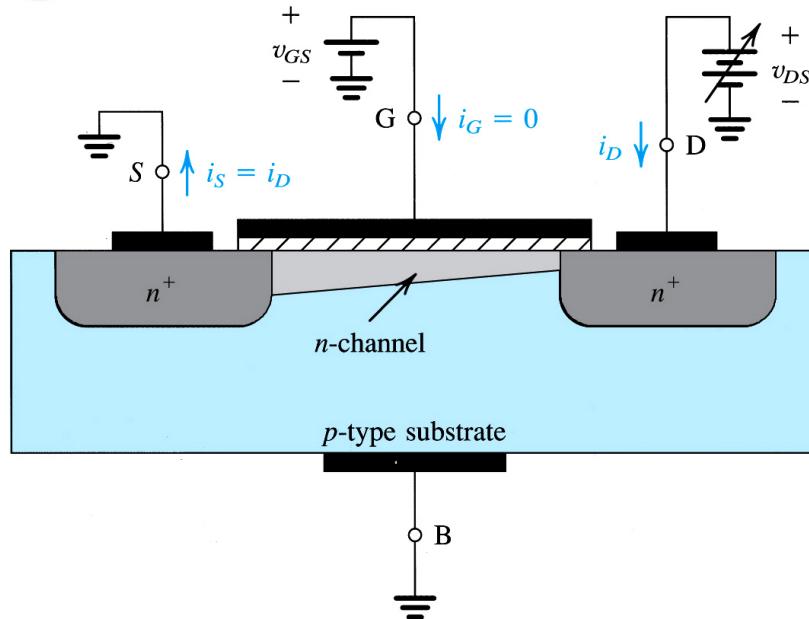
(k_n is often called β_n)

$$k'_n = \mu_n C_{OX} = \text{process transconductance}$$

- The most common use of a triode FET is as a switch
- In the example above r_{ds} is set $\ll R_D$, so when the FET switch is off $v_{ds} = V_{DD}$ and when the FET switch is on $v_{ds} \approx 0$



Triode Region



For a MOSFET in Triode :

$$I_D = k' \left(\frac{W}{L} \right) \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

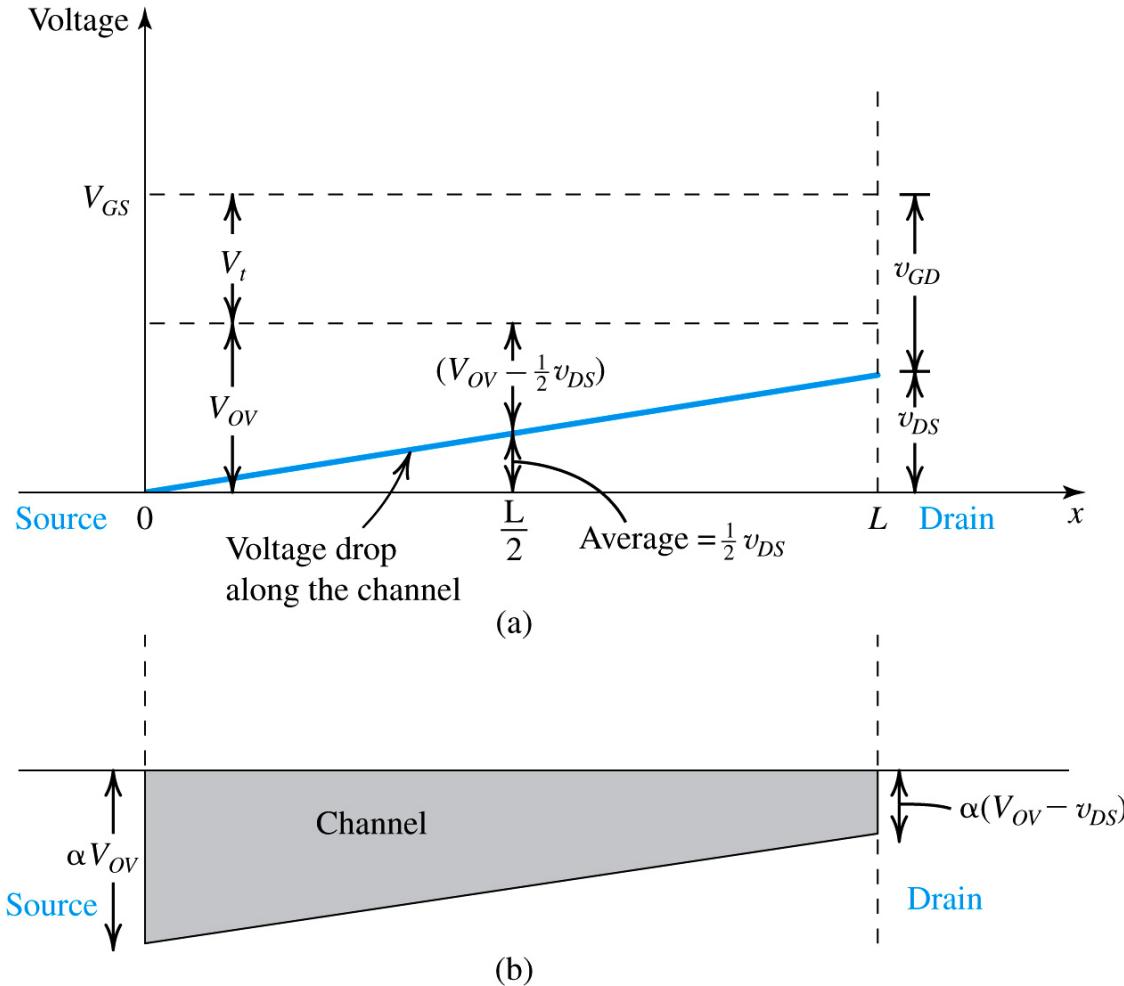
valid for : $V_{GS} > V_t$

and : $V_{DS} < V_{DS-sat} = V_{GS} - V_t$

- For a MOSFET in triode, as V_{DS} increases current flows from drain to source
- The drain current, I_D , increases linearly at first as V_{DS} is increased > 0 (for small values of V_{DS})
- As V_{DS} increases further, I_D increases more slowly since the resistance of the channel near the drain end goes up as V_{DS} increases
 - The gate-to-channel voltage is smaller at the drain end!



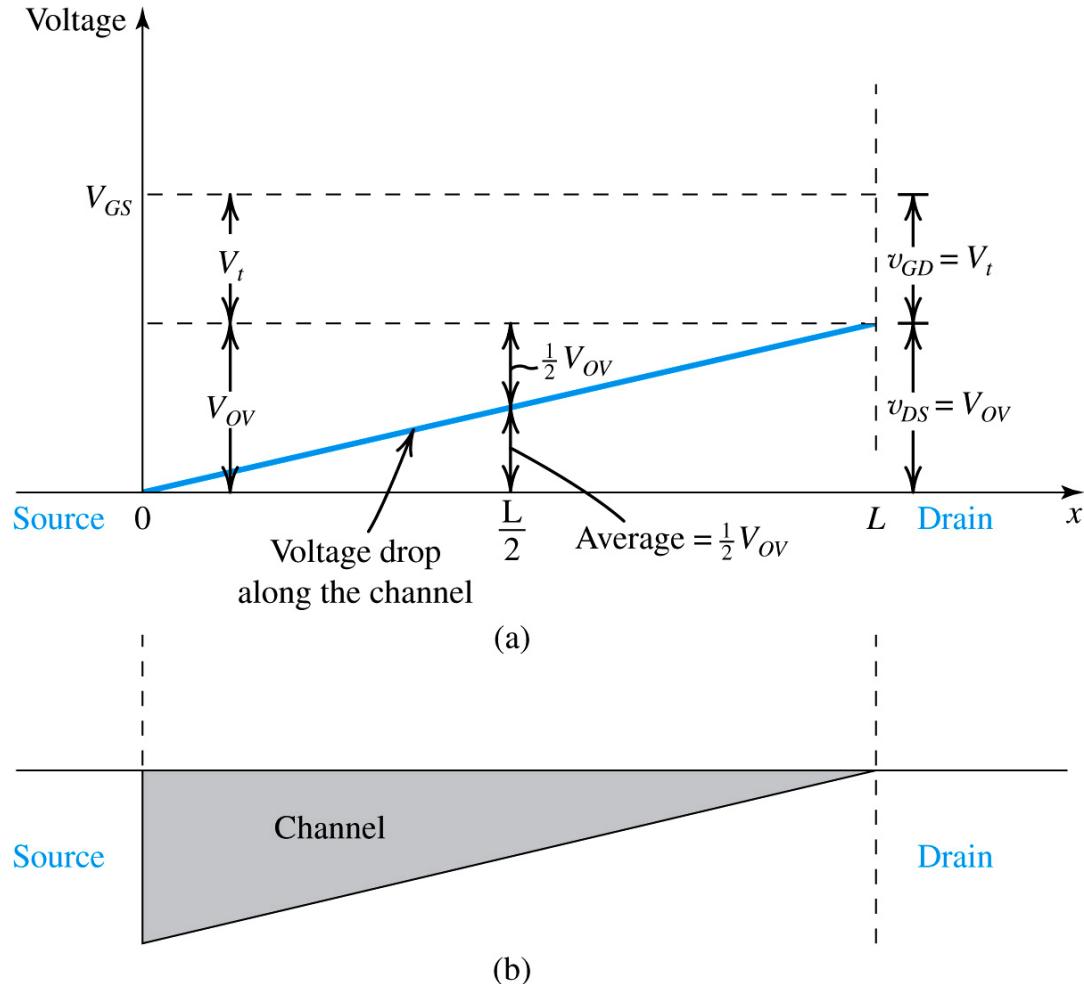
Triode Region



- The drain voltage is higher than the source voltage, so the gate-to-channel voltage is lower at the drain end than at the source end
- How much charge is in the channel at any particular point depends on the gate-to-channel voltage at that point in the channel



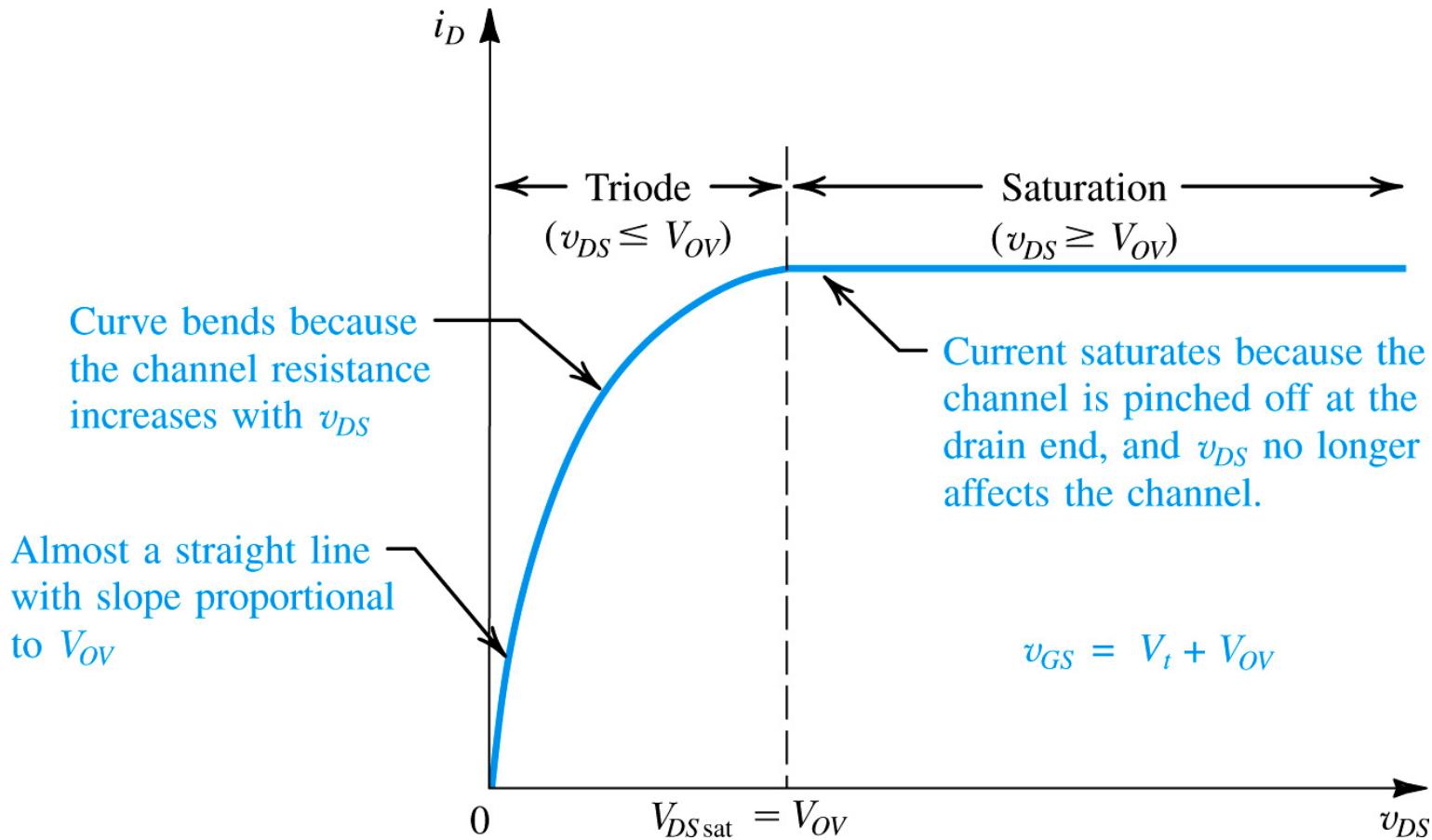
Saturation Region



- If we continue to increase V_{DS} , the gate-to-channel voltage at the drain end will eventually drop to less than V_t
- When V_{GD} is less than V_t the channel is “pinched off” (ceases to exist) near the drain!
- This is called **saturation** since I_D is \sim constant



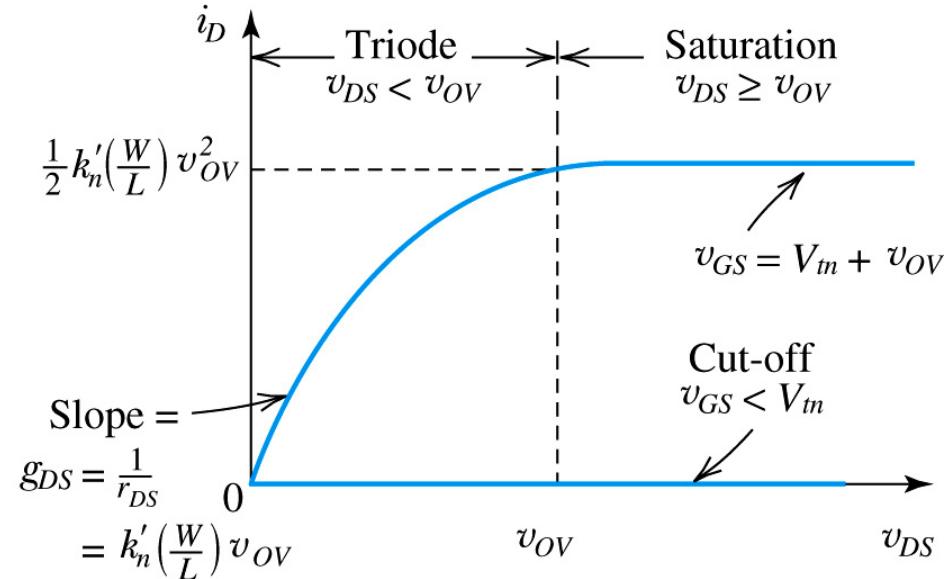
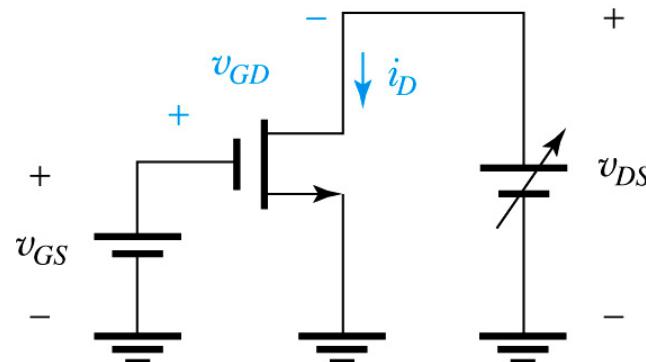
I_D vs V_{DS} Characteristic Curve



- As seen later, the I_D vs V_{DS} curve actually still has a small slope in saturation due to **channel-length modulation**



Large-signal NMOS FET I-V equations



For an NMOS in Triode :

$$I_D = k'_n \left(\frac{W}{L} \right) \left[(V_{GS} - V_{tn}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

valid for : $V_{GS} > V_{tn}$

and : $V_{DS} < V_{DS-sat} = V_{GS} - V_{tn}$

For an NMOS in Saturation :

$$I_D = \frac{k'_n}{2} \left(\frac{W}{L} \right) (V_{GS} - V_{tn})^2$$

valid for : $V_{GS} > V_{tn}$

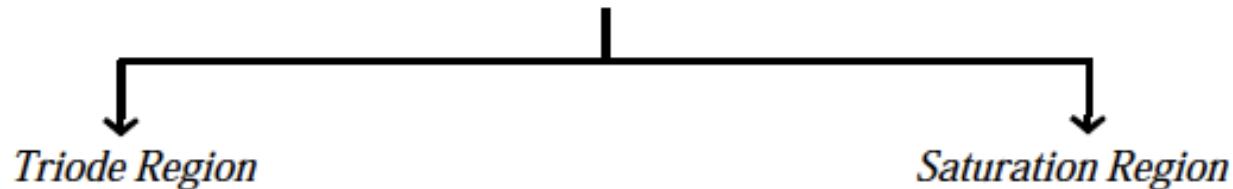
and : $V_{DS} \geq V_{DS-sat} = V_{GS} - V_{tn}$

Neglects
channel-
length
modulation



Large-signal NMOS FET I-V equations

- $v_{GS} < V_{tn}$: no channel; transistor in cut-off; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched-off at the drain end;



Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k'_n \left(\frac{W}{L} \right) \left[(v_{GS} - V_{tn}) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$$

or equivalently,

$$i_D = k'_n \left(\frac{W}{L} \right) \left(v_{OV} - \frac{1}{2} v_{DS} \right) v_{DS}$$

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

Then

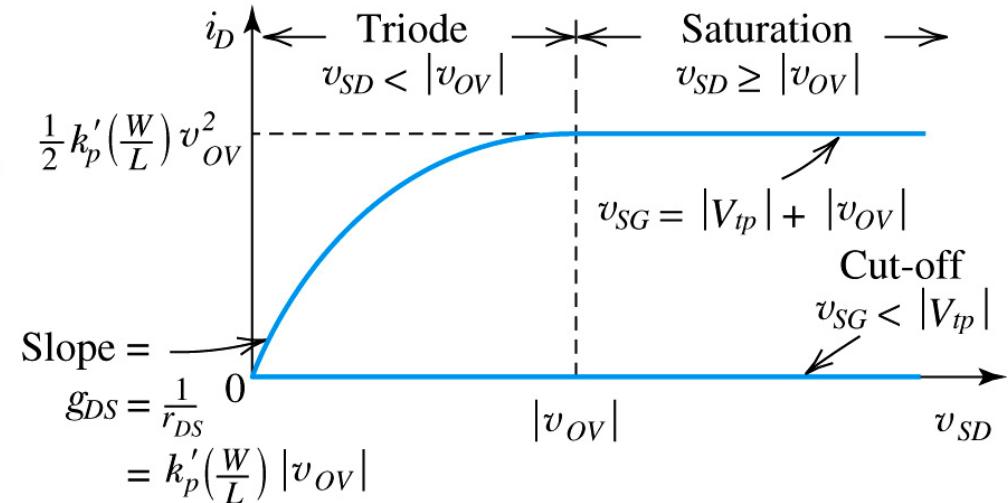
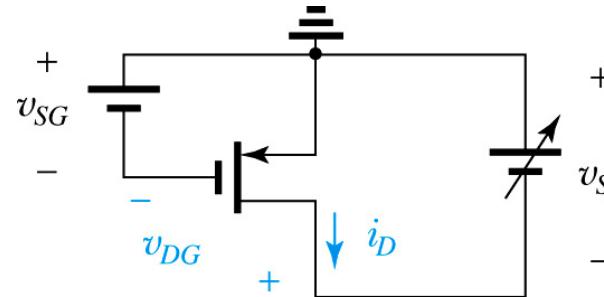
$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2$$

or equivalently,

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) v_{OV}^2$$



Large-signal PMOS FET I-V equations



For a PMOS in Triode :

$$I_D = k'_p \left(\frac{W}{L}\right) \left[(|V_{GS}| - |V_{tp}|) |V_{DS}| - \frac{1}{2} V_{DS}^2 \right]$$

valid for : $|V_{GS}| > |V_{tp}|$

and : $|V_{DS}| < |V_{DS-sat}| = |V_{GS}| - |V_{tp}|$

For a PMOS in Saturation :

$$I_D = \frac{k'_p}{2} \left(\frac{W}{L}\right) (|V_{GS}| - |V_{tp}|)^2$$

valid for : $|V_{GS}| > |V_{tp}|$

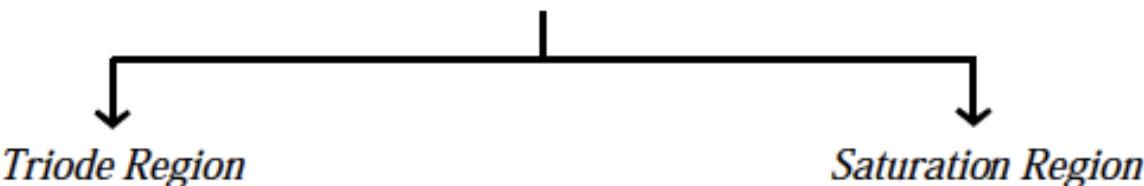
and : $|V_{DS}| \geq |V_{DS-sat}| = |V_{GS}| - |V_{tp}|$

Neglects
channel-
length
modulation



Large-signal PMOS FET I-V equations

- $v_{SG} < |V_{tp}|$: no channel; transistor in cut-off; $i_D = 0$
- $v_{SG} = |V_{tp}| + |v_{OV}|$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched-off at the drain end;



Continuous channel, obtained by:

$$v_{DG} > |V_{tp}|$$

or equivalently:

$$v_{SD} < |v_{OV}|$$

Then,

$$i_D = k'_p \left(\frac{W}{L} \right) \left[(v_{SG} - |V_{tp}|) v_{SD} - \frac{1}{2} v_{SD}^2 \right]$$

or equivalently

$$i_D = k'_p \left(\frac{W}{L} \right) \left(|v_{OV}| - \frac{1}{2} v_{SD} \right) v_{SD}$$

Pinched-off channel, obtained by:

$$v_{DG} \leq |V_{tp}|$$

or equivalently

$$v_{SD} \geq |v_{OV}|$$

Then

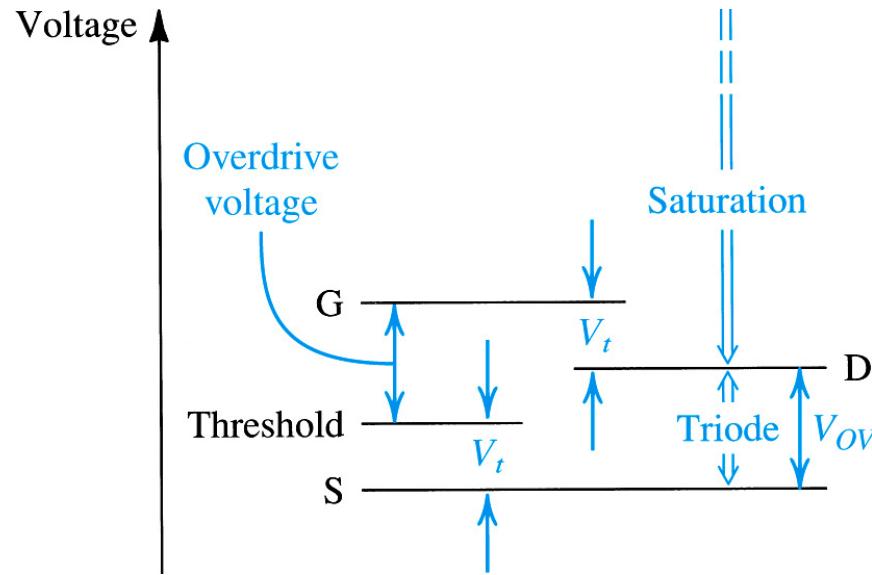
$$i_D = \frac{1}{2} k'_p \left(\frac{W}{L} \right) (v_{SG} - |V_{tp}|)^2$$

or equivalently

$$i_D = \frac{1}{2} k'_p \left(\frac{W}{L} \right) v_{OV}^2$$

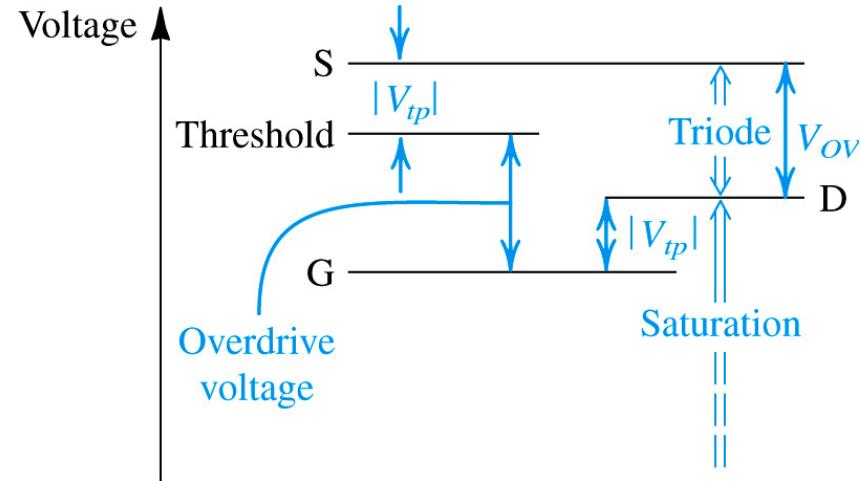


Another way to look at $V_{DS} > V_{OV}$



For NMOS FETs :

- $V_{GS} = V_t + V_{OV}$
- In Triode for $V_{DS} < V_{OV}$
- In Saturation for $V_{DS} \geq V_{OV}$ or for $V_{GD} < V_t$ (same!)



For PMOS FETs :

- $|V_{GS}| = |V_t| + |V_{ov}|$
- In Triode for $|V_{DS}| < |V_{ov}|$
- In Saturation for $|V_{DS}| \geq |V_{ov}|$ or for $|V_{GD}| < |V_t|$ (same!)



Example 5.2

Consider an NMOS transistor fabricated in a 0.18- μm process with $L = 0.18 \mu\text{m}$ and $W = 2 \mu\text{m}$. The process technology is specified to have $C_{ox} = 8.6 \text{ fF}/\mu\text{m}^2$, $\mu_n = 450 \text{ cm}^2/\text{V}\cdot\text{s}$, and $V_{tn} = 0.5 \text{ V}$.

- Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with $I_D = 100 \mu\text{A}$.
- If V_{GS} is kept constant, find V_{DS} that results in $I_D = 50 \mu\text{A}$.
- To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with $V_{DS} = 0.3 \text{ V}$. Find the change in I_D resulting from v_{GS} changing from 0.7 V by +0.01 V and by -0.01 V.

Solution

First we determine the process transconductance parameter k'_n

$$\begin{aligned}k'_n &= \mu_n C_{ox} \\&= 450 \times 10^{-4} \times 8.6 \times 10^{-15} \times 10^{12} \text{ A/V}^2 \\&= 387 \mu\text{A/V}^2\end{aligned}$$

and the transistor transconductance parameter k_n ,

$$\begin{aligned}k_n &= k'_n \left(\frac{W}{L} \right) \\&= 387 \left(\frac{2}{0.18} \right) = 4.3 \text{ mA/V}^2\end{aligned}$$



(a) With the transistor operating in saturation,

$$I_D = \frac{1}{2}k_n V_{OV}^2$$

Thus,

$$100 = \frac{1}{2} \times 4.3 \times 10^3 \times V_{OV}^2$$

which results in

$$V_{OV} = 0.22 \text{ V}$$

Thus,

$$V_{GS} = V_{tn} + V_{OV} = 0.5 + 0.22 = 0.72 \text{ V}$$

and since operation is at the edge of saturation,

$$V_{DS} = V_{OV} = 0.22 \text{ V}$$

(b) With V_{GS} kept constant at 0.72 V and I_D reduced from the value obtained at the edge of saturation, the MOSFET will now be operating in the triode region, thus

$$I_D = k_n \left[V_{OV} V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$50 = 4.3 \times 10^3 \left[0.22 V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

which can be rearranged to the form

$$V_{DS}^2 - 0.44 V_{DS} + 0.023 = 0$$



This quadratic equation has two solutions

$$V_{DS} = 0.06 \text{ V} \quad \text{and} \quad V_{DS} = 0.39 \text{ V}$$

The second answer is greater than V_{OV} and thus is physically meaningless, since we know that the transistor is operating in the triode region. Thus we have

$$V_{DS} = 0.06 \text{ V}$$

(c) For $v_{GS} = 0.7 \text{ V}$, $V_{OV} = 0.2 \text{ V}$, and since $V_{DS} = 0.3 \text{ V}$, the transistor is operating in saturation and

$$\begin{aligned} I_D &= \frac{1}{2} k_n V_{OV}^2 \\ &= \frac{1}{2} \times 4300 \times 0.04 \\ &= 86 \mu\text{A} \end{aligned}$$

Now for $v_{GS} = 0.710 \text{ V}$, $v_{OV} = 0.21 \text{ V}$ and

$$I_D = \frac{1}{2} \times 4300 \times 0.21^2 = 94.8 \mu\text{A}$$

and for $v_{GS} = 0.690 \text{ V}$, $v_{OV} = 0.19 \text{ V}$, and

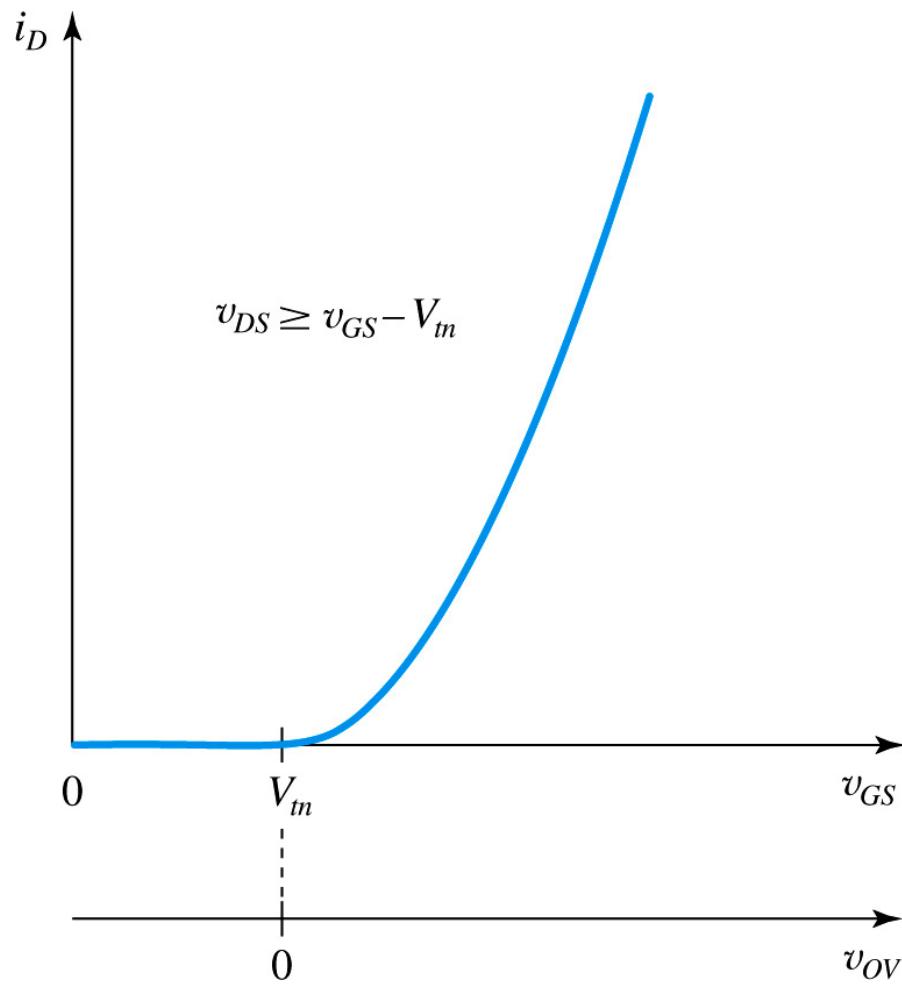
$$I_D = \frac{1}{2} \times 4300 \times 0.19^2 = 77.6 \mu\text{A}$$

Thus, with $\Delta V_{GS} = +0.01 \text{ V}$, $\Delta I_D = 8.8 \mu\text{A}$; and for $\Delta V_{GS} = -0.01 \text{ V}$, $\Delta I_D = -8.4 \mu\text{A}$.

We conclude that the two changes are almost equal, an indication of almost-linear operation when the changes in v_{GS} are kept small. This is just a preview of the “small-signal operation” of the MOSFET studied in Sections 5.4 and 5.5.



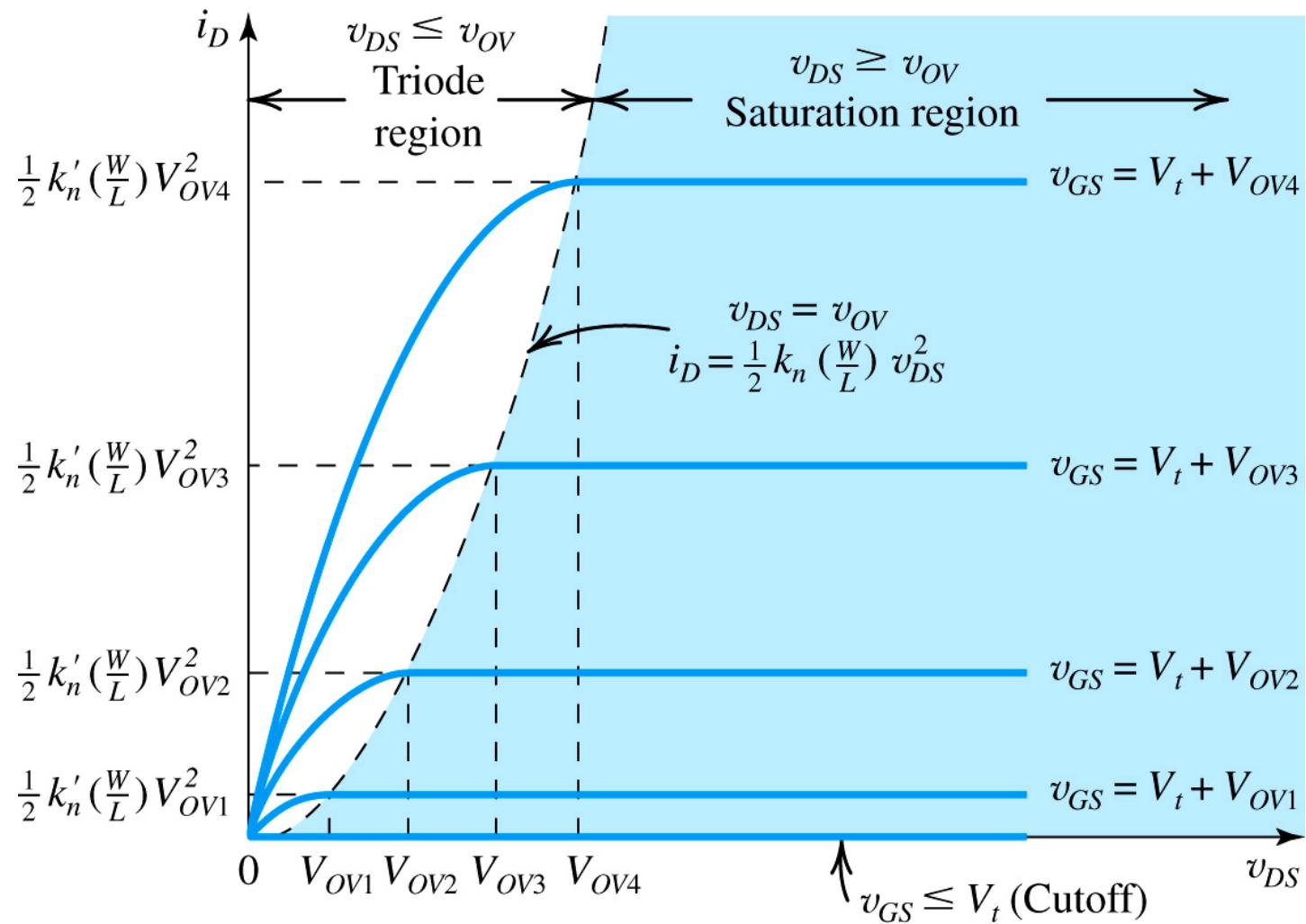
Id vs Vgs in Saturation



- In saturation the drain current, I_D , increases proportional to the square of $V_{OV} = V_{GS} - V_t$
- Because of this, MOSFETs are often referred to as “square law devices”
- Can plot I_D versus V_{GS} (usually done), or instead plot I_D versus V_{OV} just by shifting the x-axis by V_t (i.e., redefine where $x = 0$)



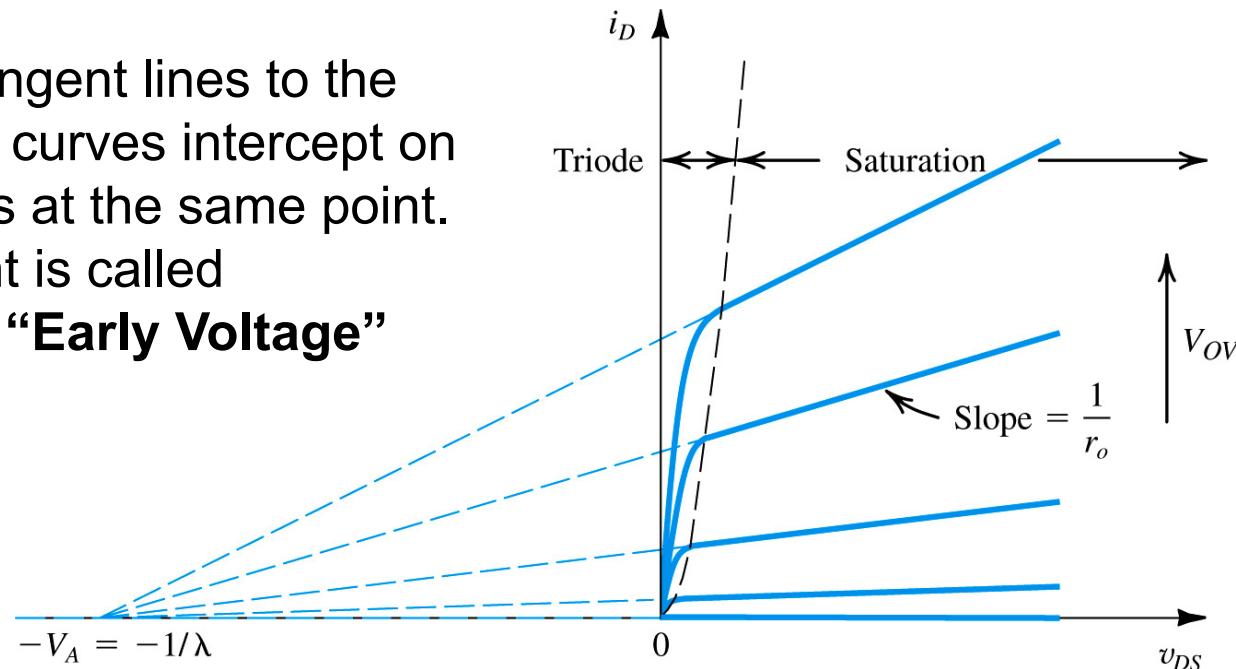
i_D vs V_{DS} curves as V_{GS} is increased





Channel-length Modulation

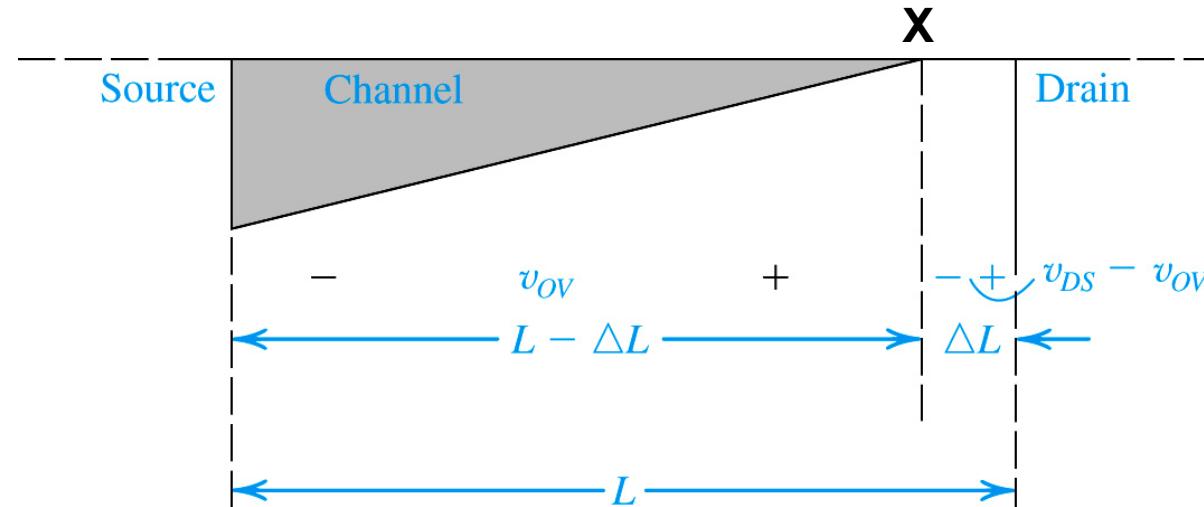
All the tangent lines to the I_D vs V_{DS} curves intercept on the x-axis at the same point. This point is called **V_A = the “Early Voltage”**



- MOSFET I_D vs V_{DS} curves actually do have a small slope in saturation. That is, I_D does increase slightly as V_{DS} increases. This is due to **channel-length modulation**.
→ *This wasn't included in the I-V equations discussed so far, so we need to add another term to the equations to model this effect!*



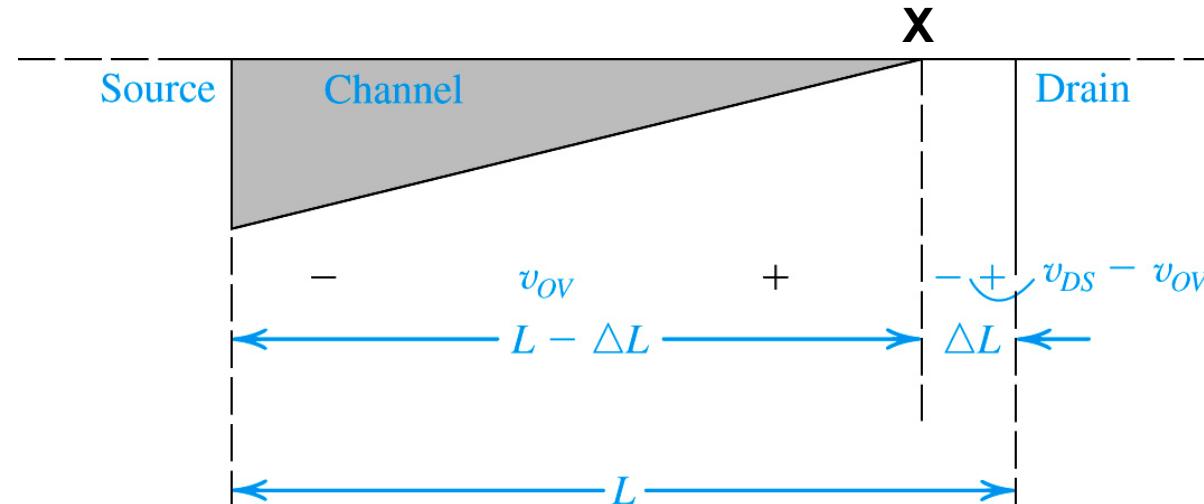
Channel-length Modulation



- In saturation the channel pinches off near the drain end, since V_{GD} is $< V_t$, the minimum gate-to-channel voltage required for the channel to exist. At the “tip of the triangle” (point x) the gate-to-channel voltage is exactly equal to V_t
 $V_{Gx} = V_G - V_x = V_{GS} - V_{xs} = V_t \rightarrow V_{xs} = V_{GS} - V_t = V_{ov}$
→ **The voltage across the channel = $V_{ov} = V_{GS} - V_t$**
→ **All of $V_{DS} > V_{ov}$ appears across the depletion region!**



Channel-length Modulation



- As V_{DS} is increased above V_{OV} , the extra V_{DS} all appears across the depletion region between the end of the channel and the drain. Therefore as V_{DS} is increased this depletion region gets wider, which pushes the “tip of the triangle” back closer to the source → The channel gets shorter!
- This causes the resistance of the channel to go down as V_{DS} increases. With the same voltage drop across a smaller resistance, the drain current has to increase!



Channel-length Modulation

For NMOS FETs in Saturation :

$$I_D = \frac{1}{2} k_n \left(\frac{W}{L} \right) (V_{GS} - V_{tn})^2 (1 + \lambda_n V_{DS})$$

or,

$$I_D = \frac{1}{2} k_n \left(\frac{W}{L} \right) (V_{GS} - V_{tn})^2 \left(1 + V_{DS}/V_{An} \right)$$

where : $V_{An} = \frac{1}{\lambda_n}$ and : $V_{An} \propto L$

For PMOS FETs in Saturation :

$$I_D = \frac{1}{2} k_p \left(\frac{W}{L} \right) (|V_{GS}| - |V_{tp}|)^2 (1 + \lambda_p |V_{DS}|)$$

or,

$$I_D = \frac{1}{2} k_p \left(\frac{W}{L} \right) (|V_{GS}| - |V_{tp}|)^2 \left(1 + |V_{DS}|/V_{Ap} \right)$$

where : $V_{Ap} = \frac{1}{\lambda_p}$ and : $V_{Ap} \propto L$

- To model the channel-length modulation effect in our I_D equations, we add a term including either lambda or V_A
- V_A goes up as L increases, since ΔL is a smaller fraction of L



Body Effect

- The MOS threshold voltage is actually a function of V_{SB} , the source-to-body voltage. This is called **body effect**.
- This is true because the capacitance from gate-to-channel is actually in series with the depletion region capacitance between the channel and the body. As V_{SB} increases the depletion region widens, which reduces the channel depth. To return the channel to its former size V_{GS} must increase, which is modeled as an increase in the threshold voltage.
- For uniform body doping, V_t is a nonlinear function of V_{SB} :

$$V_t = V_{t0} + \gamma \left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f} \right]$$

$$\text{with : } \gamma = \frac{\sqrt{2qN_{sub}\epsilon_S}}{C_{ox}}$$

$$\phi_f = \frac{kT}{q} \ln \left(\frac{N_{sub}}{n_i} \right)$$

- Modern IC FETs use retrograde body doping, which causes a linear variation in V_t : $V_t = V_{t0} + \alpha V_{SB}$ where : $\alpha = 3t_{ox}/W_{d\ max}$



Other important 2nd and 3rd order effects

- **Leakage currents:** PN junction leakage (worse at high T), gate leakage (for $L \leq 0.13\mu m$), sub-threshold leakage
- **Drain-Induced Barrier Lowering (DIBL):** V_t goes down at short channel lengths, since V_D helps to form the channel
- **Velocity saturation:** Carrier velocity reaches a maximum at high electric field strengths, and $v = \mu E$ is no longer true
- **Mobility degradation:** Mobility drops at high V_{GS} values due to increased surface collisions for high vertical E-field
- **Breakdown:** PN junctions break down at high reverse bias
- **Punch-through:** If the depletion regions surrounding the drain and source touch (at high V_{DS}), very large I_D can flow
- **Temperature effects:** As temperature increases both V_t and μ (and therefore k') decrease, causing I_D to go down



DC biasing of MOSFETs

- Similar to PN junction diodes, MOSFETs need to be biased “on” in order to respond to small-signal variations in the input signal.
- For discrete circuits on printed circuit boards (PCBs), this is usually done using several resistors to set the DC voltage levels and currents, plus coupling and bypass capacitors to separate the DC levels between circuits.
- For integrated circuits these capacitors and resistors are too large (and therefore expensive) to be practical. Instead MOS circuits on ICs are biased using transistor current sources to set the DC current values. Since coupling capacitors cannot be used to separate the DC bias between circuits, they are DC-coupled instead (i.e., the DC bias of circuits interact with one another).



Example 5.3

Design the circuit of Fig. 5.21, that is, determine the values of R_D and R_S , so that the transistor operates at $I_D = 0.4 \text{ mA}$ and $V_D = +0.5 \text{ V}$. The NMOS transistor has $V_t = 0.7 \text{ V}$, $\mu_n C_{ox} = 100 \mu\text{A/V}^2$, $L = 1 \mu\text{m}$, and $W = 32 \mu\text{m}$. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

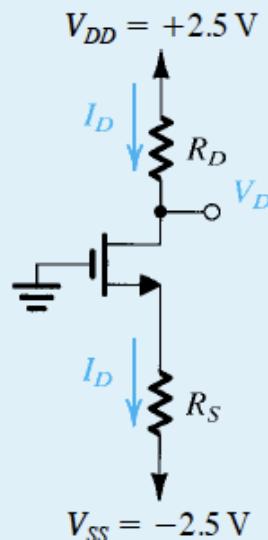


Figure 5.21 Circuit for Example 5.3.

Solution

To establish a dc voltage of $+0.5 \text{ V}$ at the drain, we must select R_D as follows:

$$\begin{aligned} R_D &= \frac{V_{DD} - V_D}{I_D} \\ &= \frac{2.5 - 0.5}{0.4} = 5 \text{ k}\Omega \end{aligned}$$



To determine the value required for R_S , we need to know the voltage at the source, which can be easily found if we know V_{GS} . This in turn can be determined from V_{OV} . Toward that end, we note that since $V_D = 0.5$ V is greater than V_G , the NMOS transistor is operating in the saturation region, and we can use the saturation-region expression of I_D to determine the required value of V_{OV} ,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{OV}^2$$

Then substituting $I_D = 0.4$ mA = 400 μ A, $\mu_n C_{ox} = 100$ μ A/V², and $W/L = 32/1$ gives

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} V_{OV}^2$$

which results in

$$V_{OV} = 0.5$$
 V

Thus,

$$V_{GS} = V_t + V_{OV} = 0.7 + 0.5 = 1.2$$
 V

Referring to Fig. 5.21, we note that the gate is at ground potential. Thus, the source must be at -1.2 V, and the required value of R_S can be determined from

$$\begin{aligned} R_S &= \frac{V_S - V_{SS}}{I_D} \\ &= \frac{-1.2 - (-2.5)}{0.4} = 3.25 \text{ k}\Omega \end{aligned}$$



Example 5.6

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1 \text{ V}$ and $k'_n(W/L) = 1 \text{ mA/V}^2$. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

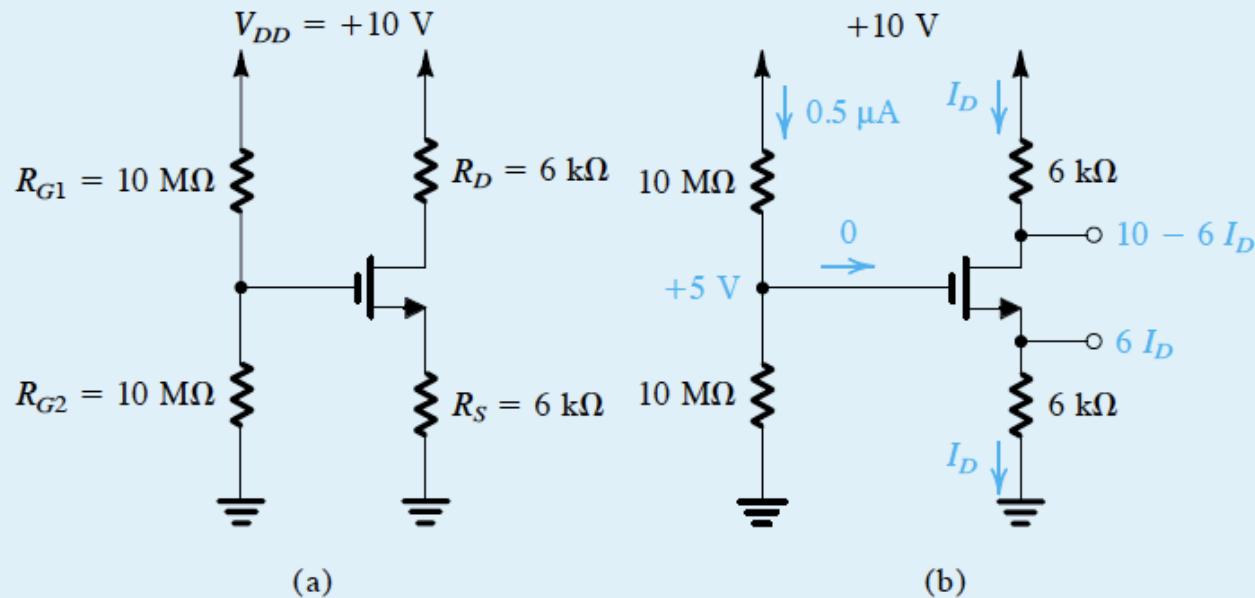


Figure 5.24 (a) Circuit for Example 5.6. (b) The circuit with some of the analysis details shown.

Solution

Since the gate current is zero, the voltage at the gate is simply determined by the voltage divider formed by the two $10\text{-M}\Omega$ resistors,

$$V_G = V_{DD} \frac{R_{G2}}{R_{G2} + R_{G1}} = 10 \times \frac{10}{10 + 10} = +5 \text{ V}$$



With this positive voltage at the gate, the NMOS transistor will be turned on. We do not know, however, whether the transistor will be operating in the saturation region or in the triode region. We shall assume saturation-region operation, solve the problem, and then check the validity of our assumption. Obviously, if our assumption turns out not to be valid, we will have to solve the problem again for triode-region operation.

Refer to Fig. 5.24(b). Since the voltage at the gate is 5 V and the voltage at the source is I_D (mA) \times 6 ($k\Omega$) = $6I_D$, we have

$$V_{GS} = 5 - 6I_D$$

Thus, I_D is given by

$$\begin{aligned} I_D &= \frac{1}{2}k'_n \frac{W}{L}(V_{GS} - V_{tn})^2 \\ &= \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2 \end{aligned}$$

which results in the following quadratic equation in I_D :

$$18I_D^2 - 25I_D + 8 = 0$$

This equation yields two values for I_D : 0.89 mA and 0.5 mA. The first value results in a source voltage of $6 \times 0.89 = 5.34$ V, which is greater than the gate voltage and does not make physical sense as it would imply that the NMOS transistor is cut off. Thus,

$$I_D = 0.5 \text{ mA}$$

$$V_S = 0.5 \times 6 = +3 \text{ V}$$

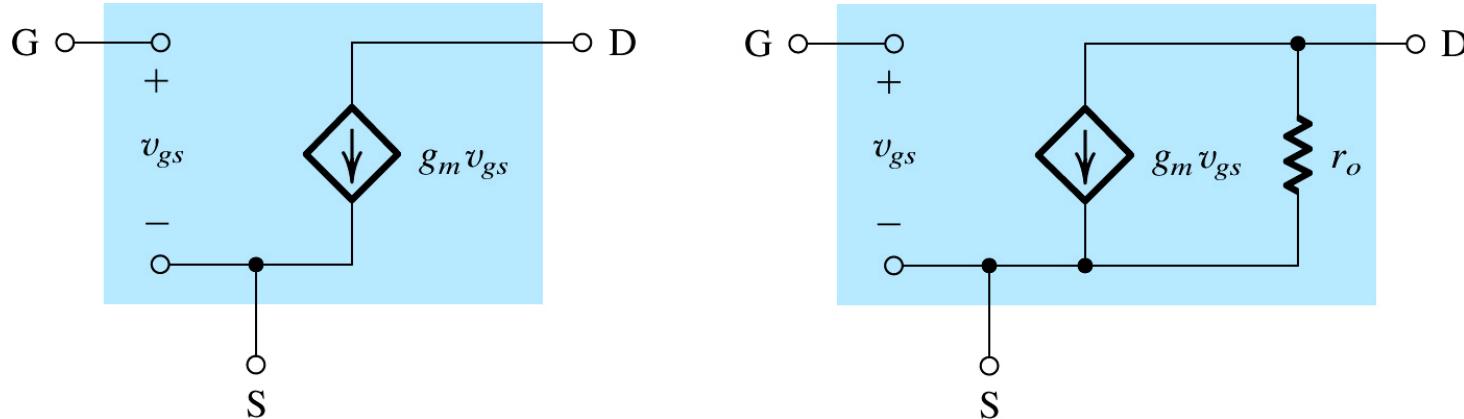
$$V_{GS} = 5 - 3 = 2 \text{ V}$$

$$V_D = 10 - 6 \times 0.5 = +7 \text{ V}$$

Since $V_D > V_G - V_{tn}$, the transistor is operating in saturation, as initially assumed.



Small-signal MOSFET models



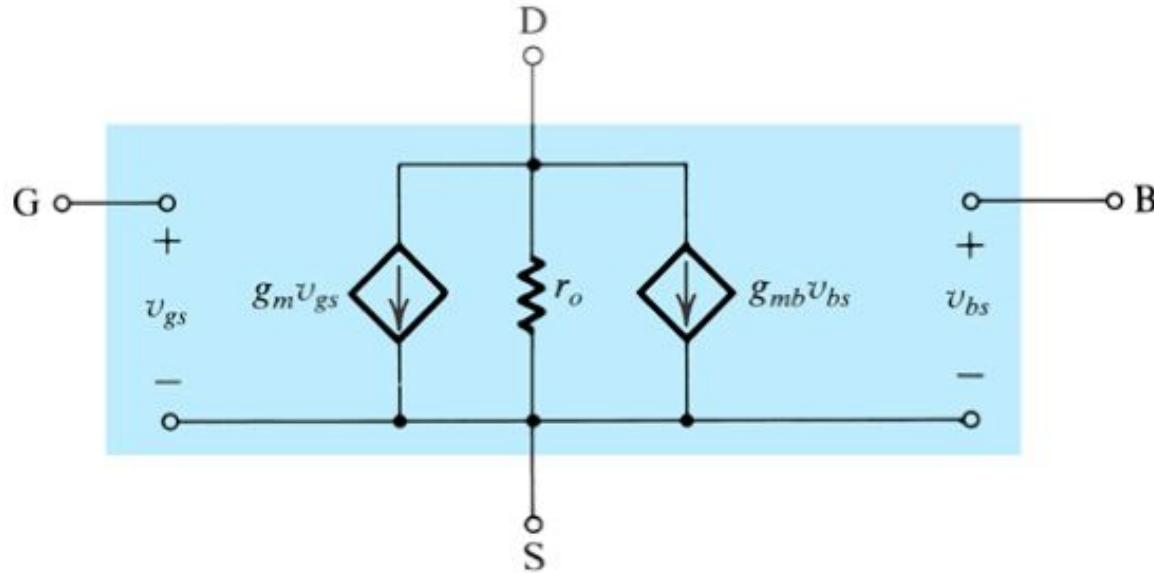
- For small-signal analysis MOSFETs in saturation are modeled with a g_m transconductance source (i_d controlled by v_{gs}), plus an output resistance called r_o (also called r_{ds})

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = k' \frac{W}{L} (V_{GS} - V_t) = \sqrt{2k' \frac{W}{L} I_D} = \frac{2I_D}{V_{GS} - V_t} = \frac{2I_D}{V_{OV}}$$

$$r_o = r_{ds} = \frac{1}{g_{ds}} = \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1} = \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$$



Small-signal MOSFET models



- For MOSFETs with $V_{SB} \neq 0$ an additional transconductance source is added to model the dependence of I_D on V_{SB} due to the body effect. This g_{mb} source is called the **back gate**

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \chi g_m$$

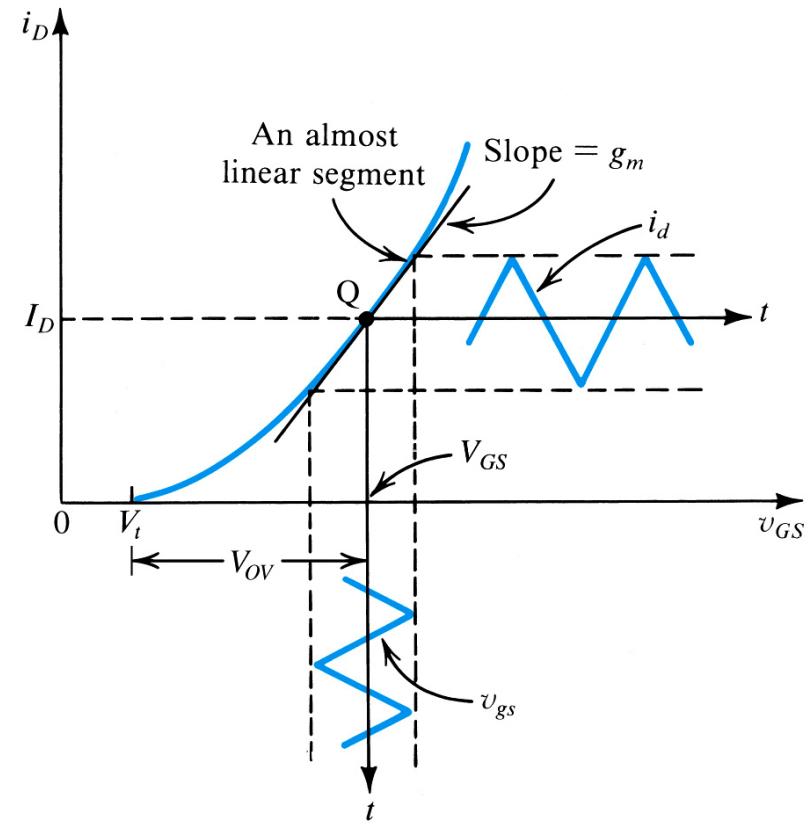
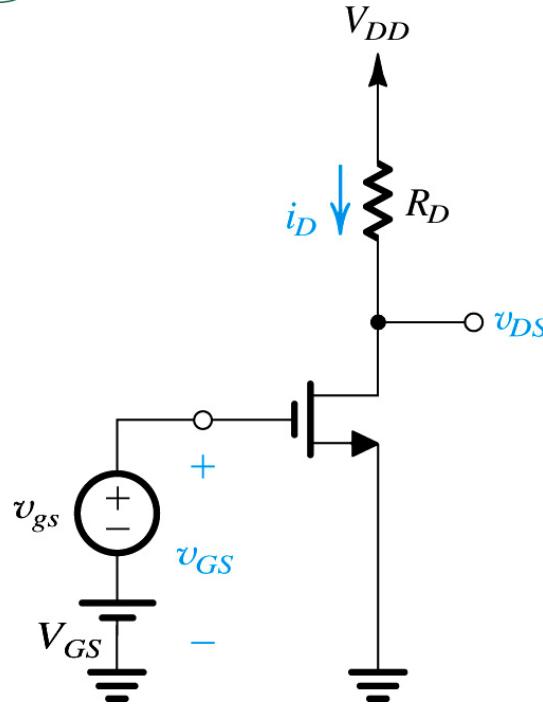
where for uniform body doping :

$$\chi = \frac{\partial V_t}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}}$$

and for retrograde body doping : $\chi = \alpha = 3t_{OX}/W_{d\max}$



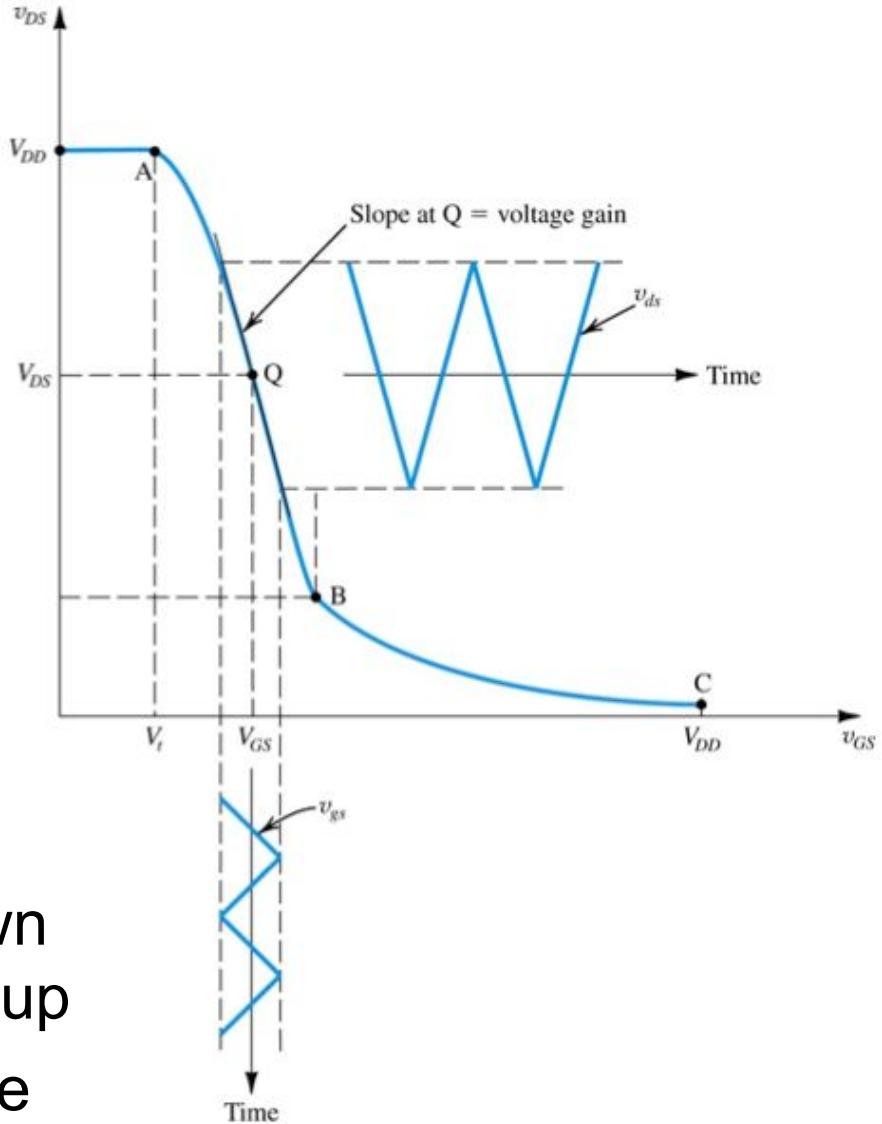
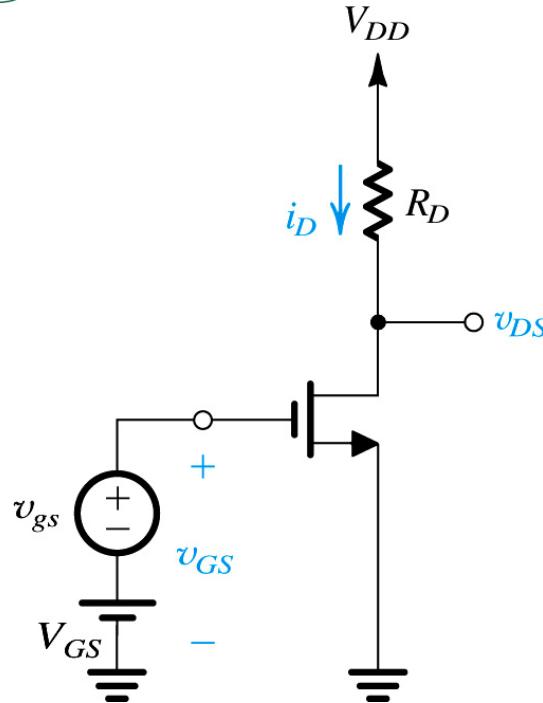
MOSFETs as voltage amplifiers



- MOSFET amplifiers can be analyzed using standard linear circuit analysis techniques for small-signal variations around a DC bias point (a.k.a. a DC operating point or Q-point)



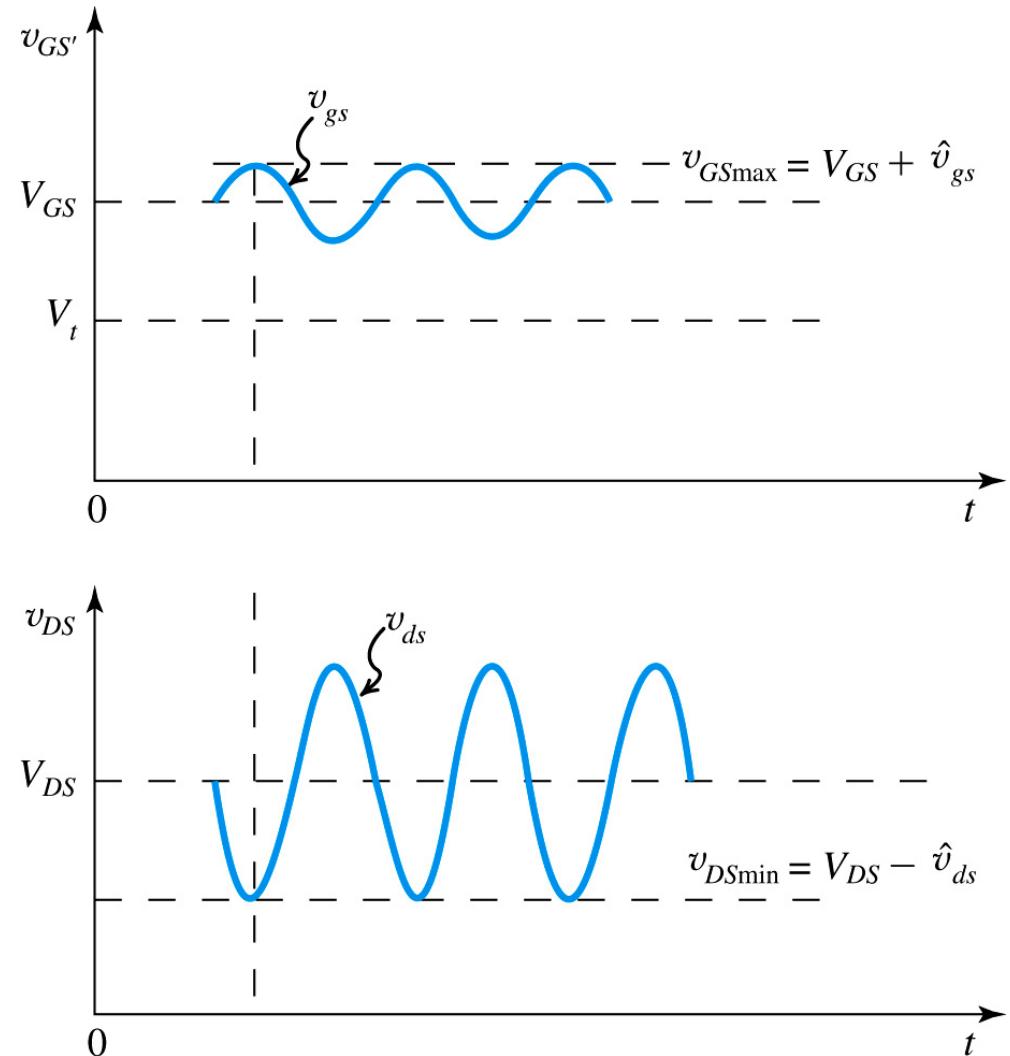
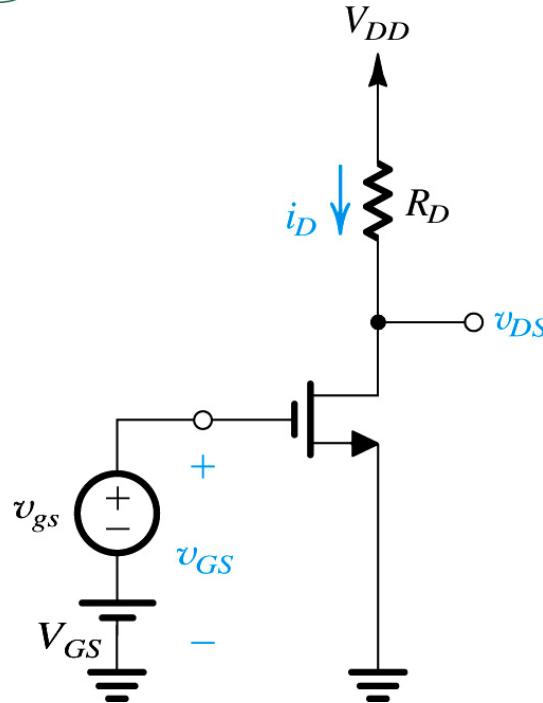
MOSFETs as voltage amplifiers



- This voltage amplifier inverts the input signal (the gain is negative) since V_{DS} goes down as V_{GS} and therefore I_D goes up
- $A_V = \text{slope of } V_{DS} \text{ vs } V_{GS} \text{ curve}$



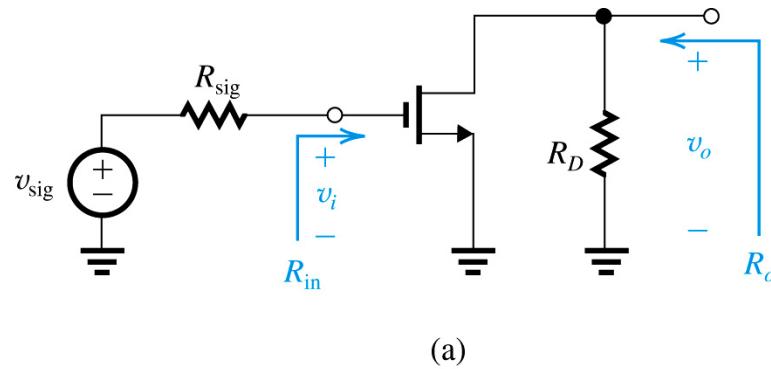
MOSFETs as voltage amplifiers



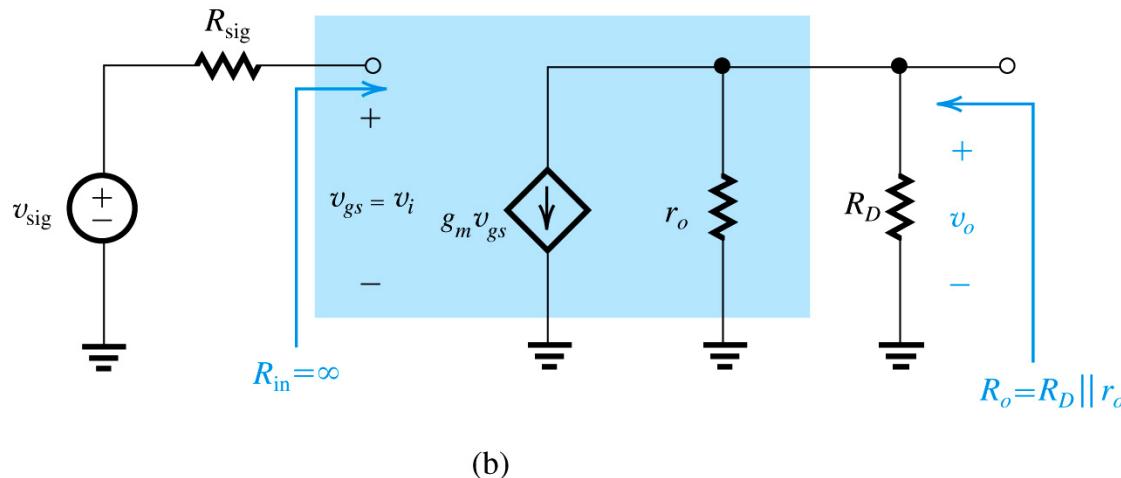
- Small-signal variations occur around the DC bias point
- These can be added to get the total values



Example of a MOSFET Voltage Amp



(a)



(b)

To find the gain :

1. Find DC bias point
2. Calculate the values of the small-signal parameters g_m , r_o , at the DC bias point
3. Solve for the value of the small-signal voltage gain at this DC bias point :

$$A_V = -g_m (r_o \parallel R_D)$$



Example of a MOSFET Voltage Amp

For the MOSFET amplifier shown, find the voltage gain if :

$I_D = 400 \mu A$, $R_D = 25 k\Omega$, $W/L = 200$, $k' = 100 \mu A/V^2$, $\lambda = 0.1 V^{-1}$

Solution :

1st, find the small-signal parameters at this bias point :

$$I_D = \frac{k' W}{2 L} (V_{GS} - V_t)^2 \Rightarrow V_{OV} = \sqrt{\frac{2I_D}{k'(W/L)}} = \sqrt{\frac{2(400)}{100(200)}} = 0.2V$$

$$\Rightarrow gm = \frac{2I_D}{V_{OV}} = \frac{2(400)}{0.2} = 4000 \mu A/V = 4 mA/V$$

$$and \ g_{ds} = \lambda I_D = (0.1)(400) = 40 \mu A/V \Rightarrow r_{ds} = 1/g_{ds} = 25 k\Omega$$

$$Then : A_V = -g_m(R_D \parallel r_{ds}) = -4(25 \parallel 25) = -50 \Rightarrow A_V = -50 V/V$$

Note that λ must be included to find gain, but is often neglected for bias



Summary of Key Concepts

- NMOS and PMOS FET device structures & symbols
- Regions of Operation
 - Cutoff, Triode, Saturation, Sub-Threshold
- Large-signal MOSFET I-V equations
- Key second-order effects
 - Channel-length modulation, Body effect
- Additional important 2nd and 3rd order effects
 - Leakage currents, DIBL, velocity saturation, mobility degradation, breakdown & punch-through, temperature effects
- DC biasing of MOSFETs
- Small-signal MOSFET models
- Using MOSFETs as voltage amplifiers