CpE 151 CMOS and VLSI Design

Section 3

Project 1

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INTRODUCTION

In this project, the student was introduced to a new tool called Cadence Virtuoso tool that includes some widely used basic CMOS logic gates. The objective is to understand and be able to layout some basic CMOS logic gates that were taught in the discussion class. There are five required circuits needed to be laid out including: an inverter, 2-input NAND gate, 2-input NOR gate, 2-input XOR gate, and a complex gate. For each gate, it requires a schematic and layout designs as well as creating a symbol to use for testbench and analyze the simulation.

CIRCUITS

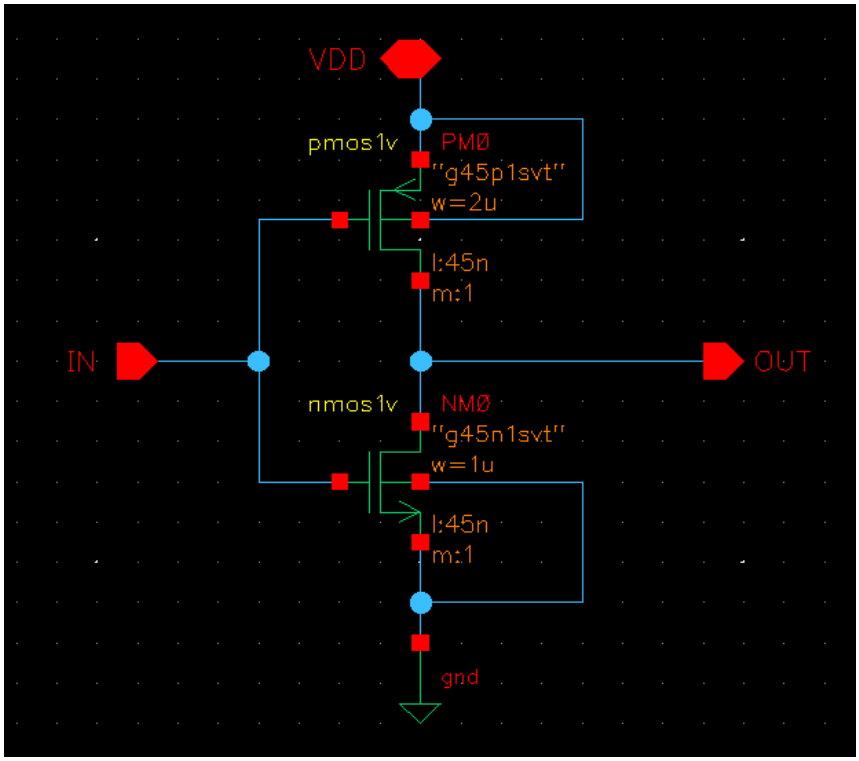
1. Inverter

Design Purpose:

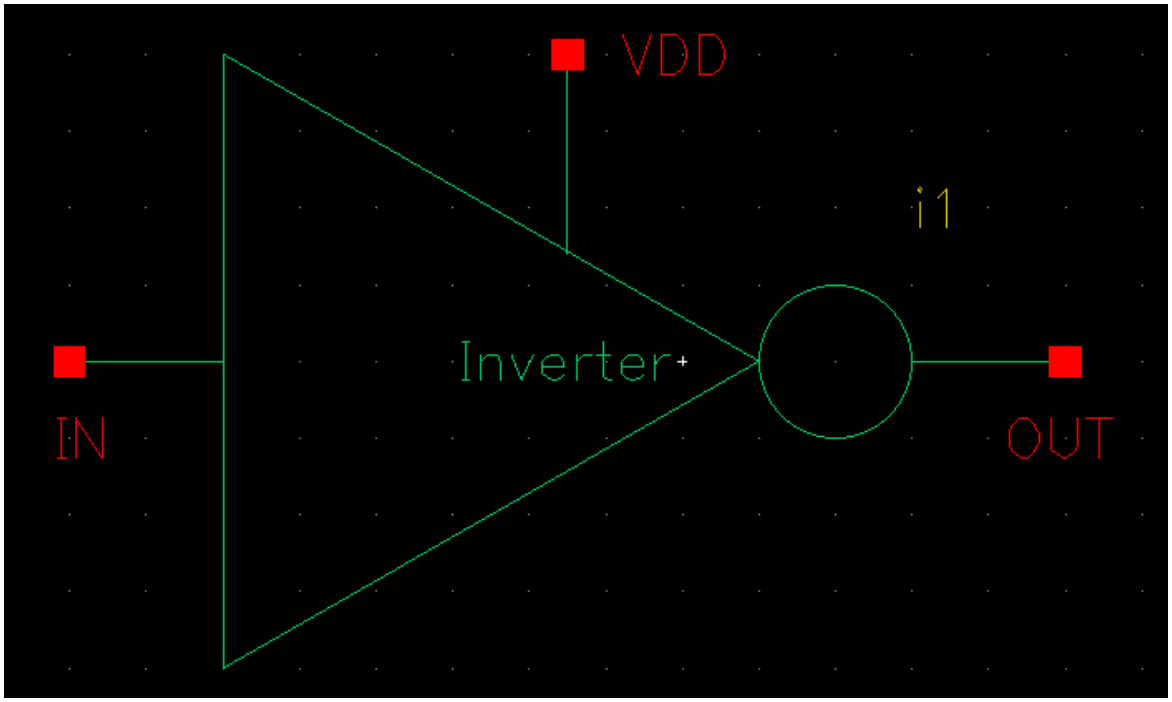
The purpose for this is to build the most basic schematic diagram using PMOS and NMOS. The inverter only uses 1 PMOS and 1 NMOS with 1 input and 1 output. For the inverter, I am required to use (W/L)n = 1.0/0.045 and (W/L)p = 2.0/0.045 in μm.

Engineering Data:

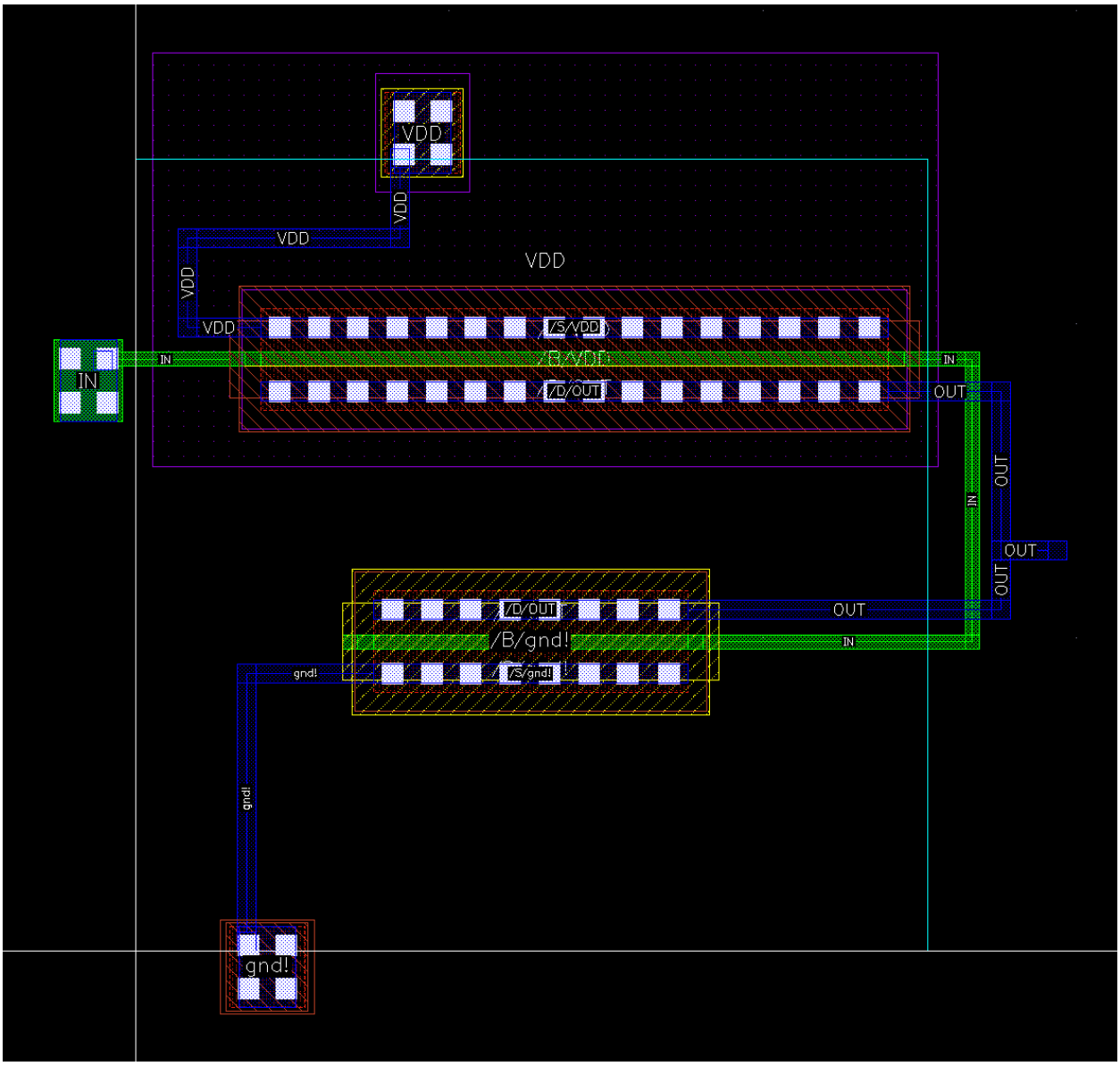
For the schematic diagram, I used the PMOS and connected the important parts: VDD to the drain, output to source, and input to gate. On the other hand, I also used an NMOS connected the following parts: output to drain, ground to source, and input to gate. Below is the full schematic diagram for the inverter.



After that, I created a symbol for the inverter that will be used for testbench later. Below is the inverter symbol.

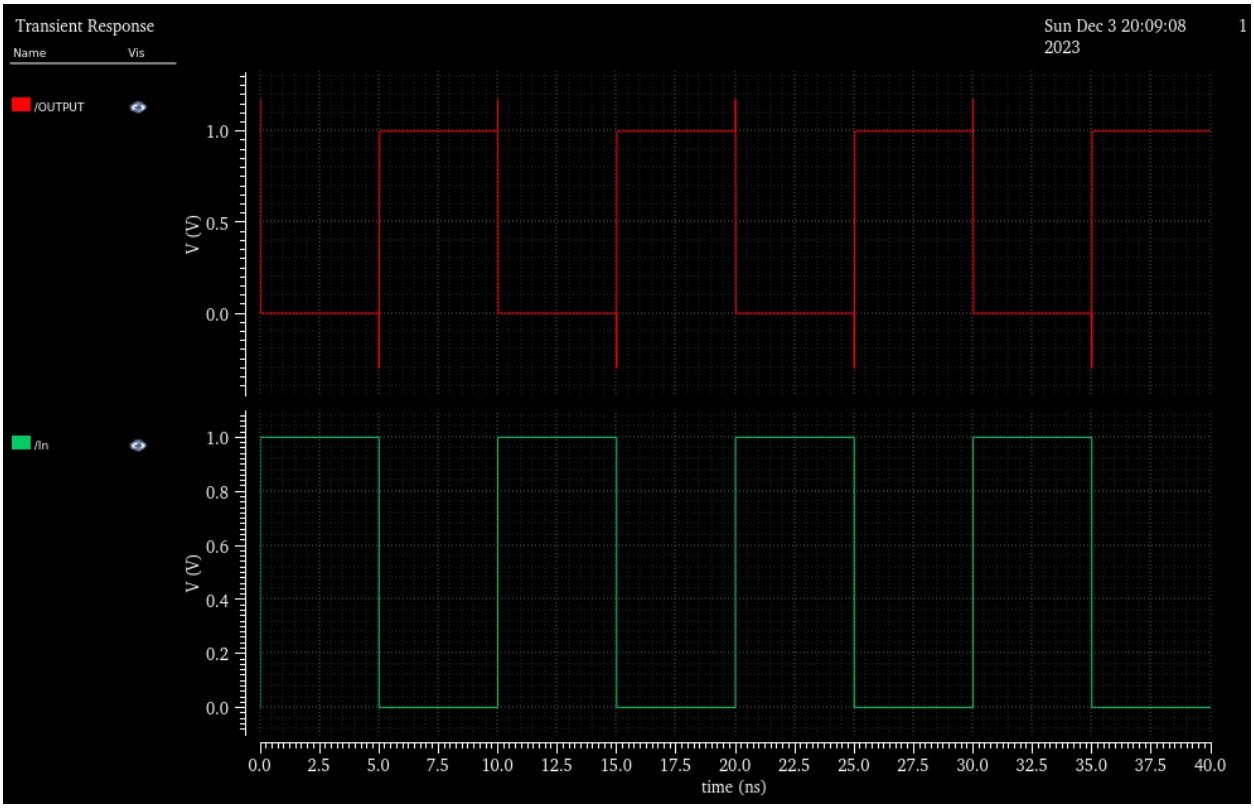


On the other hand, I created a layout for the inverter by generating the instances from the schematic diagram I designed earlier and connect the right parts. After that, I was able to complete the design which is shown below.



Simulation:

After the design, I did a simulation using the symbol created as instance earlier. I was able to connect the Vdc using 1V to VDD and Vpulse to the input with Voltage 1 = 0V (logic low), Voltage 2 = 1V (logic high), Rise time = 10ps, Fall time = 10ps, Period=10ns, Pulse width =5ns, and add GND. After that, I ran the ADE L and set the analysis to tran and Stop Time to 40 ns. Below is the simulation result.



Result Discussion

After the design layout, I was able to check DRC and LVS which gave me no errors and was able to do the simulation. On the other hand, I got couple of problems encountered throughout the process of designing the layout including the overlapping and not connected wires. Other than that, I was able to do extraction, but the extraction view doesn't show the same as the instruction.

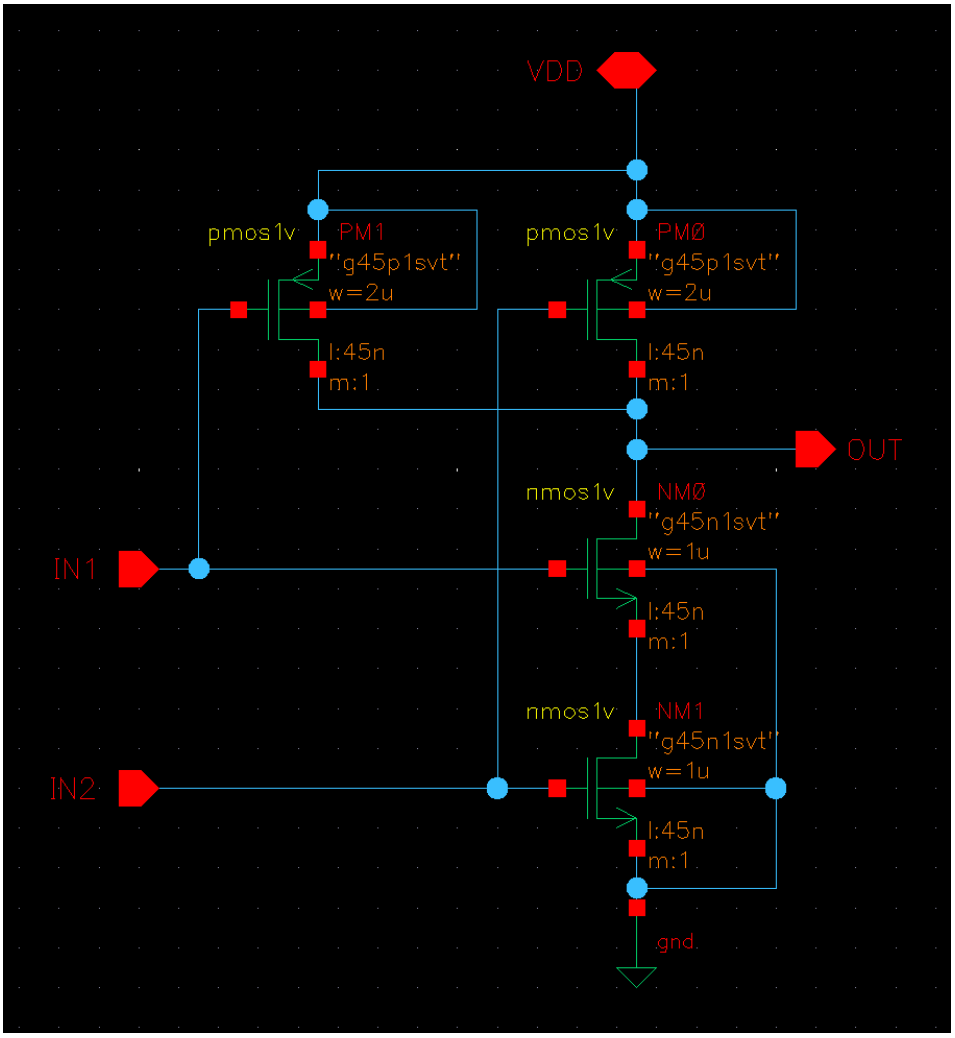
2. A 2-input NAND gate

Design Purpose:

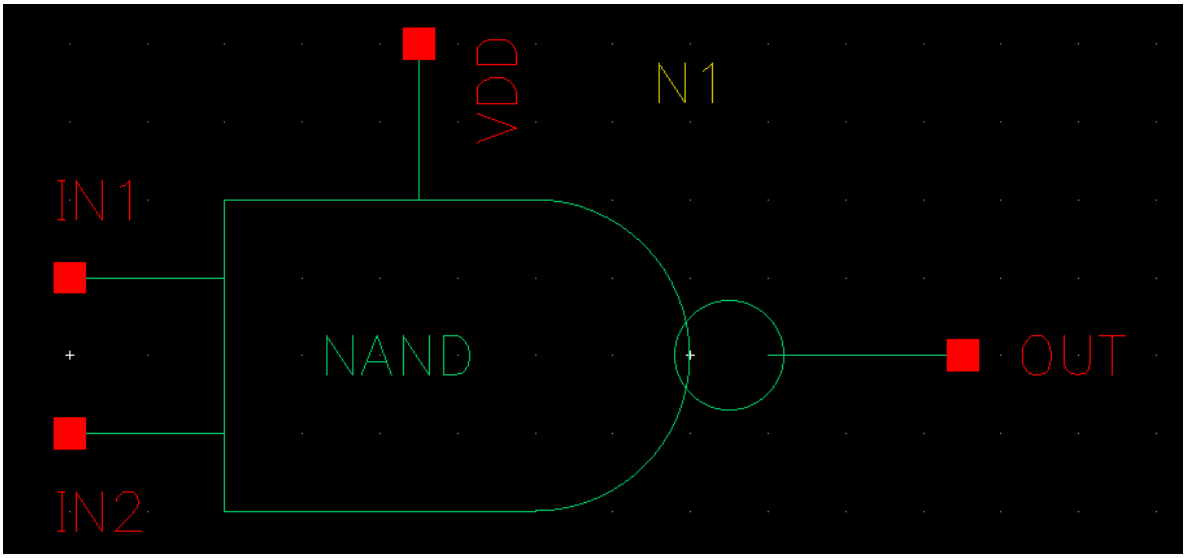
The purpose for this is to understand the NAND gate and the use of 2 PMOS in parallel connected to VDD and 2 NMOS that are series to the ground.

Engineering Data:

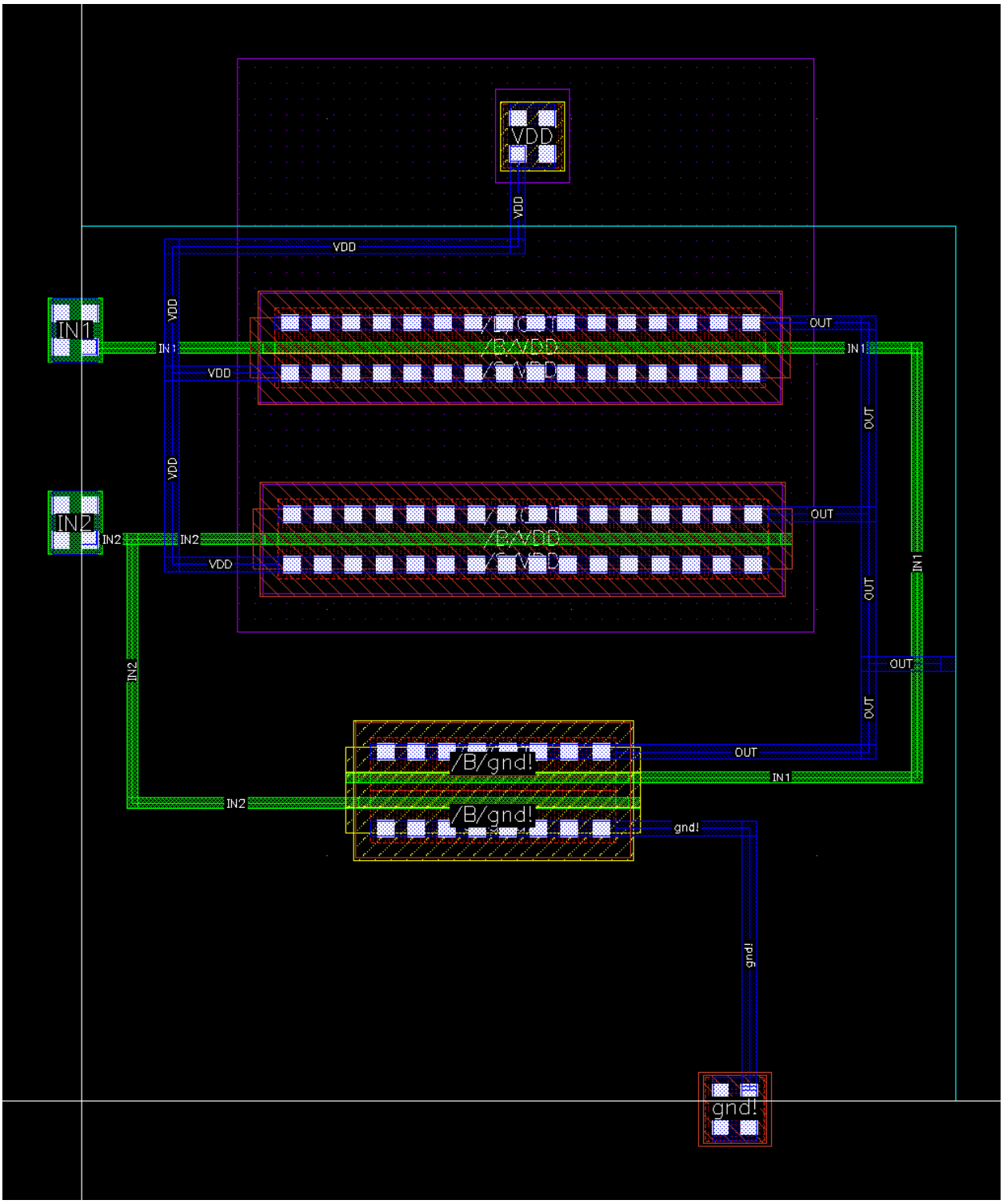
Similar to the inverter, I needed to connect the PMOS to the VDD and NMOS to the ground. However, the design for the NAND requires 2 PMOS that are in parallel and 2 NMOS in series. Below is the full schematic diagram for NAND gate.



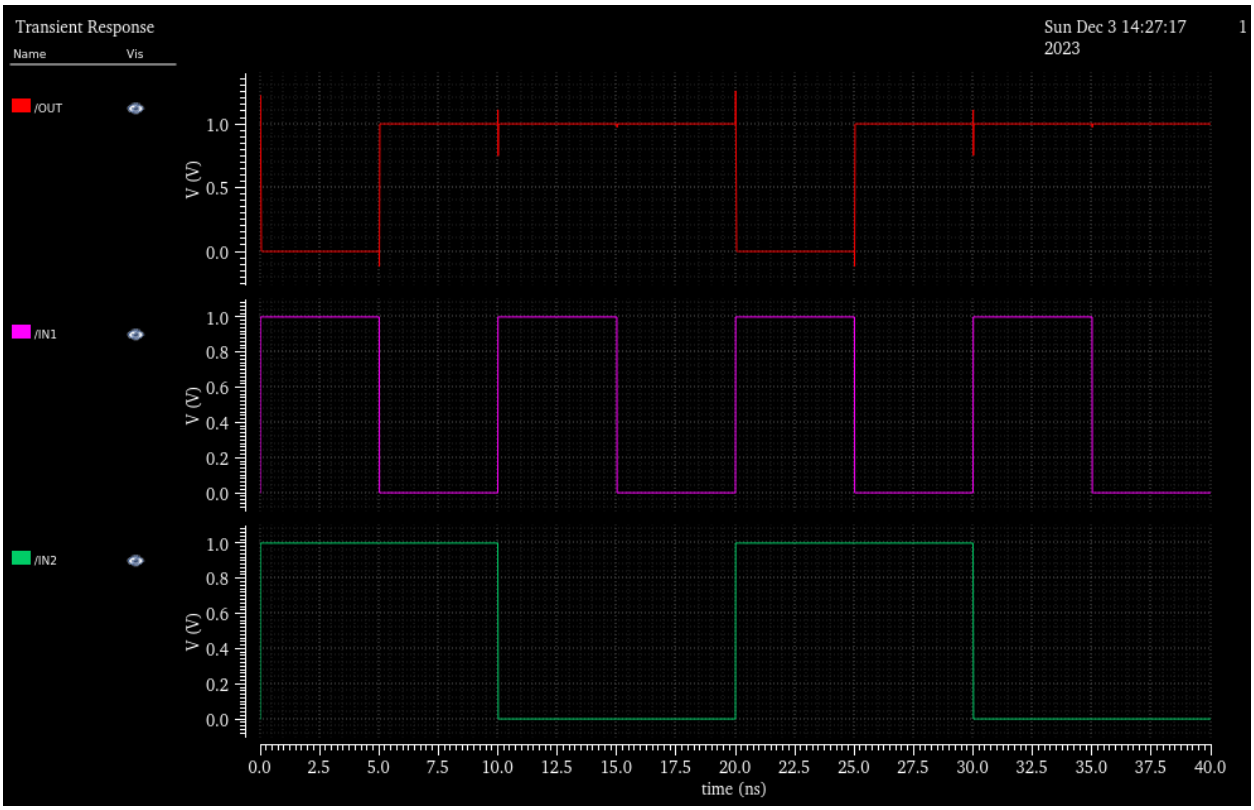
After that, I created the symbol for the NAND gate shown below.



On the other hand, I created the layout for the NAND gate which is shown below. Upon designing the layout, I was able to combine the two NMOS overlapping the side indicating that they are connected.


VDD
VDD
VDD
IN1
IN1
VDD
/B/VDD
OUT
OUT
IN1
VDD
IN2
IN2
IN2
VDD
/B/VDD
OUT
OUT
IN1
OUT
OUT
IN2
/B/gnd!
OUT
IN1
/B/gnd!
IN2
gnd!
gnd!
gnd!

Simulation:



Result Discussion

After designing the inverter, the NAND gate is a little bit difficult and confusing in terms of the layout and simulation. From the simulation, we can observe that when the inputs 1 and 2 are both high, the output is low, while the rest for the output will be high. On the other hand, the design for the NAND is straightforward on having a two PMOS in parallel and two NMOS in series.

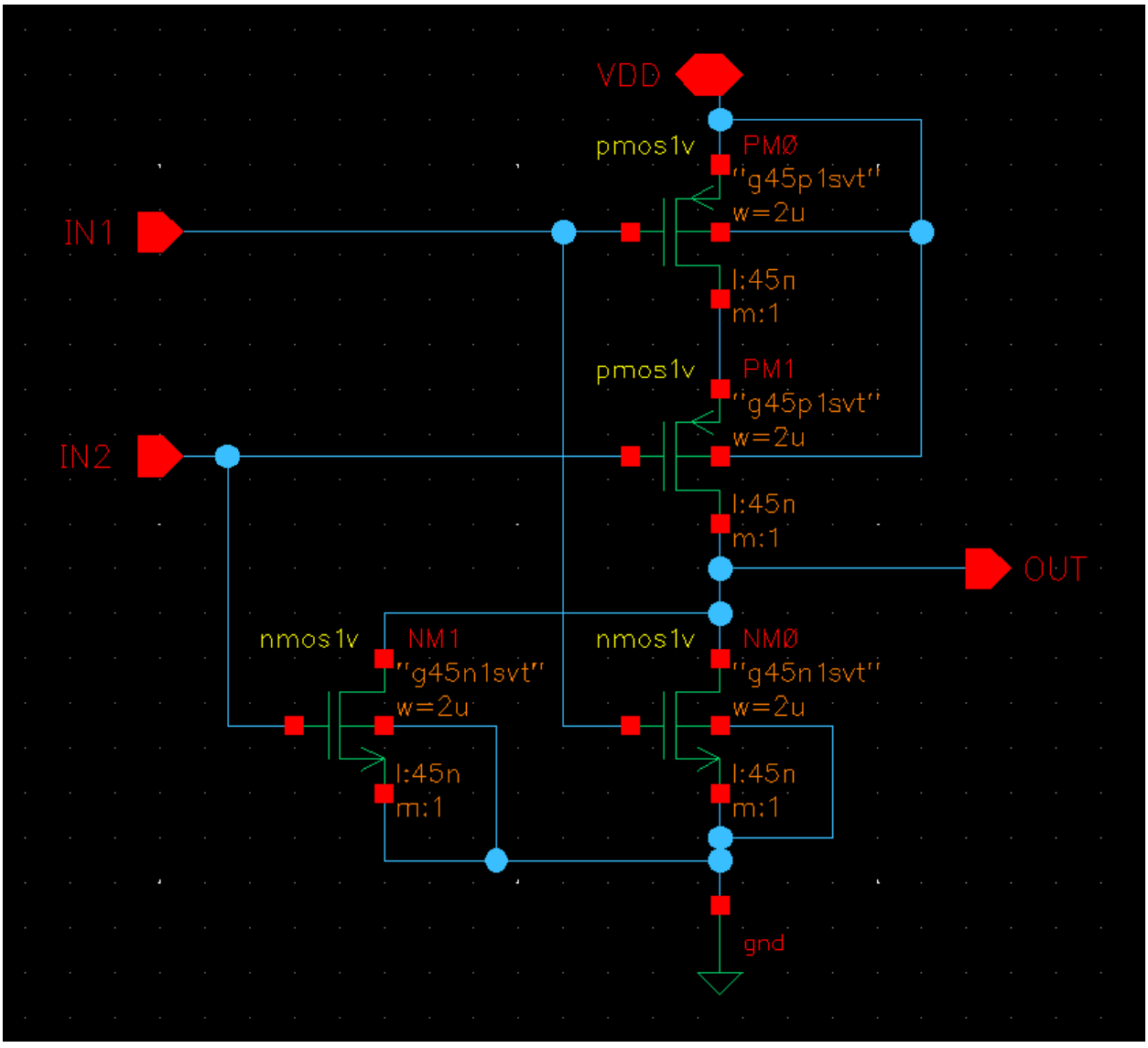
3. A 2-input NOR gate

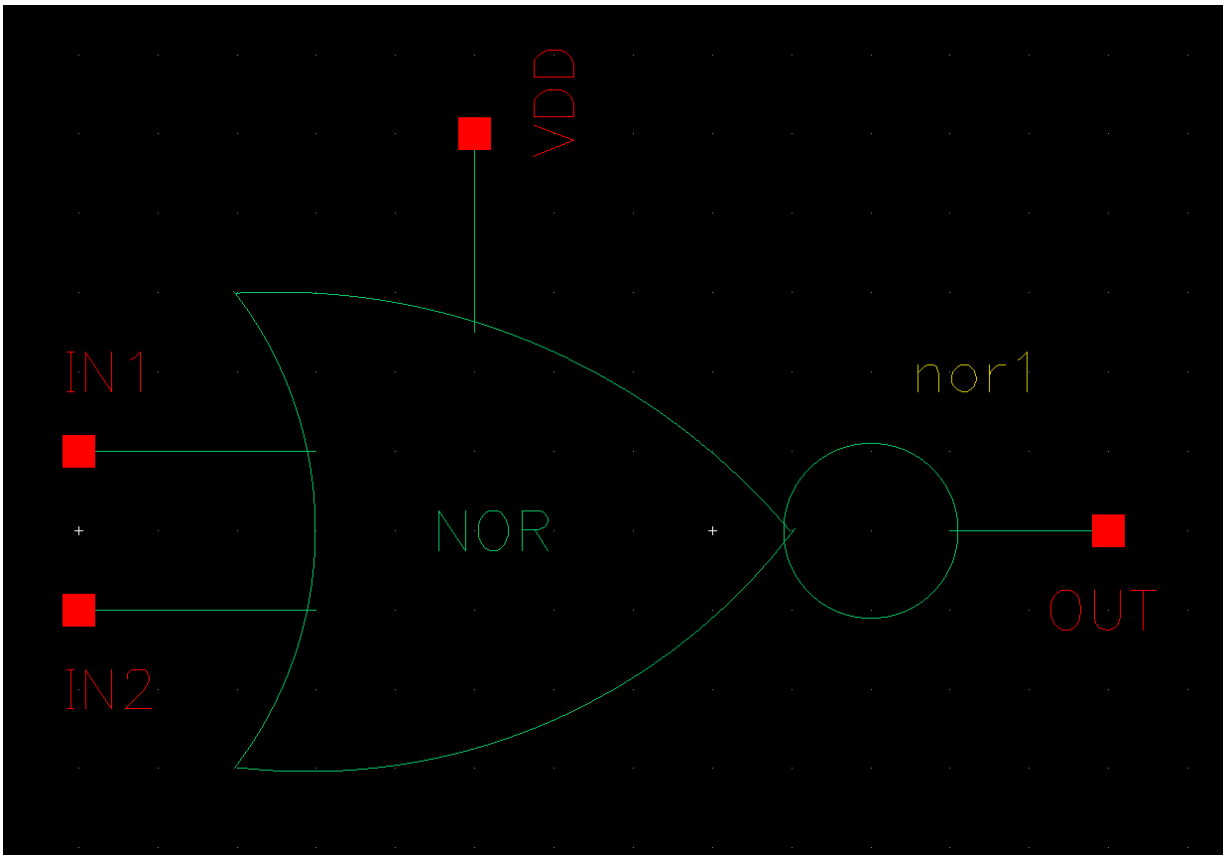
Design Purpose:

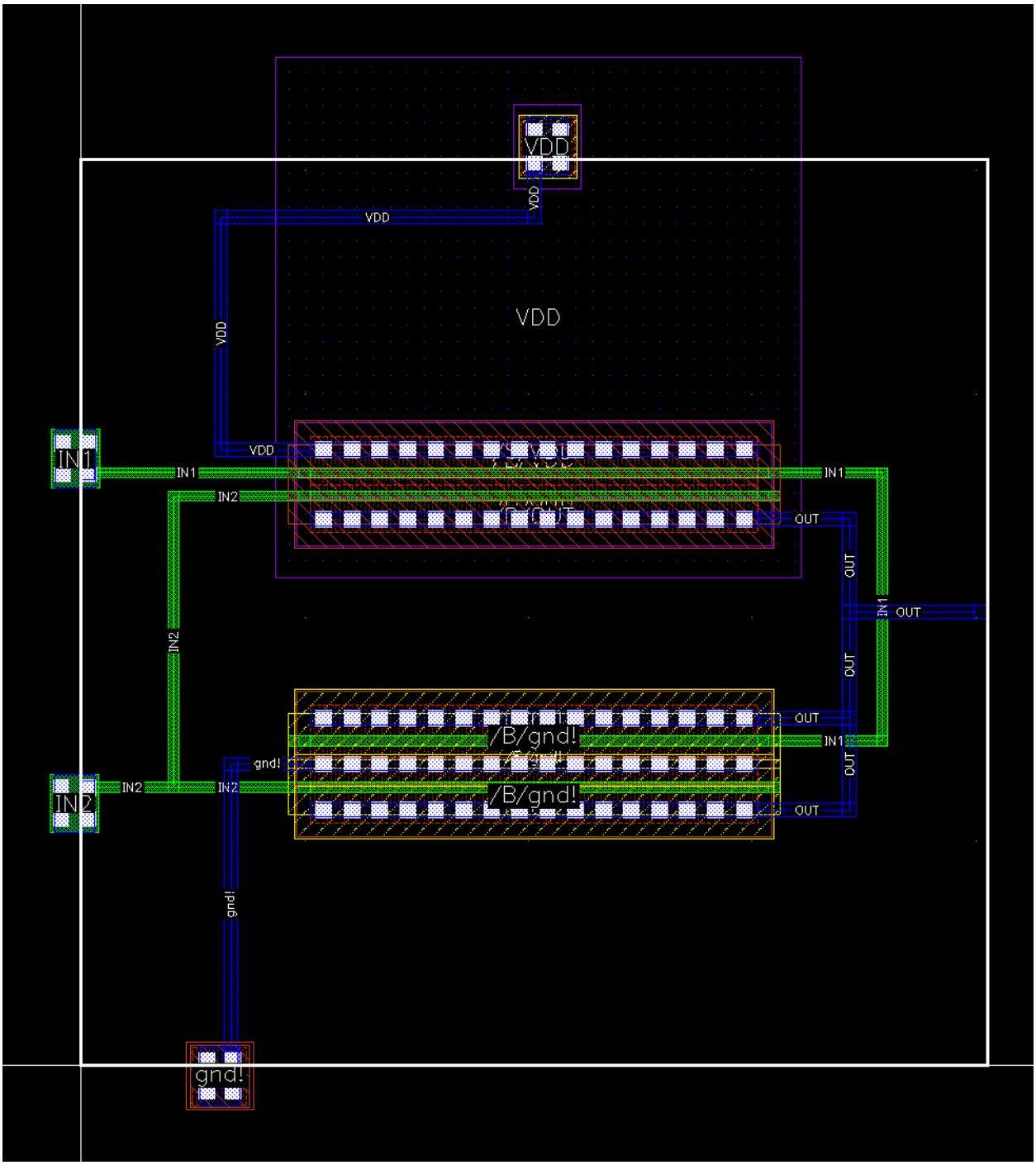
The purpose for this is to understand the NOR gate and the use of 2 PMOS in series and 2 NMOS in parallel.

Engineering Data:

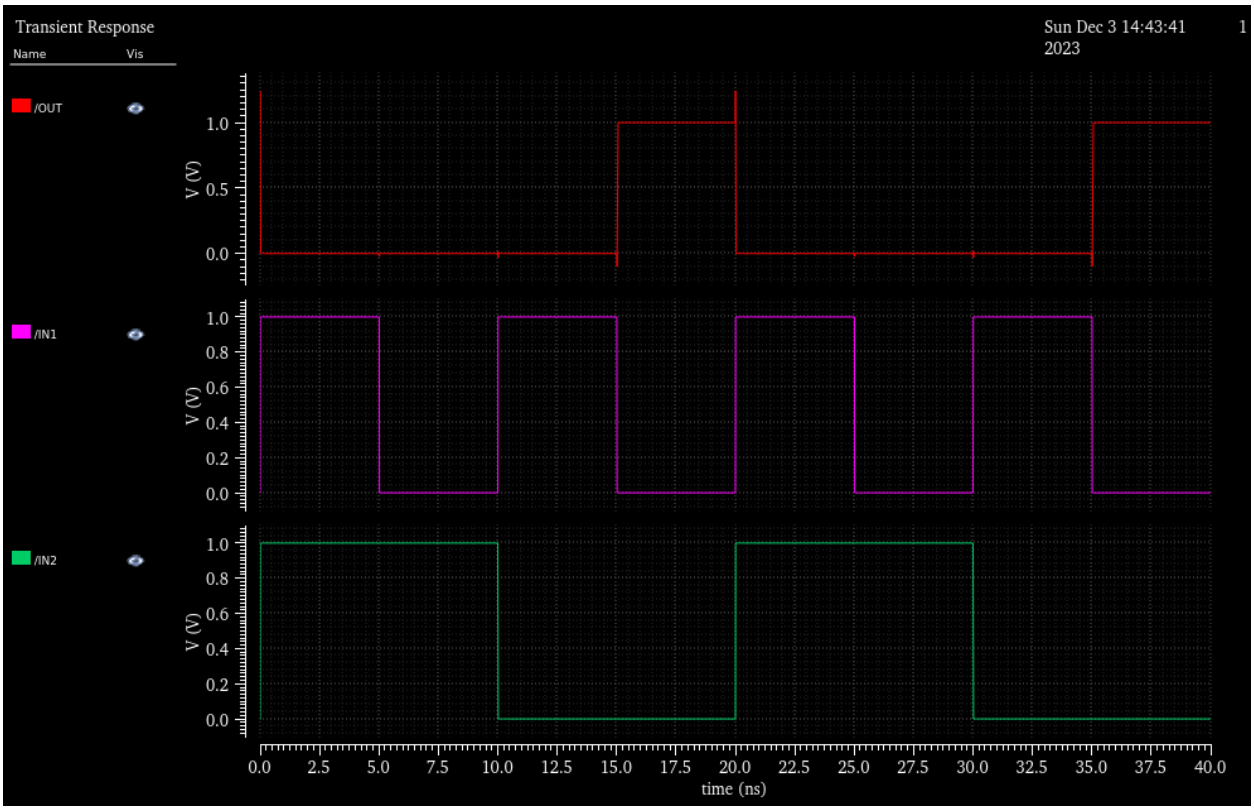
Similar to the NAND gate, the schematic design for NOR gate has two PMOS and two NMOS. However, the design for this gate switched as the PMOS in series and NMOS in parallel.




VDD
IN1
nor1
NOR
OUT
IN2


VDD
VDD
VDD
VDD
VDD
IN1
IN1
IN1
IN2
IN2
OUT
OUT
OUT
OUT
OUT
OUT
IN1
IN2
IN2
gnd!
/B/gnd!
/B/gnd!
gnd!
gnd!

Simulation:



Result Discussion

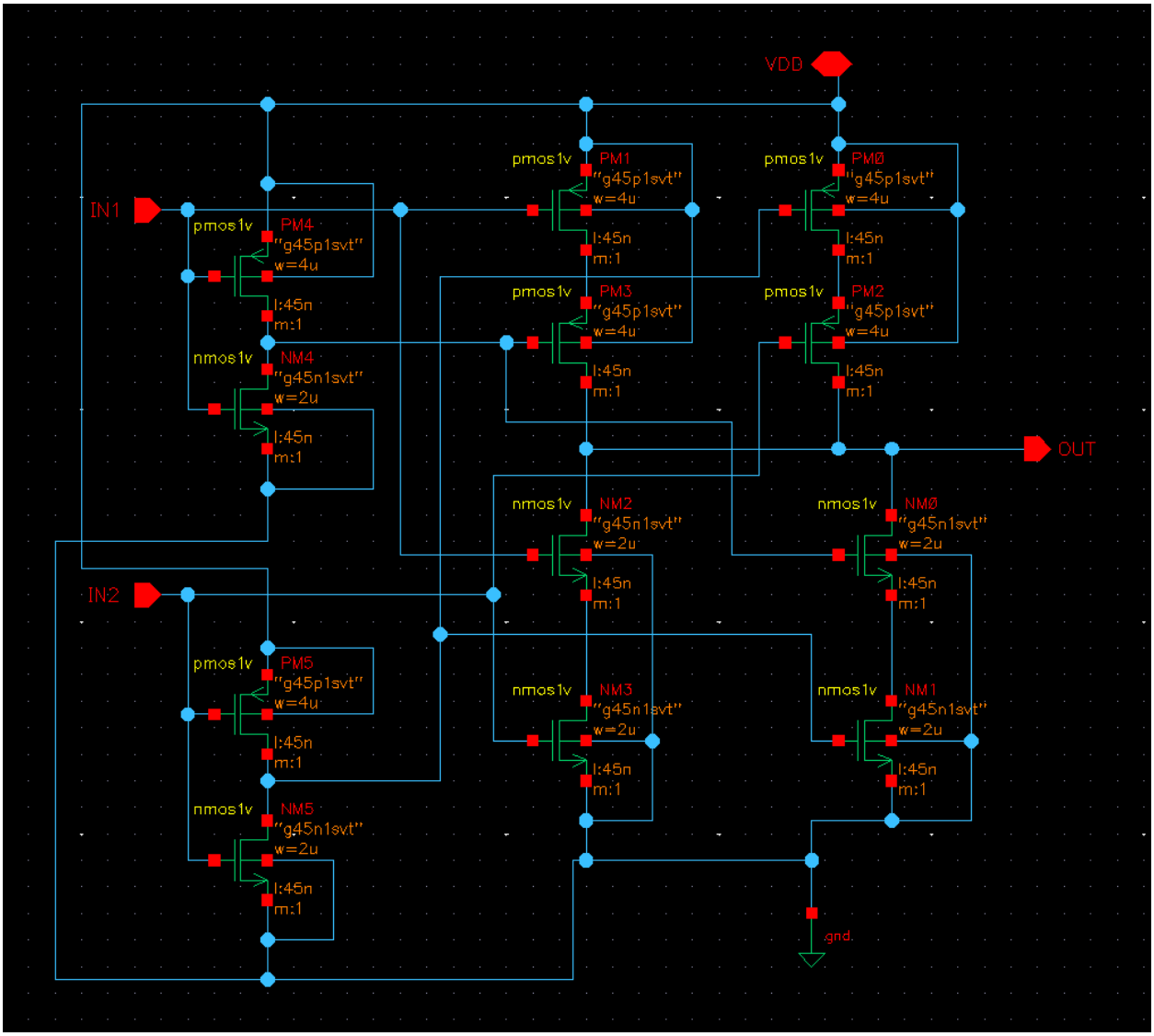
Similar to the previous gates, I was able to run the RDC and LVS with no errors. From the simulation, we can verify that when the inputs 1 and 2 are low, the output is high while the rest will be low regardless of the inputs. This just shows the opposite output for the NAND gate.

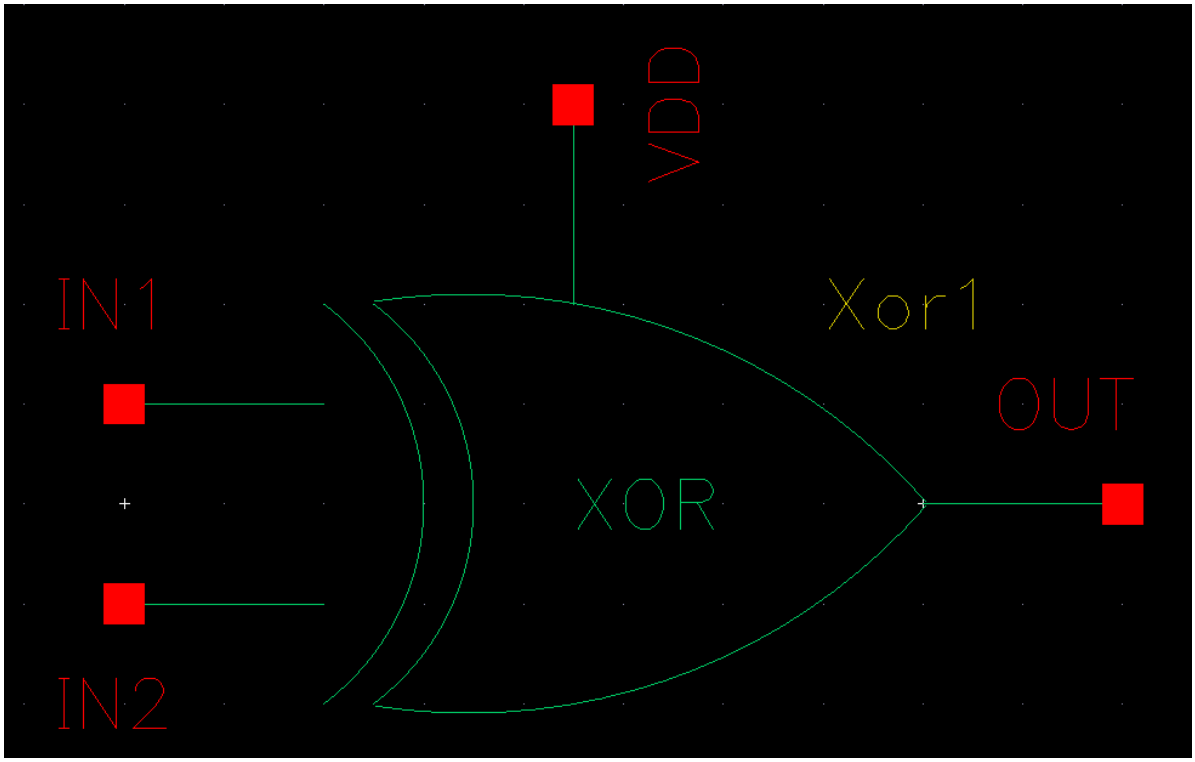
4. A 2-input XOR gate

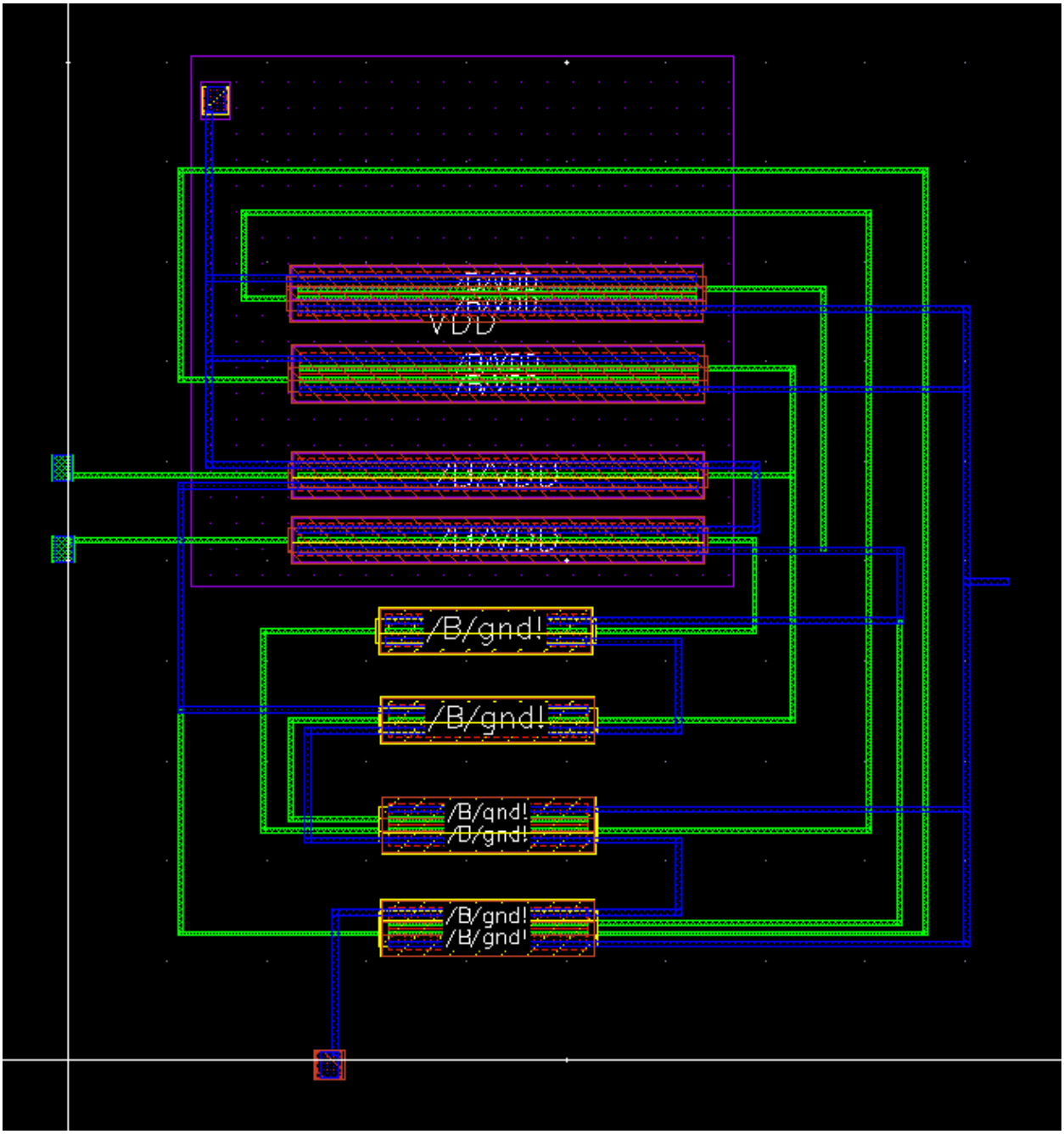
Design Purpose:

The purpose for this is to understand the XOR gate and the use of 6 PMOS and 6 NMOS. In this gate, we need to use the overall concept from the previous design with the inverter and using PMOS and NMOS with both series and parallel.

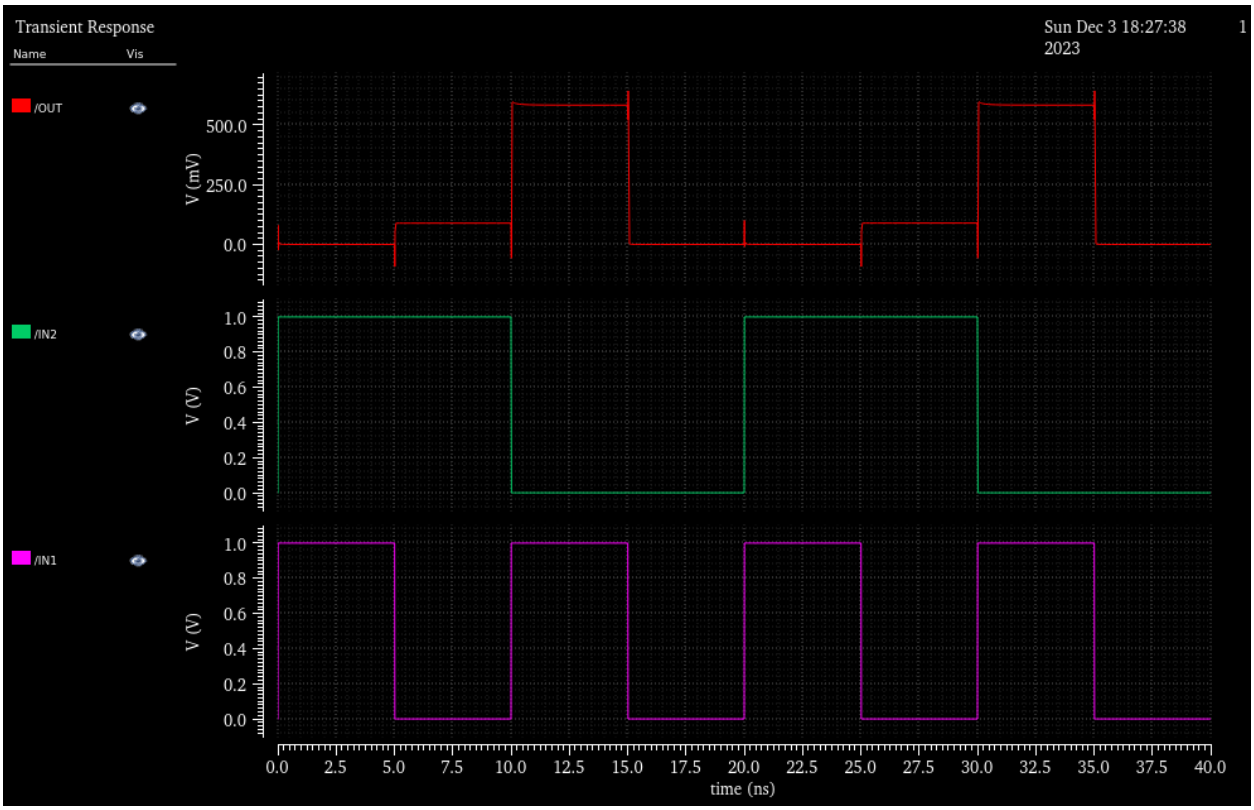
Engineering Data:




VDD
IN1
Xor1
OUT
XOR
IN2


VDD
/B/gnd!
/B/gnd!
/B/gnd!
/B/gnd!
/B/gnd!
/B/gnd!

Simulation:



Result Discussion

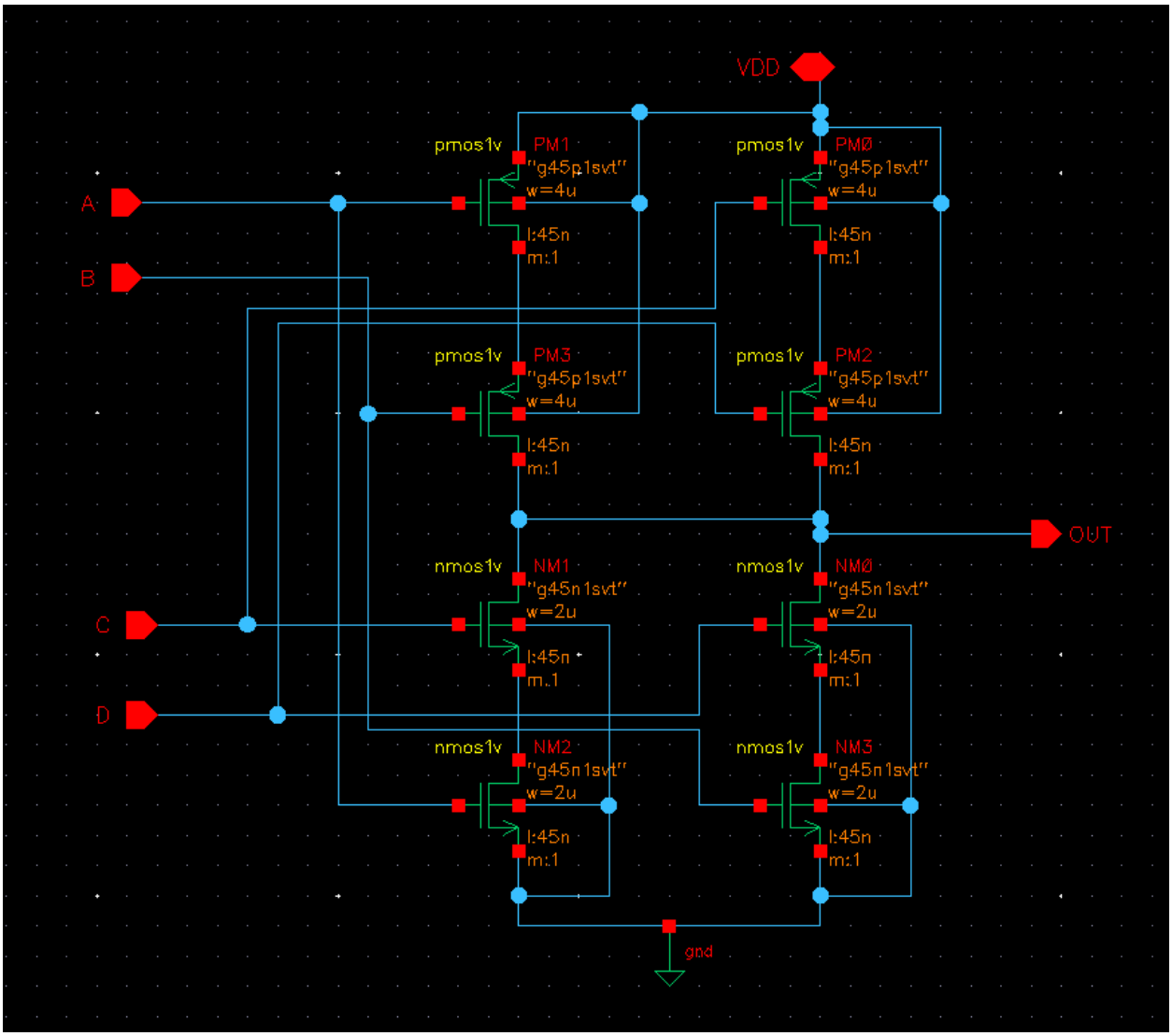
As I progressed on the gates, it became very complex with designing both schematic and layout. The XOR design requires four PMOS and NMOS, however, I needed to use the concept of the inverter for the inputs for the actual XOR design. From the simulation, I was able to generate the output, however, there is a low voltage generated when the input 1 is low and input 2 is high.

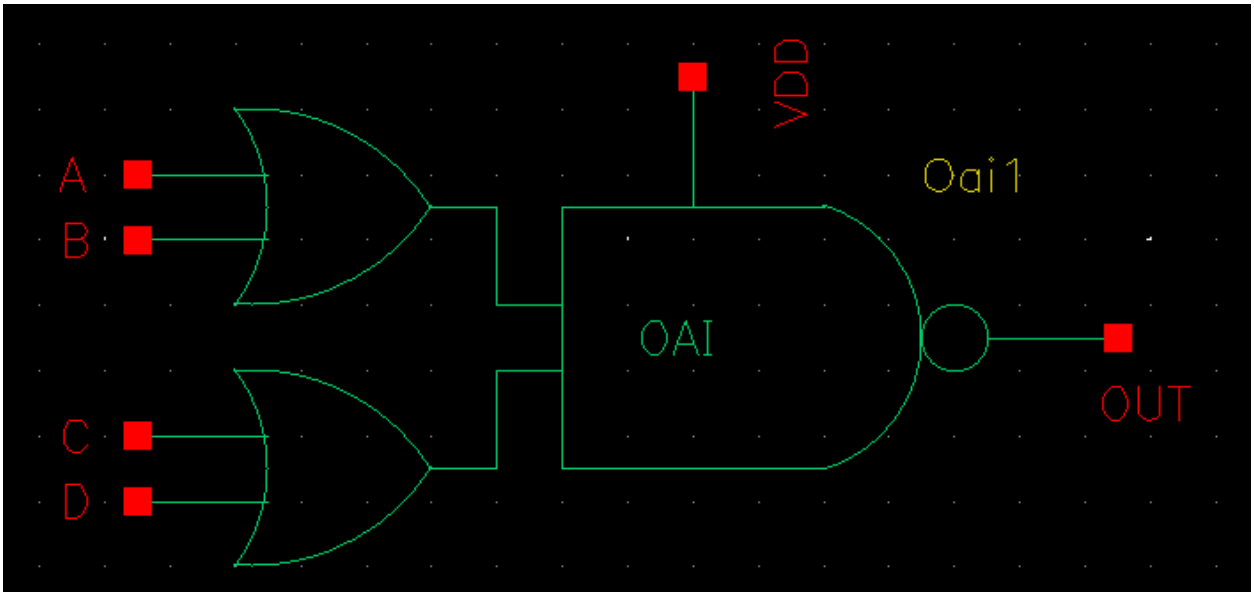
5. A complex gate F = $\overline{(A + B) \bullet (C + D)}$

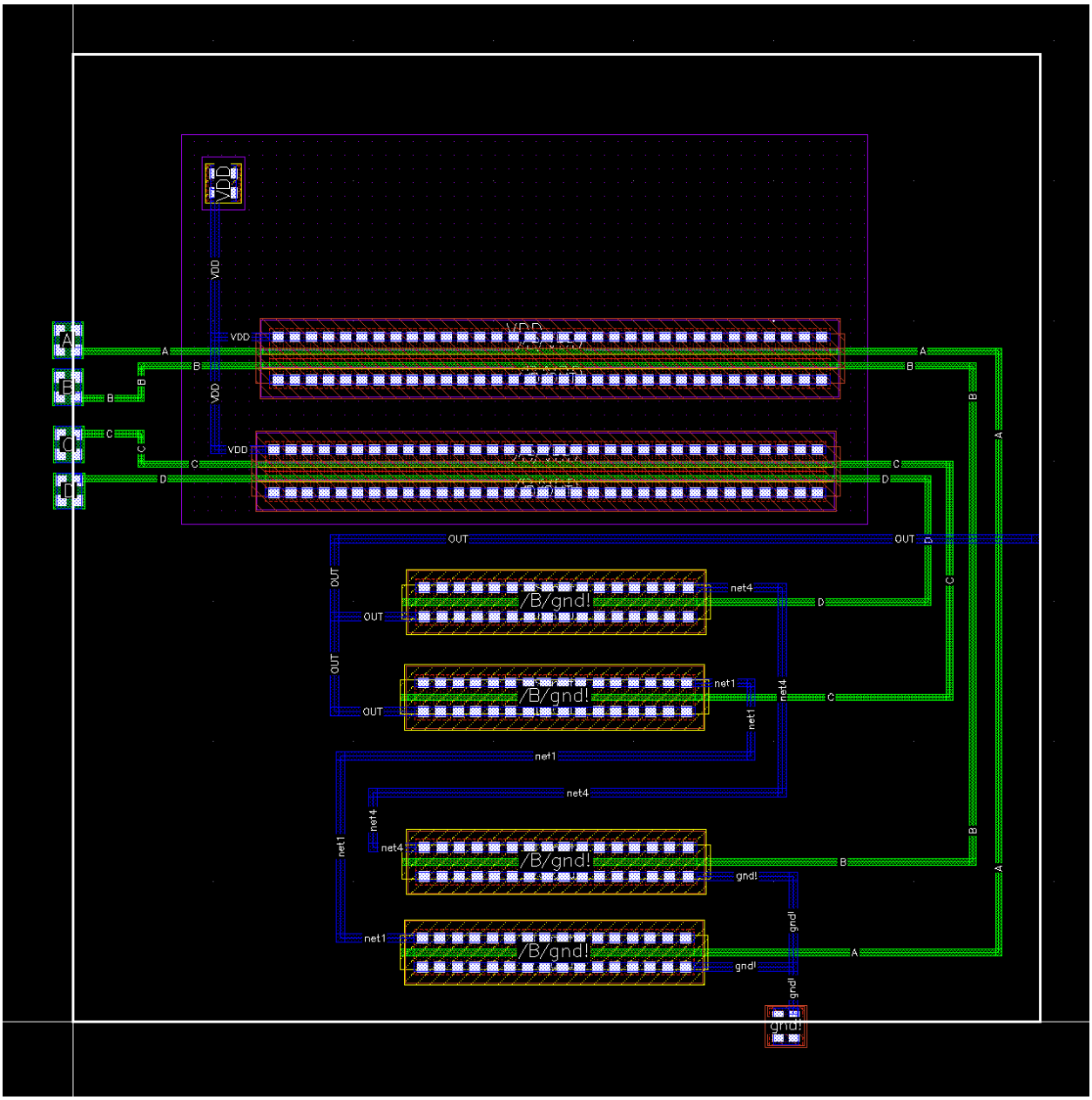
Design Purpose:

The purpose of this design is to apply all the concepts learned from the previous gate designs with PMOS and NMOS and the use of series and parallel.

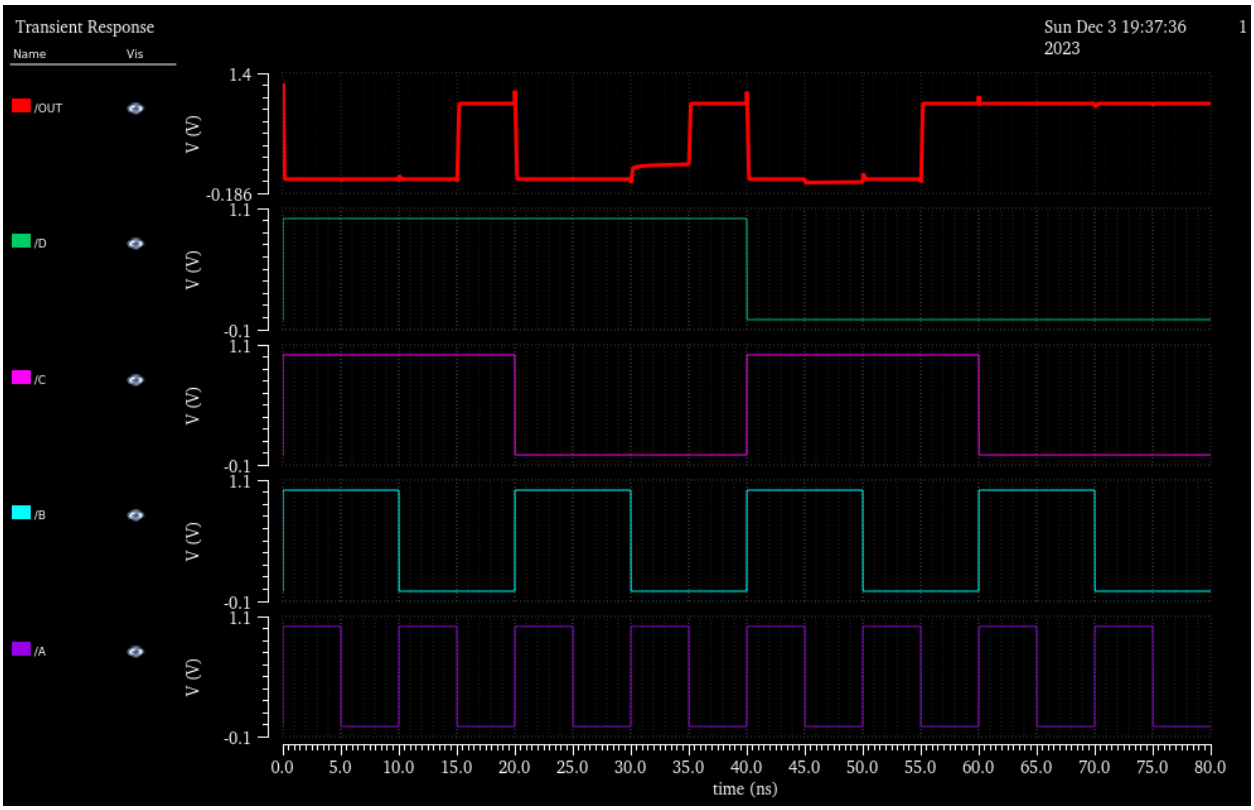
Engineering Data:




VDD
Oai1
A
B
OAI
C
D
OUT


VDD
A
B
C
D
OUT
net4
net1
gnd!
/B/gnd!

Simulation:



Result Discussion

For this complex gate, I was able to apply the concepts that I learned from the previous gates including the use of series and parallel for both PMOS and NMOS. The schematic and layout are much simpler than the XOR since it doesn't need inverters but replaced by another input labels. On the other hand, I was able to run DRC but encountered problem with LVS which the warning says, "unable to find cell g45inds."

CONCLUSION

Within this project, I was introduced to use the Cadence Virtuoso tool to design the basic CMOS logic gates. I was able to design the schematic and layout for each gate, however, layout is a little bit different in position compared to schematic. On the other hand, I was able to simulate all the gates, however, got a different result for the XOR and the complex gate. Furthermore, I was able to run DRC and LVS through all the gates. For the extraction, I was able to do the first three gates and didn't see any changes within the layout for parasitic views.