California State University, Sacramento
The College of Engineering and Computer Science

CPE 166 Advanced Logic Design

Midterm 1 – Part 2

Fall 2022

Student Name: _____

You need to write Verilog design for the following two questions. Testbench is not required for each question.

Part2.1 [10 points]. Implement the clock division hardware design in Verilog.
The input clock is clk and the output clock is clk2. The frequency of clk2 is equal to the frequency of clk divided by 50.

```
module   clkdiv50 ( clk,  clk2);
```

Part2.2 [26 points] Design a single Mealy finite state machine to recognize sequence 100 or sequence 1000.

```
module fsm ( reset, clk,  a,  y);
input   reset, clk;
input    a;              // “a” represents the incoming data
output  y;               //  “y” is a mealy output for detecting the correct sequence.
```