# CALIFORNIA STATE UNIVERSITY SACRAMENTO


## DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

**EEE 108L**
***Electronics I_ Laboratory, 1 unit***

**Summer_ 2022**

***Lab - 05 Report***

*Submitted to*

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*By*

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## ***INTRODUCTION:***

In this laboratory, the student needs to explore the DC characteristics of a MOS transistor. The student must use the model of an n-channel transistor in the CD4007 MOS transistor for both SPICE simulations and the actual laboratory measurements. To have a better understanding, this laboratory divided into three parts. For the first part, the student must the equations given to calculate for the initial questions that will be use to the later part of this laboratory. This also introduced the 3 different state: cutoff, saturation (forward active), and linear (triode) region. For the next part of the laboratory, the student must simulate the given circuit shown in figure 1. The circuit needs to be run with different simulation generating graphs requiring to analyze and gather data. For the last part of this laboratory, the student must build the actual circuit using the model that has separate source and bulk connections. Using the AD2, the student must utilize the settings for the graphs to generate and record the data that were asking.

## ***Part1 – Preliminary Calculations***

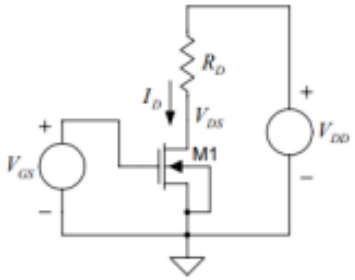



**Figure 1**

1. The condition for forward active (saturation) region $\boldsymbol{V_{DS} > (V_{GS} - V_{th})}$ is equivalent to $\boldsymbol{V_{GD} < V_{th}}$. (Refer to appendix for full proving)

2. From figure 1, if $\boldsymbol{R_D = 4.7k\Omega}$, $\boldsymbol{V_{DD} = 5V}$, $\boldsymbol{\lambda = 0}$,
   - When $\boldsymbol{V_{GS} = 1V}$: $\boldsymbol{I_D = 0}$ and the device is the cutoff region.
   - When $\boldsymbol{V_{GS} = 2V}$: $\boldsymbol{I_D = 196.8\,\mu A}$ and the device is the saturation region.
   - When $\boldsymbol{V_{GS} = 4\,V}$: $\boldsymbol{I_D = 1.025\,mA}$ and the device is the linear (triode) region.

3. $\boldsymbol{I_D = 35\,\mu}$ when $\boldsymbol{V_{GS} = 1.46V}$ and $\boldsymbol{I_D = 430\,\mu}$ when $\boldsymbol{V_{GS} = 2.18V}$:

   $\boldsymbol{V_{th} = 1.172\,V}$

## ***Part2 - Simulations Results***

For this part of the laboratory, the student simulated the circuit from the figure 1 into the SPICE and set the $V_{DD}$ = 5V and other specific values from preliminary calculations. The circuit in SPICE simulation is shown below.

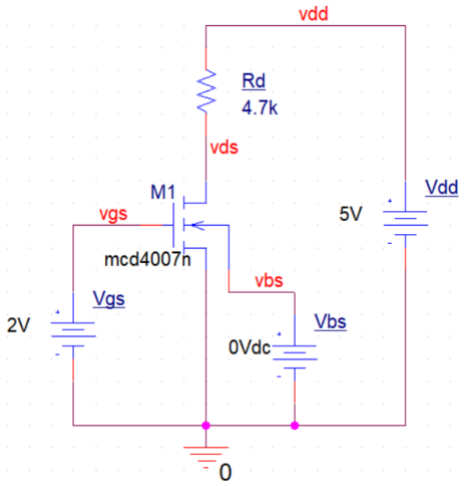



Figure 2. Circuit in SPICE simulation

After entering the circuit in SPICE simulation, the student run DC Sweep for $V_{GS}$ from 0 to 5V. With this, the student was able to generate a plot of $I_D$ as a function of $V_{GS}$ shown in figure 3. Additional, the student was able to gather the information for the model of the CD4007 n-channel transistor.

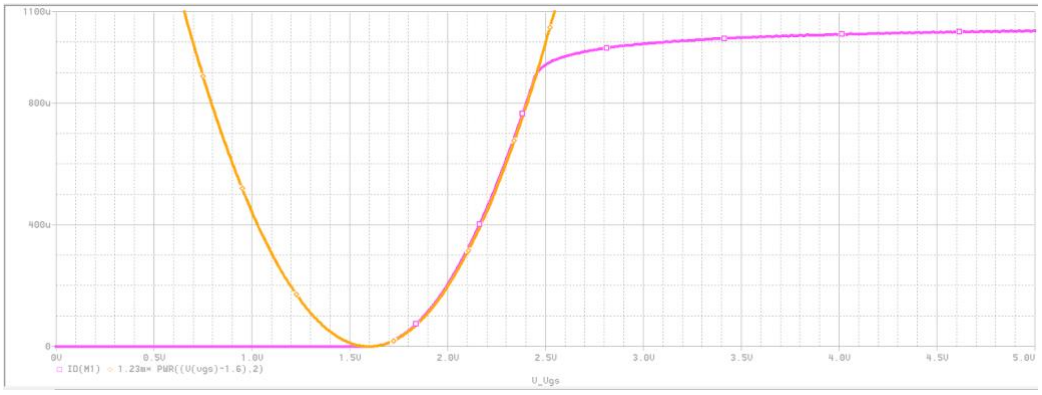



Figure 3. DC Sweep for $I_D$ as a function of $V_{GS}$

On the other hand, the student add a plot showing $V_{GS}$, $V_{GD}$, and $V_{th}$ shown in figure 4 below which uses a math function of two circuit voltages to plot $V_{GD}$ and enter "1.6" as the trace expression for $V_{th}$. In the graph below, we can see that the blue trace is $V_{GS}$, the orange trace is $V_{GD}$, and the purple trace is $V_{th}$.

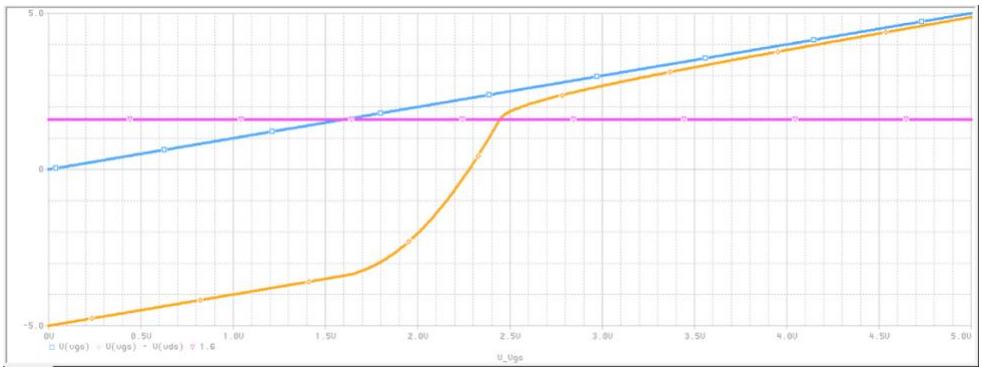


Figure 3. DC Sweep for $V_{GS}$, $V_{GD}$, and $V_{th}$

Using vertical lines from the previous graph, the student labeled the three regions of operation: cutoff, forward active, and linear (triode) which shown in figure below.

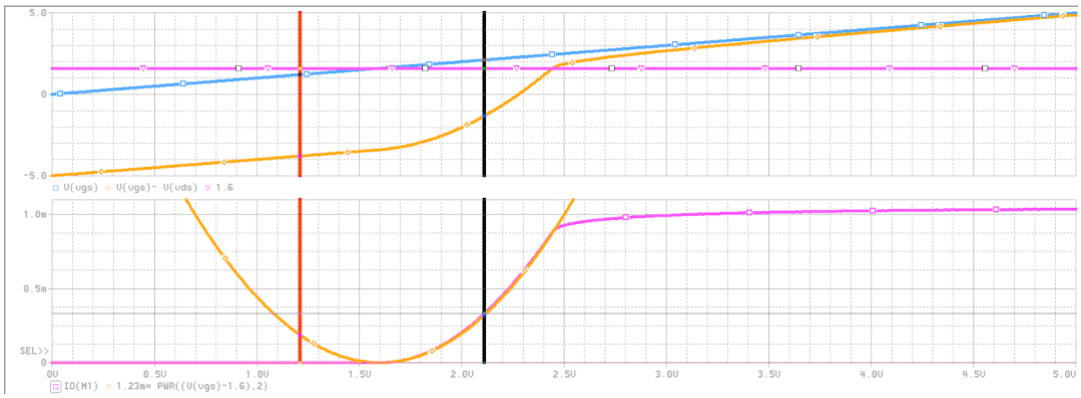


Figure 4. DC Sweep for $V_{GS}$, $V_{GD}$, and $V_{th}$ showing the cutoff region and forward active region

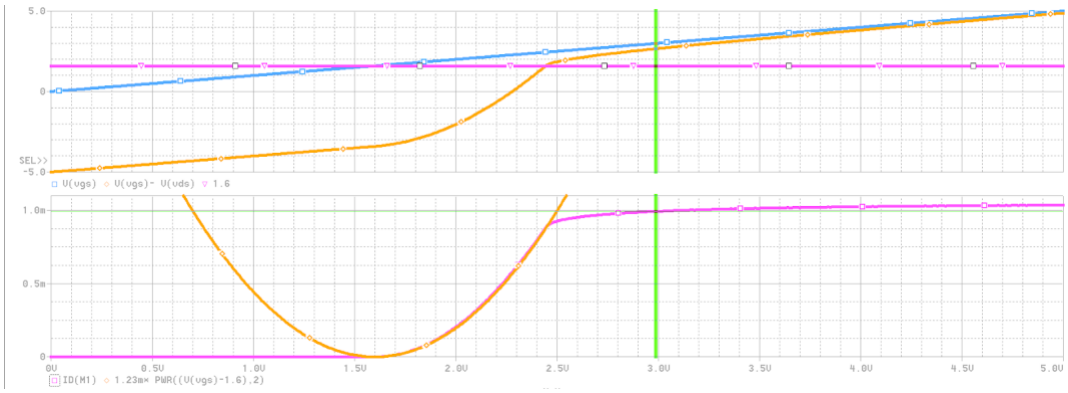


Figure 5. DC Sweep for $V_{GS}$, $V_{GD}$, and $V_{th}$ showing the linear (triode) region

Analyzing from the graphs figure 4, we can see that the red vertical line showing its in the cutoff region in which the cutoff region is below 1.5V while the black vertical line shows in the forward active region in which this region is between 1.5V to 2.5V. On the other hand, we can see in figure 5 that the green vertical line is in the linear region in which this region is anything above 2.5V.

After that, the student change the circuit by removing $R_D$ and replacing it with a wire which makes $V_{DS} = V_{DD}$. Assigning a DC value of 2V to $V_{GS}$ and sweep $V_{DD}$ from 0 to 5V, the student was able to obtain a plot of $I_D$ shown below.

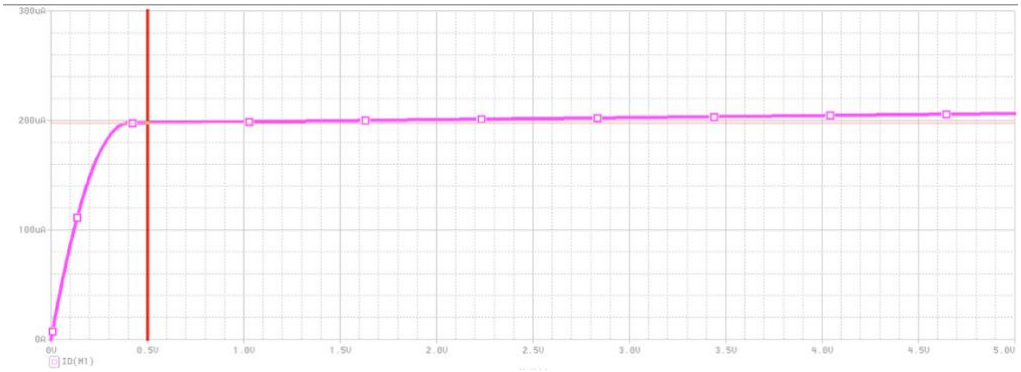



Figure 6. DC Sweep as $V_{DD}$ set as the voltage for $I_D$

Analyzing the graph above, we can see the red vertical line representing the transistor transitions into saturation which the value is at 0.5V.

On the other hand, the student find an approximate value for $\Delta V_{DS}/\Delta I_D$ in each region. The region that the student did are the linear region and the saturation region which shown in figure 7.

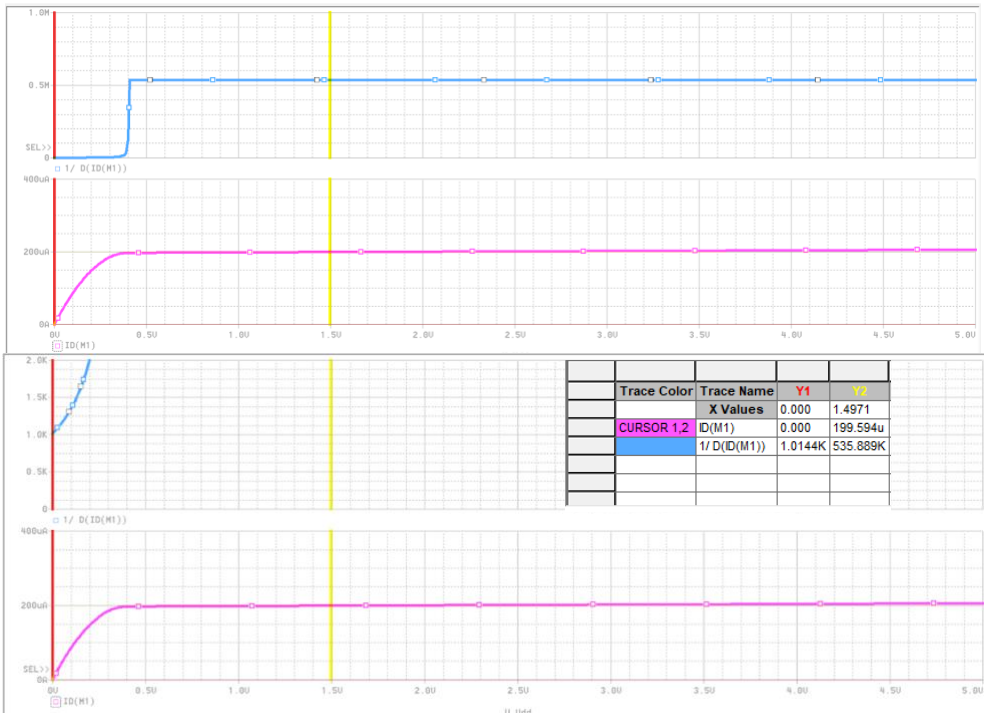



Figure 7. plot for $\Delta V_{DS}$ and $\Delta I_D$

From the figure 7, we can see that the blue trace in the second graph is zoomed in which we can clearly see the values more clearly to identify the values for each regions. Looking at the graph, the red vertical line show as the linear region which is at 1.0144 kΩ while the yellow line shown as the saturation region which is 535.889 kΩ.

After, the student put back the $R_D$ in the circuit and simulated with the bulk of the transistor connected to -1V instead of ground shown in figure 8.

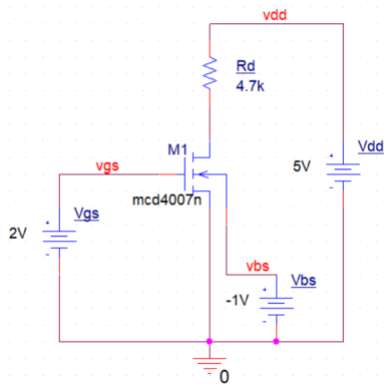



Figure 8. Circuit in PSPICE $V_{bs}$ is set to -1V

After setting up the new circuit, the student run the bias point and found the value of $V_{th}$ which is 2.58 V shown in the figure below.

## ***Part3 – Laboratory Measurements***

In this part of the laboratory, the student constructed the circuit from figure 1 into the breadboard using the laboratory kit given shown in figure 9.

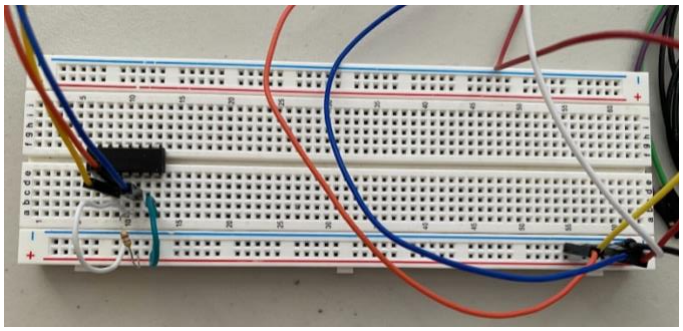
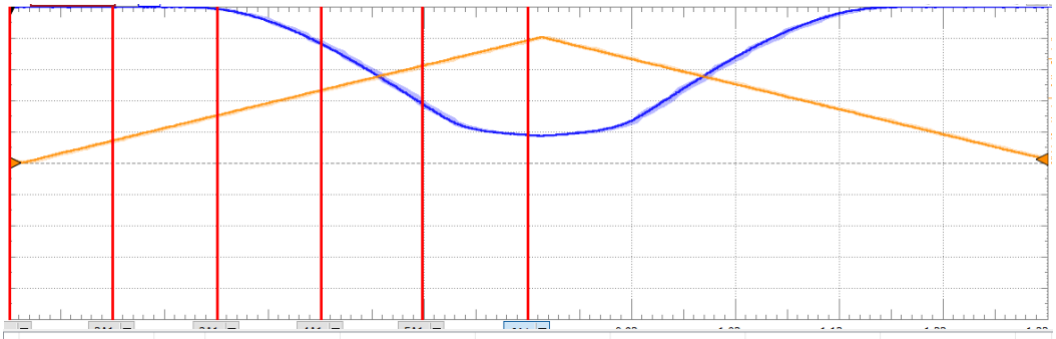


Figure 9. Actual circuit in breadboard

After setting it up, the student set $V_{DD}$ to 5V and sweep $V_{GS}$ from 0 to 5V shown in figure below.



| | Position | Ref | Δ X | 1/ΔX | C1 | C1 ΔY | C2 | C2 ΔY |
|---|---|---|---|---|---|---|---|---|
| 1 | 312.25 us | none | | | 0.150895 V | | 4.97658 V | |
| 2 | 419.05 us | 1 | 106.8 us | 9.3629 kHz | 0.690137 V | 539.2 mV | 4.9729 V | -3.6832 mV |
| 3 | 520.69 us | 1 | 208.44 us | 4.7975 kHz | 1.50668 V | 1.356 V | 4.91028 V | -66.2969 mV |
| 4 | 619.74 us | 1 | 307.49 us | 3.2521 kHz | 2.30816 V | 2.157 V | 3.82106 V | -1.1555 V |
| 5 | 717.93 us | 1 | 405.68 us | 2.465 kHz | 3.09209 V | 2.941 V | 1.8916 V | -3.085 V |
| 6 | 818.71 us | 1 | 506.46 us | 1.9745 kHz | 3.89979 V | 3.749 V | 0.880527 V | -4.0961 V |

Figure 10. Simulated sweep $V_{GS}$ from 0 to 5V

After the simulation, the student was able to record $V_{GS}$ and $V_{DS}$ as well as calculated $I_D$ shown in table 1.

Table 1. Recorded $V_{GS}$, $V_{DS}$ and calculated $I_D$

| $V_{GS}$ | $V_{DS}$ | $I_D$ |
|---|---|---|
| 0.150895 V | 4.97658 V | 1.03172 |
| 0.690137 V | 4.9729 V | 0.91699 |
| 1.50668 V | 4.91028 V | 0.74325 |
| 2.30816 V | 3.82106 V | 0.57273 |
| 3.09209 V | 1.8916 V | 0.40593 |
| 3.89979 V | 0.880527 V | 0.23408 |

Other than that the student obtain data points for the forward active region shown in figure 11 and data points for the linear region shown in figure 12.

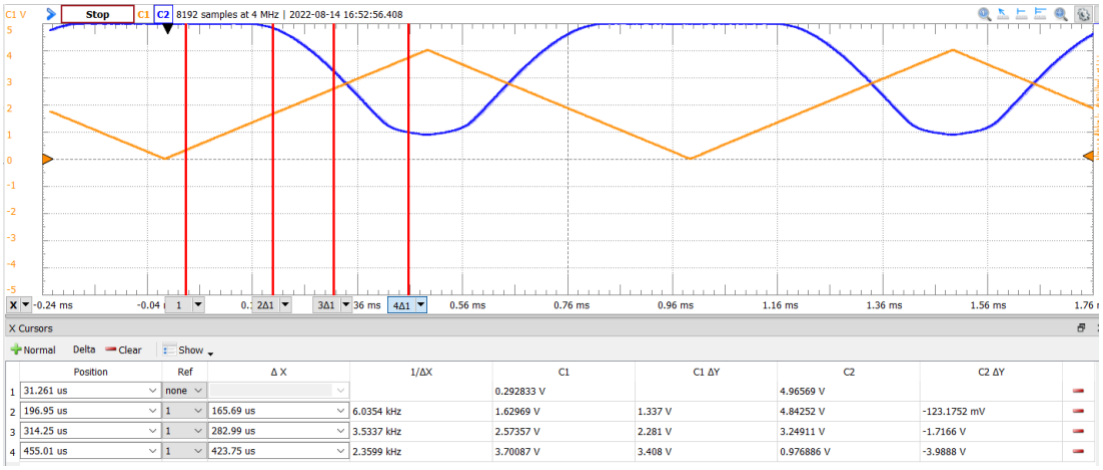



Figure 11. Graph and data points for the forward active region

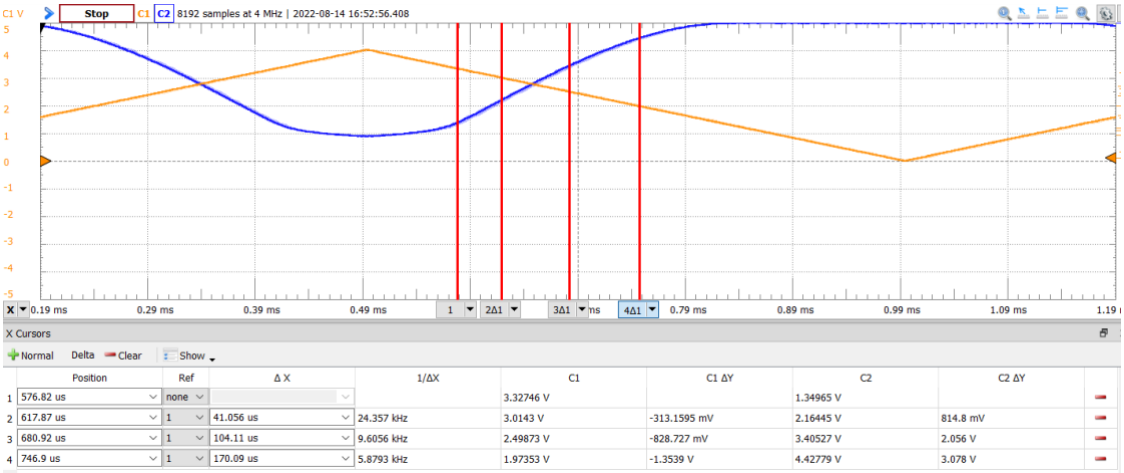



Figure 12. Graph and data points for the linear region

Analyzing figures 11 and 12, we can both see the red lines which indicates each data points used consisting of 4 data points recorded below the graph. With this, the student was able to determine the value for $V_{th}$ which is equal to 1.6 V.

On the other hand, the student adjusted the $V_{GS}$ so that the $V_{DS}$ = 2V from the figure 1. With this adjustment, the student was able to record the values of $V_{GS}$ shown below.


Figure 13. The values for $V_{GS}$ and $V_{DS}$

For that, the student vary $V_{DD}$ from zero to about 7 volts and recorded $V_{DS}$ and $I_D$ with 4 data points in linear region and saturation region shown in table below.

Table 2. Recorded data $V_{DS}$ and $I_D$ for Linear and Saturation region

| Volts | $V_{DS}$ (Linear) | $V_{DS}$ (Saturation) | $I_D$ (Linear) | $I_D$ (Saturation) |
|---|---|---|---|---|
| 1 | 0.246095 V | 0.332117 V | 0.1604 | 0.1421 |
| 2 | 0.287919 V | 0.2931303 V | 0.3642 | 0.36316 |
| 3 | 2.97163 V | 2.87718 V | 0.00603 | 0.02613 |
| 4 | 3.72503 V | 3.98142 V | 0.0585 | 0.00395 |

After recording the values, the student then connect the bulk terminal of the transistor under test to a fixed voltage equal to -1V and found a new value of $V_{th}$ equal to 2.58V.

## ***CONCLUSION:***

In this laboratory, the student explored the DC characteristics of a MOS transistor. There are 3 parts of MOS which consists of gain, source, and drain. On the other hand, there are also region operation including the cutoff region, forward active (saturation) region, and the linear (triode) region. To further understand the goal of this laboratory, the student worked with three different parts. The first part of this laboratory uses the skills and things learned from the lecture and apply the equations and calculations to the questions. We found out the that one of the conditions for forward active region $\boldsymbol{V_{DS}}$ > ($\boldsymbol{V_{GS}}$ - $\boldsymbol{V_{th}}$) is equivalent to $\boldsymbol{V_{GD}}$ < $\boldsymbol{V_{th}}$. We also investigated the different region with the given $\boldsymbol{V_{GS}}$ and calculated for the $\boldsymbol{I_D}$. For the second part of the laboratory, the student used the SPICE simulation and also showed different regions. Step-by-step, the student showed each graph adding different voltages such as $\boldsymbol{V_{GS}}$, $\boldsymbol{V_{GD}}$, and $\boldsymbol{V_{th}}$ with different regions divided. On the last part of the laboratory, the student setup the actual circuit using the model CD4007 MOS transistor and used AD2 to simulate and measure. Same as the SPICE simulation and the hand calculation, the student obtain many data points for the regions.

Table 3. The comparison for three parts of the laboratory

| | Preliminary | Simulation | Experimentation |
|---|---|---|---|
| $V_{GS}$ | 1.46 | 1.46 | 1.09 |
| $V_{th}$ | 1.17 | 1.6 | 1.6 |
| $V_{th}$ with -1V | 2.3 | 2.58 | 2.58 |

# *APPENDIX*

## PRELIMINARY CALCULATIONS

1. $V_{DS} = V_D - V_S$ , $V_{GS} = V_G - V_S$

$V_{DS} > (V_{GS} - V_{th})$

$V_D - V_S > V_G - V_S - V_{th}$

$V_D - V_G > -V_{th}$

$V_G - V_D < V_{th}$

$V_{GD} < V_{th}$

2. • If $V_{GS} = 1V$

$V_{GS} < V_{th} \longrightarrow$ cutoff region

$I_D = 0$

FROM THE MODEL:

$$K = \frac{\mu C_{OX}}{2}\frac{W}{L} = \frac{K_p}{2}\cdot\frac{W}{L} = \frac{0.000820}{2}\cdot\frac{15}{5} = 1.23\times10^{-3}$$

$V_{th} = 1.6V$

• If $V_{GS} = 2V$

$V_{GS} \geq V_{th} \longrightarrow$ ON

$$R_D = \frac{V_{DD} - V_{DS}}{I_D} \Rightarrow V_{DS} = V_{DD} - R_D I_D$$

ASSUME SATURATION:

$I_D = K(V_{GS} - V_{th})^2$

$I_D = 1.23\times10^{-3}(2 - 1.6)^2$

$= 1.968\times10^{-4}\,A$

$\approx 196.8\,\mu A$

$V_{DS} = 5 - (4.7K)(1.968\times10^{-4})$

$= 4.075$

$V_{DS} > (V_{GS} - V_{th})$

$4.075 > 2 - 1.6$ ✓

in saturation region

• If $V_{GS} = 4V$

$V_{GS} \geq V_{th} \longrightarrow$ ON

$$R_D = \frac{V_{DD} - V_{DS}}{I_D} \Rightarrow I_D = \frac{V_{DD} - V_{DS}}{R_D}$$

ASSUME SATURATION:

$I_D = K(V_{GS} - V_{th})^2$

$I_D = 1.23\times10^{-3}(4 - 1.6)^2$

$= 7.0848\times10^{-3}\,A$

$= 7.085\,mA$

$$I_D = K'\left(\frac{W}{L}\right)\left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$(2.46\times10^{-3})\left[(4-1.6)V_{DS} - \frac{1}{2}V_{DS}^2\right] = \frac{5 - V_{DS}}{4.7K}$$

$1.23\times10^{-3}V_{DS}^2 + 29.31\times10^{-3}V_{DS} + 1.0638\times10^{-3} = 0$

$V_{DS} = 0.1805\,V$

CHECKING:

$V_D = I_D R_D = (7.085m)(4.7K)$

$= 33.3\,V \gg 5V$ (in Triode region)

$I_D = 1.025\times10^{-3}\,A$

$\approx 1.025\,mA$

3. When $V_{GS} = 1.46V$, $I_D = 35\mu$

When $V_{GS} = 2.18V$, $I_D = 430\,\mu A$

$I_D = K(V_{GS} - V_{th})^2$

$$\frac{35\mu}{430\mu} = \frac{K(1.46 - V_{th})^2}{K(2.18 - V_{th})^2}$$

$$(2.18 - V_{th})\sqrt{35/430} = (1.46 - V_{th})$$

$0.715\,V_{th} = 0.838$

$V_{th} = 1.172\,V$