Lab Number 5
EEE 108L – Electronics I - Laboratory
MOS Characteristics (One week)

Background

This lab will explore the DC characteristics of a MOS transistor. For the SPICE simulations and for the actual circuit, use the model of an n-channel transistor in the CD4007 MOS transistor.

Preliminary Calculations:

1. One of the conditions for forward active (saturation) region operation is $V_{DS} > (V_{GS}-V_{th})$. Show that this condition is equivalent to $V_{GD} < V_{th}$.
2. For the circuit of Figure 1, if $R_D = 4.7k\Omega$, $V_{DD} = 5V$, $\lambda = 0$. Calculate I_D and state whether the device is in the cutoff, saturation (forward active) or linear (triode) region of operation if V_{GS} =1V, 2V, and 4V.
3. Suppose that an n-channel MOSFET (not a CD4007 type) is measured to have $I_D = 35\mu$ when V_{GS} =1.46V and $I_D = 430\ \mu$ when V_{GS} = 2.18V. Find V_{th} for this MOSFET.

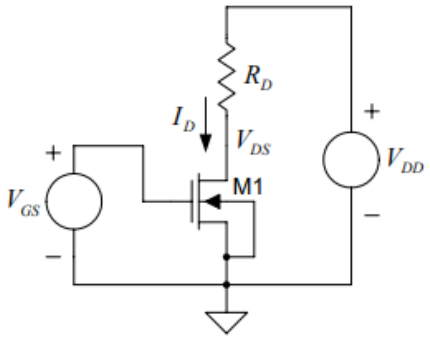

Figure 1

SPICE Simulations:

1. Enter the circuit of Figure 1 into SPICE. Do not specify the W and L values of the MOSFET on the schematic; these values are already in the model file. Set $V_{DD} = 5V$.
2. Run DC Sweep. Sweep V_{GS} from 0 to 5 volts. Obtain a plot of I_D as a function of V_{GS}. Also add a trace that is a mathematical expression for the drain current in the forward active region. $I_D = K(V_{GS}-Vth)^2$

   where $K = \frac{\mu C_{ox}}{2}\frac{W}{L}$,

   μCox is the SPICE model parameter K_P, Vth is the SPICE model parameter V_{TO}, and W and L are the transistor dimensions.) Refer to the model file of the CD4007 n-channel transistor to obtain these parameters.

3. Add a plot showing V_{GS}, V_{GD}, and V_{th}.
    - To plot V_{GD}, you will need to use a math function of two circuit voltages.
    - To plot V_{th}, just enter "1.6" as the trace expression.
4. Using vertical lines drawn on the graph, label the three regions of operation: cutoff, forward active, and linear (triode).
5. Change the circuit by removing R_D and replacing it with a wire. Now, V_{DS}= V_{DD}. Assign a DC value of 2V to V_{GS}, and then sweep V_{DD} from 0 to 5V. Obtain a plot of I_D.
6. Identify the value of V_{DS} at which the transistor transitions into its saturation (i.e., forward active) region.
7. Find an approximate value for ΔV_{DS} / ΔI_D in each region.
8. In the linear region, find R_{DS} = ΔV_{DS}/ ΔI_D and compare it with $R_{DS} = \left[\mu C'_{ox} \frac{W}{L}\left(V_{GS} - V_{th}\right)\right]^{-1}$
9. In the saturation region, find r_o= ΔV_{DS}/ ΔI_D and compare it with $r_o = \frac{1}{\lambda I_D}$
10. Put R_D back in the circuit. Repeat the simulation with the bulk terminal of the transistor connected to −1V instead of ground.
11. Run Bias point and find the value of V_{th}.

Laboratory Measurements:

1. Construct the circuit of Figure 1. Use one of the n-channel transistors on the CD4007 that has separate source and bulk connections. Connect the bulk terminal (pin 7) to the source terminal externally. Use the value of R_D used before.
2. It is preferable to use independently adjustable positive power supplies for V_{DD} and V_{GS}. Set V_{DD} to 5V and sweep V_{GS} from 0-5V. Record V_{GS}, V_{DS}, and calculate I_D. Tabulate your data. Take 4 data points that are in the forward active region and four that are in the linear region.
3. Determine values of V_{th}. Assume that $\lambda = 0$
4. For the circuit of Figure 1, adjust V_{GS} so that V_{DS} = 2V. Record this value of V_{GS}, and do not change it.
5. Vary V_{DD} from zero to about 7 volts, recording V_{DS} and I_D at about four data points in the linear region and about four points in the saturation region. Tabulate your data.
6. Connect the bulk terminal of the transistor under test to a fixed voltage equal to −1V.
7. Find a new value of V_{th}.