CPE 166 Quiz 2

Started: Nov 8 at 3:29pm

Quiz Instructions

Question 1 — 1 pts

What is the symbol used for signal assignment?

Your answer is _____ <= **_____**

Question 2 — 1 pts

```
process (CLK, reset)
 begin
    if (reset = '1') then
       Q <= '0';
   elsif (CLK'event and CLK = '1') then
       Q <= D;
   end if;
 end process;
```

The above code is the process for which hardware?

Your answer is _____ D Flip-Flop **_____**

Question 3 — 1 pts

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY shiftreg is
PORT (   CLK          : IN  STD_LOGIC;
         Sin          : IN  STD_LOGIC;
         Sout         : OUT STD_LOGIC);
END shiftreg;

ARCHITECTURE behavior OF shiftreg IS
   SIGNAL sreg        : STD_LOGIC_VECTOR(3 DOWNTO 0);
BEGIN

PROCESS(clk)
BEGIN
      IF FALLING_EDGE(CLK) THEN
                  sreg <= Sin & sreg(3 DOWNTO 1);
            END IF;
      END IF;
end process;
Sout <= sreg(0);
end behavior;
```

What is the synthesized hardware circuit for the above VHDL code?

The answer is _____ The falling edge triggered right s

_____

Question 4

1 pts

s(15 downto 0) <= s(15)&s(15)&s(15)&s(15 downto 3);

What is the synthesized hardware circuit for the above VHDL code?

The answer is _____ A 16-bit arithmetic shift right by

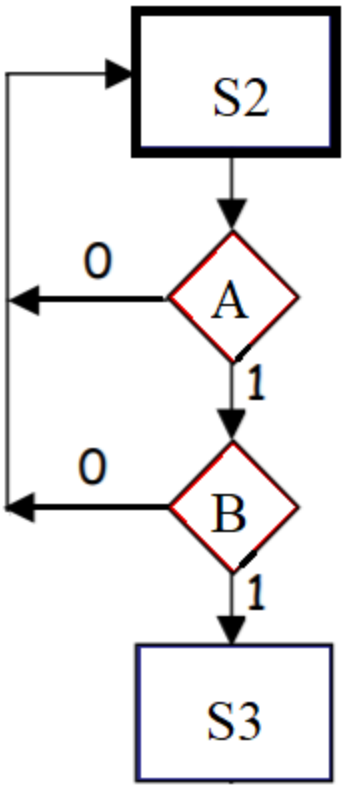
_____

Question 5 — 1 pts

Generate the following waveform for signal x by using VHDL.

x <= '1', '0' after 2 ns, '1' after _ 3 _ ns, '0' after 4 ns, '1' after 5 ns;

Question 6 — 1 pts



Part of the ASM chart is shown above. Fill out the blank1 for the VHDL code below.

```
process(state, A, B)
begin
case state is
when s0 => …
when s1 => ...
when s2 => if A = '0' then next_state <= s2;
            elsif B = '0' then
                next_state <= s2;
            else next_state <= ____ s3 ___;
            end if;
```

```
…
End case;
End process;
```

Question 7

1 pts

```
…
Architecture  circuit of  mydesign is
signal    m:                std_logic_vector(1 downto 0);
signal    f, g, h, k:                 std_logic;
signal    q, p, w:          std_logic;
beign

with  m  select
          q <=  f and g when “00”,
                h  when “01”,
                h  when  “10”,
                k  when  others;

process(  clk )
begin
    if (rising_edge clk ) then
          p <=  q;
          w <=  not p;
```

end if;

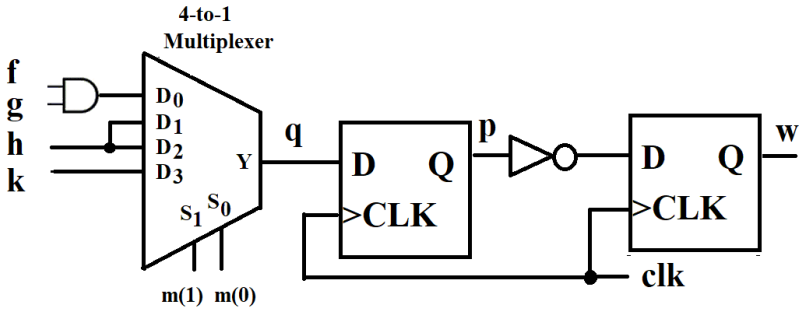
end process;

end circuit;

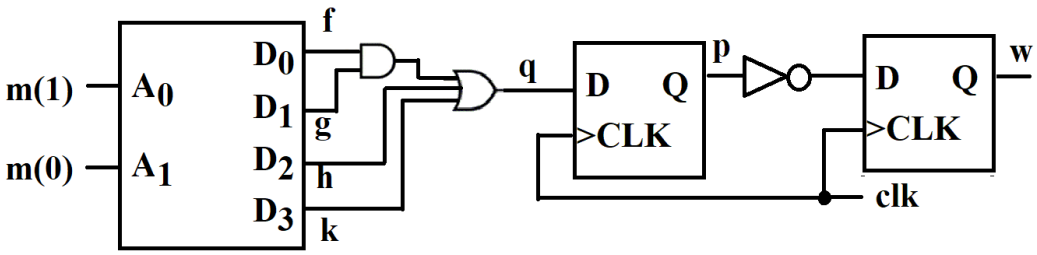
Which synthesized circuit corresponds to the VHDL design above?

Your answer is _____ a _____.

(a).



(b).



(c). None of above

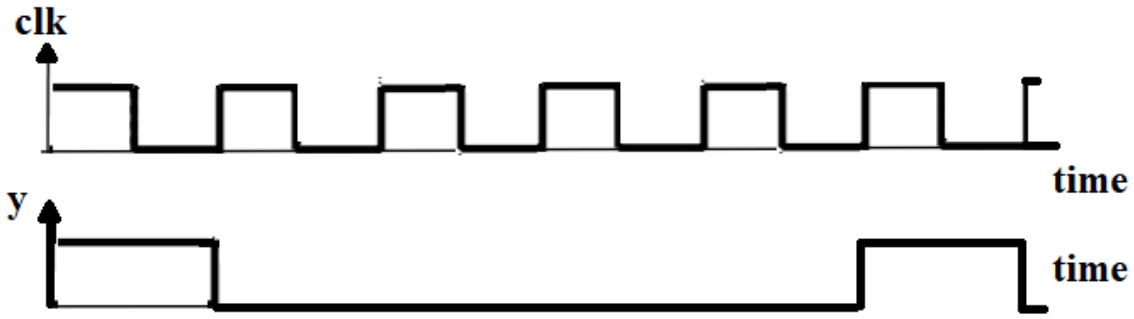
Question 8 — 1 pts

library ieee;

```
use ieee.std_logic_1164.all ;
use ieee.std_logic_unsigned.all ;
use ieee.std_logic_arith.all;
entity pulse is
port( clk, reset: in std_logic;
w: in std_logic_vector (3 downto 0) ;
y: out std_logic );
end pulse;

architecture arch of pulse is
signal r_reg : std_logic_vector(3 downto 0) ;
begin

process (clk, reset)
begin
if (reset='1') then
  r_reg <= (others=>'0');
  y     <= '0';
elsif (clk'event and clk='1') then
  if(r_reg = __ "100" __)  then
     r_reg <= (others=>'0');
     y <= '1';
  else
     r_reg <= r_reg + 1;
     y <= '0';
  end if;
```

```
end if;

end process;


end arch;
```

Suppose the VHDL design above is used to design the following pulse y output based on the clk waveform shown below. The waveform y is a periodic pulse with logic ‘1’ for one clk cycle and logic ‘0’ for four clk cycles. The value for __[blank1]__ is



Question 9

1 pts

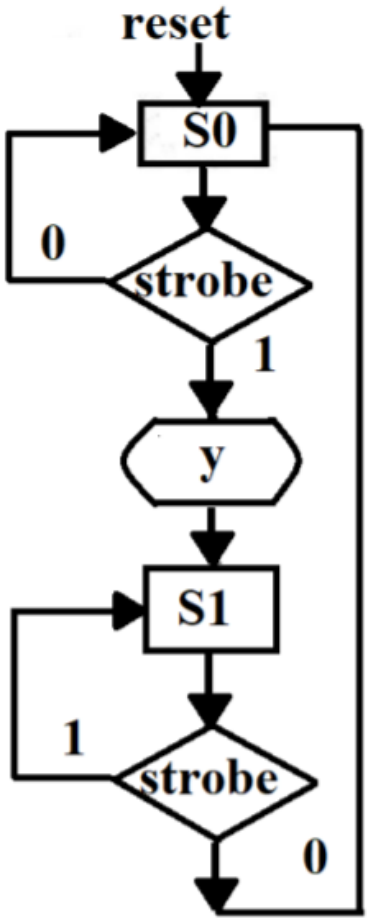
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

 entity ram is
 port (
  address :in    std_logic_vector ( 4 downto 0);
  data    :inout std_logic_vector ( 1 downto 0);
  cs      :in    std_logic;
  we      :in    std_logic;
```

```
  oe      :in    std_logic
 );
end ram;

architecture beh_ram of ram is
type memory is array (0 to 31) of std_logic_vector (1 downto 0);
signal mem : memory ;
begin

  MEM_WRITE:
  process (address, data, cs, we)
  begin
    if (cs = '1' and we = '1') then
      mem(conv_integer(address)) <= data;
    end if;
  end process;

  MEM_READ:
  process (address, cs, we, oe, mem)
  begin
    if (cs = '1' and we = '0' and oe = '1')  then
      data <= mem(conv_integer(address));
    else
      data <=  (others => 'Z' );
    end if;
  end process;


end beh_ram;
```

The VHDL code above corresponds to a RAM of ___ 32 by 2 ___

Question 10 — 1 pts

The ASM chart and the corresponding VHDL design are shown below.




```
library ieee;
use ieee.std_logic_1164.all;
entity design1 is
port(
reset,clk: in std_logic;
strobe:    in std_logic;
y :        out std_logic
);
end design1;
architecture arch of design1 is
constant S0: std_logic:= '0';
constant S1: std_logic:= '1';
```

```
signal cs, ns: std_logic;
begin
process (clk, reset)
begin
if reset = '1' then
  cs <= S0;
elsif (rising_edge(clk)) then
  cs <= ns;
end if;
end process;

process(cs, strobe)
begin
case cs is
when S0=> if strobe = '1' then
ns <= S1;
else
ns <= S0;
end if;
when S1=> if strobe = '1' then
ns <= S1;
else
ns <= S0;
end if;
when others=> ns <= S0;
end case;
end process;
```

y <= '1' when ____ (cs=S0) and (strobe='1') ____ else '0';

end arch;

The above VHDL design is used to detect __ rising edge ___of the strobe input.

No new data to save. Last checked at 3:31pm

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