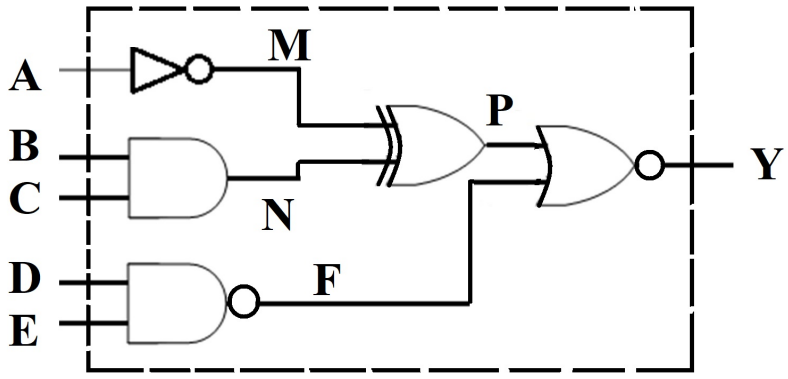
CPE166 Midterm 1 - Part 1

Started: Oct 7 at 9:03am

Quiz Instructions

Question 1 — 16 pts

Write the Verilog program for the following combinational circuit.



module cir1 (A, B, C, D, E, Y);

__ input __ A, B, C, D, E;

__ output __ Y;

__ wire __ M, N, P, F;

assign M = __ ~A __ ;

assign F = ___ ~ (D & E) __ ;

assign N = ___ B & C ___;

assign P = ___ M ^ N ___;

assign Y = ___ ~ (P | F) __;

endmodule

Question 2

48 pts

2.[22 points] Use Verilog hierarchical design method to design the following circuit.
1). Design rising edge clock triggered 1-bit D FlipFlop with high active synchronous reset.

module dff (D, clk, reset, Q);

input ____ D, clk, reset _____;

output ___ Q _____;

reg _____ Q _____;

always@(___ posedge __clk_)

begin

if (reset)

_____ Q <= 0; _____;

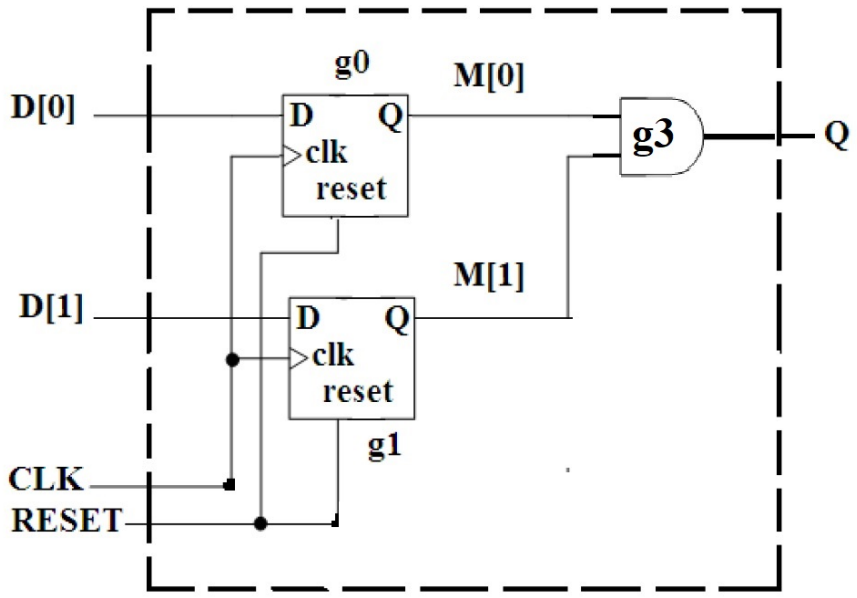
else

_____ Q <= D _____;

end

endmodule

2). Use dff above to implement the following circuit and complete the Verilog design.



module cir2 (D, CLK, RESET, Q);

input ___ D, CLK, RESET _____;

input CLK, RESET;

output Q;

_____ wire ___Q_____ ; // Other internal signals

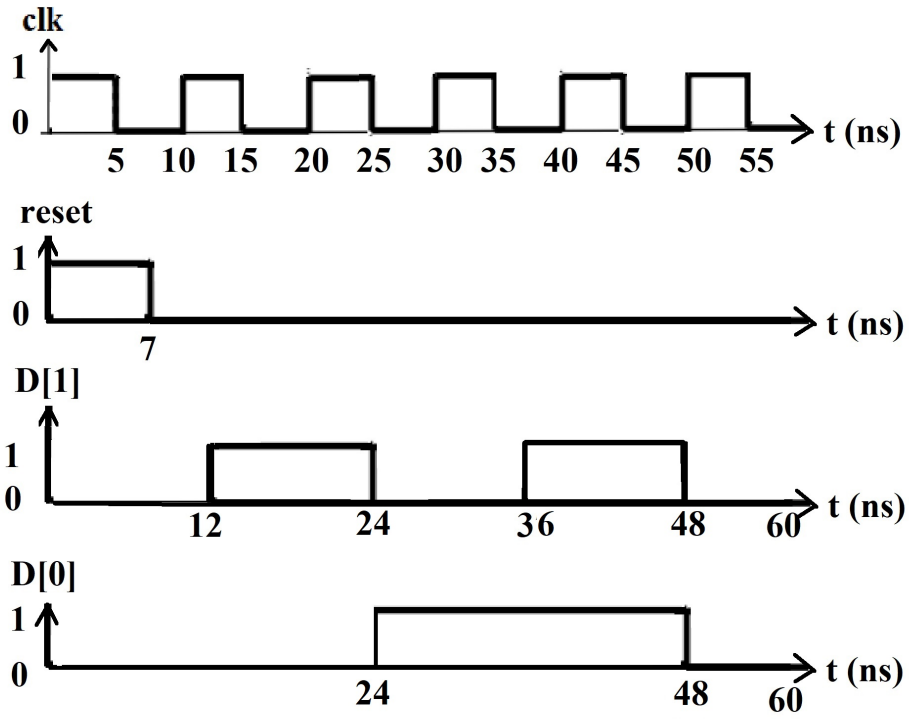
dff g0(_____ D[0], CLK, RESET, M[0] _____);

dff g1(_____ D[1], CLK, RESET, M{1] _____);

and g3 (___ M[0], M[1], Q _____);

endmodule

3). Write Verilog testbench for the above cir2.v design based on the following waveform.



`timescale 1ns/1ns

module tb;

____ input __ clk, reset;

____ input [1:0] D ___;

____ output __ Q;

cir2 uut (____ CLK, RESET, D, Q ____);

initial clk = __ 1 ___;

always __ #5 ___ clk = ~ clk;

initial begin

reset = __ 1 ____;

D = __ 2'b00 ____;

#7 reset = __ 0 ____;

__ #5 D=2'b01 ____;

__ #12 D=2'b01 ____;

__ #10 D = 2'b11 ____;

__ #12 D=2'b11 ____;;

#10 $stop;

end

endmodule

Quiz saved at 9:58am

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