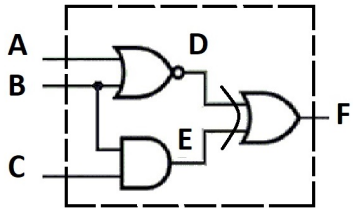
CPE166 Quiz 1 Results for Casey Chan

ⓘ Correct answers are hidden.

Score for this attempt: **100** out of 100
Submitted Mar 1 at 2:54pm
This attempt took 23 minutes.

Question 1

18 / 18 pts



Design the above circuit in Verilog by selecting one correct answer from each drop box below.

module cir (A, B, C, F);

__input ____ A, B, C;

__output ____ F;

__wire ____ D, E;
assign D = __~ (A | B) ____ ;
assign E = __B & C ____ ;
assign F = __D ^ E ____ ;
endmodule

Answer 1:

input

Answer 2:

output

Answer 3:

wire

Answer 4:

~ (A | B)

Answer 5:

B & C

Answer 6:

D ^ E

Question 2

18 / 18 pts

```
// This is a testbench for question 1.
module cir_tb;

__reg ______  A, B, C    ;

__wire ______   F  ;

__integer ______     i;

cir   uut (  ______A, B, C, F ______     ) ;

initial

begin

      for ( i = 0;   i < _____8 ______     ; i=i+1 )
      begin
          _______{ A, B, C } = i; ______ ;
         #10;
      end

     #10  $stop;
end
endmodule
```

Answer 1:

reg

Answer 2:

wire

Answer 3:

integer

Answer 4:

A, B, C, F

Answer 5:

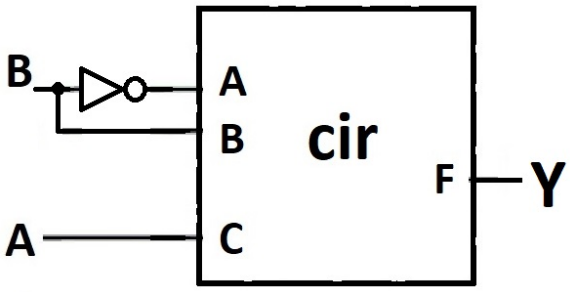
8

Answer 6:

{ A, B, C } = i;

Question 3

4 / 4 pts



// The verilog design of cir.v is the same as that used in question 1.

module question3 (A, B, Y);

input A, B;

output Y;

cir g1 (.A ([Select]), .B (

[Select]), .C (

[Select]), .F(

[Select]));

endmodule

Answer 1:

~B

Answer 2:

B

Answer 3:

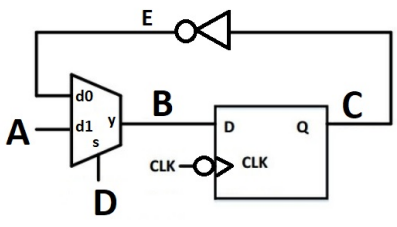
A

Answer 4:

Y

Question 4

18 / 18 pts



Design the above circuit in Verilog and select one answer for each drop box below.

```
module cir2 ( A,  D, C, CLK );

input  A, D, CLK;

output  C;

____wire ___  E;

____reg ___  B;

 ____reg ___C;

assign  E = ~ C;

always@( ___A or D or E __)
begin

    if (___D __)
        ___B=A __;
    else
        ___B=E __;
end
always@(___negedge CLK __)
  ___C<=B __;

endmodule
```

Answer 1:

wire

Answer 2:

reg

Answer 3:

reg

Answer 4:

A or D or E

Answer 5:

D

Answer 6:

B=A

Answer 7:

B=E

Answer 8:

negedge CLK

Answer 9:

C<=B

Question 5

12 / 12 pts

Design a counter circuit in Veirlog. The counter updates its value on the rising edge of the clock. It counts from 0 to 219, and then repeats..

```
module  cir4 ( clk, cnt );        // cnt is the counter output
input      clk;

// Use minimally allowed number of bits for

// the following blanks.

output  [  __ 7 __ : 0   ]   cnt;

reg       [  __ 7 __ : 0 ]  cnt;

always@(posedge  clk)

begin
```

```
    if (  cnt == __ 219 __ )          // Type a decimal number
here
          cnt <= __ 0 __ ;            // Type a decimal number
here
    else
        cnt  <= cnt  + 1;
end
endmodule
```

Answer 1:

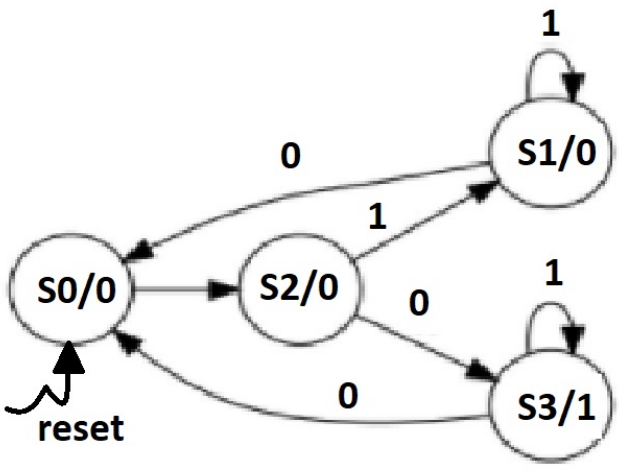
219

Answer 2:

0

Question 6

30 / 30 pts



Design the above finite state machine in Verilog by selecting one correct answer for each of the drop boxes below.

```
module   fsm ( reset, clk,  a,  y );

input    reset,  clk,  a;

output    a;

reg         a;

parameter  S0 = 2'b00, S1=2'b01, S2=2'b10, S3=2'b11;

__reg [1:0] __   cs,  ns;
// cs:  current state,   ns: next state

always@(  posedge clk or posedge reset )
begin

      if(reset)

        ___cs<=S0 _;
      else
          ___cs <= ns _;
end

always@(  cs or a )

begin
    case( cs)
      S0:        ns = S2;
      S1:        if (a)   ns = __S1 _;
                 else    ns = __S0 _;

      S2:        if (a)   ns = __S1 _;
                 else    ns = __S3 _;

      S3:        if (a)   ns = __S3 _;
                 else    ns = __S0 _;

      default:    ns = S0;

      endcase

end

always@(  cs )

begin
    case( cs)
      S0:        y= ___0 _;
      S1:        y= ___0 _;
```

```
    S2:     y= ___0 _;
    S3:     y= ___1 _;
    default:  y = 0;
    endcase
end
```

Answer 1:

reg [1:0]

Answer 2:

posedge clk or posedge reset

Answer 3:

cs<=S0

Answer 4:

cs <= ns

Answer 5:

S1

Answer 6:

S0

Answer 7:

S1

Answer 8:

S3

Answer 9:

S3

Answer 10:

S0

Answer 11:

cs

Answer 12:

0

Answer 13:

0

Answer 14:

0

Answer 15:

1

Quiz Score: **100** out of 100