

Laboratory 04

CPE 166 Advanced Logic Design

Section 03

Vigomar Kim Algador

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INTRODUCTION

This laboratory is an extensive topic using Verilog and the other designs that were introduced previously in the past laboratories such as FSM and hierarchical design. This laboratory is divided into 2 main topics. The first part of the laboratory introduces the SRAM which stands for Static Random Access Memory. This part of the laboratory will be designing an FSM, RAM, and the final top design combining the two. The second part of the laboratory is writing a simplified microprocessor design. This part of the laboratory is divided into 2 sub parts: Microprocessor Data Path Design and Microprocessor Design.

PART 1: SRAM DESIGN

Design Purpose and Engineering Data

This part of the laboratory introduced to student about the concept of SRAM designing. The student is required to write a 4'b1010 into the 32 address locations of the SRAM and read data from RAM. The SRAM is based on the following function table given by the laboratory manual shown below.

WE	CS	OE	Function
X	L	X	High – z
L	H	L	High – z
L	H	H	Read Data
H	H	X	Write Data

RAM Design

At first, the student design the RAM for this project based on what information learned from the lecture. Using the instructions given, the student was able to format the design by changing the address and data.

```
1 module ram ( address, data, cs, we, oe);
2   input cs, we, oe;
3   input [4:0] address;
4   inout [3:0] data;
5
6   reg [3:0] data_out ;
7   reg [3:0] mem [0:31];    //32-bit address bus, 8-bit data bus.
8
9   assign data = (cs && oe && !we) ? data_out : 4'bzzzz;
10
11  always @ (cs or we or data or address)
12  begin
13      if (cs && we)
14          mem[address] = data;    // write
15  end
16
17  always @ (cs or we or oe or address or data)
18  begin
19      if (cs && !we && oe)
20          data_out = mem[address];    // read
21  end
22  endmodule
```

Figure 1. RAM Verilog design (ram.v)

For the second design, the student is required to design an FSM which is shown below.

```

1 module mem_fsm ( clk, reset, address, data, cs, we, oe);
2 input  clk, reset;
3 output [4:0] address;
4 inout  [3:0] data;
5 output  cs, we, oe;
6
7 reg  cs, we, oe;
8 reg  [4:0] address;
9 reg  [3:0] data_reg;
10 reg  [2:0] state;
11 parameter idle = 3'b000, s1=3'b001, s2=3'b010, s3=3'b011, s4=3'b100;
12 assign data = data_reg;
13
14 always@(posedge clk or posedge reset)
15 begin
16     if (reset) begin
17         state <= idle;
18         address <= 0;
19     end
20     else
21         case (state)
22             idle: begin
23                 state <= s1;
24                 address <= 0;
25             end
26             s1: begin
27                 state <= s2;
28                 address <= 0;
29             end
30             s2: begin
31                 address <= address + 1;
32                 if(address == 31)
33                     state <= s3;
34                 else
35                     state <= s2;
36             end
37             s3: begin
38                 state <= s4;
39                 address <= 0;
40             end
41             s4: begin
42                 address <= address + 1;
43                 if(address == 31)
44                     state <= idle;
45                 else
46                     state <= s4;
47             end
48         endcase
49         state <= idle;
50         address <= 0;
51     end
52 endcase
53 end
54
55 always@(state)
56 begin
57     case (state)
58         idle: begin
59             cs = 0; we = 0; oe = 0;
60             data_reg = 4'bzzzz;
61         end
62         s1: begin //writing
63             cs = 1; we = 1; oe = 0;
64             data_reg = 4'b1010;
65         end
66         s2: begin //writing
67             cs = 1; we = 1; oe = 0;
68             data_reg = 4'b1010;
69         end
70         s3: begin //reading
71             cs = 1; we = 0; oe = 1;
72             data_reg = 4'b1010;
73         end
74         s4: begin //reading
75             cs = 1; we = 0; oe = 1;
76             data_reg = 4'b1010;
77         end
78         default: begin
79             cs = 0; we = 0; oe = 0;
80             data_reg = 4'bzzzz;
81         end
82     endcase
83 end
84 endmodule

```

Figure 2. FSM Verilog Design (mem_fsm.v)

Final SRAM design

Lastly, the student needs to combine the files by creating a top design.



Figure 3. Final TOP Verilog design (top.v), testbench (top_tb.v), and simulation

Result Discussion

For this part of this laboratory, I was able to design the whole SRAM project with 3 files: RAM, FSM, and TOP. The only challenging part of this design is the FSM for this project, however, the guidelines and information taught in the class are really helpful to design the overall project.

PART 2: SIMPLIFIED MICROPROCESSOR DESIGN (1)

Design Purpose and Engineering Data

For this part of the laboratory, I will be designing the first component which is the microprocessor data path design of the simplified microprocessor block diagram shown below.

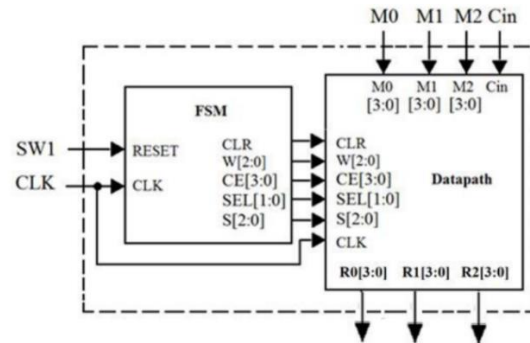


Figure 4. Simplified Microprocessor Block Diagram

Within the Datapath, below is the full design shown below.

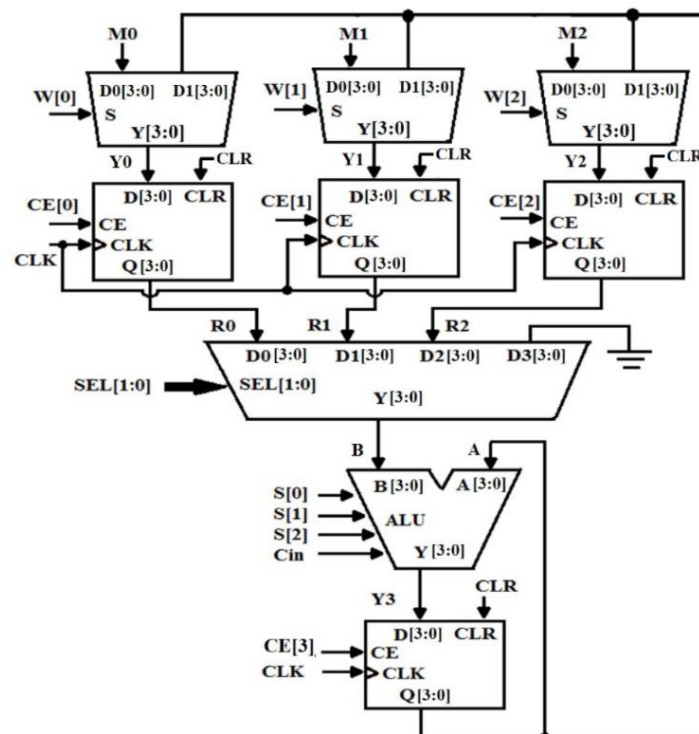


Figure 5. Simplified Microprocessor Datapath Circuit

With the given information, this part 2 requires using structural hierarchical design method to implement the data path circuit.

Multiplexer Design

For the first design, I was able to write the multiplexer using the knowledge I have from previous laboratories. There will be two different multiplexers for this project. The first multiplexer will be the mux2 which is the top part of the data path circuit shown below.

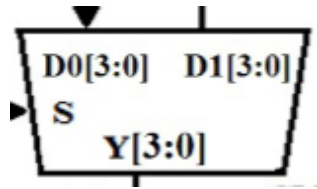


Figure 6. multiplexer for mux2 block

With this, I was able to write the Verilog and testbench for it shown below.

```

1 // Vigomar Kim Algador
2 // CpE166 Section 03
3 // Laboratory 04: Part 02-03
4 // 4-bit multiplexer (MUX2)
5
6 module mux2_tb;
7     reg [3:0] D0, D1;
8     reg S;
9     wire [3:0] Y;
10    integer k;
11
12    mux2 u1(D0, D1, S, Y);
13
14    initial begin
15        for (k = 0; k < 512; k = k+1)
16            #10 {D0, D1, S} = k;
17        #10 $stop;
18    end
19 endmodule
20
1 // Vigomar Kim Algador
2 // CpE166 Section 03
3 // Laboratory 04: Part 02-03
4 // 4-bit multiplexer (MUX2)
5
6 module mux2(D0, D1, S, Y);
7     input [3:0] D0, D1;
8     input S;
9     output [3:0] Y;
10    reg [3:0] Y;
11
12    always @ (D0 or D1 or S)
13    begin
14        if (S == 1)
15            Y = D1;
16        else
17            Y = D0;
18    end
19 endmodule
20

```

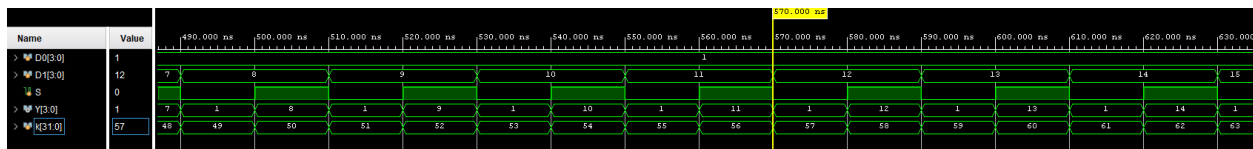


Figure 7. mux2 Verilog, testbench, and simulation

For another multiplexer design, below is the mux4 block diagram that I need to follow and write in Verilog. Using the same design from mux2, I was able to modify changes and write the Verilog as well as testbench shown in figure 9.

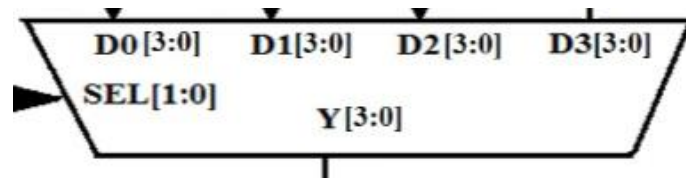


Figure 8. multiplexer mux4 block

```

1 // Vigomar Kim Algador
2 // CpE166 Section 03
3 // Laboratory 04: Part 02-03
4 // 4-bit multiplexer (MUX4)
5
6 module mux4_tb;
7     reg [3:0] D0, D1, D2, D3;
8     reg [1:0] SEL;
9     wire [3:0] Y;
10    integer k;
11
12    mux4 u2(D0, D1, D2, D3, SEL, Y);
13
14    initial begin
15        for (k = 0; k < 262144; k = k+1)
16            #10 {D0, D1, D2, D3, SEL} = k;
17        #10 $stop;
18    end
19 endmodule
20
21
22

```

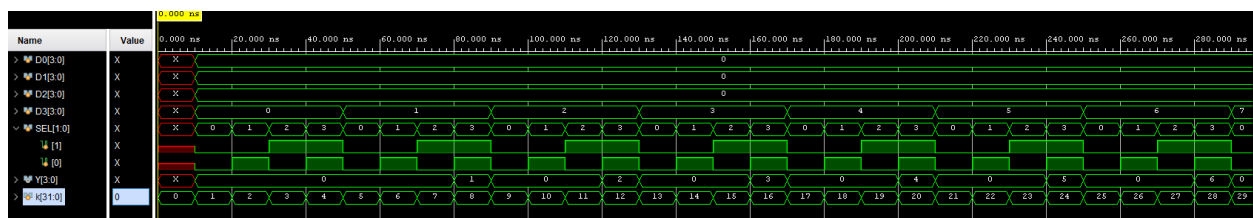


Figure 8. mux4 Verilog, testbench, and simulation

D Flip-Flop Design

Next, I was able to check the block for the d flipflop design shown below. With this, I was able to write the Verilog and testbench shown in figure 10.

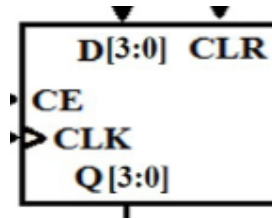


Figure 9. D Flip-Flop block

```

1 // Vigomar Kim Algador
2 // CpE166 Section 03
3 // Laboratory 04: Part 02-03
4 // D-Flip Flop (dff.v)
5
6 module dff(D, CLR, CE, CLK, Q);
7     input [3:0] D;
8     input CLR, CE, CLK;
9     output reg [3:0] Q;
10
11     always@(posedge CLK or posedge CLR)
12     begin
13         if (CLR)
14             Q <= 0;
15         else if (CE)
16             Q <= D;
17     end
18 endmodule
19
20 // Vigomar Kim Algador
21 // CpE166 Section 03
22 // Laboratory 04: Part 02-03
23 // D-Flip Flop (dff.v)
24
25 module dff_tb;
26     reg [3:0] D;
27     reg CLR, CE, CLK;
28     wire [3:0] Q;
29
30     dff u1(D, CLR, CE, CLK, Q);
31
32     initial CLK = 0;
33     always #10 CLK = ~CLK;
34
35     initial begin
36         CLR = 1; D = 1; CE = 1;
37         #10 CLR = 0;
38         #10 CE = 0;
39         #50 $stop;
40     end
41 endmodule

```

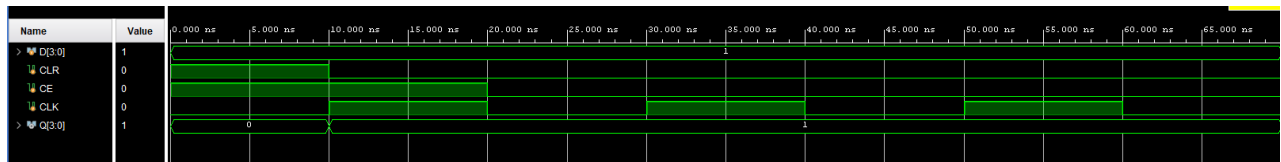


Figure 10. D flipflop Verilog, testbench, and simulation

ALU Design

For the next design, I need to design the ALU diagram shown below.

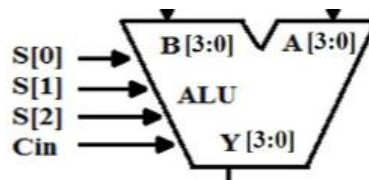


Figure 11. ALU block

There is a truth table for the ALU diagram inside the data path circuit shown below.

S[2]	S[1]	S[0]	ALU Output F
0	0	0	$F = A + B + \text{Cin}$
0	0	1	$F = A + B' + \text{Cin}$
0	1	0	$F = B$
0	1	1	$F = A$
1	0	0	$F = A \text{ AND } B$
1	0	1	$F = A \text{ OR } B$
1	1	0	$F = A'$
1	1	1	$F = A \text{ XOR } B$

```

1 // Vigomar Kim Algador
2 // CpE166 Section 03
3 // Laboratory 04: Part 02-03
4 // ALU
5
6 module ALU(A, B, S, Cin, Y);
7     input [3:0] A, B;
8     input [2:0] S;
9     input Cin;
10    output [3:0] Y;
11    reg [3:0] Y;
12
13    always@(S) begin
14        case(S)
15            0: Y = A + B + Cin;
16            1: Y = A + (~B) + Cin;
17            2: Y = B;
18            3: Y = A;
19            4: Y = A&B;
20            5: Y = A|B;
21            6: Y = ~A;
22            7: Y = A^B;
23        endcase
24    end
25 endmodule

```

```

1 // Vigomar Kim Algador
2 // CpE166 Section 03
3 // Laboratory 04: Part 02-03
4 // ALU
5
6 module ALU_tb;
7     reg [3:0] A, B;
8     reg [2:0] S;
9     reg Cin;
10    wire [3:0] Y;
11    integer i,j;
12
13    ALU uut(B, A, S, Cin, Y);
14
15    initial begin
16        A = 0; B = 0; Cin = 0; S = 0; #10;
17
18        for (i = 0; i < 2; i = i+1) begin
19            for (j = 0; j < 8; j = j+1) begin
20                A = 6; B = 12; Cin = i; S = j; #10;
21            end
22        end
23        #10 $stop;
24    end
25 endmodule

```

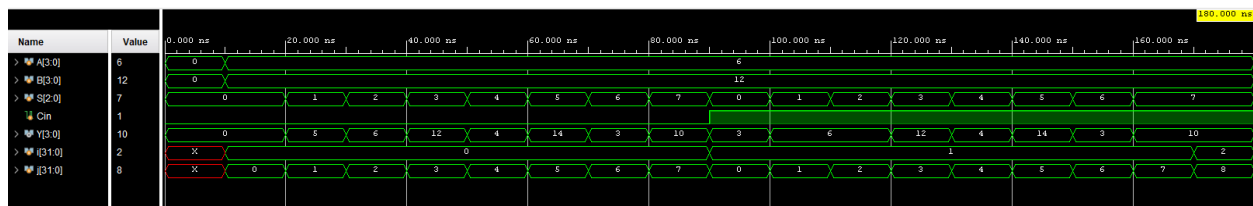


Figure 12. ALU Verilog, testbench, and simulation

Final Microprocessor Data Path Design

Finally, I need to connect all the components I did to create the Datapath that was shown in figure

5. Below is the full Verilog, testbench, as well as the final simulation for the Datapath.

```
1 // Vigomar Kim Algador
2 // CpE166 Section 03
3 // Laboratory 04: Part 02-03
4 // Datapath Verilog
5
6
7 module datapath(M0, M1, M2, Cin, CLR, W, CE, SEL, S, CLK, R0, R1, R2);
8     input [3:0] M0, M1, M2, CE;
9     input [2:0] W, S;
10    input [1:0] SEL;
11    input Cin, CLR, CLK;
12    output [3:0] R0, R1, R2;
13
14    wire [3:0] Y0, Y1, Y2, Y3, A, B;
15
16    mux2 m1 (.D0(M0), .D1(A), .S(W[0]), .Y(Y0));
17    mux2 m2 (.D0(M1), .D1(A), .S(W[1]), .Y(Y1));
18    mux2 m3 (.D0(M2), .D1(A), .S(W[2]), .Y(Y2));
19
20    dff d1 (.D(Y0), .CLR(CLR), .CE(CE[0]), .CLK(CLK), .Q(R0));
21    dff d2 (.D(Y1), .CLR(CLR), .CE(CE[1]), .CLK(CLK), .Q(R1));
22    dff d3 (.D(Y2), .CLR(CLR), .CE(CE[2]), .CLK(CLK), .Q(R2));
23
24    mux4 m4 (.D0(R0), .D1(R1), .D2(R2), .D3(0), .SEL(SEL), .Y(B));
25
26    ALU al (.A(A), .B(B), .S(S), .Cin(Cin), .Y(Y3));
27
28    dff d4 (.D(Y3), .CLR(CLR), .CE(CE[3]), .CLK(CLK), .Q(A));
29
30 endmodule
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CONCLUSION

This part of laboratory introduced to more topics using Verilog. This laboratory was divided into 2 parts: SRAM and Microprocessor Design. The first part of the laboratory, I was able to design SRAM project with 3 files: RAM, FSM, and the top combining the RAM and FSM. This part of the laboratory was simple as I was able to use the knowledge I learned from the lecture with the RAM and FSM from the previous laboratory. In the second part of the laboratory, Microprocessor design, I was only able to write the Datapath without the FSM as I ran into issues with Datapath and ran out of time with demonstration. Within the Datapath, I was tasked to use the structural hierarchy to design the circuit. I was able to write the components such as the multiplexer, D flip-flop, and ALU. However, the final step which is combining the whole component got me stuck with the testbench as the output I got doesn't match to the correct output. With this, I checked each component all over again and test it one-by-one to check for any errors. After several times, I was able to fix it and got the correct output. This part of the laboratory was definitely challenging as I am designing an application to the previous topics discussed.