## EEE64-CpE64\_TentativeScheduleSpring2022.xlsx

| WEEK                 | DATE      | LECTURE TOPIC  | HOMEWORK | LAB: See your Lab Instructor for       |
|----------------------|-----------|--|----------|--|
| <u>1</u>             | 1/25/2022 | Intro./Number Systems  |          | Discussion Activities                  |
|                      |           | Logic Intro  |          |  |
| <u>2</u>             | 2/1/2022  | Binary Numbers   |          | Activity Lab0: Lab Intro               |
|                      |           | Number Conversions   |          |  |
| <u>3</u>             | 2/8/2022  | Logic Gates,   |          | Activity Lab1:Logic gates              |
|                      |           | Truth Tables, Schematics   | HW#0 due |  |
| 4                    | 2/15/2022 | Boolean Algebra, DeMorgan's Theorem                              |          |  |
|                      |           | DeMorgan's Theorem   |          |  |
| <u>5</u>             | 2/22/2022 | FPGA and Verilog Introduction, Schematics                        |          | Activity Lab2: Combinational Logic / V |
|                      |           | Minterms & Maxterms  | HW#1 due |  |
| <u>6</u>             | 3/1/2022  | Karnaugh Map Theory & Examples                                   |          |  |
|                      |           | Binary Addition & Adders, Carry Bit                              |          |  |
| <u>7</u>             | 3/8/2022  | Signed Numbers, 2's Comp   |          | Activity Lab3:                         |
|                      |           | Comparators, Sign Bit  |          |  |
| <u>8</u><br><u>9</u> | 3/15/2022 | Catchup & MidTerm Review   | HW#2 due |  |
|                      | 2/22/222  | MidTerm #1   |          | Activity Lab4:                         |
|                      | 3/22/2022 | Spring Recess  |          |  |
| <u>10</u>            | 3/29/2022 | Introduction To Latches & Flip Flops                             |          |  |
|                      |           | S-R Latches & D & T & JK Flip Flops                              |          |  |
| 11                   | 4/5/2022  | Registers, Counters  |          |  |
|                      |           | Simulation & Timing Diagrams                                     | HW#3 due |  |
| <u>12</u>            | 4/12/2022 | State Machine Analysis   |          | Activity Lab4:                         |
|                      |           | Verilog Descriptions of State Machines                           |          |  |
| <u>13</u>            | 4/19/2022 | Catchup & MidTerm Review   | HW#4 due |  |
|                      |           | MidTerm #2   |          | Activity Lab5: State Machintes         |
| <u>14</u>            | 4/26/2022 | State Machine Designs with Mealy & Moore                         |          |  |
|                      |           | State Machine Designs with Mealy & Moore                         |          | Activity Lab6: State Machines Applicat |
| <u>15</u>            | 5/3/2022  | LEDs & Seven Seg., Resistors, Decoders                           |          |  |
|                      |           | Buffers/Drivers, Tri-State Devices ALUs and output Flags -NCVZ   | HW#5 due | Activity Lab7:Project State Mach. App  |
| <u>16</u>            | 5/10/2022 | Memory & Data Transfers, Basic CPUs                              |          | Lab Project Presentation               |
|                      |           | Microprocessor Instructions & Opcodes, Registers and I/O Devices |          |  |
| <u>17</u>            | 5/17/2022 | Finals Week  | HW#6 due |  |
|                      |           |  | HW#7 due |  |
|                      |           |  |          |  |

Homework from selected sources **General Notes:** 

References **OpenSourceBooks** 

<u>Mano</u>

Digi
Digital Logic
Exp
Reference

EEE64-CpE64 Syllabus EEE64-CpE64 Website

EEE64-CpE64 ECS Webclass