# Semiconductors

Perry L Heedley, Ph.D.

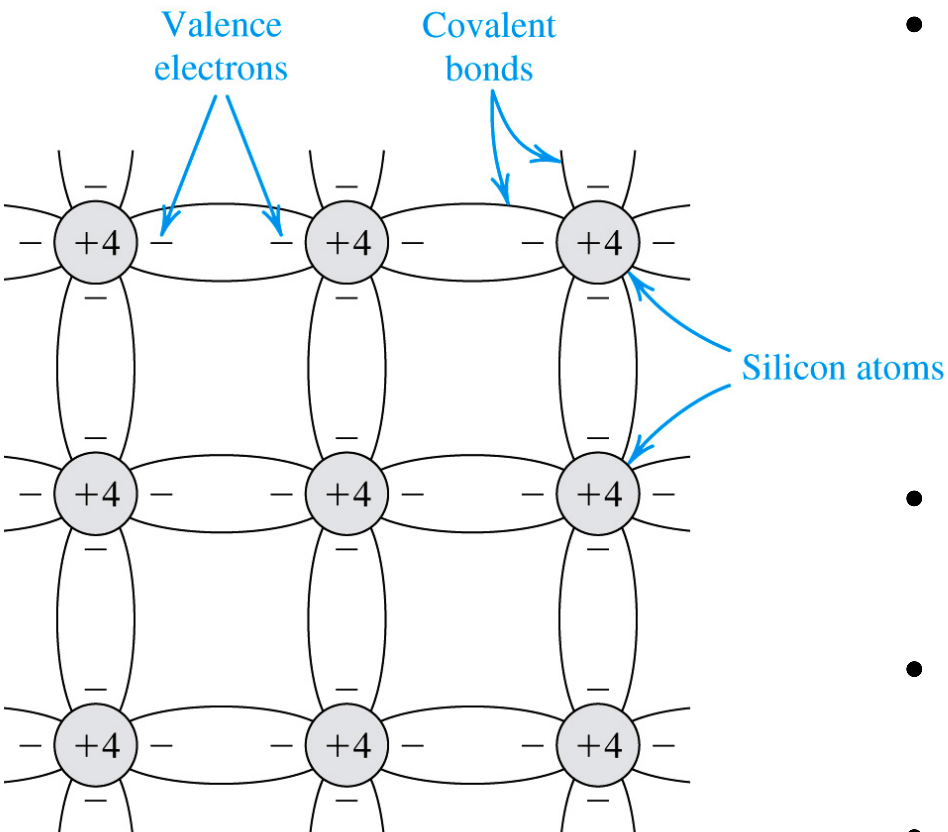


* Most figures and examples are from the course textbook "Microelectronic Circuits" by Adel S. Sedra and Kenneth C. Smith, 6th Edition, © 2010 by Oxford University Press, Inc.

# Outline

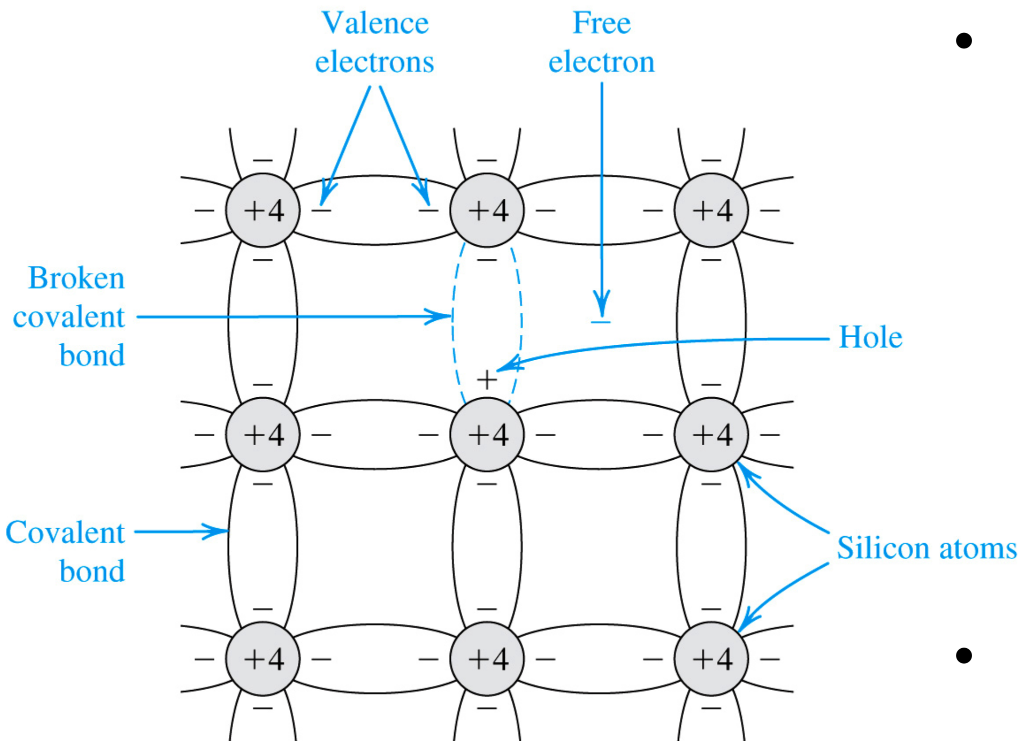
- Semiconductor Fundamentals
  - Intrinsic Semiconductors
  - Doped Semiconductors
- PN junctions
  - Physical structure, the depletion region, built-in voltage
  - Current-Voltage relationship
  - Reverse Breakdown
  - Capacitance of PN junctions
    - Depletion region capacitance
    - Diffusion capacitance
- Summary of key concepts

# Intrinsic Semiconductors




- **Semiconductors** are materials whose resistance can be varied over a wide range by adding controlled amounts of impurity atoms, which is called **doping**
- **Intrinsic semiconductors** are pure, without doping
- **Silicon** is the most widely used semiconductor today
- Silicon has 4 electrons in its outermost shell, which form **covalent bonds** to form a **crystal**

# Intrinsic Semiconductors




- At room temperature (300°K = 27°C) there is enough thermal energy to break some bonds and create **electron-hole pairs**
  - Called **Thermal Generation**
  - True at any temp > 0°K (0°K = **Absolute Zero**)
- These free electrons and holes are **charge carriers** which can move around and conduct electricity

  **p = number of free holes**

  **n = number of free electrons**

- A hole is really just the absence of an electron, but can be thought of as a positively charged particle

# Intrinsic Semiconductors

The **intrinsic carrier concentration**, $n_i$ , is given by :

$$\boxed{n_i = BT^{3/2}e^{-E_g/2kT} \approx 1.5\,x10^{10}/cm^3 \;\; at\; 300^\circ K}$$

$$for\; Si: \;\; Eg = 1.12eV, \;\; B = 7.3x10^{15}cm^{-3}K^{-3/2}$$

$$\boxed{\begin{array}{l} p = n = n_i \\ \Rightarrow pn = n_i^2 \end{array}}$$

## Example 3.1

Calculate the value of $n_i$ for silicon at room temperature ($T \simeq 300$ K).

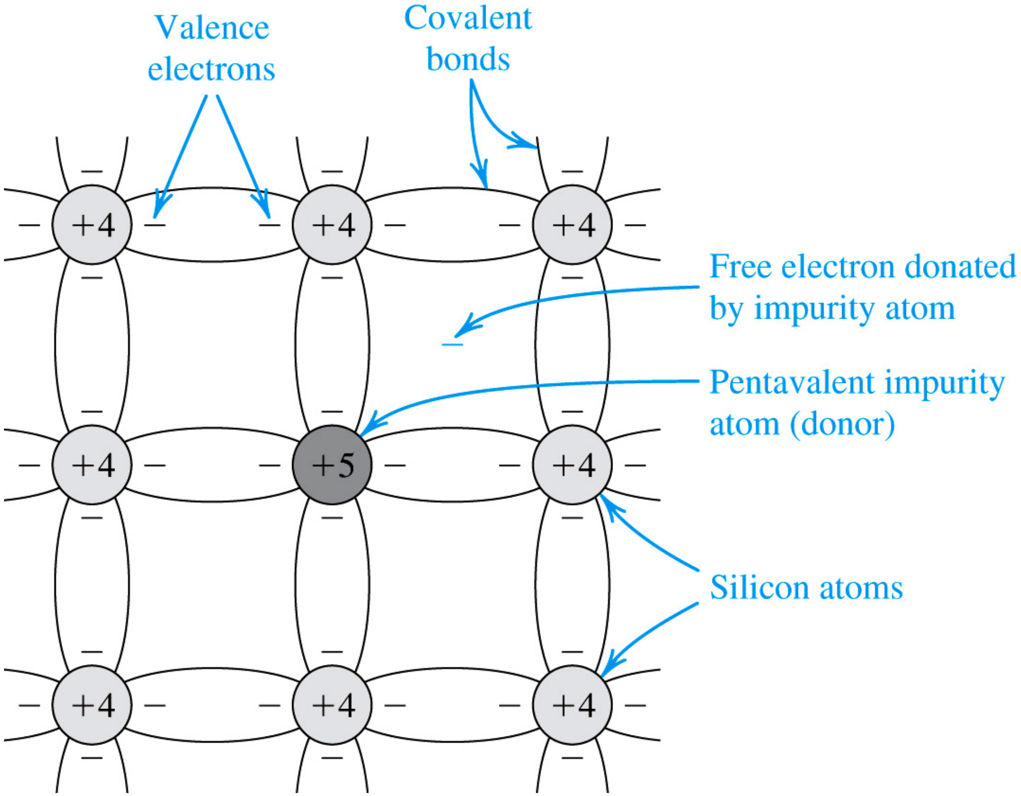
**Solution**

Substituting the values given above in Eq. (3.1) provides

$$\begin{aligned} n_i &= 7.3 \times 10^{15}(300)^{3/2}e^{-1.12/(2 \times 8.62 \times 10^{-5} \times 300)} \\ &= 1.5 \times 10^{10}\text{carriers/cm}^3 \end{aligned}$$

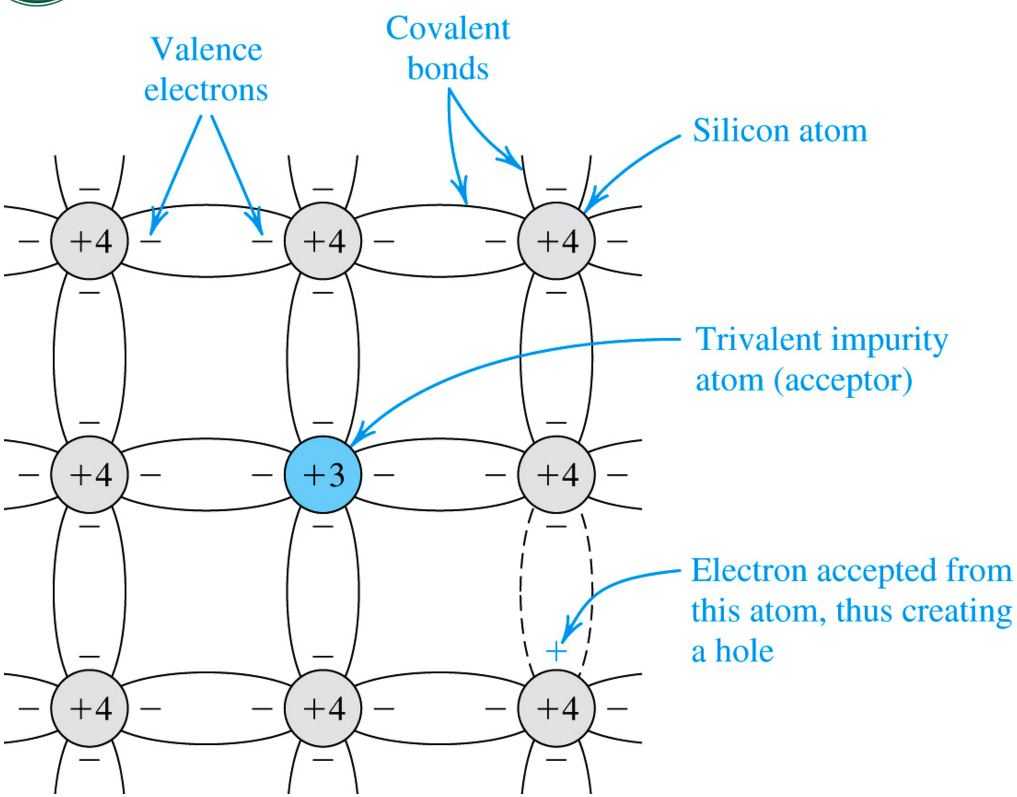
Although this number seems large, to place it into context note that silicon has $5 \times 10^{22}$ atoms/cm$^3$. Thus at room temperature only one in about $5 \times 10^{12}$ atoms is ionized and contributing a free electron and a hole!

# Doped Semiconductors




- Semiconductors can be **doped** with different materials to add more electrons or holes
- **Donor** atoms have 5 electrons in their outermost shell, so they can be used to “donate” an extra electron
- Since the extra electron is not part of a covalent bond, very little energy is needed to free it so it can conduct current
- The result of adding donor atoms is **n-type** silicon
- Phosphorus (P) and Arsenic (As) are often used as donors

# Doped Semiconductors




- **Acceptor** atoms have 3 electrons in their outermost shell, so they can be added to "accept" an electron, which creates a hole
- Very little energy is needed to free this extra hole so that it can conduct current
- Both holes & electrons leave **immobile ions** (atoms that can't move, and have + or – charge)

- The result of adding acceptor atoms is **p-type** silicon
- Boron (B) is often used as an acceptor atom

## Example 3.2

Consider an $n$-type silicon for which the dopant concentration $N_D = 10^{17}/\text{cm}^3$. Find the electron and hole concentrations at $T = 300$ K.

### Solution

The concentration of the majority electrons is

$$n_n \simeq N_D = 10^{17}/\text{cm}^3$$

The concentration of the minority holes is

$$p_n \simeq \frac{n_i^2}{N_D}$$

*Note the use of :*

$$\boxed{pn = n_i^2}$$

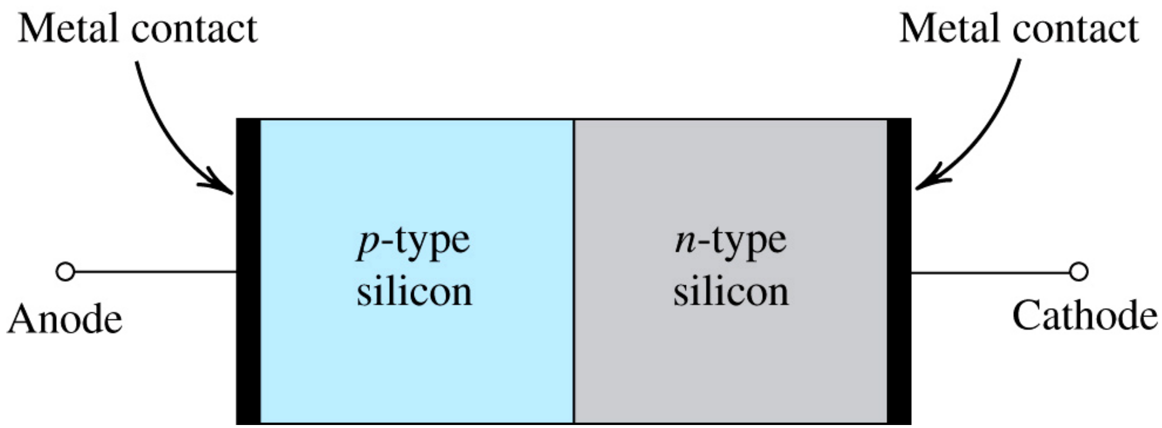
In Example 3.1 we found that at $T = 300$ K, $n_i = 1.5 \times 10^{10}/\text{cm}^3$. Thus,

$$p_n = \frac{(1.5 \times 10^{10})^2}{10^{17}}$$

$$= 2.25 \times 10^3/\text{cm}^3$$

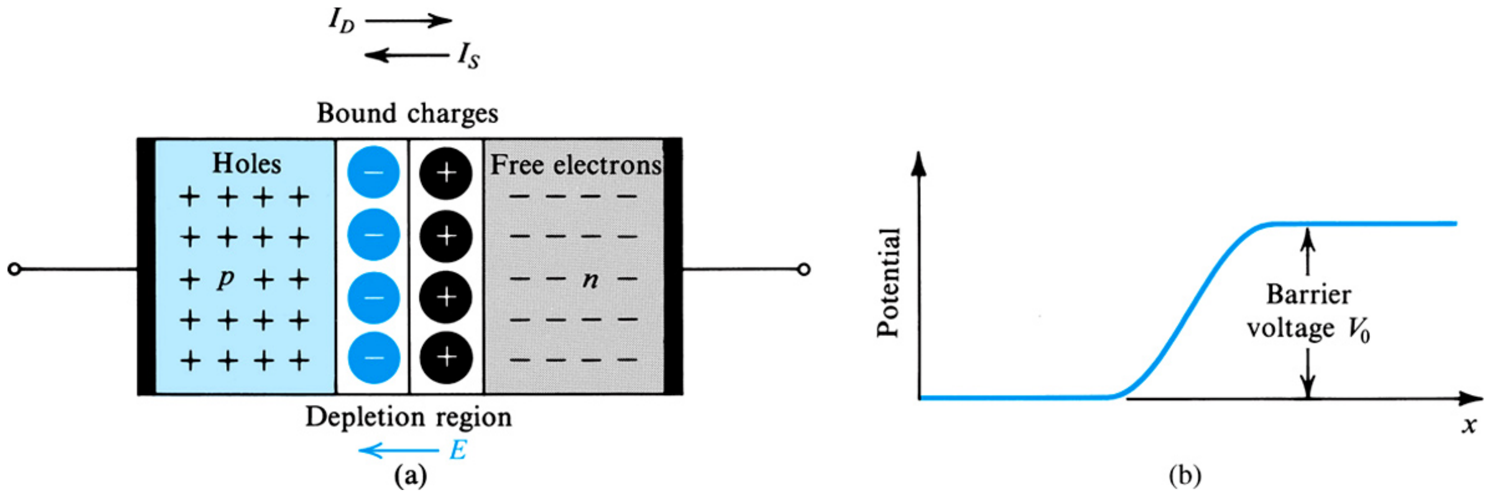
Observe that $n_n \gg n_i$ and that $n_n$ is vastly higher than $p_n$.

# PN Junction Structure (simplified)




- When p-type silicon is brought into contact with n-type silicon, a **PN Junction** is formed
- This is also often referred to as a **semiconductor diode**
  - If a positive voltage is applied to the P-type side with respect to the N-type side, the diode turns on and current flows
  - If a negative voltage is applied to the P-type side with respect to the N-type side, the diode remains off and ~ zero current flows
  - The P side is called the **anode**, and the N side is the **cathode**

# PN Junction Depletion Region




- When p-type Si is brought into contact with n-type Si, holes diffuse from the P side to the N side, and electrons diffuse from the N side to the P side. This causes :

1. A **depletion region** to be formed around the junction (i.e., the area around the junction is depleted of free holes and electrons)
2. The donors and acceptors near the junction are ionized, leaving behind **uncovered bound charge** (+ on the N side, - on the P side)
3. This separation of charge creates an electric field which opposes further diffusion, and a **barrier voltage** that must be overcome

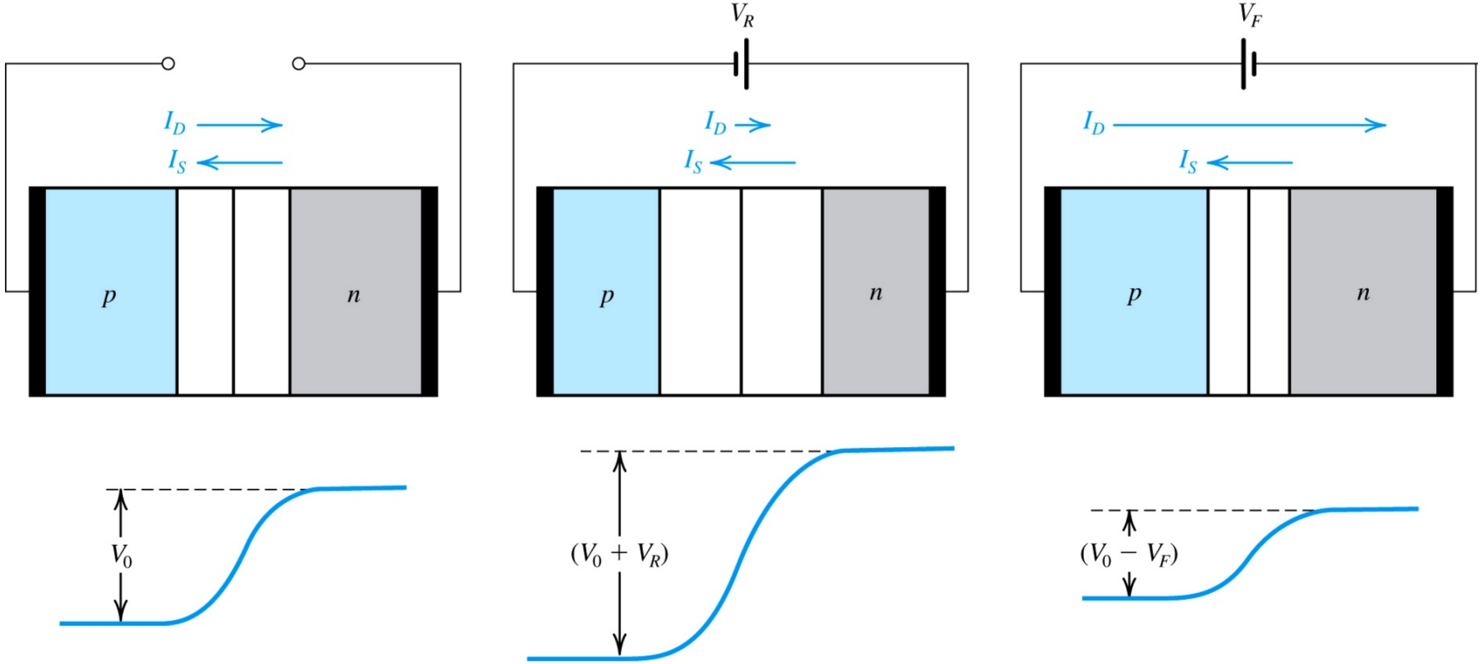
# PN Junction Built-in Voltage

- The barrier voltage for the PN junction is more typically called the junction's **built-in voltage**.
- In equilibrium (no applied voltage), the built-in voltage can be calculated from the PN doping concentrations
- Also notice that :
  - Higher $N_A$, $N_D$ → Higher $V_0$
  - $V_0$ changes slowly with doping, due to the log function
  - $V_0$ varies with absolute temperature in °K due to both $V_T$ and $n_i$

$$\boxed{V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) = \text{"}the\ built-in\ voltage\text{"}}$$

$$V_T = \frac{kT}{q} \approx 26mV\ at\ 300°K$$

# PN junction with Bias Voltage applied




(a) Open-circuit (Equilibrium)

(b) Reverse Bias

(c) Forward Bias

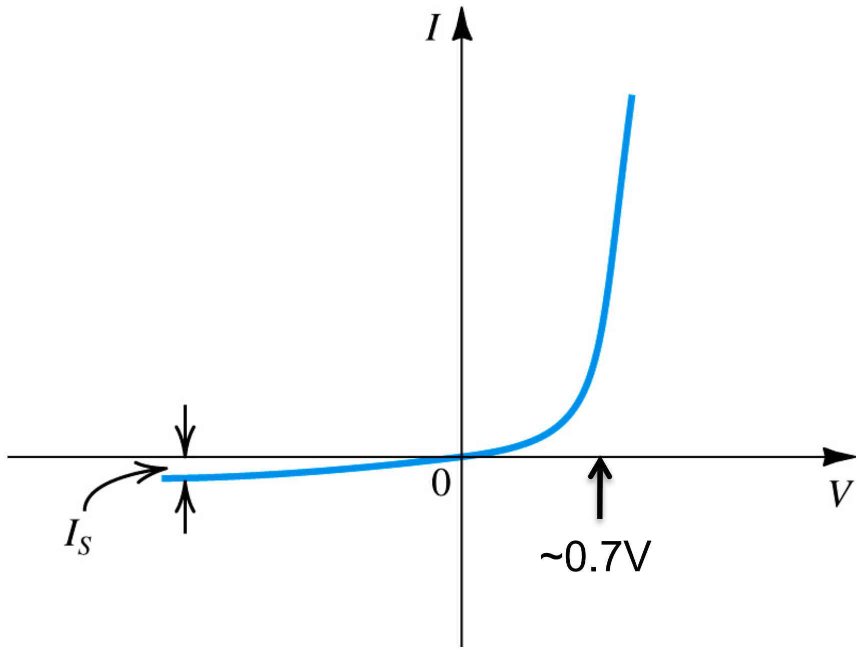
- A PN junction in **reverse bias** (V on P-side < V on N-side)

→ Depletion region width & potential barrier both **increase**

- A PN junction in **forward bias** (V on P-side > V on N-side)

→ Depletion region width & potential barrier both **decrease**

# PN Junction I-V Characteristic



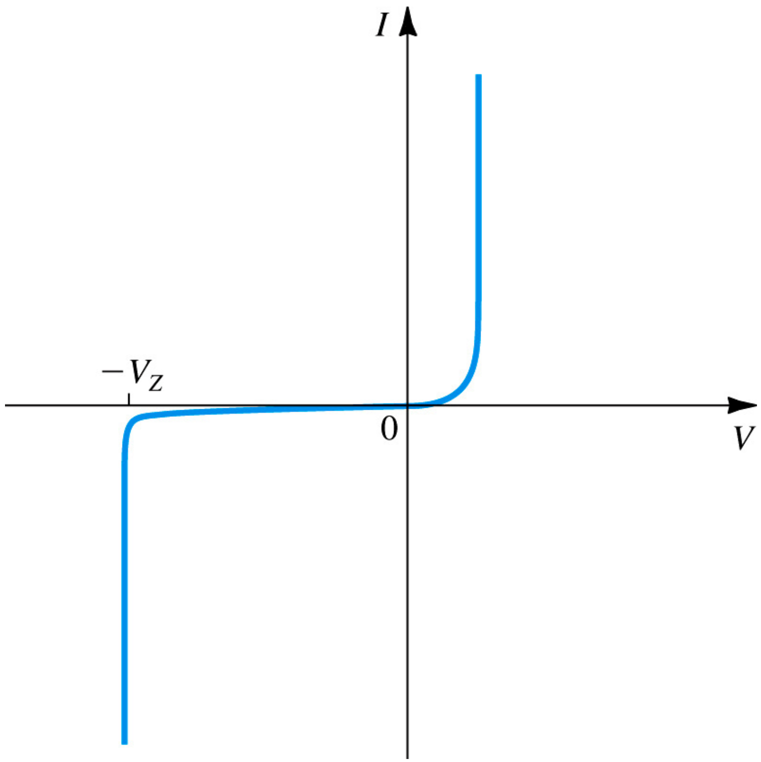

$$\boxed{I = I_S\left(e^{V/V_T} - 1\right) \quad where:\ V_T = \frac{kT}{q}}$$

$$and:\ \boxed{I_S = q A n_i^2\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right)}$$

- In forward bias, the current grows exponentially as the voltage applied across the PN junction increases
- In reverse bias, the current is a very small value, $I_S$, the **reverse saturation current**
  - Typical value for $I_S \sim 10^{-14}$ A
- $L_p$, $L_n$ = **diffusion lengths** for holes and electrons
  - Characterizes how far a carrier travels before it recombines

$$concentraion\ drops \propto e^{-x/L}$$

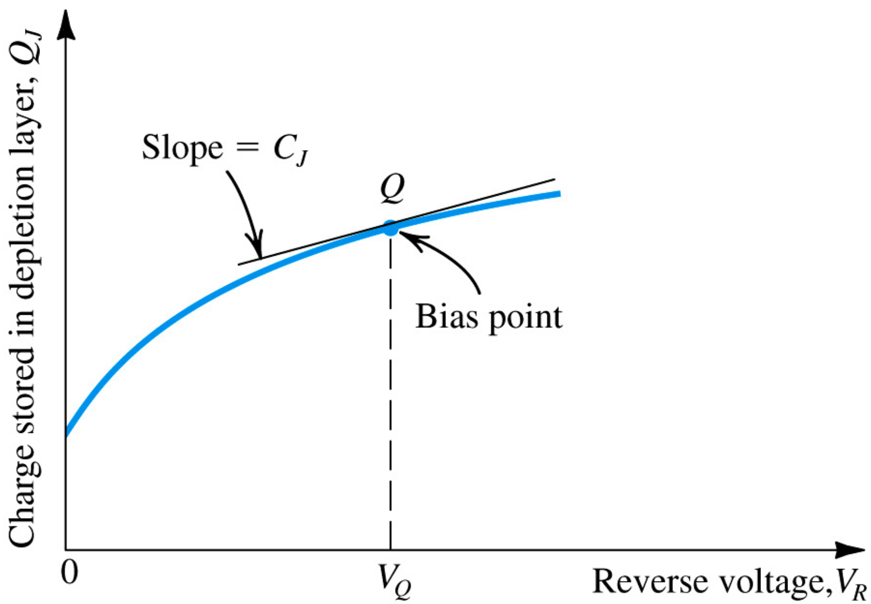
# Reverse Breakdown




**$V_Z$ = the reverse breakdown voltage** for the PN junction

- If the reverse bias voltage across a PN junction gets too high, the junction **breaks down** and the current increases rapidly
  - I increases rapidly while V stays ~ constant at $V_Z$
  - Caused by high E-fields
- Two different effects can cause this breakdown :
  - **Zener** effect (for $V_Z < 5V$)
  - **Avalanche** effect ($V_Z > 7V$)
- $V_Z$ drops as doping levels are increased

# Depletion Region Capacitance




$$C_J = \frac{dQ_j}{dV_R} \quad at\ a\ bias = V_Q$$

$$\Rightarrow \boxed{C_J = \frac{C_{j0}}{\left(1 + V_R / V_0\right)^m}}$$

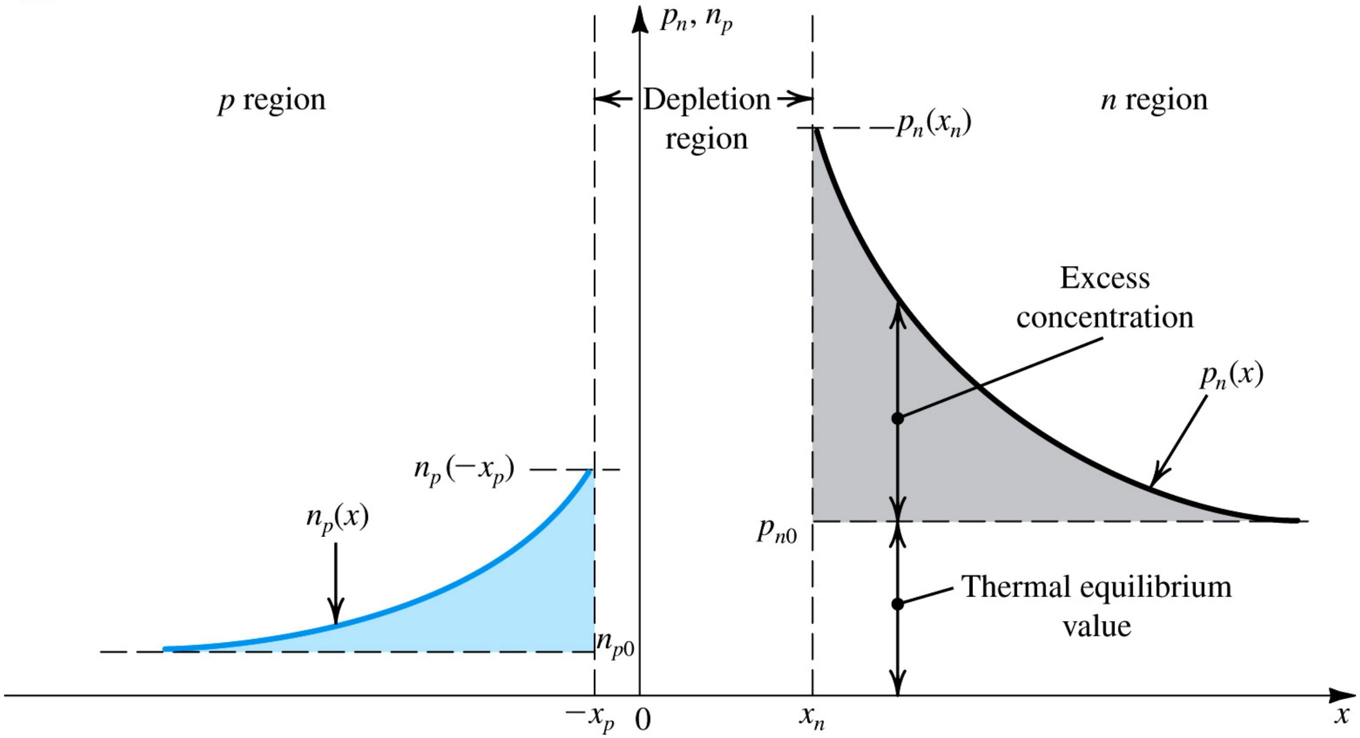
$$where:\ C_{j0} = C_J\ at\ V_R = 0$$

- Since the charge stored in the depletion region varies with the bias voltage, this looks like a capacitance!
- The **depletion or junction capacitance** is nonlinear, and drops as the reverse bias voltage increases
- The **grading coefficient** m depends on how the PN junction is made :

  m = 1/2 for abrupt **step** junctions

  m = 1/3 for **linear** junctions

# Diffusion Capacitance




$$C_D = \frac{dQ}{dV} \Rightarrow$$

$$\boxed{C_D = \left(\frac{\tau_T}{V_T}\right) I}$$

$\tau_T$ = mean time needed for carriers to recombine

- Since the excess carrier concentration in a forward biased PN junction varies with the applied bias, this variation in the stored charge also looks like a capacitance!
- This is called the **diffusion capacitance**, and depends on the bias current, $V_T = kT/q$ , and the **mean transit time**, $\tau_T$

# Summary of Key Concepts

- Semiconductors are materials whose resistance can be varied over a wide range by adding controlled amounts of impurity atoms, called doping. Silicon is the most widely used semiconductor today.
- PN junctions are formed when a P-type semiconductor comes into contact with an N-type semiconductor
  - A depletion region forms due to diffusion, which creates a built-in voltage that opposes the further diffusion of carriers
  - When a PN junction is forward biased, current increases exponentially with V. In reverse bias, only a tiny $I_S$ current flows
  - At high reverse bias a junction breaks down and high I can flow
  - PN junctions have both depletion and diffusion capacitances