California State University, Sacramento
The College of Engineering and Computer Science

CPE 166 Advanced Logic Design

Midterm 1 – Part 2

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You need to write Verilog design for the following two questions. Testbench is not required for each question.

Part2.1 [10 points]. Implement the clock division hardware design in Verilog.
The input clock is clk and the output clock is clk2. The frequency of clk2 is equal to the frequency of clk divided by 50.

```
module   clkdiv50 ( clk,  clk2);
input clk ;
output  clk2;
reg [2:0] cnt ;
initial  cnt = 0;
always @ (posedge  clk)
begin
    if ( cnt == 49)
    begin
        cnt <= 0
        clk 2 <= 1
    end
    else if (cnt < 24)
    begin
        cnt <= cnt + 1;
        clk2 <= 1;
    end
    else
    begin
        cnt <= cnt + 1;
        clkout <= 0;
    end
end
end module
```

Part2.2 [26 points] Design a single Mealy finite state machine to recognize sequence 100 or sequence 1000.

module fsm (reset, clk, a, y);
input reset, clk;
input a; // "a" represents the incoming data
output y; // "y" is a mealy output for detecting the correct sequence.

```
reg y;
reg [1:0] cs, ns;
parameter A=2'b00, B=2'b01, C=2'b10;

always @(posedge clk or posedge reset)
begin
   if (reset) cs <= A;
   else       cs <= ns;
end

always @(cs or a)
begin
   case (cs)
    A: if (a) ns = B;
       else   ns = A;
    B: if (a) ns = B;
       else   ns = C;
    C: if (a) ns = C;
       else   ns = A;
    default: ns = A;
   endcase
end

always @(cs)
begin
   case (cs)
      A: y = 1;
      B: y = 0;
      C: y = 0;
     default: y=0;
   endcase
end
endmodule
```