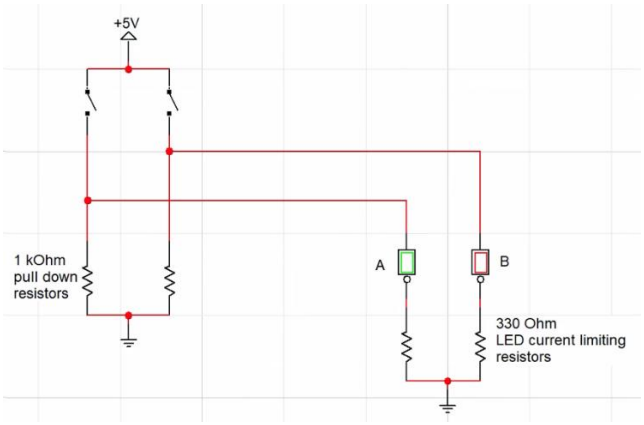
Algador, Vigomar Kim
CpE-64 – 05

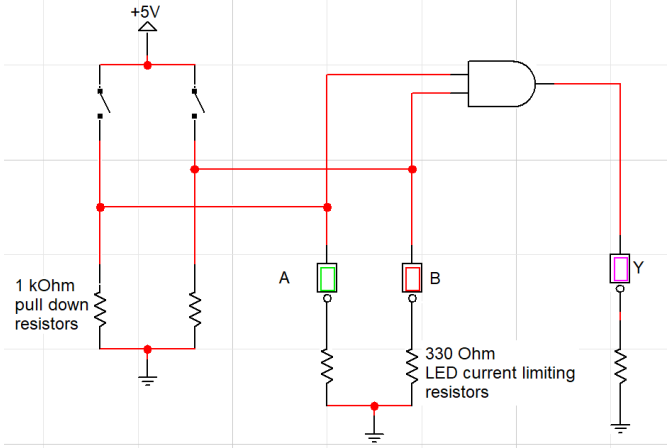
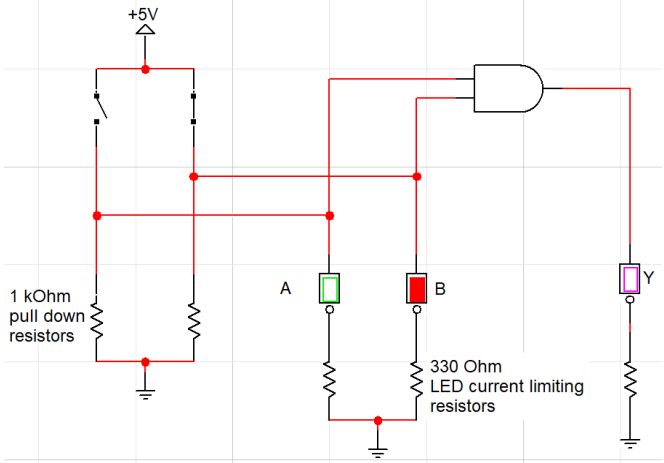
Laboratory 3: Logic Gates

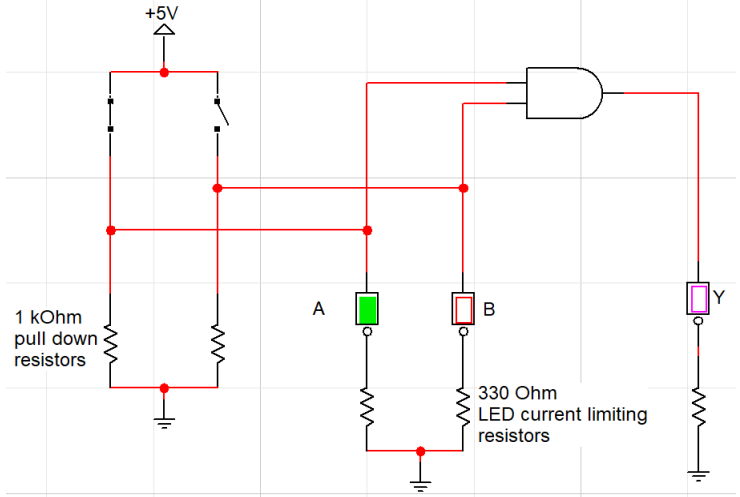
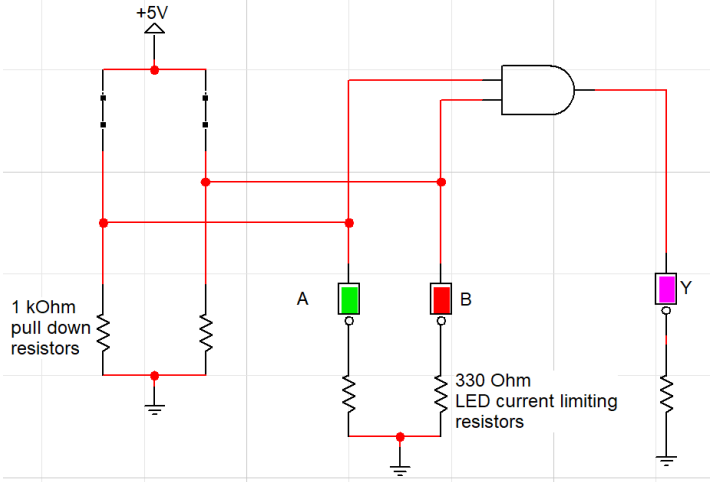
Part I: Simulated Template Circuit



Part II: AND gate

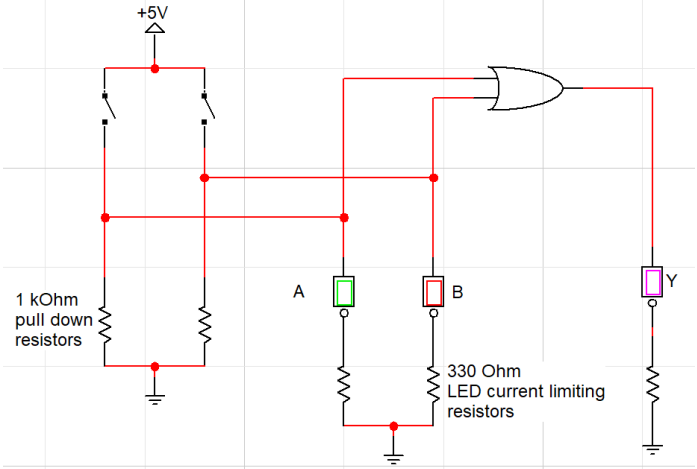
Truth Table

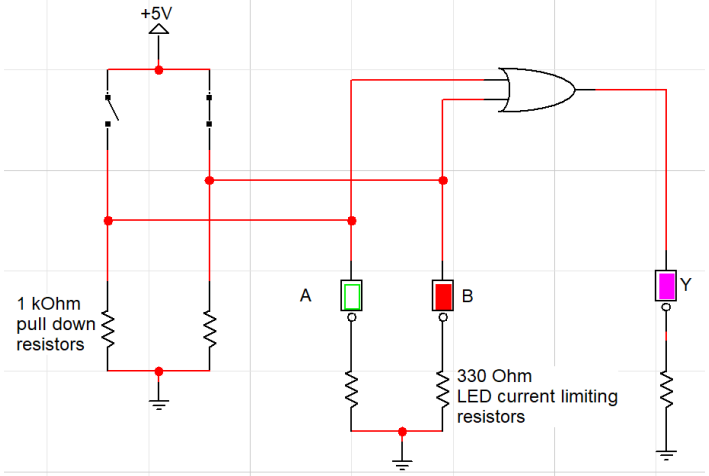
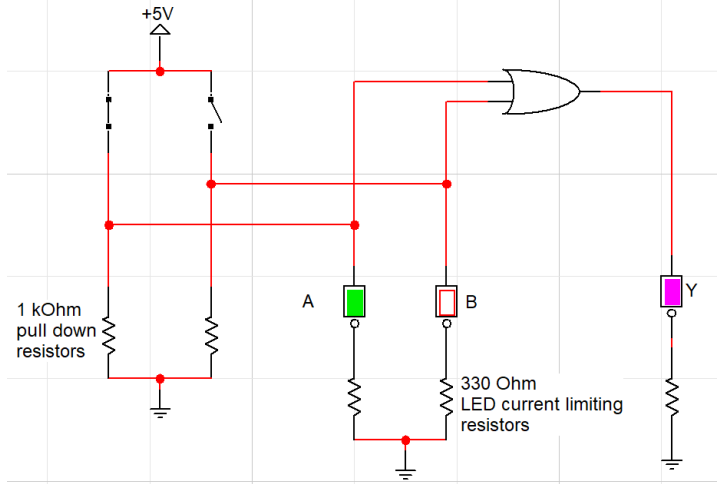
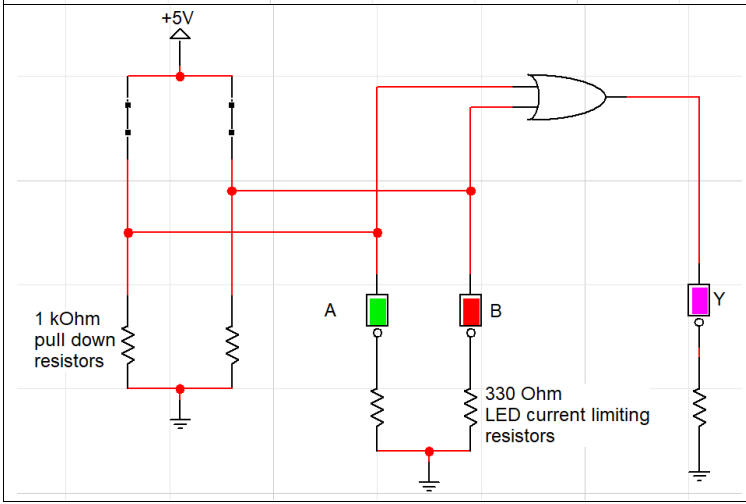
Simulation	A	B	Y
	0	0	0
	0	1	0

	1	0	0
	1	1	1

Part III: OR gate

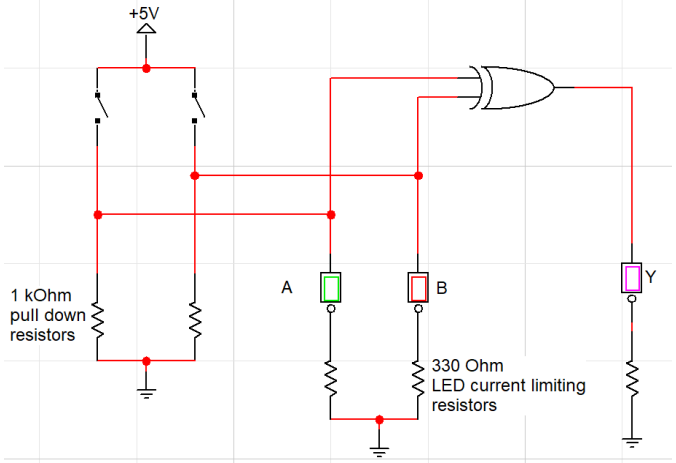
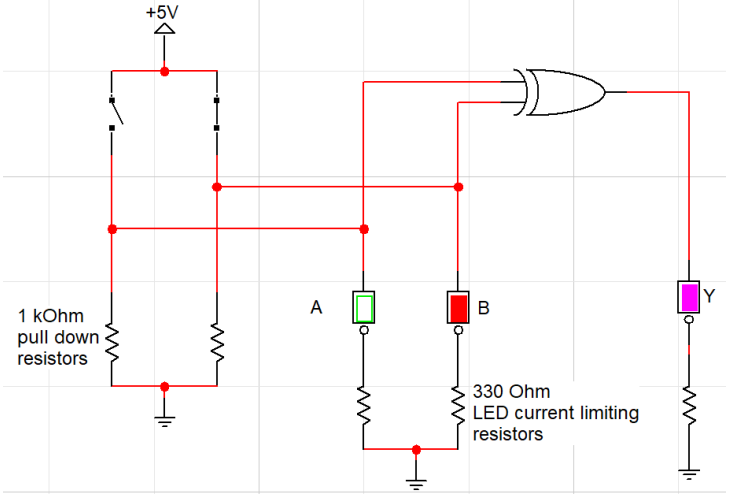
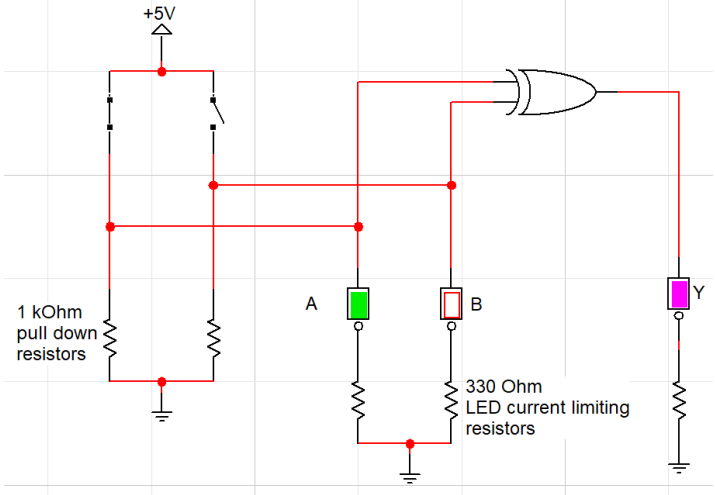
Truth Table

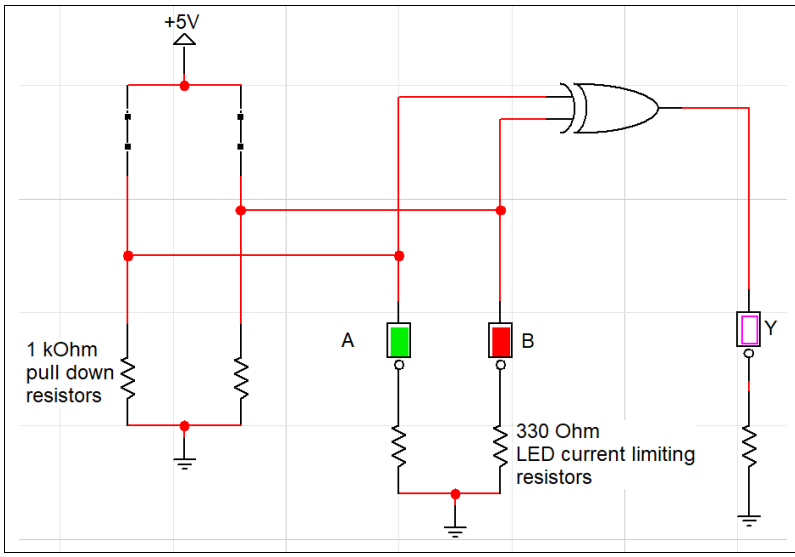
Simulation	A	B	Y
	0	0	0

 +5V 1 kOhm pull down resistors A B Y 330 Ohm LED current limiting resistors	0	1	1
 +5V 1 kOhm pull down resistors A B Y 330 Ohm LED current limiting resistors	1	0	1
 +5V 1 kOhm pull down resistors A B Y 330 Ohm LED current limiting resistors	1	1	1

Part IV: XOR gate

Truth Table

Simulation	A	B	Y
	0	0	0
	0	1	1
	1	0	1

 +5V 1 kOhm pull down resistors A B Y 330 Ohm LED current limiting resistors	1	1	0