Syllabus for Fall 2022

Course: CPE166 Advanced Logic Design
Lectures: MWF 9:00 - 9:50 a.m.
Instructor: Prof. Pang
Email: jpang@csus.edu
Office Hours: Monday 10:00 a.m. - 11:50 a.m., Monday 2:50 p.m. – 4:00 p.m.

Course Description:

Present the advanced topics in digital logic design, including finite state machine designs, use of hardware description languages as a practical means to implement hybrid sequential and combinational designs, digital logic simulation, rapid prototyping techniques, metastability, hazards, races, testability, boundary scan, scan chains. VHDL and Verilog Hardware Description Languages are studied and used. Commercial Electronic Design Automation (EDA) tools and lab equipments are used to implement and test lab projects containing a hierarchy of modules into Field Programmable Gate Arrays (FPGAs).

Prerequisite:

□ Completing CpE64, an introduction to logic design course
□ Completing Engr 17, a basic circuit theory course

Course Objectives:

1. Provide in-depth design experiences that require students to:
    a. develop good time management practices on their part
    b. develop problem solving skills
    c. meet design requirements and keep design within a resource limitation
    d. think creatively on complex assignments
    e. produce clear, concise written reports
    f. learn how to associate with others in the course, yet do individual work
2. Cover wide-ranging topics in logic design at an advanced technical level
3. Students become proficient in the use of high-level design tools

Textbook:

Register Transfer Level (RTL) Hardware Design Using VHDL,
Author: Chu
Publisher: John Wiley & Sons Inc.,
Copyright: 2006
ISBN: 9780471720928

Reference:

Design Through Verilog HDL
Author: Padmanabhan
Publisher: John Wiley & Sons, Inc.
Copyright: 2004
ISBN: 978047144148

Grading:

Quiz 2%
Labs 38%
Midterm 1 20%
Midterm 2 20%
Final (Comprehensive) 20%

A: ≥ 92% A-: ≥ 90%
B+: ≥ 85% B : ≥ 82% B-: ≥ 80%
C+: ≥ 75% C: ≥ 72% C- : ≥ 70%
D+: ≥ 65% D: ≥ 62% D-: ≥ 60%
F : <60 %

Class Schedule

Weeks	Dates	Topics	Reading Assignments
Week 1	Aug. 29 – Sep. 2	Introduction to the Course, How to be Successful in this Course, Verilog Basics	Padm. Chap. 1, Chap. 2, Chap. 3, Chap. 4
Week 2	Sep. 5 – Sep. 9	Hierarchical Design	Padm. Chap. 3, Chap 4, Chap. 6
	September 5	Labor Day (Holiday Campus Closed), Monday	
Week 3	September 12 – September 16	Verilog Behavior Design, Queues, Finite State Machine,	Padm. Chap 7 (p159-p201), Chap. 12
Week 4	September 19 – September 23	Verilog Timing Control, More on Verilog	Padm. Chap. 5, Chap 7 (p201-p216), Handout Chap 8 (p230-P268)
Week 5	September 26 – September 30	**Midterm1 Review,** VHDL syntax, entities, and architectures	Chu Chap 1, 2, and 3
Week 6	October 3 – October 7	Midterm 1, More on VHDL	Chu Chap 9, Handout
Week 7	October 10 – October 14	ASM Chart	Chu Chap 4, Chap 10, Handout
Week 8	October 17 – October 21	Even-Odd Parity, Hamming Code, Cyclic Redundancy Check	Chu Chap 7, Handout
Week 9	October 24 – October 28	Memory, Datapath Control	Chu Chap5, Chap 8, Handout
Week 10	October 31 – November 4	Metastability, **Midterm 2 Review**	Chu Chap 6, Chap 16, Handout

Week 11	November 7 – November 11	Hazards, Midterm 2	Handout
	November 11	Veteran's Day (Holiday, Campus Closed), Friday	
Week 12	November 14 – November 18	Video Design	Handout
Week 13	November 21 – November 25	FPGA Architecture	Handout
	November 24 – November 25	Thanksgiving Holiday (Holiday, Campus Closed), Thursday & Friday	
Week 14	November 28 – December 2	JTAG, boundary scan, scanchains	Handout
Week 15	December 5 – December 9	Transmission line effect, **Final Exam Review**	Handout
Week 16	December 12 – December 16	Final Exam	

Course Policy:

1. You must pass both exam session (mid1+mid2+final) and also lab session (quiz + labs) in order to get better grade than "F" in this course. Failure in either exam session or the lab session will result in "F" grade of this course.
2. You are responsible for all the materials presented and announcements made in class.
3. You cannot do project assignment in just 2 hour 40 minutes per week during the lab session.
   It may take two or three times longer.You are welcome to work on your project whenever there are lab computers available online all week including weekends.
4. Every student must submit an independent solution for each lab assignment. However, you may discuss assignments with your classmates but you must submit a separate and independent solution.
5. Lab 5 report will be due on Sunday of Week 15. No later report submission will be accepted.

For Policy on Academic Integrity refer to
https://www.csus.edu/umanual/student/stu-100.htm

This syllabus is tentative and it is subject to change at the instructor's discretion