CPE166 Midterm1 - Part 2 - 2nd At

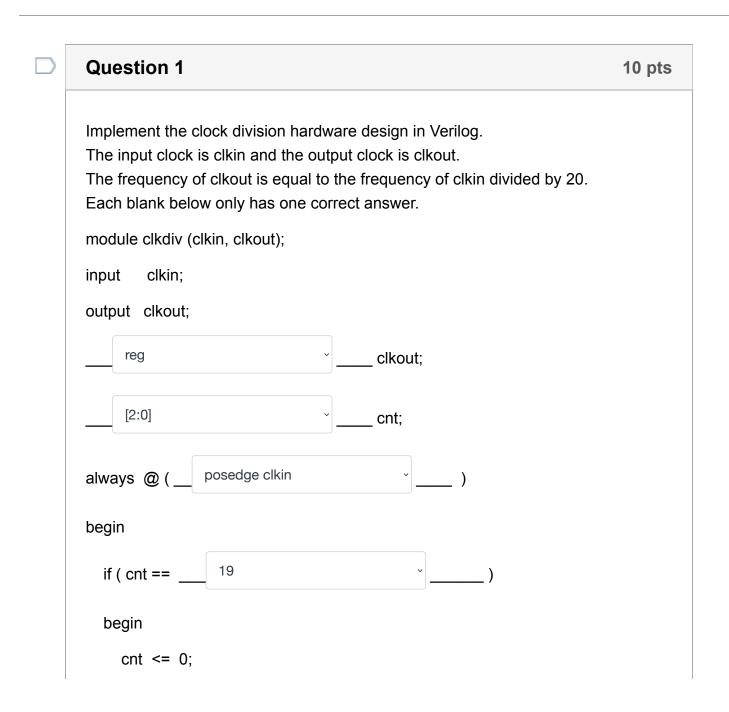
Started: Oct 28 at 9:36am

Quiz Instructions

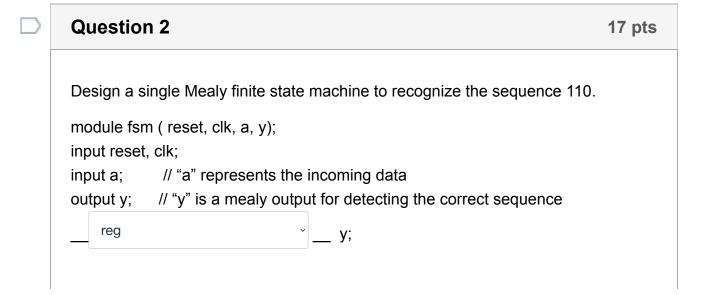
Students can take the "CPE166 Midterm1 - Part 2 - 2nd" test this Friday 10/28/2022 from 9:00am to 9:50am with a maximum score of 27.

If your previous part 2 test score is above 27, you don't have to take this test on this Friday. You can study VHDL lecture notes and work on the lab project assignments.

The highest score for "CPE166 Midterm 1 - Part 2" and "CPE166 Midterm1 - Part 2 - 2nd" will be considered as the Part 2 score.



```
clkout <= 1;
 end
      else if
                                          (cnt < 9)
begin
               cnt + 1
   cnt <=
  clkout <= 1;
 end
else
 begin
               cnt + 1
   cnt <=
   clkout <=
 end
    end
    endmodule
```



```
[1:0]
                                   __ cs, ns; //cs: current state, ns: next state
parameter s0 = 2'b00, s1=2'b01, s2=2'b10;
                 posedge clk or posedge reset
always @ (
begin
              cs <= s0
if(reset)_
              cs <= ns
else
end
               cs or a
always@(_
begin
case@(cs)
                    s1
s0: if(a) ns = _
     else ns =
                    s0
                    s2
 s1: if(a) ns = ___
                    s0
     else ns = __
 s2: if(a) ns =__
                     s2
     else ns = _
                    s0
  default : ns = s0;
 endcase
end
always @(
                  cs or a
begin
case(cs)
                 0
s0:
                 0
s1:
```

s2: if(a) $y = ____0$ ____; else $y = ____1$ ____; default: y = 0; endcase end endmodule

Saving...

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