CPE166 Lab 3 Part 2
By: Prof. Pang

Lab 3

Part 2: Pseudorandom Number Generator

A linear feedback shift register (LFSR) is a shift register whose input bit is the output of a linear logic function of two or more of its previous states. The LFSR circuit can be used as pseudorandom number generator. This project is a design of a 5-stage LFSR circuit shown below.

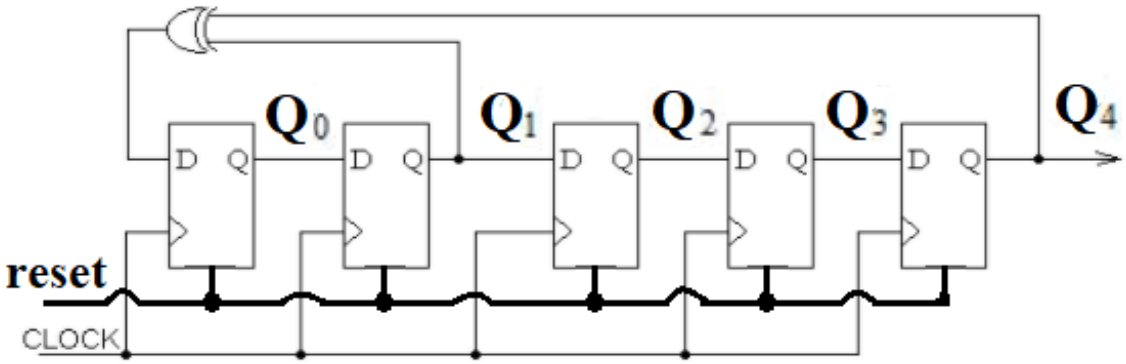

Figure 1. 5-stage LFSR diagram

Demo Requirement

Make sure that this LFSR design uses a non-zero value as the initial seed value. You need to demonstrate the final simulation waveform of this design to your lab instructor and show that the value of Q (4 drops to 0) repeats every 31 clock cycles.

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Lab Procedure

Step 1. LFSR Design Review

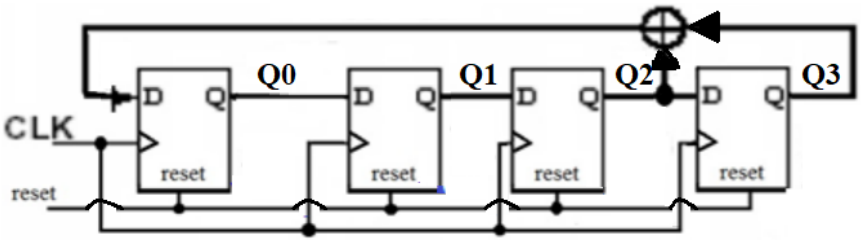


Figure 2. 4-stage LFSR diagram

Review the above circuit you have learnt in class with the VHDL design below.

```
Library ieee;
Use ieee.std_logic_1164.all;
Entity lfsr is
        Port (  reset, clk:   in std_logic;
                Q:  out std_logic_vector (3 downto 0)  );
End lfsr;
Architecture beh of lfsr is
Signal   m:  std_logic_vector (3 downto 0);
Begin
              Process(reset, clk)
              Begin
                  If ( reset = '1')  then
                        m <=  ( 0=> '1', others =>'0');                --- value of “0001”
                  elsif (rising_edge(clk) ) then
                        m(3 downto 1) <= m(2 downto 0);
                         m(0) <= m(2) xor m(3);
                  end if;
             end process;
            Q <= m;
```

```
end beh;
```

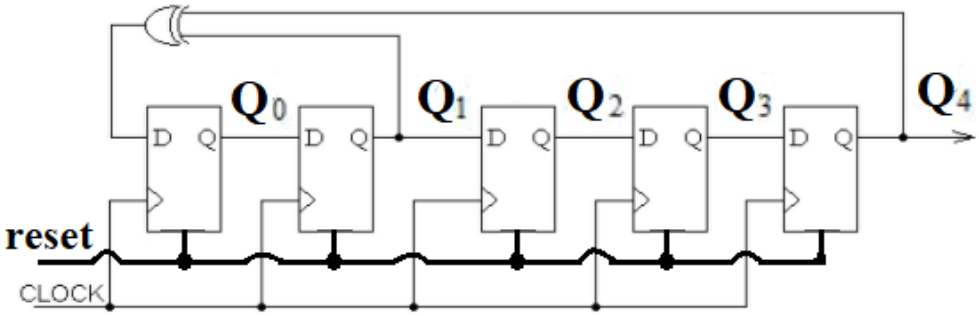
Step 2. LFSR Testbench Design Review for Fig. 2 Circuit

```
Library ieee;
Use ieee.std_logic_1164.all;
Entity lfsr_tb is
End lfsr_tb;
Architecture tb of lfsr_tb is
signal clk, reset: std_logic;
signal Q:   std_logic_vector (3 downto 0);
component lfsr
      Port (  reset, clk:   in std_logic;
            Q:  out std_logic_vector (3 downto 0)  );
End component;
Begin
      uut:  lfsr port map(reset, clk, Q);
      Process
      Begin
          Clk <= '0';
          Wait for 5 ns;
         Clk <= '1';
         Wait for 5 ns;
      End process;

    Process
    Begin
       Reset <= '1';
       Wait for 2 ns;
```

```
        Reset <= '0';
        Wait for 200 ns;
        Wait;
    End process;
End tb;
```

Step 3. LFSR Design and Testbnech Simulation of Fig. 1 Circuit



Steps 1 and 2 are for optional exercise purposes.

Step 3 is a required task for this laboratory experiment.

You need to write a VHDL design and testbench for this 5-stage LFSR, and run simulations to verify that the value of Q (4 downto 0) repeats every 31 clock cycles.