ECE 2140 Design of Logic Systems I

Lab 5 Report

Graham Feldman

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1 Purpose

The purpose of this lab was to design a system to operate one of the Basys Board's 7-segment displays to show hexadecimal digit from 0 to 15. The digits from 0 to 9 should be the base 10 representations and the digits. The digits from 10 to 15 should be letter equivalents (A for 10, b for 11, C for 12, d for 13, E for 14, F for 15). All the digits should be presented as vertical mirror images of the original (Figure 1).

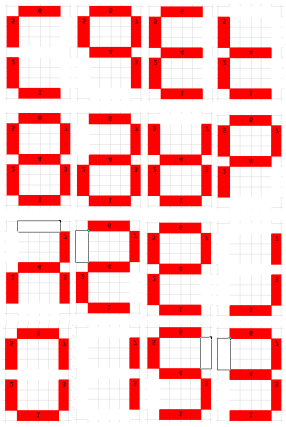

Figure 1 – 7-Segment Display Mirror Image [3]

Switch SW4, SW5, SW6 and SW7 on the Basys board represent the two hexadecimal binary input from most to least important digit [1].

2 Equipment

- Digelent Basys Board with USB
- Xilinx Design Suite 13.2
  - Software to program the Basys Board
- Digilent Adept Software, Version 2.3.0
  - Software to upload design

3 Design

The initial part of the design was to identify the function of minterms required for each of the seven segments of the display (referred to as a to g). In other word what numbers

require each specific segment to be illuminated. Figures 2 to 8 show the functions, the Karnaugh maps, and the logic gates that were determined necessary.

$$f_a(a,b,c,d) = \sum m\,(0,2,3,5,6,8,9,11,12,13,14)$$

$abcd$	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	1	1	0	1
10	1	1	1	0

$$f = a\bar{c} + \bar{a}c\bar{d} + \overline{\bar{a}\bar{b}}de + bc\bar{d} + abce + \overline{\bar{b}c\bar{d}} + b\bar{c}d + \bar{b}cd$$

Figure 2 – Karnaugh Map and Suitable Logic Gates For *a* segment

$$f_b(a,b,c,d) = \sum m\,(0,1,3,4,5,6,7,8,9,10,11,13)$$

$abcd$	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	0	1	0	0
10	1	1	1	1

$$f = \bar{a}b + a\bar{b} + \bar{c}d + \bar{a}d + \overline{\bar{a}c}$$

Figure 3 – Karnaugh Map and Suitable Logic Gates For *b* segment

$$f_c(a,b,c,d) = \sum m\,(0,1,2,3,4,7,8,9,10,13)$$

$abcd$	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	0	1	0	0
10	1	1	0	1

$$f = \overline{\bar{a}\bar{b}} + \overline{\bar{b}\bar{d}} + a\bar{c}d + \bar{a}cd + \overline{\bar{a}cd}$$

Figure 4 – Karnaugh Map and Suitable Logic Gates For *c* segment

$$f_d(a,b,c,d) = \sum m\,(0,2,3,5,6,7,8,9,10,12,14,15)$$

$abcd$	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	1	0	1	1
10	1	1	0	1

$$f = c\bar{d} + bc + \bar{a}c + \overline{bd} + \bar{a}bd + a\overline{cd} + a\overline{bc}$$

Figure 5 – Karnaugh Map and Suitable Logic Gates For *d* segment

$$f_e(a,b,c,d) = \sum m\,(0,4,5,6,8,9,10,11,12,14,15)$$

$abcd$	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	1	0	1	1
10	1	1	1	1

$$f = a\bar{b} + ac + \overline{cd} + \bar{a}b\bar{c} + bc\bar{d}$$

Figure 6 – Karnaugh Map and Suitable Logic Gates For *e* segment

$$f_f(a,b,c,d) = \sum m\,(0,2,6,8,10,11,12,13,14,15)$$

$abcd$	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	1	1	1	1
10	1	0	1	1

$$f = ab + ac + c\bar{d} + \overline{bd}$$

Figure 7 – Karnaugh Map and Suitable Logic Gates For *f* segment

$$f_g(a,b,c,d) = \sum m\,(2,3,4,5,6,8,9,10,11,13,14,15)$$

$abcd$	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	0	1	1	1
10	1	1	1	1

$$f = a\bar{b} + c\bar{d} + ad + \bar{a}b\bar{c} + \overline{ab}c$$

Figure 8 – Karnaugh Map and Suitable Logic Gates For *g* segment

Once the logic was determined, Xilinx Design Suite software was used to program the logic gates on the Basys Board. Four inputs were assigned the variables *a*, *b*, *c*, *and d*, corresponding to the digit represented. Seven output were assigned the variables *fa, fb, fc, fd, fe, ff,* and *fg,* corresponding to the segment of the display they represent (Figure 9).. The logic derived in Figure 1 was added as syntax that could be understood by the software (Figure 10). Because the 7-segment displays on the Basys Board are common anode, all of the logic functions determined in figures 2 to 8 were complimented.

Port	Pin	Device	Type
a	P18	Switch SW4	input
b	P12	Switch SW5	input
c	P10	Switch SW6	Input
d	P6	Switch SW7	input
AN0	P34	Disable 7-Segment	input
AN1	P33	Disable 7-Segment	input
AN2	P32	Disable 7-Segment	input
fa	P25	a segment	output
fb	P16	b segment	output
fc	P23	c segment	output
fd	P21	d segment	output
fe	P20	e segment	output
ff	P17	f segment	output
fg	P83	g segment	output

Figure 9 – Pin Assignment for Input Variables [2]

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:           The George Washington University
// Engineer:          Graham Feldman
//
// Create Date:       16:26:01 02/26/2016
// Design Name:       Lab5
// Module Name:       Lab5
// Project Name:      Da Vinci upside down mirror wirtinfg
// Target Devices:    Xilinx xc3s250e-4tq144
// Tool versions:     ISE Project Navigator 13.2
// Description:       This design displays the mirror upside down hexadecimal
//                    digits from a four bit binary input using Karnaugh maps and
//                    logic gates to illuminate corresponding segments of a seven
//                    segment display.
//
// Dependencies:      None
//
```

```
// Revision:                    2
// Revision                     0.03 - File Created
// Additional Comments:         The design will make use of the 7-segment display AN3.
//
//////////////////////////////////////////////////////////////////////////////////
module Lab5 (
        input a,
        input b,
        input c,
        input d,
        output fa,
        output fb,
        output fc,
        output fd,
        output fe,
        output ff,
        output fg,
        output AN0,
        output AN1,
        output AN2
         );

    assign fa = ~((a & ~c) | (~a & c & ~d) | (b & c & ~d) | (~b & ~c & ~d) | (b & ~c & d) |
        (~b & c & d));
    assign fb = ~((~a & b) | (a & ~b) | (~c & d) | (~a & d) | (~a & ~c));
    assign fc = ~((~a & ~b) | (~b & ~d) | (a & ~c & d) | (~a & c & d) | (~a & ~c & ~d));
    assign fd = ~((c & ~d) | (b & c) | (~a & c) | (~b & ~d) | (~a & b & d) | (a & ~c & ~d) | (a
        & ~b & ~c));
    assign fe = ~((a & ~b) | (~c & ~d) | (a & c) | (~a & b & ~c) | (b & c & ~d));
    assign ff = ~((a & b) | (c & ~d) | (~b & ~d) | (a & c));
    assign fg = ~((a & ~b) | (c & ~d) | (a & d) | (~a & b & ~c) | (~a & ~b & c));
    assign AN0 = 1'b1;
    assign AN1 = 1'b1;
    assign AN2 = 1'b1;


endmodule
```

Figure 10 – Verilog Source Code

A test bench was created to verify the outputs were working as desired. This was accomplished by simulating stimulus for each input value from 0 to 15. The code creating the stimulus is shown in Figure 11, and the resulting timing diagram from running the simulation is shown in figure 12.

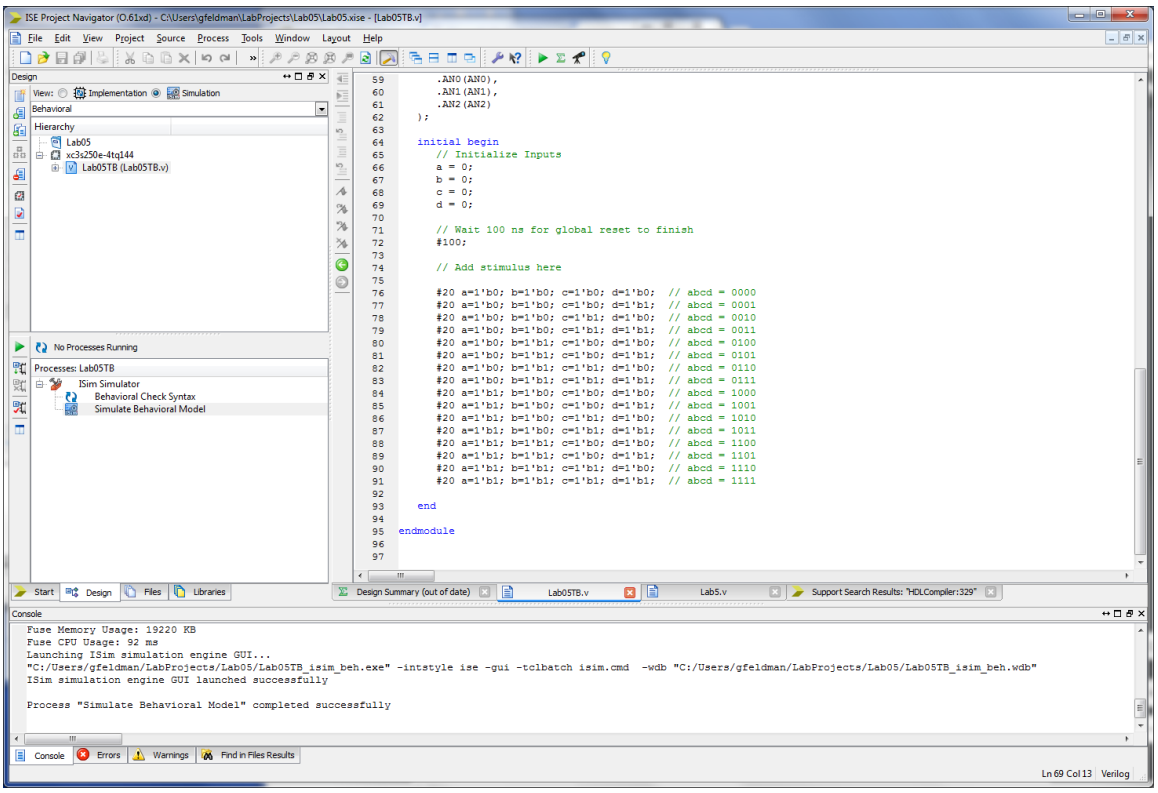

Figure 11 – Stimulus Code

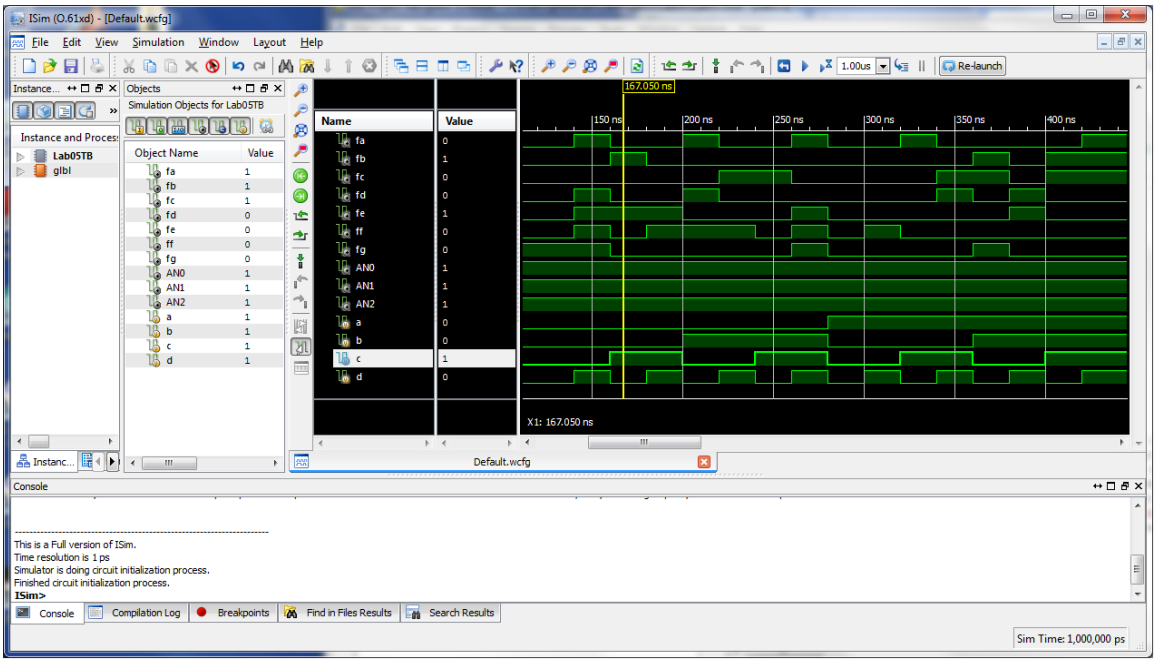

Figure 12 – Timing Diagram for Simulation

A program file of the design was created. Using the Digilent Adept software the program file was uploaded on the Basys board [2].

4 Observations

There were some noteworthy errors made during the design process. It was not noticed until loading the project on the Basys Board that the 7-segment displays is common anode. Therefore the display illuminated the incorrect segments for each digit. The simplest fix was to compliment or negate the initial logic gate combinations. There was also an error in the placement of one segment in the number four. This caused the Karnaugh map and solution for two of the segments to be reworked. After the errors were found and corrected the design worked beautifully.

5 Conclusion

The lab was the most complicated performed thus far. It required multiple logic structures to work seamlessly with one another. Which, in this case, showed how a slight error could be amplified. However, unlike previous labs, once identified errors could be corrected quite easily because of the Verilog software.

6 References

[1] GWU SEAS ECE Department. "Lab 5: 7-Segment Displays and Karnaugh Maps." The ECE 2140 Course Website, Spring 2016.

[2] Digilent, Inc., “Digilent Basys Board Reference Manual,” Aug. 2007.

[3] Rainbow, Daniel. 7-Segment Display Images. Digital image. Photobucket. N.p., n.d. Web. 10 Mar. 2016. <http://s160.photobucket.com/user/daniel_rainbow/media/ahscrewit/Electronics_lessons/2_zps99951651.png.html>.