Release Notes

Constraints:

CPLD device address:

PC-SMBUS : address: 0x20 for BMC.

FPGA-IIC : address: 0x10 BMC does not care.

In-band register address width ： 8-bit

Out-of-band register address width ： 32-bit

Abbreviation:

RO read only

RW read and write

RWSC read and write, self-clearing

RSV reserved

CPLD Register List:

Address：0x00 version_date register

Bit Field	Name	Reset Value	Types	Description
31:0	version_date	version_date	RSV	CPLD version time information register, expressed in hexadecimal. Such as 0x20170629.

Address：0x01 bom ID register

Bit Field	Name	Reset Value	Types	Description
31:0	device_id	0x0	RSV	Reserved.

Address：0x02 device ID register

Bit Field	Name	Reset Value	Types	Description
31:0	build_id	Build_id	RSV	CPLD version SVN information register.

Address：0x04 FPGA power register

Bit Field	Name	Reset Value	Types	Description
31:17	RSV	0x0		Reserved.
16:0	fpga_power	0x0	RO (in-band) RO (out-of-band)	FPGA power register. Value refreshes every second. Unit: W.

Address：0x05 FPGA config register

Bit Field	Name	Reset Value	Types	Description
31:3	RSV	0x0		Reserved.
2	program_b	0x0	RWSC (out-of-band)	When value = 1, the main FPGA is forced to reload. Self-clearing high. It is recommended to drive this signal only if the primary FPGA ICAP fails, allowing the FPGA to load the safe version.
1:0	~~fpga_sel[1:0]~~	~~0x0~~	~~RWSC~~	~~Control FPGA loading version 00 = safe; 01 = working.~~

Address：0x06 CPLD ICAP config register

Bit Field	Name	Reset Value	Types	Description
31:2	RSV	0x0		Reserved.
1	cpld_start	0x0	RWSC (out-of-band)	1 = active, controls the main FPGA to enter the reload process.
0	cpld_sel	0x0	RWSC (out-of-band)	0 = safe; 1 = working.

Address：0x07 flash enable register

Bit Field	Name	Reset Value	Types	Description
31:1	RSV	0x0		Reserved.
0	flash_en	0x0	RW	Upgraded flash enable control. BMC permission control. 1 = valid.

Address：0x08 FPGA DONE register

Bit Field	Name	Reset Value	Types	Description
31:1	RSV	0x0		Reserved.
0	FPGA_done	0x0	RO	Main FPGA load completion signal. 1 = completed.

Address：0x09 power chip register 0x88

Bit Field	Name	Reset Value	Types	Description
31:16	RSV	0x0		Reserved.
15:0	VIN	0x0	RO (in-band)	Input voltage in 100mV units.

			RO (out-of-band)	

Address：0x0a power chip register 0x89

Bit Field	Name	Reset Value	Types	Description
31:16	RSV	0x0		Reserved.
15:0	IIN	0x0	RO (in-band) RO (out-of-band)	Input current: unit =input maximum current divided by 31. The maximum current is 31A.

Address：0x0b power chip register 0x8b

Bit Field	Name	Reset Value	Types	Description
31:16	RSV	0x0		Reserved.
15:0	VOUT	0x0	RO (in-band) RO (out-of-band)	Output voltage in 5mV units.

Address：0x0c power chip register 0x8c

Bit Field	Name	Reset Value	Types	Description
31:16	RSV	0x0		Reserved.
15:0	IOUT	0x0	RO (in-band) RO (out-of-band)	Output current. Unit: A.

Address：0x0d power chip register 0x8d

Bit Field	Name	Reset Value	Types	Description
31:16	RSV	0x0		Reserved.
15:0	TM	0x0	RO (in-band) RO (out-of-band)	Temperature. Unit: Celsius.

Address：0x0e power chip register 0x97

Bit Field	Name	Reset Value	Types	Description
31:16	RSV	0x0		Reserved.
15:0	PIN	0x0	RO (in-band) RO (out-of-band)	Input power consumption. Unit: W.

Address：0x0f power chip register 0xea

Bit Field	Name	Reset Value	Types	Description
31:24	tmax_iinmax	0x0	RO (in-band) RO (out-of-band)	
23:16	protect_isl	0x0	RO (in-band) RO (out-of-band)	
15:8	avg_ocp	0x0	RO (in-band) RO (out-of-band)	
7:0	imax	0x0	RO (in-band)	

Bit Field	Name	Reset Value	Types	Description
			RO (out-of-band)	

Address：0x10 ICAP config register (CPLD loading)

Bit Field	Name	Reset Value	Types	Description
31:2	RSV	0x0		Reserved.
1	start	0x0	RWSC (in-band)	1 = active, controls the CPLD to enter the reload process.
0	sel	0x0	RWSC (in-band)	0 = safe; 1 = working.

Address：0x11 imax_set_q register (power chip fixed current value)

Bit Field	Name	Reset Value	Types	Description
31:0	imax_set_q	0x0	RW (in-band)	Power chip fixed current value.

Address：0x12 imxa_set_en register (fixed current enable)

Bit Field	Name	Reset Value	Types	Description
31:1	RSV	0x0		Reserved.
0	imax_set_en	0x0	RWSC (in-band)	1 = active, controls CPLD writes of the values in 0x11/0x14/0x15 to the power chip, self-clearing.

Address：0x13 temperature register

Bit Field	Name	Reset Value	Types	Description
31:0	temper	0x0	RO (out-of-band)	Temperature register. Value refreshes every second. The BMC needs to read the value of *temper* and convert it to the actual FPGA temperature. The formula is as follows: Temperature = (((*temper* & 0xffff) 501.3743f) / 65536 - 273.6777f); Formula result unit: Celsius.

Address： 0x14 set_avg_ocp register (power chip current protection value)

Bit Field	Name	Reset Value	Types	Description
31:0	set_avg_ocp	0x0	RW (in-band)	Power chip current protection value.

Address：0x15 write_protect register (power chip current protection value)

Bit Field	Name	Reset Value	Types	Description
31:0	write_protect	0x0	RW (in-band)	Power chip protection value.

Address：0x16 set_tmax_iinmax register (maximum current)

Bit Field	Name	Reset Value	Types	Description
31：0	set_tmax_iinmax	0x0	RW (in-band)	Maximum current.

Address：0x17 read_vid_value register (read VID register value)

Bit Field	Name	Reset Value	Types	Description
31:8	RSV	0x0	RO (in-band)	Reserved.
&:0	read_vid_value	0x0	RO (in-band)	Read set_vid register value (power chip address 0xda).

Address：0x18 set_vid register (set VID register value)

Bit Field	Name	Reset Value	Types	Description
31:8	RSV	0x0	RW (in-band)	Reserved.

Bit Field	Name	Reset Value	Types	Description
7:0	set_vid	0x79	RW (in-band)	Set set_vid value, default 0x79.

Address：0x19 set_vid_en register (set the VID enable register)

Bit Field	Name	Reset Value	Types	Description
31:1	RSV	0x0	RWSC (in-band)	Reserved.
0	set_vid_en	0x0	RWSC (in-band)	Value = 1 will enable the corresponding set_vid value, self-clearing.

Address： 0x20 fpga_ver register

Bit Field	Name	Reset Value	Types	Description
15:0	fpga_ver	0x0	RO (in-band) RO (out-of-band)	Hardware version information.

Address： 0x21 Manufacturer register (part 1)

Bit Field	Name	Reset Value	Types	Description
31:0	Manufacturer [63:31]	0x0	RO (out-of-band)	Manufacturer information.

Address：0x22 Manufacturer register (part 2)

Bit Field	Name	Reset Value	Types	Description
31:0	Manufacturer [31:0]	0x0	RO (out-of-band)	Manufacturer information.

Address：0x23 Part_Number4 register

Bit Field	Name	Reset Value	Types	Description
31:0	Part_Number4	0x0	RO (out-of-band)	Hardware information.

Address：0x24 Part_Number 3 register

Bit Field	Name	Reset Value	Types	Description
31:0	Part_Number3	0x0	RO (out-of-band)	Hardware information.

Address：0x25 Part_Number 2 register

Bit Field	Name	Reset Value	Types	Description
31:0	Part_Number2	0x0	RO (out-of-band)	Hardware information.

Address：0x26 Part_Number 1 register

Bit Field	Name	Reset Value	Types	Description
31:0	Part_Number1	0x0	RO (out-of-band)	Hardware information.

Address：0x27 Part_Number 0 register

Bit Field	Name	Reset Value	Types	Description
31:0	Part_Number0	0x0	RO (out-of-band)	[15:0] Hardware information. [31:16] Hardware version.

Address：0x28 SN5 register

Bit Field	Name	Reset Value	Types	Description
31:0	SN5	0x0	RO (out-of-band)	SN information.

Address：0x29 SN5 register

Bit Field	Name	Reset Value	Types	Description
31:0	SN4	0x0	RO	SN information.

Bit Field	Name	Reset Value	Types	Description
			(out-of-band)	

Address：0x30 SN3 register

Bit Field	Name	Reset Value	Types	Description
31:0	SN3	0x0	RO (out-of-band)	SN information.

Address：0x31 SN2 register

Bit Field	Name	Reset Value	Types	Description
31:0	SN2	0x0	RO (out-of-band)	SN information.

Address：0x32 SN1 register

Bit Field	Name	Reset Value	Types	Description
31:0	SN1	0x0	RO (out-of-band)	SN information.

Address：0x33 FW register

Bit Field	Name	Reset Value	Types	Description
31:16	RSV	0x0	RO (out-of-band)	Reserved.
15:0	fpga_version	0x0	RO (out-of-band)	FPGA version.

Address：0x34 Ina226 Shunt register 0x01

Bit Field	Name	Reset Value	Types	Description
31:16	Shunt_0	0x0	RO (in-band) RO (out-of-band)	Monitor 12V, In226 slave_addr=0x1000_000 Shunt register, value refreshes every second. Actual value = (read value) *2.5, Unit: uV
15:0	Shunt_1	0x0	RO (in-band) RO (out-of-band)	Monitor 3.3V, In226 slave_addr=0x1000_001 Shunt register, value refreshes every second. Actual value = (read value) *2.5, Unit: uV

Address：0x35 Ina226 Bus Voltage register 0x02

Bit Field	Name	Reset Value	Types	Description
31:16	Bus_Voltage_0	0x0	RO (in-band) RO (out-of-band)	Monitor 12V, In226 slave_addr=0x1000_000 Bus_Voltage register, value refreshes every second. Actual value = (read value) *1.25

Bit Field	Name	Reset Value	Types	Description
				Unit: mV
15:0	Bus_Voltage_1	0x0	RO (in-band) RO (out-of-band)	Monitor 3.3V, In226 slave_addr=0x1000_001 Bus_Voltage register, value refreshes every second. Actual value = (read value) *1.25 Unit: mV

Address：0x36 Ina226 Current register 0x04

Bit Field	Name	Reset Value	Types	Description
31:16	Current_0	0x0	RO (in-band) RO (out-of-band)	Monitor 12V, In226 slave_addr=0x1000_000 Current register, value refreshes every second. Actual value = (read value) *500 Unit: uA
15:0	Current_1	0x0	RO (in-band) RO (out-of-band)	Monitor 3.3V, In226 slave_addr=0x1000_001 Current register, value refreshes every second. Actual value = (read value) *500 Unit: uA

Address：0x37 Ina226 Power register 0x03

Bit Field	Name	Reset Value	Types	Description
31:16	Power_0	0x0	RO (in-band) RO (out-of-band)	Monitor 12V, In226 slave_addr=0x1000_000 Power register, value refreshes every second. Actual value = (read value) *12.5 Unit: mW
15:0	Power_1	0x0	RO (in-band) RO	Monitor 3.3V, In226 slave_addr=0x1000_001

Bit Field	Name	Reset Value	Types	Description
			(out-of-band)	Power register, value refreshes every second. Actual value = (read value) *12.5 Unit: mW

Address：0xaa Board ID register

Bit Field	Name	Reset Value	Types	Description
31:0	Para	0x07	RO (in-band) RO (out-of-band)	Board ID register, value 0x07.