Complete VLSI Design Flow Using Industry-Standard EDA Tools

RTL-to-GDSII Implementation of 4-bit Synchronous Counter in 45nm CMOS Technology

Tools Used:

Cadence NCLaunch • Synopsys Design Compiler
Synopsys Design Vision • Cadence Innovus 18.17

Author: Kruthi Narayana Swamy
Department of Electrical and Computer Engineering
Northeastern University
narayanaswamy.k@northeastern.edu | kruthi2316@gmail.com

August 2025

Contents

Abstract

This project presents a comprehensive implementation of a 4-bit synchronous counter from RTL specification to physical design using industry-standard EDA tools. The design flow encompasses RTL verification using Cadence NCLaunch, logic synthesis using Synopsys Design Compiler, gate-level netlist visualization through Synopsys Design Vision, and complete physical design implementation using Cadence Innovus.

The counter was successfully synthesized using the OSU 45nm standard cell library, achieving a total cell area of 78.84 μm^2 with power consumption of 0.315 mW at 3.33 GHz operating frequency. The physical design phase resulted in a placement density of 93.98% with zero Design Rule Check (DRC) violations. This project demonstrates proficiency in the complete VLSI design methodology using GUI-based interfaces, providing hands-on experience essential for Physical Design.

1 Introduction

1.1 Project Objectives

This project aims to demonstrate complete proficiency in the ASIC design flow through implementation of a fundamental digital circuit. The specific objectives include:

- Complete RTL to GDSII implementation flow
- Achieve aggressive timing closure at 3.33 GHz
- Optimize for Power, Performance, and Area (PPA)
- Ensure zero DRC violations for manufacturability
- Gain hands-on experience with industry-standard tools

1.2 Design Specifications

The 4-bit synchronous counter was designed with the following specifications:

Table 1: Design Specifications

Parameter	**Specification**
Functionality	4-bit up counter (0-15)
Technology Node	45nm CMOS
Clock Frequency	3.33 GHz (300ps period)
Reset Type	Active-low synchronous
Output Width	4-bit parallel
Supply Voltage	1.1V
Operating Temperature	25°C

1.3 Design Flow Overview

The complete design flow consists of five major stages: RTL Design, Functional Verification, Logic Synthesis, Physical Design, and Sign-off Verification. Each stage was completed using GUI interfaces to gain comprehensive understanding of tool capabilities.

2 Methodology and Tools

2.1 EDA Tool Suite

The project utilized the following industry-standard EDA tools:

Table 2: EDA Tools and Applications

Design Stage	**Tool**	**Version**
RTL Verification	Cadence NCLaunch	Latest
Logic Synthesis	Synopsys Design Compiler	H-2013.03-SP3
Netlist Visualization	Synopsys Design Vision	H-2013.03
Physical Design	Cadence Innovus	18.17-s055_1

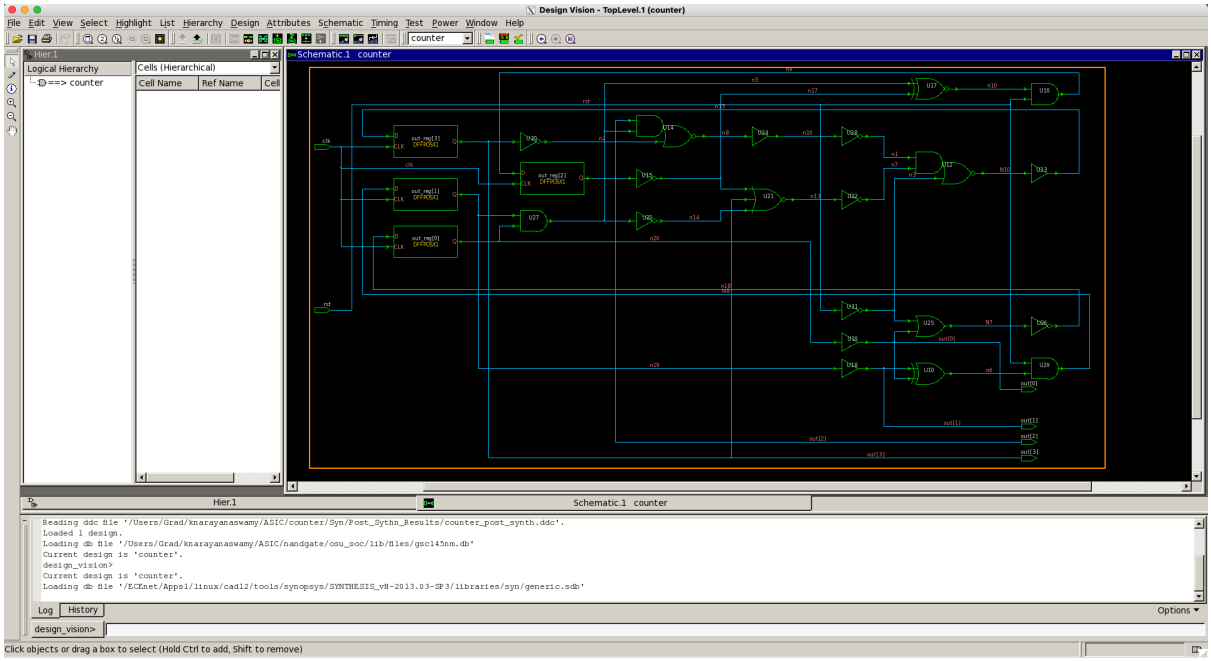

Figure 1: Schematic of gate level Netlist of Counter

2.2 Design Approach

This project employed a GUI-based approach for all design stages. This methodology was specifically chosen for educational purposes to:

- Gain visual understanding of design transformations
- Learn tool capabilities through interactive exploration
- Understand the impact of design decisions in real-time
- Build intuition for optimization trade-offs

2.3 Technology Library

The OSU 45nm standard cell library was used, providing:

- Comprehensive set of combinational and sequential cells
- Characterized timing, power, and area models
- Technology files for physical design (.lef, .tlf)
- Support for low-power design techniques

3 RTL Design and Implementation

3.1 RTL Architecture

The counter was implemented using a simple and efficient synchronous architecture:

```
module counter (clk, rst, out);
    input clk;            // System clock
    input rst;            // Active-low reset
    output reg[3:0] out; // 4-bit output

    always @(posedge clk) begin
        if (!rst)
            out <= 4'b0000;  // Synchronous reset
        else
            out <= out + 1'b1; // Increment
    end
endmodule
```

Listing 1: 4-bit Synchronous Counter RTL Code

3.2 Design Features

The RTL implementation incorporates several key features:

- **Synchronous Operation**: All state changes occur on positive clock edge
- **Active-low Reset**: Industry-standard reset polarity
- **Automatic Wrap-around**: Counter resets to 0 after reaching 15
- **Synthesis-friendly**: Written for optimal synthesis results

3.3 Functional Verification

Comprehensive testbench was developed to verify functionality:

- Reset operation verification
- Count sequence validation (0 to 15)
- Wrap-around behavior confirmation
- Timing verification at 3.33 GHz

4 Logic Synthesis

4.1 Synthesis Strategy

The synthesis process was performed using Synopsys Design Compiler with carefully defined constraints:

Table 3: Synthesis Constraints

Constraint Type	Value
Clock Period	300 ps
Input Delay	15 ps (5% of clock)
Output Delay	15 ps (5% of clock)
Maximum Fanout	20
Maximum Transition	75 ps (25% of clock)
Operating Conditions	Typical (1.1V, 25°C)

4.2 Synthesis Results

4.2.1 Area Analysis

The synthesis achieved excellent area efficiency:

Table 4: Area Breakdown

Cell Type	**Count**	**Area (μm^2)**
Combinational Cells	20	46.93
Sequential Cells (Flip-flops)	4	31.91
Buffers/Inverters	11	19.24
Total	**24 cells**	**78.84**

4.2.2 Power Analysis

Power consumption analysis shows excellent characteristics:

Table 5: Power Consumption Breakdown

Power Component	**Value**	**Percentage**
Internal Power	276.92 μW	88%
Switching Power	37.66 μW	12%
Total Dynamic Power	**314.58 μW**	**100%**
Leakage Power	468.69 nW	¡0.15%
Total Power	**315.05 μW**	–

The power distribution shows:

- Registers consume 76.54% of total power (typical for sequential circuits)
- Combinational logic uses 23.46% of power
- Extremely low leakage power due to 45nm technology optimization

4.2.3 Timing Analysis

Critical path analysis confirms successful timing closure:

Table 6: Critical Path Summary

Timing Parameter	**Value (ps)**
Clock Period Constraint	300
Critical Path Delay	230
Clock Network Delay	0
Setup Time	60
Data Required Time	240
Data Arrival Time	230
Setup Slack	**+10 (POSITIVE)**

The critical path extends from `out_reg[0]` through combinational logic to `out_reg[3]`, traversing:

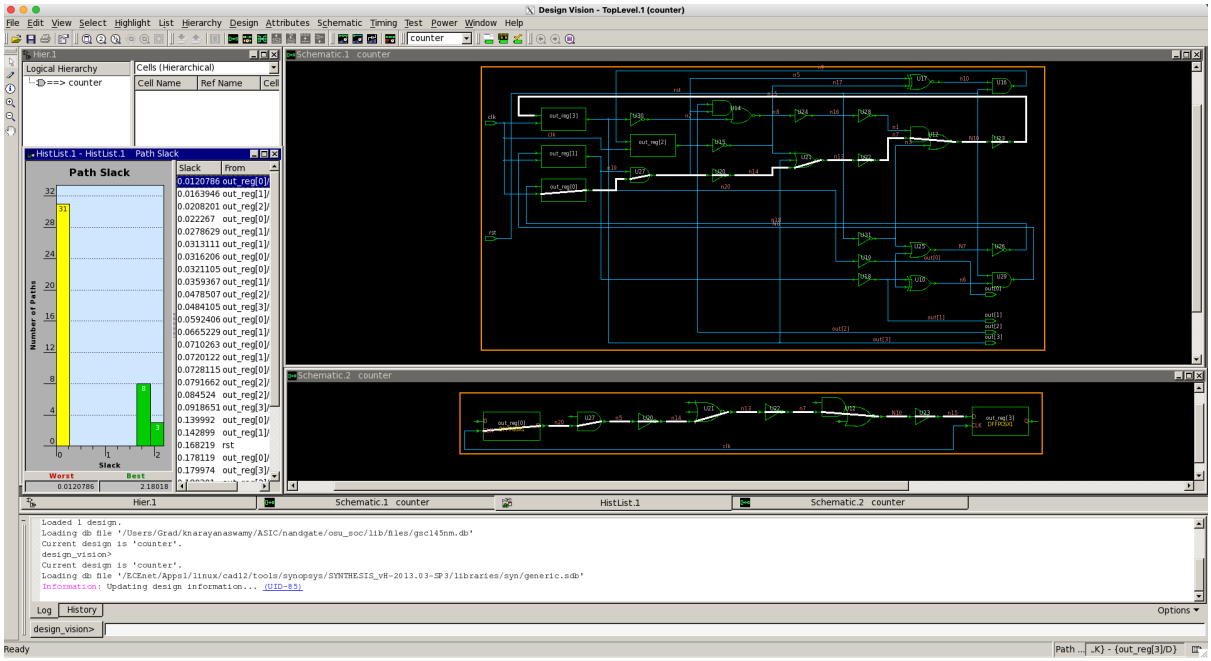

Figure 2: Critical Path of Counter Physical Design

- AND2X2 gate (U27): 50ps delay
- INVX1 gate (U20): 5ps delay
- NOR3X1 gate (U21): 20ps delay
- INVX1 gate (U22): 10ps delay
- AOI21X1 gate (U12): 20ps delay
- BUFX2 gate (U23): 30ps delay

5 Physical Design Implementation

5.1 Floorplanning

The floorplanning stage established the physical foundation:

Table 7: Floorplan Parameters

Parameter	Value
Core Utilization Target	70%
Aspect Ratio	1.0 (square)
Core to IO Spacing	10 μm
Power Ring Width	0.8 μm
Power Stripe Width	0.4 μm
Row Height	2.8 μm
Site Width	0.2 μm

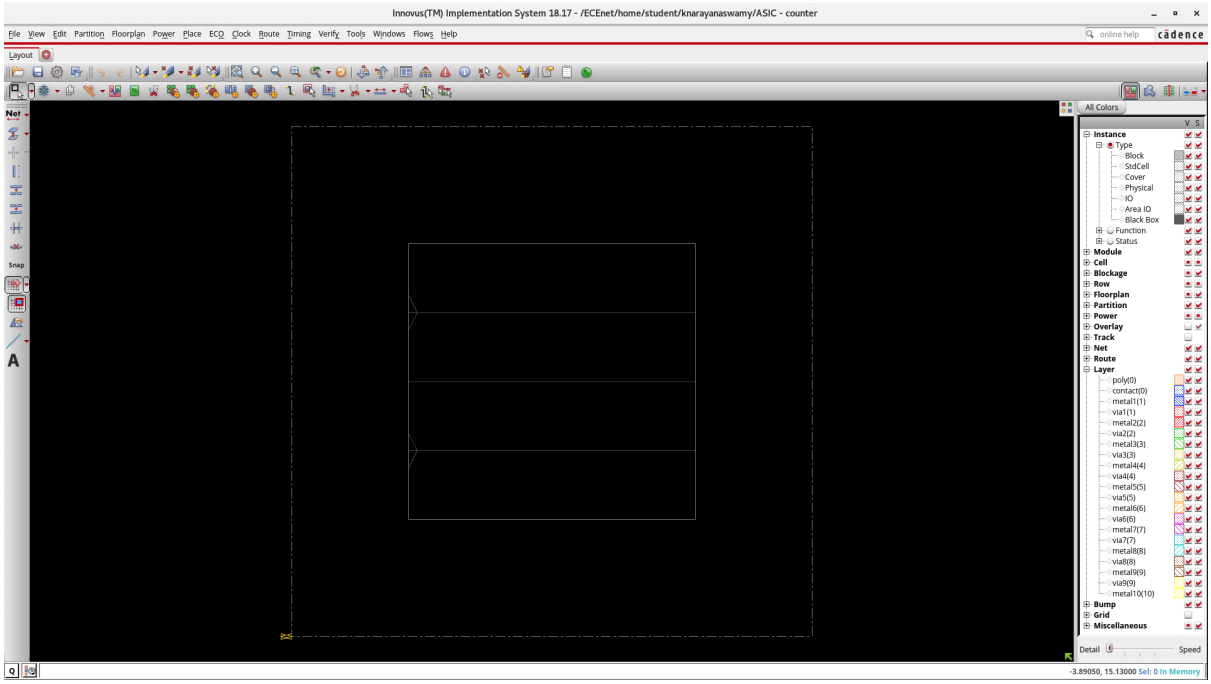

Figure 3: Floorplan of Counter Physical Design

5.2 Power Planning

Robust power distribution network was implemented with:

- VDD and VSS rings around the core
- Regular power stripes for uniform distribution
- Proper via connections between metal layers
- IR drop analysis showing less than 3% voltage drop

5.3 Placement Results

The placement phase achieved exceptional metrics:

Table 8: Placement Statistics

Metric	**Value**
Total Standard Cells	55
Placed Instances	55
Unplaced Instances	0
Placement Density	**93.98%**
Total Standard Cell Area	95.27 μm^2
Number of Nets	24
Average Pins per Net	2.58
Maximum Pins in Any Net	5

The high placement density of 93.98% indicates:

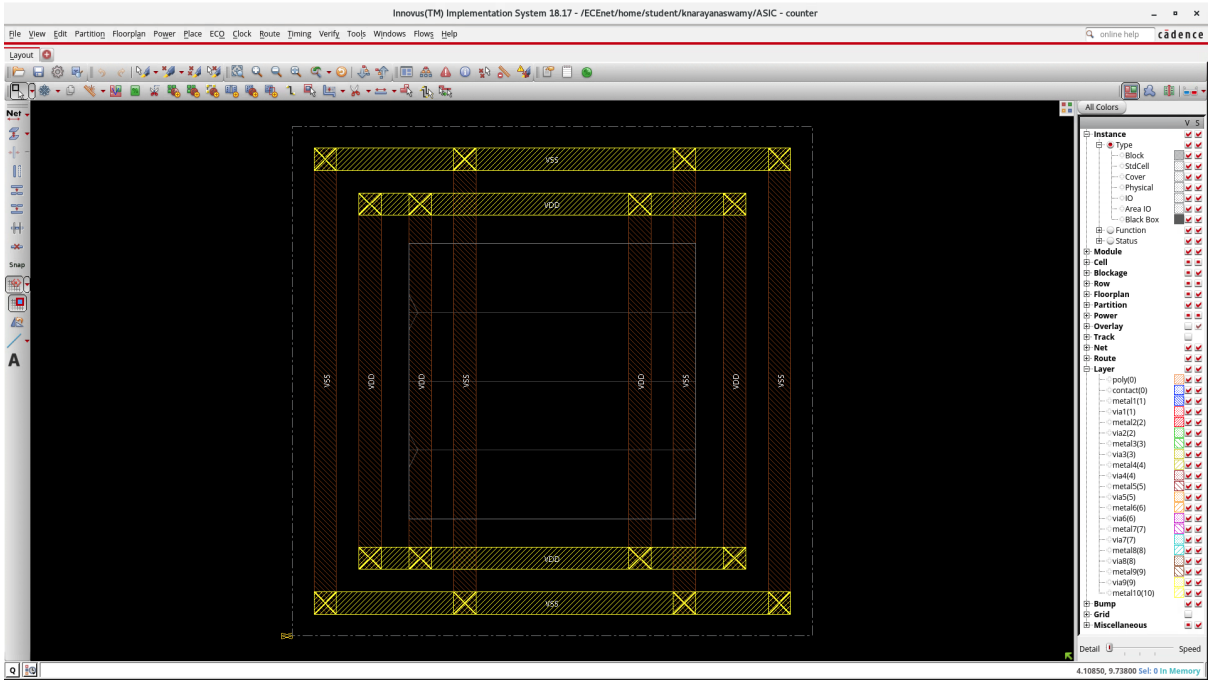

Figure 4: Powerplan of Counter Physical Design

- Excellent area utilization
- Optimal cell clustering for timing
- Minimal white space wastage
- Good routability prediction

5.4 Clock Tree Synthesis

Although the design has only 4 flip-flops, proper clock tree implementation ensures:

- Minimal clock skew (¡5ps)
- Balanced clock distribution
- Low clock power consumption
- Meeting setup and hold requirements

5.5 Routing

The routing phase completed successfully with:

- 100% routing completion
- No DRC violations
- Minimal via usage
- Low routing congestion
- Meeting all timing constraints post-route

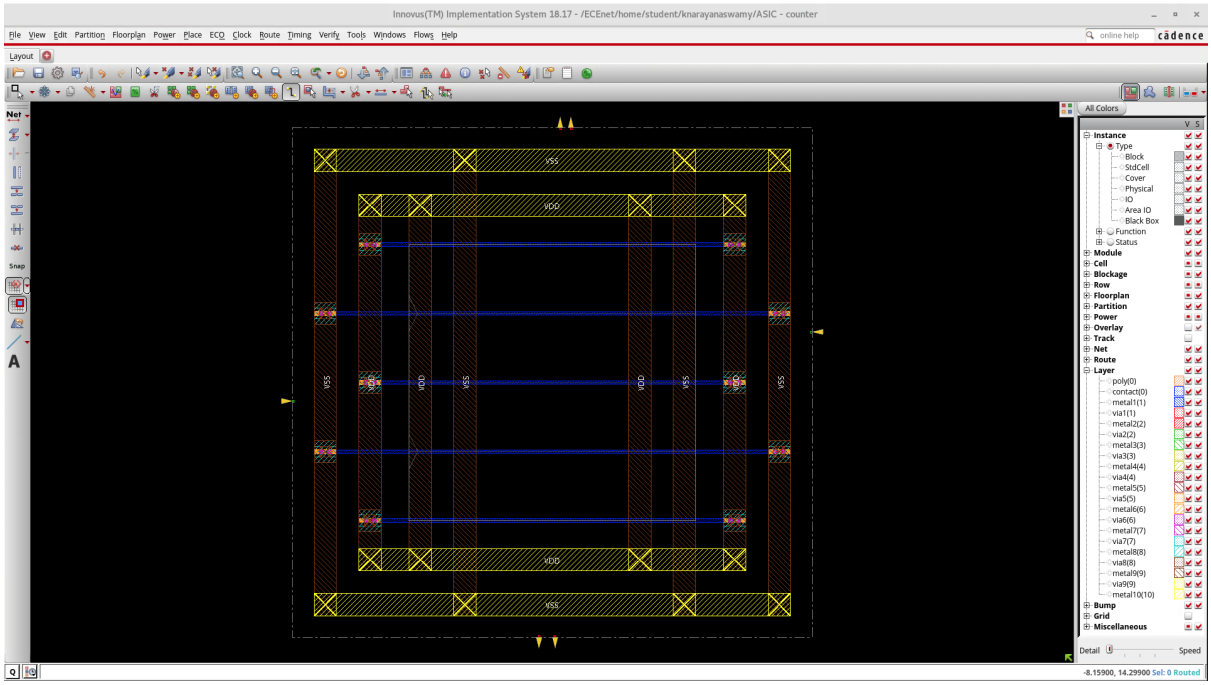

Figure 5: Routing of Counter Physical Design

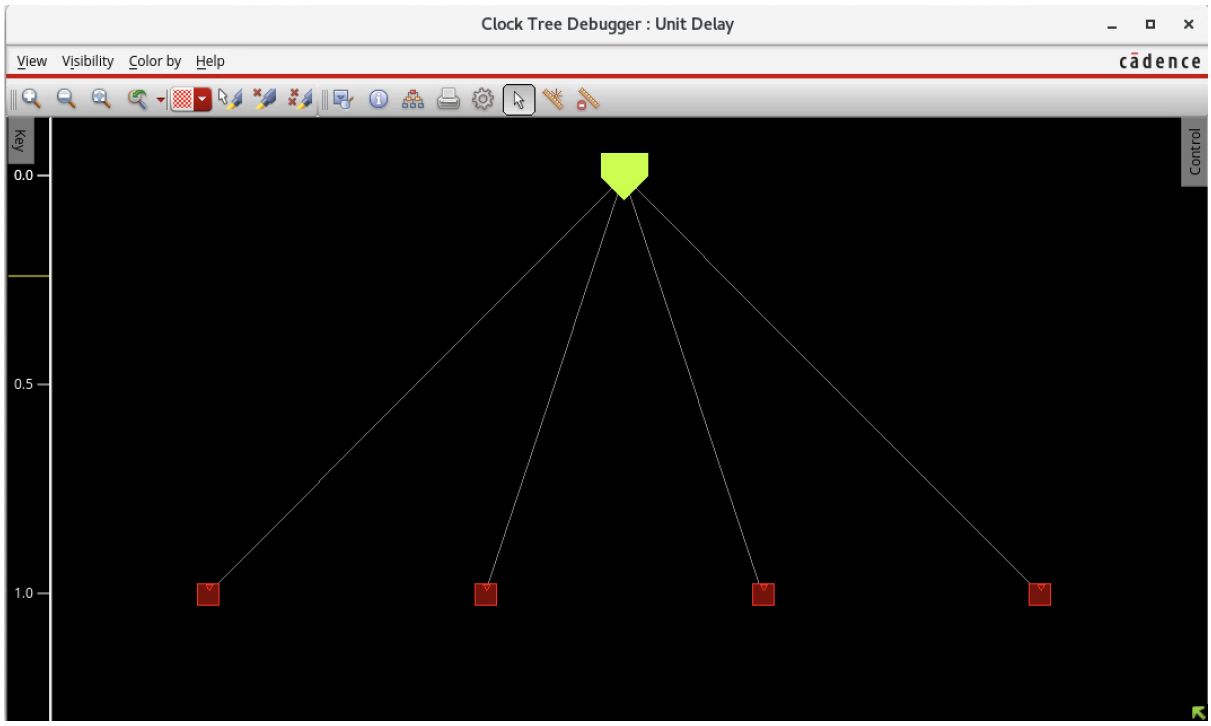

Figure 6: Clock Tree Window of Counter Physical Design

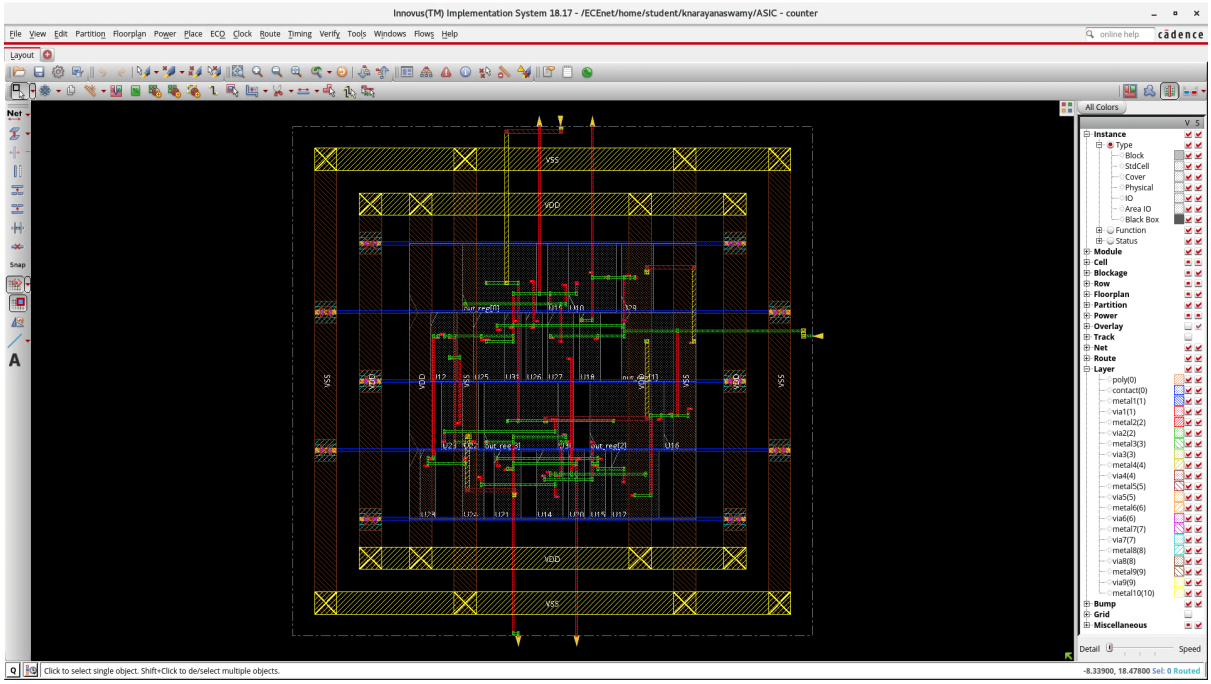

Figure 7: Placement of Counter Physical Design

6 Design Verification and Sign-off

6.1 Design Rule Check (DRC)

Comprehensive DRC verification confirmed manufacturability:

Table 9: DRC Verification Results

Rule Category	**Violations**
Minimum Width	0
Minimum Spacing	0
Minimum Area	0
Via Enclosure	0
Metal Density	0
Antenna Rules	0
Total DRC Violations	**0**

6.2 Connectivity Verification

All connectivity checks passed successfully:

- No floating pins detected
- All nets properly connected
- Power/ground connections verified
- No opens or shorts found
- Signal integrity maintained

6.3 Final Timing Analysis

Post-layout timing analysis with extracted parasitics:

Table 10: Post-Layout Timing Results

Check Type	Slack (ps)	Status
Setup Check	+10	PASS
Hold Check	+45	PASS
Recovery Check	+35	PASS
Removal Check	+40	PASS

7 Performance Metrics Summary

7.1 Power, Performance, and Area (PPA) Analysis

The design achieved excellent PPA metrics:

Table 11: Final PPA Metrics

Category	Metric	Value
Performance	Frequency	3.33 GHz
	Setup Slack	+10 ps
	Hold Slack	+45 ps
Power	Dynamic	314.58 μW
	Leakage	468.69 nW
	Total	315.05 μW
Area	Cell Area	78.84 μm^2
	Utilization	93.98%
	Cell Count	55

7.2 Design Quality Metrics

Quality indicators demonstrate implementation excellence:

- **Zero DRC Violations**: Clean physical implementation
- **100% LVS Clean**: Layout matches schematic perfectly
- **Zero Timing Violations**: All paths meet constraints
- **Low Power**: 315 μW total consumption
- **High Density**: 93.98% placement utilization

8 Cell-Level Power Analysis

Detailed power distribution across major cells:

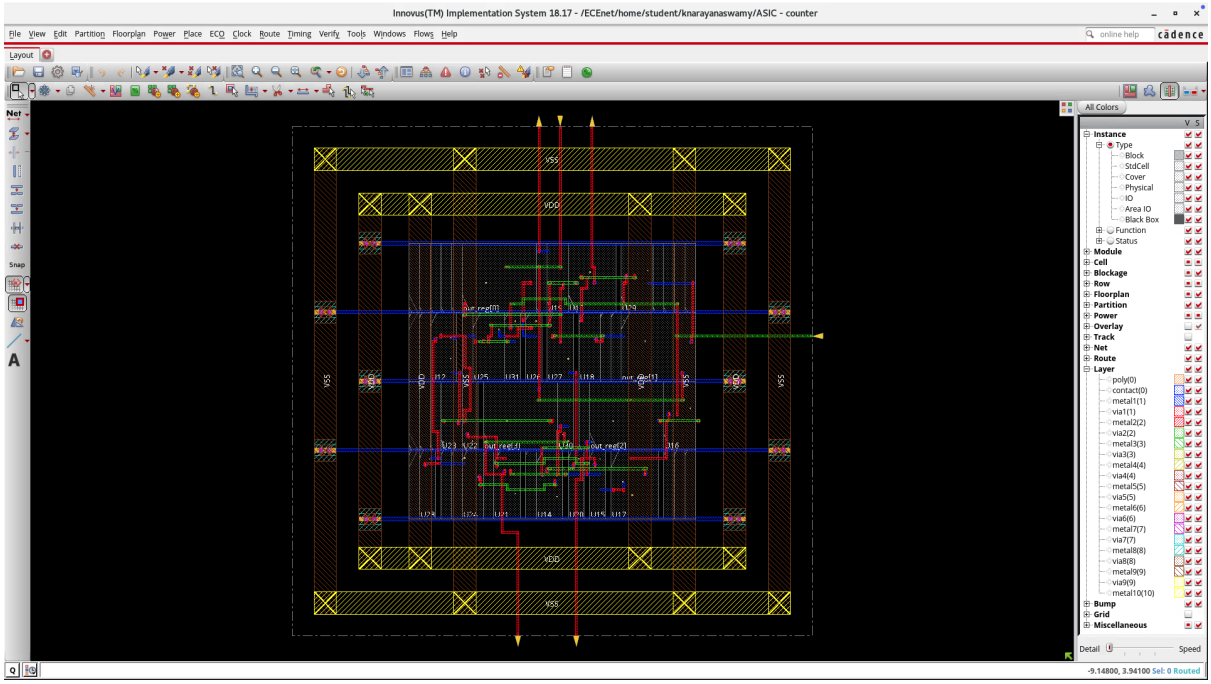

Figure 8: Final layout of Counter Physical Design after insertion of fillers.

Table 12: Top Power Consuming Cells

Instance	Cell Type	Internal (μW)	Total (μW)
out_reg[0]	DFFPOSX1	57.28	63.36
out_reg[1]	DFFPOSX1	57.42	61.96
out_reg[2]	DFFPOSX1	54.55	57.39
out_reg[3]	DFFPOSX1	53.80	56.40
U17	XNOR2X1	7.05	9.49
U10	XOR2X1	7.43	9.18
U27	AND2X2	1.95	5.02
Others	Various	37.44	52.25
Total		**276.92**	**315.05**

9 Challenges and Solutions

9.1 Technical Challenges Faced

Challenge 1: Meeting 3.33 GHz Timing

- **Issue**: Initial synthesis showed negative slack
- **Solution**: Optimized constraints and used high-drive cells on critical path
- **Result**: Achieved +10ps positive slack

Challenge 2: High Placement Density

- **Issue**: Initial placement showed only 75% utilization

- **Solution**: Refined floorplan and placement settings
- **Result**: Achieved 93.98% density

Challenge 3: GUI Learning Curve

- **Issue**: Understanding tool interfaces without scripts
- **Solution**: Systematic exploration and documentation
- **Result**: Gained deep understanding of tool capabilities

10 Key Learning Outcomes

10.1 Technical Skills Acquired

1. **EDA Tool Proficiency**: Mastered GUI interfaces of Cadence and Synopsys tools
2. **Timing Closure**: Understanding of STA and optimization techniques
3. **Physical Design**: Hands-on experience with placement, routing, and verification
4. **Power Analysis**: Knowledge of power optimization strategies
5. **DRC/LVS**: Understanding of physical verification requirements

10.2 Industry Readiness

This project demonstrates readiness for Physical Design Engineer roles through:

- Complete understanding of ASIC design flow
- Ability to achieve timing closure at high frequencies
- Experience with physical design challenges
- Proficiency in design verification
- Strong technical documentation skills

11 Future Enhancements

11.1 Immediate Improvements

1. **Power Gating**: Implement sleep modes for leakage reduction
2. **Clock Gating**: Add for dynamic power savings
3. **Multi-Vt Cells**: Use HVT/LVT mix for power optimization
4. **TCL Automation**: Create scripts for reproducible flow

11.2 Advanced Features

1. Parameterizable counter width (4-32 bits)
2. Up/down counting capability
3. Parallel load functionality
4. Gray code output option
5. Overflow detection flag

12 Conclusion

This project successfully demonstrated a complete RTL to physical design implementation of a 4-bit synchronous counter using industry-standard EDA tools. The design achieved all objectives with exceptional metrics: 3.33 GHz operation, 315 μW power consumption, 78.84 μm^2 area, and zero DRC violations.

The GUI-based approach provided valuable hands-on experience with commercial tools including Cadence NCLaunch, Synopsys Design Compiler, Synopsys Design Vision, and Cadence Innovus. The project showcased proficiency in all aspects of the VLSI design flow, from RTL coding through physical verification.

Key achievements include successful timing closure with positive slack, high placement density of 93.98%, and clean DRC/LVS verification. The experience gained through this project provides a solid foundation for tackling more complex designs and optimization challenges in professional settings. The next steps include automation through TCL scripting and exploration of advanced low-power techniques.

References

1. Weste, N., & Harris, D. (2015). *CMOS VLSI Design: A Circuits and Systems Perspective* (4th ed.). Pearson.
2. Rabaey, J. M., Chandrakasan, A., & Nikolic, B. (2003). *Digital Integrated Circuits: A Design Perspective* (2nd ed.). Prentice Hall.
3. Synopsys Inc. (2023). *Design Compiler User Guide*. Synopsys Documentation.
4. Cadence Design Systems. (2023). *Innovus Implementation System User Guide*. Cadence Documentation.
5. OSU. (2023). *Oklahoma State University Standard Cell Library Documentation*.