Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.780 ns	Worst Hold Slack (WHS):	0.228 ns	Worst Pulse Width Slack (WPWS):	19.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	6130	Total Number of Endpoints:	6130	Total Number of Endpoints:	3220

All user specified timing constraints are met.

After synthesis:

Name 1	Slice LUTs (63400)	Slice Registers (126800)	F7 Muxes (31700)	F8 Muxes (15850)	Bonded IOB (210)	BUFGCTRL (32)
N MIPS_Processor	5530	3409	1113	90	173	1
DM (Data_Memory)	2864	2240	609	2	0	0
DU (Decode_Unit)	72	63	0	0	0	0
Mux1 (Mux2_1_32bit)	16	0	0	0	0	0
Mux2 (Mux2_1_32bit_0)	24	0	0	0	0	0
Mux3_1 (Mux3_1_32bit)	37	31	0	0	0	0
PC (Program_Counter)	1398	51	248	24	0	0
PCB (PCBranch)	30	0	0	0	0	0
RF (Register_file)	1089	1024	256	64	0	0

Utilization **Post-Synthesis** | Post-Implementation

Graph | **Table**

Resource	Estimation	Available	Utilization...
LUT	5530	63400	8.72
FF	3219	126800	2.54
IO	173	210	82.38
BUFG	1	32	3.13

After impl:

Name	Slice LUTs (63400)	Slice Registers (126800)	F7 Muxes (31700)	F8 Muxes (15850)	Slice (15850)	LUT as Logic (63400)	LUT Flip Flop Pairs (63400)	Bonded IOB (210)	BUFGCTRL (32)
N MIPS_Processor	5675	3409	963	90	2831	5675	365	173	2
DM (Data_Memory)	2862	2240	609	2	2079	2862	3	0	0
DU (Decode_Unit)	70	63	0	0	59	70	0	0	0
Mux1 (Mux2_1_32bit)	16	0	0	0	15	16	0	0	0
Mux2 (Mux2_1_32bit_0)	24	0	0	0	24	24	0	0	0
Mux3_1 (Mux3_1_32bit)	37	31	0	0	36	37	0	0	0
PC (Program_Counter)	1548	51	98	24	649	1548	1	0	1
PCB (PCBranch)	30	0	0	0	8	30	0	0	0
RF (Register_file)	1089	1024	256	64	859	1089	0	0	0

Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization...
LUT	5675	63400	8.95
FF	3219	126800	2.54
IO	173	210	82.38
BUFG	2	32	6.25