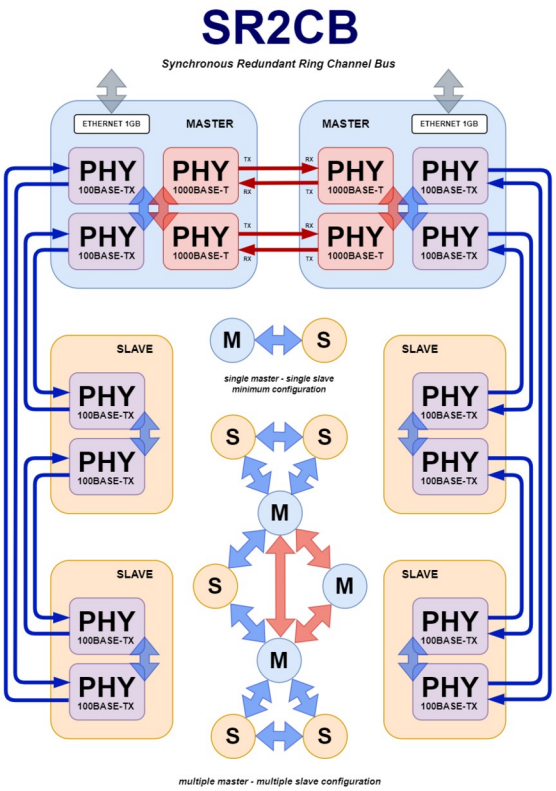
Krynen Technology

SR2CB

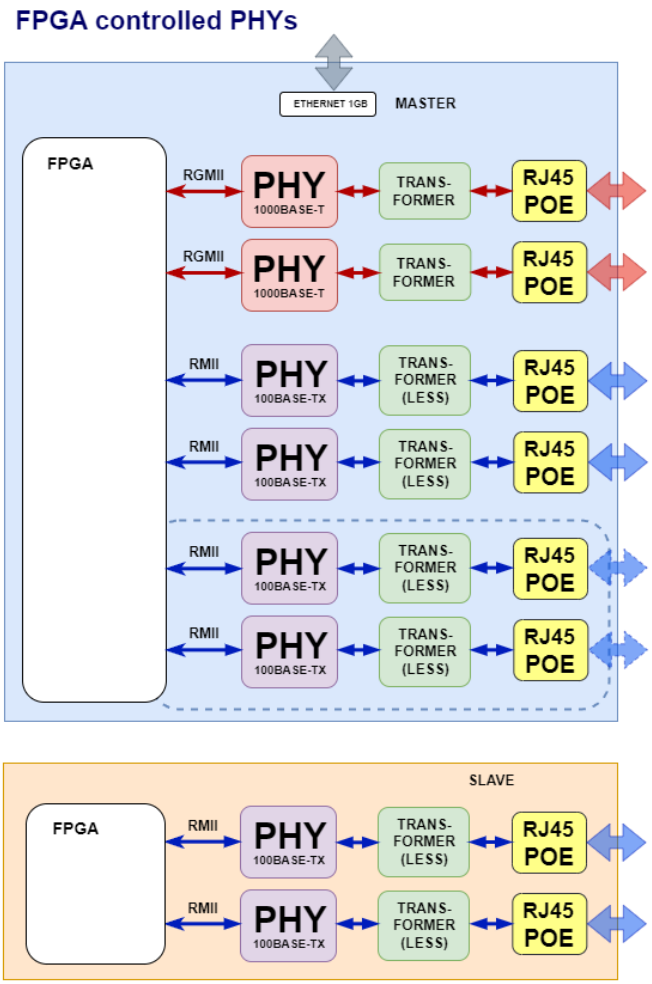
The Synchronous Redundant Ring Channel Bus (*S-R-square-Channel-Bus*) is a data bus with a open ring topology where a data *channel* is constructed from successive frames fixed bit/bits/byte/word/dword/qword/etc. positions. The SR2CB network protocol supports *synchronous* operation by means of a distributed clock mechanism. Each ring node has two full duplex (TX/RX) hardware ports.

The physical interface (*layer*) between SR2CB nodes is based on 1000BASE-T, 100BASE-TX, RS-485 or LVDS. 1000BASE-T and 100BASE-TX PHYs are also common for the ethernet network physical layer but not bound to transmit solely ethernet frames. The SR2CB frames are continuously transmitted by the ring nodes clockwise and counterclockwise. Slave nodes retransmit those SR2CB frames after receipt and insert or extract channel data 'on the fly'. Within a SR2CB master/slave ring the single master node starts the redundant ring initialization and transmits the SR2CB frames. Master nodes do not pass SR2CB frames around except for a broken redundant ring (*single point of failure*) or when the redundant ring is exclusivly build from master nodes.

A minimum SR2CB system configuration consist of a single master and a single slave. The number of slave nodes could be extended to a maximum of 8192 slave nodes for each master/slave ring. Each node has a packet propagation delay of about 0.5 us, so a ring with the maximum number of nodes has a total delay of ~4 ms. This the maximum packet delay between the slave nodes adjacent to the master (counter and counterclockwise first ring node position). Multiple SR2CB master devices could assemble a ring where data channels from different master/slave ring configurations could be shared.

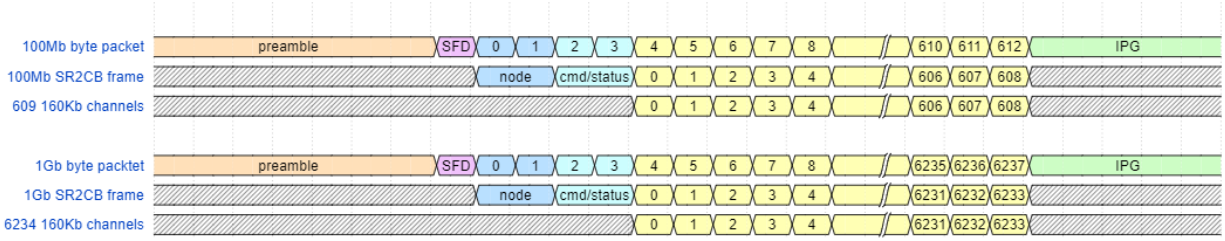


Master nodes might have a separate ethernet port. 1000BASE-T and 100BASE-TX PHYs full duplex ports could be controlled by an FPGA. PHY RGMII interface setup reduces the number of PCB traces for the 1000BASE PHY, RMII does this for the 100BASE-TX PHY.



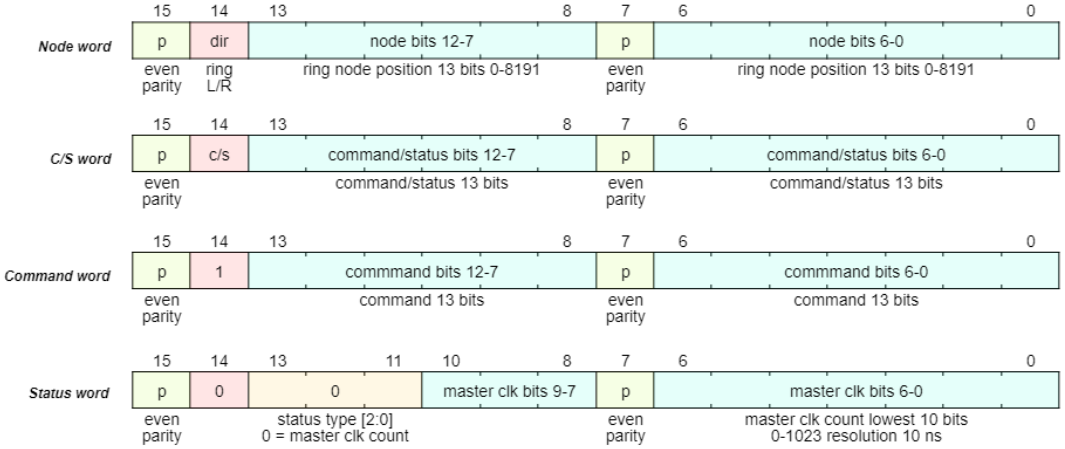
The number of SR2CB frames per second depends on the frame packet size which for the 'ethernet' PHYs starts with a SFD (*Start Frame Delimeter*) byte preceding by seven preamble bytes and ends with an IPG (*Idle Packet Gap*) sequence of five bytes. An audio application 20k SR2CB frames per second gives a byte channel speed of 160kB/s (20k times 8 bits) and offers 609 byte channels for 100BASE-TX and 6234 byte channels for 1000BASE-T PHYs. The 160kB/s is high enough for good audio quality APCM (voice - low latency - described in the Bluetooth A2DP specification) and Opus (voice and music) codecs - if required AES encrypted and authenticated.

SR2CB 100Mb/1Gb PHY serial communication

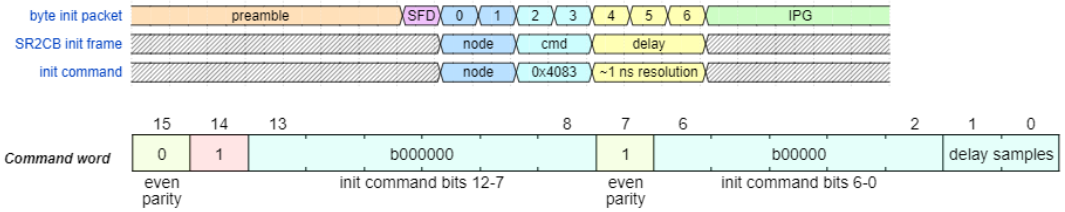


The PHY serial bit stream is LSB first on byte level and little endian on multiple byte level (word, dword, qword)

Preamble 7 bytes 0x55, SFD (Start Frame Delimeter) 1 byte 0xD5, IPG 5 bytes (Inter Packet Gap - PHY generated), serial stream is LSB on byte level, first 8 packet bytes from left to right gives b1010101010101010101010101010101010101010101010101010101010101011!



SR2CB ring initialization, master/slave clock synchronization



SR2CB frame channel configuration