BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
INSTRUCTION DIVISION
FIRST SEMESTER 2017 - 2018
COURSE HANDOUT (PART II)

Date: 02 / 08 / 2017

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No : **CS F342**
Course Title : **Computer Architecture**
Instructor-in-charge : S. MOHAN
Instructors (Lecture) : S. Gurunarayanan
Instructors (Lab) : Mayuri D., Sai Sesha Chalapathi, Prerna Kaushik

1. Scope and Objective:

This course aims at introducing the concept of computer architecture and organization. It involves design aspects, and deals with the current trends in computing architecture. System resources such as memory technology and I/O subsystems needed to achieve proportional increase in performance will also be discussed.

2. Text Book:

(T1) Patterson, David A & J L Hennenssy, *Computer Organisation & Design*, Elsevier, 4th Ed., 2009.
(T2) Samir Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*, Pearson Education Asia, 2nd Ed. 2006.
(T3) W. Stallings, *Computer Organisation & Architecture,* PHI, 10th ed., 2015

3. Reference Books:

(i) J.L. Hennessy & D.A. Patterson, *Computer Architecture: A Quantitative Approach*, Morgan Kauffmann, 5th Ed, 2012.

4. Course Plan:

Lecture No.	Topics to be covered	Reference to T1
01, 02	Introduction	Ch. 1.1-1.3.1.5-1.10
03, 04, 05	MIPS Architecture & Instruction Set	Ch. 2
06	Computer Arithmetic	Ch. 3.1 – 3.5
07,08	Floating Point Arithmetic	Ch 3.6 – 3.10
09, 10	Role of Performance	Ch. 1.4
11,12, 13	Data path Design	Ch. 4.1 – 4.4
14, 15	Control Hardware	Appendix – D
16, 17, 18	Exceptions & Microprogramming	Ch. 4.9
19, 20	Memory Organisation- Introduction	Ch5.1
21, 22	Cache Memory Organisation	Ch.5.2
23, 24, 25	Cache Performance	Ch. 5.3
26, 27	I/O Organisation	Ch. 6
28, 29	Pipelining – Design Issues	Ch. 4.5 – 4.6
30, 31	Data Hazards	Ch. 4.7

32, 33	Control Hazards	Ch. 4.8
34, 35	Static Branch Prediction	notes
36	Dynamic Branch Prediction	notes
37	Advanced Concepts in pipelining	Ch. 4.12
38, 39,40	Modern Processors	Ch7

5. Evaluation Scheme:

EC No.	Evaluation Component	Duration (min)	Weightage	Date, Time & Venue	Nature of Component
1	Mid Sem Test	90	70	14/10 9:00 - 10:30 AM	Closed Book
2	Lab/Assignments **	-----	45	-----	Open Book
3	Comprehensive	180	85	13/12 FN	Partly Open Book

** Details of assignments will be announced in the class & on course web page.
Text book **T2** will be used for Lab Assignments.

6. Chamber Consultation Hours: ***SM: Tuesday 4PM to 5PM***
SG: Monday 4PM to 5PM

7. Notices: Notices regarding the course will be put up on the CS notice board.

Instructor - in - charge
CS F342