DCS Lab01

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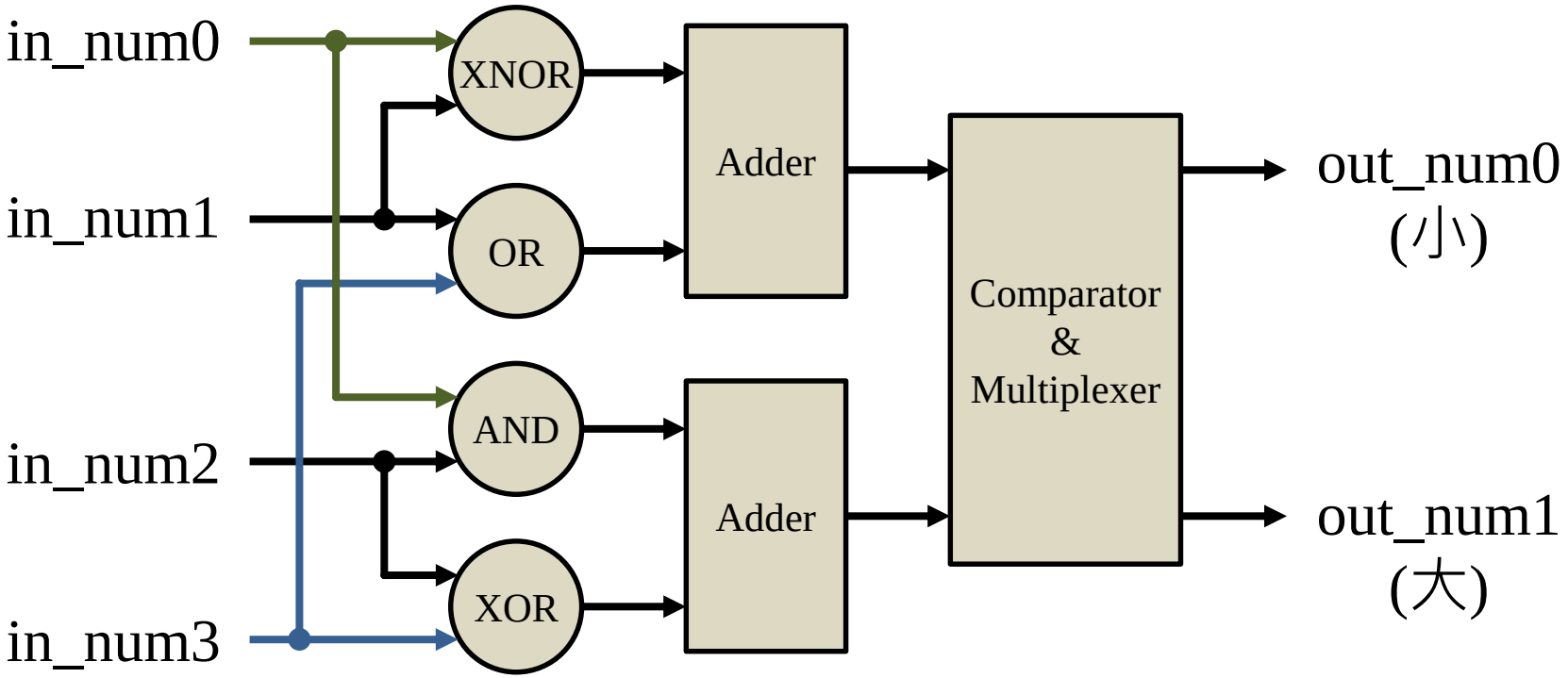
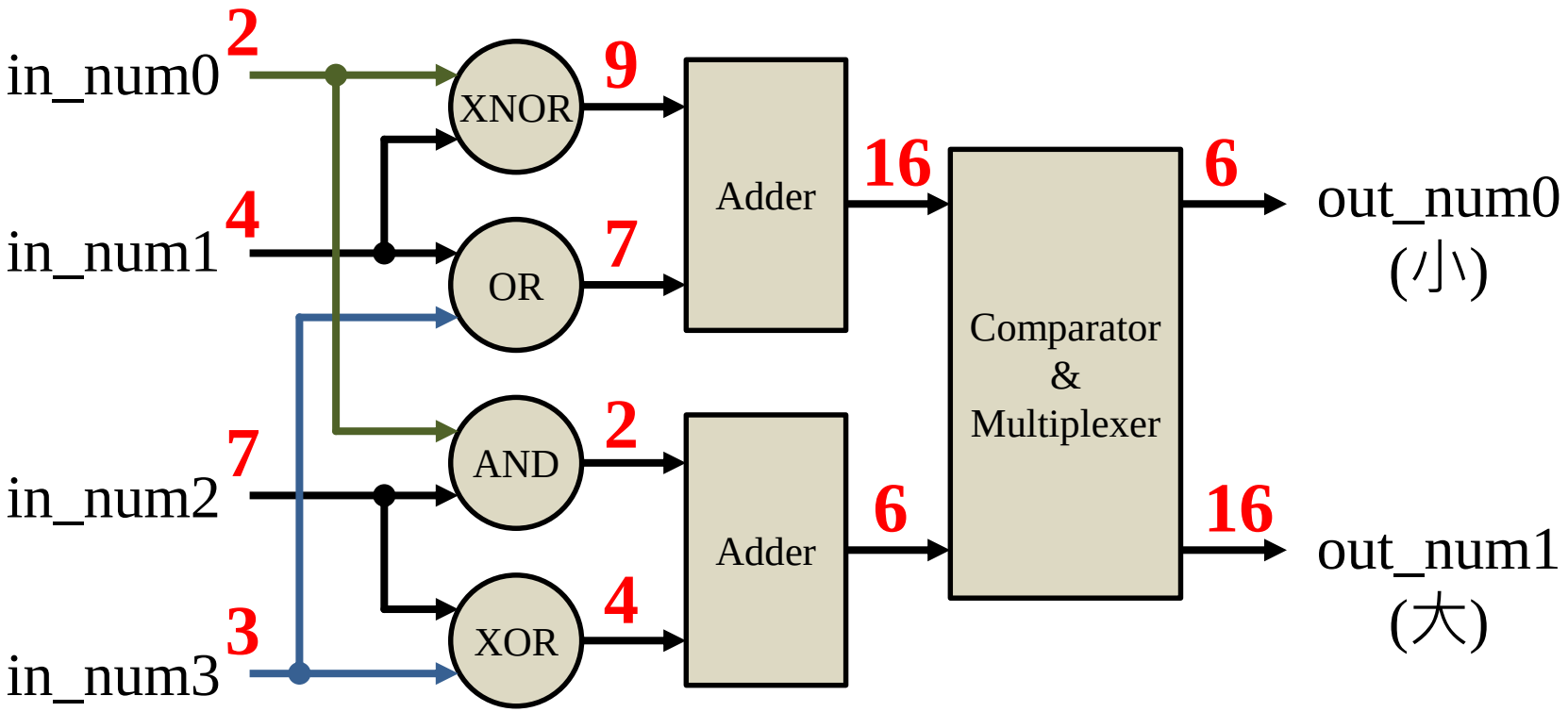
Combinational

- 會有四個數字輸入in_num0 ~ in_num3
  - Ex: in_num0 ~ in_num3 = [2, 4, 7, 3]
- 將數字依照範例，分別做**Bitwise** XNOR, OR, AND, XOR後，
  - Ex: A = in_num0 XNOR in_num1 = 0010 XNOR 0100 = 1001 = 9
    B = in_num1 OR in_num3 = 0100 OR 0011 = 0111 = 7
    C = in_num0 AND in_num2 = 0010 AND 0111 = 0010 = 2
    D = in_num2 XOR in_num3 = 0111 XOR 0011 = 0100 = 4
- 再將運算後的數字依照範例，分AB、CD兩組相加，
  - Ex: A + B = 9 + 7 = 16, C + D = 2 + 4 = 6
- 最後排序**由小至大**輸出。
  - Ex: out_num0 = 6, out_num1 = 16

Block diagram for your reference



Block diagram for your reference



Comb.sv

Input Signal	Bit width	Definition
in_num0	4	Random 4-bit numbers
in_num1	4	
in_num2	4	
in_num3	4	

Output Signal	Bit width	Definition
out_num0	5	out_num0 ≤ out_num1
out_num1	5	

Command

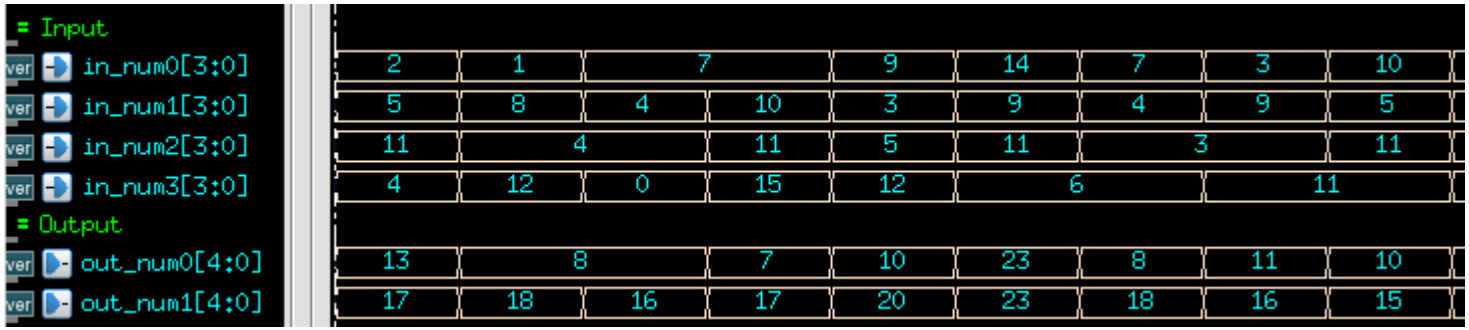
- tar -xvf ~dcsta01/Lab01.tar
- 3/3(四)15:30 (上機課時)
  才會在Server上開放tar檔案

Directory

- Lab01
  - 00_TESTBED
  - 01_RTL
    - 01_run
    - 09_clean_up
    - **Comb.sv**
  - 02_SYN
    - 01_run_dc
    - 09_clean_up
  - 09_UPLOAD
    - 01_upload
    - 02_download

RTL simulation

- cd Lab01/01_RTL/
- ./01_run (電路模擬)
- ./09_clean_up (清除波型檔)
- nWave & (看波型)
  - 範例波型:



Synthesis

- cd ../02_SYN/
- ./01_run_dc　(合成電路)
- ./09_clean_up (清除合成結果)
  - 合成結果: (不能有Error、要有Area report、Timing report slack met、不能有Latch)

```
Number of ports:                          48
Number of nets:                          185
Number of cells:                         161
Number of combinational cells:           161
Number of sequential cells:                0
Number of macros/black boxes:              0
Number of buf/inv:                        38
Number of references:                     18

Combinational area:               2864.030431
Buf/Inv area:                      379.209614
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  2864.030431
Total area:                 undefined
```

Synthesis

- 合成的timing report中的slack必須≧0 (MET)
- 如果出現timing violation (slack < 0) → Demo Fail

```
Startpoint: in_num0[1] (input port)
Endpoint: out_num1[0]
          (output port)
Path Group: default
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
input external delay                     0.00       0.00 r
in_num0[1] (in)                          0.00       0.00 r
U250/Y (INVXL)                           0.06       0.06 f
U166/Y (AOI222XL)                        0.58       0.64 r
U218/Y (AOI222XL)                        0.34       0.98 f
U307/Y (AOI222XL)                        0.58       1.56 r
U308/Y (OAI22X1)                         0.20       1.76 f
U309/Y (AOI31X4)                         0.51       2.27 r
U211/Y (MXI2X1)                          0.25       2.53 f
U205/Y (AOI222X1)                        0.45       2.98 r
U245/Y (AOI222XL)                        0.25       3.22 f
U203/Y (AOI2BB1XL)                       0.34       3.56 f
U253/Y (OAI31XL)                         0.23       3.79 r
U202/Y (OAI2BB1X1)                       0.13       3.92 f
U248/Y (AOI21X1)                         0.24       4.16 r
U201/Y (INVX3)                           0.16       4.32 f
U313/Y (MXI2X1)                          0.24       4.56 f
U197/Y (AOI222X1)                        0.48       5.04 r
U196/Y (AOI222XL)                        0.31       5.35 f
U314/Y (AOI222XL)                        0.45       5.81 r
U195/Y (OAI21XL)                         0.19       5.99 f
U239/Y (AOI2BB1XL)                       0.29       6.29 f
U315/Y (AOI31X1)                         0.28       6.57 r
U316/Y (AOI2BB1X2)                       0.18       6.75 f
U175/Y (INVX2)                           0.19       6.94 r
U275/Y (MXI2XL)                          0.30       7.24 r
U172/Y (INVX1)                           0.13       7.37 f
U185/Y (AOI222X1)                        0.40       7.77 r
U321/Y (AOI222XL)                        0.25       8.01 f
U171/Y (AOI2BB1XL)                       0.33       8.34 f
U183/Y (OAI31XL)                         0.23       8.57 r
U323/Y (OAI2BB1X1)                       0.16       8.73 f
U182/Y (AOI21X2)                         0.35       9.08 r
U170/Y (INVX2)                           0.20       9.28 f
U332/Y (AOI22X1)                         0.72      10.00 r
out_num1[0] (out)                        0.00      10.00 r
data arrival time                                  10.00

max_delay                               10.00      10.00
output external delay                    0.00      10.00
data required time                                 10.00
-----------------------------------------------------------
data required time                                 10.00
data arrival time                                 -10.00
-----------------------------------------------------------
slack (MET)                                        0.00
```

Pass !

```
U875/Y (NAND2X4)                         0.08       5.05 r
U974/Y (NAND3X4)                         0.16       5.21 f
out_n[7] (out)                           0.00       5.21 f
data arrival time                                   5.21

max_delay                                5.00       5.00
output external delay                    0.00       5.00
data required time                                  5.00
-----------------------------------------------------------
data required time                                  5.00
data arrival time                                  -5.21
-----------------------------------------------------------
slack (VIOLATED)                                   -0.21
```

Fail !

Synthesis

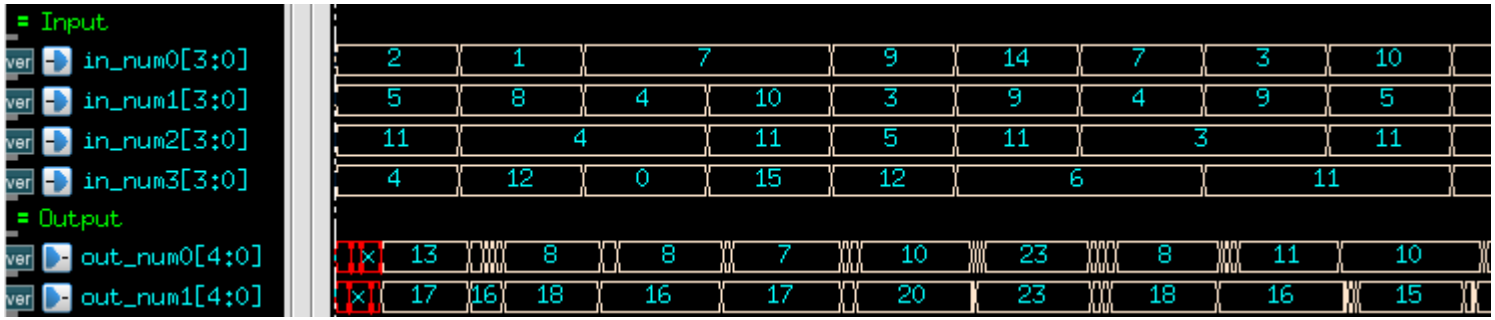
- 記得檢查是否合成出Latch
  - 可以在syn.log用ctrl+F尋找關鍵字Latch
- 如果出現Latch → Demo Fail

```
#=================================================
#  Read RTL Code
#=================================================
read_sverilog {$DESIGN\.sv}
Loading db file '/usr/synthesis/libraries/syn/dw_foundation.sldb'
Loading db file '/usr/synthesis/libraries/syn/standard.sldb'
Loading db file '/RAID2/COURSE/iclab/iclabta01/umc018/Synthesis/slow.db'
Loading db file '/usr/synthesis/libraries/syn/gtech.db'
  Loading link library 'slow'
  Loading link library 'gtech'
Loading sverilog file '/home/RAID2/COURSE/dcs/dcsta02/TA/Lab02/01_RTL/Sort.sv'
Detecting input file type automatically (-rtl or -netlist).
Reading with Presto HDL Compiler (equivalent to -rtl option).
Running PRESTO HDLC
Compiling source file /home/RAID2/COURSE/dcs/dcsta02/TA/Lab02/01_RTL/Sort.sv

Inferred memory devices in process
        in routine Sort line 52 in file
                '/home/RAID2/COURSE/dcs/dcsta02/TA/Lab02/01_RTL/Sort.sv'.
===============================================================================
|    Register Name     | Type  | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|    out_num2_reg      | Latch |   6   |  Y  | N  | N  | N  | -  | -  | -  |
===============================================================================
```

Gate-level simulation

- cd Lab01/03_GATE/
- ./01_run (電路模擬)
- ./09_clean_up (清除波型檔)
- nWave & (看波型)
  - 範例波型:



Upload

- cd ../09_UPLOAD/
- ./01_upload　　(上傳code)
- ./02_download [argument] (下載上傳結果)
  - [argument] = demo1 or demo2
  - 檢查是否上傳成功&正確
- Demo1: 3/3, 16:25:00，Demo2: 3/4, 23:59:59

```
linux01 [Lab02/09_UPLOAD]% ./01_upload

module Sort(
    // Input signals
  :

endmodule
------------------------------------------------------------
The 1st demo deadline is Thu Mar 18 16:25:00 CST 2021 ,
It is Fri Mar 12 18:15:48 CST 2021 now!
It will upload to demo1.
It will overwrite your file if you have uploaded before.
Is this the file you want to upload?(y/n):y
Upload done!
linux01 [Lab02/09_UPLOAD]%
```

```
linux01 [Lab02/09_UPLOAD]% ./02_download demo1
Download done!
```