

## DCS Lab 07 Pattern

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#### Pattern

- 這次Lab寫pattern去測錯誤的design,找到其錯誤
- 這次Lab只需要寫00\_TESTBED/pattern.sv
- lab07\_1.sv代表第一個spec錯誤的design,依此類推。lab07.sv 是正確的design。
- lab07\_x.sv & lab07.sv 都不要動到
- 可以參考之前幾次的pattern和講義

### lab07.sv

Input Signal	Bit Width	Definition
clk	1	10 ns Clock for 1 cycle
rst_n	1	Asynchronous reset when reset negedge, all output should be zero
in_number	4	範圍(-8,7),連續給4個數字。方便之後說 明,分別用in_1、in_2、in_3跟in_4代表
mode	2	幾種運算模式,請看下一頁
in_valid	1	in_valid high when giving number

<b>Output Signal</b>	Bit Width	Definition
out_valid	1	High for 1 cycle
out_result	7	High for 1 cycle,計算後的結果,如下頁 所示

#### mode

需先將input四個數值(in\_1~in\_4)進行排序由小至大,假設以下經過排序後sort\_1最小, sort\_4最大

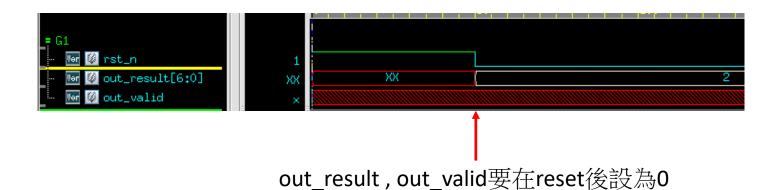
Input signal :mode		
0	out_number = sort_1 + sort_2	
1	out_number sort_2 – sort_1	
2	out_number = sort_4 - sort_3	
3	out_number = sort_1 - sort_4	

# **Specifications**

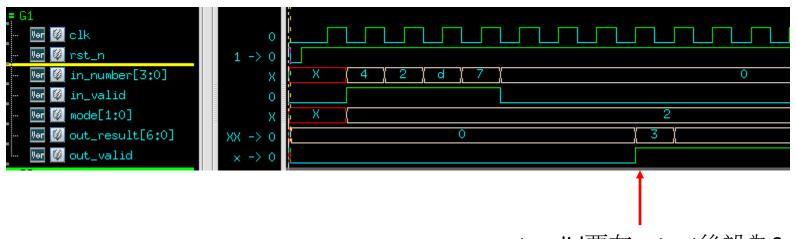
- Top module name : lab07 (File name: lab07.sv)
- Spec1 : reset後output signal要歸零
- Spec2:計算完吐完值後1cycle, out\_valid要歸零 (out\_valid只維持1cycle)
- Spec3: input data 給完之前, out\_valid不能為high
- Spec4: 100cycle內要計算完成(out\_valid為high)
- Spec5: function要對(前一頁的公式會有錯要檢查出來)

• 註:請用random多跑幾組去檢測(建議100以上)

- Waveform SPEC1 error
  - reset後output signal要歸零



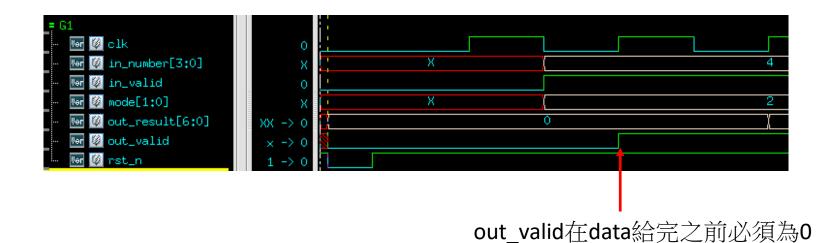
- Waveform SPEC2 error
  - 計算完吐完值後1cycle, out\_valid要歸零(out\_valid只 維持1cycle)



out\_valid要在output後設為0 只能維持1cycle

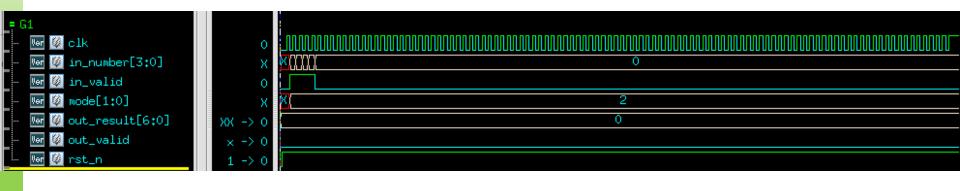
SPEC2! Output should be zero after check

- Waveform SPEC3 error
  - input data 給完之前, out\_valid不能為high



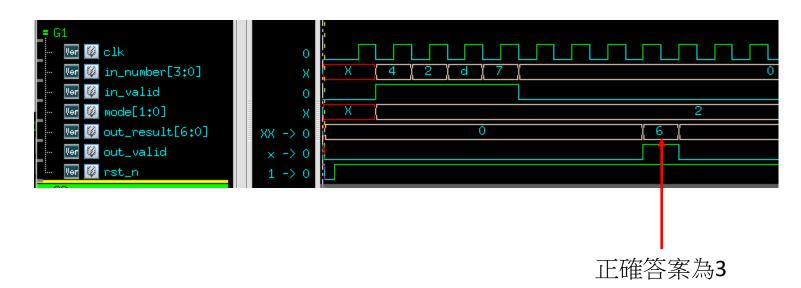
SPEC3!
Outvalid should be zero before give data finish

- Waveform SPEC4 error
  - 100cycle內要計算完成(out\_valid為high)



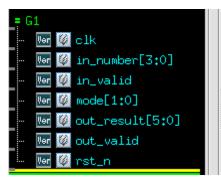
```
SPEC4!
The execution latency are over 100 cycles
```

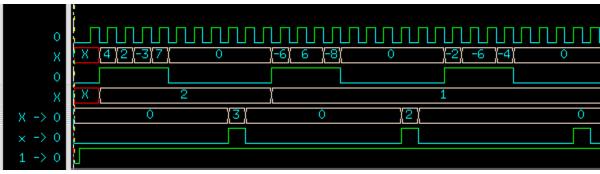
- Waveform SPEC5 error
  - function要對(前幾頁的公式會有錯要檢查出來)



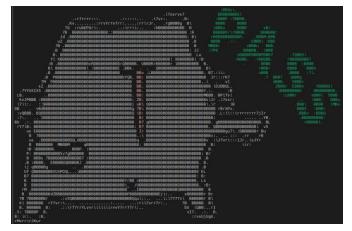
SPEC5!
YOUR: 6
GOLDEN: 3

- Waveform PASS
  - function要對(前幾頁的公式會有錯要檢查出來)





Congratulations!
You have passed all patterns!
time: 1001500 ns



(非必要)

#### Command

- tar -xvf ~dcsta01/Lab07.tar
- ./01\_run\_spec1 : run for check spec1(should display SPEC1 Fail)
- ./01\_run\_spec2 : run for check spec2(should display SPEC2 Fail)
- ./01\_run\_spec3 : run for check spec3(should display SPEC3 Fail)
- ./01\_run\_spec4 : run for check spec3(should display SPEC4 Fail)
- ./01\_run\_spec5 : run for check spec4(should display SPEC5 Fail)
- ./01\_run : run for right design(should display Congratulation)
- You should Pass all spec!

#### Command

請參考pattern.sv裡這段,需要各自秀出
 SPEC1.2.3.4.5等資訊,以免助教demo時抓不到

```
$display ("-----
$display ("
                                                                      SPEC1!
$display ("
$display ("--
$display ("--
                                                                      SPEC2!
$display ("
$display ("
                                                           Output should be zero after check
$display ("--
$display ("---
$display ("
                                                                      SPEC3!
                                                   Outvalid should be zero before give data finish
$display ("
$display ("-------
$display ("-----
                                                                      SPEC4!
$display ("
                                                      The execution latency are over 100 cycles
$display ("
$display ("--
$display ("--
$display ("
                                                                     SPEC5!
$display ("
                                                                     YOUR: %d
                                                                                                                       ',out result)
$display ("
                                                                     GOLDEN: %d
$display ("
```

#### Command

- tar -xvf ~dcsta01/Lab07.tar
- Upload
  - cd 09\_upload
  - ./01\_upload
  - ./02\_download demoX

## Tips

- CYCLE 記得要給值喔~
- 不然模擬會卡住

#### DCS期末考時間調查

 https://docs.google.com/forms/d/1TQUNoeKz\_C yL1bApmBnhDQeGk9n4mLZxjQUUZAaeqc/viewform

