DCS Lab02
Timer

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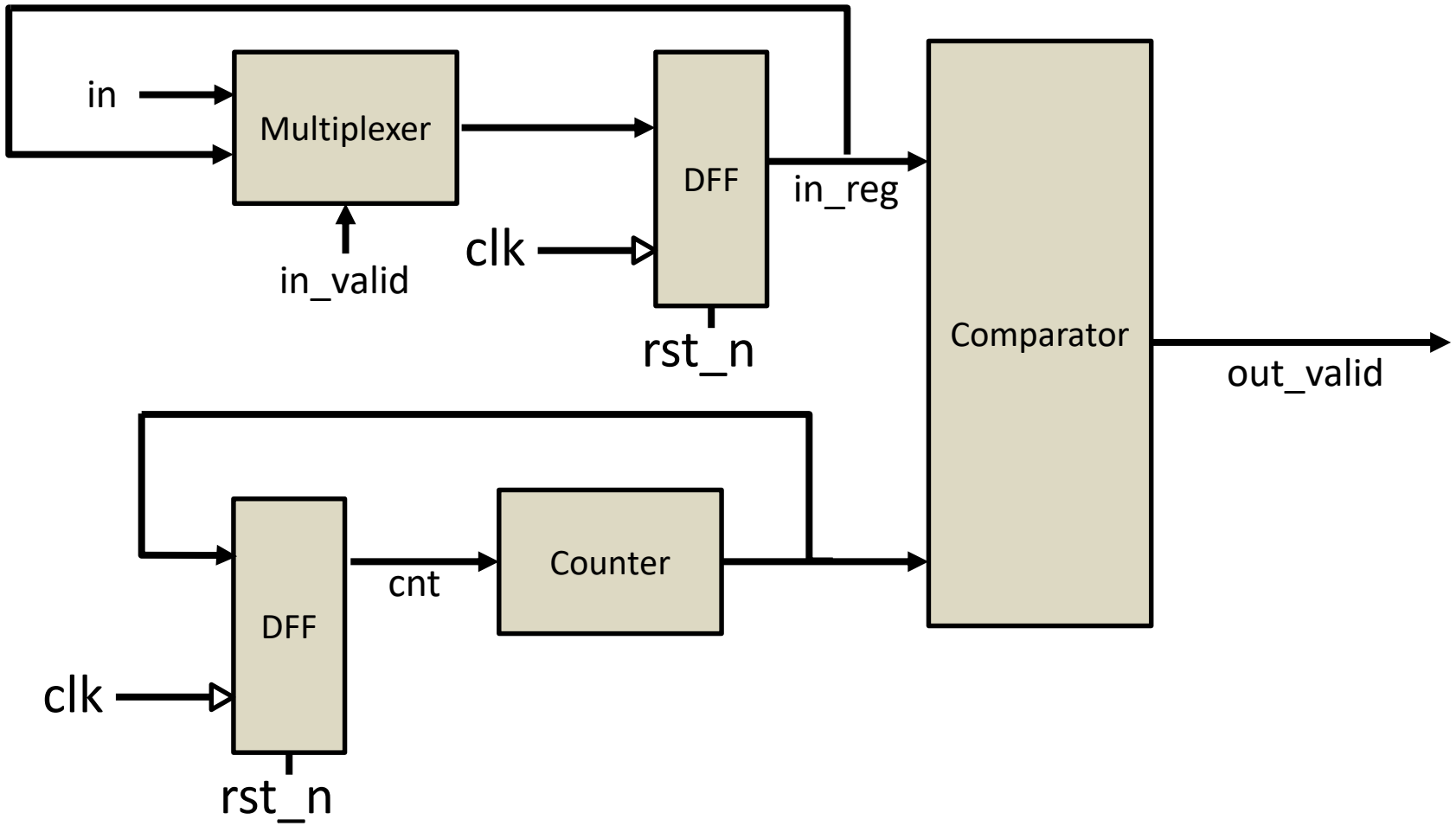
Timer-計時器

- 一開始會輸入rst_n，請將out_valid設為0
  - rst_n變為0時做reset
- 會有一個數字輸入 in, 範圍是1~31
  - 只有當in要輸入的那個cycle才會有數值，其餘時間為0
- 同時會有一個訊號invalid輸入
  - 0: 無動作，1: 輸入in，只會high一個cycle
- 接收到in, in_valid訊號後，開始倒數，過in個cycle後將out_valid拉至high
  - out_valid只能輸出1個cycle
- 下一個要倒數的pattern會在2~5個cycle輸入

Block diagram for your reference



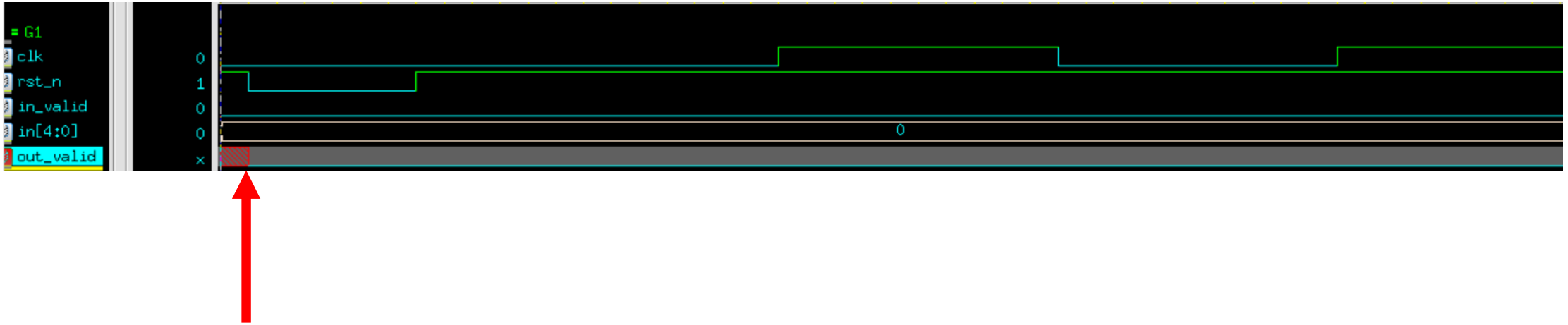
Timer.sv

Input signal	Bit width	Definition
clk	1	10ns clock
rst_n	1	Asynchronous reset 當reset negedge時，out_valid須為0
in_valid	1	Clk負緣時輸入in時，in_valid為1，其餘為0
in	5	Clk負緣時輸入要倒數的cycle數

Output signal	Bitwidth	Definition
out_valid	1	倒數時間到，輸出1，其餘時間為0

Output & Waveform

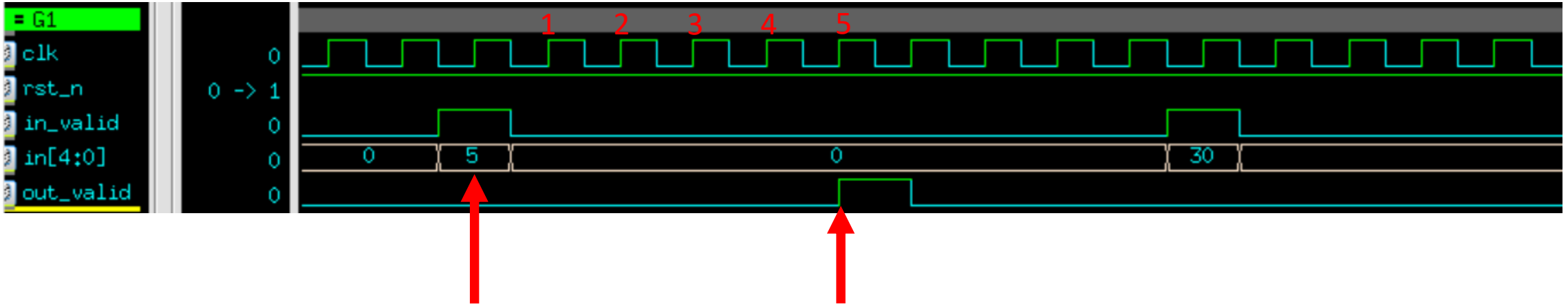
- Reset Waveform



Out_valid要在rst_n負緣時之後設為0， rst_n與clk非同步

Output & Waveform

- Waveform



讀取欲倒數的cycle數　　將out_valid拉為high 1cycle

Command

- tar -xvf ~dcsta01/Lab02.tar
- Need 02_SYN
  - No Latch
  - No error
  - No timing violation (MET)
  - Separate sequential and combinational block

Demo1: 3/10, 16:25:00，Demo2: 3/10, 23:59:59

Separate sequential and combinational block

```
assign XOR = A ^ B;
always_ff @(posedge clk or negedge rst_n) begin
    if(!rst_n) Ans <= 0;
    else Ans <= XOR;
end
```

Good design

```
always_ff @(posedge clk or negedge rst_n) begin
    if(!rst_n) Ans <= 0;
    else Ans <= A ^ B;
end
```

Bad design

Appendix

- 更改訊號進制顯示