KEREN ZHU

2501 Speedway, Austin, TX 78712 ◇ The University of Texas at Austin
keren.zhu@utexas.edu ◇ (608)886-2404 ◇ https://krz.engineer
Postdoctoral Fellow ◇ Department of Electrical & Computer Engineering

RESEARCH INTERESTS

Electronic Design Automation for Custom Circuits

- Physical design automation for analog and mixed-signal circuits
- CAD for emerging technologies

Machine Learning for Electronic Design Automation

EDUCATION

The University of Texas at Austin, TX, USA *Aug. 2016 – June 2022*
Ph.D., Department of Electrical and Computer Engineering
Advisor: David Z. Pan
Dissertation title: *Fully-Automated Layout Synthesis for Analog and Mixed-Signal Integrated Circuits*

University of Wisconsin-Madison, WI, USA *Sep. 2012 – May. 2016*
B.S.E.E. graduated with Highest Distinction, Department of Electrical and Computer Engineering
(GPA 3.97/4.0)
(Rank top 8/819)

PROFESSIONAL EXPERIENCE

The University of Texas at Austin, TX, USA *June 2022 –*
Postdoctoral Fellow

Nvidia Inc., TX, USA *May 2021 – May 2022*
Internship
ASIC and VLSI Research Group: Design Automation

Cerebras System, CA, USA *May 2020 – Oct. 2020*
Internship
Software Stack: Place and Route

Apple, TX, USA *May 2018 – Aug. 2018*
Internship
SOC: Physical Design

RELATED PROJECTS

Machine generated analog IC layout
Open-source tool **MAGICAL** for automatically generate layout for analog and mixed signal circuits [C2, C10, J1, J3]

- https://github.com/magical-eda/MAGICAL

Analytical placement algorithm [C7, C15, C17]
Efficient routing algorithm [C1, C8]
Automated constraint extractions from the netlist with statitical methods [C3, C13, C19]
Netlist-to-GDSII fully automated flow [C5, C10, C14]
Machine-learning guided physical design and analog layout performance modeling [C1, C4, C15, C17, C19]

Machine learning-assisted VLSI CAD
ML in CAD for analog and mixed signal circuits [C1, C4, C13, C17, C19]
ML in logic synthesis [C9]

Efficient and Emerging Computing for ML
Analog computing and emerging devices for neural network acceleration [C10, C18, C21]
Efficient ML framework [C6, C12]

TEACHING

Graduate Teaching Assistant	EE382M: VLSI CAD and Optimization	Fall 2018
Teaching Assistant	ECE230: Circuit Analysis	Fall 2015

MENTORING

Supervised senior undergraduates for capstone project UT, 2021
Title: "MAGICAL: ML for Automated Analog IC Layout"
Mentees: Mina Gawargious, Jason Juliette, Justin Ko and Lang Zhou

Served as mentor for first-year graduate students UT, 2021
UT ECE graduate partner program
Mentees: Gillian Yost, Lekhaj Patha, Yancheng Du and Weiran Huang

SKILLS

Programming Languages
C/C++, Python

EDA Tools
Cadence Innovus, Synopsys Design Compiler, Synopsys Prime Time

AWARDS AND HONORS

Best Student Paper Award Nomination *2021*
IEEE Custom Integrated Circuits Conference (CICC)

Best Paper Award Nomination *2020*
IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)

Harry Philip Whitworth Endowed Graduate Fellowship *2021*
The University of Texas at Austin

Hilldale Undergraduate/Faculty Research Fellowship *2015*
University of Wisconsin-Madison

Hugo Jr. and Pennie Longemann Scholarship *2014*
University of Wisconsin-Madison

Vincent Rideout Scholarship *2013*
University of Wisconsin-Madison

PUBLICATIONS

Journal Papers

[J3] **Keren Zhu**, Hao Chen, Mingjie Liu and David Z. Pan, "Tutorial and Perspectives on MAGICAL: A Silicon-Proven Open-Source Analog IC Layout System," in *IEEE Transactions on Circuits and Systems II*, 2022.

[J2] Hao Chen*, Mingjie Liu*, Xiyuan Tang* **Keren Zhu***, Nan Sun and David Z. Pan, "Challenges and Opportunities Toward Fully Automated Analog Layout Design," in *Journal of Semiconductors*, 2020. (* indicates in alphabetic order, Invited) **Featured on Cover**

[J1] Hao Chen*, Mingjie Liu*, Biying Xu* **Keren Zhu***, Xiyuan Tang, Shaolan Li, Yibo Lin, Nan Sun and David Z. Pan, "MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII," in *IEEE Design & Test*, 2020. (* indicates equal contributions in alphabetic order, Invited)

Conference Papers

[C21] Harrison Jin, Hanqing Zhu, **Keren Zhu**, Thomas Leonard, Mahshid Alamdar, David Z. Pan, and Jean Anne C. Incorvia, "Design of Domain Wall-Magnetic Tunnel Junction Analog Content Addressable Memory using Current and Projected Prototype Data," in *Annual Conference on Magnetism and Magnetic Materials (MMM)*, Minneapolis, MN, October 31 - November 4, 2022. (Under Review)

[C20] Mingjie Liu*, Xiyuan Tang*, **Keren Zhu**, Hao Chen, Nan Sun, and David Z. Pan, "1MS/s and 80MS/s SAR ADCs in 40nm CMOS with End-to-End Compilation," in *IEEE Asian Conference on Solid-State Circuits (ASSCC)*, Taipei, November 6-9, 2022. (* indicates equal contributions in alphabetic order) (Under Review)

[C19] **Keren Zhu**, Hao Chen, Walker Tuner, George Kokai, David Z. Pan and Haoxing Ren, "TAG: Learning Circuit Spatial Embedding From Layouts," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Francisco, CA, July 10-14, 2022. **Best Paper Candidate Nominated from Track** (Accepted)

[C18] Hanqing Zhu, **Keren Zhu**, Jiaqi Gu, Harrison Jin, Ray T. Chen, Jean Anne Incorvia, and David Z. Pan, "Fuse and Mix: ACAM-Enabled Analog Activation for Energy-Efficient Neural Acceleration," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Francisco, CA, July 10-14, 2022. (Accepted)

[C17] **Keren Zhu**, Hao Chen, Mingjie Liu and David Z. Pan, "Automating Analog Constraint Extraction: From Heuristics to Learning," in *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Virtual Conference, January 17-20, 2022. (Invited)

[C16] Ahmet F. Budak*, Zixuan Jiang*, **Keren Zhu**, Azalia Mirhoseini, Anna Goldie, and David Z. Pan, "Reinforcement Learning for Electronic Design Automation: Case Studies and Perspectives," in *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Virtual Conference, January 17-20, 2022. (* indicates equal contributions in alphabetic order)

[C15] **Keren Zhu**, Hao, Chen, Mingjie Liu, Xiyuan Tang, Wei Shi, Nan Sun, and David Z. Pan, "Generative-Adversarial-Network-Guided Well-Aware Placement for Analog Circuits," in *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Virtual Conference, January 17-20, 2022.

[C14] Mingjie Liu, Xiyuan Tang, **Keren Zhu**, Hao Chen, Nan Sun, and David Z. Pan, "OpenSAR: An Open Source Automated End-to-end SARADC Compiler," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Conference, November 1-5, 2021.

[C13] Hao Chen, **Keren Zhu**, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, "Universal Symmetry Constraint Extraction for Analog and Mixed-Signal Circuits with Graph Neural Networks," in *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, December 5-9, 2021.

[C12] Zixuan Jiang, Jiaqi Gu, Mingjie Liu, **Keren Zhu**, and David Z. Pan, "Optimizer Fusion: Efficient Training with Better Locality and Parallelism," in *International Conference on Learning Representations (ICLR) Workshop, Hardware Aware Efficient Training (HAET)*, May 07, 2021.

[C11] Xiangxing Yang, **Keren Zhu**, Xiyuan Tang, Meizhi Wang, Mingtao Zhan, Nanshu Lu, Jaydeep P. Kulkarni, David Z. Pan, Yongpan Liu and Nan Sun, "An In-Memory-Computing Charge-Domain Ternary CNN Classifier," in *IEEE Custom Integrated Circuits Conference (CICC)*, Virtual Event, April 25-30, 2021. **Best Student Paper Award Nomination**

[C10] Hao Chen*, Mingjie Liu*, Xiyuan Tang*, **Keren Zhu***, Abhishek Mukherjee, Nan Sun and David Z. Pan, "MAGICAL 1.0: An Open-Source Fully-Automated AMS Layout Synthesis Framework Verified With a 40-nm 1 GS/s $\Delta\Sigma$ ADC," in *IEEE Custom Integrated Circuits Conference (CICC)*, Virtual Event, April 25-30, 2021. (* indicates equal contributions in alphabetic order)

[C9] **Keren Zhu**, Mingjie Liu, Hao Chen, Zheng Zhao and David Z. Pan, "Exploring Logic Optimizations with Reinforcement Learning and Graph Convolutional Network," in *ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Virtual Event, Iceland, November 16-20, 2020.

[C8] Hao Chen, **Keren Zhu**, Mingjie Liu, Xiyuan Tang, Nan Sun and David Z. Pan, "Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, November 02-05, 2020.

[C7] **Keren Zhu**, Hao Chen, Mingjie Liu, Xiyuan Tang, Nan Sun and David Z. Pan, "Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, November 02-05, 2020. **Best Paper Candidate Nominated from Track**

[C6] Zixuan Jiang, **Keren Zhu**, Mingjie Liu, Jiqi Gu, and David Z. Pan, "An Efficient Training Framework for Reversible Neural Architectures," in *European Conference on Computer Vision (ECCV)*, Glasgow, United Kingdom, August 23-27, 2020.

[C5] Mingjie Liu, **Keren Zhu**, Xiyuan Tang, Biying Xu, Wei Shi, Nan Sun and David Z. Pan, "Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis," in *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, July 19-23, 2020.

[C4] Mingjie Liu*, **Keren Zhu***, Jiqi Gu, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, "Towards Decrypting the Art of Analog Layout: Placement Quality Prediction via Transfer Learning," in *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France, Mar. 09-13, 2020. (* indicates equal contributions in alphabetic order)

[C3] Mingjie Liu, Wuxi Li, **Keren Zhu**, Biying Xu, Yibo Lin, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, "S^{3}DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity," in *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Beijing, China, January 13-16, 2020. **Best Paper Award Nomination**

[C2] Biying Xu, **Keren Zhu**, Mingjie Liu, Yibo Lin, Shaolan Li, Xiyuan Tang, Nan Sun and David Z. Pan, "MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, USA, November 4-7, 2019. (Invited)

[C1] **Keren Zhu**, Mingjie Liu, Yibo Lin, Biying Xu, Shaolan Li, Xiyuan Tang, Nan Sun and David Z. Pan, "GeniusRoute: A New Routing Paradigm Using Generative Neural Network Guidance for Analog Circuits," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, USA, November 4-7, 2019. **Best Paper Candidate Nominated from Track**

PROFESSIONAL SERVICE

Reviewer

IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)

IEEE Transaction on Artificial Intelligence (TAI)

ACM/IEEE Design Automation Conference (DAC)

IEEE/ACM International Conference on Computer-Aided Design (ICCAD)

Neural Information Processing Systems (NeurIPS)

IEEE International Symposium on Low Power Electronics and Design (ISLPED)