KEREN ZHU

2501 Speedway, Austin, TX 78712 \diamond The University of Texas at Austin keren.zhu@utexas.edu \diamond (608)886-2404 \diamond https://krz.engineer PhD student \diamond Department of Eletrical & Computer Engineering

RESEARCH INTERESTS

Optimization in VLSI CAD

- Physical design in VLSI CAD
- CAD for Analog and mixed signal circuits

EDUCATION

University of Texas at Austin, TX, USA

Aug. 2016 -

Ph.D. student, Department of Electrical and Computer Engineering

Advisor: David Z. Pan

(GPA 3.79/4.0)

University of Wisconsin-Madison, WI, USA

Sep. 2012 - May. 2016

B.S.E.E. graduated with Highest Distinction, Department of Electrical and Computer Engineering

(GPA 3.97/4.0)(Rank top 8/819)

PROFESSIONAL EXPERIENCE

Nvidia Inc., Austin, USA

May 2021 - Aug. 2021

Internship

ASIC and VLSI Research Group: Design Automation

Cerebras System, Palo Alto, USA

May 2020 - Oct. 2020

Internship

Software Stack: Place and Route

Apple, Austin, USA

May 2018 - Aug. 2018

Internship

SOC: Physical Design

TEACHING EXPERIENCE

Graduate Teaching Assistant Teaching Assistant EE382M: VLSI CAD and Optimization

Fall 2018

ECE230: Circuit Analysis

Fall 2015

RELATED PROJECTS

Machine generated analog IC layout

Open-source tool MAGICAL for automatically generate layout for analog and mixed signal circuits [C2, C10, J1]

• https://github.com/magical-eda/MAGICAL

Analytical placement algorithm [C7]

Efficient routing algorithm [C1, C8]

Automated constraint extractions from the netlist with statitical methods [C3, C13]

Netlist-to-GDSII fully automated flow [C5, C10]

Machine-learning guided physical design and analog layout performance modeling [C1, C4]

Machine learning-assisted VLSI CAD

ML in CAD for analog and mixed signal circuits [C1, C4, C13]

ML in logic synthesis [C9]

Efficient and Emerging Computing for ML

Analog computing for ML [C10]

Efficient ML framework [C6, C12]

RELATED COURSES

Prof. David Pan • EE382M: Optimization Issues in VLSI CAD • EE382M: VLSI I Prof. Jacob Abraham • EE382M: VLSI II Prof. Mark McDermott • EE382M: VLSI Testing Prof. Nur Touba • EE382M: Analog IC design Prof. Nan Sun • EE382M: VLSI Physical Design Automation Prof. David Pan • EE360C: Algorithms Prof. David Soloveichik • CS388G: Algorithms: Techniques and Theory Prof. Greg Plaxton • ORI391Q: Integer Programming Prof. Jonathan Bard Prof. Scott Niekum and Prof. Peter Stone • CS394R: Reinforcement Learning: Theory and Practice • EE382M: Verification of Digital Systems Prof. Jacob Abraham

Prof. Constantine Caramanis

SKILLS

Programming Languages

C/C++, Python

EDA Tools

Cadence Innovus, Synopsys Design Compiler, Synopsys Prime Time

• EE381V: Polyhedral Combinatorial Optimization

AWARDS AND HONORS

Hilldale Undergraduate/Faculty Research Fellowship	University of Wisconsin-Madison	2015
Hugo Jr. and Pennie Longemann Scholarship	University of Wisconsin-Madison	2014
Vincent Rideout Scholarship	University of Wisconsin-Madison	2010

PUBLICATIONS

Journal Papers

- [J2] Hao Chen*, Mingjie Liu*, Xiyuan Tang* **Keren Zhu***, Nan Sun and David Z. Pan, "Challenges and Opportunities Toward Fully Automated Analog Layout Design," in *Journal of Semiconductors*, 2020. (* indicates in alphabetic order, Invited) **Featured on Cover**
- [J1] Hao Chen*, Mingjie Liu*, Biying Xu* **Keren Zhu***, Xiyuan Tang, Shaolan Li, Yibo Lin, Nan Sun and David Z. Pan, "MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII," in *IEEE Design & Test*, 2020. (* indicates equal contributions, Invited)

Conference Papers

- [C13] Hao Chen, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, "Universal Symmetry Constraint Extraction for Analog and Mixed-Signal Circuits with Graph Neural Networks," in ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, December 5-9, 2021. (Accepted)
- [C12] Zixuan Jiang, Jiaqi Gu, Mingjie Liu, **Keren Zhu**and David Z. Pan, "Optimizer Fusion: Efficient Training with Better Locality and Parallelism," in *International Conference on Learning Representations (ICLR) Workshop, Hardware Aware Efficient Training (HAET)*, May 07, 2021.
- [C11] Xiangxing Yang, Keren Zhu, Xiyuan Tang, Meizhi Wang, Mingtao Zhan, Nanshu Lu, Jaydeep P. Kulkarni, David Z. Pan, Yongpan Liu and Nan Sun, "An In-Memory-Computing Charge-Domain Ternary CNN Classifier," in *IEEE Custom Integrated Circuits Conference (CICC)*, Virtual Event, April 25-30, 2021. (Accepted) Best Student Paper Award Nomination

- [C10] Hao Chen*, Mingjie Liu*, Xiyuan Tang*, Keren Zhu*, Abhishek Mukherjee, Nan Sun and David Z. Pan, "MAGICAL 1.0: An Open-Source Fully-Automated AMS Layout Synthesis Framework Verified With a 40nm 1 GS/s ΔΣ ADC," in *IEEE Custom Integrated Circuits Conference (CICC)*, Virtual Event, April 25-30, 2021. (* indicates, equal contributions in alphabetic order)
- [C9] Keren Zhu, Mingjie Liu, Hao Chen, Zheng Zhao and David Z. Pan, "Exploring Logic Optimizations with Reinforcement Learning and Graph Convolutional Network," in ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), Virtual Event, Iceland, November 16-20, 2020.
- [C8] Hao Chen, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun and David Z. Pan, "Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits," in IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Virtual Event, November 02-05, 2020.
- [C7] Keren Zhu, Hao Chen, Mingjie Liu, Xiyuan Tang, Nan Sun and David Z. Pan, "Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow," in IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Virtual Event, November 02-05, 2020. Best Paper Candidate Nominated from Track
- [C6] Zixuan Jiang, Keren Zhu, Mingjie Liu, Jiqi Gu, and David Z. Pan, "An Efficient Training Framework for Reversible Neural Architectures," in European Conference on Computer Vision (ECCV), Glasgow, United Kingdom, August 23-27, 2020.
- [C5] Mingjie Liu, Keren Zhu, Xiyuan Tang, Biying Xu, Wei Shi, Nan Sun and David Z. Pan, "Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis," in ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, July 19-23, 2020.
- [C4] Mingjie Liu*, **Keren Zhu***, Jiqi Gu, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, "Towards Decrypting the Art of Analog Layout: Placement Quality Prediction via Transfer Learning," in *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France, Mar. 09-13, 2020. (* indicates equal contributions)
- [C3] Mingjie Liu, Wuxi Li, **Keren Zhu**, Biying Xu, Yibo Lin, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, "S³DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity," in *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Beijing, China, January 13-16, 2020. **Best Paper Award Nomination**
- [C2] Biying Xu, Keren Zhu, Mingjie Liu, Yibo Lin, Shaolan Li, Xiyuan Tang, Nan Sun and David Z. Pan, "MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence," in IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Westminster, CO, USA, November 4-7, 2019. (Invited)
- [C1] Keren Zhu, Mingjie Liu, Yibo Lin, Biying Xu, Shaolan Li, Xiyuan Tang, Nan Sun and David Z. Pan, "GeniusRoute: A New Routing Paradign Using Generative Neural Network Guidance for Analog Circuits," in IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Westminster, CO, USA, November 4-7, 2019. Best Paper Candidate Nominated from Track

PROFESSIONAL SERVICE

Reviewer

IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)

ACM/IEEE Design Automation Conference (DAC)

IEEE/ACM International Conference on Computer-Aided Design (ICCAD)

IEEE International Symposium on Low Power Electronics and Design (ISLPED)