Performance-Driven Analog Layout Automation: Current Status and Future Directions

(Invited Paper)

Peng Xu, Jintao Li, Tsung-Yi Ho, Bei Yu and Keren Zhu*
CSE Department, The Chinese University of Hong Kong, Hong Kong SAR, China

***Abstract*—Optimizing circuit performance presents a pivotal challenge in the realm of automatic analog physical design. The intricacy of analog performance arises from its sensitivity to layout implementation, frequently lacking a viable approach for direct optimization. This talk initiates with a comprehensive overview of the present challenges and the techniques currently in use. The emphasis will be laid on the recent advancements in employing black-box optimization for enhancing analog performance. Subsequently, we will delve into a detailed case study and analysis of post-layout performance distribution for a typical analog circuit. This study will showcase various layout implementations generated by the open-source analog layout generator, MAGICAL. Future directions will be discussed based on the case study.**

I. Introduction

In the realm of electronics, the design layout for analog integrated circuits (ICs) has traditionally heavily relied on manual processes. This dependence has emerged as a significant bottleneck in the modern IC design cycle, delaying both innovations and product releases. Although recent academic advancements in electronic design automation (EDA) have shown promising progress in automating analog layout design.

Recent trends in analog layout automation research heavily focus on demonstrating an end-to-end flow. Conventionally, research in academic analog place-and-route (PNR) algorithms often targets the optimization of proxy objectives, such as wire length and area [1]. Such an approach fails to reveal the capability of the automation algorithms for important metrics such as performance and manufacturability. Modern analog layout generation frameworks complete the layout generation flow and can demonstrate their effectiveness through post-layout simulation and validation. There are template-based methods, such as BAG [2] and LAYGO [3], [4], which utilize user-defined layout patterns or floorplans to implement the layout. Several studies propose the use of digital PNR tools to complete the physical design [5], [6]. These approaches either have limitations in the circuit architecture or require extensive manual efforts. Analog PNR-based layout generation, on the other hand, provides a fully automated solution where the physical design process is treated as an optimization process. MAGICAL [7], [8] and ALIGN [9] are two representative open-source analog PNR software tools, both incorporating machine learning (ML) techniques to enhance their capabilities [10]. The success of these automation methods has been demonstrated in various silicon tapeouts, including template-based methods [11]–[15], digitally synthesized methods [16], and PNR methods [17], [18]. However, a general and effective approach to considering post-layout circuit performance remains an open question.

* Corresponding author: kerenzhu@cse.cuhk.edu.hk

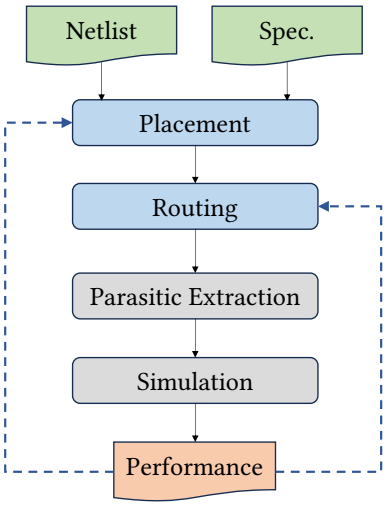

Fig. 1: Typical analog physical design flow. Performance-driven analog physical design needs to consider post-layout circuit performance in the placement and routing stages.

Analog circuit performance is highly sensitive to layout intricacies and can be adversely affected by layout parasitics, coupling, and noise. Manual design often relies on experience, design expertise, and trial-and-error to search for a satisfactory layout. Template-based automation also encounters challenges and may require human efforts to design and adjust the layout templates. In contrast, automatic PNR algorithms intrinsically optimize the layout design and have the potential to create a fully automated, performance-driven automation paradigm. Nevertheless, evaluating and optimizing performance remains a challenge.

Evaluating post-layout analog circuit performance typically involves parasitic extraction and simulations after the layout implementation. Figure 1 illustrates a typical physical design flow for analog ICs. Given a netlist and design specifications, a placer determines the device locations and creates their physical implementation in the chip layout. Subsequently, a

router implements the interconnect based on the placement solution. Parasitics from the resulting layout are extracted, and simulations are conducted on the extracted netlist to assess post-layout performance. The parasitic extraction and simulation processes are often complex, and their explicit calculations are not practical. Furthermore, analog circuits exhibit diverse architectures and various performance metrics. It is commonly assumed that a universal performance model, akin to the static timing model used in digital designs, is unavailable in the analog IC domain [19]. The challenge of evaluating and modeling post-layout analog performance persists, making performance-driven analog physical design an unresolved issue.

In this paper, we provide a comprehensive overview of the current state and offer our insights into performance-driven analog physical design. We introduce related research on this topic, encompassing both conventional approaches and recent advancements (Section II). We also present several case studies along with their analysis, focusing on analog performance in automatically generated analog layouts, using the open-source analog layout generator MAGICAL [7] (Section III). Subsequent to the analysis, we present our perspectives on future directions in this field (Section IV). Finally, we conclude the paper in Section V.

II. Related Work

Analog physical design has been a well-established field for decades. ILAC [20], one of the early initiatives in automating analog layout generation, explored the use of PNR algorithms to optimize analog layout. ILAC incorporates an optimization-based layout generator called MOSAIC, which employs a simulated annealing algorithm to place layout modules and route the design. Over time, this methodology has been extended to accommodate various technologies and constraints. However, in traditional approaches, performance optimization is not directly addressed; instead, it is indirectly achieved through the optimization of proxy objectives. Section II-A provides a concise overview of these conventional techniques in analog physical design. Furthermore, Section II-B delves into existing methods that focus on performance-aware analog physical design, highlighting the evolution of strategies in this domain. With the advent and advancement of machine learning (ML) techniques, a new challenge has emerged in modeling performance during the PNR process. Section II-C introduces this aspect of analog performance modeling, emphasizing its significance and the novel opportunities it presents for advancing analog physical design.

A. Conventional analog physical design

Conventional analog PNR formulations rely on geometric constraints to meet performance requirements. In essence, the problem formulation is akin to digital PNR, with the incorporation of supplementary geometric constraints.

Analog placement often resembles a floorplan problem, where multiple modules must be arranged within a plane. Typically, the algorithm's objective is to optimize area and wire length while adhering to analog placement constraints. Symmetry constraints have played a crucial role in analog layout design, ensuring the symmetrical placement of specific cells, as observed in early research [20]–[22]. Various extensions to this concept include symmetry islands [23], which group symmetry devices, common-centroid layouts [24], and array-like module arrangements for regularity [25], [26]. To minimize parasitics, proximity constraints [24], [27] and boundary constraints [28], [29] are also employed, which serve to reduce wire lengths.

Routing in analog design also introduces additional constraints beyond the standard routing formulation. Symmetry pair routing constraints are widely adopted in this context [21], [30]–[40]. Other works focus on forbidding routing over the active regions of transistors [31], [33], optimizing power routing [41], [42], and proposing methods for shielding critical nets [36]. Exact routing is proposed to match the interconnect parasitic between two nets [43], [44]. This approach necessitates that the pair of wire lengths be the same for every layer so that the wiring parasitics are precisely matched. In contrast, Chen et al. [38] propose to maximize the degree of symmetry even without an explicit symmetry constraint.

Optimization-based PNR methods have greatly facilitated numerous demonstrations of automatically generated analog layouts. A comprehensive survey of related methods can be found in [45]. However, it's important to note that the constraints and objectives employed in these methods do not guarantee post-layout circuit performance.

B. Recent Developments in Performance-aware Analog Physical Design

In addition to advancements in algorithmic improvements over conventional problem formulations [26], [38], [40], [46]–[49], there has been a growing interest in performance-aware analog physical design within many studies.

Several studies have concentrated on minimizing wire load in routing [35], [50]. The proposed methods enable planar routing [35] or incorporate routing considerations into incremental placement [50], aiming to reduce VIA usage. These approaches align with traditional physical design objectives, emphasizing wire length and VIA count minimization. Similar practices involve enforcing a monotonic direction for placement along current flows, as investigated in [51]–[54]. Building upon this concept, some studies explicitly consider critical signal flows, as demonstrated in [48], which presents a signal flow-aware framework for analog and mixed-signal placement, showcasing performance improvements in post-layout analysis. These additional constraints and objectives enrich the conventional problem formulation, although their primary focus is not direct performance optimization.

Some research has focused on mitigating layout-dependent effects (LDE) and thermal effects that could adversely impact performance. For instance, in [55]–[57], placement techniques are proposed to reduce LDEs, such as the well proximity effect (WPE), length of diffusion (LOD), and oxide-to-oxide spacing effect (OSE). The WPE is also directly related to the

well island generation problem, which has been studied in the placement stage [58]–[60]. Additionally, thermal effects are considered in analog placement [61], [62], aiming to prevent performance degradation caused by these related effects. However, while these methods address specific challenges, they do not provide a comprehensive methodology for performance preservation in general.

To establish a general methodology for ensuring performance, researchers have explored the use of machine learning (ML) techniques to extend the retargeting approach into general layout synthesis. Retargeting typically involves extracting geometric constraints from manual layouts to form layout templates. These resulting layout templates can generate new layouts with different technologies and sizing, preserving the structures present in manual designs to maintain performance [63]. However, this method cannot be used for unseen designs. To bridge this gap, several methods have leveraged ML modeling. Zhu et al. [37] propose the use of generative ML models to learn design strategies from manual layouts. They train a variational autoencoder (VAE) model to predict the routing regions chosen by designers. These predicted routing regions are then translated into routing guidance that an automatic detailed router can follow to produce human-like routing solutions. This learned knowledge can be applied to unseen designs, thus extending the retargeting idea into general automatic layout synthesis. Similarly, in [60], a generative adversarial network (GAN) is employed to learn manual well design and integrate this knowledge into automatic placement. Another approach, presented in [64], uses VAE in analog primitive cell layout synthesis tasks. These "learn-from-human" methods offer an approach to preserving performance in analog physical design. However, they also face challenges related to small dataset sizes and the absence of direct performance optimization.

With the availability of an end-to-end layout generation flow, it has become possible to directly optimize post-layout performance. In the work presented in [65], the approach treats layout generation and performance evaluation as a black box and employs Bayesian optimization (BO) to directly optimize post-layout performance. In this method, net weights are considered as input parameters, and BO is utilized to optimize performance with respect to these net weights. This workflow automatically explores different placements and identifies those that yield good performance. As a result, this framework can effectively discover high-quality layouts. However, due to the slow nature of the simulations involved, the method may have limitations in terms of runtime efficiency and may be best suited for smaller circuits.

C. Machine Learning-Based Analog Performance Modeling

Conducting extraction and simulation within the optimization loop is expensive and inefficient. A potential solution is to employ ML-based performance modeling. Optimizing a neural network output can be much more efficient.

The recent progress focuses on modeling post-layout performance from the placement stage. The work [19] proposes a method that utilizes machine learning to predict performance with various placement solutions. It leverages MAGICAL [7] to generate tens of thousands of different placements for the same circuit. These placements are extracted into several images, and a convolutional neural network is employed to predict the corresponding performance based on these images. The model demonstrates transferability between different schematic designs. Subsequently, the accuracy of this model is further enhanced through neural network architecture search [66].

Several efforts have been made to employ prediction models to enable performance-driven automatic analog placement. The work [67] introduces a performance-driven analog placement approach based on wire length estimation derived from star models. However, it may suffer from inaccuracies because it does not use actual layout data for training and may face challenges in transferring the model between different circuits. In contrast, the work [46] addresses a similar learning problem as [19], where the labels are simulated performance data. It employs a graph neural network model as the underlying machine learning architecture, which can produce predictions that are transferable between different designs. This approach combines a simulated annealing-based placement framework that optimizes the predicted performance, allowing for direct performance optimization.

III. Case Study on MAGICAL-Generated Layouts

A. Introduction to the Analog Performance Modeling Lifecycle

In the performance modeling of analog circuits, an aspect that is often overlooked is the time required for various stages in the modeling lifecycle. We divide the analog performance modeling cycle into three stages: data acquisition, model training, and performance-aware PNR inference.

The data acquisition stage includes PNR and parasitic parameter extraction (PEX), as well as post-layout performance simulation (Post-Sim). The PNR stage is often completed with a single layout design, while post-layout performance simulation is carried out along with the PEX process. The layout obtained from PNR is typically used as the input $\boldsymbol{x}$ for performance modeling, while the post-layout performance results serve as the corresponding labels $\boldsymbol{y}$.

Figure 2 presents a case study focusing on the lifecycle for building a performance model on Operational Transconductance Amplifier (OTA) layout design. The first significant observation is that the data collection time occupies most of the performance modeling lifecycle, while the training and inference time only account for a small portion. The training and inference time comprise only 7.11% of the entire lifecycle, while data collection time accounts for 92.89%. Data collection becomes a significant bottleneck in the entire lifecycle.

The second important observation is that the time required to obtain model inputs is much smaller compared to the time required to obtain model labels. The time required to obtain labels through the PEX and Post-Sim stage, as shown in Figure

1, is roughly equivalent to the time it takes to perform 3-4 PNR iterations.

These two observations provide us with important insights. By reducing the time spent on data acquisition, especially PEX and Post-Sim, we can effectively shorten the performance modeling lifecycle. On the one hand, from recent advancements in hardware-accelerated EDA workflows [68], [69], we can see that parallelizing PEX and Post-Sim is an effective solution. On the other hand, by considering the cost of acquiring data inputs and labels, selecting representative samples through active learning [70] may also be an economically efficient approach.

B. Exploring Model Transferability in Performance Modeling on OTA Designs

The transferability of performance models is a widely discussed topic in analog performance modeling. Even if the implemented functionalities are similar, the topology design and transistor sizes may vary. Due to the scarce cost of obtaining labels, it is natural to consider transferring performance models from one dataset to another for inference.

In the case shown in the Table I, we quantitatively discuss the issue of performance model transferability on OTA designs. We mainly consider two scenarios: transfer between the same topology with different sizing configurations and transfer between different topologies. We verify two scenarios of performance model construction, namely **From Scratch** and **Transfer**.

From Scratch: If there is no available layout data for the current design, we propose obtaining a small amount of sampling data. We then model the prediction of the model as a binary classification problem and use balanced sampling to enable the model to achieve accurate predictions with a small amount of data, as in [71].

Transfer: Another way is to leverage the transferability of the pre-trained model obtained from other designs. In this way, we can obtain a relatively accurate model with a few samples through fine-tuning, which requires less time.

From these data results, we can identify two important findings. Overall, the accuracy of the transferred models is reliable. Compared to training from scratch, which requires more data collection time, the accuracy reduction ranges from 3% to 22%. However, there are still cases where the model performance deviates. This is because the transferability of the models varies under different scenarios and metrics. Transfer between different sizing configurations is often easier than transfer between different topologies. Different topologies and sizing settings result in different performance distributions in the layout, which can cause the transfer to fail.

On the one hand, from a generalization perspective, we consider how to improve transfer training by obtaining effective pretraining weights using methods like meta-learning [72]. On the other hand, from a detection perspective, we consider different distributions to determine when transfer is possible. Current research on out-of-distribution (OOD) detection [73] provides technical support for identifying when the model is effective.

TABLE I: Placement prediction results with collected data for training from scratch and transfer learning results.

Design	Prediction Accuracy Metrics	From Scratch	Transfer	Acc-Δ
OTA1	Offset Voltage(%)	**95.54**	91.67	3.87
	CMRR(%)	**91.96**	77.68	14.29
	BandWidth(%z)	**96.43**	95.54	0.89
	DC Gain(%)	**93.62**	88.01	5.61
	Noise(%)	**91.96**	79.14	12.82
OTA2	Offset Voltage(%)	**81.35**	65.39	15.96
	CMRR(%)	**82.33**	62.02	20.31
	BandWidth(%)	**80.71**	72.14	8.58
	DC Gain(%)	**81.35**	59.50	21.85
	Noise(%)	**88.80**	69.29	19.52

C. Navigating the Multi-Objective Pitfall in Post-Layout Performance Optimization

In this case, we aim to demonstrate the importance of multi-objective optimization by comparing the placements obtained through weighted-based Bayesian optimization (BO) and multi-objective optimization Bayesian optimization (MOBO) [74] in four OTA benchmarks.

It is necessary to optimize the layout-related parameters toward different objectives to enhance performance metrics, which improves the overall performance of analog layouts. It is common practice to use a user-defined figure-of-merit (FOM) representation, a weighted sum of post-layout simulation metrics.

However, when it comes to performance-driven analog placement and routing, it becomes necessary to consider the trade-offs between conflicting metrics to achieve the desired layout solutions. It goes beyond what can be accomplished through a simple linear combination. One alternative objective is to find solutions not dominated by others, known as Pareto optimal solutions. The problem of finding Pareto optimal solutions given multiple criteria is called multi-objective optimization.

As shown in Figure 3, the MOBO method outperforms Weighted-BO in terms of the number of top-1 metrics achieved for the obtained layout. MOBO achieves top-1 performance in almost all metrics in Offset Voltage, CMRR, BandWidth, and DC Gain. For all designs, MOBO outperforms the Weighted-BO for 3 to 5 metrics. The results corroborate that the multi-objective optimization method moves the layout solution toward the Pareto frontier.

Recent advancements have been witnessed in the field of multi-objective optimization, especially for gradient-based strategies [75]–[77]. It is imperative to carefully consider how these advancements in the field of multi-objective optimization can be applied to enhance performance-driven analog layout automation.

IV. Perspectives and Future Directions

Our quantitative case study demonstrates important future directions in performance model training and physical design optimization. The need for efficient and performance-

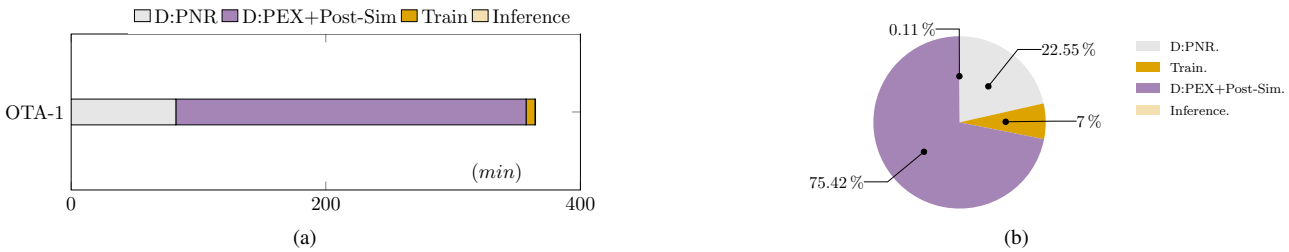

Fig. 2: The runtime breakdown of different methods on OTA1 benchmarks:

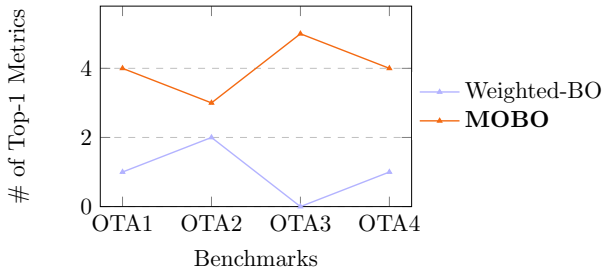

Fig. 3: The number of top-1 metrics for different methods.

driven analog physical design calls for further research. In this section, we give our perspectives on the challenges and opportunities in future research in the field.

A. On Modeling Performance

Efficient Data Acquisition

Data collection is a major bottleneck in building the performance models. Both PEX and Post-Sim cost significant time, which makes the data collection expensive. Efficient data acquisition can benefit the development of analog performance models.

Selecting representative samples can reduce the amount of data needed for the training. Active learning dynamically selects representative samples for the training process [70]. A similar approach can be applied to analog performance data acquisition. By smartly choosing the layouts to be simulated, the performance model training process can be more efficient using fewer samples and, therefore, save costs in running PEX and Post-Sim.

Accelerating the simulation may be beneficial to the data collection. For example, recent studies further accelerate circuit simulation via efficient matrix multiplication [78] and reinforcement learning-based stochastic stepping policy [79]. Faster SPICE simulation can help the performance model training obtain more training data within a limited budget.

Better transferability

Transferring pre-trained models to unseen circuits is crucial in ensuring both accuracy and inference efficiency. As our case studies indicate, the performance models have good transferability between different sizing of the same netlists and slightly slower accuracy for transferring between different typology designs. Increasing the accuracy and the scope of circuits can avoid or reduce costs in finetuning the models in inference time.

Neural network architecture is critical in determining the model performance. One of the challenges in predicting analog performance lies in managing the multimodal input features. These features originate from various stages, such as pre-layout schematics, placement, and routing, and are represented in diverse data formats. Existing research has used a convolutional neural network to process placement information [19] and a graph neural network to extract topology knowledge [80]. A general multimodal neural network for performance modeling may benefit the field.

Adopting a pretraining methodology can further boost the transferability. Analog circuits involve different types, architectures, topologies, and sizing. The circuit performance is also affected by the manufacturing technologies. It would be costly to train individual models separately for each scenario. In [81] proposes to use a "pretrain-then-finetune" approach for increasing data efficiency in layout constraint and parasitic prediction tasks. A similar methodology may apply to layout performance modeling as well.

B. On Optimization Physical Design

Placement and Routing Representation

Representing placement and routing in the ML-enabled performance-driven analog physical design is an overlooked problem. The work [80] treats the performance modeling as a black box. It uses randomized simulated annealing to generate different placements and uses the model to evaluate its performance. In [65], a BO-based framework tunes net weights as a proxy to generate different placements. The net weights decide the priority of different nets and, therefore, impact the resulting layouts. Bridging the placement and routing representation can potentially increase the efficiency of optimization.

Multi-objective optimization

Analog circuit performance is more complicated than digital circuits. Each circuit can have multiple performance metrics. Many of them are competing with the others. The analog design cycle requires efficient optimization given different design specifications. Therefore, efficient and effective multi-objective physical design optimization is essential. As illustrated in the case studies, MOBO can produce higher-quality layouts than a simple weighted-BO strategy. Integrating multi-

objective optimization in the physical design process will be an important future direction in the field.

V. Conclusion

In this paper, we present an overview of the recent developments in performance-aware analog physical design and give our perspectives. Several case studies are conducted using the open-source analog layout generator, MAGICAL, to illustrate the important issues for the problems. The statistical findings highlight the significance of efficiently building ML-based performance models and polishing the optimization algorithms in physical design. Several future directions are suggested based on the case studies.

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