SAAD ISLAM KHAN

Hardware Design & Verification Engineer | BS in Electronics

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EXPERIENCE

Jr. Hardware Engineer

DreamBig Semiconductors Inc.

Esptember 2022

♀ Isb, Pakistan

- Working as an Jr. Design Verification Engineer
- Using Universal Verification Methodology UVM to verify SMART-NIC SOC's Design
- Deep learning of various interconnects and comm-protocols PCIE CXL NIC APB CMN AXI AHB
- Working on environment for stimulus to pass through various comm-protocols and error reporting in "VCS".

Design Verification Training SINES-NUST

June 2022 - August 2022

♀ Isb. Pakistan

- Hands-on System Verilog based verification which includes User defined data type and structures, Interfaces and virtual interfaces, Clocking blocks, Classes, Randomization, Coverage and Mailbox. Verified a memory design using System Verilog through randomized stimulus in System Verilog.
- Created Layered Testbench, generated and drove transactions to DUT, Monitored and Verified with golden results in Scoreboard.
- Hands-on learning and implementation of architecture and flow of transaction in UVM with Cadence Xcelium.

PROJECTS

FPGA Based 7-Segment Rolling Display

- Design included basic design like clock dividers and 7-segment conding, decoding.
- Synthesized the design successfully on FPGA Spartan3

Memeory Read/Write using AHB-Lite Protocol

 Verified a memory module connected to Test-Bench using AHB-Lite protocol by passing stimulus and comparing expected result with actual results.

Smart Home Automation Device

• Used MQTT Protocol to control an Arduino based Home Automation system. Created website and provided remotely accessibility.

Social-Distance Measuring Robot

 Created an Arduino based human following robot for Medical robotics development. It can detect distance between two objects and produce a voice alert to mentain social distance real-time.

EDUCATION

BS-Electronics CUI, Islamabad

2018 - 2022

♀ ISB

HSSC Jinnah Institute of Informatics

2015 - 2017

♀ RWP

SSC St Mark's High School

2003 - 2015

RWI

SKILLS

Verilog SystemVerilog UVM RTL

Linux Synopsis Candence Yaml

Shell-Scripting Git-Lab

Version Control LateX

COURSEWORK

- Digital Logic Design
- Object- Oriented Programming
- Digital System Design
- Computer Architecture
- Electronics I & II
- Circuit Thoery

LANGUAGES

English

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Urdu

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ACHIEVEMENTS

- Completed DV-E Training held at SINES, NUST by 10xEngineers, Dreambig-Semi, AQL-Tech and Impare Inc.
- Got appointed for interview by DreamBig-Semiconductor & 10xEngineers. Recieved Job offers by both. Got hired by DreamBig Semiconductors Inc.