Ferroelectric capacitance and current measurement system

EE344 Project

Team: MON-06

210070045 K S Ahilan
210070096 Yash Udayan Paritkar
210070099 Zala Mayursinh Meghrajsinh
21d070008 Aditya Kumar Roy

Tasks:

Tasks for this project and their brief introduction:

1. Component level testing:
   We test the components to determine whether they perform as expected—moreover, we probe for solutions in case of any error. We will try it again.

2. Cumulative Level Testing:
   We will test the whole setup by arranging them using the breadboard, cable wires, and jumper wires. After all the testing, we would like to remove redundant components. Moreover, iterate this whole process again.

3. Schematic Design:
   We prepare a diagram which shows the pin and components of all components.

4. PCB Design:
   Floor planning of PCB board for components via

5. User Interface Design:
   Prepare a python code to write the observed data into a csv file

6. 3D Design:
   Design a 3D model to house the PCB and FPGA. Done through Autodesk Fusion.

7. PCB Assembling:
   Design PCB for efficient component placement and to avoid heap of wires. Done through Autodesk Fusion.

8. PCB Testing:

Component Level Testing

We will briefly mention the tests and their results below table:

Component	Date	Success/ Failure	Target	Result	Video Link
MAX1184	16/03	S	Sleep mode working Output corresponds to the input voltage	Success	
LD1117	05/03	S	Constant Voltage Output	3.8 V constant voltage	
MAX680	05/03	S	Voltage supply`	Voltage varied with load supplied to it.	PT_MAX680
AD5445					
TPS25200	-	S	Circuit protection		
TL082	07/03	S			

Digital-to-Analog Converter (DAC): AD5445

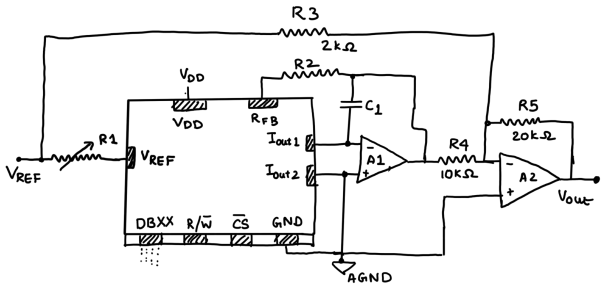
Details from Datasheet:

- *Input*: 2.5V - 5.5V
- *Output*: ∓ 10 V
- *Relative Accuracy*: ± 1 V
  (Also known as endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function.)
-
- 14 bit DAC
- Pins:

Pin Name	**Pin Number**	**Description**
I_{out1}	1	DAC Current O/P

Pin Name	Pin Number	Description
I_{out2}	2	DAC AGND
GND	3	GND
DB	4 - 15	Parallel Data Bits
CS bar	16	Chip Select
R/W	17	Read/Write
V_{DD}	18	Digital Power Supply (2.5 V - 5.5 V)
V_{REF}	19	DAC Reference Voltage Input Terminal
R_{FB}	20	DAC Feedback Resistor

- Theory of operation:
    - Ladder DAC:
    - @Image from Yash_Documentation_sheets
    - We intend to use the circuit in the *Bipolar mode of Operation.*
- **Bipolar Mode of Operation:**



Analog-to-Digital Converter: MAX1184

Details from the datasheet:

- Digital Input: 3 V (typical), 0.3 - 3.6 V (Absolute)
- Analog Single-ended input: ± 1 V
- Maximum Frequency: 20 MHz
- Internal
- Power Dissipation: 100mW
- Pin Table:

Pin Symbol	Pin Number	Description
COM	1	Common-Mode Voltage I/O. Bypass with 0.1 µF

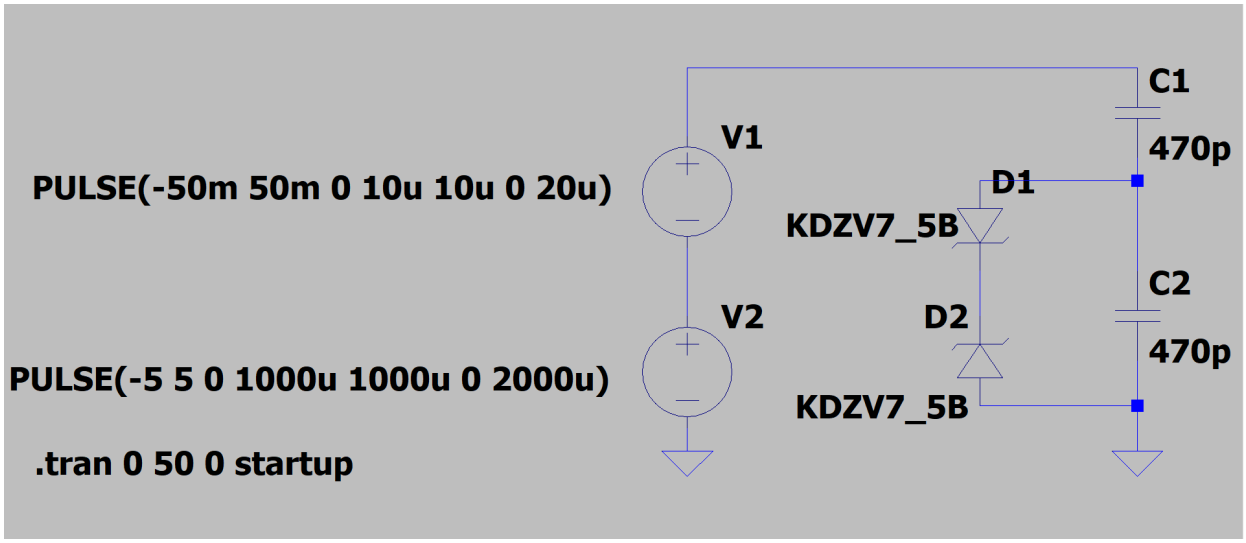
V_{DD}	2, 6, 11, 14, 15	Analog Supply Voltage. Bypass each pin to GND with a 0.1µF capacitor. The analog supply accepts an input range of 2.7V to 3.6V.
GND	3, 7, 10, 13, 16	Analog Ground
INA+	4	Channel A Positive Analog Input. For single-ended operation, connect the signal source to INA+.
INA-	5	Channel A Negative Analog Input. For single-ended operation, connect INA- to COM.
INB-	8	Channel B Negative Analog Input. For single-ended operation, connect INB- to COM.
INB+	9	Channel B Positive Analog Input. For single-ended operation, connect a signal source to INB+.
Clk	2	Clock Input
T/B	17	T/B selects the ADC digital output format. High: Two's complement. Low: Straight offset binary
Sleep	18	Sleep Mode Input. Low: Normal operation, High: It deactivates the two ADCs, leaving the reference bias circuit active.
PD	19	Power-Down Input. High: Power-down mode, Low: Normal operation.
$\overline{OE}$	20	Output Enable Input. High: Digital outputs disabled, Low: Digital outputs enabled
DXB	21 - 30	Three-State Digital Output, Channel B
OGND	31, 34	Output Driver Ground
OV_{DD}	32, 33	Output Driver Supply Voltage. Bypass each pin to OGND with a 0.1µF capacitor. The output driver supply accepts an input range of 1.7V to 3.6V.
DXA	35 - 44	Three-State Digital Output, Channel A with D9A as MSB
REFOUT	45	Internal Reference Voltage Output. It may be connected to REFIN through a resistor or a resistor divider.
REFIN	46	Reference Input. VREFIN = 2 x (VREFP - VREFN). Bypass to GND with a >1nF capacitor.
REFP	47	Positive Reference Input/Output. Conversion range is ± (VREFP - VREFN). Bypass to GND with a > 0.1µF

		capacitor.
REFN	48	Negative Reference Input/Output. Conversion range is ± (VREFP - VREFN). Bypass to GND with a > 0.1µF capacitor.
EP	-	Exposed Pad. Connect to analog ground.

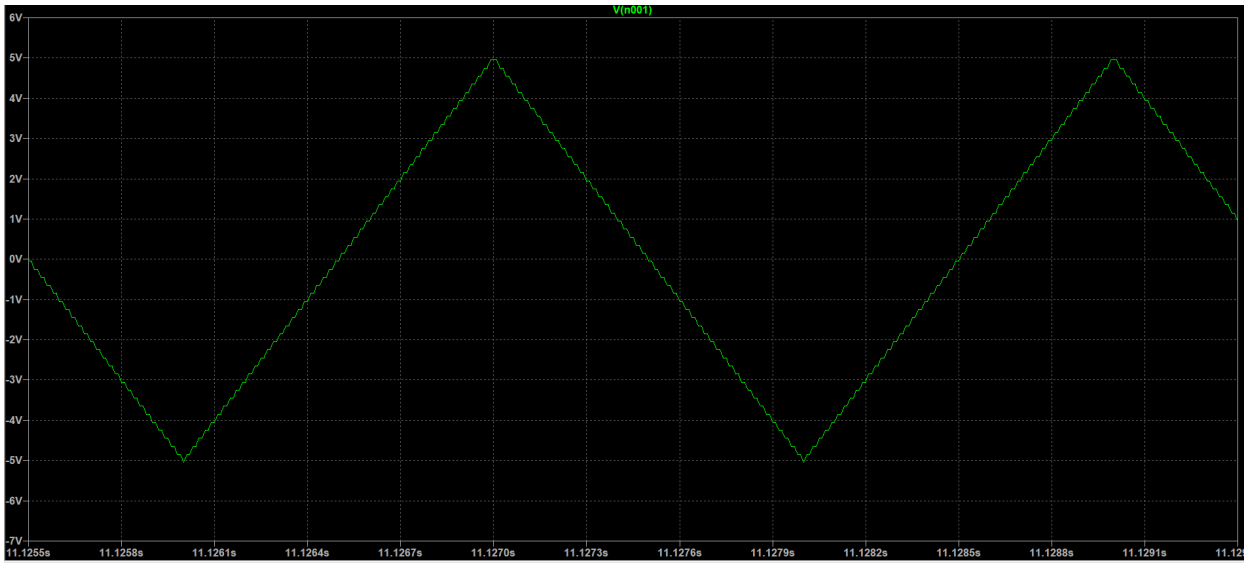
- Grounding, Bypassing and Board Layout
  - Locate all bypass capacitors as close to the device as possible, preferably on the same side as the ADC.
  - V_{DD}, REFP, REFN and COM 2 x 0.1 μF and 22 μF (bipolar) to GND
  - Use split around the plane to match the physical location or analog ground (GND) and digital output driver ground (OGND)on the ADC package
  - Join two ground at a port along the gap by 1 Ω - 8 Ω.
  - Keep high-speed digital signals away from analog.

- Theory:
  - Nine stages of fully differential pipelined architecture
  - @Image from the paper
  - 5-clock cycle latency
  - Three modes: Internal, Buffered external, unbuffered external

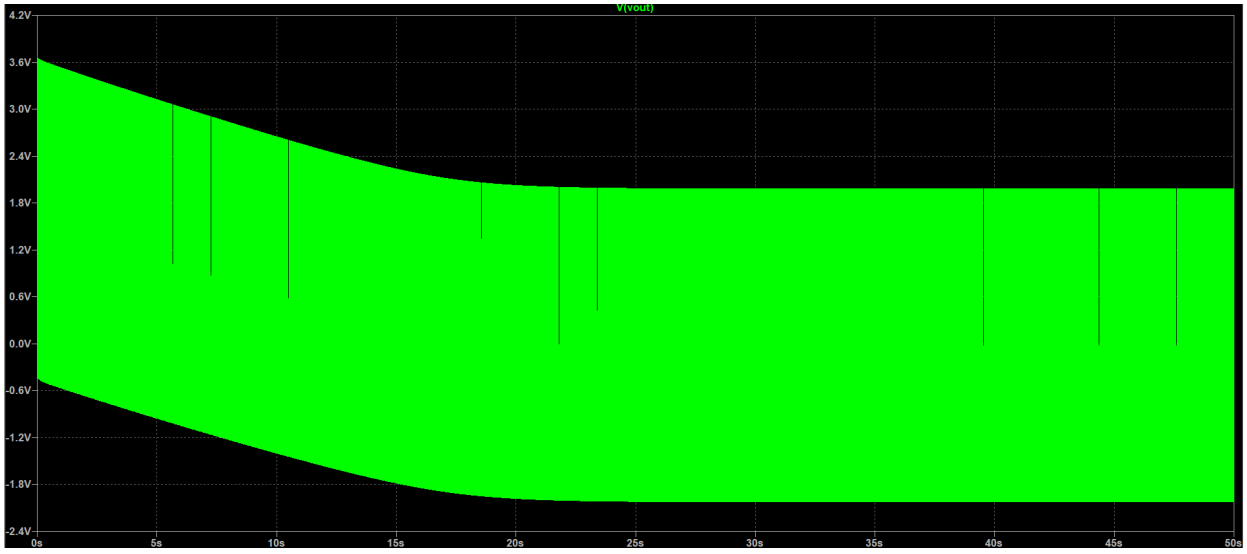
LTspice Simulation



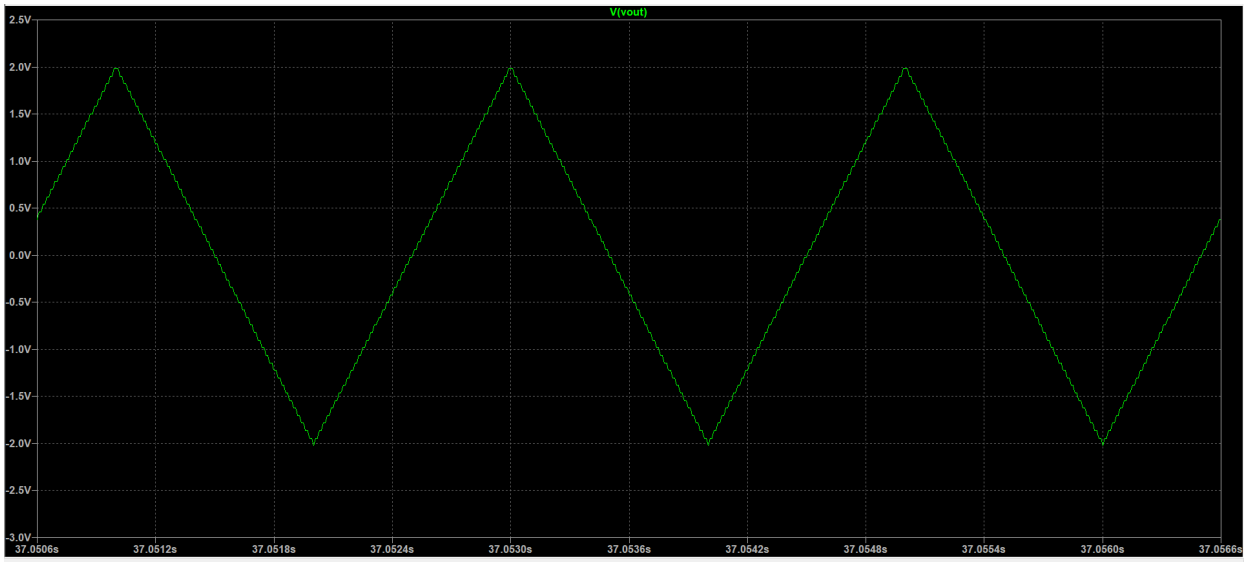
- The circuit sums two triangle waves
    - The low-frequency wave is the primary
    - High-frequency wave has ‘n’ times more frequency and ‘n’ time lesser amplitude hence same slope either in falling or rising edge
- This simulates the wave generated from the ADC block very well



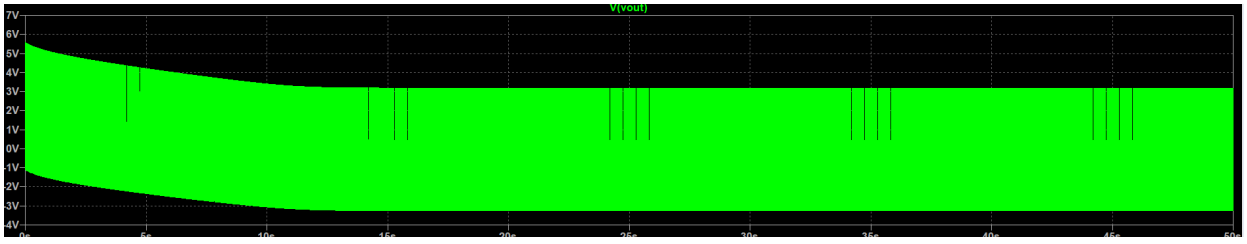
- These were fed to the testing block
- For the output voltage, one can see it has a high frequency triangular wave with constant decay in its mean value and settles to mean zero in about 20 seconds.
- As expected, this settling time improved after reducing the capacitances to 47 pF.

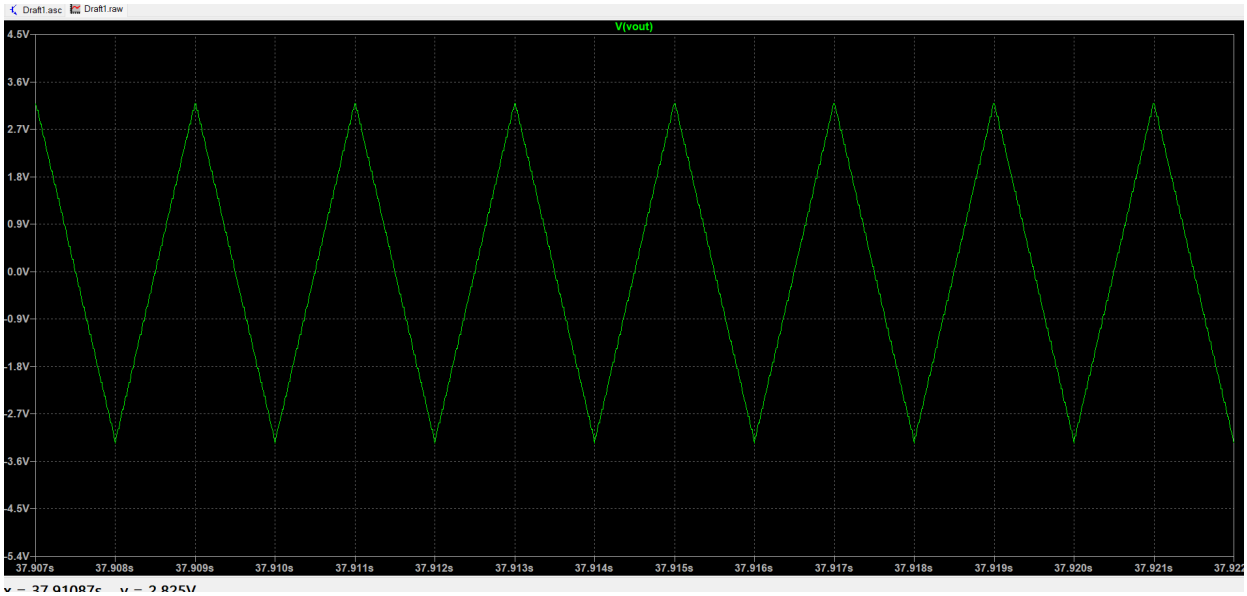


- The choice of a good Zener diode is very essential; a considerable part of the current was passing through Zener protection
- The value of the current taken by the measurement block is relatively small, in the 50uA range, which can be easily supplied by the chosen OpAmp
- The output close up looks like follows



- As expected, using a lower reference value for the same C_DUT reduces settling time
- This also improved the output voltage swing from about 4 Vpp to about 5.4 Vpp, this will improve % accuracy of the system



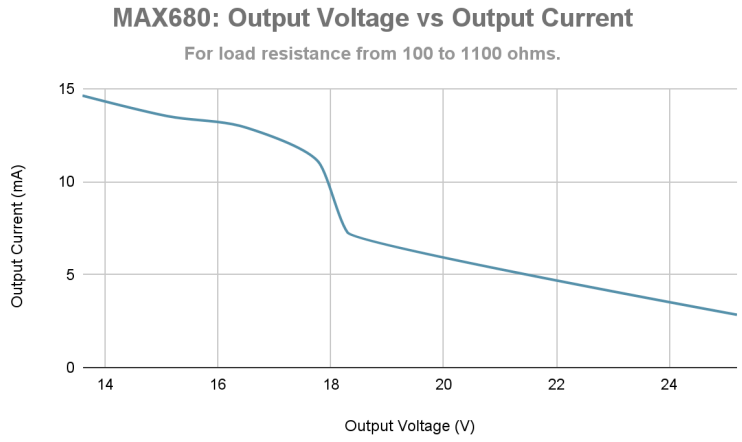


MAX680 Charge Pump:

Brief Details:

- ±10V from +5V Logic Supply
- Needs four capacitors of 1µF - 100µF
- As output current increases, the output voltage decreases

Output Voltage (V)	Output Current (mA)
14.63	13.6
13.53	15.1
12.91	16.5
10.99	17.8
7.26	18.3
2.84	25.2



MAX680 Testing:

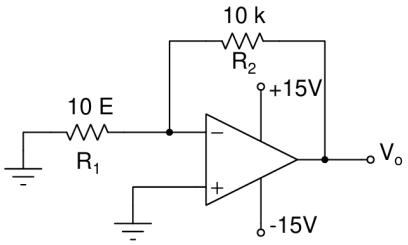
Operational Amplifier (OpAmp): TL082H

- *Power Supply*: ± 5 to ± 15 V
- *Low offset voltage*: 1mV
- *Low drift*: 2 μV/C
- I_{BIAS} = ± 120 pA max
- V_{CM} = V_{CC} + 1.8
- *A* = 125 dB
- *I* = 2.8 mA
- It can supply upto 20mA with about 5 % drop in output swing
- Alternative just in case current supply limit is reached
    - Current Booster circuit
    - OPA551 instead of this OpAmp

Testing:

1. *Offset Voltage*:

$$V_o = V_{OS}(1 + \frac{R_2}{R_1}) + R_2 I_B^- \rightarrow ①$$



For dominating V_{OS} and very large R_2/R_1

$$V_{OS} = \frac{R_1 V_o}{R_2}$$

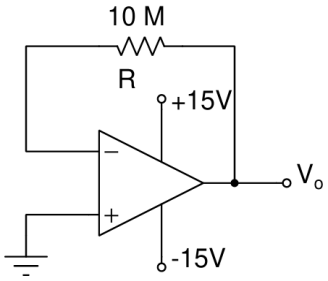
For R_1 = 10.1 Ω and R_2 = 10.28 kΩ, we get V_o =

Therefore, V_{OS} = 4.00 mV, 2.22 mV

2. Bias Current, I_B^-:

If we divide Equation ① with R_2 (= 10M) we will get,

$$I_B^- = \frac{V_o}{R} = 0.42\,nA,\ 0.24\,nA$$

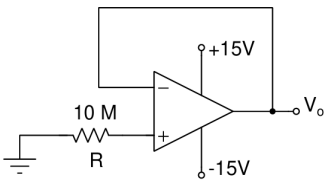


Note: R = 10 MΩ

3. Bias Current, I_B^+:

$$V_o = V_{OS} + RI_B^+ \rightarrow (2)$$

On dividing result (2) with R(= 10 MΩ), we get

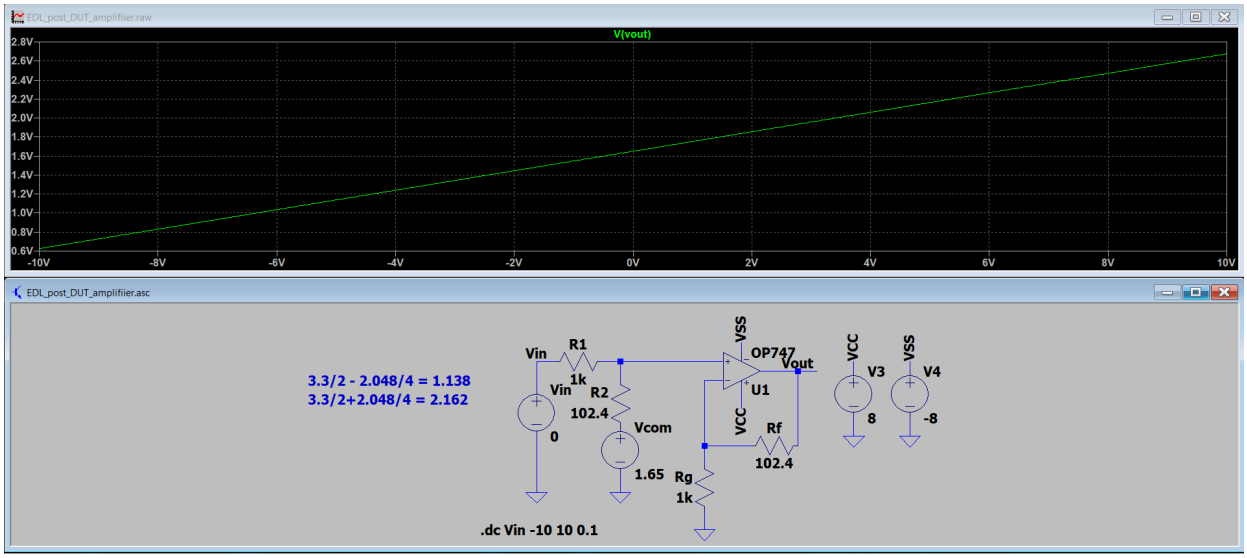


$$I^{+}_{B} \approx \frac{V_o}{R} = 0.3\ \mu A, 0.14\ \mu A$$

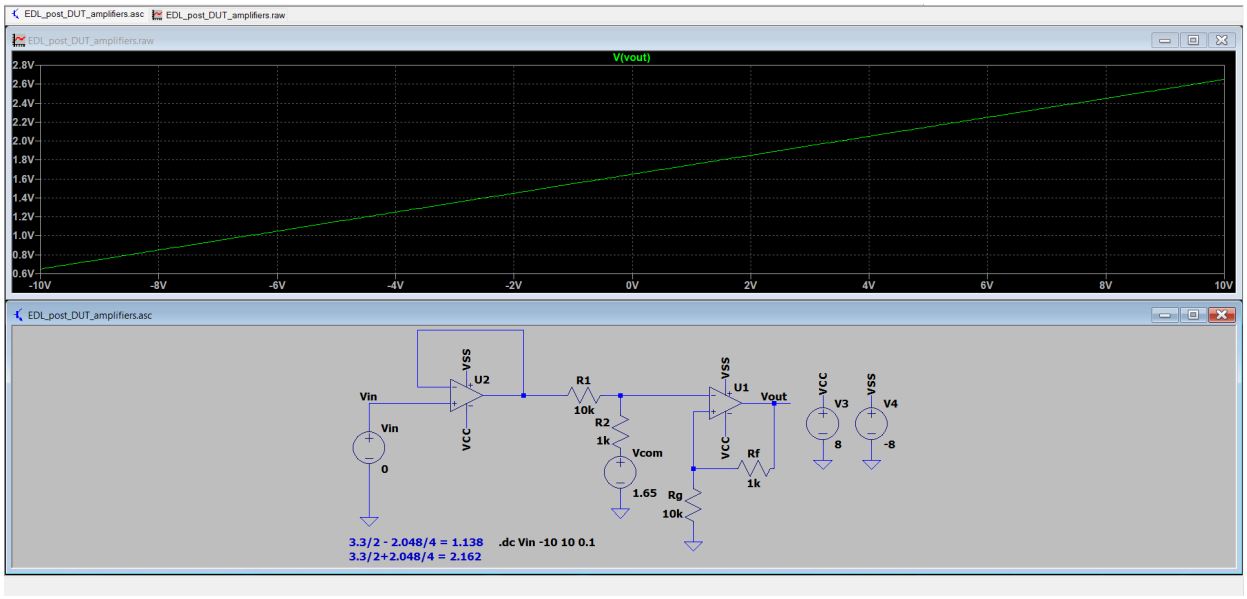
MAX1184 basic test(11.03.2024)

After powering MAX1184, the COM voltage settles to VDD/2 internally, and REFOUT = 2.048 V by default. This confirms the final fine points in schematics. Now, the design of the final amplifier is to map the output of DUT to the operating range of ADC.

Designing of the post-DUT amplifier (12.03.2024)

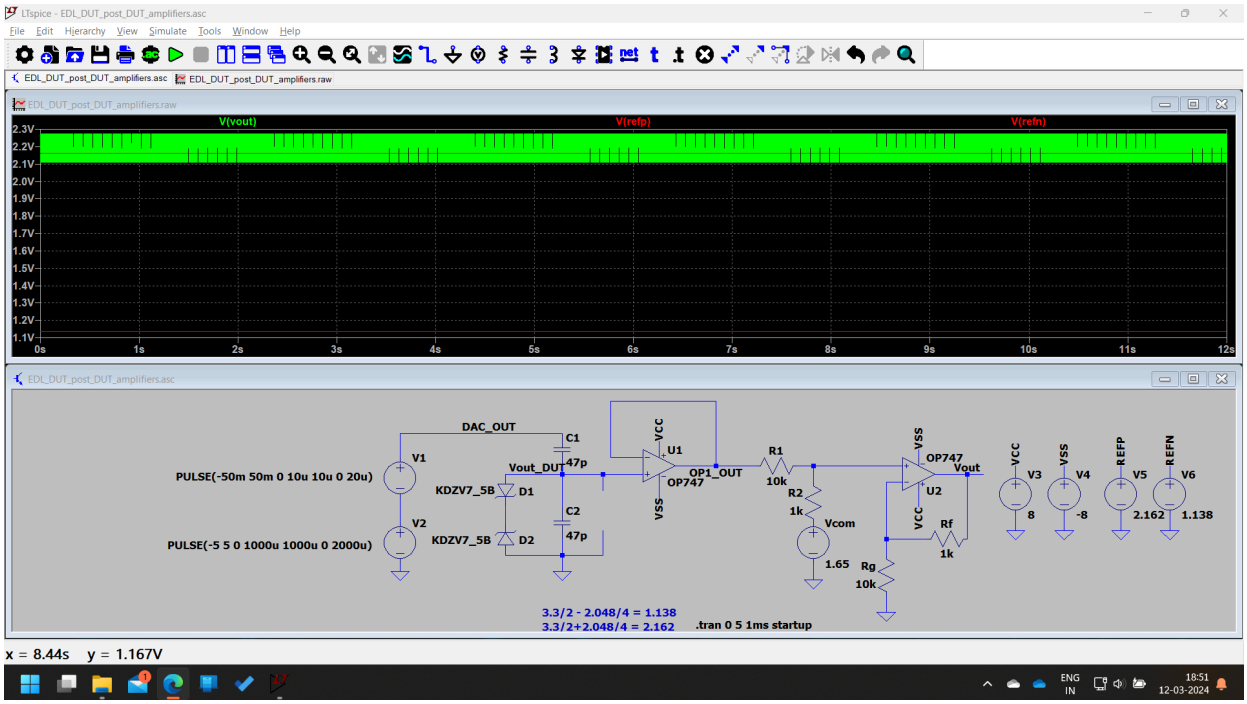


- Using the single supply Op Amp slides, we derived the required ratios of $\frac{R_2}{R_1}$ and $\frac{R_F}{R_G}$.
- With this, we linearly mapped the DC voltage output of DUT to the input range of ADC.
- In this design, if the input is 10 V due to some error in the charge pump and OpAmp, the ADC will work well as the resulting voltages are still within absolute tolerances of ADC.
- Since the exact value of 0.1024 is not available in any ratio in real life, the simulations are done using the ratio of 0.1. This also gives the advantage of little large-scale



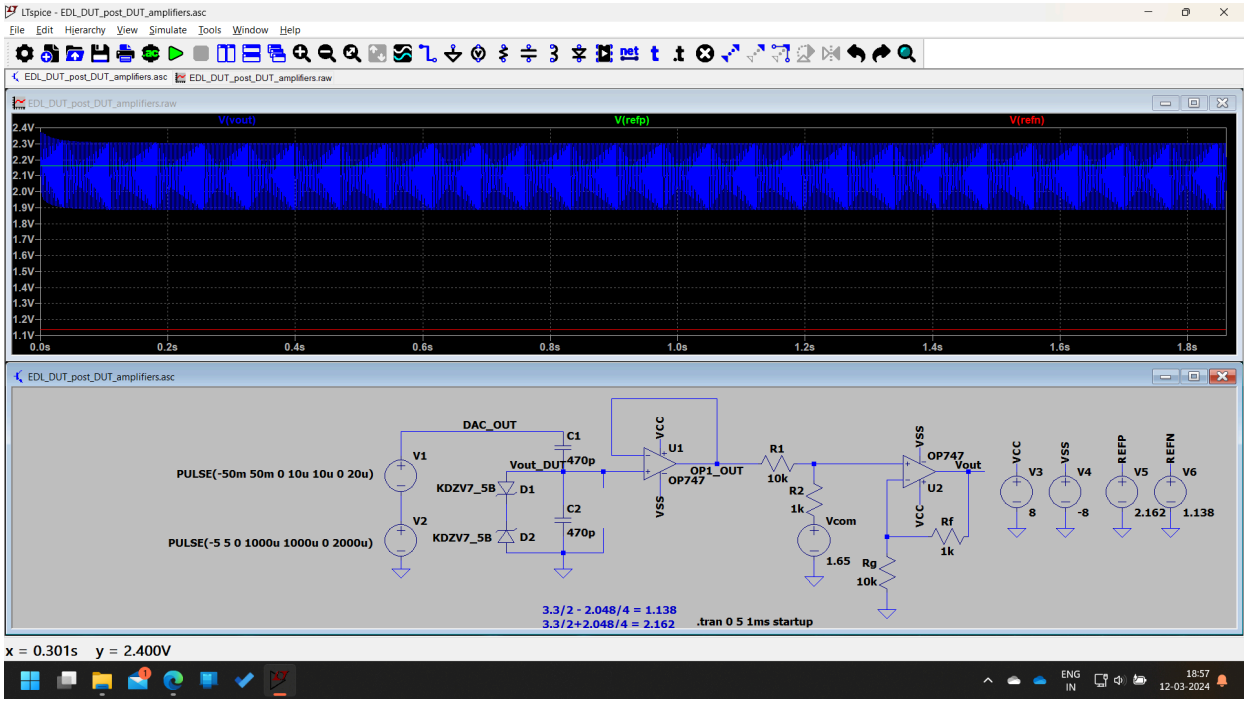
Vin (V)	Vout_sim (V)	Vout_actual (V)
-10	0.65 (0.626)	
-7		
-5	1.15 (1.138)	
-3		
0	1.65 (1.65)	
3		
5	2.15 (2.162)	
7		
10	2.65 (2.674)	

Combined DUT + post-DUT amplifier test

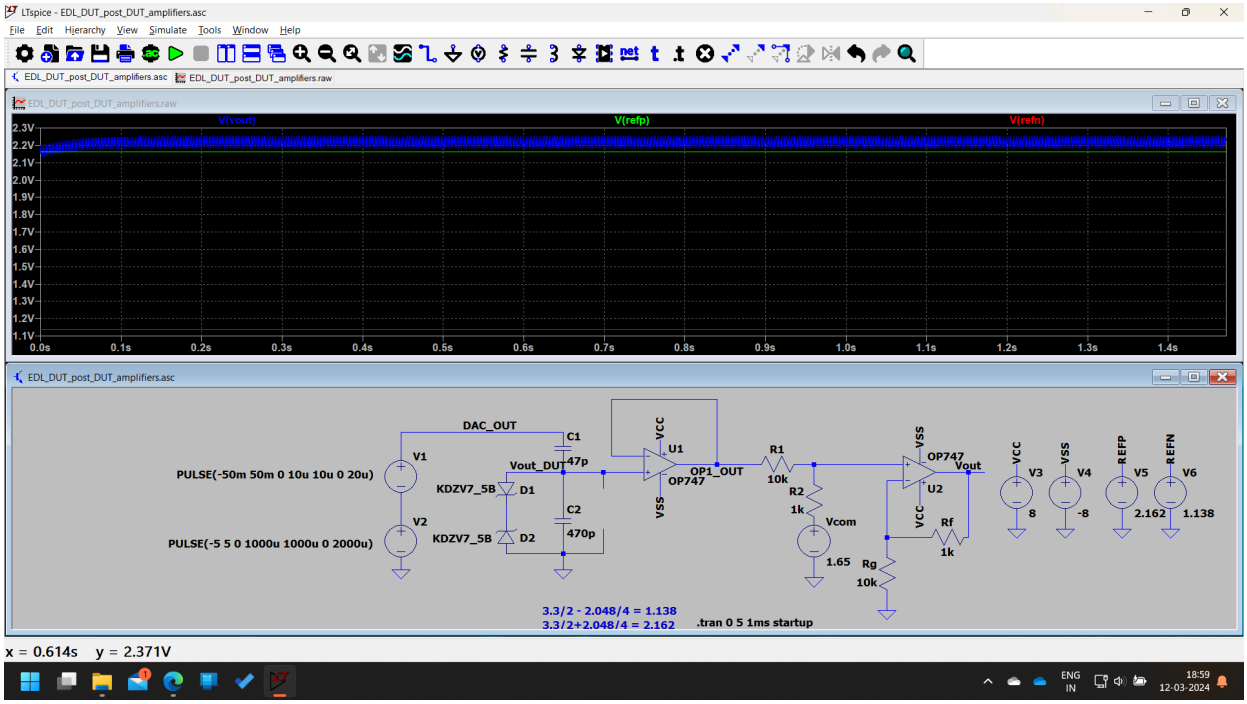


One can clearly see that this goes out of the range for the ADC, hence it will be important to adjust the C2

Figure: DUT 470pF, ref 470pF



Flg: DUT 47pF, ref 470pF



In both above cases, the peak to peak is just 0.07 V, which is of the order or 8-bit result change

In order to be able to measure whole, $\frac{R_1}{R_2}$ needs to be lower than 0.05, but now, the V_{out} varies only 30 mVpp.

Hence, it is necessary to have the ability to switch between reference capacitors.

TESTING 13.03.2024

The UGF is working correctly. The output of the range transfer opamp is not correct

V_{in} (V)	$V_{out\text{-}sim}$ (V)	$V_{out\text{-}actual}$ (V)
-10	0.65 (0.626)	
-7		(glitchy)
-5	1.15 (1.138)	2.21
-3		2.54

0	1.65 (1.65)	3.22
3		3.97
5	2.15 (2.162)	4.36
7		4.74
10	2.65 (2.674)	

Test Result:

- Output impedance of the COM pin is not very high, hence cant be used as a reference voltage.
- Possible solution: Apply UGB at the COM pin.

Test (2) results: Now the voltage is linear and COM. Also, the COM is actually at 1.83 V, not at VDD/2

V_{in} (V)	$V_{out\text{-}sim}$ (V)	$V_{out\text{-}actual}$ (V) (After buffer)
-10	0.65 (0.626)	
-7		
-5	1.15 (1.138)	2.4
-3		2.78
0	1.65 (1.65)	3.32
3		3.84
5	2.15 (2.162)	4.19
7		4.54
10	2.65 (2.674)	

Observation: This swing was also more than expected.
Possible cause: current drawn from circuit too much

V_{in} (V)	$V_{out\text{-}sim}$ (V)	$V_{out\text{-}}$I (V) (After buffer)
-10	0.65 (0.626)	
-7		

-5	1.15 (1.138)	1.31
-3		1.53
0	1.65 (1.65)	1.84
3		2.14
5	2.15 (2.162)	2.32
7		2.54
10	2.65 (2.674)	

Conclusion: Circuit is operating as expected.

[eFuse] TPS25200 Testing [FAILED] Ditch

Rlim = 120 kOhm (I lim = 808 mA)

Testing	Expected Result	Actual Result
Short Circuit Test	Load is disconnected	
Input voltage variation (Under No Load condition)	1. Undervoltage lockout 2. Vin = Vout 3. Overvoltage clamp 4. Overvoltage lockout	
Current Limit Test		

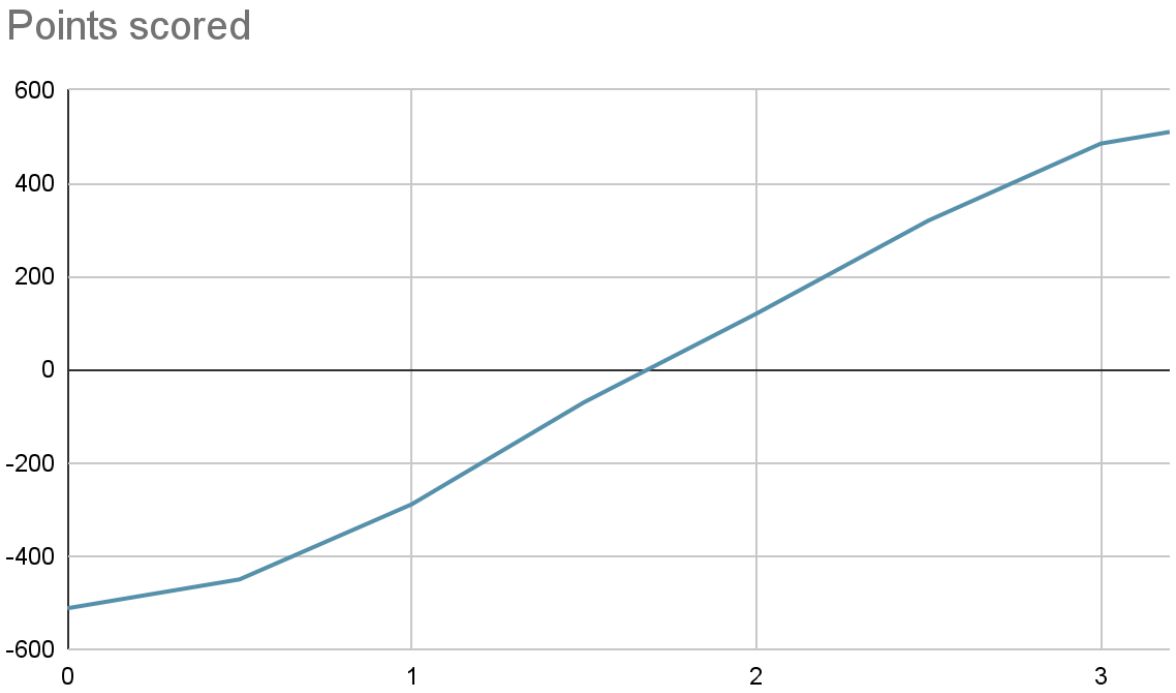
No Load Voltage Test

Input Voltage	Output Voltage

ADC Testing

Observation:

Input Voltage	Output Reading (20 reading average)
0	-512
0.5	-450
1.0	-288.8
1.5	-70
2.0	120
2.5	320
3.0	485
3.2	510



Very linear characteristics in Vin: 0.5V -> 3.0 V

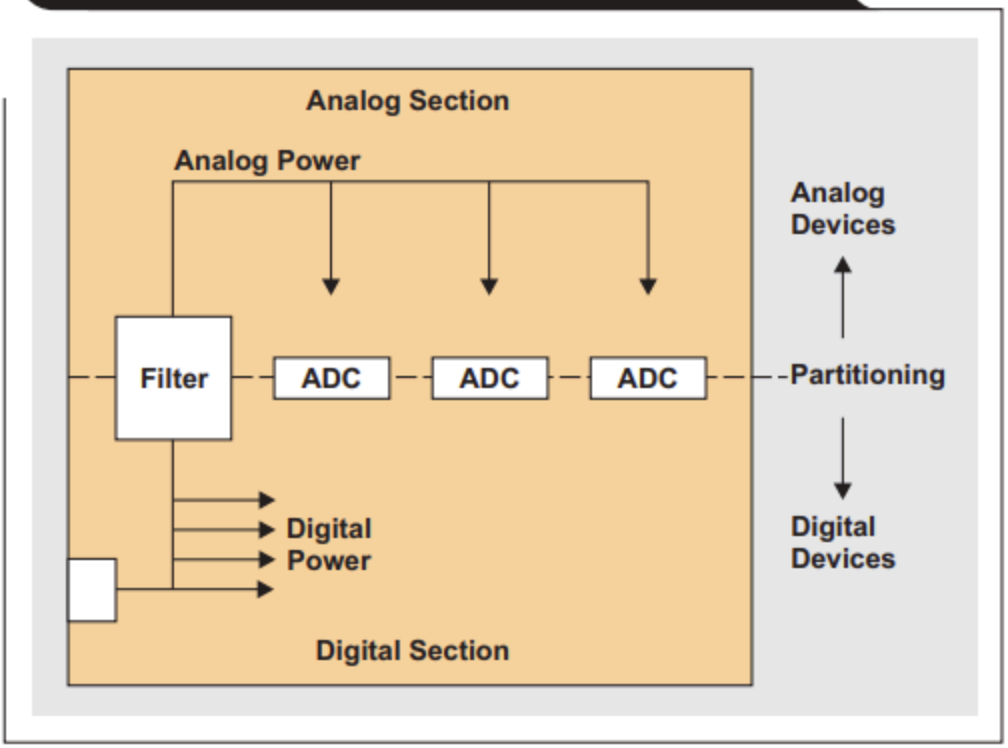
ADC = 382.3657*(Vin - 1.68)

Conclusion: Sleep mode: Working
T/B: Working
Clock: Working (O/P does not change when clock is stopped)

PCB Designing

Procedure: For grounding, we will follow the paper by Texas Instrunments. Since we are using multiple ICs linking Analog and Digital domain, we will have use this approach

Figure 7. Power and ground for PCB with multiple ADCs



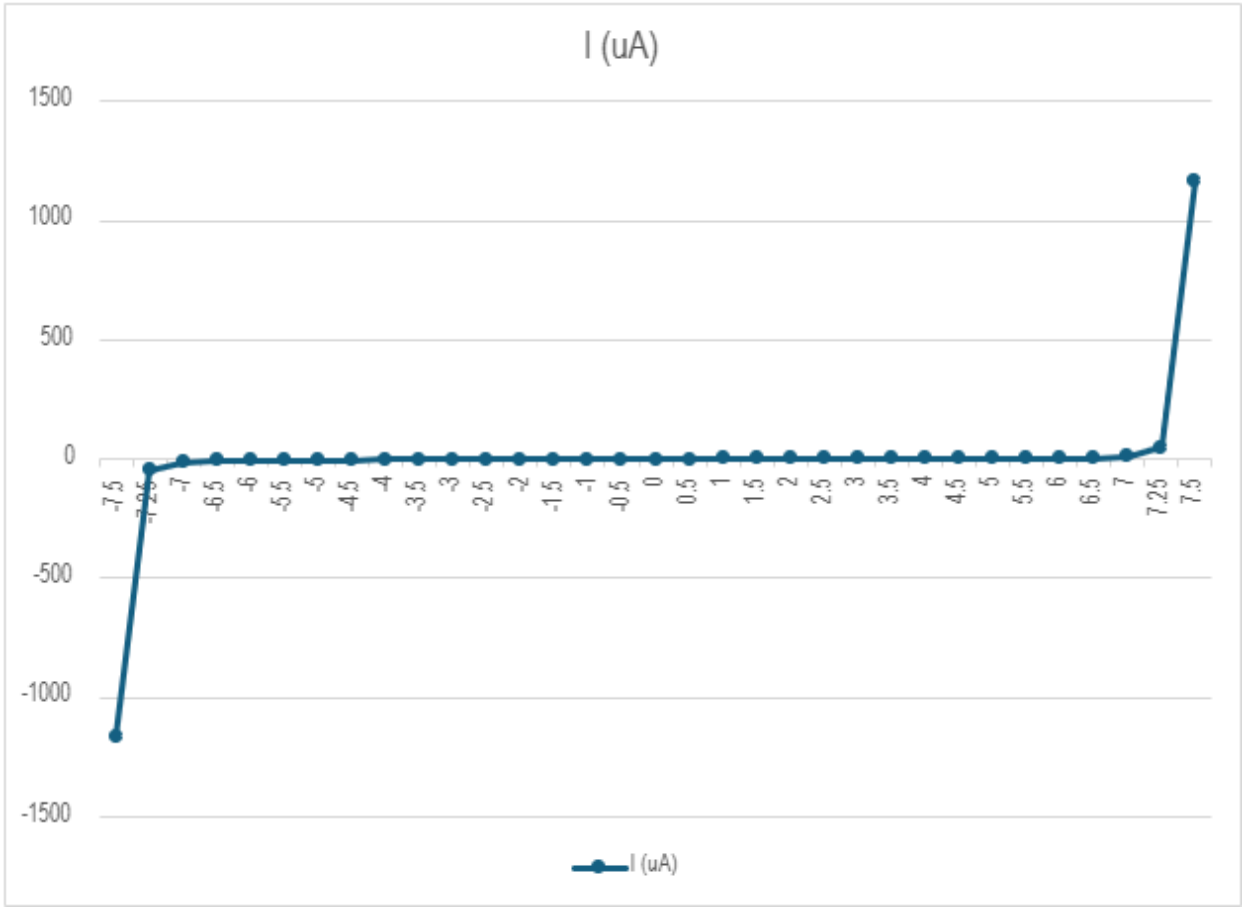
Dimensions of the Connector: 58mm * 9mm

PCB Review:

- Removed powerplane, it will just act as a capacitor
- Replace it with ground plane
- Straightened the traces
- Usedvias for non high speed traces
- Moved decoupling capacitors even closer for ADC

Zener Protection Testing 22.03.2024

Testing R



esults

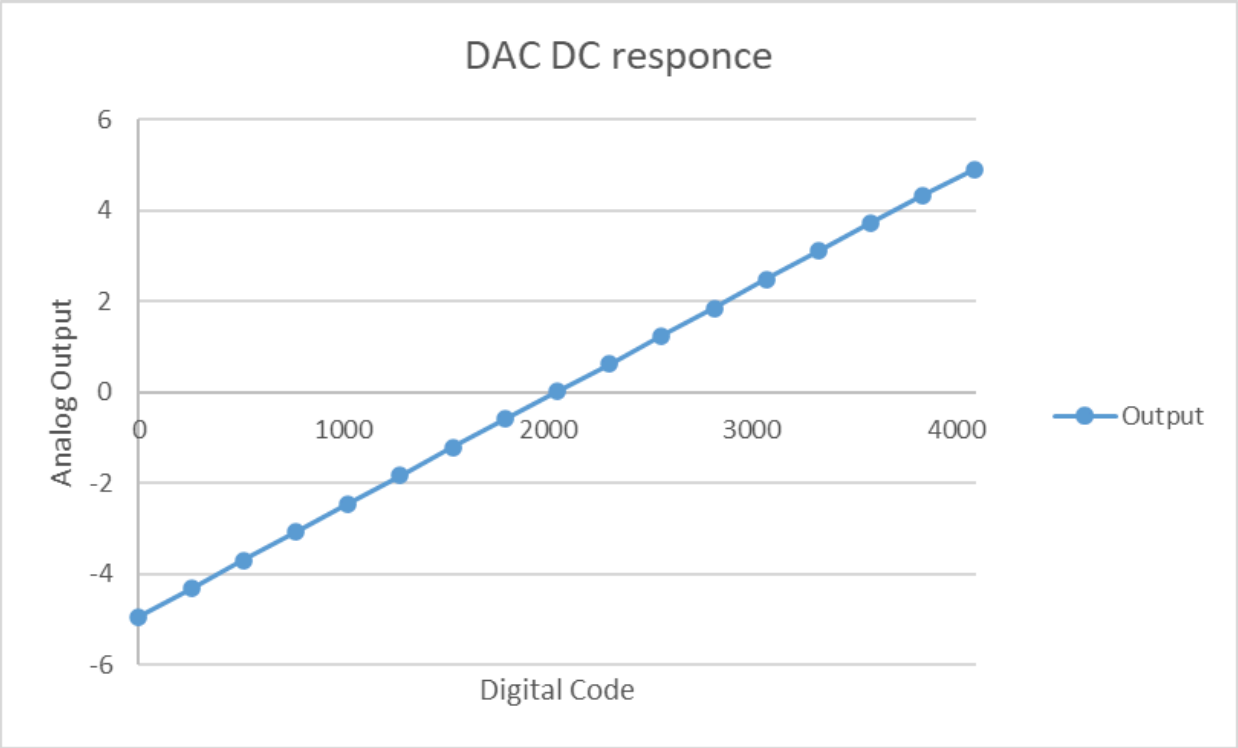
Observation: The protection does not draw significant current till the voltage across it is >7 V
Conclusion: This can be used to select resistors for the DUT-ADC amplifiers

DAC DC response test

Procedure: In this test, we used Arduino to provide a clock and a constant input. We then checked the output voltage of the DAC + amplifier.

Observations: With pots, we can adjust scale and zero offsets with very good accuracy.
Reason: The Vref pot reduces full scale range and Rref pot is for zero adjust.

Note*: Because of lack of good supply and good potsover the weekend, the testing result does not exactly match with expected output.*



[Testing Result]

Conclusion: The test is successful.

3D CAD design

- Box with sliding door on top
- Holes for USB Type A port, Vents

FPGA wave generation and data receiving and transmission:

Choosing microcontroller or FPGA for wave generation

- As system requires 100kHz triangular wave with at least 100 samples/cycle, we require our microcontroller/FPGA, DAC and ADC to work at at least speed of 100x100 kilosample/cycle which is equal to 10 megasample/cycle,

microcontroller has clock of 80MHz but as it does work serially, we can't rely on that and that's why FPGA was chosen as it works in parallel.

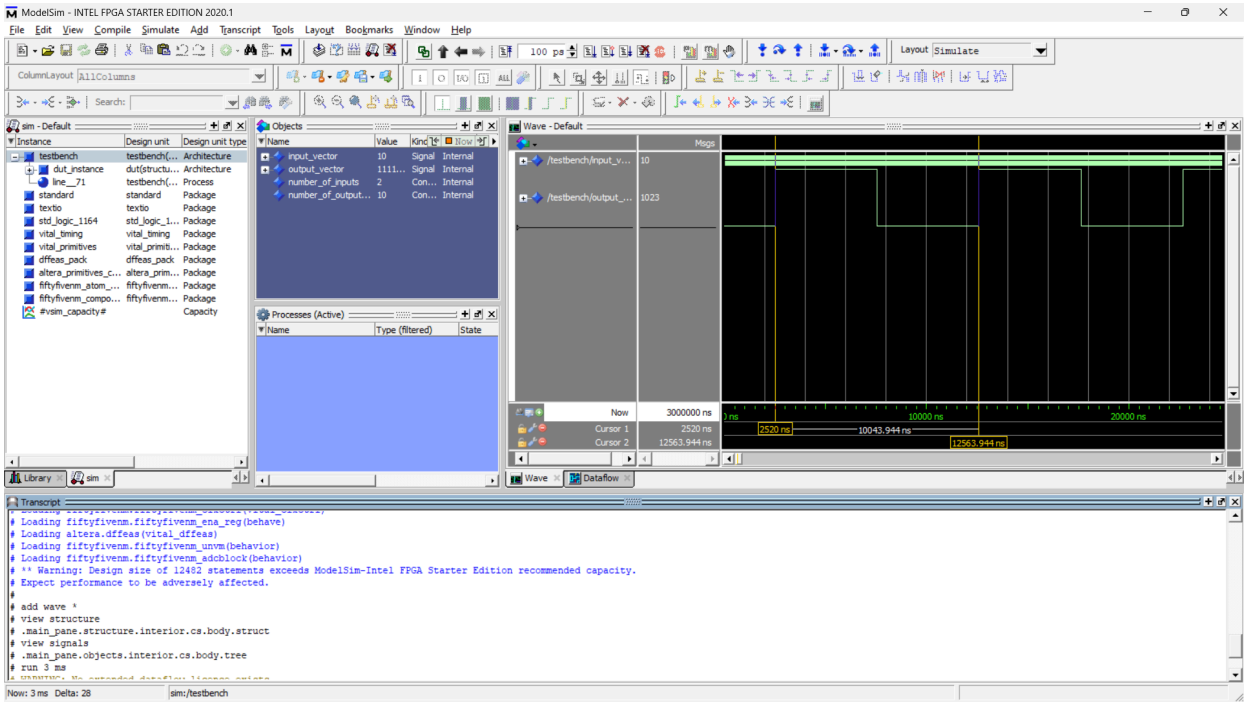
VHDL code for wave generation

- Two VHDL code files, fg.vhdl and clockdivider.vhdl were made.
- fg.vhdl takes inputs like frequency, sample numbers, mode of operation etc and gives 12 bit output which corresponds to the magnitude of the input.
- clockdivider.vhdl takes clock and a factor as an input and gives appropriate output clock based on that.
- fg.vhdl code can be modified to give at maximum 8 kind of modes as output.

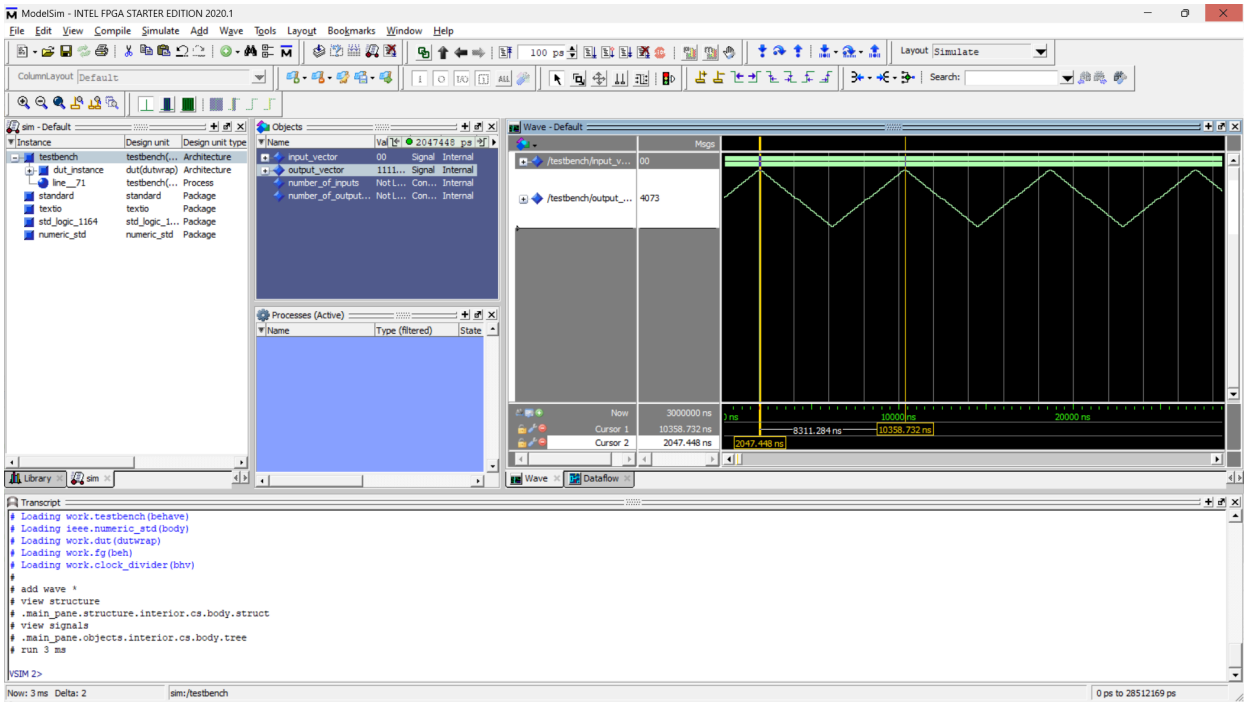
RTL simulation of the code

- Here are RTL simulation result for the fg.vhdl file as a top level file:

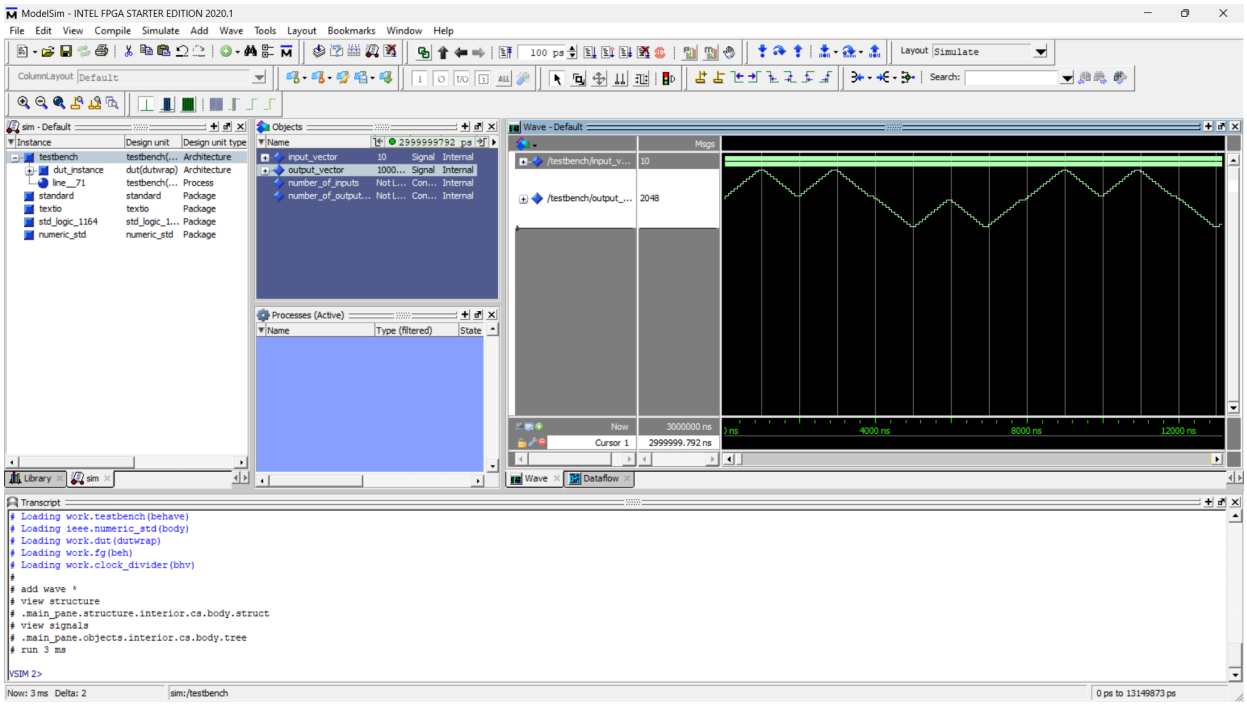
Square wave:



Triangular wave:



Double triangular wave:



Wave testing with DAC

- Now the output of fg.vhdl was checked on cyclone IV E FPGA using DAC.
- Square waves were giving almost equal frequency that of the input frequency.
- Triangular waves or double triangular waves were giving frequency offset above 10kHz. So, for the operational range above 10kHz we have to compensate for this offset.
- The DAC output photos are given above in documentation.

UART interface to communicate data with PC

- For UART interface, code for UART was referred from below given source,
- UART in VHDL and Verilog for an FPGA (nandland.com)
- This code was tested through a sample code using serial port monitor.

VHDL code for receiving parameters, transmitting data and controller

- Now to conclude the design the parameter_receiver.vhdl, data_tranmeter.vhdl and controller.vhdl were made.
- parameter_receiver.vhdl receives 24 bits of input data serially from the PC using UART and gives that parameters(17 bits for frequency, 3 bits for mode, 4 bits for number of seconds for burst mode(for 0 seconds it will consider single cycle mode)) to the controller.vhdl.
- controller.vhdl sends the data to fg.vhdl while enabling data reading by sending command to data_transmitter.vhdl and makes output equal to that of fg.vhdl and calculates the cycles until time of cycles becomes that of input time.
- data_transmitter.vhdl saves data of both input and output in memory and sends it to PC via UART after competition of output wave

Testing of the code with ADC

-