First logon to tacc stampede machines by doing ssh from terminal

**ssh ksai444@stampede.tacc.uteaxs.edu**

and enter the password, you will be logged in to one of the four login machines and that request for processors by executing idev command

**idev –m** (time in min)

u will be granted processors,only you can get access to.

Full details of your machines hardware configuration is stored in /proc/cpuinfo file

**cat /proc/cpuinfo**

The cache performance statistics are calculated by using perf commands and passing appropriate arguments to perf command to get the L1 load misses and LLC load misses

The command used is

perf stat -e L1-dcache-loads,L1-dcache-load-misses,LLC-loads,LLC-load-misses java (and arguments to java program)

mean is varied from 10 to 100 in steps of 10

number of threads is varied from 2 to 32 in steps of multiples of 2

and all the Locks are calculated for the mean and threads values

The graphs is plotted in excel file with file named mcproject2

The script is written in python, instructions to execute the project is written in readme file.

As you can see from the graph of cache performance that cache misses are in the order of

TASLock > TTAALock > TTASBackoffLock > CLHLock

Throughput is almost same for TASLock, TTASLock, TTASBackoffLock and is less for CLHLock