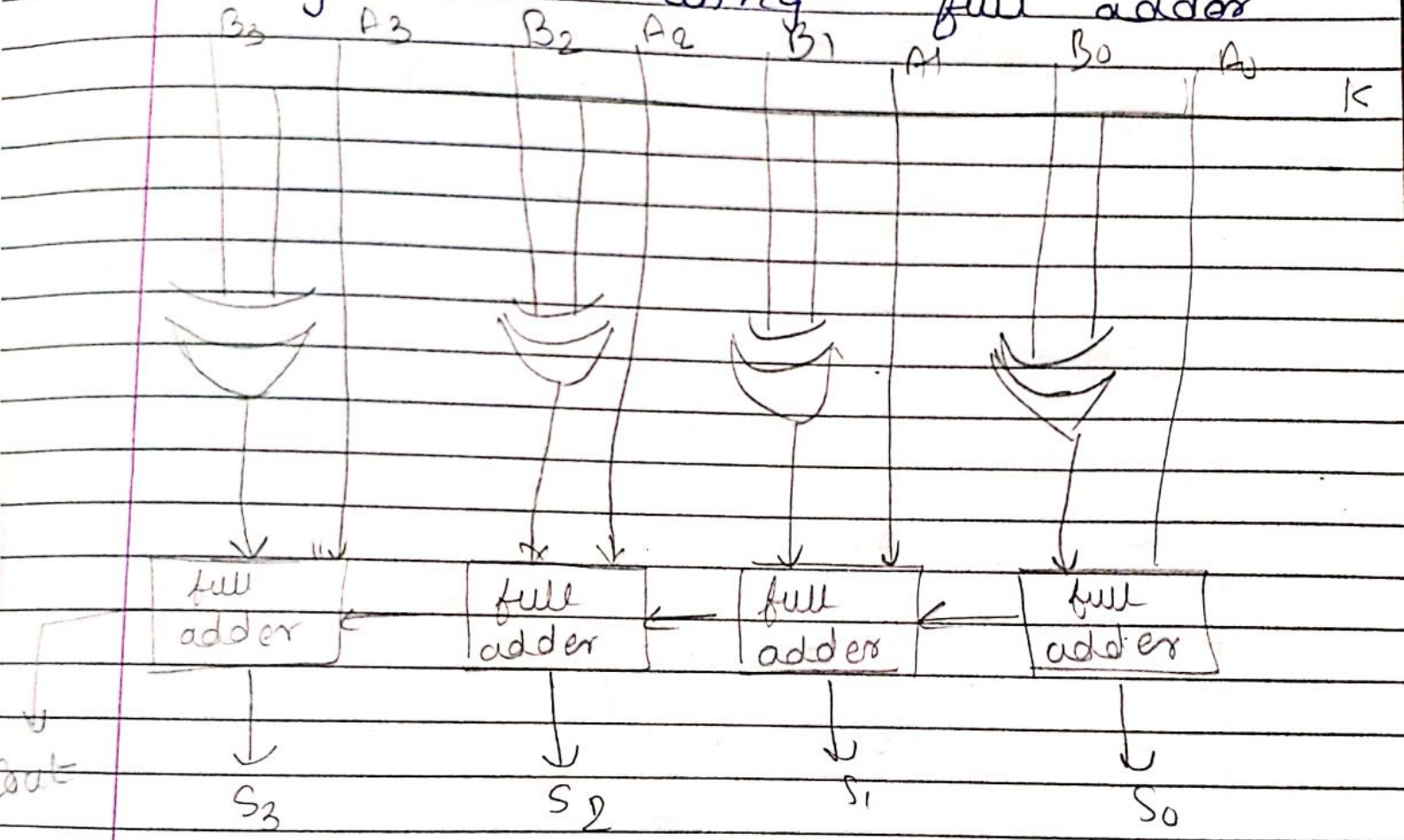
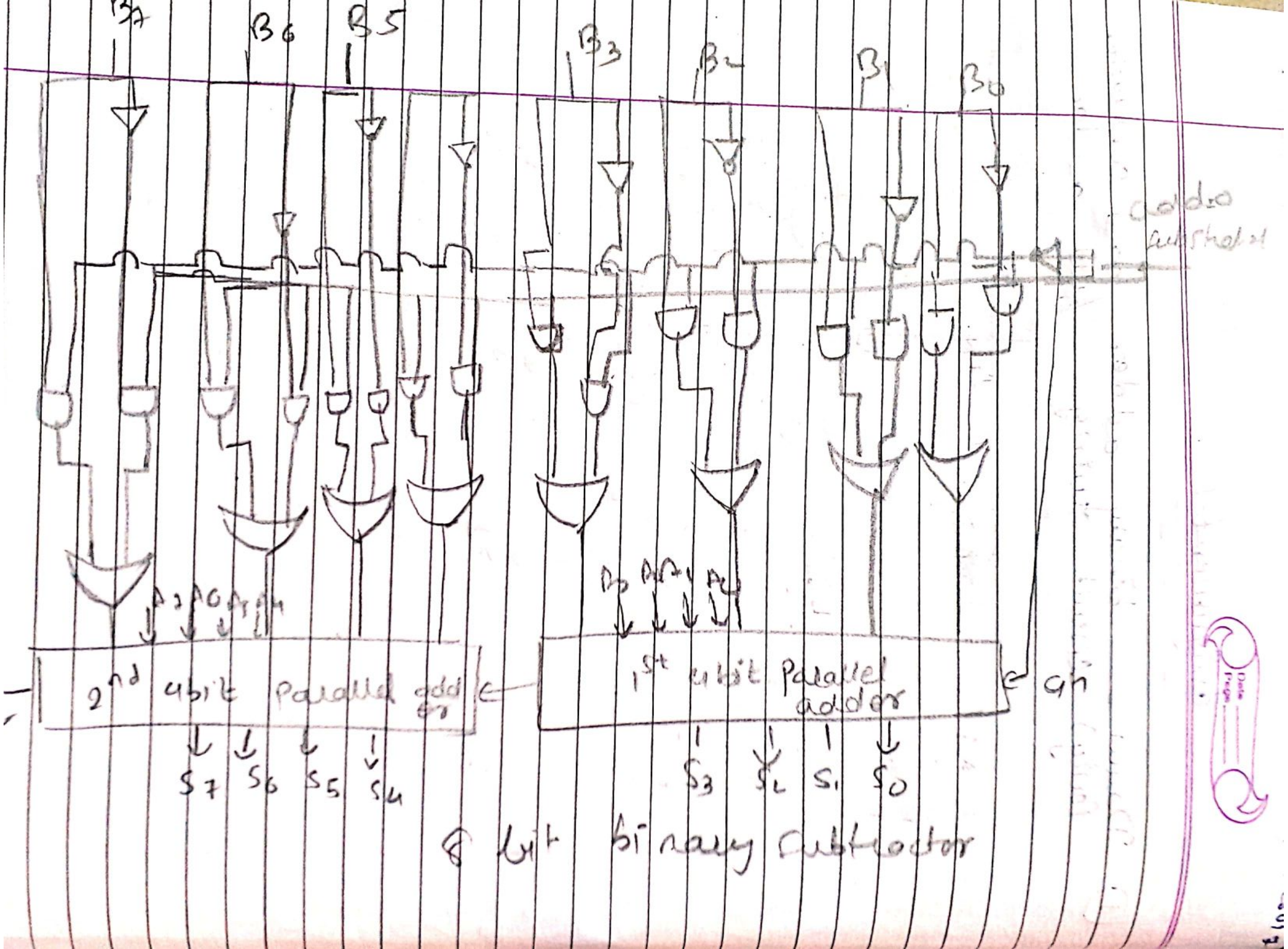
18DCS017

Assignment-1

(1) Draw ____ binary adder and subtractor (only) circuit using full adder

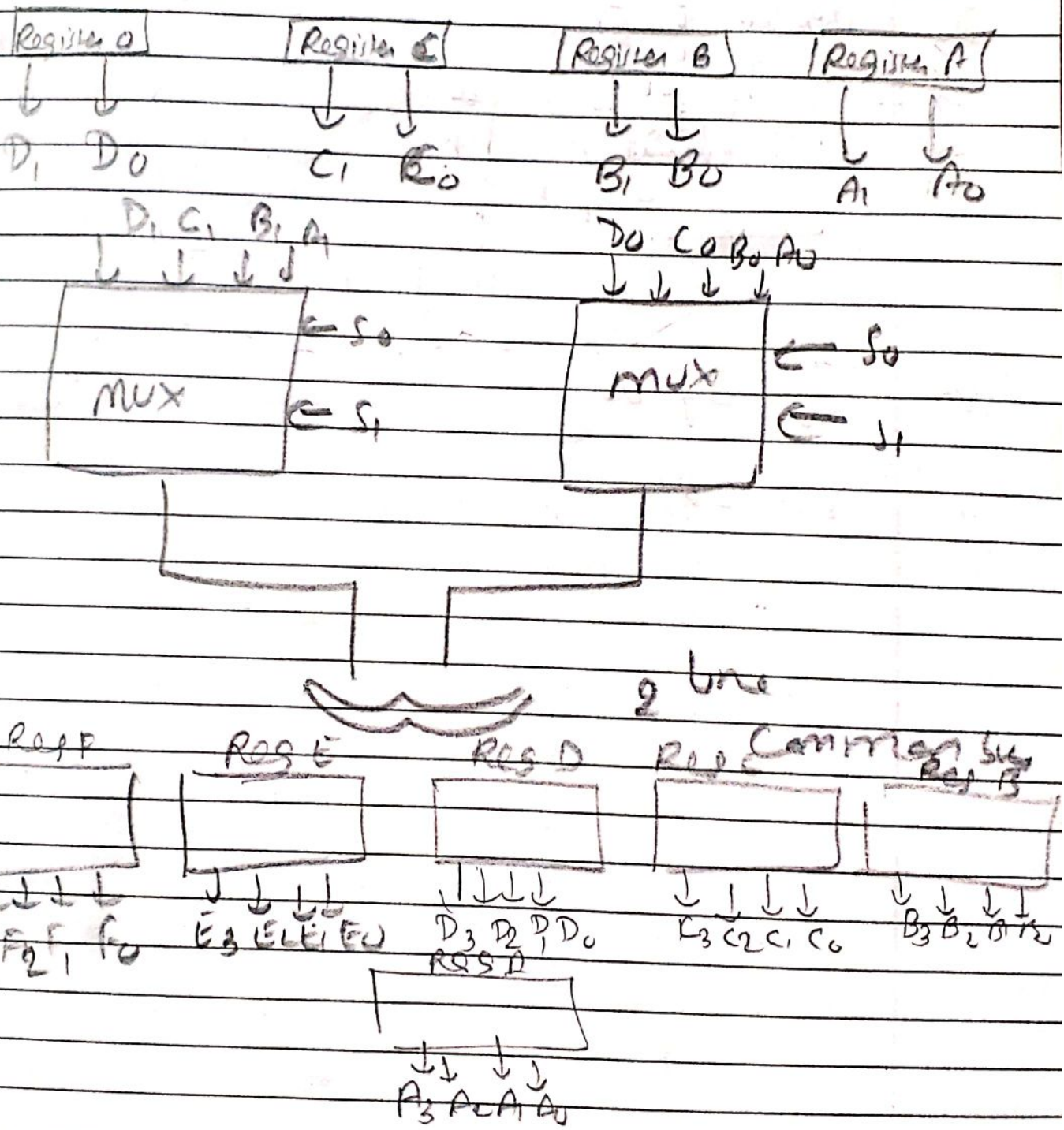


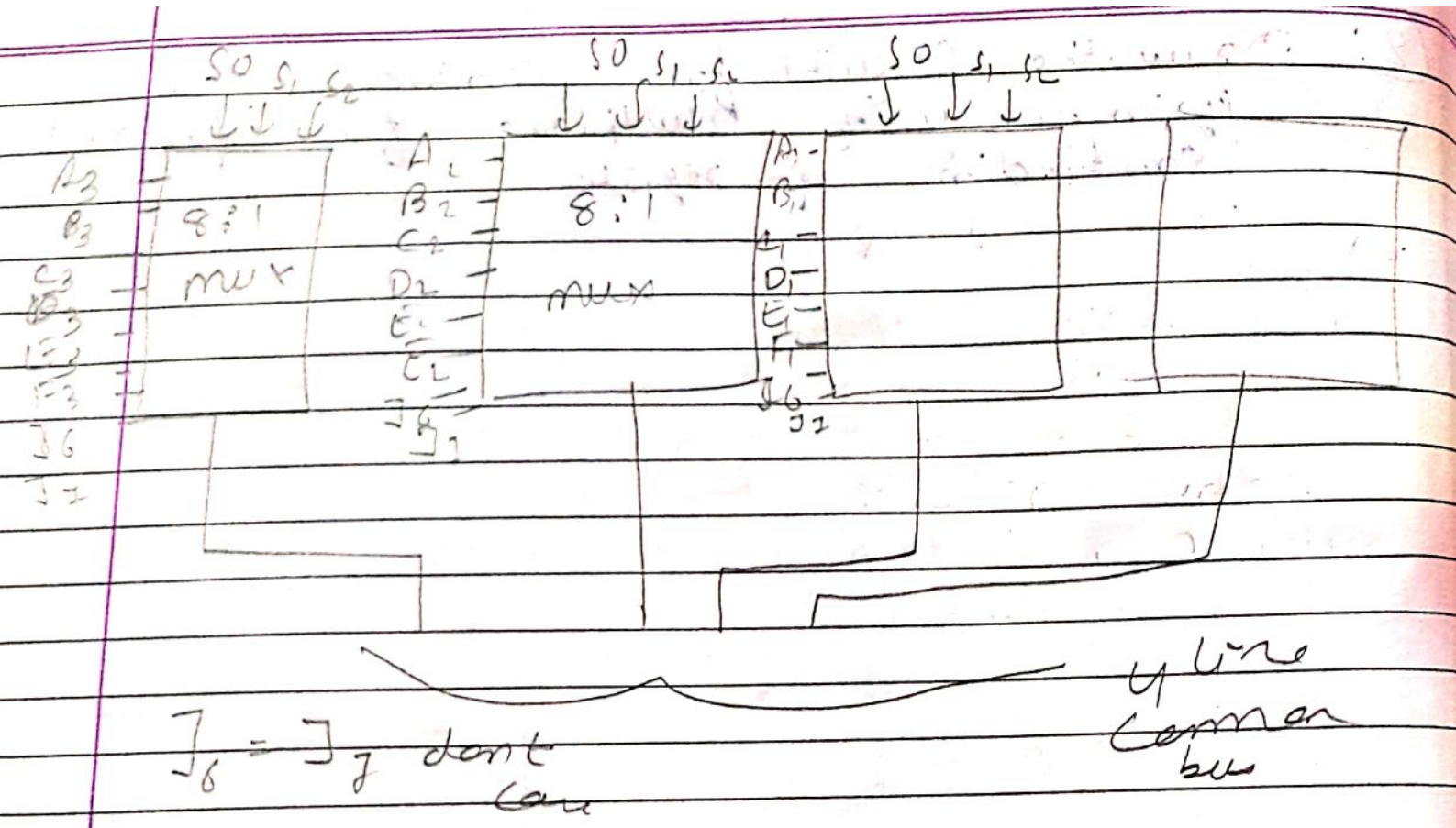
4 bit binary adder



(2) Draw the circuits for common bus system using multiplexers for following combination of registers

⇒





$J_6 = J_7$ don't care

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(3) No, other harddisk interrupts the microprocessor for data transfer the current executing instruction is stored at some specific location from program counter and then the interrupt occurs After the transferring of data from harddisk the remaining execution of instruction is started from that specific location where where address is stored.

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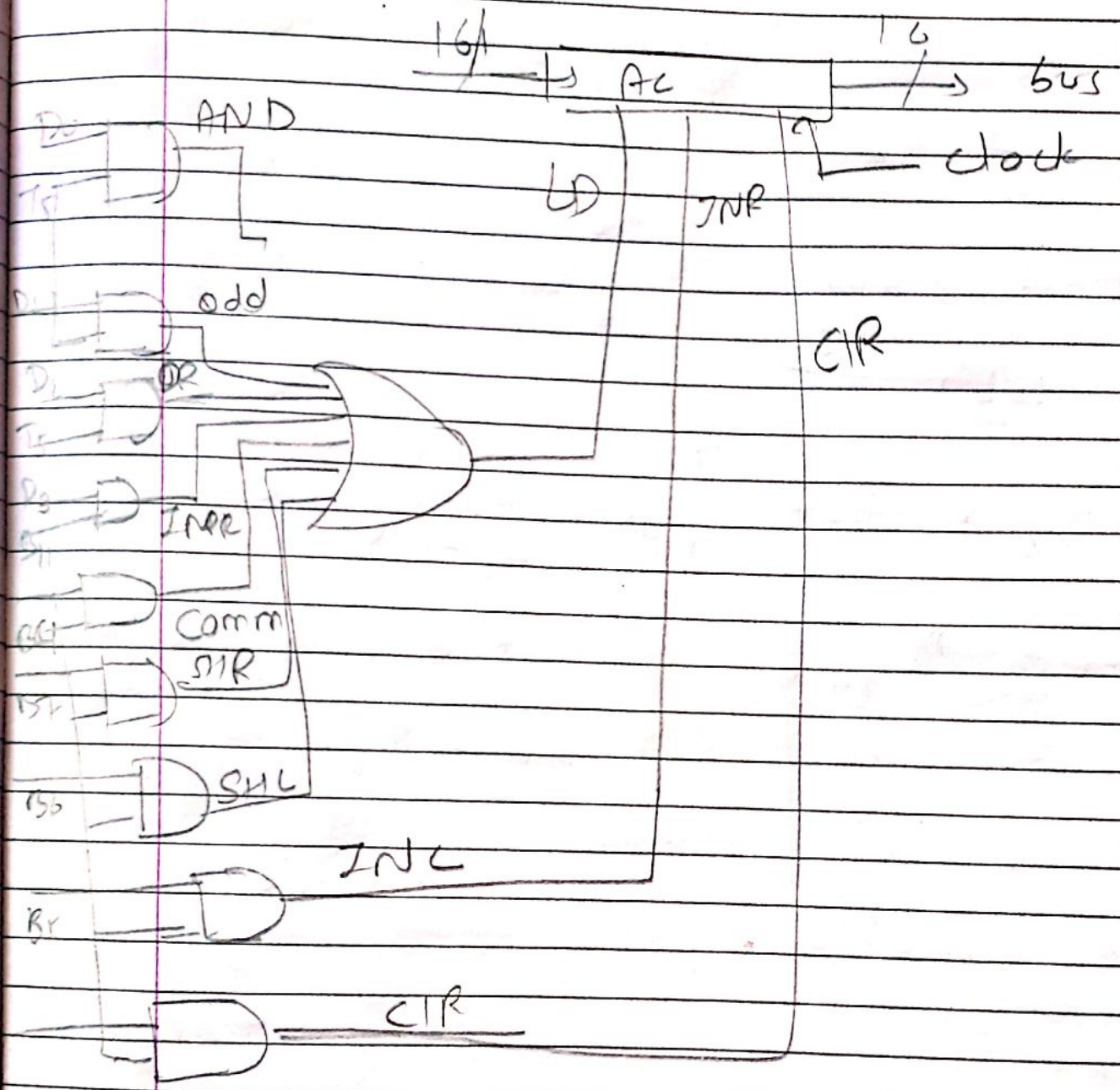
(6) 6.1 Control of AC Register



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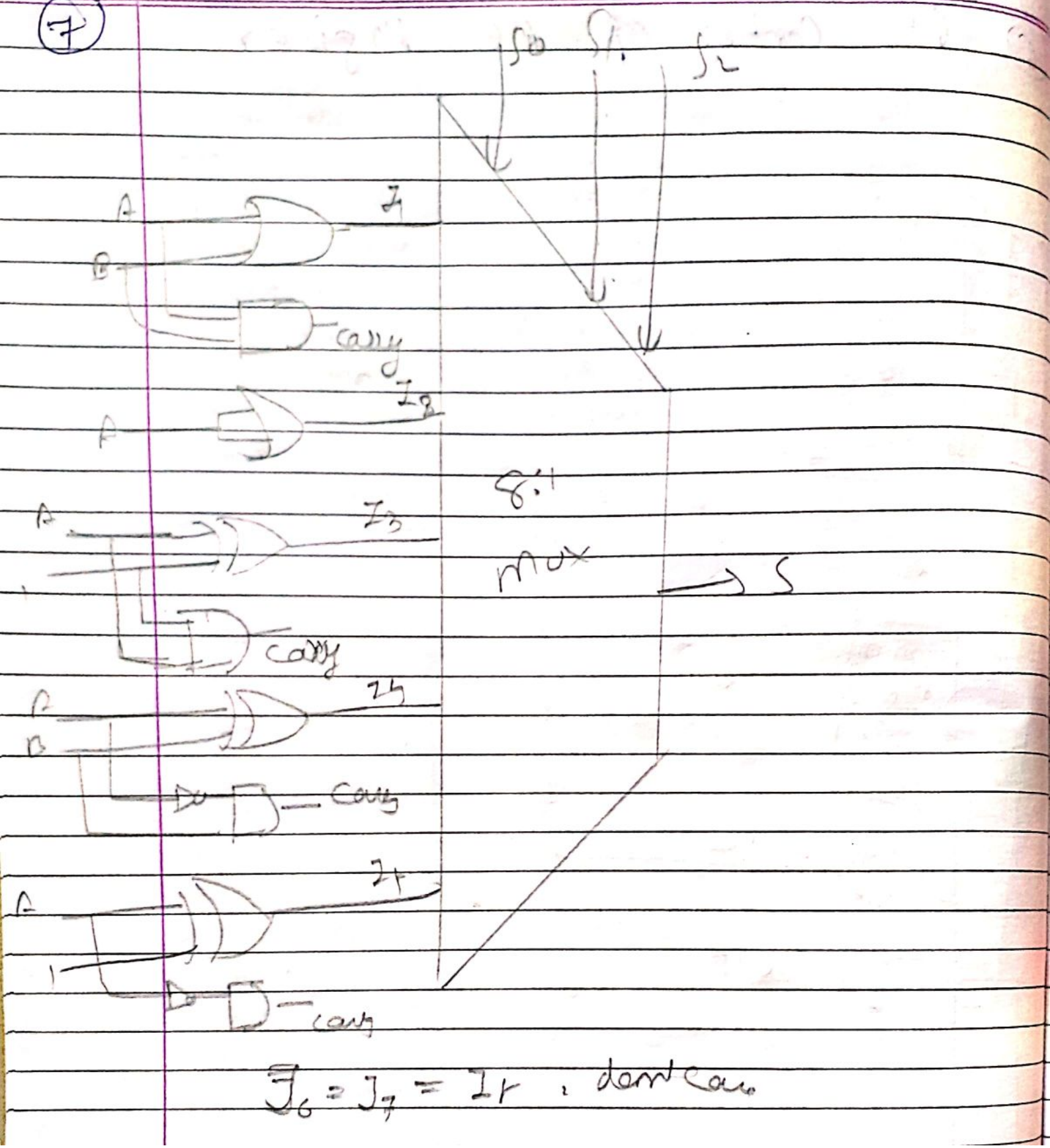
(7)



$J_6 = J_7 = I_r$: don't care

Q1 PC = 2, R1 = 1, XR = 3 address = 4d

Addressing mode	Effective address	Content of Ac
Direct address	401	3
Immediate operand	-	401
Indirect address	3	401
Relative address	403	5
Indexed address	404	6
Register	-	1
Register indirect	-	-
Auto Increment	402	4
auto decrement	400	2

Q2 PC = 2, R1 = 2 XR = 3 address = 4d

Addressing mode	Effective address	content of Ac
Direct address	401	3
Immediate operand	-	401
Indirect address	3	401
~~Relative address~~ Register	~~403~~ 404	5
Register indirect	404 -	6
Auto increment	402	2
Auto decrement	400	2

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8.3 PC = 2 R_1 = 3 XR = 3 address = 401

addressing mode	Effective address	Content of A
Direct address	401	3
Immediate operand	-	401
Indirect address	3	401
Relative address	403	5
Indexed address	404	6
Register	-	3
Register indirect	3	401
Auto increment	402	4
Auto decrement	400	2

8.4 PC = 2 R_1 = 4 XR = 3 address 401

addressing mode	effective address	content of AC
Direct address	401	3
immediate operand	-	401
Indirect addr	3	401
indexed address	403	5
Register	-	4
register indirect	4	-
Auto increment	402	4
Auto decrement	400	2

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8.5 PC = 2 R1 = 1 XR = 6 address = 410

address mode	effective add.	Content of Ac
Direct address	410	12
Immediate operand	—	410
Indirect address	12	—
Indexed address	416	—
Register	—	1
Register indirect	1	—
auto increment	411	13
auto decrement	409	11
Relative address	412	14

8.6 PC = 2 R1 = 2 , XR = 6 , address = 410

address mode	effective address	Content of Ac
Direct address	410	12
immediate operand	—	410
indirect address	12	—
indexed address	416	—
Relative address	412	14
Register	—	2
Register indirect	2	—
auto increment	411	13
auto decrement	409	11

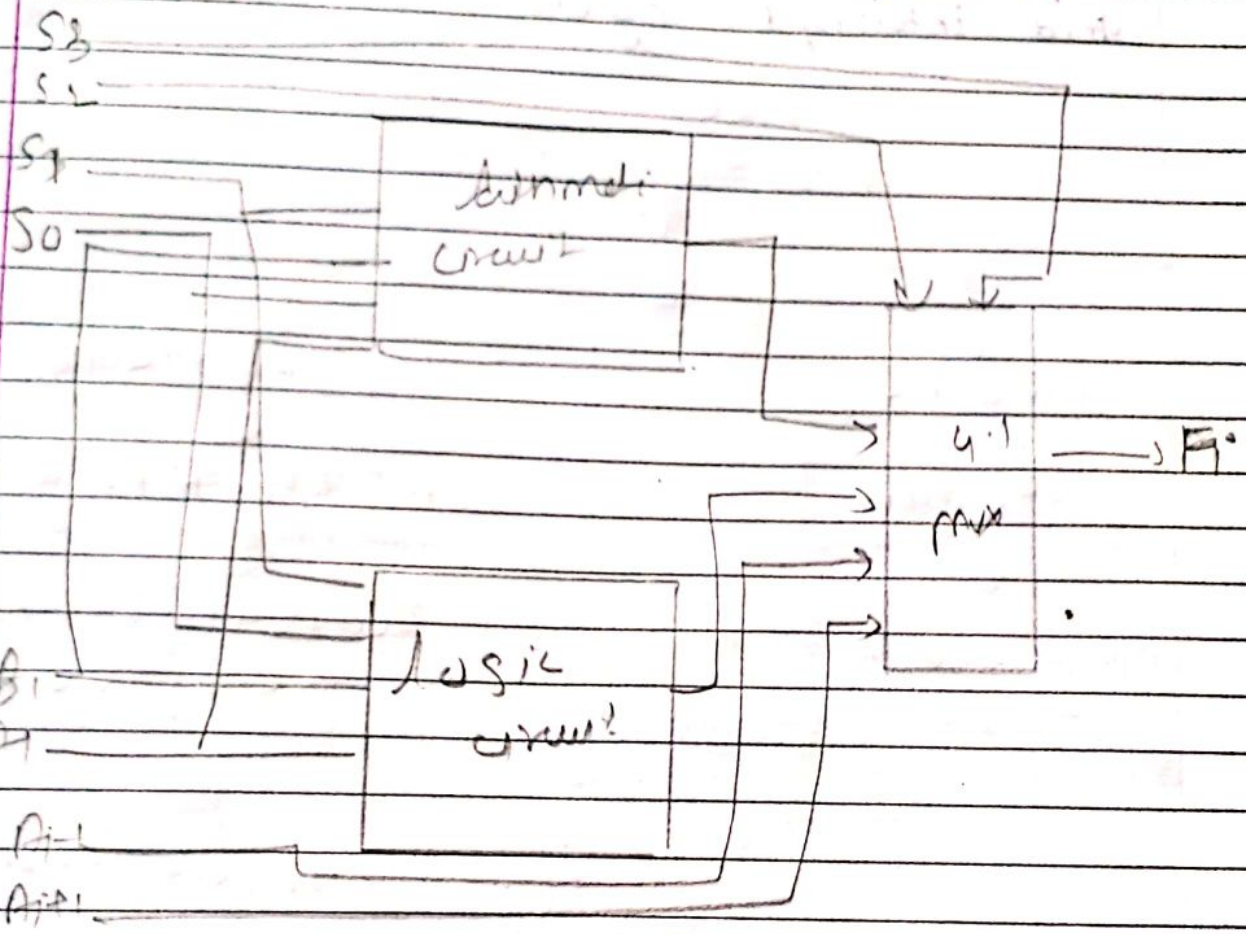
8.7 PC = 2 R_1 = 12 XR = 6 address = 410

addres mode	effective mode	Content of Ac
Direct add	410	12
immediate operand	-	410
indirect addres	12	-
Indexed Retat addres	416	
Relative addres	416	14
Register	-	2
Register indirect	2	-
Auto increment	411	13
Auto decrement	409	11

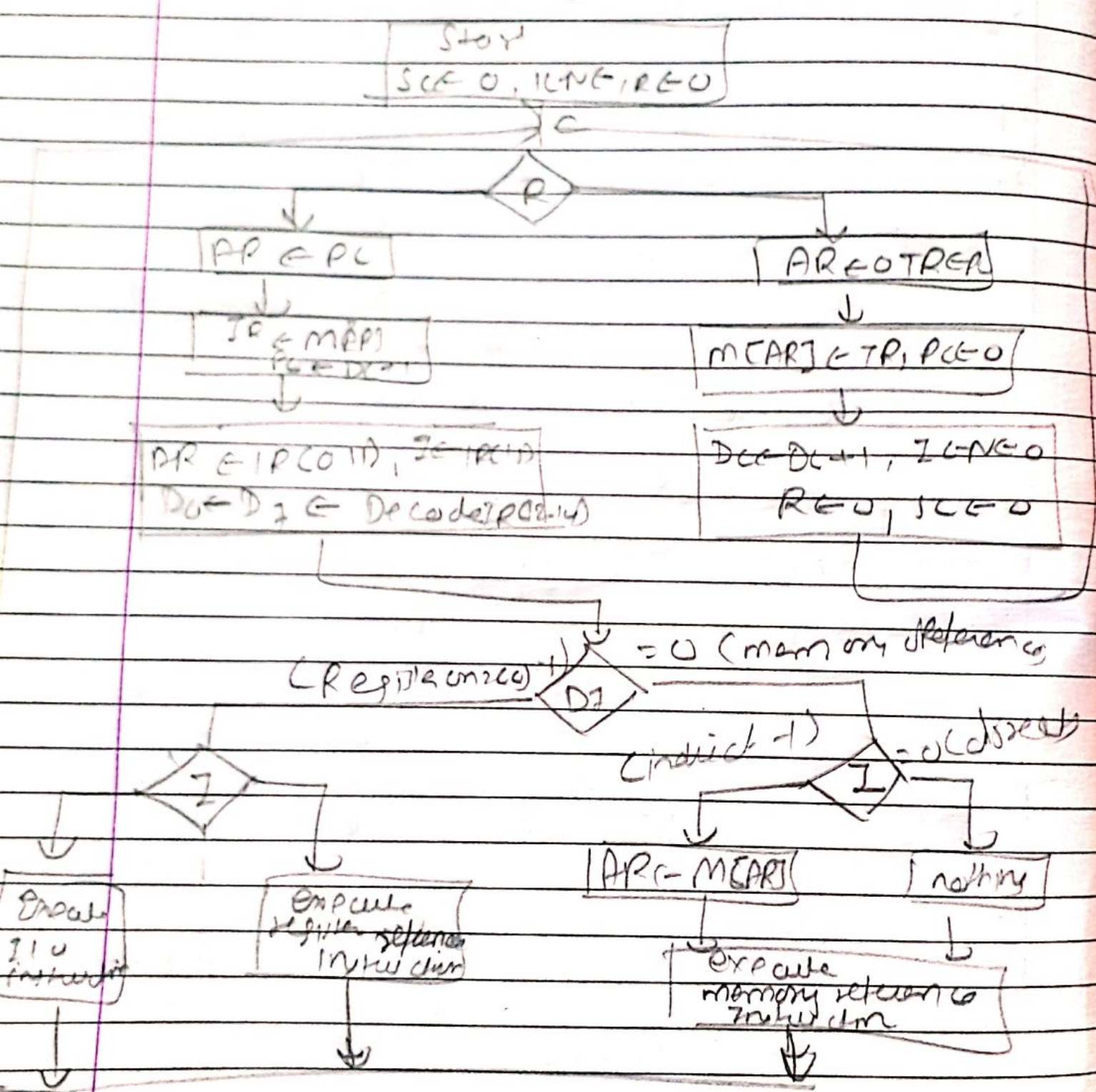
8.8 PC = 2 R_1 = 4 XR = 6 addres = 410

addres mode	effective addres	content of Ac
Direct add	410	12
immediate operand	-	410
indirect add	12	-
Indexed add	412	14
Relative add	416	-
Register	-	6
Register indirect	6	-
Auto inc	411	13
Auto dec	409	11

15 Draw circuit for one stage of arithmetic, logic and shift unit

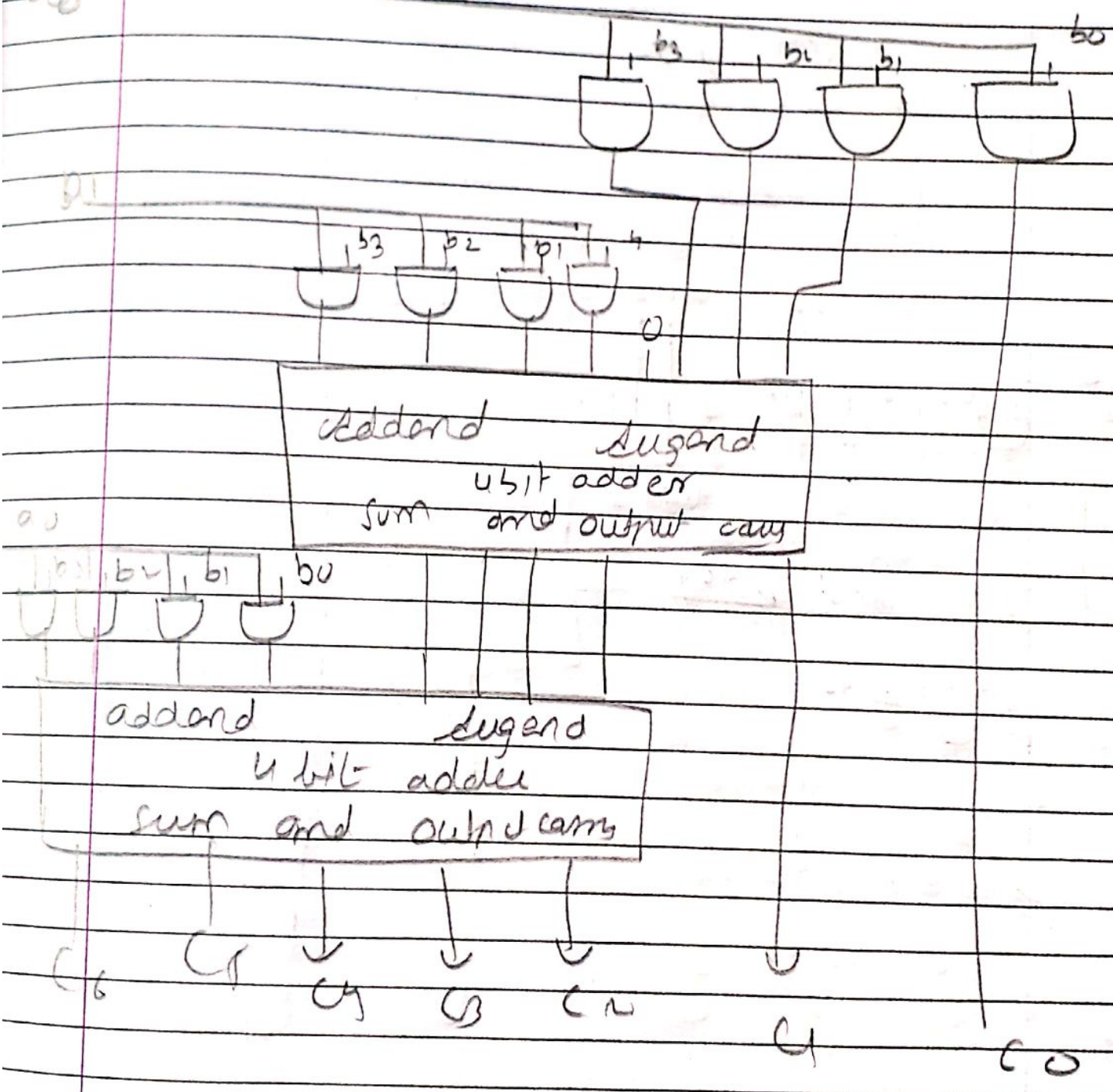


(18) Draw flow chart for computer operation combining of initial instruction and interrupt cycle

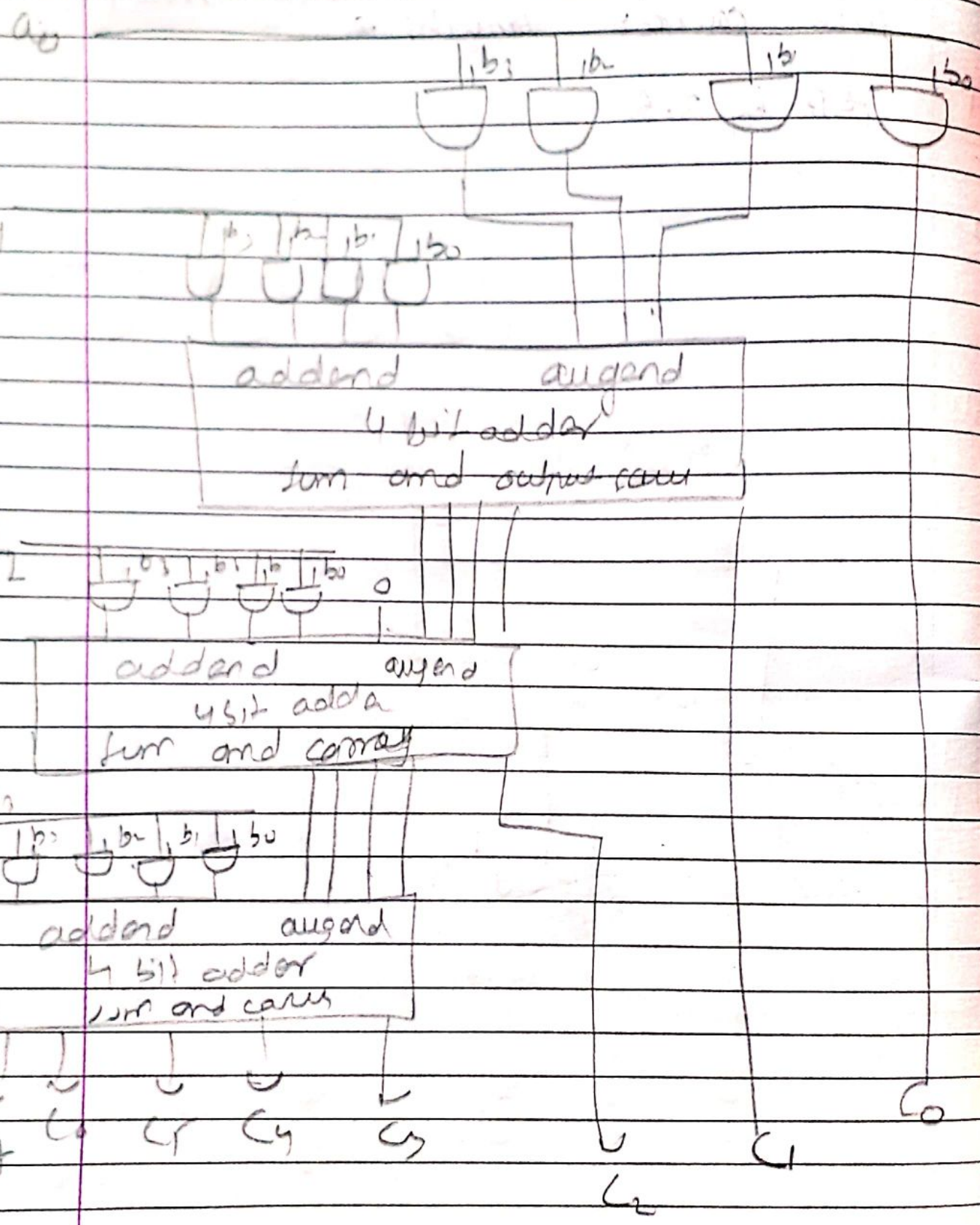


Q5/ Draw a circuit for following length of multiplicand and multiplier with carry save multiplier

Q5.1 4bit by 3-bit



25.2 4 bit by 4 bit



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Q.3 2 bit by 2-bit